UNIVERSITY OF CALIFORNIA
RIVERSIDE

Growth and Fabrication of Quasi-1D vdWs Nanowires for Microelectronic Applications

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Chemistry

by

Jing Jin

September 2024

Dissertation Committee:
Dr. Ludwig Bartels, Chairperson
Dr. Matthew Conley
Dr. Boniface Fokwa Tsinde

The Dissertation of Jing Jin is approved:

_____

_____

_____

Committee Chairperson

University of California, Riverside

ABSTRACT OF THE DISSERTATION

Growth and Fabrication of Quasi-1D vdWs Nanowires for Microelectronic Applications

by

Jing Jin

Doctor of Philosophy, Graduate Program in Chemistry
University of California, Riverside, September 2024
Dr. Matthew Conley, Chairperson

Advancing electronic devices requires not just new ideas but also the scalable and industry-friendly synthesis of innovative materials. As copper interconnects continue to shrink to the nanoscale, their resistivity rises sharply due to surface and grain boundary scattering, pushing the need for alternative solutions. Quasi-one-dimensional (quasi-1D) transition metal trichalcogenides, with their promising metallic properties, stand out as potential replacements. In our previous research, we successfully grew $TaSe_3$ nanowires with cross-sectional areas as small as 7 nm, and notably, their resistivity did not increase at these small scales. These nanowires also showed an electromigration activation energy twice that of copper and could handle current densities far beyond what copper can endure. These promising results highlight $TaSe_3$ as a viable candidate for downscaled electronic devices, a topic explored in detail in Chapter 1 as the driving motivation for this study.

Chapter 2 dives into the history of the materials relevant to this research, focusing on transition metal trichalcogenides and elemental tellurium. It explores their unique electronic properties, which make them attractive alternatives to conventional interconnect materials. Chapter 3 shifts to the experimental side, describing the techniques used in this study, with a particular emphasis on the chemical vapor deposition (CVD) process. This process was adapted to grow $ZrTe_3$ and Te nanowires, overcoming specific challenges related to the activation properties of selenium and tellurium. The fine-tuning of CVD parameters led to the successful deposition of high-quality nanowires on SiO_2 substrates.

Chapter 4 presents the results from these optimized processes, comparing the performance of $ZrTe_3$ and Te nanowires, and highlighting their impressive current-carrying capabilities and stability under varying conditions. These findings reinforce the potential of quasi-1D van der Waals materials for next-generation microelectronic applications, providing a promising route to address the scaling challenges that traditional interconnect materials like copper currently face.

Chapter 5 explores the impact of ion implantation on the electrical properties of CVD-grown Te nanowires, focusing on the enhancement of conductivity through ion beam-induced modifications. The chapter details the fabrication of multi-terminal devices and examines the effects of varying ion fluence on the current-voltage characteristics of Te nanowires. The findings demonstrate that ion implantation significantly improves the nanowires' electrical performance by introducing defects that enhance charge carrier mobility. These results underscore the potential of ion implantation as a precise doping

method to tailor the electronic properties of quasi-1D materials, paving the way for their integration into advanced semiconductor devices.

Chapter 6 investigates the patterned growth of $TaSe_3$ nanowires on lithographically prepared substrates, employing techniques such as UV optical photolithography and electron-beam lithography to direct the growth and alignment of nanowires. By designing specific patterns and creating artificial defects, the chapter showcases the controlled nucleation and guided growth of $TaSe_3$, achieving desired orientations and interconnections. The study highlights the scalability of these methods for microelectronic applications and sets the foundation for future work on device fabrication, comparing the electrical properties of pre-patterned nanowires to single nanowire counterparts. This approach aims to establish $TaSe_3$ nanowires as viable alternatives for on-chip interconnections, addressing the limitations of traditional materials.

ACKNOWLEDGEMENTS

First and foremost, I would like to express my deepest gratitude to my thesis advisor, Dr. Ludwig Bartels, for his invaluable guidance, support, and mentorship throughout my Ph.D. program at the University of California, Riverside. His expertise and encouragement have been fundamental to the completion of this work.

I also wish to extend my sincere appreciation to my committee members, Dr. Matthew Conley and Dr. Boniface Fokwa Tsinde. Your insightful feedback and unwavering support have been instrumental in guiding me through this journey.

A special thanks goes to Dr. Thomas A. Empante, whose mentorship in the field of chemical vapor deposition has greatly enriched my research experience. Your guidance has been a cornerstone of my development as a researcher.

I am profoundly grateful to the members of my lab, the department staff, and my family for their unwavering support and encouragement. The camaraderie, friendships, and shared experiences have been a cherished part of my time at UC Riverside, and I will always hold these memories close.

Lastly, I would like to acknowledge the financial support provided by the National Science Foundation (NSF) through the Division of Materials Research (DMR) program "Designing Materials to Revolutionize and Engineer our Future (DMREF)" under project DMR-1921958, entitled “Collaborative Research: Data Driven Discovery

of Synthesis Pathways and Distinguishing Electronic Phenomena of 1D van der Waals Bonded Solids." This support has been pivotal in enabling this research.

From the bottom of my heart, thank you to everyone who has been a part of this journey.

TABLE OF CONTENTS

LIST OF PUBLICATIONS

1. Jin J, Wurch M, Baraghani S, Coyle DJ, Empante TA, Kargar F, et al. Metallic transport in chemical vapor deposition ZrTe3 nanoribbons on a SiO2 wafer substrate. Cryst Growth Des. 2021;21(11):6537–42.

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

MOTIVATION

Advancements in semiconductor technology are driven by the relentless pursuit of miniaturization, where scaling down the dimensions of electronic components, including interconnects, is essential. Interconnects are critical elements that connect various components within integrated circuits, facilitating communication and power distribution across the chip (1). As device dimensions continue to shrink, traditional interconnect materials such as copper (Cu), cobalt (Co), and ruthenium (Ru) face significant challenges that limit their performance and reliability. These limitations arise from increased resistivity, electromigration, and integration difficulties at nanoscale dimensions, which impede the overall efficiency and reliability of modern electronic devices (2,3).

The quest for alternative interconnect materials is fueled by the need to address these challenges and to meet the ever-increasing demands of future technology nodes. Functional monolithic 3D integration of memory devices and aggressive downscaling in CMOS (Complementary Metal-Oxide-Semiconductor) technology require innovative solutions that go beyond the capabilities of conventional metals (2,4,5). This chapter explores the motivation behind seeking new interconnect materials, highlighting the fundamental limitations of traditional metals at nanoscale dimensions and introducing quasi-one-dimensional (1D) van der Waals (vdW) metals as promising candidates for next-generation interconnect applications (4–7).

1.1 The Need for New Interconnect Materials

The continual downscaling of electronic components has placed immense pressure on interconnect technologies to maintain low resistance, high current-carrying capacity, and reliability under increasingly demanding conditions. Conventional interconnect materials, particularly copper, have been the industry standard due to their excellent electrical conductivity and widespread compatibility with existing fabrication processes. However, as device dimensions shrink to the nanometer scale, the performance of copper interconnects deteriorates due to increased electron scattering at grain boundaries and surfaces, which leads to higher resistivity. This rise in resistivity not only compromises the speed and efficiency of integrated circuits but also increases power consumption, thermal load, and the risk of failure mechanisms such as electromigration.

Electromigration, the phenomenon where atoms within a conductor migrate due to momentum transfer from conducting electrons, becomes more severe as interconnect dimensions shrink and current densities rise. This can cause voids and hillocks within the interconnect material, leading to circuit failures that jeopardize the reliability of electronic devices (7–10). The semiconductor industry's roadmap, as outlined by the International Technology Roadmap for Semiconductors (ITRS), indicates that future technology nodes will demand interconnect materials that can sustain much higher current densities than what copper and other conventional metals can manage without compromising performance and reliability (11–14).

1.2 Challenges of Conventional Interconnect Materials

Copper has served as the primary interconnect material due to its high conductivity and relatively low cost. However, its effectiveness diminishes significantly at nanoscale dimensions. The primary issue with copper at these scales is the dramatic increase in resistivity due to surface scattering and grain boundary effects. As the dimensions of copper interconnects approach the electron mean free path (~40 nm), the resistivity can increase by several times its bulk value, severely impacting circuit performance (15,16). This increased resistivity leads to longer signal propagation delays, reduced bandwidth, and increased energy consumption, which are critical challenges for high-performance computing and mobile applications.

Beyond resistivity concerns, copper interconnects are also highly susceptible to electromigration, especially as device dimensions shrink and current densities increase. The formation of voids and other defects due to electromigration compromises the mechanical integrity of the interconnects, leading to increased failure rates and reduced overall device reliability. To address these issues, various approaches such as barrier layers, alloying, and new fabrication techniques have been explored, but these solutions often introduce additional complexity and do not fully resolve the underlying material limitations.

1.3 Limitations of Alternative Metals and Emerging Solutions

To mitigate the issues associated with copper, alternative metals such as cobalt and ruthenium have been considered for interconnect applications. Cobalt, while offering improved electromigration resistance, suffers from higher resistivity compared to copper, which becomes a significant drawback at smaller scales. Ruthenium presents a potential advantage in terms of direct contact applications and lower integration barriers, but its electrical performance at reduced dimensions still falls short of what is required for future technology nodes (17).

The limitations of these alternative metals underscore the need for fundamentally different materials that can deliver low resistivity, high current-carrying capacity, and superior reliability under aggressive scaling conditions. This has led to a growing interest in exploring low-dimensional materials, particularly quasi-one-dimensional (1D) van der Waals metals, which exhibit unique structural and electronic properties that could overcome the challenges faced by conventional interconnect materials.

1.4 Quasi-One-Dimensional van der Waals Metals: A Promising Alternative

Quasi-one-dimensional (1D) van der Waals metals are an emerging class of materials that hold significant promise for next-generation interconnects. These materials consist of atomic chains weakly bound into bundles by van der Waals forces, resulting in a structure with minimal grain boundaries and defects. This configuration offers a distinct advantage over traditional metals, as it significantly reduces electron scattering and maintains low resistivity even at the nanoscale. Additionally, the lack of grain boundaries in single-crystal 1D structures helps mitigate electromigration, enhancing the overall reliability of these interconnects under high current densities (18).

Among the most promising 1D vdW materials are transition metal trichalcogenides (TMTs), such as MX_3 compounds where M represents a transition metal (e.g., vanadium, niobium, or tantalum) and X is a chalcogen (e.g., sulfur, selenium, or tellurium). These materials feature conducting chains of transition metal atoms surrounded by chalcogen atoms, creating a quasi-1D conductive pathway that is well-shielded from external influences. For example, $TaSe_3$ is a trichalcogenide with a linear chain structure that provides a highly conductive core, protected by selenium atoms that minimize interaction with neighboring chains. This unique structure allows 1D vdW metals to maintain excellent electrical properties and mechanical stability, making them ideal candidates for ultra-scaled interconnect applications (19).

1.5 Need for Further Exploration of 1D Transition Metal Trichalcogenides

While significant progress has been made in understanding 2D materials like graphene and transition metal dichalcogenides, the exploration of 1D van der Waals metals, particularly transition metal trichalcogenides (TMTs), is still in its nascent stages. The full range of properties of these materials—including their electrical conductivity, thermal stability, mechanical strength, and integration potential with current semiconductor processes—requires further investigation. Addressing these knowledge gaps is essential to fully harness the potential of 1D TMTs for practical applications in microelectronics (20).

This dissertation aims to advance the understanding of 1D TMTs by investigating their synthesis, characterization, and integration into interconnect technologies. The research will focus on identifying suitable 1D vdW metals for use in next-generation interconnects, developing scalable fabrication methods, and evaluating their performance in comparison to traditional metals (21). By systematically exploring the properties of 1D TMTs, this work seeks to establish a foundation for their potential deployment in future microelectronic devices.

1.6 Objectives and Scope of the Dissertation

The primary objective of this dissertation is to explore the feasibility of using 1D van der Waals metals, specifically transition metal trichalcogenides, as advanced interconnect materials. The research will be conducted across several key areas:

1. **Material Selection and Characterization:** Identify and characterize suitable 1D vdW metals for interconnect applications, focusing on their structural, electrical, and thermal properties. Detailed analysis will be conducted to understand their resistivity behavior, current-carrying capacity, and performance under high-stress conditions.
2. **Fabrication Process Development:** Develop innovative fabrication techniques for incorporating 1D vdW metals into interconnect structures, including lines, vias, and contacts. This will involve optimizing deposition processes, patterning, and integration with existing semiconductor technologies to ensure compatibility and scalability.
3. **Performance Evaluation:** Conduct extensive testing to assess the performance of 1D vdW interconnects in comparison to conventional materials like copper, cobalt, and ruthenium. Key performance metrics will include resistivity, electromigration resistance, mechanical integrity, and overall reliability under operational conditions.

By addressing these objectives, this dissertation aims to contribute to the advancement of interconnect technology by identifying and validating new materials that can meet the rigorous demands of future semiconductor devices. The findings from this

research will not only enhance the understanding of 1D van der Waals metals but also provide a pathway for their practical implementation in next-generation interconnect solutions, potentially transforming the landscape of microelectronics.

CHAPTER 2

HISTORY OF RELEVANT MATERIALS

2.1 History of Transition Metal Trichalcogenides

Transition metal trichalcogenides (TMTs) are a class of low-dimensional materials that have garnered attention due to their distinctive structural and electrical properties. Unlike their more widely studied dichalcogenide counterparts, TMTs are synthetic materials that do not occur naturally. The synthesis of TMTs dates back to 1938 when Biltz first demonstrated the creation of TaS_3 using a method similar to Chemical Vapor Transport (CVT). This pioneering work laid the foundation for further synthesis and exploration of other TMTs, such as $TaSe_3$, which were found to possess unique rod-like structural configurations (22,23)

Interest in TMTs surged in the 1970s, largely driven by their potential in applications involving charge density waves (CDW) (24). These materials exhibited intriguing conductive properties, setting them apart from conventional metals and even other transition metal dichalcogenides. The rod-like chains within TMTs, composed of transition metal atoms surrounded by chalcogen atoms, are loosely bound together by van der Waals forces. This structural arrangement allows TMTs to maintain high conductivity and resistivity stability even as their dimensions are scaled down, making them attractive for microelectronic applications (22).

Despite the promising properties of TMTs, the traditional CVT method used for their synthesis presented significant challenges, particularly in scalability. The CVT process involves high-temperature reactions, often exceeding 900°C, within a sealed

quartz tube under vacuum conditions and in the presence of halogen gases like iodine or bromine. These processes can take from several days to over a week, making them resource-intensive and unsuitable for high-throughput manufacturing. Moreover, the bulk crystals produced through CVT require additional processing, such as exfoliation and transfer to substrates, for nanoscale applications, further complicating their use in industrial settings (12,25–27).

In response to these challenges, recent research has focused on developing more efficient and scalable synthesis methods. Modern approaches aim to reduce synthesis temperatures to below 400°C and shorten reaction times significantly, thereby aligning with the industry's demand for rapid, cost-effective production. Advances in chemical vapor deposition (CVD) and other techniques have been instrumental in addressing these needs. For example, novel CVD processes have enabled the growth of nanometer-scale TMT wire bundles with tightly packed atomic chains at lower temperatures and in shorter time frames than traditional methods (27).

The evolution of synthesis techniques has not only improved the practicality of producing TMTs but has also expanded their potential applications. TMTs, along with other low-dimensional materials like transition metal dichalcogenides (TMDs), graphene, and MXenes, have transformed the field of nanotechnology. These materials share a common feature—a van der Waals gap within their crystal structures—that facilitates a layer-like or tubular arrangement. This structural characteristic is crucial for enhancing their optoelectronic properties, minimizing electron scattering, and improving thermal and electrical conductivities (28–30).

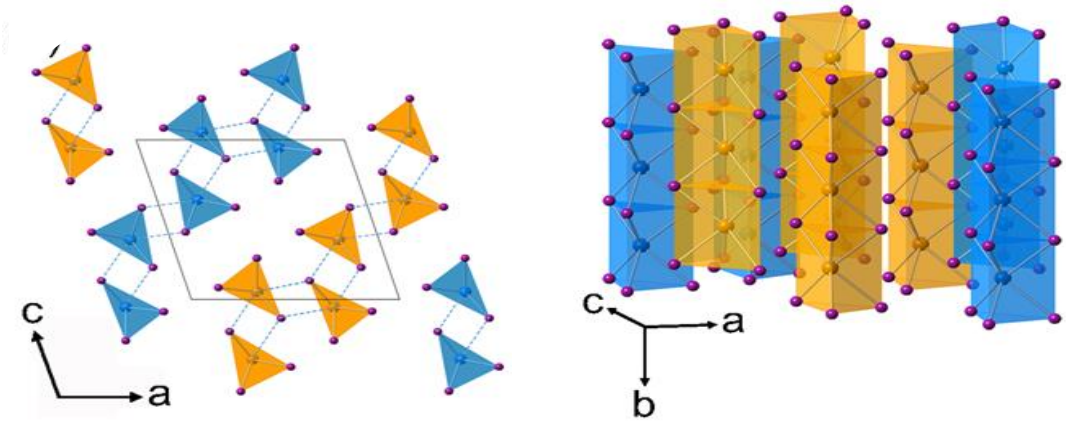

Figure 2.1: Ball and stick illustration to show the rod-like nature of transition metal trichalcogenide nanorods.

Recent advancements have particularly highlighted the potential of 1D TMTs like $TaSe_3$ and $ZrTe_3$, which have shown exceptional conductivity and resilience under high current densities. These properties make TMTs strong candidates for next-generation electronic devices, especially in applications requiring reliable performance at nanoscale dimensions. The successful development of CVD techniques, as detailed in Section 3.4, demonstrates that these materials can be synthesized efficiently to meet the stringent requirements of the semiconductor industry (28,31).

As the demand for more efficient and scalable electronic components continues to grow, the importance of materials like TMTs cannot be overstated. Their unique structural properties, combined with advancements in synthesis and integration techniques, position TMTs as pivotal materials for the future of microelectronics. Continued research and innovation will be essential to fully harness their capabilities, ensuring that TMTs can be effectively utilized in next-generation technologies (32–34).

2.1.1 Electrical Properties of Transition Metal Trichalcogenides

As electronic devices continue to shrink, the density of components on a chip increases, presenting significant challenges for interconnect materials. One major issue is the exponential rise in the resistivity of copper interconnects as their cross-sectional dimensions decrease. In contrast, TMTs maintain their bulk conductivity even at nanoscale, avoiding the adverse effects of surface and grain boundary scattering that typically plague traditional metals at sizes as small as 10 nm (35).

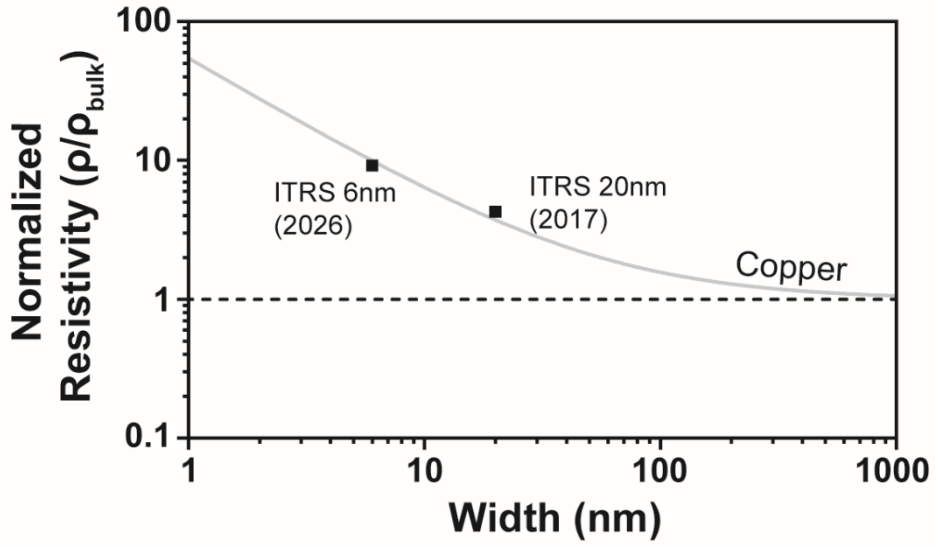

Figure 2.2: The change in the normalized resistivity of copper interconnects as the cross-section is scaled down to 1 nm. Reproduced from 2014 ITRS roadmap.

For example, previous studies from our group on $TaSe_3$ have shown that it exhibits remarkable resistance to electromigration—more than double that of copper—and can sustain current densities exceeding 10^8 A/cm² (31). These characteristics position TMTs as strong contenders to replace copper as interconnect materials, especially as copper approaches its scaling limits, a transition predicted by the 2023 ITRS roadmap.

We conducted extensive testing on numerous nanowires, using atomic force microscopy (AFM) and scanning electron microscopy (SEM) to assess their dimensions. As shown in Figure 2.3, the resistivity of 1D vdW $TaSe_3$ nanowires remains stable across various cross-sections, down to dimensions as small as 7 nm in both width and height. This stability is a stark contrast to copper, whose performance deteriorates significantly at the nanoscale, as illustrated by a reference line in Figure 2.3b based on prior studies by Steinhögl et al., which assumes specific scattering amplitudes.

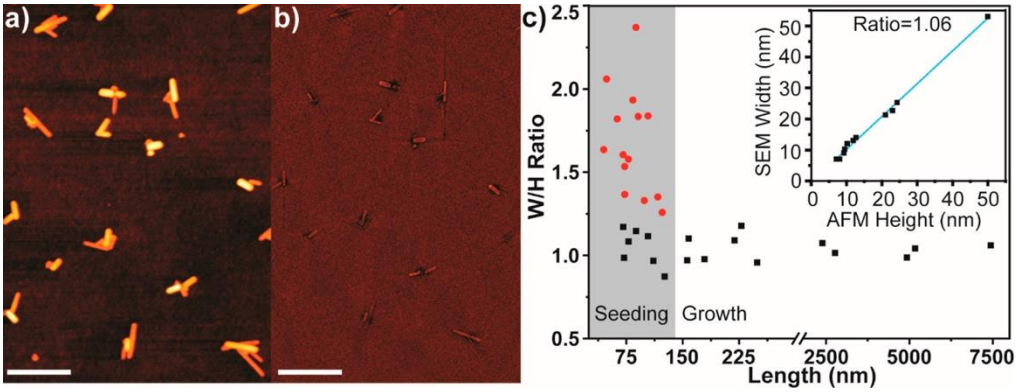

Figure 2.3 a,b) Atomic force microscopy (AFM) and scanning electron microscopy. Reproduced from Ref (31).

In examining bulk $TaSe_3$ and its configurations, including 2D bilayers, 2x2 and 2x1 wire bundles, and individual wires, we observed that confined wire geometries exhibit a higher density of states (DOS) at the Fermi level (EF) compared to the bulk material. This suggests that quantum confinement may enhance charge transport in $TaSe_3$ rather than impede it (31).

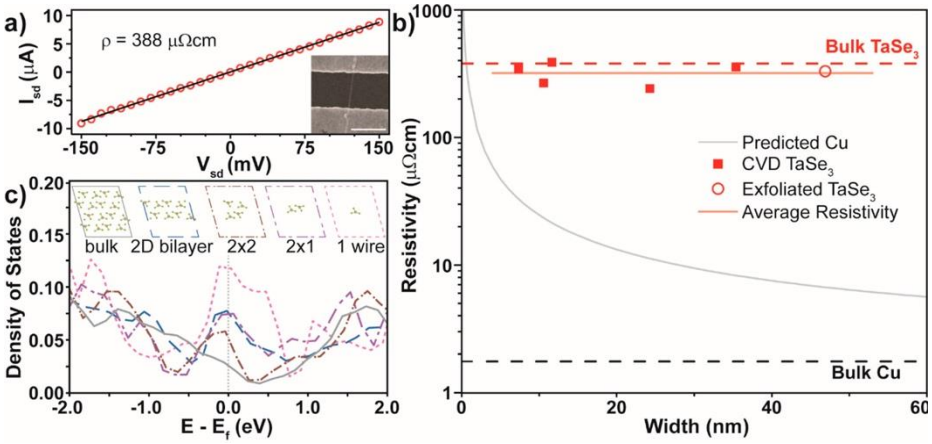

Figure 2.4: a) Source-Drain Current vs. Voltage (Isd vs. Vsd) for a 11.6 nm $TaSe_3$ nanowire; a linear dependence is observed in this two-probe measurement that corresponds to the current density shown on the y-axis and the resistivity highlighted. The inset shows an SEM image of a 1D vdW $TaSe_3$ nanowire bridging two electrodes (scalebar is 500 nm); b) resistivity of $TaSe_3$ nanowire bundles with width-to-height aspect ratios near unity (1.0-1.1) as a function of bundle width. For reference, we include bulk values for copper and $TaSe_3$ as dashed lines, as well as a prediction for the scaling of the copper resistivity with wire width based on Ref. 72 The smallest exfoliated nanowire of our prior studies is indicated as open dot. c) Calculated density of states (DOS) near the Fermi level (EF) for bulk $TaSe_3$, a 2D bilayer of wires, a 2×2 wire bundle, a 2×1 wire bundle and a single wire. The confined wire geometries have higher DOS at EF than the bulk material suggesting that quantum confinement does not adversely affect charge transport in $TaSe_3$. Reproduced from Ref (31).

We analyzed a typical current-voltage (I-V) characteristic for a $TaSe_3$ nanowire, measuring approximately 11.6 nm in both width and height, with electrodes spaced 500 nm apart. The linear I-V relationship indicated a resistivity of 388 μΩ·cm, along with corresponding current density details. Comparisons of the DOS from bulk $TaSe_3$ to smaller configurations, such as a bilayer and finite wire stacks, revealed an increase in DOS at the EF as the wire bundle was reduced, implying that certain geometries might achieve higher conductivity than the bulk material. However, this analysis does not consider fundamental stability limitations, such as those posed by the Mermin-Wagner theorem, necessitating further research to fully understand these findings. The smallest

wire bundle measured had dimensions of approximately 7 nm, consisting of about 100 wires in parallel, highlighting the need for additional studies to reconcile experimental results with computational models.

This exploration underscores the promising electronic properties of $TaSe_3$ nanowires, indicating their potential as next-generation conductive materials, provided that the challenges of stability and scalability are addressed in future research (29,30,35,36).

2.2 History of Tellurium Nanowires

Tellurium (Te), a member of the chalcogen family, was discovered by Franz-Joseph Müller von Reichenstein in 1782 (37,38). It is a relatively rare element in the Earth's crust, with an abundance of about 0.002 parts per million (ppm), similar to platinum, which highlights its exclusivity and value. Tellurium is known for its semiconductive properties, possessing a narrow bandgap of approximately 0.35 eV at room temperature. This makes it an attractive material for a variety of electronic applications, including thermoelectrics and optoelectronics, where its ability to efficiently conduct electricity and respond to changes in temperature and light are particularly valuable (39–41).

The unique electronic properties of tellurium stem from its distinct electron configuration, which includes six outer electrons in a $5s^2\ 5p^4$ arrangement. This configuration plays a critical role in its chemical reactivity and electrical characteristics, influencing its behavior in various devices. In recognition of its potential, the Materials Genome Initiative in 2011 identified tellurium as one of the two key materials for future technologies, emphasizing its importance alongside platinum (25). Tellurium's primary commercial uses include enhancing the machinability of steel and copper alloys, contributing to solar panels, and serving as a semiconductor material in various electronic devices (42).

Controlling the size and shape of tellurium nanocrystals is essential, as these parameters significantly impact the material's properties by altering the surface area and the ratio of surface atoms to bulk atoms. Over recent years, there has been considerable

progress in manipulating the morphology of Te nanocrystals, employing a range of synthesis methods. These methods include hydrothermal and solvothermal techniques, which utilize high pressure and temperature to achieve the desired nanostructures; photo-thermal processes, which use light to induce reactions; and sublimation-condensation, which relies on phase changes to form nanostructures. Each of these methods offers advantages in terms of controlling the crystallinity, purity, and dimensions of the resulting tellurium nanostructures (43).

Historically, research on tellurium was primarily focused on its role in organic and coordination chemistry, exploring its potential in developing novel compounds and materials. However, the exploration of Te nanostructures and their unique properties has become increasingly prominent. Tellurium's anisotropic crystal structure, characterized by helical chains of atoms covalently bonded into a hexagonal lattice, imparts both chirality and a strong tendency for one-dimensional growth. This structural anisotropy is a driving factor behind the formation of Te nanowires and other 1D nanostructures, which exhibit enhanced electrical and optical properties due to their reduced dimensionality and quantum confinement effects (44).

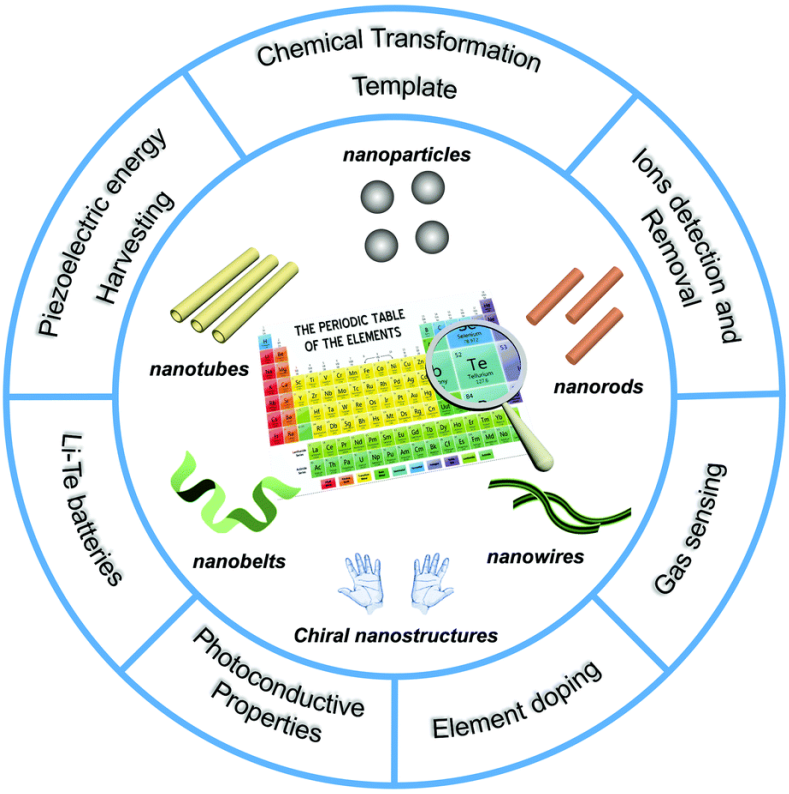

Figure 2.5: Schematic illustration of the morphology control of Te nanostructures and their wide application potentials. Reproduced from Ref (44).

In recent decades, the study of one-dimensional (1D) semiconductor nanostructures, such as nanowires, nanobelts, and nanotubes, has grown rapidly due to their potential in a wide range of applications, including nanoelectronics, sensors, and energy conversion devices. Tellurium's crystal structure, which consists of helical chains aligned along the c-axis, naturally favors 1D growth, making it particularly suitable for forming nanowires (45). Various tellurium-based 1D architectures, including nanowires and nanotubes, have been synthesized using diverse techniques, such as microwave-assisted synthesis, which provides rapid heating and uniform particle size; solvothermal and hydrothermal methods, which offer high control over crystal quality; thermal

evaporation, which is effective for producing high-purity nanostructures; the use of porous templates, which direct the growth of nanowires with specific diameters and lengths; and chemical vapor deposition (CVD), which allows for the scalable production of high-quality nanowires (46).

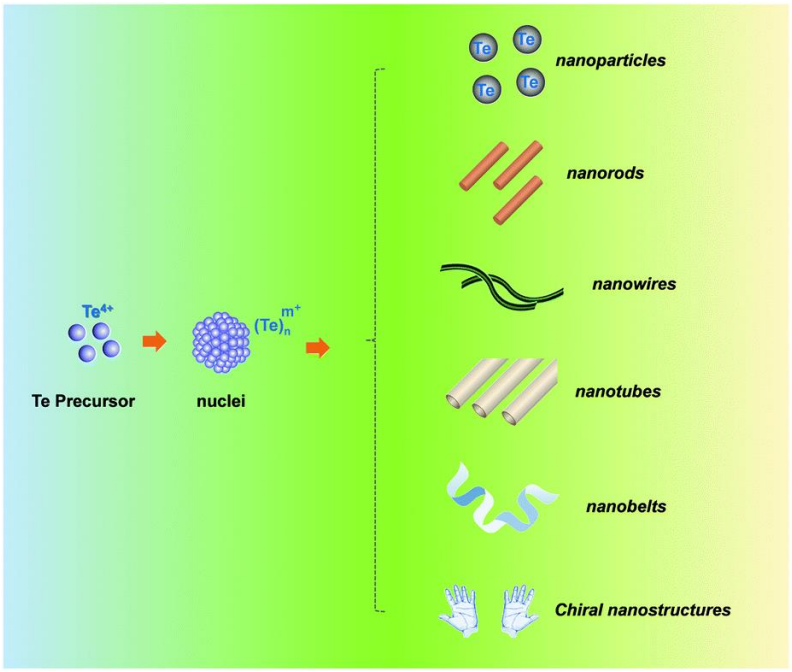

Figure 2.6: A schematic illustration of the reaction pathways that lead to Te nanostructures with different shapes. Reproduced from Ref (44).

Among these methods, hydrothermal recrystallization using tellurium powder has proven particularly effective for selectively producing single-crystalline tellurium nanowires and nanotubes. This technique leverages the anisotropic growth tendencies of tellurium, resulting in well-defined nanostructures that are ideal for detailed studies and potential applications. The ability to synthesize tellurium nanostructures with precise control over their dimensions and properties has opened new avenues for their use in advanced technologies, including thermoelectric devices, where their high Seebeck

coefficient and low thermal conductivity are advantageous for efficient energy conversion.

The historical development and ongoing research into tellurium nanostructures underscore their potential as key materials in the future of microelectronics and nanotechnology. As the demand for miniaturized and high-performance electronic components continues to grow, the unique properties of tellurium nanowires, combined with advances in synthesis techniques, position them as promising candidates for a wide range of innovative applications. Continued exploration and refinement of these materials will be essential to fully harness their capabilities and integrate them into practical devices (47).

2.2.1 Electrical Properties of Tellurium

Tellurium (Te) is a narrow-bandgap semiconductor with a distinctive helical chain crystal structure, where the chains are held together by weak van der Waals interactions. This one-dimensional (1D) structure facilitates efficient charge transport along the chains, making Te particularly suitable for forming nanowires and nanotubes. The helical arrangement of Te atoms allows for directional conductivity with minimal scattering, which is a key advantage for electronic applications requiring high conductivity and stability at reduced dimensions.

Due to its 1D van der Waals structure, Te exhibits lower resistivity at the nanoscale compared to its bulk form, where the resistivity of bulk Te crystals is approximately 90 μΩ·m. In nanostructured Te, the confined pathways for charge carriers and reduced scattering result in improved electrical performance, making Te nanowires and nanotubes promising candidates for next-generation electronic devices. This reduction in resistivity at smaller scales enhances the efficiency of Te nanostructures, which can maintain stable electrical properties even as their dimensions decrease significantly (48).

Te nanostructures, such as nanowires, predominantly exhibit p-type semiconducting behavior, which is advantageous for applications in thermoelectric devices, sensors, and field-effect transistors. The p-type nature of Te is due to its ability to accept electrons easily, facilitating hole conduction. This characteristic is further enhanced in nanostructured forms due to the increased surface-to-volume ratio, which influences charge transport properties. Additionally, the conductivity of Te nanowires can

be tuned through doping and structural modifications, allowing for customization of their electrical performance for specific technological applications.

Overall, tellurium's unique 1D van der Waals structure and its resulting electrical properties position it as a valuable material in the development of advanced microelectronic components (30,41,49,50). Its ability to achieve lower resistivity at nanoscale dimensions, combined with its inherent semiconducting characteristics, underscores Te's potential for integration into future electronic devices. Continued research into optimizing Te nanostructures, refining synthesis techniques, and enhancing material stability will be essential to fully leverage its capabilities in practical applications.

CHAPTER 3

EXPERIMENTAL TECHNIQUES

3.1 Chemical Vapor Deposition

Chemical Vapor Deposition (CVD) is a widely used technique in materials engineering, valued for its ability to produce uniform, high-purity coatings and structures essential for various advanced applications. Unlike chemical vapor transport, which operates in more confined systems, CVD utilizes an open-system configuration that offers greater flexibility and precise control over the deposition process. This method involves flowing inert gases, such as argon or nitrogen, through a quartz tube to transport reactant gases while maintaining a controlled atmosphere. A water-sealed bubbler system serves as a one-way valve, ensuring the stability of the process environment (51).

The precise temperature control available in CVD, ranging from ambient conditions up to 1200°C, allows for the synthesis of materials with tailored properties to meet specific requirements (52). Flowmeters are used to regulate gas flow rates, enabling fine adjustments to deposition rates and the thickness of the deposited layers. This level of control is crucial for producing materials with consistent quality and performance, making CVD a versatile tool in material fabrication.

CVD's versatility extends to its compatibility with a wide range of reagents, including solids, liquids, and gases, as well as diverse substrates, whether amorphous or crystalline. This broad compatibility is not limited by lattice matching or chemical compatibility, allowing CVD to be used for complex multilayer structures and coatings

on substrates with irregular surfaces. Such flexibility makes CVD an invaluable technique for applications that require precision and adaptability in material synthesis.

In the semiconductor industry, CVD is extensively employed for fabricating thin films and nanostructures. It is essential for producing uniform, defect-free layers of materials like silicon, germanium, and gallium arsenide, which are fundamental to the construction of integrated circuits and photovoltaic cells. Additionally, CVD plays a crucial role in the deposition of advanced materials, such as graphene and carbon nanotubes, which are pivotal in the development of next-generation electronic and energy devices (53). These materials offer improvements in speed, efficiency, and miniaturization, driving innovation in the field.

Beyond electronics, CVD has significant applications in other industries. In optics, CVD is used to deposit transparent conductive oxides and anti-reflective coatings, enhancing the performance of optical devices. In the aerospace industry, CVD contributes to the development of thermal barrier coatings that protect engine components from extreme heat and corrosion, improving the durability and efficiency of these systems.

Looking ahead, the adaptability of CVD is expected to play a crucial role in emerging fields such as additive manufacturing and 3D printing. In these areas, CVD could enable the precise deposition of metals and ceramics, supporting advanced manufacturing techniques. Furthermore, ongoing advancements in CVD processes are focused on improving environmental sustainability, including the development of lower-temperature processes and the use of less hazardous chemical precursors.

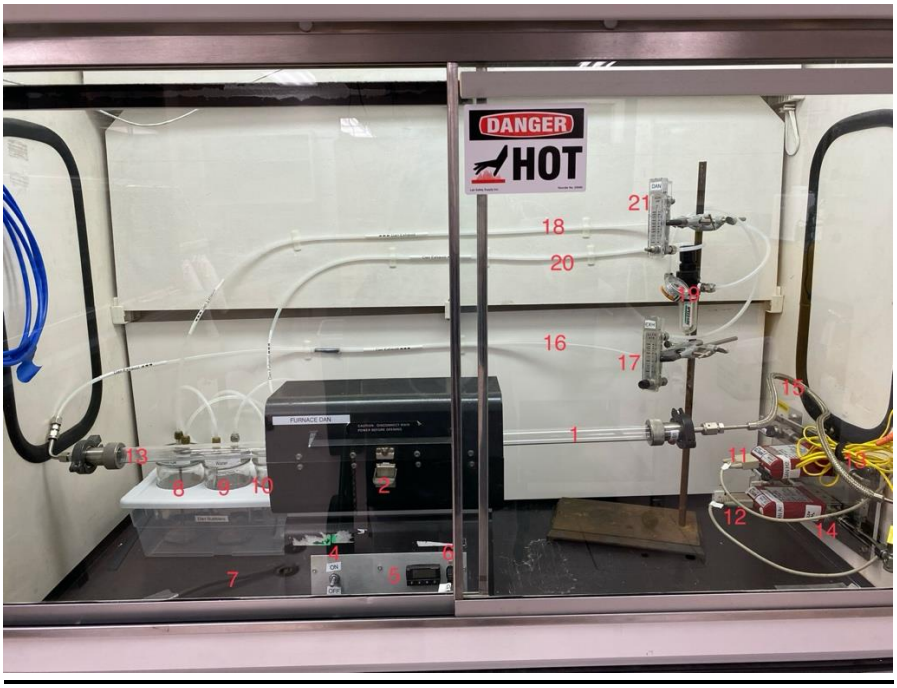

Figure 3.1: Image of a chemical vapor deposition system consisting of 1). Inlet Gas Flow, 2). Furnace Latch, 3). Outlet Gas Flow, 4). Power Switch, 5), Furnace Controller, 6). USB Connection, 7). Power Cord, 8). Bubbler System (Silicon Oil), 9). Bubbler System (H_2O), 10). Bubbler System (Silicon Oil), 11). H_2 mass flow controller, 12). Ar mass flow controller, 13). H_2 line, 14). Ar line, 15). H_2 + Ar mixed gas line, 16). Furnace Exhaust Tubing to Test Flow Meter , 17). Bubbler Test Flow Meter (for bubblers testing only), 18). Furnace Exhaust Tubing to Bubblers, 19), Air Filter. 20). Furnace Exhaust Tubing to Gas Filter, 21). Furnace Dan Exhaust Flow Meter

In conclusion, Chemical Vapor Deposition is a cornerstone technology in materials science, providing unmatched control, versatility, and capability in the synthesis of advanced materials. Its continued evolution is poised to drive significant progress across multiple industries, facilitating innovative applications that leverage its unique strengths.

3.2 Electronic Transport Measurements

The electronic transport properties of materials are typically evaluated using 2-terminal, 3-terminal, and 4-terminal device configurations. In a basic 2-terminal setup, two electrodes are connected to the material: one acts as the source and the other as the drain. A common instrument used for this configuration is Keithley source meters, which apply a voltage bias to the source electrode, inducing a current through the material to measure its resistance. However, a limitation of 2-terminal measurements is that they include the contact resistance at both the source and drain electrodes, which can obscure the true resistance of the material (32,54,55).

To mitigate the effect of contact resistance, 3-terminal measurements are employed. This approach introduces a third electrode, which can be placed between the source and drain or externally. The third electrode is connected to an electrometer with high impedance (approximately 10^{11} Ω) to measure the voltage drop across the contact point. By applying Ohm's law, the contact resistance can be accurately determined, providing a clearer understanding of the interactions at the electrode interfaces and enhancing the accuracy of the overall measurement (56).

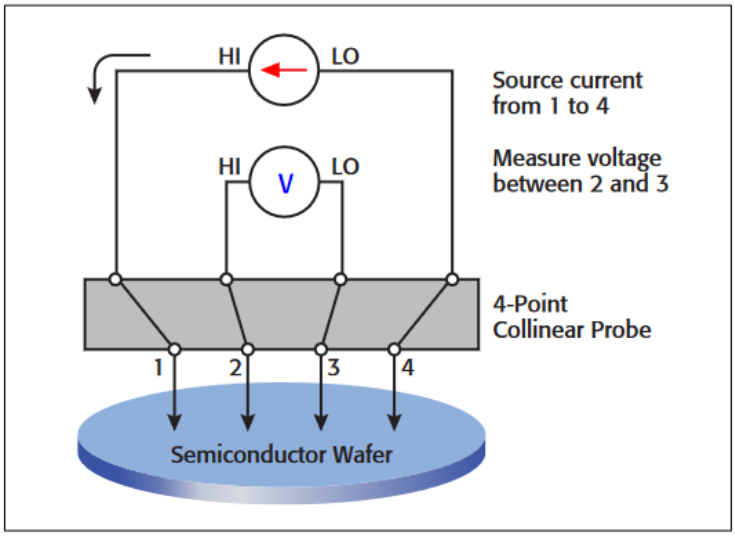

Figure 3.2: Four-point probe resistivity test circuit. Reproduced from https://www.tek.com. [Internet]

The 4-terminal measurement technique further improves accuracy by incorporating four electrodes. In this configuration, two electrodes are used to apply the current (source and drain), while the other two are placed between the current-carrying electrodes and are connected to a voltmeter. When a voltage bias is applied, the electrometers measure the voltage at these intermediary electrodes. The voltage difference is then used to calculate the resistance of the material, excluding any contact resistance. This technique provides the most precise representation of the material's inherent resistance, as it isolates the measurement from external influences such as contact resistance (57).

Expanding further, the 4-terminal measurement technique is particularly advantageous for materials where precision is critical, such as semiconductors and nanostructured materials. By eliminating the effects of contact resistance, this method allows researchers to obtain a more accurate assessment of the material's intrinsic

electrical properties, which is essential for the development of advanced electronic devices. This approach is especially valuable in research areas where electrical properties, such as conductivity and resistivity, are influenced by nanoscale effects. The 4-terminal configuration enables detailed mapping of resistance changes across the material, providing insights that are crucial for applications like integrated circuits and sensor technology.

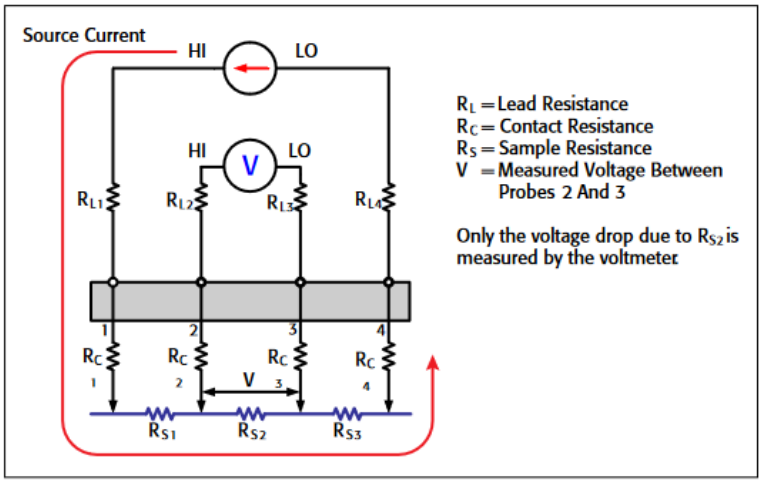

Figure 3.3: Test setup showing circuit resistances. Reproduced from https://www.tek.com. [Internet]

Overall, the 4-terminal measurement technique is a sophisticated tool in materials science, offering the precision needed to advance the functionality and efficiency of electronic materials. This method not only enhances the reliability of the data collected but also contributes significantly to the fundamental understanding of material behavior under various electrical conditions. By providing a more accurate evaluation of electronic transport properties, the 4-terminal measurement technique plays a critical role in driving innovations in electronic device design and performance (10,47).

CHAPTER 4

$ZrTe_3$

The following chapter contains excerpts from "Jin, J.; Wurch, M.; Baraghani, S.; Coyle, D.; Empante, T.; Kargar, F.; Balandin, A.; Bartels, L. Metallic Transport in Chemical Vapor Deposition $ZrTe_3$ Nanoribbons on a SiO_2 Wafer Substrate. Crystal Growth & Design. 2021 21 (11), 6537-6542."

4.1 Abstract

We report on the chemical vapor deposition (CVD) growth of quasi-one-dimensional zirconium tritelluride ($ZrTe_3$) at temperatures below 600 °C and process times under an hour, which results in a material on a SiO_2/Si wafer substrate that offers electrical conductivity comparable to the bulk. This study combines tailored CVD processing using a tube-in-a-tube technique with characterization by optical microscopy, Raman spectroscopy, and scanning electron microscopy. Transmission electron microscopy validates the composition and offers atomic contrast. Electrical transport measurements employ an yttrium-gold stack to achieve good adhesion and low contact resistance. A positive temperature coefficient is observed, as expected for a metallic material. The obtained results are important for the proposed applications of quasi-one-dimensional van der Waals materials in the next-generation electronic devices.

4.2 Introduction

The continued progress in miniaturization of microelectronic devices provides materials and fabrication challenges pertaining not only to the active semiconducting region of the transistors, but also to the electrical leads, interconnects, and wiring systems. Finer wires have a higher surface to volume ratio, resulting in greater resistance originating from the surface and grain–boundary scattering of electrons. Copper has been the material of choice for the past 2 decades for interconnects in high-end semiconductor devices. Because of its long mean free path (MFP) for electrons, which is ~40 nm at room temperature, (58,59) copper is susceptible to electron surface scattering and exhibits substantially higher resistivity at current sub-20 nm interconnect cross sections. In contrast, the resistivity of materials that do not rely on long MFP for excellent conductivity, such as cobalt and ruthenium, is less affected by surface scattering; recent work at Intel and elsewhere transitioned away from interconnects made from copper for that reason (60,61). Alternate contact materials such as cobalt (62) and ruthenium (63–65) trade inferior bulk conductivity against reduced surface scattering. They also offer new process challenges; for instance, because of their refractory nature, annealing to mitigate the effect of grain boundaries is more difficult. Metallic one-dimensional (1D) or quasi-1D materials may play an important role in future nanoscale devices because their van der Waals (vdW) gap between adjacent wires in a bundle natively shields electrical transport along their main axis from surface scattering, thus avoiding the problem inherent to elemental metals and their alloys. Indeed, in a previous study, (31) we have shown that $TaSe_3$ wire conductivity is not affected by surface scattering down to the

minimal wire cross section we could produce (7 nm). However, 1D materials will only be of importance in technological utility if they (a) have a sufficiently low native resistivity and (b) can be deposited on an oxide surface using chemical vapor deposition (CVD) or related techniques at both low enough temperatures and short enough process times.

The 1D and quasi-1D vdW materials have long been studied for the charge density waves they support (11,28,66–68). Recently, increased interest has been attracted by them, and a multitude of $MX_{3...5}$ (M: transition metal such as Ta (31), Zr (6,7,11,69–73) and Nb (50,67) X chalcogen: S, Se, and Te) have been synthesized for electronic, (10,19,31,39) magnetic, superconducting, and optical characterization. In this study, we build on our prior work on $TaSe_3$ CVD (31) land develop a tailored technique to provide access to $ZrTe_3$ on SiO_2 substrates—simple transference of the growth technique developed for $TaSe_3$ does not lead to $ZrTe_3$ growth. Bulk $ZrTe_3$ has a better conductivity (74,75) than $TaSe_3$; this was also found in a number of studies on exfoliated microscopic flakes (76). While selenium and tellurium share many chemical properties as both chalcogens and metalloids, their ease of activation is quite different, with tellurium typically requiring higher temperatures or more time. Conventionally, $ZrTe_3$ crystals have been grown using chemical vapor transport techniques, in which zirconium and tellurium precursors are allowed to react over days or weeks in the presence of a transport agent (e.g., iodine) to form large crystallites of the desired material. Derived from that approach, Yu et al. (69) showed in an impressive study a CVD technique, which provided high-quality samples by requiring a process temperature in excess of 600 °C and hold times on the order of an hour. Here, we focused on reducing hold time and temperature so

as to better comply to thermal budget requirements; in particular, we show how $ZrTe_3$ crystallites can be grown in situ on SiO_2 at process temperature well below 600 °C and process times well below 1 h. The resultant nano- and micron-scale material is highly crystalline and feature metallic conductivity (e.g., positive temperature coefficient of resistivity and bulk-like high electric conductivity).

A key challenge in the development of CVD growth methods of 1D nanomaterials is the identification and characterization of the product material. This is particularly the case when working with tellurium because elemental tellurium also forms 1D structures (77–81). To guide future practitioners, we also characterized the tellurium wire byproducts that form when the process conditions are slightly off. The presence of common Raman modes of tellurium wires overlapping with that of $ZrTe_3$ provides characterization challenges that are best resolved by rotating the polarization axis of the incoming laser relative to the wire axis. This study offers a combination of tailored CVD process conditions and thorough characterization of the resultant material including polarization-dependent Raman spectroscopy and temperature-dependent transport measurements.

4.3 Results

Figure 4.1a provides a schematic representation of the growth setup using a clamshell-type tube furnace with a 2″ process tube. We use elemental tellurium powder (99.8%, Sigma-Aldrich) and zirconium tetrachloride (99.9%, Sigma-Aldrich) as tellurium and zircon precursors, respectively. To increase the chemical potential of tellurium at the CVD growth location, we place a 0.5-inch test tube (with closed end) inside the 2-inch process tube. The open end of the test tube (facing upstream) is constricted with ceramic fiber wool. Inside the test tube, we place a 1 mL alumina boat (Coors) filled with a mixture of both precursors homogenized by stirring in chlorobenzene prior to growth. The wafer substrate is placed directly atop the boat.

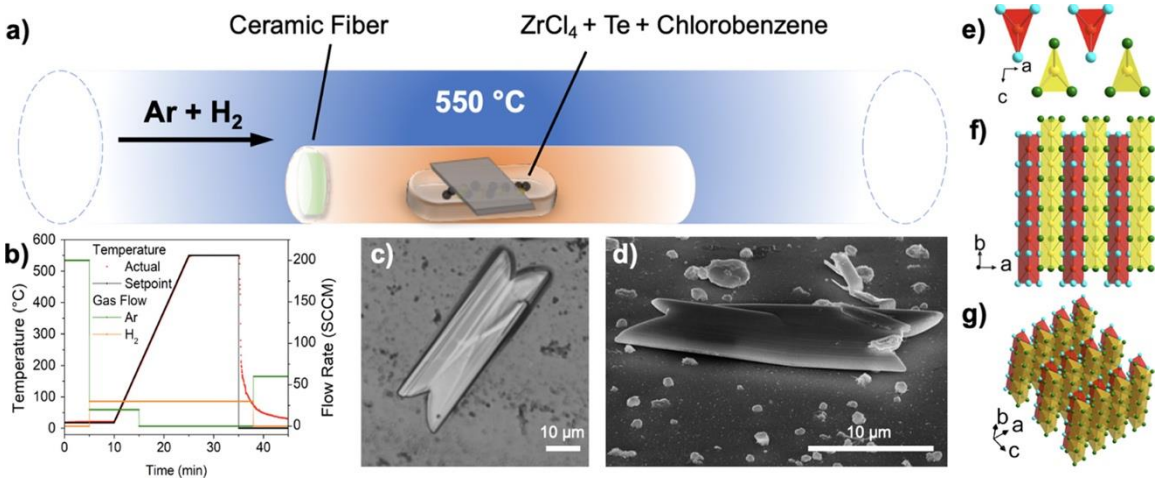

Figure 4.1: (a) Schematic representation of the CVD growth setup consisting of a process tube housing a test tube stoppered by a bale of porous ceramic fiber. Inside the test tube growth, precursors are placed inside an alumina boat and the growth substrate on top. (b) Temperature and gas profile during the growth. The hold time is 10 min. (c) Optical image of a $ZrTe_3$ crystallite grown on SiO_2/Si. (d) Scanning electron microscopy image of a $ZrTe_3$ crystallite obtained at 60-degree tilt of the gun. (e–g) Crystallographic structure of $ZrTe_3$ plotted from different angles.

Figure 4.1b shows the temperature and process gas transients as applied here. Argon is used for purging, and the CVD proceeds in a hydrogen atmosphere. Hydrogen serves two purposes: providing a reducing atmosphere to prevent oxidation of the species and, importantly, much improved thermal conductivity compared to argon or nitrogen, resulting in more rapid thermal transients at the sample location. These are also visible from the good compliance of the temperature trace to the setpoint temperature.

Following growth, so as to shield the samples from oxygen in air, we covered them immediately in a ~500 nm thick layer of polymethyl methacrylate (PMMA) resist (MicroChem); care was taken to reduce the oxygen dissolved in the PMMA by keeping it consistently in a nitrogen-filled glovebox. All spectroscopic studies and optical imaging were performed through that PMMA layer; this layer was also used for subsequent lithographic processing.

Figure 4.1c shows an optical imge of a representative $ZrTe_3$ crystallite several tens of microns long. $ZrTe_3$ crystallites typically appear as two trapezoids attached at their shorter sides. Their surface is flat, and their thickness much smaller than their width (i.e., about 1/10 depending on the crystallite). These crystallites exhibit a metallic sheen and are very reflective in optical images, which amplifies the contrast of small steps/facets on their surface under proper illumination.

Scanning electron microscopy (SEM) provides higher resolution imagery of the $ZrTe_3$ crystallites grown on the oxide substrate. Figure 4.1d shows a tilted (60^o) view of one of the larger $ZrTe_3$ crystallites. Practically, all of them grow in this double trapezoid shape, which we tentatively attribute to a dislocation at the center of the crystallite. Yu et

al. observed similar shapes. As a result, only one side of the islands lies flush on the substrate, whereas the other is lifted up. Depending on the hold duration during growth, we observe these crystallites to grow tens of micrometers in the long axis; shorter crystallites are obtained at shorter growth duration.

The crystallographic structure of monoclinic $ZrTe_3$ is depicted in Figure 4.1e–g. Two of the $ZrTe_3$ formula units comprise a unit cell of the crystal. The vertical rods in panel f are the direction of high conductivity; these colored rods represent the quasi-1D wires of this material. They assemble in sheets, which in turn stack to make up the bulk. The geometric data underlying this plot were obtained from the Materials Project database.

Figure 4.2 shows transmission electron microscopy (TEM) data obtained on a $ZrTe_3$ crystallite after transferring it onto a lacey carbon-coated 300 mesh copper TEM grid by first scraping the crystallites with a tungsten needle off the substrate and then catching the resultant particles from distilled water. Panels (a–c) show elemental maps obtained by energy-dispersive X-ray spectroscopy that confirm the crystallites to be homogeneous in composition and to consist of zirconium and tellurium. Quantitative evaluation of the emitted X-rays is consistent with the 1:3 composition of the material.

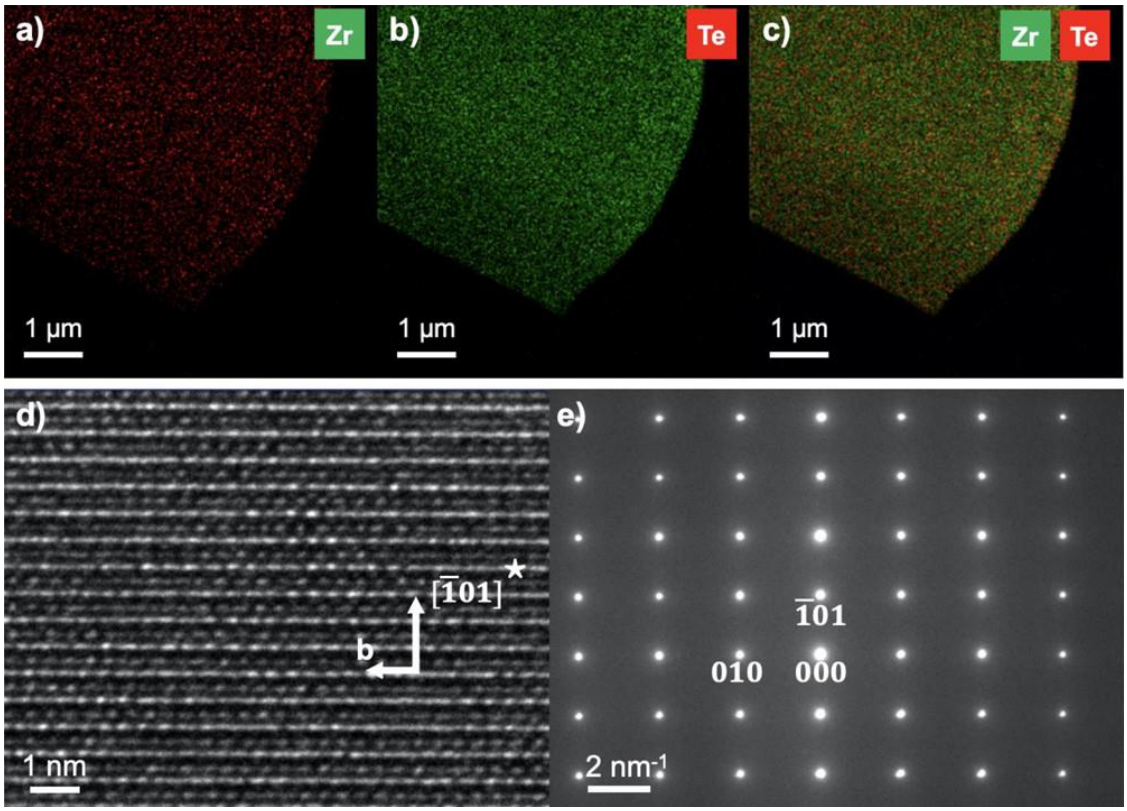

Figure 4.2: (a–c) Energy-dispersive X-ray spectroscopy elemental map images of the spatial distribution of Zr K and Te L signals. The uniform signal level confirms that the observed crystallite has homogeneous stoichiometric composition; (d) High-resolution transmission electron microscopy image showing the ordered and homogeneous composition of the $ZrTe_3$ crystallites; and (e) corresponding selected area electron diffraction pattern taken with the electron beam parallel to the [101] zone axis.

High-resolution TEM imaging (Figure 4.2d) further confirms the homogeneous single crystal nature of the particles and the absence of any significant precipitates or extended structural defects. An indexed selected area electron diffraction pattern (Figure 4.2e) taken with the electron beam parallel to the [101] zone axis of the $ZrTe_3$ crystallite shown in Figure 4.2d confirms the single crystal nature of the studied particles. The forbidden 010 reflection appears from dynamic multiple scattering in the relatively thick

crystal along the electron beam direction, which is consistent with the monoclinic P21/m space group symmetry of $ZrTe_3$.

Further characterization of the material was carried out using Raman spectroscopy (Horiba Labram HR800) with 532 nm laser wavelength excitation. The power of the incident light on the sample was 0.8 mW. We readily noticed great variation of the spectra depending on the orientation of the plane of polarization with respect to the crystallographic axis of the islands. Similar observations were made also by Zwick et al. (25) Figure 4.3a shows two spectra with the polarization of the excitation laser parallel and perpendicular to the long axis of the 1D wire. The A_g(c), A_g(d), A_g(f), and A_g(h) modes are found at 84, 113, 138, and 214 cm^{-1}, respectively. The labeling of the modes in Figure 4.3a follows the work by Hu et al. (11) Panel 3b shows a polar plot of the strongest modes of the Raman spectrum. The angular dependence of the A_g(c), A_g(d), and A_g(f) modes is well represented by a $\sin^2$ fit. The Ag(h) mode was fitted by a superposition of two orthogonal $\sin^2$ dependences. The numerical fit suggests a slight ($\sim$1 cm^{-1}) shift between the components at different orientation, which may be attributed to an A_g band. Hu et al. (11) also observed the presence of the 215 cm^{-1} in both polarization directions and attributed it to defects.

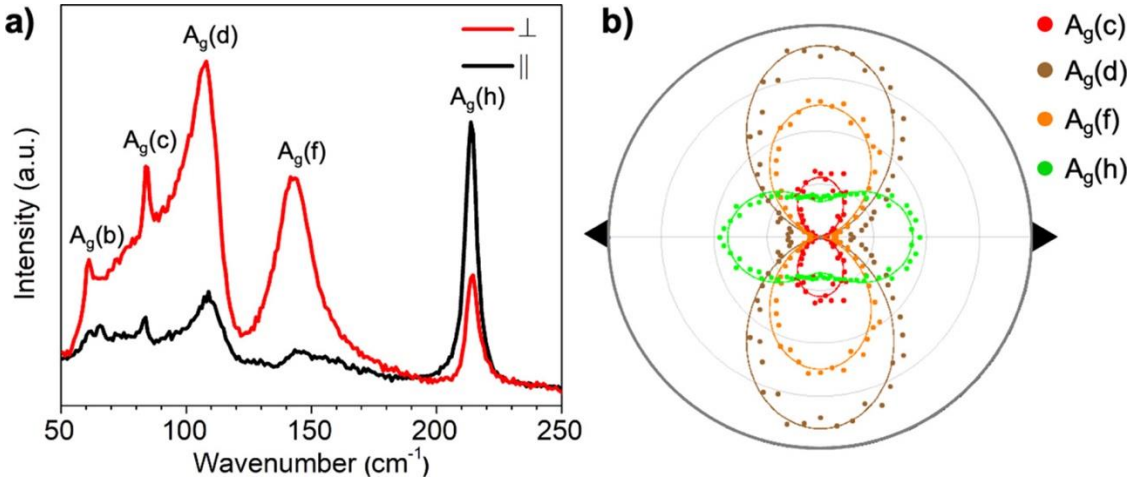

Figure 4.3: (a) Raman spectra with the excitation laser aligned parallel (red) and perpendicular (black) to the $ZrTe_3$ ribbon long axis. The mode assignment is based on ref (11). (b) Polar plot of the angular intensity variation of the Raman peaks of panel (a) and the associated fit curve. The wire direction is indicated by the marks on the left and right of the plot.

To ascertain the electrical transport properties of the CVD material grown in situ on SiO_2, we fabricated four terminal devices on their side (we deposited five terminals, in case one of them had a fabrication problem). Only the contacts applied to one side of each crystallite offer electrical connectivity; those on the opposite side are not connected to the leads because that side of the crystallite is lifted up (Figure 4.1d).

Device fabrication employs the PMMA layer that was initially deposited as an oxidation barrier for the first lithographic step. Electron beam lithography was used to define pads, leads, and contacts to the crystallites. Within minutes after development, we deposited an adhesion layer of 10 nm of yttrium followed by 300 nm of gold at pressures better than 1×10^{-6} torr. Rapid deposition of this contact layer is crucial to avoid excessive contact resistance. Subsequently, the sample was sealed again in a PMMA

layer. In a second lithographic step, the PMMA was removed from the contact pads. Electrical characterization proceeded in a probe station under a nitrogen atmosphere.

Four-point measurements employed a Keithlyer 2400 source meter operated in voltage control to apply a current between the two inner of the four electrodes in a row. To each of the outside electrodes, a Keithley 6517 electrometer is connected. Plotting the current versus the voltage difference between the electrometers generates the *I-V* plot shown in Figure 4.3 and eliminates contact (and lead) resistance from the $ZrTe_3$ wire resistance. A linear relationship indicative of a metallic material is observed; the resistance at room temperature (17 °C) is 21 Ohm.

Comparing the electrometer voltages to the source-meter voltage, we found a combined lead and contact resistance of typically ~10 Ohm. This comparatively low value is a result of optimizing the yttrium adhesion layer deposition. Attributing the entire resistance ~10 Ω to contact resistances, an upper limit of the contact resistance of $1 \times 10^{-6}\ \Omega \times cm^2$ is found.

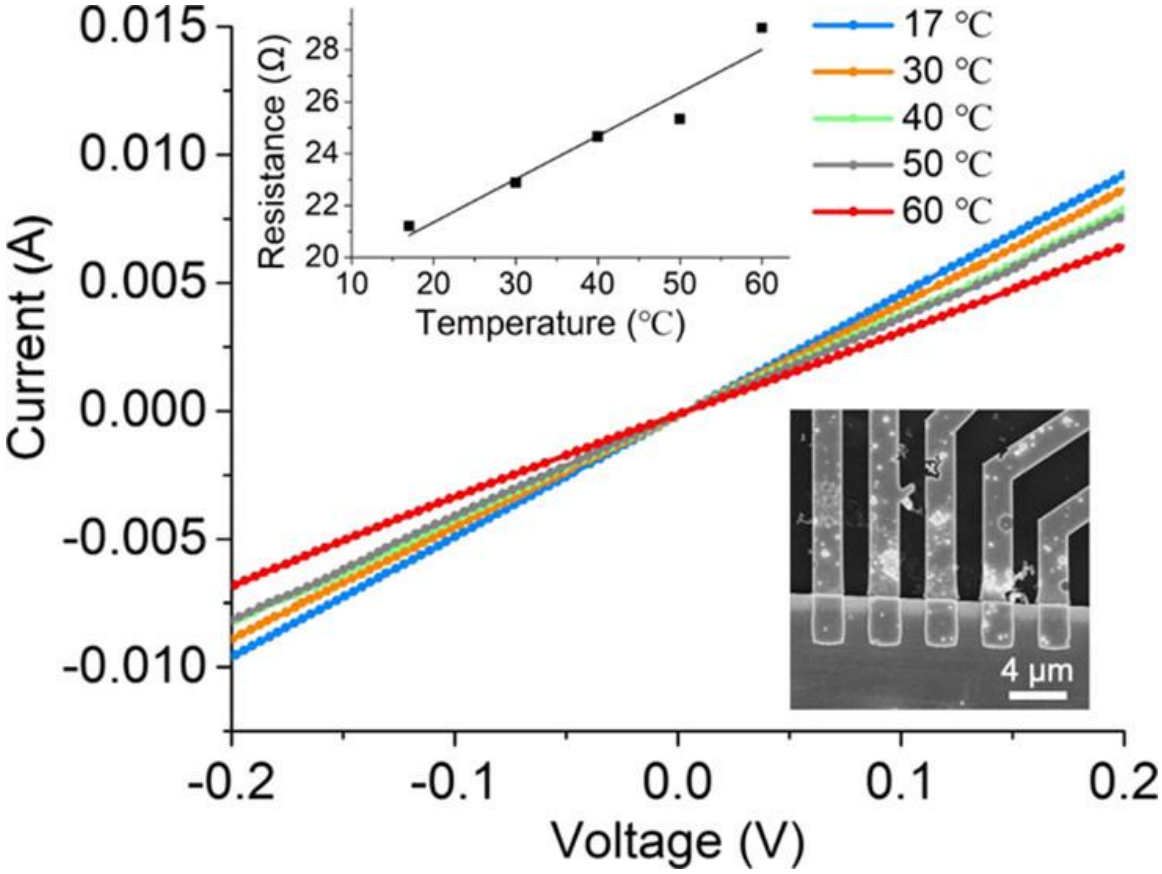

Figure 4.4: Electrical transport of a $ZrTe_3$ crystallite. A linear *I-V* relationship at 21 Ω is observed at room temperature (17 °C). The bottom inset shows an SEM image of the device with a channel length of 1.9 μm, width of 2.9 μm, and depth of 0.7 μm. The top inset shows how the $ZrTe_3$ wire resistance increases with temperature, as expected for a metal.

If we assume that the entire bulk of the material between the electrodes contributes equally to the conduction, then a resistivity ρ^o at 17 °C of $\frac{21\Omega \times 0.7\mu m \times 2.9\mu m}{1.9\mu m} = 2.3\ m\Omega \times cm$ results for a device with a channel thickness (i.e., the thickness of the crystallite) of 0.7 micron, channel width (i.e., the distance the electrodes span onto the crystallite) of 2.9 microns and a channel length (i.e., the separation between the electrodes) of 1.9 microns. The actual resistivity is expected to be lower because only a thin sheet and not the entire volume of the material contributes to the transport in

reality. A simulation in COMSOL assuming isotropic resistivity and contact both at the side wall and the top of the crystallites suggests a value of 1.7 mΩ × cm for the resistivity. As such, the conductivity approaches the bulk one within an order of magnitude. The reported values of resistivity for bulk $ZrTe_3$ are listed in Table 1 for comparison (39,74,75). The remaining deviation is attributed to our assumption of isotropic resistivity and scattering on the $ZrTe_3$ ribbon surface.

Table 4.1: Comparison of Bulk Resistivity Values for $ZrTe_3$ in the Literature

Material	**Resistivity (mΩ×cm)**	**Reference**
$ZrTe_3$ single crystal	A-axis: 0.07	ref (74)
	B-axis: 0.14	ref (74)
$ZrTe_3$ single crystal	A-axis: 0.18	ref (75)
	B-axis: 0.25	ref (75)
$ZrTe_3$ single crystal	B-axis: 0.18	ref (39)
$ZrTe_3$ single crystal	B-axis: 0.1	ref (39)
$ZrTe_3$ polycrystal	B-axis: 14	ref (39)
$ZrTe_3$ CVD crystallites	B-axis: 1.7	This work

Fitting temperature-dependent transport measurements to a linear model of the resistivity $\rho(T + \Delta T) = \rho^o (1 + c \times \Delta T)$ reveals a positive temperature (T) coefficient c of

0.0056 1/K. To our knowledge, this is the first time that a positive temperature coefficient was directly measured on a microscopic 1D vdW sample other than carbon nanotubes.

Figure 4.5 illustrates the COMSOL simulation used to predict the electronic and structural behaviors of $ZrTe_3$ nanowires under various conditions, providing a robust theoretical foundation that complements our experimental findings. COMSOL Multiphysics enabled a detailed exploration of theoretical electron density, charge distribution, and potential energy profiles across the nanowires. By modeling these aspects, we gained valuable insights into the performance of $ZrTe_3$ nanowires in different electronic environments, which is crucial for their application in advanced semiconductor devices. Notably, the simulation results aligned closely with our experimental data, significantly enhancing the credibility of our research.

Integrating COMSOL simulations with empirical methods provided a comprehensive understanding of $ZrTe_3$ nanowires' capabilities, uncovering complex material interactions that are often difficult to detect through experiments alone. These insights are expected to guide the optimization of synthesis processes and support the development of more effective and reliable semiconductor applications utilizing $ZrTe_3$.

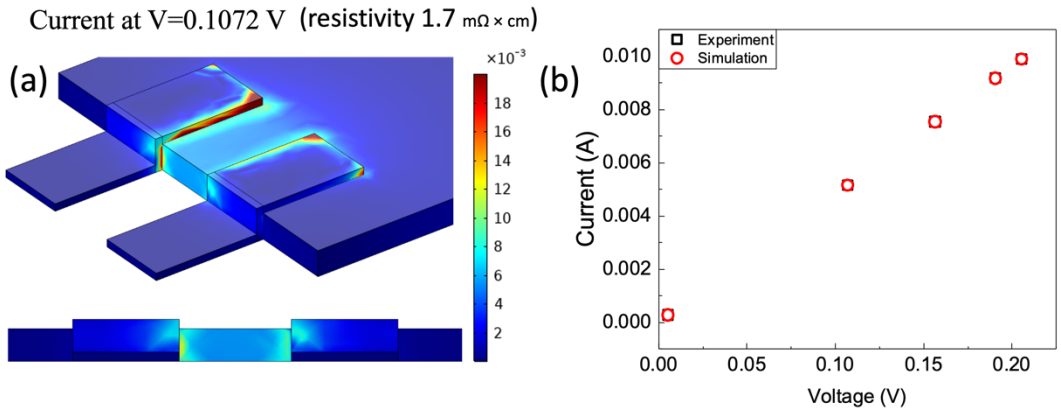

Figure 4.5: COMSOL Simulation

In summary, the strong correlation between COMSOL simulation predictions and experimental data not only validates the reliability of the theoretical models used but also highlights the potential of simulations to advance the development of nanomaterials and facilitate their integration into cutting-edge technology applications.

4.4 Conclusion

In conclusion, we find that $ZrTe_3$ ribbons can be grown by CVD in a rapid process on SiO_2/Si using inexpensive zirconium-(IV)-chloride and tellurium as reactants. The process yields material of high crystallinity and sufficient size for electronic processes; its electrical conductivity is comparable to the bulk. This effort brings the realization of 1D vdW materials as interconnects in electronic devices one step closer.

4.5 Experimental Section

$ZrTe_3$ Nanoribbon Growth

$ZrTe_3$ nanoribbons were synthesized using atmospheric pressure chemical vapor deposition (CVD) in a conventional single-temperature hot-wall furnace. A mixture of 0.3 g of $ZrCl_4$ powder (99.9%, Sigma-Aldrich) and 0.5 g of tellurium powder (99.8%, Sigma-Aldrich) served as the precursors. The powders were combined with a few drops of chlorobenzene and stirred until homogenized in a 1 mL alumina boat (Coors). A pre-cleaned 1.2 cm × 1 cm SiO_2/Si substrate was placed directly on the boat, which was positioned in the center of a small semi-open quartz tube. The boat was inserted 50 mm from the substrate. Ceramic wool was inserted at the open end of the tube to stabilize the reaction environment and prevent contamination. The tube was then placed inside a larger quartz tube, and argon (20 sccm) was purged for 15 minutes during the ramp-up and then turned off during the 10-minute hold period. Hydrogen (30 sccm) was flowed during both the ramp and hold times. The furnace was heated to 550 °C, held for 10 minutes, and allowed to cool naturally to room temperature.

Characterization

The synthesized $ZrTe_3$ nanoribbons were characterized using optical microscopy, field transmission electron microscopy (FTEM, Quanta, FEI) equipped with energy-dispersive X-ray spectroscopy (EDX), scanning electron microscopy (Zeiss), and Raman spectroscopy (LabRAM HR800, Horiba Jobin Yvon, with a 532 nm laser as the excitation source). Electron beam lithography (EBL) was employed to fabricate contacts comprising 5 nm of yttrium for adhesion and 50 nm of gold for conductivity and stability.

Electrical measurements were conducted using a 4-point probe station with a Keithley 2400 source meter and Keithley 6517 electrometer.

CHAPTER 5

Te NANOWIRES

5.1 Abstract

This study investigates the growth, structural characteristics, and electronic properties of tellurium (Te) nanowires (NWs) synthesized using a space-confined chemical vapor deposition (CVD) method. The unique hexagonal crystal structure of Te, with its spiral atomic chains bound by weak van der Waals forces, facilitates the formation of one-dimensional (1D) nanostructures such as nanowires and nanoribbons. The CVD process, optimized to operate at a reduced temperature of 400°C with a brief hold time of 3 minutes, enables the efficient production of Te NWs with high uniformity and controlled morphology, making them suitable for semiconductor applications, especially in Back End of Line (BEOL) integration.

Electrical characterization of the Te NWs demonstrated a significantly lower resistivity compared to bulk Te, with measurements indicating an intrinsic resistivity of approximately 38.87 μΩ·cm at room temperature. This value highlights the superior electrical transport properties of Te NWs, positioning them as promising candidates for miniaturized electronic devices. Additionally, the effects of ion implantation on the Te NWs were explored, revealing that ion exposure can enhance conductivity through defect formation and charge carrier modulation, although challenges such as nanowire breakage due to radiation damage and stress accumulation were observed.

The study concludes that Te NWs synthesized via space-confined CVD exhibit excellent potential for application in advanced electronic devices due to their tunable

electrical properties and scalable production process. Future work will focus on optimizing ion implantation conditions to mitigate structural damage and further enhance the electronic performance of Te NWs, thereby expanding their applicability in next-generation semiconductor technologies.

5.2 Introduction

In recent years, there has been a significant interest in the growth of nanostructured materials with enhanced optical, magnetic, electrical, and chemical properties (82). One-dimensional (1D) nanostructures, such as nanowires, hold considerable promise for applications in nanoscale electronic devices and provide valuable insights into the effects of electron confinement on transport properties. In this project, we focus on the growth of tellurium (Te) nanostructures using chemical vapor deposition (CVD), a widely used technique due to its simplicity and effectiveness in synthesizing various nanomaterials (52)

CVD offers control over the growth environment by adjusting parameters such as source and deposition temperatures, pressure, and carrier gas flow rate. The degree of supersaturation during vapor phase growth plays a critical role: high supersaturation typically results in powder formation, medium supersaturation favors the growth of whiskers and nanowires (20,52,83), and low supersaturation is suitable for bulk single crystal growth. This controlled environment allows for the precise tailoring of Te nanowire growth, optimizing their properties for specific applications (15).

Tellurium is an elemental semiconductor with a bandgap of 0.34 eV, exhibiting p-type conductivity due to lattice defects acting as acceptors (15,47,84). It has a range of unique properties, including photoconductivity, thermoelectric effects, catalytic activity, and strong piezoelectric effects, making it suitable for various applications such as optical recording media, thin-film transistors, strain gauges, infrared detectors, and gas sensors. At normal pressure, Te crystallizes in a hexagonal lattice, where the atoms are arranged

in spiral chains, with neighboring atoms rotated by 120°, each sharing covalent bonds with two of its nearest neighbors. These chains are oriented along the c-axis, held together by weak van der Waals forces. This anisotropic crystal structure is conducive to the growth of 1D structures, such as nanowires and nanotubes, which are ideal for advanced electronic applications.

Nanowires, which are typical 1D nanomaterials, provide a versatile platform for both basic and applied scientific research. In addition to carbon nanotubes and metal nanowires, semiconductor nanowires have attracted significant attention due to their unique properties, making them suitable for use in light-emitting diodes (LEDs), logic gates, lasers, waveguides, and energy conversion devices. Tellurium, with its narrow-bandgap and helical chain structure, shows potential for high-efficiency electrical devices, leveraging its natural 1D form to enhance conductivity and performance in electronic applications (7,40,85).

Further miniaturization in electronics and photonics is often limited by the complexity and cost of conventional top-down manufacturing techniques. Quasi one-dimensional nanostructures, like semiconductor nanowires, serve both as functional components and as interconnects in nanoscale devices. These nanowires are ideal building blocks for functional nanoscale devices, as they combine the roles of active elements and wiring in a single structure. Many prototype devices based on semiconductor nanowires have been demonstrated in electronics, photonics, mechanics, and sensors, highlighting their versatility and potential for widespread applications.

However, despite the success of various semiconductor nanowire devices, full-scale applications in electronics and photonics require effective and controlled doping. Doping modifies the electrical, optical, and magnetic properties of semiconductors but remains challenging for nanowires due to their small size. Doping can be achieved through growth-phase incorporation, ion implantation (86), or diffusion. Ion implantation is a well-established method in the semiconductor industry that allows precise control of dopant concentration, depth, and species, beyond the solubility limits of traditional doping techniques (87,88). This method offers the flexibility of using any element from the periodic table for doping experiments.

The primary challenge of ion implantation, however, is the concurrent production of defects, which can impede the activation of the implanted impurities. This necessitates post-implantation annealing to repair the damage, a process that is complicated in nanostructures due to their reduced thermal stability compared to bulk materials (89,90). Understanding and mitigating these challenges are crucial for the effective application of ion implantation in nanostructured devices.

In this project, we explore the effects of ion implantation on Te nanowires grown via CVD. We investigate how this process influences their electrical, structural, and functional properties, aiming to optimize the synthesis and integration of Te nanowires for advanced semiconductor applications. This study will provide insights into the challenges and opportunities associated with ion implantation in 1D nanostructures, paving the way for the development of more efficient and reliable nanowire-based devices (87,90,91).

5.3 Results

The crystal structure of tellurium (Te) is hexagonal, as depicted in Figure 5.1c. In this arrangement, Te atoms form spiral chains with neighboring atoms rotated by 120°, each atom covalently bonded to two adjacent atoms. These chains align along the c-axis and establish a hexagonal lattice, with chains positioned at the center and each of the six corners of the hexagon. The chains are held together by weak van der Waals forces, facilitating the growth of one-dimensional (1D) structures such as nanowires and nanotubes. These structures are particularly suited for electronic applications due to their unique anisotropic properties.

Te nanowires (Te NWs) were synthesized using a space-confined chemical vapor deposition (CVD) method, valued for its simplicity and precise control over growth conditions. As shown in Figure 5.1a, the CVD setup consists of an inner quartz tube with one end sealed, placed inside a larger outer tube within the furnace. High-purity (99.99%) Te powder, used as the precursor, was positioned near the sealed end of the inner tube within the high-temperature zone to ensure efficient vaporization. The SiO_2/Si substrates, where the nanowires were grown, were placed downstream in the cooler region at the open end of the inner tube. This arrangement creates a temperature and vapor concentration gradient, which is crucial for the controlled nucleation and growth of Te NWs on the substrate.

The growth was carried out at atmospheric pressure with an argon gas flow of 100 sccm and a hydrogen gas flow of 20 sccm. The closed-upstream design of the inner tube confines the vapor, minimizing the effect of gas flow rates on the deposition process.

This confinement stabilizes the growth environment, enhancing the uniformity and quality of the nanowires by maintaining consistent vapor pressure and a steady temperature gradient. A notable achievement of this method is its ability to synthesize Te nanowires at lower temperatures and within shorter processing times compared to conventional CVD techniques. By optimizing CVD parameters, we successfully reduced the synthesis temperature to 400°C, with a hold time of just 3 minutes. Although the setup temperature of 400°C is slightly below Te's melting point, the confined heat within the small tube ensures that the temperature is adequate to vaporize the precursor.

These conditions are energy-efficient and meet the requirements for Back End of Line (BEOL) integration, which is critical for semiconductor device manufacturing. The reduced temperature and processing time conserve energy and minimize thermal stress on the substrate, preserving its structural integrity and facilitating the integration of Te NWs into various electronic device architectures. This approach demonstrates the potential of space-confined CVD for the efficient and scalable production of high-quality nanomaterials with controlled morphology and properties, making them suitable for advanced semiconductor applications. Figure 5.1b shows the optical images of the as-grown Te nanowires under various hold time, highlighting the size tunable growth.

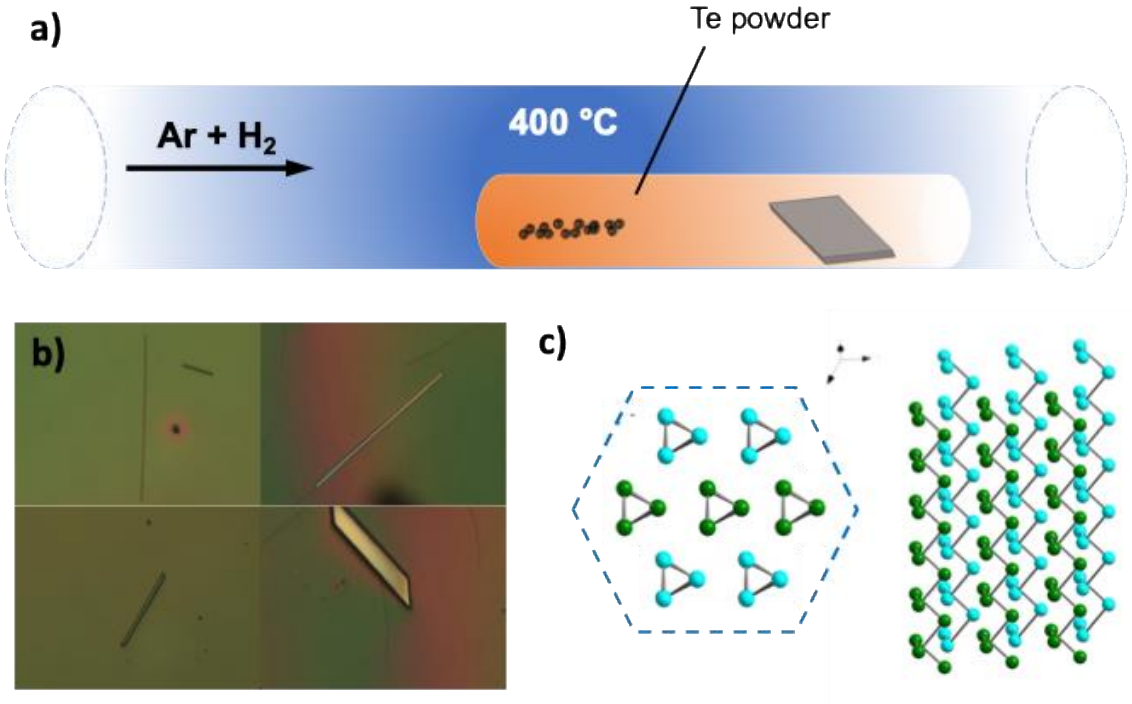

Figure 5.1: (a) CVD setup for the synthesis of Te NWs. (b) Optical images of Te NWs grown under various hold time (c) Atomic structure of hexagonal Te NRs (viewed from c-axis and b-axis).

The optical images of the synthesized tellurium (Te) nanostructures in Figure 5.1 from the CVD process revealed two distinct morphologies on the substrate: nanoribbons and nanowires. To further investigate the structural differences between these morphologies, scanning electron microscopy (SEM) was employed with a 30-degree tilt angle of the electron gun. This approach allowed for a detailed examination of their cross-sectional geometries, providing insights into the underlying growth mechanisms.

The SEM analysis identified two distinct cross-sectional shapes: pentagonal and hexagonal. These variations are attributed to differences in the stacking arrangements of Te atomic chains, as depicted in Figure 5.2. The pentagonal and hexagonal shapes likely result from the varying numbers of Te helices that stack during the growth process,

influencing the overall morphology of the nanostructures. This structural diversity suggests that the stacking configuration plays a crucial role in determining whether a nanostructure develops as a nanoribbon or a nanowire.

Existing literature indicates that the formation energy of Te nanoribbons is higher than that of nanowires when considering the same number of Te helices. This difference in formation energy suggests that nanoribbons, which often exhibit a metallic appearance, may form under specific conditions that favor higher energy configurations. These conditions could arise from kinetic factors during the CVD process, such as rapid deposition rates or fluctuating temperatures, which may temporarily favor the formation of the less stable, higher energy nanoribbons.

Additionally, the surface-to-volume ratio is a critical factor influencing the morphology of Te nanostructures. Nanowires, with their higher surface-to-volume ratio compared to nanoribbons, may be thermodynamically favored, promoting their growth over nanoribbons under certain conditions. This could explain the simultaneous presence of both nanowires and nanoribbons on the substrate, as the growth conditions oscillate between those favoring kinetic versus thermodynamic stability. The balance between these factors—thermodynamic stability favoring nanowires and kinetic pathways leading to nanoribbons—ultimately dictates the observed structural diversity.

Understanding the interplay between these growth dynamics and structural outcomes is essential for optimizing the synthesis process to achieve the desired nanostructure with tailored properties for specific applications. By fine-tuning parameters such as temperature, gas flow rates, and deposition time, it may be possible to selectively

control the formation of nanowires or nanoribbons, enhancing their suitability for use in advanced semiconductor and optoelectronic devices. This comprehensive approach underscores the importance of detailed structural characterization in guiding the development of high-quality Te nanomaterials.

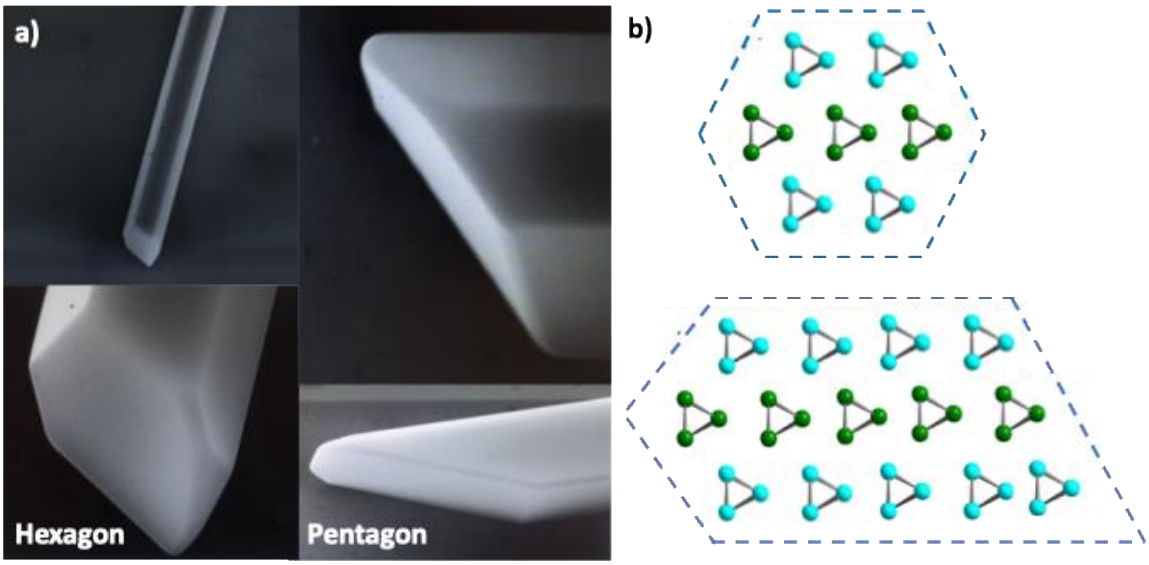

Figure 5.2: (a) SEM images of 2 different shapes of tellurium nanowires. (b) Illustration of the cross-sectional view of Te nanostructures

The reported growth conditions for tellurium (Te) nanowires (NWs) using different synthesis methods are summarized in Table 2. The growth techniques include hydrothermal/solvothermal synthesis, physical vapor deposition (PVD), and chemical vapor deposition (CVD), each offering unique advantages and specific conditions. Hydrothermal/solvothermal synthesis was used to grow Te NWs with a thickness of approximately 10 nm at relatively low reaction temperatures between 100 and 200°C, over extended durations ranging from 12 to 48 hours. While this method provides controlled growth of nanowires, it is time-intensive (92–94).

In contrast, PVD has been utilized to produce Te NWs with a broader thickness range of 10 to 100 nm under high-temperature conditions, involving heating at 1000°C and reacting at 490°C, which also entails a lengthy process time. CVD methods have gained favor for their ability to precisely control nanowire dimensions and properties. Notably, the current work refined this process further by employing a space-confined CVD technique, successfully producing Te NWs with a thickness of 62 nm at a significantly lower reaction temperature of 400°C in just 3 minutes. This approach not only substantially reduces energy consumption and thermal stress on substrates but also aligns with the stringent requirements for Back End of Line (BEOL) integration in semiconductor manufacturing (95,96).

Table 5.1: Comparison of Reported Te NWs Growth Conditions

Te NWs Thickness	**Growth Method**	**Reaction Temperature**	**Process Time**	**Reference**
10 nm	Hydrothermal/Solvothermal Synthesis	100 – 200 ℃	12 – 48 hours	Ref (92)
10 – 100 nm	PVD	1000 ℃ heating 490 ℃ reacting	80 mins heating 2 mins reacting	Ref (93)
230 nm	PVD	450 ℃	-	Ref (94)
200 nm	CVD	600 ℃	-	Ref (95)
68 nm	CVD	750 ℃	5 mins	Ref (96)
62 nm	CVD	400 ℃	3 mins	This work

Raman spectroscopy is a powerful, non-destructive characterization technique widely used to investigate material properties and interactions within layered structures through lattice vibrations (28,47,97,98). In the case of tellurium (Te) nanowires, Raman spectroscopy provides insights into chain-to-chain interactions and the vibrational modes

of the crystal lattice. Consistent with theoretical analysis, the Raman spectrum of Te nanowires revealed three prominent first-order Raman active modes: E_1, A_1, and E_2, located at 92 cm^{-1}, 120 cm^{-1}, and 140 cm^{-1}, respectively. The A_1 mode is associated with chain expansion, where atoms move within the basal plane, while the E_1 and E_2 modes correspond to bond-bending and bond-stretching vibrations, with E_2 showing a larger admixture.

To further analyze the Te nanowires (NWs), we measured the angular dependence of the Raman modes. Figure 5.2a shows the SEM image of a Te crystallite, with the inset displaying an optical image. Figures 5.2b and 5.2c present the Raman spectrum of a Te nanowire and the polar plot of peak intensity, respectively. Notably, no modes exhibited maximum intensity perpendicular to the long axis of the crystallites. The peak Raman response was observed to be offset by approximately 15 degrees from the growth direction of the Te nanowires, suggesting that the nanowires may grow at an angle to the high-symmetry direction, indicating a possible misalignment with the crystallographic axes.

This angular dependence implies that the highest intensity occurs at an angle of approximately 15° between the long axis of the nanowire and the plane of polarization of the excitation laser. Such observations are crucial as they indicate a preferential orientation and potential strain within the nanowires, which can impact their electronic and optical properties. Understanding these angular dependencies and their origins can help refine the growth process, ensuring better alignment and uniformity of the

nanowires, which is essential for their application in electronic and optoelectronic devices.

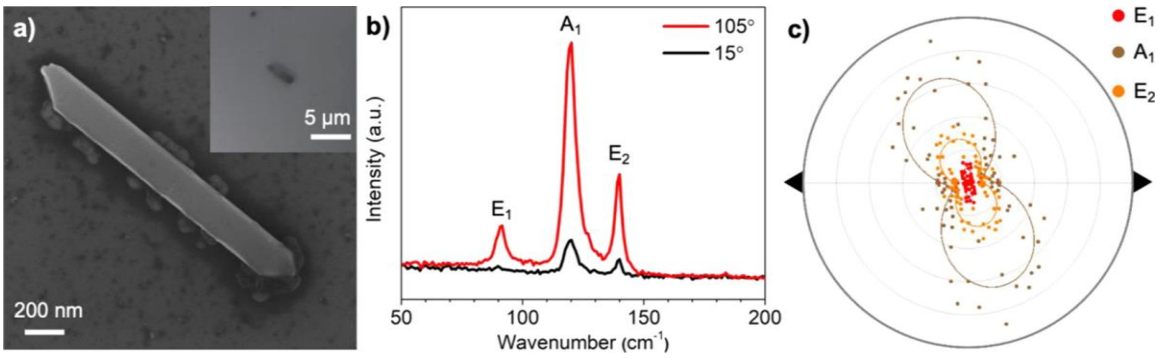

Figure 5.3: (a) SEM image of a tellurium nanowire; the inset shows an optical image. (b) Raman spectrum on the tellurium nanowire and (c) polar plot of the peak intensity.

The unique helical structure of tellurium (Te) significantly influences its electronic and thermal properties. This structure, characterized by specific atomic arrangements and rotational angles, impacts the band structure, leading to low-dimensional conductivity and anisotropic thermal dissipation. These attributes make Te and its compounds highly suitable for thermoelectric applications, where efficient heat and electrical conductivity are crucial for device performance.

To explore the electrical properties of as-grown 1D van der Waals (vdWs) Te nanowires (NWs), we fabricated multi-terminal devices with isolated Te nanowires serving as the channel material. These devices were constructed on a silicon substrate with a 300 nm layer of silicon dioxide (SiO_2) as the gate dielectric. Yttrium/gold (Y/Au, 5/50 nm) electrodes were patterned using electron-beam lithography, followed by electron-beam evaporation and a liftoff process. This precise fabrication method ensured robust contact formation, which is essential for accurate electrical measurements.

The I–V characteristics, as shown in Figure 5.4a, exhibit a linear current-voltage relationship with a resistance of 355.3 kΩ at room temperature (17°C), indicating ohmic behavior. Atomic force microscopy (AFM) and scanning electron microscopy (SEM) were employed to measure the nanowire dimensions, which included a channel length of 1.7 μm, a width of 0.3 μm, and a thickness of 0.062 μm. These precise measurements were critical for calculating the intrinsic resistivity of the Te nanowires, which was found to be approximately 38.87 μΩ·cm at room temperature—significantly lower than the resistivity of bulk Te crystals at around 100 μΩ·cm. This translates to a relative resistivity ratio of 0.39, which is notably lower than ratios observed in nanowires of metals such as copper (Cu), gold (Au), and platinum (Pt) of similar dimensions. These results highlight the superior electrical transport properties of Te nanowires, especially at reduced dimensions, positioning them as promising candidates for miniaturized electronic devices.

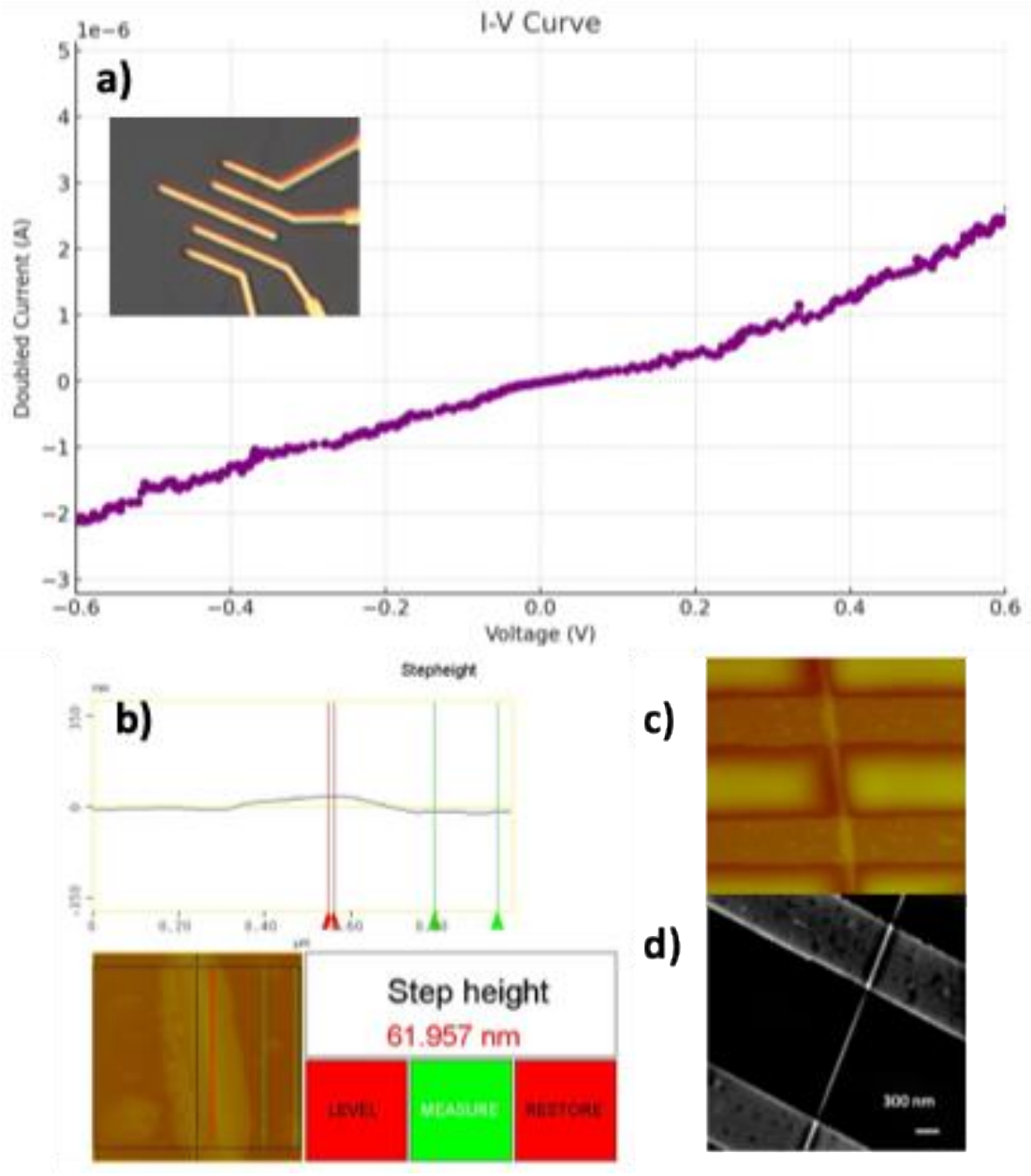

Figure 5.4: (a) Electrical transport of a Te nanowire. A linear *I-V* relationship at 355.3 kΩ is observed at room temperature (17 °C). The top inset shows an optical image of the device with a channel length of 1.7 μm, width of 0.3 μm, and depth of 0.062 μm. (b) AFM image of the measured wire. (c) AFM image of the device. (c) SEM image of the device.

To further understand the electrical properties of Te nanowires synthesized via chemical vapor deposition (CVD), we examined the effects of ion beam-induced conductivity through ion implantation. Ion implantation is a widely utilized technique for the precise modification of material properties, enabling fine-tuning of morphological, mechanical, electronic, and optical characteristics. This method is particularly advantageous for doping one-dimensional nanomaterials with high precision and control. During ion implantation, incident ions interact with the target material through a series of collisions, including nuclear and electronic collisions, as well as charge exchange interactions. These interactions cause the ions to gradually lose kinetic energy, eventually embedding as impurity atoms within the material.

Initially, implanted ions often occupy interstitial sites within the crystal lattice. Subsequent thermal treatments, such as annealing, can promote the migration of these impurities to substitutional positions, where they replace host atoms in the lattice. Substitutional doping is particularly beneficial, as it can significantly alter the electronic and structural properties of nanomaterials, enhancing their performance. By effectively incorporating dopant atoms into the lattice, ion implantation not only improves electrical conductivity but also optimizes the overall functionality of nanomaterials, making them more suitable for advanced technological applications.

In this study, we conducted two-probe measurements under ion exposure using a Keithley 4200 source meter operated in voltage control to apply current between two electrodes on the Te nanowire. Figure 5.5 illustrates the current-voltage (I-V) characteristics of a Te nanoribbon subjected to varying levels of accumulated Si^+ ion

fluence. A voltage sweep was applied across the nanoribbon, and current was measured after each ion beam exposure. The x-axis represents the voltage applied across the nanoribbon, ranging from approximately -5 to 5 volts, while the y-axis shows the measured current in amperes, ranging from about -0.00004 to 0.00004 A.

The legend in the figure specifies the accumulated shots of Si^+ ion fluence (fluence per shot: 1e9 ions/cm^2), ranging from 0.5 to 739,247.5 shots. Each curve corresponds to a different fluence value, with lower fluence curves near the origin and higher fluence curves showing increasingly larger current responses. This gradient of colors and symbols in the legend allows clear identification of the changes in I-V behavior as a function of increasing ion fluence. At lower fluence levels, the I-V characteristics are nearly linear and symmetrical around the origin, indicating minimal conductivity changes. As the accumulated ion fluence increases, the curves diverge further from the origin, showing enhanced current response at a given voltage, suggesting that ion implantation significantly enhances the conductivity of the Te nanowire. The nearly symmetrical increase in current in both positive and negative voltage regions implies uniform ion beam-induced modifications across different bias directions.

This behavior suggests that ion beam exposure introduces defects or impurities that increase charge carrier density or mobility within the nanoribbon, thereby enhancing its overall conductivity. The figure effectively demonstrates the relationship between applied voltage and resulting current across a range of ion fluences, highlighting the role of ion implantation in modifying the electrical properties of nanomaterials, which is critical for optimizing their performance in electronic devices. However, these results are

preliminary, and further verification through four-terminal measurements is recommended.

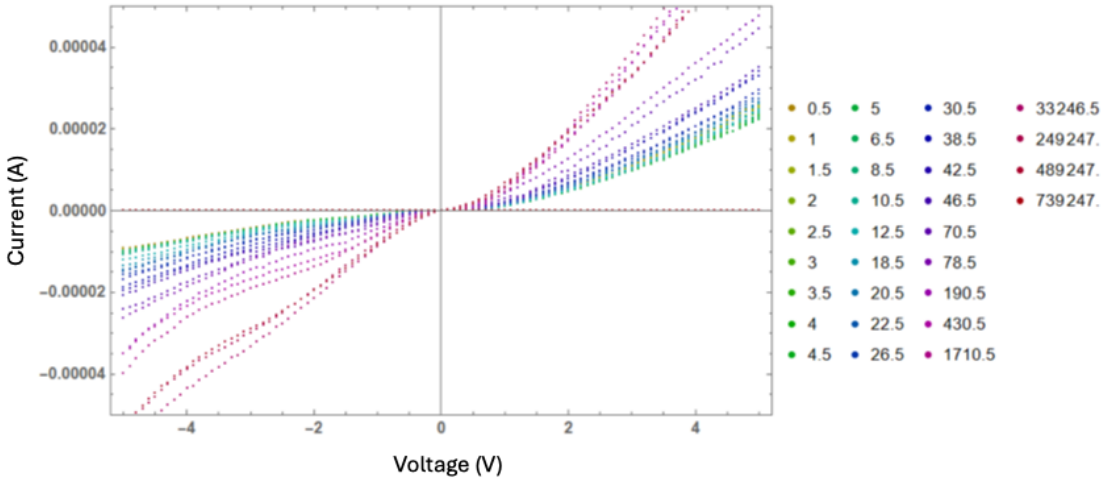

Figure 5.5: I-V Curve under accumulated Si^+ ion fluence implantation

Figure 5.6 shows the current response of a Te nanoribbon as a function of accumulated Si^+ ion fluence, with the x-axis representing fluence on a logarithmic scale (ranging from 1 to 10^6) and the y-axis displaying the current (from approximately -0.00006 to 0.00008 A). The color-coded series of dots correspond to different applied voltages, ranging from -5 V to 5 V as indicated by the legend. Notably, the figure reveals asymmetry in the current response under positive versus negative voltage, particularly at higher fluence levels. For fluences above 10^2, the current values at positive voltages (e.g., 3 V to 5 V) increase more significantly than those at equivalent negative voltages (-3 V to -5 V), indicating a directional dependence. This asymmetry suggests that ion beam-induced modifications, such as defect generation and interface changes, have a greater impact on enhancing conductivity under positive bias than under negative bias, resulting in a non-uniform current-voltage response across different fluence levels. This directional

dependence underscores the complex interactions between the ion beam and the nanoribbon, affecting its electronic properties asymmetrically.

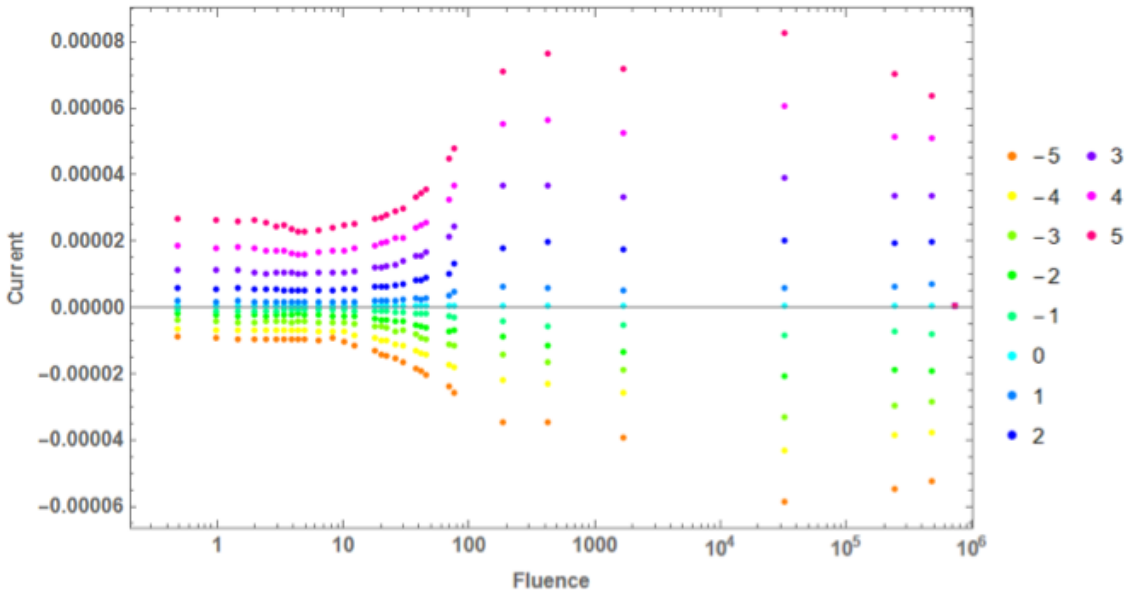

Figure 5.6: Current at different voltages shown on the right, as a function of Fluence on a Logarithmic Axis.

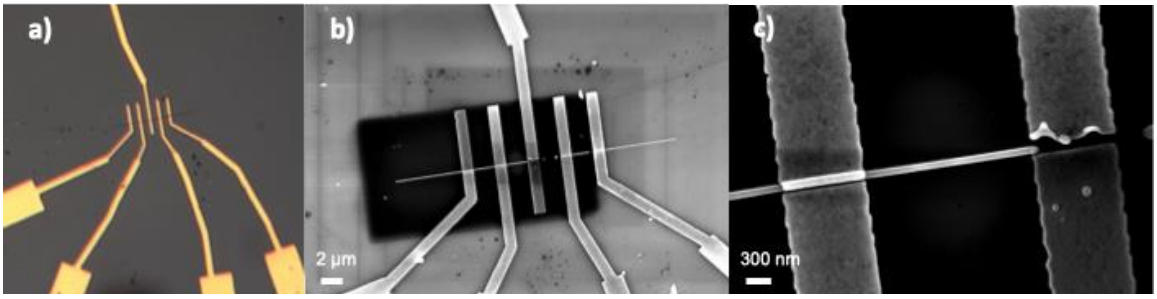

Figure 5.7: (a) Optical image of Te Nw before ion exposure (b) Postmortem SEM images of Te Nw (c)Zoom-in view of b

Figure 5.7 presents the optical image of the tellurium (Te) nanowire before ion exposure and postmortem SEM images after ion implantation. During the ion exposure, the Te nanowire fractured, likely due to a combination of thermal stress and ion fluence.

The breakage of nanowires during ion implantation can occur for several reasons. Radiation damage and defect formation are significant contributors; high-energy ions displace atoms in the nanowire, creating defects like vacancies and interstitials. As these defects accumulate, they weaken the nanowire's structure, making it more prone to breaking. Stress accumulation also plays a critical role, as the implanted ions cause localized stress due to the mismatch in atomic sizes, which can lead to microcracks or dislocations. Over time, the stress builds up to a critical point, resulting in the structural failure of the nanowire. Additionally, charging effects during ion exposure can lead to charge buildup on the nanowire, creating electrostatic forces that may distort or fracture the nanowire if the charge is not properly dissipated. Thermal effects further exacerbate the situation; localized heating from ion implantation can cause temperature spikes, leading to thermal expansion and added stress. This can further compromise the nanowire's integrity and increase the likelihood of breakage. These factors collectively contribute to the fragility of nanowires during ion implantation, underscoring the need for precise control over the implantation conditions to preserve their structural integrity.

5.4 Conclusion

This project explored the growth, characterization, and modification of tellurium (Te) nanowires (NWs) synthesized through a space-confined chemical vapor deposition (CVD) method. The unique hexagonal crystal structure of Te, consisting of spiral atomic chains bound by van der Waals forces, facilitates the formation of one-dimensional (1D) nanostructures with promising applications in advanced electronics. The space-confined CVD technique proved highly effective, allowing for the synthesis of Te NWs at reduced temperatures and processing times, achieving high-quality nanostructures suitable for semiconductor integration, particularly in Back End of Line (BEOL) processes.

A key outcome of this study was the identification of two distinct morphologies—nanoribbons and nanowires—through SEM analysis. The different cross-sectional shapes, pentagonal and hexagonal, were attributed to variations in Te atomic chain stacking during growth, highlighting the importance of growth dynamics in determining nanostructure morphology. The coexistence of these forms suggests a balance between kinetic and thermodynamic factors, emphasizing the need for precise control over growth parameters to tailor nanostructure properties for specific applications.

Electrical characterization of the Te NWs revealed superior transport properties, with resistivity significantly lower than that of bulk Te crystals, positioning them as excellent candidates for miniaturized electronic devices. The observed linear I-V characteristics and relatively low resistivity underscore the potential of Te NWs in

enhancing the performance of nanoscale electronic components, offering a pathway to improved device efficiency and reduced energy consumption.

Further investigation into the effects of ion implantation on Te NWs demonstrated that ion exposure can significantly enhance electrical conductivity, likely through the introduction of defects or impurities that alter charge carrier dynamics. However, the process also posed challenges, such as nanowire breakage due to radiation damage, stress accumulation, and thermal effects. These findings highlight the delicate balance required in ion implantation, where optimizing implantation conditions is crucial to achieving desired modifications without compromising structural integrity.

Overall, this study provides a comprehensive understanding of the growth, structural diversity, and tunable electrical properties of Te NWs, showcasing their potential for integration into advanced semiconductor devices. The insights gained from the synthesis and modification of Te NWs contribute to the broader field of nanomaterials, offering strategies for enhancing material performance through controlled growth techniques and targeted modifications. Future work should focus on refining ion implantation processes and exploring alternative doping methods to further optimize the electronic properties of Te nanostructures, paving the way for their application in next-generation electronics and optoelectronics.

5.5 Experimental Section

Te Nanowire Growth

Te nanowires were synthesized using chemical vapor deposition (CVD) in a single-temperature hot-wall furnace. A precursor of 0.8 g tellurium powder (99.8%, Sigma-Aldrich) was placed near the sealed end of the inner tube in the high-temperature zone to ensure efficient vaporization. The SiO_2/Si substrates, used for nanowire growth, were placed downstream in the cooler region at the open end of the inner tube, creating a temperature and vapor concentration gradient essential for controlled nucleation and growth. The growth process was conducted at atmospheric pressure with an argon gas flow of 100 sccm and hydrogen gas flow of 20 sccm. The inner tube's closed-upstream design confined the vapor, reducing the impact of gas flow rates on the deposition. The furnace was ramped to 400 °C in 8 minutes, maintained for 3 minutes, and then allowed to cool naturally to room temperature.

Characterization

Te nanowires were characterized using optical microscopy, Raman spectroscopy (LabRAM HR800, Horiba Jobin Yvon, with a 532 nm laser as the excitation source), atomic force microscopy (Dimension 5000 scanning probe microscope), and scanning electron microscopy (Zeiss). Electron beam lithography (EBL) was used to fabricate contacts with 5 nm of yttrium for adhesion and 50 nm of gold for conductivity and stability. Electrical measurements were performed using a 3-point probe station with a Keithley 4200 source meter.

CHAPTER 6

PATTERNED GROWTH OF $TaSe_3$

6.1 Abstract

This chapter explores the patterned growth of $TaSe_3$ nanowires on lithographically prepared substrates, utilizing strategies such as UV optical photolithography and electron-beam lithography (EBL) to control material placement, orientation, and growth. By creating artificial defects and patterned features on SiO_2 substrates, we successfully guided the nucleation of both 2D and 1D materials, including MoS_2, WS_2, and $TaSe_3$. For 2D materials, features such as etched or raised circles effectively acted as nucleation sites, allowing for precise control over film growth. For 1D nanowires, initial efforts using traditional dot patterns were inadequate due to the nanowires' linear growth nature and smaller aspect ratios. To address this, we refined the approach by developing smaller, well-spaced EBL patterns that provided distinct pathways, effectively directing nanowire growth in predetermined directions.

The findings highlight the potential of patterned substrates to act as growth templates, offering a scalable method for integrating quasi-1D materials into microelectronic applications. This approach aims to leverage the unique interconnectivity and conductivity of patterned nanowire networks, with the goal of establishing them as alternatives to conventional interconnection materials like copper in semiconductor devices. The results pave the way for more efficient and controlled integration of nanowires into electronic circuits, enhancing their application potential in next-generation microelectronics (68,70,99–102).

6.2 Introduction

In this chapter, we explore the strategies for guiding the growth of two-dimensional (2D) and one-dimensional (1D) materials using lithographically patterned wafer substrates. These substrates act as predefined "roadways," enabling precise control over the location, placement, and orientation of materials during growth, which is critical for their integration into electronic devices. Patterned growth not only improves the material quality but also aligns with the demands for scalable manufacturing processes in semiconductor industries (58,103,104).

We investigated various methods to induce preferential nucleation of 2D material growth, such as MoS_2 and WS_2, using artificially created defects on the substrate surface. Key approaches include: (1) manually scribing marks into the growth substrate to introduce nucleation sites, (2) patterning the SiO_2 surface with lithography followed by etching to generate controlled defects, and (3) utilizing photolithography or electron-beam lithography (EBL) to create specific patterns on the wafer and subsequently depositing metals like molybdenum that act as nucleation centers. Figures

6.1a and 6.1b illustrate arrays of circular patterns that have been either raised or etched down, thereby forming artificial defect edges along the wafer surface that serve as nucleation spots. Additionally, using these patterns to deposit a thin layer of molybdenum metal further enhanced seeding, resulting in the coalescence of thin-film transition metal dichalcogenides (TMDs) during chemical vapor deposition (CVD) growth into large-scale films.

For 1D materials, a critical aspect of patterned growth is assessing their potential as interconnects in electronic circuits. Unlike 2D materials, which can form continuous films, 1D nanowires require strategies that promote not only aligned growth but also functional connectivity. A fundamental question arises: can 1D materials like $TaSe_3$ nanowires merge, branch, or maintain electrical conductivity at their junctions when they come into contact? Figure 6.1c demonstrates that $TaSe_3$ nanowires possess the ability to grow in branched directions, indicating a strong potential for these materials to be directed along pre-defined patterns on a wafer.

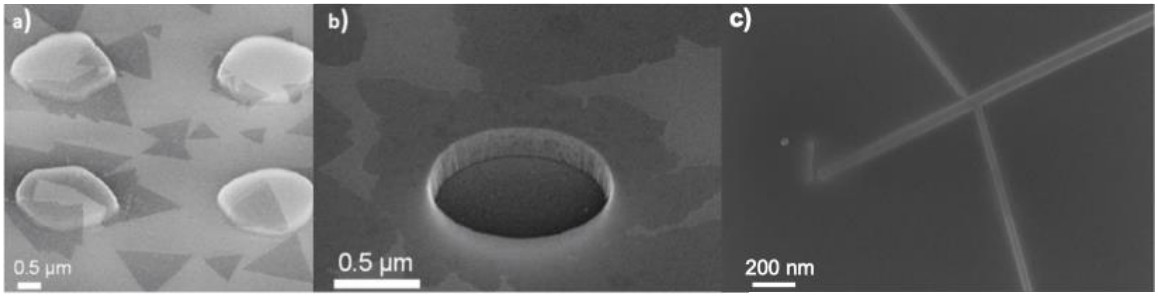

Figure 6.1: (a) SEM image of pre-patterned substrates with SiO2 circles raised 250nm from the surface (b). Circles etched down 250nm (c) As-grown branched nanowire

To extend these findings, we explored additional patterning techniques to facilitate the selective growth of $TaSe_3$ nanowires. For instance, substrates were patterned with alternating stripes of SiO_2 and hafnium oxide (HfO_2), deposited via atomic layer deposition (ALD). This patterning was designed to guide the growth of WSe_2, which showed preferential nucleation on the HfO_2 stripes, forming thicker connections while leaving only a monolayer on the SiO_2 areas. These results suggest that similar patterning techniques can be tailored to optimize the growth conditions for 1D materials, enhancing their integration into complex device architectures.

Our findings underscore the importance of patterned growth in the context of 1D $TaSe_3$ nanowires, as their ability to grow in predefined orientations and connect at junctions is crucial for their application in electronic devices, particularly as interconnects. Future work will focus on refining the patterning methods to maximize the alignment and connectivity of these nanowires (56,105,106) with the goal of achieving reliable and efficient interconnects for microelectronic applications. By fine-tuning parameters such as pattern dimensions, spacing, and material choices, we aim to further enhance the scalability and functionality of $TaSe_3$ nanowires, paving the way for their broader adoption in next-generation semiconductor technologies.

This section provides a comprehensive overview of the strategies employed for patterned growth, emphasizing the critical role of substrate engineering in dictating the nucleation and growth dynamics of both 2D and 1D materials. This approach not only advances our understanding of material growth on patterned substrates but also lays the foundation for developing scalable fabrication processes for high-performance electronic devices.

6.3 Results

This section discusses the use of UV optical photolithography and electron-beam lithography (EBL) as primary methods for patterning substrates to guide the growth of 2D and 1D materials. These patterning techniques are vital for precisely controlling material placement and orientation on wafer surfaces, enabling the strategic direction of material growth. While photolithography is suitable for creating larger aspect ratio patterns ideal for 2D materials, EBL allows for the smaller, more intricate patterns necessary for 1D nanowires.

For 2D materials like MoS_2 and WS_2, which typically form films or islands, patterning designs can handle a broad range of aspect ratios. MoS_2, for instance, often grows into triangular islands spanning 5 to 20 μm. We observed that these materials preferentially nucleate around imperfections on the substrate, such as accidental scratches on the SiO_2 layer. This led us to hypothesize that artificially created defects could be used to direct growth. To test this, we patterned the substrate using photolithography and reactive ion etching, creating circular features 1.5 to 2 μm in diameter spaced 7 to 10 μm apart. These patterns were made using both positive and negative resists: in positive resist patterns, the exposed circles were etched into the surface, and in negative resist patterns, the circles were protected while the surrounding areas were etched away, leaving raised pillars. As shown in Figure 6.2, MoS_2 consistently nucleated at the center of these features, and this behavior was similarly observed with other 2D CVD-grown materials like WS_2.

Extending these strategies to 1D nanowires, however, presented challenges. Simply replicating the standard dot pattern used for 2D materials (1.5 µm diameter, 7 µm spacing) did not effectively guide the growth of 1D nanowires, as shown in Figure 6.3a. This was attributed to the distinct aspect ratios of 1D nanowires, which typically grow about 2 µm in length and 20 to 100 nm in width. Unlike 2D materials that expand outward as films, 1D nanowires require pattern designs that specifically encourage linear growth along predefined paths.

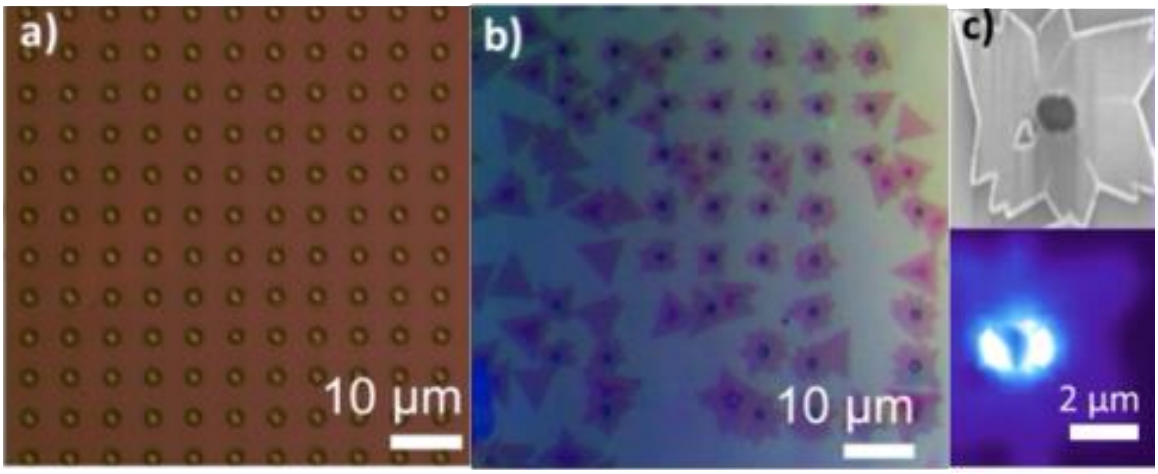

Figure 6.2: (a) Optical image of a patterned and etched SiO_2 on Si wafer piece. (b) Post-CVD growth of MoS_2 islands over the etched patterned areas confirms seeding practice. (c) SEM image and PL mapping of MoS_2 island over an etched area show higher PL response indicative of strain over the etched hole.

To address this, we used EBL to develop a refined pattern suitable for 1D nanowire growth. The optimized pattern consisted of 100 nm by 100 nm squares spaced 1 µm apart, arranged in a hexagonal outline (Figure 6.3b). This configuration provided clear growth pathways without overcrowding the seeding sites, enabling us to attribute directional growth to the pattern itself rather than random nucleation. As shown in Figures 6.3c and 6.3d, this approach successfully directed the nanowires to grow along

these predefined paths, which allowed for the subsequent fabrication of devices on interconnected nickel waypoints to collect electrical transport measurements across the nanowires and their junctions.

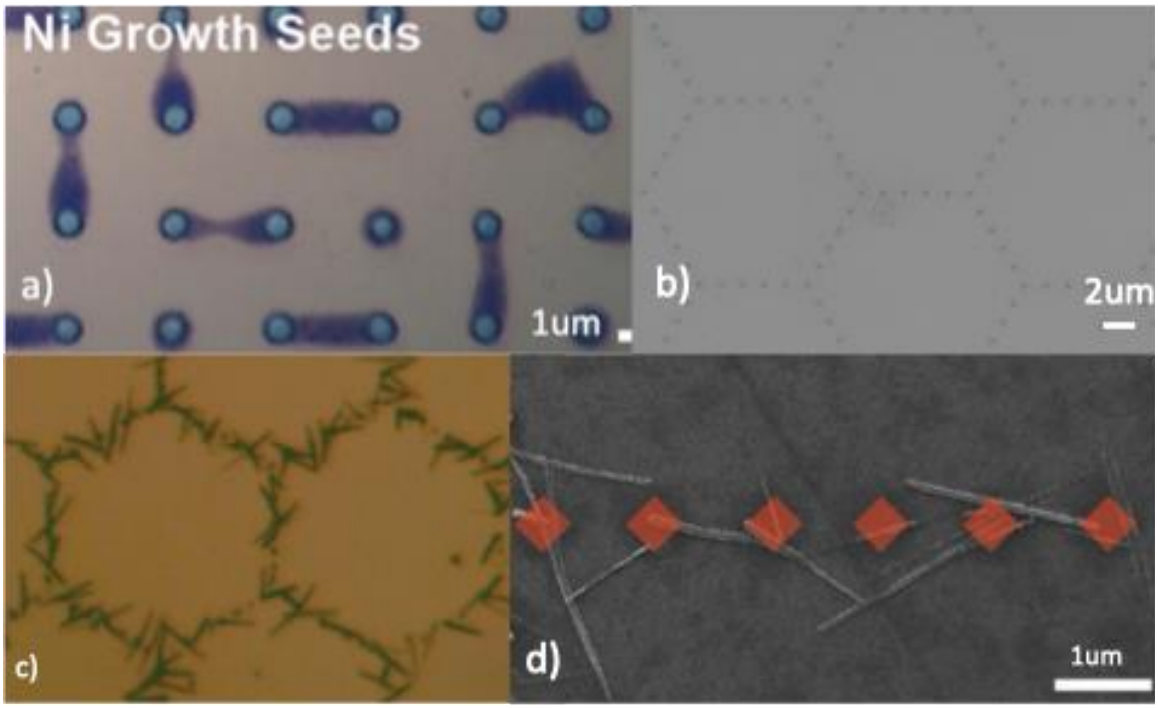

Figure 6.3: (a) Optical image of patterned SiO_2 on Si wafer where the blue dots are 25 nm thick nickel metal dots and the film between appears as pre-growth of nanowires. (b) Prototype seeding pattern for nanowires and 1D material growth. (c) Optical image of post-CVD growth of $TaSe_3$ shows great seeding affinity for the nickel dots. (d) SEM inspection of growth results in c.

Future work will involve further refining the patterned growth techniques to improve consistency and reproducibility of 1D nanowire alignment along the predefined paths. One critical area of development will be device fabrication directly on pre-patterned nanowires, which will allow for a systematic comparison of their electrical properties against those of individually grown nanowires. This approach will include designing and fabricating multi-terminal devices that leverage the patterned nanowire

networks, enabling detailed studies of their interconnect behavior, resistance, and overall conductivity.

Ultimately, the goal is to develop scalable, reliable fabrication processes that harness the unique properties of patterned nanowires for use in advanced electronic applications, such as high-performance interconnects and nanoscale transistors. This work will pave the way for integrating quasi-1D materials like $TaSe_3$ into mainstream semiconductor manufacturing, potentially replacing traditional materials like copper in microelectronic interconnections due to their superior electrical transport properties and stability at reduced dimensions.

6.4 Conclusion

In this chapter, we examined strategies for using lithographically patterned substrates to guide the growth of 2D and 1D materials, focusing on UV optical photolithography and electron-beam lithography (EBL). These techniques provide control over the placement and orientation of materials, essential for developing advanced electronic devices. For 2D materials like MoS_2 and WS_2, which grow as films or islands, we found that introducing deliberate defects on the substrate surface, such as patterned circles or etched features, successfully directed material growth. Patterns were created using both positive and negative resists, resulting in either etched or raised features that consistently acted as nucleation sites, as shown in Figure 6.2.

Applying these methods to 1D nanowires posed unique challenges due to their smaller aspect ratios and linear growth requirements. Initial tests with standard dot patterns were ineffective for nanowires, as shown in Figure 6.3a. To address this, we refined the pattern using EBL, creating smaller, 100 nm by 100 nm squares arranged in a hexagonal outline. This design provided clear growth paths without overcrowding the seeding sites, allowing for controlled and directional growth of 1D nanowires, demonstrated in Figures 6.3c and 6.3d.

Future work will involve fabricating devices directly on pre-patterned nanowires to compare their electrical properties with those of single nanowires. This approach will enable the development of multi-terminal devices that utilize patterned nanowire networks, providing insights into their interconnect behavior and overall conductivity. The goal is to establish scalable fabrication processes that exploit the properties of

patterned nanowires, positioning them as potential replacements for conventional materials like copper in microelectronic interconnections. This work aims to integrate quasi-1D materials, such as $TaSe_3$, into advanced electronic applications, enhancing device performance and efficiency.

6.5 Experimental Section

Pattern Design and Writing

Optimized patterns for 1D nanowire growth were developed using electron beam lithography. The design consisted of 100 nm × 100 nm squares spaced 1 μm apart in a hexagonal arrangement, allowing for clear growth pathways and minimizing overcrowding at seeding sites. This setup ensured that directional growth was due to the pattern rather than random nucleation. Subsequent metal deposition was carried out using an e-beam evaporator (Temescal BJD 1800 systems).

SUMMARY

This dissertation investigates the growth, characterization, and application potential of quasi-1D van der Waals (vdW) nanowires, specifically focusing on $ZrTe_3$, Te, and $TaSe_3$. The primary objective is to develop scalable synthesis methods and assess the feasibility of integrating these materials into advanced microelectronic applications, particularly as interconnects in semiconductor devices. Utilizing chemical vapor deposition (CVD) and various pattern-guided growth strategies, the research aims to address integration challenges of quasi-1D materials in current and future electronic technologies.

$ZrTe_3$ nanoribbons were successfully synthesized on SiO_2/Si substrates via CVD using cost-effective precursors, demonstrating high crystallinity and adequate size for electronic applications with electrical conductivity comparable to bulk forms. The study of Te nanowires via space-confined CVD highlighted the formation of distinct morphologies, including nanoribbons and nanowires, driven by variations in atomic chain stacking. Electrical characterization revealed superior transport properties, suggesting their suitability for miniaturized electronic devices. Ion implantation further enhanced their conductivity, though the process introduced challenges such as nanowire breakage from radiation damage and stress accumulation, underscoring the need for precise implantation control.

Additionally, the research explores the use of lithographically patterned substrates to guide the growth of 2D and 1D materials. Techniques like UV optical photolithography and electron-beam lithography (EBL) were employed to create specific

nucleation sites, effectively directing the growth of materials like MoS_2, WS_2, and $TaSe_3$. For $TaSe_3$ nanowires, refined patterns using EBL enabled controlled, directional growth, demonstrating their potential for integration into patterned nanowire networks. Future work will focus on fabricating devices on pre-patterned nanowires to compare their electrical properties with those of single nanowires, exploring their viability as alternatives to conventional interconnect materials like copper.

Overall, this dissertation provides a thorough exploration of the growth, structural characteristics, and tunable electrical properties of quasi-1D vdW nanowires. The findings highlight the promise of these materials for advanced semiconductor applications, paving the way for their integration into next-generation electronic devices and contributing valuable insights to the field of nanomaterials through innovative synthesis and modification techniques.

REFERENCE

1. Novoselov KS, Mishchenko A, Carvalho A, Castro Neto AH. 2D materials and van der Waals heterostructures. Science. 2016;353(6298).

2. Joensen P, Crozier ED, Alberding N, Frindt RF. A study of single-layer and restacked MoS2by X-ray diffraction and X-ray absorption spectroscopy. J Phys. 1987;20(26):4043–53.

3. Liu G, Debnath B, Pope TR, Salguero TT, Lake RK, Balandin AA. A charge-density-wave oscillator based on an integrated tantalum disulfide–boron nitride–graphene device operating at room temperature. Nat Nanotechnol. 2016;11(10):845–50.

4. Burducea I, Mateescu AO, Mateescu G, Ionescu C, Straticiuc M, Craciun LS, et al. AFM, RBS and tribological properties of WC/WS2 nanostructures after 1.5 MeV Nb+ implantation. Nucl Instrum Methods Phys Res B. 2019;450:357–60.

5. Advances in chemical vapor deposition. Mdpi AG; 2021.

6. Nakajima H, Nomura K, Sambongi T. Anisotropic superconducting transition in ZrTe3. Physica. 1986;143(1–3):240–2.

7. Yadav RA, Padma N, Sen S, Chandrakumar KRS, Donthula H, Rao R. Anomalous vibrational behavior of two dimensional tellurium: Layer thickness and temperature dependent Raman spectroscopic study. Appl Surf Sci. 2020;531(147303):147303.

8. Lukatskaya MR, Mashtalir O, Ren CE, Dall'Agnese Y, Rozier P, Taberna PL, et al. Cation intercalation and high volumetric capacitance of two-dimensional titanium carbide. Science. 2013;341(6153):1502–5.

9. Mak KF, Lee C, Hone J, Shan J, Heinz TF. Atomically thin MoS_2: a new direct-gap semiconductor. Phys Rev Lett. 2010;105(13):136805.

10. Stolyarov MA, Liu G, Bloodgood MA, Aytan E, Jiang C, Samnakay R, et al. Breakdown current density in h-BN-capped quasi-1D $TaSe_3$metallic nanowires: prospects of interconnect applications. Nanoscale. 2016;8(34):15774–82.

11. Hu Y, Zheng F, Ren X, Feng J, Li Y. Charge density waves and phonon-electron coupling inZrTe3. Phys Rev B Condens Matter Mater Phys. 2015;91(14).

12. Chem. Vap. Deposition (4-5-6/2015). Chem Vap Depos. 2015;21(4-5–6).

13. Empante TA, Zhou Y, Klee V, Nguyen AE, Lu IH, Valentin MD, et al. Chemical vapor deposition growth of few-layer $MoTe_2$ in the 2H, 1T′, and 1T phases: Tunable properties of $MoTe_2$ films. ACS Nano. 2017;11(1):900–5.

14. Sivaram S. Chemical vapor deposition: Thermal and plasma deposition of electronic materials. 1995th ed. New York, NY: Springer; 1995.

15. Martín-García B, Marras S, Spirito D. Chiral tellurium under polarized Raman spectroscopy: Crystal orientation and handedness. In: Proceedings of the MATSUS Spring 2024 Conference. València: FUNDACIO DE LA COMUNITAT VALENCIANA SCITO; 2023.

16. Jain A, Ong SP, Hautier G, Chen W, Richards WD, Dacek S, et al. Commentary: The Materials Project: A materials genome approach to accelerating materials innovation. APL Mater. 2013;1(1).

17. Canadell E, Rachidi IEI, Pouget JP, Gressier P, Meerschaut A, Rouxel J, et al. Comparison of the electronic structures of layered transition-metal trichalcogenides thallium triselenide, thallium trisulfide and niobium triselenide. Inorg Chem. 1990;29(7):1401–7.

18. Heidenreich J, Edelstein D, Goldblatt R, Cote W, Uzoh C, Lustig N, et al. Copper dual damascene wiring for sub-0.25 μm CMOS technology. In: Proceedings of the IEEE 1998 International Interconnect Technology Conference (Cat No98EX102). IEEE; 2002. p. 151–3.

19. Geremew A, Bloodgood MA, Aytan E, Woo BWK, Corber SR, Liu G, et al. Current Carrying Capacity of Quasi-1D $ZrTe_3$Van Der Waals Nanoribbons. IEEE Electron Device Lett. 2018;39(5):735–8.

20. Liang L, Rao T, Wu T, Li H. Determination of melamine by label-free ratiometric fluorescence using the inner-filter effect (IFE) between cadmium tellurium/cadmium sulfide quantum dots (QDs) and gold nanoparticles (Au NPs). Anal Lett. 2024;57(13):1959–73.

21. Gill JC. Dislocations and the motion of weakly pinned charge-density waves: Experiments on niobium triselenide containing mobile indium impurities. Phys Rev B Condens Matter. 1996;53(23):15586–603.

22. Bjerkelund E, Fermor JH, Kjekshus A, Wagnières M, Williams DH, Bunnenberg E, et al. On the properties of TaS3 and TaSe3. Acta Chem Scand. 1966;20:1836–42.

23. Bjerkelund E, Kjekshus A. On the properties of TaS3, TaSe3 and TaTe4. Allg Chem. 1964;328:235–42.

24. Butler SZ, Hollen SM, Cao L, Cui Y, Gupta JA, Gutiérrez HR, et al. Progress, challenges, and opportunities in two-dimensional materials beyond graphene. ACS Nano. 2013;7(4):2898–926.

25. Zwick A, Renucci MA, Kjekshus A. Raman scattering in the IVB transition-metal trichalcogenides: ZrS_3, $ZrSe_3$, $ZrTe_3$and $HfSe_3$. J Phys. 1980;13(30):5603–14.

26. Zhou D, Li H, Si N, Jiang Y, Huang H, Li H, et al. Epitaxial growth of single tellurium atomic wires on a Cu2Sb surface alloy. Appl Phys Lett. 2020;116(6):061602.

27. Zhang Y, Tan YW, Stormer HL, Kim P. Experimental observation of the quantum Hall effect and Berry's phase in graphene. Nature. 2005;438(7065):201–4.

28. Gleason SL, Gim Y, Byrum T, Kogar A, Abbamonte P, Fradkin E, et al. Structural contributions to the pressure-tuned charge-density-wave to superconductor transition inZrTe3: Raman scattering studies. Phys Rev B Condens Matter Mater Phys. 2015;91(15).

29. Kannappan P, Dhanasekaran R. Studies on structural and optical properties of ZnSe and ZnSSe single crystals grown by CVT method. J Cryst Growth. 2014;401:691–6.

30. Kaur G, Shailja, Negi P, Konwar RJ, Kumar H, Devi N, et al. Structural, optical, and electrical characteristics of anatase titanium dioxide tailored by doping of nitrogen and copper ions. Ceram Int. 2024;50(16):27710–20.

31. Empante TA, Martinez A, Wurch M, Zhu Y, Geremew AK, Yamaguchi K, et al. Low resistivity and high breakdown current density of 10 nm diameter van der Waals TaSe3 nanowires by chemical vapor deposition. Nano Lett. 2019;19(7):4355–61.

32. Nagata S, Ebisu S, Aochi T, Kinoshita Y, Chikazawa S, Yamaya K. Superconductivity in the filamentary conductor TaSe3. J Phys Chem Solids. 1991;52(6):761–7.

33. Sambongi T, Yamamoto M, Tsutsumi K, Shiozaki Y, Yamaya K, Abe Y. Superconductivity in one-dimensional $TaSe_3$. J Phys Soc Jpn. 1977;42(4):1421–2.

34. Sambongi T, Yamamoto M, Tsutsumi K, Shiozaki Y, Yamaya K, Abe Y. Superconductivity in one-dimensional $TaSe_3$. J Phys Soc Jpn. 1977;42(4):1421–2.

35. Yamamoto M. Superconducting properties of $TaSe_3$. J Phys Soc Jpn. 1978;45(2):431–8.

36. Gaurav A, Beura R, Kumar JS, Thangadurai P. Study on the effect of copper ion doping in zinc oxide nanomaterials for photocatalytic applications. Mater Chem Phys. 2019;230:162–71.

37. Hyun J, Jeong MY, Jung MC, Lee Y, Kim Y, Jung S, et al. Strain-controlled evolution of electronic structure indicating topological phase transition in the quasi-one-dimensional superconductor TaSe3. Phys Rev B. 2022;105(11).

38. Steinhögl W, Schindler G, Steinlesberger G, Engelhardt M. Size-dependent resistivity of metallic wires in the mesoscopic range. Phys Rev B Condens Matter. 2002;66(7).

39. Hooda MK, Tripathi TS, Yadav CS. Semiconducting nature and thermal transport studies of ZrTe3. J Alloys Compd. 2019;785:603–9.

40. Wei X, Wang S, Zhang N, Li Y, Tang Y, Jing H, et al. Single-orientation epitaxy of quasi-1D tellurium nanowires on M-plane sapphire for highly uniform polarization sensitive short-wave infrared photodetection. Adv Funct Mater. 2023;

41. Joensen P, Frindt RF, Morrison SR. Single-layer MoS2. Mater Res Bull. 1986;21(4):457–61.

42. Chhowalla M, Shin HS, Eda G, Li LJ, Loh KP, Zhang H. The chemistry of two-dimensional layered transition metal dichalcogenide nanosheets. Nat Chem. 2013;5(4):263–75.

43. Zha J, Tong J, Huang H, Xia Y, Dong D, Tan C. A Perspective on tellurium-based optoelectronics. Appl Phys Lett. 2024;125(7).

44. He Z, Yang Y, Liu JW, Yu SH. Emerging tellurium nanostructures: controllable synthesis and their applications. Chem Soc Rev. 2017;46(10):2732–53.

45. Wisse E, De Zanger RB, Jacobs R, McCuskey RS. Scanning electron microscope observations on the structure of portal veins, sinusoids and central veins in rat liver. Scan Electron Microsc. 1983;(Pt 3):1441–52.

46. Venkatesh R, Dhas CR, Sivakumar R, Dhandayuthapani T, Subramanian B, Sanjeeviraja C, et al. Tailoring the physical properties and electrochromic performance of nebulizer spray coated Co3O4 films through copper doping. Solid State Ion. 2019;334:5–13.

47. Sampath S, Ramanaiah KV. Electrical, electromechanical and thermal properties of thin tellurium films. Bull Mater Sci India. 1985;7(1):63–9.

48. Liang H, Su J, Wan S, Wang Q, Xia J, Wang Z, et al. Two-dimensional tellurium nanosheet: A novel sensitive and stable surface-enhanced Raman scattering substrate. Surf Interfaces. 2024;48(104351):104351.

49. Lee C, Wei X, Kysar JW, Hone J. Measurement of the elastic properties and intrinsic strength of monolayer graphene. Science. 2008;321(5887):385–8.

50. Itkis ME, Nad' FY, Levy F. Energy band structure of the quasi-one-dimensional conductor NbS3. Synth Met. 1991;43(3):3969–72.

51. Du J, Gu X, Fu H, Guo H, Liu J, Wu Q, et al. ITO-induced columnar polycrystalline silicon thin films by CVD. Chem Vap Depos. 2015;21(4-5–6):140–4.

52. Choi IJ, Kim BJ, Lee SH, Jeong BJ, Nasir T, Cho YS, et al. Fabrication of a room-temperature NO2 gas sensor using morphology controlled CVD-grown tellurium nanostructures. Sens Actuators B Chem. 2021;333(128891):128891.

53. Chiu YH, Chung RJ, Kongvarhodom C, Saukani M, Yougbaré S, Chen HM, et al. Facile combination of bismuth vanadate with nickel tellurium oxide for efficient photoelectrochemical catalysis of water oxidation reactions. ACS Appl Mater Interfaces. 2024;

54. Tritt TM, Stillwell EP, Skove MJ. Effect of uniaxial stress on the transport properties of TaSe 3. Phys Rev B. 1986;34.

55. Novoselov KS, Geim AK, Morozov SV, Jiang D, Zhang Y, Dubonos SV, et al. Electric field effect in atomically thin carbon films. Science. 2004;306(5696):666–9.

56. Lipatov A, Wilson PM, Shekhirev M, Teeter JD, Netusil R, Sinitskii A. Few-layered titanium trisulfide (TiS_3) field-effect transistors. Nanoscale. 2015;7(29):12291–6.

57. Yamaya K, Abe Y. Electrical Properties of Ta (Sx Se1-x) 3, Mol. Mol Cryst Liq Cryst. 1982;81:133–40.

58. Gall D. Electron mean free path in elemental metals. J Appl Phys. 2016;119(8).

59. Steinhögl W, Schindler G, Steinlesberger G, Traving M, Engelhardt M. Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller. J Appl Phys. 2005;97(2).

60. Beyne S, Dutta S, Pedreira OV, Bosman N, Adelmann C, De Wolf I, et al. The first observation of p-type electromigration failure in full ruthenium interconnects. In: 2018 IEEE International Reliability Physics Symposium (IRPS). IEEE; 2018. p. 6D.7-1-6D.7-9.

61. Fischer K, Agostinelli M, Allen C, Bahr D, Bost M, Charvat P, et al. Low-k interconnect stack with multi-layer air gap and tri-metal-insulator-metal capacitors for 14nm high volume manufacturing. In: 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM). IEEE; 2015.

62. Mont FW, Zhang X, Wang W, Kelly JJ, Standaert TE, Quon R, et al. Cobalt interconnect on same copper barrier process integration at the 7nm node. In: 2017 IEEE International Interconnect Technology Conference (IITC). IEEE; 2017.

63. Zhang X, Huang H, Patlolla R, Wang W, Mont FW, Li J, et al. Ruthenium interconnect resistivity and reliability at 48 nm pitch. In: 2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC). IEEE; 2016.

64. Wen LG, Adelmann C, Pedreira OV, Dutta S, Popovici M, Briggs B, et al. Ruthenium metallization for advanced interconnects. In: 2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC). IEEE; 2016.

65. Dutta S, Moors K, Vandemaele M, Adelmann C. Finite size effects in highly scaled ruthenium interconnects. IEEE Electron Device Lett. 2018;39(2):268–71.

66. Liu G, Zhang EX, Liang CD, Bloodgood MA, Salguero TT, Fleetwood DM, et al. Total-ionizing-dose effects on threshold switching in 1T -TaS2 charge density wave devices. IEEE Electron Device Lett. 2017;38(12):1724–7.

67. Yang X, Zhou Y, Wang M, Bai H, Chen X, An C, et al. Pressure induced superconductivity bordering a charge-density-wave state in NbTe4 with strong spin-orbit coupling. Sci Rep. 2018;8(1).

68. Perucchi A, Degiorgi L, Berger H. Infrared signature of the charge-density-wave gap in ZrTe3. Eur Phys J B. 2005;48(4):489–93.

69. Yu X, Wen X, Zhang W, Yang L, Wu H, Lou X, et al. Fast and controlled growth of two-dimensional layered $ZrTe_3$ nanoribbons by chemical vapor deposition. CrystEngComm. 2019;21(37):5586–94.

70. Pant A, Torun E, Chen B, Bhat S, Fan X, Wu K, et al. Strong dichroic emission in the pseudo one dimensional material ZrS_3. Nanoscale. 2016;8(36):16259–65.

71. Tang F, Ren Y, Wang P, Zhong R, Schneeloch J, Yang SA, et al. Three-dimensional quantum Hall effect and metal–insulator transition in ZrTe5. Nature. 2019;569(7757):537–41.

72. Zhu X, Lv B, Wei F, Xue Y, Lorenz B, Deng L, et al. Disorder-induced bulk superconductivity in ZrTe3single crystals via growth control. Phys Rev B Condens Matter Mater Phys. 2013;87(2).

73. Yadav CS, Paulose PL. Superconductivity at 5.2 K in $ZrTe_3$polycrystals and the effect of Cu and Ag intercalation. J Phys Condens Matter. 2012;24(23):235702.

74. Felser C, Finckh EW, Kleinke H, Rocker F, Tremel W. Electronic properties of ZrTe3. J Mater Chem. 1998;8(8):1787–98.

75. Takahashi S, Sambongi T, Brill JW, Roark W. Transport and elastic anomalies in ZrTe3. Solid State Commun. 1984;49(11):1031–4.

76. Liu G, Rumyantsev S, Bloodgood MA, Salguero TT, Shur M, Balandin AA. Low-frequency electronic noise in quasi-1D $TaSe_3$ van der Waals nanowires. Nano Lett. 2017;17(1):377–83.

77. Pokhrel D, Bastola E, Phillips AB, Heben MJ, Ellingson RJ. Aspect ratio controlled synthesis of tellurium nanowires for photovoltaic applications. Mater Adv. 2020;1(8):2721–8.

78. Mohanty P, Park J, Kim B. Large scale synthesis of highly pure single crystalline tellurium nanowires by thermal evaporation method. J Nanosci Nanotechnol. 2006;6(11):3380–3.

79. Wang Q, Li GD, Liu YL, Xu S, Wang KJ, Chen JS. Fabrication and growth mechanism of selenium and tellurium nanobelts through a vacuum vapor deposition route. J Phys Chem C Nanomater Interfaces. 2007;111(35):12926–32.

80. Qin JK, Liao PY, Si M, Gao S, Qiu G, Jian J, et al. Raman response and transport properties of tellurium atomic chains encapsulated in nanotubes. Nat Electron. 2020;3(3):141–7.

81. Du Y, Qiu G, Wang Y, Si M, Xu X, Wu W, et al. One-dimensional van der Waals material tellurium: Raman spectroscopy under strain and magneto-transport. Nano Lett. 2017;17(6):3965–73.

82. Zhu H, Chen J, Fan L, Liu H, Wei Q, Hu M, et al. Photoelectric properties of tellurium nanowires by a green thermal solvothermal method. Mater Express. 2022;12(3):511–7.

83. Liu H, Zhu H, Chen L, Shen Y, Wang K, Jin Z, et al. Enhanced intrinsic electrical properties in twisted tellurium nanowires. ACS Appl Electron Mater. 2024;

84. Qian Y, Huang S, Bai Y, Chen J, Zhang L, Guang W, et al. Growth of single-walled carbon nanotubes from tellurium nanoparticles by alcohol CVD. Chem Vap Depos. 2010;16(4–6):136–42.

85. Selamneni V, Sahatiya P. Stacked 1D tellurium nanowires/paper based pressure sensor with laser assisted patterned PDMS encapsulation. In: 2021 IEEE International Flexible Electronics Technology Conference (IFETC). IEEE; 2021.

86. Burducea I, Mateescu AO, Mateescu G, Ionescu C, Straticiuc M, Craciun LS, et al. AFM, RBS and tribological properties of WC/WS2 nanostructures after 1.5 MeV Nb+ implantation. Nucl Instrum Methods Phys Res B. 2019;450:357–60.

87. Bhandari J, Rivallin P, Vinet M, Poiroux T, Barnes JP, Previtali B, et al. Implantation through HfO_2: Calibration of simulation and study on hf behavior during implant. In: Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials. The Japan Society of Applied Physics; 2008.

88. Ionescu M, Atanacio A, Davies J, Nowotny J, Gregg D, Vance L, et al. Surface modifications of TiO_2 by ion implantation. Mater Sci For. 2014;783–786:1674–9.

89. Wei T, Zhang Y, Xu A, Gregg DJ, Karatchevtseva I, Kong L, et al. Surface evolution and radiation damage of a zirconolite glass-ceramic by Au ion implantation. Appl Surf Sci. 2019;478:373–82.

90. Voigt I, Ionasec RI, Georgescu B, Boese J, Brockmann G, Hornegger J, et al. Computational decision support for percutaneous aortic valve implantation. In: Lecture Notes in Computer Science. Berlin, Heidelberg: Springer Berlin Heidelberg; 2010. p. 247–56.

91. Jones DC, Ion Beam Modification and Analysis Laboratory, Department of Physics, University of North Texas, Denton, Texas 76203, USA, Young JM, Lakshantha WJ, Singh S, Byers TA, et al. Redistribution of nickel ions embedded within indium phosphide via low energy dual ion implantations. J Nucl Phys Mater Sci Radiat Appl. 2018;6(1):9–15.

92. Li S, Zhang H, Ruan H, Cheng Z, Yao Y, Zhuge F, et al. Programmable nucleation and growth of ultrathin tellurium nanowires via a pulsed physical vapor deposition design. Adv Funct Mater. 2023;2211527.

93. Jiang W, Wang X, Chen Y, Wu S, Wu B, Yang X, et al. End-bonded contacts of tellurium transistors. ACS Appl Mater Interfaces. 2021;13(6):7766–72.

94. Yang S, Chen B, Qin Y, Zhou Y, Liu L, Durso M, et al. Highly crystalline synthesis of tellurene sheets on two-dimensional surfaces: Control over helical chain direction of tellurene. Phys Rev Mater. 2018;2(10).

95. Peng M, Xie R, Wang Z, Wang P, Wang F, Ge H, et al. Blackbody-sensitive room-temperature infrared photodetectors based on low-dimensional tellurium grown by chemical vapor deposition. Sci Adv. 2021;7(16):eabf7358.

96. Xu M, Xu J, Luo L, Wu M, Tang B, Li L, et al. Hydrogen-assisted growth of one-dimensional tellurium nanoribbons with unprecedented high mobility. Mater Today Kidlington. 2023;

97. Qin JK, Liao PY, Si M, Gao S, Qiu G, Jian J, et al. Raman response and transport properties of tellurium atomic chains encapsulated in nanotubes. Nat Electron. 2020;3(3):141–7.

98. Gleason SL, Gim Y, Byrum T, Kogar A, Abbamonte P, Fradkin E, et al. Structural contributions to the pressure-tuned charge-density-wave to superconductor transition inZrTe3: Raman scattering studies. Phys Rev B Condens Matter Mater Phys. 2015;91(15).

99. Roucau C, Ayroles R, Monceau P, Guemas L, Meerschaut A, Rouxel J. Electron diffraction and resistivity measurements on the one-dimensional orthorhombic and monoclinic structures of TaS3. comparison with NbSe3. Phys Status Solidi Appl Res. 1980;62(2):483–93.

100. Jariwala D, Sangwan VK, Lauhon LJ, Marks TJ, Hersam MC. Emerging device applications for semiconducting two-dimensional transition metal dichalcogenides. ACS Nano. 2014;8(2):1102–20.

101. Sivakumar A, Dhas SSJ, Sivaprakash P, Manivannan M, Kumar RS, Almansour AI, et al. Tuning of electrical conductivity of lithium sulfate induced by dynamic shock waves. Ion Kiel. 2022;28(12):5389–94.

102. Monceau P. Electronic crystals: an experimental overview. Adv Phys. 2012;61(4):325–581.

103. He Q, Liu Y, Tan C, Zhai W, Nam GH, Zhang H. Quest for p-type two-dimensional semiconductors. ACS Nano. 2019;13(11):12294–300.

104. Fischer K, Agostinelli M, Allen C, Bahr D, Bost M, Charvat P, et al. Low-k interconnect stack with multi-layer air gap and tri-metal-insulator-metal capacitors for 14nm high volume manufacturing. In: 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM). IEEE; 2015.

105. Chu PK. Special Issue on Semiconductor Nanowires. Mater Sci Eng R Rep. 2010;

106. Calavalle F, Suárez-Rodríguez M, Martín-García B, Johansson A, Vaz DC, Yang H, et al. Gate-tuneable and chirality-dependent charge-to-spin conversion in tellurium nanowires. Nat Mater. 2022;21(5):526–32.