Title

Test of a 32-Channel Prototype ASIC for Photon Counting Application

Authors

Chen, Y
Cui, Y
O'connor, P
et al.

Publication Date

2015

DOI

10.1109/nssmic.2015.7582272

Peer reviewed

HHS Public Access

Author manuscript

IEEE Nucl Sci Symp Conf Rec (1997). Author manuscript; available in PMC 2017 June 15.

Published in final edited form as:

IEEE Nucl Sci Symp Conf Rec (1997). 2015 ; 2015: .

Test of a 32-channel Prototype ASIC for Photon Counting Application

Y. Chen,
Brookhaven National Laboratory, Upton, NY 11973, USA

Key Laboratory of Particle & Radiation Imaging (Tsinghua University), Ministry of Education, Beijing, 100084, China (yu-chen12@mails.tsinghua.edu.cn). He is also with Department of Engineering Physics, Tsinghua University, Beijing, 100084 China.

Y. Cui [Member, IEEE],
Brookhaven National Laboratory, Upton, NY 11973, USA

P. O'Connor [Member, IEEE],
Brookhaven National Laboratory, Upton, NY 11973, USA

Y. Seo,
University of California, San Francisco, San Francisco, CA 94143
(youngho.seo@radiology.ucsf.edu)

G. S. Camarda [Member, IEEE],
Brookhaven National Laboratory, Upton, NY 11973, USA

A. Hossain [Member, IEEE],
Brookhaven National Laboratory, Upton, NY 11973, USA

U. Roy [Member, IEEE],
Brookhaven National Laboratory, Upton, NY 11973, USA

G. Yang [Member, IEEE], and
Brookhaven National Laboratory, Upton, NY 11973, USA

R. B. James [Fellow, IEEE]
Brookhaven National Laboratory, Upton, NY 11973, USA

Abstract

A new low-power application-specific integrated circuit (ASIC) for Cadmium Zinc Telluride (CZT) detectors for single-photon emission computed tomography (SPECT) application is being developed at BNL. As the first step, a 32-channel prototype ASIC was designed and tested recently. Each channel has a preamplifier followed by CR-RC^3 shaping circuits and three independent energy bins with comparators and 16-bit counters. The ASIC was fabricated with TSMC 0.35-μm complementary metal–oxide–semiconductor (CMOS) process and tested in laboratories. The power consumption is around 1 mW/ch with a 2.5-V supply. With a gain of 400 mV/fC and the peaking time of 500 ns, the equivalent noise charge (ENC) of 360 e- has been

(phone: 631-344-5351; ycui@bnl.gov)

measured in room temperature while the crosstalk rate is less than 0.3%. The 10-bit DACs for global thresholds have an integral nonlinearity (INL) less than 0.56% and differential nonlinearity (DNL) less than 0.33%. In the presentation, we will report the detailed test results with this ASIC.

Index Terms

Test; low-power ASIC; CZT; Photon Counting; Multi-channel

I. Introduction

Room-temperature semiconductor radiation detectors, such as Cadmium Zinc Telluride (CZT) have been used in medical imaging systems such as Single-photon Emission Computer Tomography (SPECT) for their high energy-resolution and compactness. Pixelated CZT detectors with photon-counting measurements can obtain good special resolutions and efficiency [1], but require high density of readout channels.

Recently we have designed a 32-channel low-power application specific integrated circuit (ASIC) for the photon counting applications, which has been reported last year. Each channel contains analog front-end circuits, three independent window-comparators with six adjustable thresholds, together with associated 16-bit counters. The chip is fabricated by TSMC 0.25-μm CMOS process under 2.5-V power supplies. The chip area is 4.903 × 2.502 mm^2, as is shown in Fig. 1. In this paper, we summarize the tested results with the chip as well as proposed improvements in the future revision.

II. Test setups

We have set up a test systems based on the ASIC test board and a PC DAQ program, as is shown in Fig. 2. The test board (Fig. 3) contains a USB chip - Cypress EX-USB® FX2 for communication. The counting results of all the channels were first stored on board and then transmitted to the PC via a USB cable. A LabVIEW® program was used to monitor the result as well as configure the parameters of the ASIC.

A detailed structure of a signal channel configuration is shown in Fig. 4. The step pulses generated by a Tektronix® pulse generator with amplitude of ΔV and frequency of 10 kHz are injected via the “TestIN” pin and AC-coupled to every channel via an on-chip capacitor C_c = 100 fF, emulating a total input charge Q = $C_c\Delta V$. At the “IN” pin of each channel, a BAS321 diode was added to simulate the leak current I_{leak} = 4 nA as well as the capacitor C_d = 0.6 pF of the detector. By default, within a period of 100ms, the USB controller acquired counting results from three energy regions inside every channel and then reset the counters. To test the performance of the front end circuits in each channel, the analog waves were monitored via the “AnalogOUT” pin and measured by a Tektronix® oscilloscope.

III. Experimental Results

A. Gain and output waveforms

Fig. 5 shows the waveforms of input and output signals. The comparators and DDL module will pick out the signals with amplitude in certain energy window and generate a square pulse to the related counter. The undershoot at the tail of the analog out is due to the fast tailing edge of input test pulses.

Fig. 6 shows the peak amplitude of analog output pulses according to the equivalent input charges. Four different gains are designed to enlarge the dynamic range up to at least 20 fC. Thanks to the precise pole-zero cancellation of the continuous reset pre-amplifier we used in our chip [2], the linearity of the front-end channel is excellent before the output signal approaches the power rail.

The gain variation between channels was measured. Eight channels, located at the top, center and bottom of the chip, are shown in Fig. 7. The maximum difference between all the channels is less than 10 mV/fC and can be compensated by a 4-bit fine-gain adjustment in each channel. As we used CR-$(RC)^3$ architecture in shaping circuit, the charge gain when peaking time T_{sh} = 500 ns is larger than that of T_{sh} = 200 ns.

B. Current-steering DAC for threshold setting

The ASIC consists of 6 10-bit current-steering digital-to-analog converters (DACs) to generate the threshold voltage for all channels, forming three energy regions for photon counting among different energy windows. A segmented architecture [3] is used in the current-steering arrays for a tradeoff between linearity and chip area. The Fig. 8 shows the measured differential nonlinearity (DNL) in LSBs. The large DNL occurs at every 32 digits due to the mismatch between the lower 5-bit current array and the higher 5-bit one, which can be improved by better layout in future revision. However in the photon counting application, the nonlinearity is not critical as each channel has a 3-bit DAC to trim each threshold voltage, which will be described in the following. Measured by the full scale of DAC output, the DNL is 0.33% and the integral nonlinearity (INL) is 0.56%.

C. Counting performance of each channel

The counting performance was measured by the following method. The frequency of the input signals and the acquisition time were fixed to 10 kHz and 100 ms respectively. By increasing the threshold while fixing the input amplitude, we obtained as shown in Fig. 9. By fitting the S-shape curves with integral of Gaussian function (solid curves in Fig. 9), we determined the noise level in measured channels. Channel 0 has a much larger noise as expected due to extra monitoring circuits. Beside of that, the maximum standard deviation among the rest channels is 23.03 mV, related to 362 e^- ENC with a gain of 396 mV/fC. The larger noise level than expected mainly results from the oscillation on the baseline due to the instability of the baseline holder we used and will be improved in our future design.

It could be found that there occurs a big difference on the real threshold voltage due to the mismatch between channels, which would seriously affect the performance in such a multi-

channel system. The fine-gain adjustment with a local 3-bit DAC in each channel is implemented to compensate the difference and the final results after tuning are shown in Fig. 10. The maximum variance of the threshold voltage is not more than 16.29 mV, smaller than the noise level.

When shaping time is 500 ns, it has been tested that the chip is able to achieve a counting rate of 600 kHz with an error less than 0.1%, which matches the design specifications of the ASIC.

D. Power consumption

With a 2.5-V power supply, the current consumed by all 32 channels together with bias circuits is 13.31 mA, leading to a power consumption of 1.04 mW per channel. This meets the low-power requirement of our ASIC.

In the test, the current-steering DACs were biased at a total current of 1.692 mA. However, this current doesn't depend on the number of channels and will contribute much less to the total current in the next 128-channel version of the ASIC.

E. Crosstalk

Under the maximum gain of 396 mV/fC, we injected pulses equivalent of 6 fC into one channel to maximize the amplitude of output pulses into the saturation region. Then for all the adjacent channels, no output signals above the noise level were picked out. By setting the threshold below the noise level, we measured the average count of these adjacent channels less than 30 in 100 ms, indicating a crosstalk smaller than 0.3%.

IV. Summary and Future Work

We have designed and tested a low-power 32-channel ASIC for photon counting applications in SPECT systems. The performance of the chip is summarized in Table I. Apart from the noise performances, all the other properties have met the design requirements, especially the low power consumption, low crosstalk rate and small variations of counting performance between each channel after calibration, which indicates the possibility for the integration of more channels into one signal chip. A 128-channel version of the chip is being fabricated. Electronics test and detector test results will be reported later.

Acknowledgments

This work was supported by U.S. Department of Health & Human Service, National Institute of Health Grant #R01 EB012965. The manuscript has been authored by Brookhaven Science Associates, LLC under Contract No. DE-AC02-98CH10886 and DE-SC0012704 with the U. S. Department of Energy. This work was also supported by China Scholarship Council (File No. 201406210171).

References

1. De Geronimo G, Dragone A, et al. ASIC with Multiple Energy Discrimination for High-rate Photon Counting Application. IEEE Trans. Nuclear Science. Oct; 2007 54(2):303–312.
2. De Geronimo G, O'Connor P. A CMOS detector leakage current self-adaptable continuous reset system: Theoretical analysis. Nucl. Intrum. Methods Phys. Res. A. 1999; 421(1-2):322–333.

3. Van den Bosch A, Borremans MAF, et al. A 10-bit 1GSample/s Nyquist Current-Steering CMOS D/A converter. IEEE J. Solid-State Circuits. Oct; 2001 36(3):315–324.

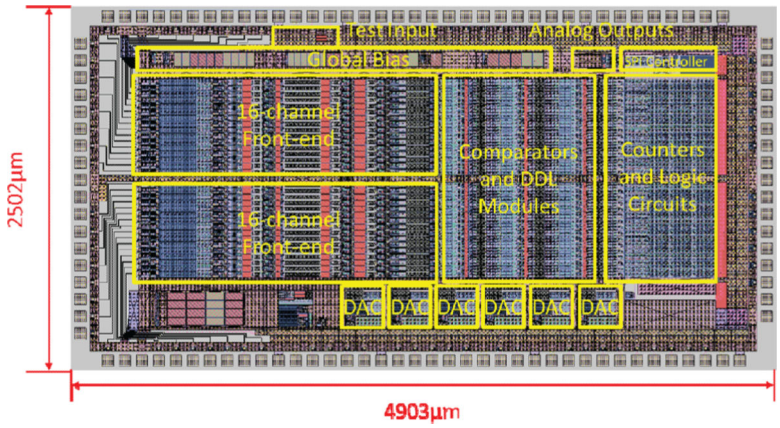

Fig. 1.
Layout and general structures of 32-channel ASIC.

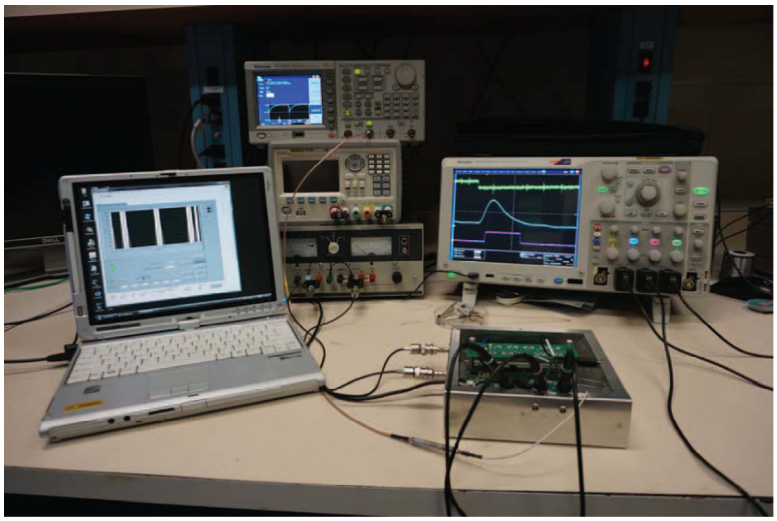

Fig. 2.
Configuration of the whole multi-channel ASIC test system.

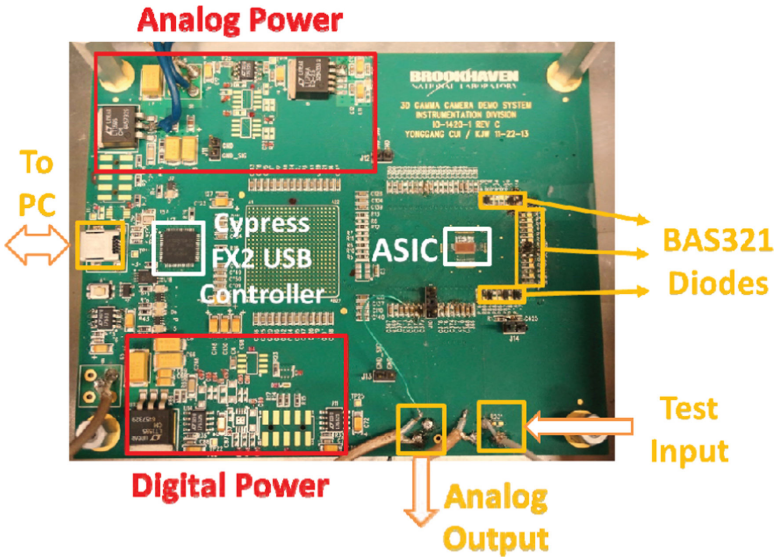

Fig. 3.
Layout of the ASIC test PCB board.

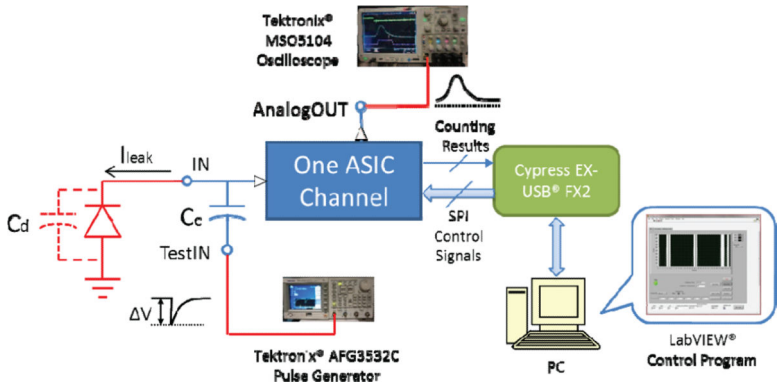

Fig. 4.
Signaling pathway of each ASIC cannel.

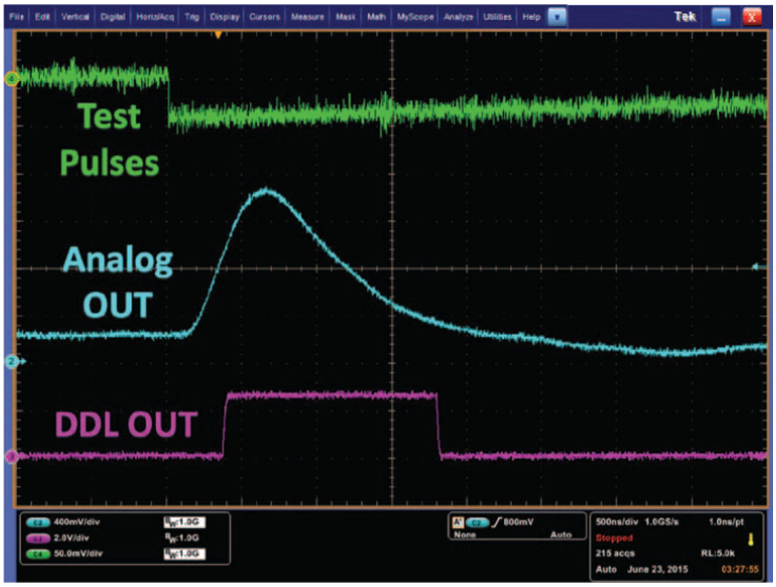

Fig. 5.
Waveforms captured by the oscilloscope.

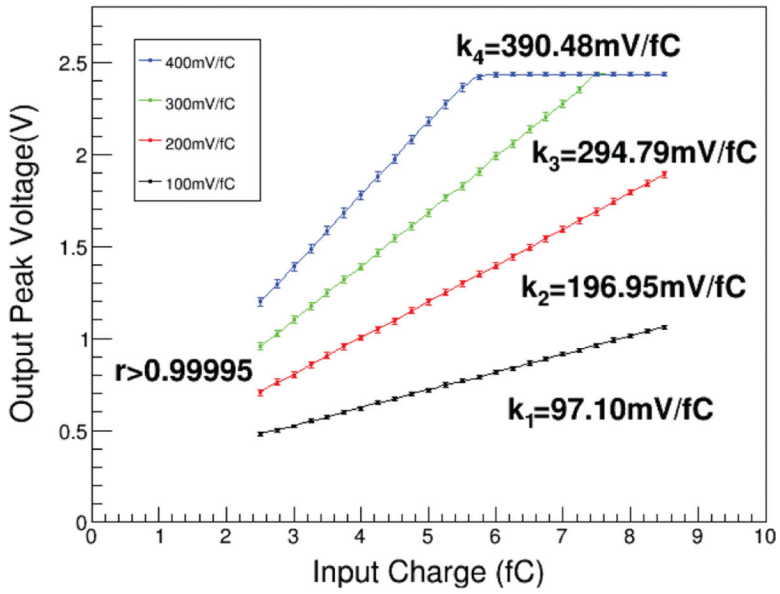

Fig. 6.

The output peak voltage of the front-end signals measured by the oscilloscope. Peaking time was set 500 ns. The ASIC is designed to have 4 different gains. The curve statures when the peak voltage approached 2.5 V, the power voltage.

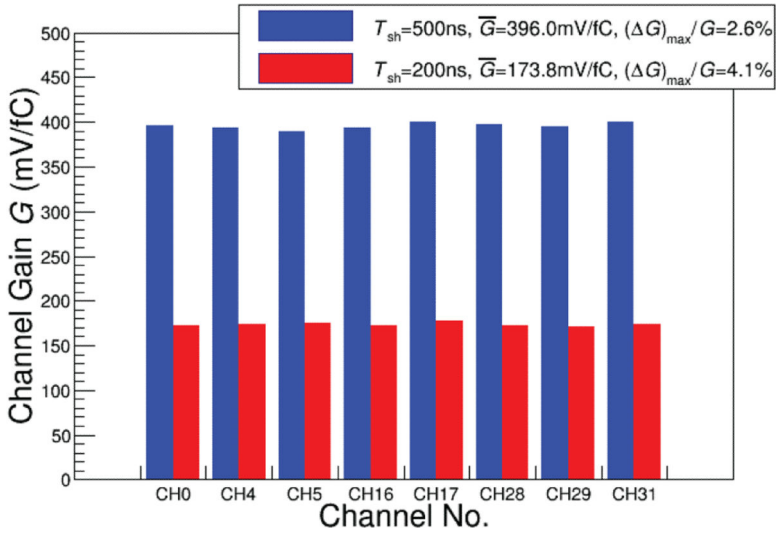

Fig. 7.

The differences of the gains between 8 critical channels. The 400 mV/fC gain was used. The gain is about 2.5 time larger with peaking time of 500 ns than with 200 ns due to the shaping circuits deployed.

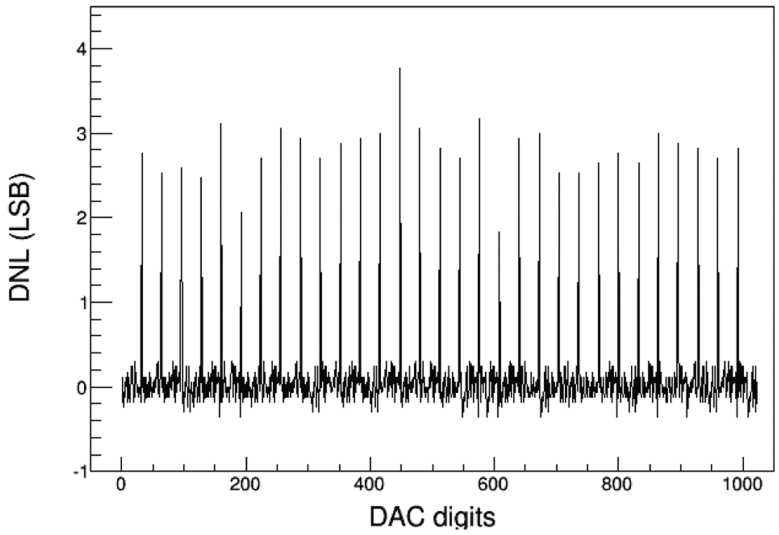

Fig. 8.

The DNL of the 10-bit DAC for global threshold setting. Big values occur every 32 digits due to the mismatch between the higher 5-bit current array and the lower 5-bit one, which can be compensated by the local DAC in each channel.

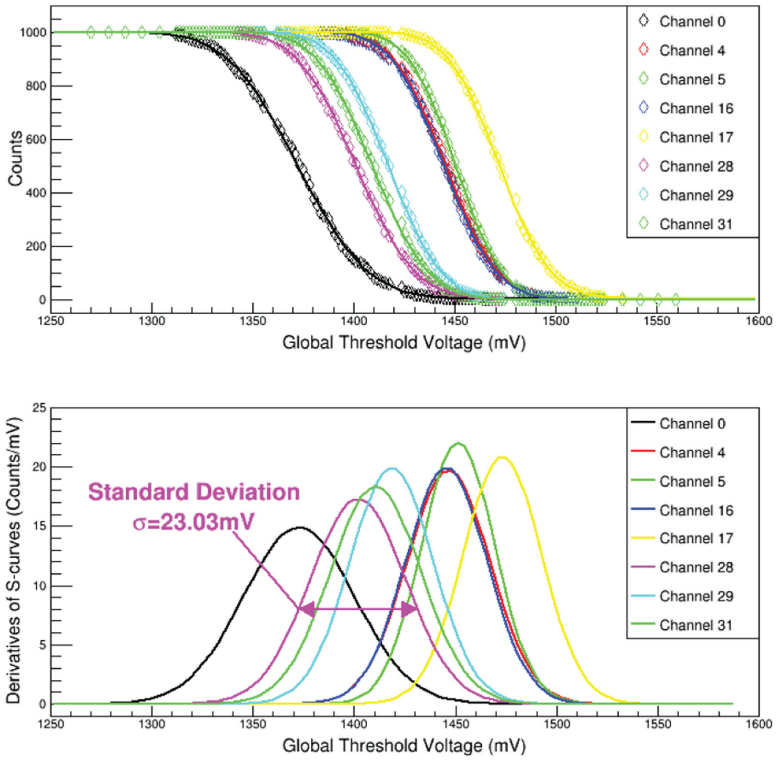

Fig. 9.

S-curves of 8 channels before compensations. The solid curve is the fitting curve using the integration of a Gaussian function. A much larger noise level in Channel 0 results from several extra monitoring circuits for tests.

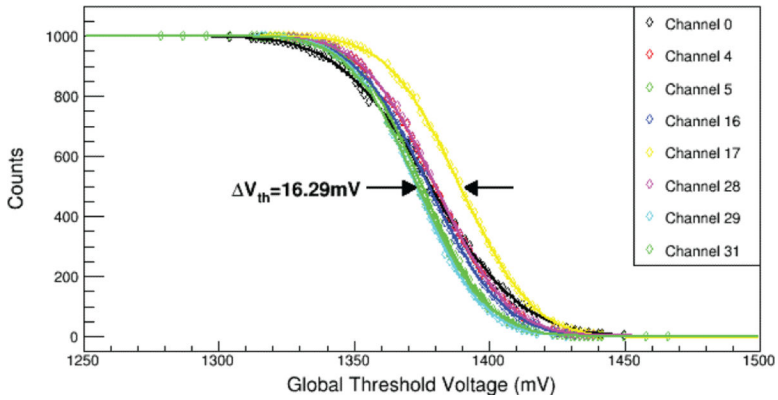

Fig. 10.
S-curves after gain and threshold voltage compensations.

Table I

Parameters Summary of the ASIC

Parameters	Designed Value	Measured Value
No. of channels	32	--
Process	0.25-μm CMOS	--
Area (μm × μm)	4903 × 2503	--
Power (per Channel)	1 mW	1.04 mW
Dynamic Range	10 fC	>20 fC
Maximum Gain	400 mV/fC	396 mV/fC
ENC (e-)	200	362
Crosstalk	1%	<0.3%
Counting Rate	500 kHz	>600 kHz