Title

High-Performance Grid-Tied Single-Phase Power Converter Design with Applications in Electric Vehicle Charging and Residential Photovoltaic Systems

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High-Performance Grid-Tied Single-Phase Power Converter Design with Applications in Electric Vehicle Charging and Residential Photovoltaic Systems

By

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Associate Professor Robert Pilawa-Podgurski, Chair
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High-Performance Grid-Tied Single-Phase Power Converter Design with Applications in Electric Vehicle Charging and Residential Photovoltaic Systems

Abstract

High-Performance Grid-Tied Single-Phase Power Converter Design with Applications in Electric Vehicle Charging and Residential Photovoltaic Systems

By

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Doctor of Philosophy in Engineering — Electrical Engineering and Computer Sciences

University of California, Berkeley

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Single-phase power converters enable people to connect any electronic device to the ac grid. As the electricity demand of our world continues to grow, it is crucial to continually research and develop novel power electronic technologies that have improved performance. Specifically, traits of minimal power loss, high volumetric power density, high gravimetric power density, high levels of reliability, and long lifetimes are desired.

In the first part of this thesis, a novel two-stage power converter design is proposed for the application of level-2 electric vehicle on-board charging. For the ac-to-dc rectification stage, a hybrid-switched capacitor converter, which utilizes the ultra-high energy densities of class two ceramic capacitors to minimize the passive component sizing of the converter, is proposed. For the energy buffer stage of the on-board charger, an active buffer topology that minimizes the system's physical volume and weight without compromising efficiency is presented. The active buffer topology in the electric vehicle charger is further investigated, with a novel control and circuit topology introduced that significantly reduces any voltage and current ripple along the dc-link.

In the second part of this thesis, a novel two-stage inverter solution is proposed for a residential microinverter. The inverting stage of the microinverter is divided into two parts: a step-up stage and an inverting stage. Both parts are implemented with hybrid switched-capacitor converter topologies to (1) reduce system volume through leveraging the high energy densities of capacitors and (2) increase system efficiency by utilizing lower voltage switches with high figures of merit and soft-switching techniques. The passive component volume and switching stress of the step-up stage are theoretically analyzed and compared to other converter topologies, showcasing it as a practical converter choice for the microinverter application space. This two-part inverting stage creates a high voltage dc bus where the energy buffer can be placed in the system. This reduces the required buffer capacitance,

enabling the engineer to have a broader range of capacitor choices to design a more reliable and energy-dense system.

Overall, this thesis showcases the design and utilization of several hybrid switched-capacitor converters, active buffer topologies, and control in the single-phase application area. Modeling and theoretical analysis techniques of power converter volume and power stress are explained in detail. High-performance hardware prototypes, experimental results, and test setup designs are included.

To my family and friends.
A mi familia y amigos.

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Acknowledgments

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Chapter 1

Introduction

1.1 Introduction

This thesis focuses on two specific applications of single-phase converters. In the first part, level-2 electric vehicle charging is examined. A novel hybrid switched-capacitor converter is proposed for the power factor correction stage, and an active buffer solution is offered for the energy buffer stage. Following this section, suggestions for improvement of the energy buffer stage, which reduces any current and voltage ripple along the dc-link, are given. In the second part of this thesis, a novel two-stage inverting system is proposed for the application area of microinverters. A passive component and switching stress analysis is completed to motivate the selection of the converter topology of the first stage, followed by a detailed description of the entire system solution. High-performance hardware prototypes and experimental results are showcased in this manuscript.

1.2 Organization of Thesis

Chapter 2: Fundamentals of Power Converters in Single-Phase Systems

Single-phase power conversion systems require a power converter to rectify the ac power sourced by the ac grid to a dc power waveform that is processed by the dc port. This process can also occur by an inverting means, where the power converter must invert the dc power sourced by the dc port to an ac power that meets ac grid regulations. Conventional single-phase power conversion systems have two stages: a power factor correction/inverting stage and a buffer stage that regulates the twice-line frequency power pulsation ripple along the dc bus. Conventional designs for both stages of the single-phase power conversion system are discussed. Suggestions for improvements in their design that offer increased volumetric and gravimetric power densities, increased efficiency, and improved reliability and lifetimes are given.

Part I: Single-Phase Power Conversion for Electric Vehicle Charging Applications

Chapter 3: Electric Vehicle On-Board Charger

Level II electric vehicle (EV) on-board chargers provide ac-dc conversion capability to charge on-board high-voltage (HV) batteries. Bidirectional EV chargers can also allow the EV to act as an ac source in vehicle-to-grid services. Chargers should have high power density, high power-handling capability, and low weight in charging and inverter applications. This chapter showcases the architecture of an optimized bidirectional EV charger system that can convert from both low-line (120 V_{ac}) and high-line (240 V_{ac}) ac voltages to a 400 V_{dc} output. The operation and control of the complete system, thermal management, enhanced power stage design, and start-up procedure are discussed. Experimental results demonstrating dc-ac high power operation and system start-up are reported.

Chapter 4: Series-Stacked Buffer with and without the Charge Injection Method

Single-phase power converter systems require a reactive circuit branch tied to the dc-link. The reactive branch buffers the twice-line frequency power pulsation that couples to the dc bus due to the mismatch in instantaneous power between the dc and ac ports. The Series-Stacked Buffer (SSB) has been presented as an active buffer topology that moderates this reactive power while maintaining a low physical volume and high efficiency. However, the SSB requires additional loss compensation control, producing a residual twice-line frequency ac current and voltage ripple coupled to the dc-link. This chapter proposes hardware and corresponding control that injects charge into the SSB to compensate for losses. This eliminates the twice-line frequency ripple from the dc-link through decoupling the reactive and real power handling. The charge injection technique is verified with an SSB hardware prototype rated for 1.5 kW and 400 V operation.

Part II: Multi-Level Power Converters for Residential Solar Panel Microinverter Applications

Chapter 5: Residential Solar Panel Survey

This chapter presents a survey that examines the open circuit voltage (V_{oc}), the maximum power voltage (V_{mp}), and the rated power levels of many residential solar panels. Basic terminologies for key electrical characteristics in solar panel datasheets used in this survey are defined. The findings of the surveyed material provide voltage and power design requirements for any nominal microinverter system.

Chapter 6: A 1-to-10 Cascaded Series-Parallel Converter

Resonant hybrid switched-capacitor converters (ReSCs) can achieve high efficiency, power density, and power-handling capabilities. However, ReSCs have yet to be widely explored in high-voltage (HV) step-up application areas. This chapter attempts to bridge the gap between ReSCs and the HV step-up application space by proposing a 1-to-10 step-up cascaded series-parallel (CaSP) converter. The principles of operation and functionality of the circuit are discussed and are validated with a hardware prototype. Experimental results are provided up to 300 W and 350 V output, including efficiency and load regulation measurements and zero-current switching (ZCS) demonstration.

Chapter 7: A Two-Stage Multi-level Hybrid Switched-Capacitor Microinverter

This chapter explores using a two-stage architecture for a photovoltaic microinverter that utilizes efficient and compact hybrid switched-capacitor topologies. The first stage is a 1-to-10 step-up Cascaded Series Parallel (CaSP) dc-dc converter. The CaSP stage demonstrates the feasibility of using a fixed-ratio resonant switched-capacitor converter in the microinverter application space. Instead of advanced startup circuitry, the CaSP converter provides a startup sequence for the overall system architecture. The second stage offers voltage regulation and inversion: a flying capacitor multilevel (FCML) converter that converts the intermediate high voltage dc bus that is between 350 V to 400 V, to a 240 V_{rms} ac output. Experimental results validate the system architecture's functionality, highlighting the possibilities of using the CaSP converter in renewable applications.

Chapter 8: Conclusion

This chapter concludes this thesis. Conventional power converter designs for electric vehicle converters and microinverters are discussed, followed by a brief discussion of how system improvements can be made. The proposed power converter systems for these two applications in this thesis are summarized, with experimental and hardware results noted.

Chapter 2

Fundamentals of Power Converters in Single-Phase Systems

2.1 Single-Phase System Architecture

In single-phase power conversion systems, a power converter (shown in Fig. 2.1) is required to convert the ac power waveform provided from the ac grid to a dc power waveform, where the dc load determines the power and dc voltage requirements. In single-phase inverting applications, the power converter operates as an inverting topology, where it inverts the dc power provided by its dc source to required levels for the ac distribution grid [1], [2]. In the United States, the ac voltage supplied by the grid is conventionally either 120 V_{ac} or 240 V_{ac} [3]. There is an abundance of single-phase applications that have strict specifications for the dc port voltage and power levels. For example, in single-phase electric vehicle (EV) charging, the dc load is the car's dc battery, which is typically rated between 400 V_{dc} to 800 V_{dc} and must be charged by power levels rated in the kilowatts [4]–[6]. Another example is residential solar panel inverters, which are commonly referred to as "microinverters," where the low voltage (LV) dc solar panel can be rated up to 60 V_{dc} and can be connected to a

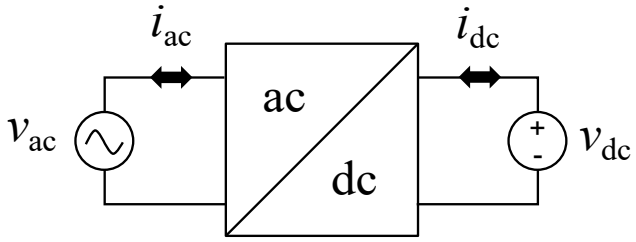


Figure 2.1: A bidirectional single-phase power conversion system. The power converter must either rectify the ac power waveforms to meet the demands of the corresponding dc load or invert the dc energy from the dc source to required levels for the ac distribution grid.

240 V_{ac} grid [7], [8].

A conventional power conversion system has two stages. The first is an ac-to-dc power conversion stage, which handles the power factor correction, or a dc-to-ac inversion stage, pending on the desired application. The second stage is the twice-line frequency energy buffer, which is required to store and release the twice-line frequency power pulsation along the dc-link of the system caused by the instantaneous power mismatch between the ac and dc ports. Figs. 2.2 and 2.3 display the placement of the two stages in a single-phase power

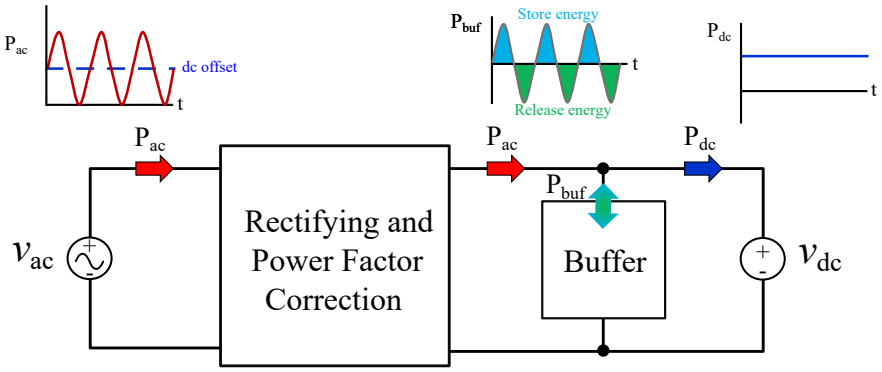


Figure 2.2: A single-phase power conversion system that rectifies the ac power waveform that is supplied by the ac grid to a dc power waveform that meets the electrical specifications of the dc load. The system is encompassed by a power factor correction (PFC) stage that performs the power rectification and a buffering stage that regulates the twice-line frequency power pulsation on the dc port to minimize dc-link voltage and current ripple.

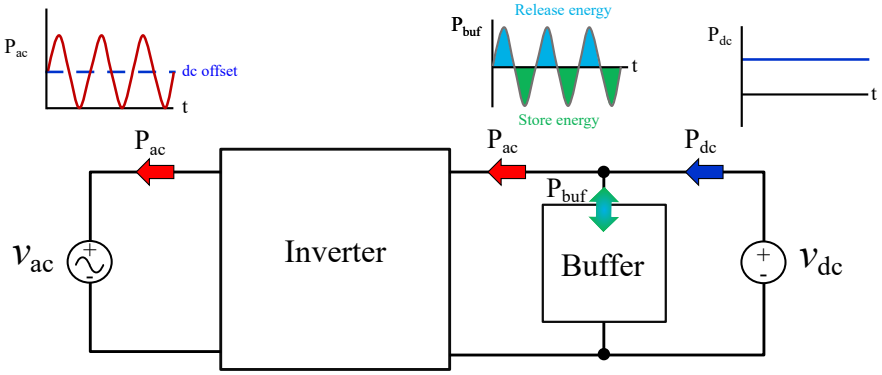


Figure 2.3: A single-phase power conversion system that inverts the dc power waveform that is supplied by a dc source to an ac power waveform that meets the electrical specifications of the local ac distribution grid. The system is encompassed by an inverting stage that performs the power inversion and a buffering stage that regulates the twice-line frequency power pulsation on the dc port to minimize dc-link voltage and current ripple.

conversion system for rectification and inversion systems, respectively, along with the power waveforms that are processed by each port and stage in the system.

Assuming the voltage and current waveforms along the ac port of the system are in phase with one another, the power processed by the ac port can be derived as

$$P_{\text{ac}} = V_{\text{ac}}\sin(\omega_{\text{L}}t) \cdot I_{\text{ac}}\sin(\omega_{\text{L}}t), \tag{2.1}$$

where V_{ac} and I_{ac} are the magnitudes of the ac voltage and current waveforms, respectively, and ω_{L} is the angular frequency of the rated line frequency f_L, which is a rated 60 Hz frequency in the United States. The product in (2.1) can be simplified to

$$P_{\text{ac}} = P_0 - P_0\cos(2\pi f_{2\text{L}}t), \tag{2.2}$$

where P_0 is equal to $\frac{V_{\text{ac}}I_{\text{ac}}}{2}$ and $f_{2\text{L}}$ is $2\times$ the rated lines frequency, which is equal to 120 Hz in the United States.

2.2 Conventional Single-Phase Power Converter Solutions

Power Factor Correction and Inverting Stage

Single-phase power converters can be broken into two separate categories: isolated designs, which utilize a transformer in the PFC/inverting stage that provides galvanic isolation in the system, and non-isolated designs, which have no transformer in the PFC/inverting stage. Noted, for the non-isolated designs, an isolation transformer must be placed elsewhere in the system if required by regulation in the intended application area. This thesis only examines non-isolated designs since they offer higher volumetric and gravimetric energy densities.

In a non-isolated PFC design, there is no transformer. Commonly, the output-to-input voltage gain depends on the converter's duty cycle. In applications where the voltage must be stepped up from the grid, such as in EV charging applications, a two-level boost converter is used as a conventional solution [9]. Similarly, in step-down and step-up-down applications, a two-level buck converter and two-level buck-boost can be used, respectively. Fig. 2.4 shows a two-level step-up power converter utilized in a single-phase power converter application. In this solution, the duty cycle of switch $\text{S}_{1\text{b}}$ determines the gain of the power converter. Unlike a conventional isolated solution, such as the LLC converter [10], [11], the two-level solution utilizes only one magnetic component (L_{boost}, as shown in Fig 2.4) to handle the energy storage and transfer as well as the power factor correction.

Twice-Line Frequency Buffering Stage

Conventionally, a bank of capacitors is used to buffer the twice-line frequency power pulsation along the dc-link of the system. The capacitance requirement is determined by the engineer's

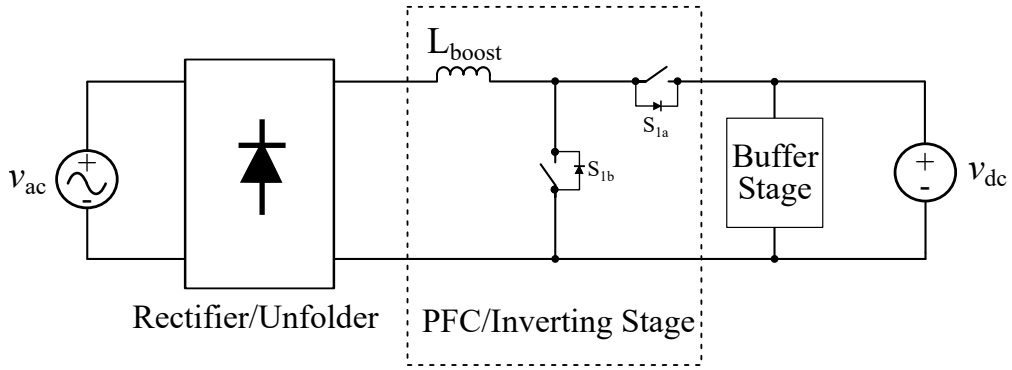


Figure 2.4: A two-level step-up power converter used as the power factor correction and inverting stage in a single-phase system.

desired voltage ripple along the dc-link, as well as the rated power of the system:

$$C_{\text{buffer}} = \frac{P_{\text{sys}}}{2\pi f_{\text{2L}} \cdot v_{\text{dc}} \cdot \Delta v_{\text{dc}}}, \tag{2.3}$$

where P_{sys} is the rated power of the system, v_{dc} is the dc voltage of the dc port, and Δv_{dc} is the desired peak-to-peak voltage ripple of the dc-link [12], [13]. There are several capacitive solutions, and each offers its benefits:

- Multi-layer ceramic capacitors (MLCCs) - Offer low values of ESR and ESL, further improving the system efficiency. Class 2 MLCCs offer high energy density levels [14], [15] but suffer from capacitance derating such that the capacitance decreases with higher dc voltages. Class 1 MLCCs do not experience this derating but offer poorer power density metrics. Ceramic capacitors overall have high reliability and long lifetimes.
- Film capacitors - Offer high precision capacitance, high reliability, long lifetimes, low values of ESR, and can withstand highly rated voltages and currents. However, film capacitors suffer from larger physical volumes and weights than other capacitive solutions.
- Aluminum electrolytic capacitors - Offer high levels of capacitance and energy density, especially between 100 V_{dc} to 800 V_{dc} [14], [15]. However, aluminum electrolytic capacitors suffer from high ESR values, low-reliability levels, and shorter lifetimes [16].

Conventionally, a bank of electrolytic capacitors is used as the twice-line frequency buffering stage due to their high levels of capacitance and both volumetric and gravimetric energy densities [15], specifically in the range of 100 V_{dc} to 800 V_{dc} which are standard voltages for the dc port in a single-phase system.

2.3 Methods for Improvements in Single-Phase Systems

To summarize the previous section, a two-level converter is commonly used as the PFC/inverting stage in a non-isolated single-phase power converter. In addition, a bank of electrolytic capacitors is conventionally used as the twice-line frequency energy buffer stage. The system's passive components dominate the converter's physical volume and weight in this conventional approach. Moreover, the switches used must be rated to block large voltages.

To reduce this conventional solution's physical, volume, and weight, the two-level converter can be replaced with a N-level converter, depicted in Fig. 2.5. Whereas the two-level converter has only two dc voltages present in the system, ground and the dc port voltage, the N-level converter has N dc voltages present in the design, ground, the dc port voltage, and $N-2$ other dc voltages maintained by "flying" capacitors. The capacitors are further utilized for energy storage and transfer, minimizing the power processing requirements of the inductor. Moreover, capacitors have orders of magnitude higher power densities [15] than inductors, allowing the overall passive component volume and weight of the system to be further reduced. To operate the N-level converter, a phase-shifted pulse width modulation technique of the N-level converter decreases the $V \cdot s$ product of the inductor, enabling a lower inductance requirement and lesser amount of filtering elements in the power conversion system [17], [18]. Lastly, as demonstrated in Fig. 2.5, the N-level converter utilizes switches with lower blocking voltages than those used in the two-level converter. Lower voltage switches, specifically GaN, demonstrate superior performance metrics to that of high voltage switches (e.g., on-state resistance, gate charge, output capacitance, etc.), and overall higher figures of merit [19]–[21]. Table 2.1 highlights the critical differences between the two-level and N-level solutions.

Both the physical volume and weight can also be further reduced in the power conversion system by replacing the electrolytic capacitor bank with a buffer that utilizes a combination of capacitive and inductive components, as well as active circuitry, as shown in Fig. 2.6. The buffer in Fig. 2.6, which is tied to a dc source with source impedance $\mathrm{R_s}$ and an inverter modeled by current i_{inv}, utilizes the capacitor shown in the figure to buffer the twice-line frequency power pulsation. However, unlike the electrolytic capacitor bank solution, the capacitor is allowed to have a much larger voltage ripple displaced across it, allowing for reductions in the capacitance requirement. This reduction in capacitance allows for higher volumetric and gravimetric power densities and enables the engineer to use capacitors with longer lifetimes and higher temperature ratings such as MLCCs and film capacitors [16]. The network of active circuitry and additional passive components are controlled such that the the sum of the voltage across the capacitor $\mathrm{C_1}$ and the active network produce a dc voltage, as required by the dc port.

In single-phase power conversion systems where the dc port is rated for a lower voltage, such as in residential microinverter applications, the electrolytic capacitor bank is typically

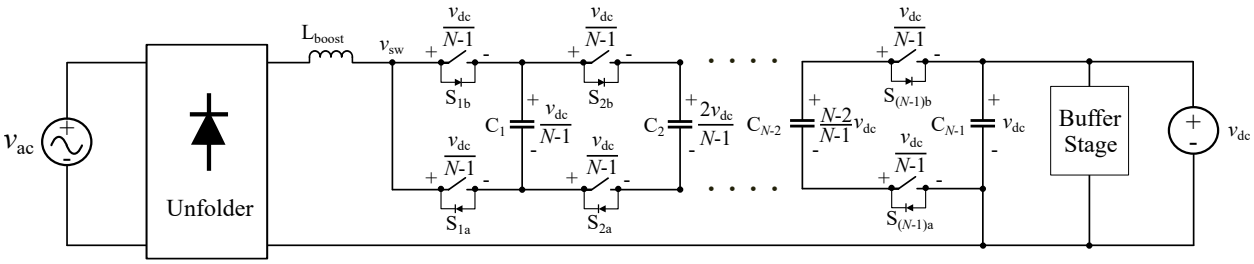


Figure 2.5: An N-level step-up power converter used as the power factor correction and inverting stage in a single-phase system.

Table 2.1: Key differences between a two-level converter and an N-level converter

Parameter	Two-level	N-level
Switch voltage stress	v_{dc}	$\frac{v_{\text{dc}}}{(N-1)}$
Inductor ripple frequency	f_{sw}	$(N\text{-}1)\cdot f_{\text{sw}}$
v_{sw} ripple amplitude	v_{dc}	$\frac{v_{\text{dc}}}{(N-1)}$
Energy storage	Inductive	Capacitive and inductive
Conversion ratio	$\frac{1}{1-D}$	$\frac{1}{1-D}$

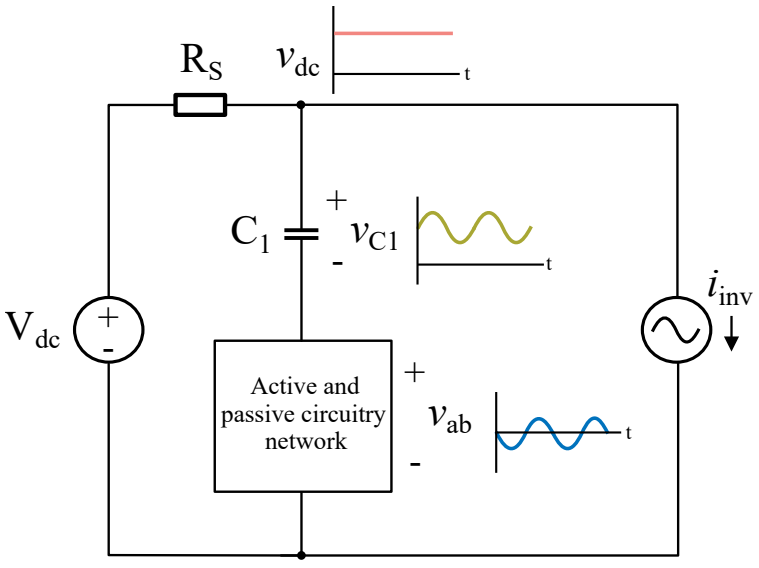


Figure 2.6: An example of an active buffer topology that reduces the capacitance requirement of the buffer stage by utilizing a network of active and passive circuitry in series with C_1.

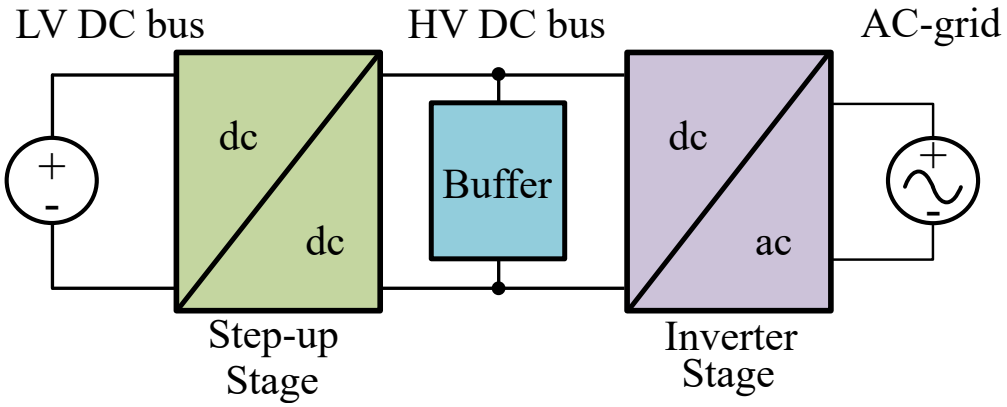


Figure 2.7: An example of separating the inverting/PFC stage into two stages. The engineer can now place the energy buffer across the HV dc bus for low-voltage dc systems, such as residential microinverters, decreasing the capacitance requirement.

also on the low-voltage dc bus, where a more significant amount of current ripple must be buffered due to the low dc-link voltage. As a result, a substantial amount of capacitance is required, therefore not only increasing the volume of the overall system but also forcing the engineer to utilize only electrolytic capacitors, which have even lower lifetimes and reliability in higher temperature environments such as solar applications [22], [23]. Although the active solution, such as in Fig. 2.6, can be applied to reduce the capacitance requirement, a more straightforward and more practical solution would be to place the energy buffer along a high voltage (HV) dc bus. To do so, the regulating inverter stage (or PFC for rectifier systems) can be divided into two stages, a step-up stage and an inverting stage, where the energy buffer is now placed on the HV dc bus between the two stages. Fig. 2.7 shows how the single-stage inverting solution can be divided into two stages. As a result, the capacitance requirement is decreased as described in (2.3), allowing the engineer to select a capacitive solution that has significantly higher volumetric and gravimetric energy densities [14], [15], higher levels of reliability, and longer lifetimes. Moreover, the two-stage solution gives the engineer more options and flexibility for the topological designs of the power conversion stages to make the whole system more compact, reducing manufacturing and shipping costs for large-scale manufacturing.

To illustrate the volume and weight differences between the placement of the buffer stage along the HV bus in comparison to the LV bus, the volumetric and gravimetric energy densities between a 400 V rated electrolytic capacitor and 40 V rated electrolytic capacitor are shown in Table 2.2. The two capacitors showcased in Table 2.2 have the highest volumetric energy densities for 40 V and 400 V rated electrolytic capacitors based on the collected data from the surveys in [14], [15].

Table 2.2: Energy density differences between a 40 V and a 400 V aluminum electrolytic capacitor

Parameter	40 V_{dc}	400 V_{dc}
Manufacturer	KEMET	Nichicon
Part number	ALT22A223DD040	LGL2G821MELB50
Volumetric energy density ($\mu J/mm^3$)	435	1785
Gravimetric energy density ($\mu J/mg$)	373	1568

Part I

Single-Phase Power Conversion for Electric Vehicle Charging Applications

Chapter 3

Electric Vehicle On-Board Charger

3.1 Introduction

Level II electric vehicle (EV) on-board chargers interface with the ac grid to charge the dc battery inside the car and provide ancillary services to the grid when electrical energy demands are high. As a result, EV chargers must be equipped to handle 120-240 V_{ac} at the ac port and at least 400 V_{dc} at the dc port with power-handling capabilities in the kilo-watts range [24]. EV chargers must also be highly efficient to reduce charging times that remain competitive with gasoline-powered vehicles' refueling times [25], [26]. Moreover, it is advantageous for the on-board charger to be both volumetrically and gravimetrically power-dense due to its location inside the vehicle at all times.

In a conventional non-isolated single-phase design, a two-level step-up converter is used as the power factor correction stage (and inverting stage) while an electrolytic capacitor bank is used as the twice-line frequency buffering stage [9]. In the two-level boost solution shown in Fig. 3.1, the inductor is needed to regulate the ac current in both PFC and inverting applications to maintain a high power factor and low distortion. At the same time, the capacitor bank must buffer the twice-line frequency power pulsation and minimize the voltage ripple along the dc-link. Although the boost inductor and capacitor bank are necessary components for the conventional EV charger solution to operate, they are typically the most significant contributors to the physical volume of the charger and often the barriers to having a power-dense solution.

This work explores a novel system architecture that significantly reduces the volume of the PFC (and inverting) and the buffer stage without undermining the system's efficiency. This system uses an FCML as the PFC and inverting stage, while a Series-Stacked Buffer (SSB) is used as the twice-line frequency buffering stage. The system topology is shown in Fig. 3.2. The FCML is a hybrid switched-capacitor converter that utilizes a combination of capacitors, with up to 1000x higher energy density than inductors, and an inductor for energy storage and transfer. The phase-shifted pulse width modulation (PSPWM) control scheme of the FCML significantly reduces the volt-seconds of the inductor, further contributing to

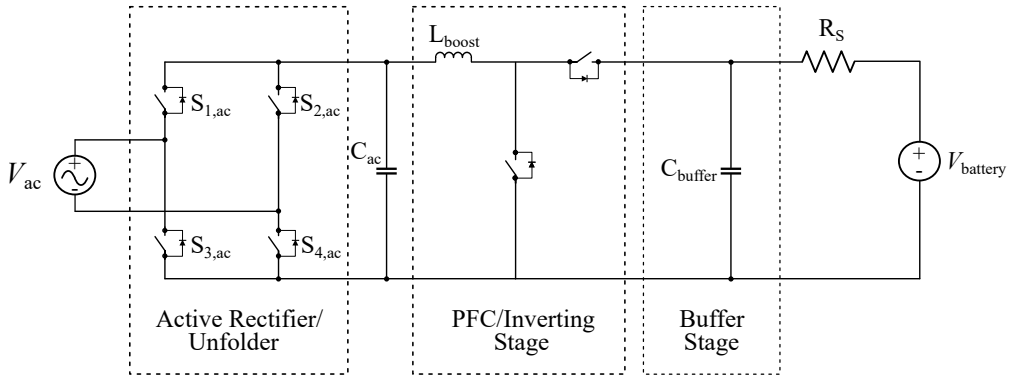


Figure 3.1: A conventional non-isolated two-level boost converter used for electric vehicle on-board charging.

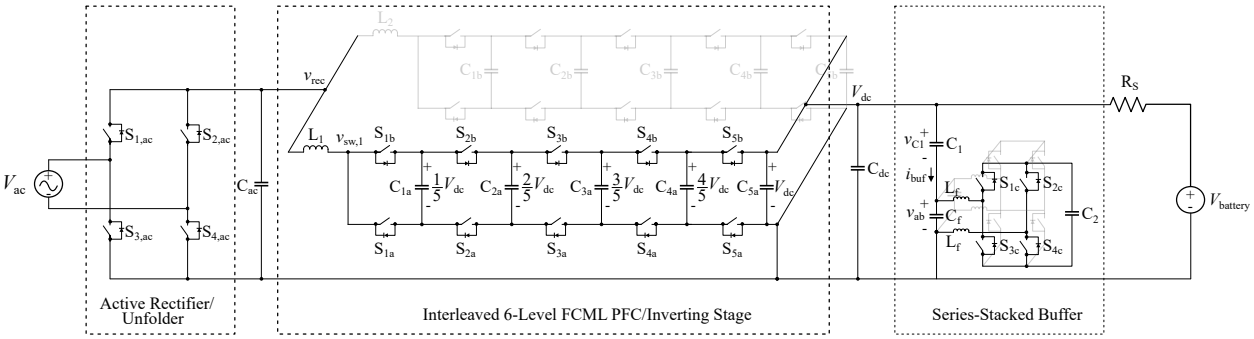


Figure 3.2: Schematic of the overall system with active rectifier (unfolder), interleaved FCML, and SSB.

a smaller physical volume of the passive components compared to the two-level solution. Moreover, the FCML converter's switch voltage stress is significantly reduced in comparison to the two-level solution, allowing for the usage of lower voltage switches that typically have high-performance metrics and figures of merit [19], [21], [27]. The SSB topology comprises a high voltage capacitor between the dc bus and auxiliary full-bridge converter [28]–[32]. The capacitor in the SSB is allowed to have a large ac voltage ripple, allowing for a significant reduction in the buffer capacitance. The capacitor also blocks the dc bus voltage from the full-bridge converter, reducing the voltage stress and power processed by the full-bridge converter allowing the active buffer to have high efficiency.

The system was designed to have a minimized overall volume. As a result, different stages of the EV charger system are implemented on separate modular printed circuit boards (PCBs). All components that generate the most significant amount of heat are placed on the same side of the system to simplify the thermal design. A cold plate that cools the system with liquid and water is used to extract heat from the system.

The rest of this chapter is organized as follows: Section 3.2 gives an overview of the system design and principles of operation; Section 3.3 explains the design of the electrical and thermal hardware for both the first and second revisions of this system; Section 3.4 shares the results from both the first and second revisions of hardware for the EV charger system; lastly, Section 3.5 concludes this chapter.

3.2 System Architecture and Principles of Operation

The complete electrical system schematic of the EV charger is shown in Fig. 3.2. From the ac to the dc port, the electrical system consists of a full-bridge active rectifier stage that rectifies the ac input, two interleaved FCML converters that function as the power factor correction (PFC) boost stage (or inverting if run in reverse), and a paralleled SSB module that buffers the twice-line frequency power pulsation along the dc bus. The system's controller designs are detailed in [33], [34].

FCML Stage

Two interleaved 6-level FCML converters are used as the PFC and inverting stage for the EV charger system. An even-level count was chosen in this work based on the natural charge balancing effect between the flying capacitors in the FCML [35]. Noted, although the even-level case is more immune to charge imbalance than odd-level cases, the capacitor charge balancing is still heavily dependent on the output capacitance of the switches and the input impedance of the power converter system [35], [36]. Each FCML module uses a combination of four flying capacitors and an inductor for energy storage and transfer. By leveraging the higher energy density of class two multi-layer ceramic capacitors, the passive component volume for each FCML module is much smaller volumetrically and gravimetrically than a magnetic-based power converter solution [15], [37].

Each FCML module is controlled by PSPWM; each PWM is phase-shifted by $\frac{360^\circ}{N} = 72^\circ$, where N is the number of levels of the converter [18], [38], [39]. The duty cycle for each phase-shifted PWM is calculated from the PFC or inverting closed-loop control output described in [33] and [34], respectively. Fig. 3.4 displays an example of the PSPWM scheme for a 6-level FCML performing a dc-dc step-down conversion (the schematic of the converter is shown in Fig. 3.3). As shown in Fig. 3.4, the PSPWM control scheme causes a frequency multiplication effect at the switched-node of FCML. For a 6-level FCML, the frequency at the switched-node is $5 \cdot f_{\text{sw}}$, resulting in $25\times$ reduction in the inductor filter in comparison to the two-level non-isolated power converter.

The FCML stage of the EV charger system shown in Fig. 3.2 can be controlled to act as a PFC rectifier or an inverter. When the system is controlled for PFC rectification, the FCML stage operates in a boost mode, and the inductor current is regulated to be in phase with the ac input voltage. When the system is controlled as an inverter, the FCML stage operates in buck mode, producing a rectified sine wave. In both cases, a cascaded full-bridge

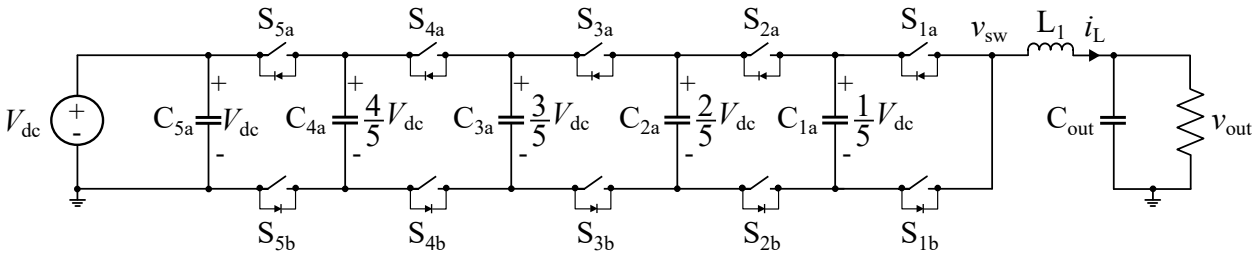


Figure 3.3: A 6-level FCML converter configured for a dc-dc step-down conversion.

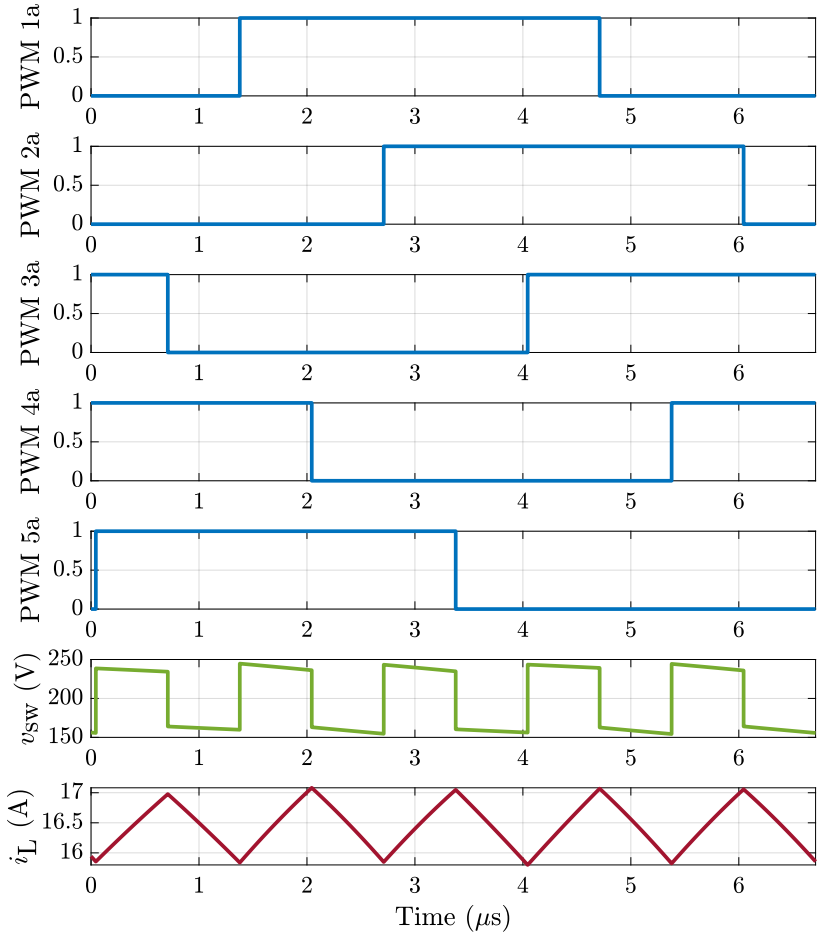


Figure 3.4: The inductor current i_{L} and switched-node voltage v_{sw} during one switching period for the 6-level FCML shown in Fig. 3.3. The input voltage, output power, switching frequency, and duty cycle of the topology are $V_{\mathrm{dc}} = 400$ V, $P_{\mathrm{out}} = 3.3$ kW, $f_{\mathrm{sw}} = 150$ kHz, and d = 0.5, respectively.

stage comprised of high-conductivity devices acts as an active rectifier and interfaces the LC filter of the FCML converter to the grid voltage [13].

Series-Stacked-Buffer Stage

The SSB architecture and control for charging applications are detailed in [33], [40]. The SSB in the EV charger system uses the traditional loss compensation control methodology described in Section 4.2. Capacitor C_1 is the main energy-buffering capacitor connected in series with a full-bridge converter. Capacitor C_2 operates as the dc voltage source for the full-bridge converter. Voltage v_{C1} is allowed to have a large ac voltage ripple, which is canceled by the voltage produced by the full-bridge converter v_{ab}. The derivation of voltage v_{ab} based on the sensed physical parameters of the EV charger system and its closed-loop control can be found in [40]. Because v_{C1} is allowed to have a significant ripple, the capacitance and volume of C_1 can be significantly reduced compared to conventional dc bus capacitor filters. Moreover, because the dc bus voltage is displaced across C_1, the full-bridge processes a minimal real power, further improving the overall system efficiency.

3.3 Hardware Implementation

Figs. 3.5 and 3.6 show the constructed hardware prototype of the proposed system and control for the first and second revisions of the EV charger system, respectively. Table 3.1 lists the hardware components used in the sub-modules of the EV charger system for both revisions. The system hardware prototype is comprised of two interleaved FCML converters, an SSB with energy storage capacitor C_1 and full-bridge DC source capacitor C_2, a full-bridge active rectifier, and a logic connector board. The logic connector board connects the FCML, SSB, and active rectifier stages to a TI C2000 microcontroller (TMS320F28379D) on which the system control loops are implemented. Power is transferred from one module to another via bolt-type connectors. The design philosophy of the 3D integration for both the electrical and thermal systems is discussed in [34]. The start-up module is shown in Fig. 3.10. It connects the system between the active rectifier bridge and the FCML filter inductor.

FCML Module

This chapter discusses two hardware revisions of the FCML stage's design. Both revisions have the same overlying structure. The first revision of the FCML module is designed with lower voltage switches and is showcased in Section 3.4 up to 6.1 kW for a 400 V_{dc} to 240 V_{ac} inverter operation. The second revision was designed to reduce the commutation loop inductance of the FCML switch pairs [41]. Moreover, the second revision utilizes higher voltage switches to account for the increased voltage ripple seen at the switch-node of the

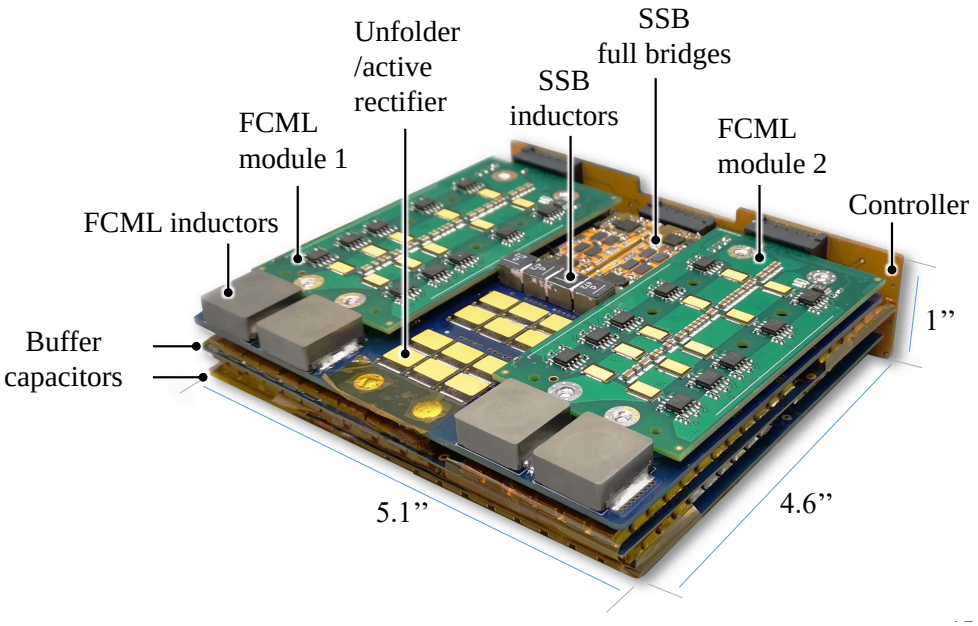


Figure 3.5: The first revision of the EV charger assembly, excluding the thermal management, with key subsystems labeled. In this depiction, the first revision of the FCML is shown. (Figure was created in collaboration with Sophia Chou and Zitao Liao.)

FCML that is caused by voltage imbalance along the flying capacitors [35], [36], [42], and is used to validate the EV charger system's start-up procedure.

First revision of the FCML module

The EV charger system is designed to handle a voltage along the dc-link up to $V_{\text{dc}} = 400$ V. As a result, the switches of the FCML must have a dc rating of at least 80 V. Thus, in the first revision of the FCML module, 100 V GaN Systems GS61008T switches were used. To achieve a relatively low commutation inductance, a lateral commutation loop is used in this FCML revision [43]. The resulting power density by box volume of the 3-kW FCML module presented here is 1800 W/in^3.

As illustrated in Fig. 3.2, most of the switches in the interleaved FCML modules are not directly tied to the ground, resulting in a more complex gate drive solution. Isolated dc-dc power converters are the most straightforward option to resolve this issue. However, they suffer from low efficiency, sometimes demonstrating less than 10% efficiency [44]. To conserve gate drive power losses, the FCML modules utilize a cascaded bootstrap methodology with LDOs [42], [45], [46].

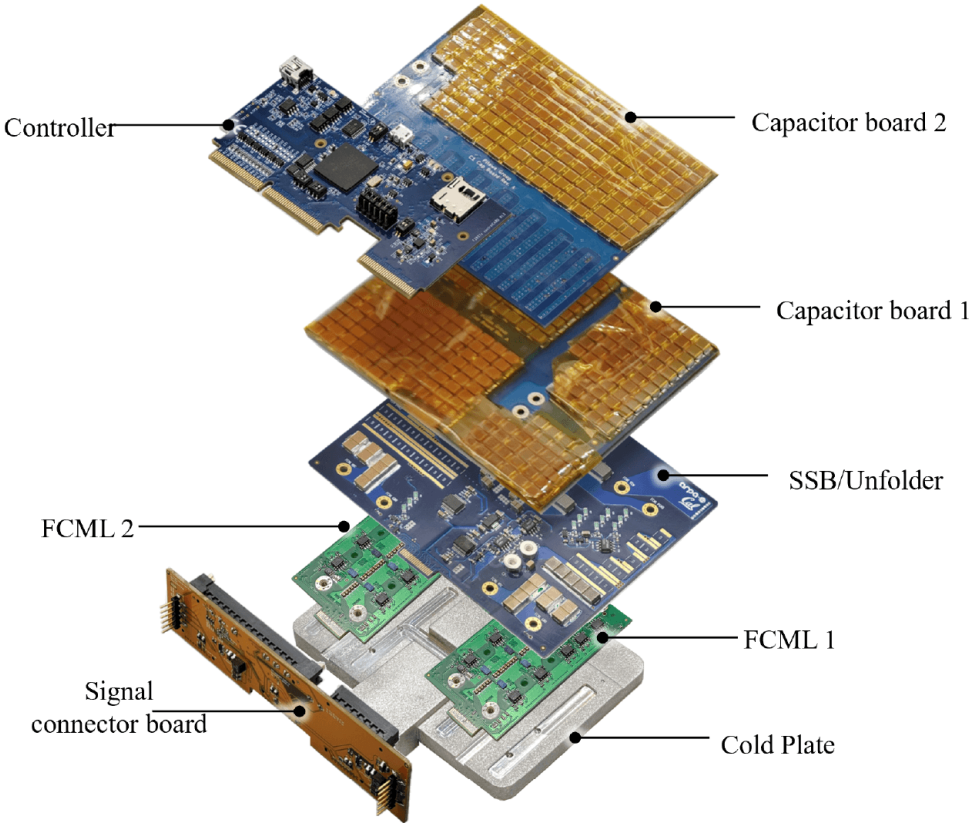


Figure 3.6: A stack-up of the second revision of the EV charger assembly, showing the modular hardware design. In this assembly depiction, the second revision of the FCMLs is shown and interfaces with the custom additively manufactured cold plate. (Figure created in collaboration with Sophia Chou, Rahul Iyer, Ting Ge, and Zitao Liao.)

Second revision of the FCML module

The second revision of the FCML module was designed to handle high output currents and to mitigate flying capacitor charge imbalance. Under heavy load or transient conditions, the flying capacitor voltages may experience charge imbalance [35], causing the blocking voltages of the switches to increase past their nominal value. To resolve this issue, switches with a higher voltage rating can be implemented in the FCML module. Specifically, a high voltage power semiconductor with low $R_{DS,on}$ can be chosen, enabling lower conduction loss and higher efficiency at high power operation. Increasing the device voltage rating to handle higher load currents instead of increasing the flying capacitance allows us to improve our passive component energy utilization and prevent power density penalties associated with larger flying capacitances at high-power operations.

The FCML module was also designed to decrease commutation loop inductance from previous hardware prototypes [34]. By reducing the FCML switch pair's loop inductance,

Table 3.1: Component listing of both revisions of the EV charger system

Subsystem	Component	**Part No.**	**Parameters**
Interleaved 6-Level FCML (per leg)	GaN FETs (Rev. 1)	GaN Systems GS61008T	100 V, 7 $m\Omega$
	GaN FETs (Rev. 2)	EPC 2033	150 V, 5 $m\Omega$
	Isolated Gate Drivers	Si8271GB-IS	Silicon Labs Si827x Series
	Flying Capacitors	TDK C5750X6S225K250KA	2.2 μF × 2–5 (parallel, $\sim$ 2.6μF effective)
	Inductors	Vishay IHLP6767GZER100M11	10 μH
Active Rectifier / Unfolder	GaN FETs	GaN Systems GS66516T	650 V, 25 $m\Omega\times$ 3 (parallel)
	Isolated Gate Drivers	Si8274GB1-IS1	Silicon Labs Si827x Series
Interleaved Series-Stacked Buffer (per leg)	GaN FETs	EPC 2033	150 V, 7 $m\Omega$
	Isolated Gate Drivers	Si8274GB1-IM1	Silicon Labs Si827x Series
	Inductors	Coilcraft XAL7070-472	4.7 μH × 2 (series)
Buffer Capacitors	C_1	TDK C5750X6S225K250KA	× 820 (parallel)
	C_2	TDK C5750X7S2A156M250KB	× 200 (parallel)
Control	Microcontroller	TI F28379D controlCARD	C2000 Series Microcontroller
Start-Up	MOSFETs	Infineon IPT65R033G7	650 V, 33 $m\Omega$ x 4 (parallel)
	Diode	ON Semiconductor MUR160G	600 V, 1 A
	Isolated Gate Driver	Si8271GB-IS	Silicon Labs Si827x Series
	Isolated Gate Driver	ADuM5010	Analog Devices isoPower

ringing across the switches' drain-to-source can be further reduced, lessening the voltage stress of the switches [47]. This FCML revision places copper shield planes directly under each commutation loop of complementary switch pairs and adjacent flying capacitors. The current transient in the power stage creates a changing magnetic field, which induces eddy currents inside the shield plane. By Lenz's law, the eddy currents flow in the opposite direction of the current in the power stage and generate magnetic fields that counter the original fields. As a net result, the drain-to-source voltage ringing associated with each switch transition is significantly reduced. Fig. 3.7 shows the location of the copper shield planes and the eddy current induced from the power stage current. Fig. 3.8 shows simulated results in ANSYS Q3D of the loop inductance of the FCML modules with and without a copper shielding layer concerning frequency. With the addition of a copper shield plane, the commutation loop inductance decreases and is nearly halved at higher frequencies.

Series-Stacked Buffer and Active Unfolder

Fig. 3.6 shows the placement of the SSB system about the rest of the EV charger system. To minimize the physical volume of the converter without increasing the number of layers in the SSB/Unfolder PCB, the full-bridge converter in the SSB, is comprised of individual four-layer PCB "switching cells" mounted onto the SSB/Unfolder PCB module. These switching cells are placed on the bottom side of the SSB/Unfolder board such that the full-bridge switches and inductive filtering components can be thermally connected to the cold plate for cooling. The switching cells and the inductive filtering components are shown on the SSB/Unfolder board in Fig. 3.9. The C_1 capacitor naturally blocks the dc-link voltage from the full-bridge converter, such that the switches in the full-bridge converter must be rated to block the voltage across C_2. Therefore, 150 V EPC2033 switches were used in this system design.

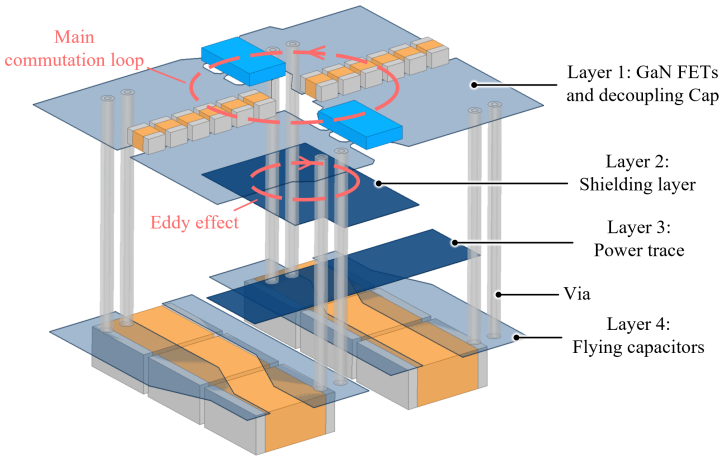


Figure 3.7: PCB design of FCML module power stage that uses copper shield planes to reduce the parasitic loop inductance. (Figure created in collaboration with Ting Ge and Rahul Iyer.)

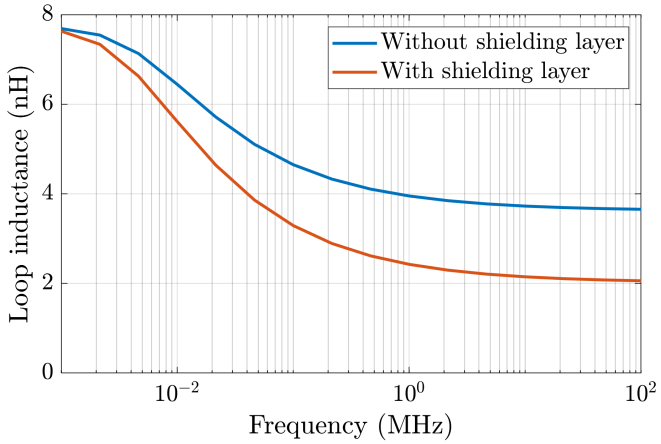


Figure 3.8: Commutation loop inductance simulated in ANSYS Q3D for lateral commutation loop with and without shielding layer. (Figure created in collaboration with Ting Ge and Rahul Iyer.)

Class 2 multi-layer ceramic capacitors (MLCCs) have been found to have significantly larger energy densities, even with capacitance de-rating with voltage, than compared to other types of capacitors, such as electrolytic and film capacitors. Therefore, two separate two-layer PCBs were designed to parallel many class 2 MLCCs for C_1 and C_2. These boards are shown in the system stack up in Figs 3.5 and 3.6. To minimize the physical volume of the system, the individual MLCCs are all soldered to the PCB and are not stacked. On

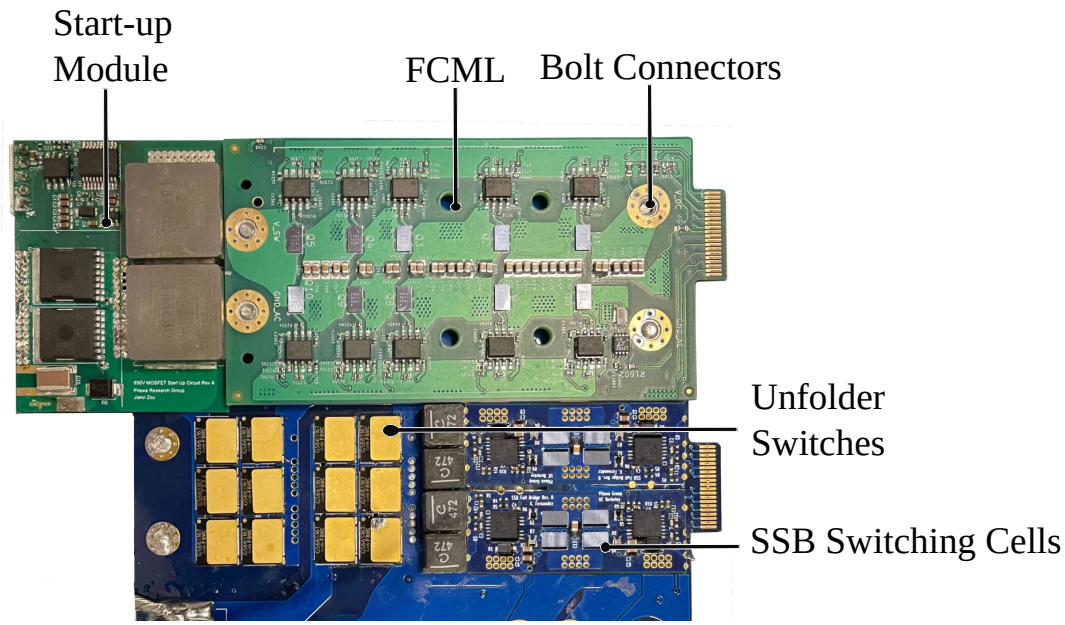


Figure 3.9: Assembly of the EV charger system showing the SSB switching cells, which are mounted on to the SSB/Unfolder board depicted in Fig. 3.6, and the start-up PCB daughter-board, which is mounted on to the FCML converter PCB. (Figure created in collaboration with Ting Ge, Rahul Iyer, and Jiarui Zou.)

capacitor board 2, physical space was intentionally left empty on the top side of the PCB to allow room for the microcontroller connection. This allows the full height of the controller to meet more or less the height of the top-sided capacitors on capacitor board 2, not adding any additional size to the box volume of the system.

In the first revision of this work, the PWMs of the two individual full-bridge switching cells of the SSB were interleaved. For example, a PWM is generated for S_{1c} in one of the full-bridge switching cells, while the same PWM with a 180° phase shift is generated for S_{1c} in the second full-bridge switching cell. However, this causes larger RMS currents to flow through the filter inductors L_f of the SSB in comparison to when the switching cells are in phase, generating more power loss and significantly increasing the thermal stress of the filtering inductors. Therefore, in the second revision of this work, the two full-bridge converters operate in phase with one another, decreasing the RMS currents in the filter inductors and their thermal temperatures at high power operation.

Start-Up Module

Without a start-up module, the EV charger system could experience catastrophic damage if a high voltage instantaneously connects to the dc or ac port. Therefore, A start-up circuit daughter board, shown in Fig. 3.10, is designed to integrate the startup devices and

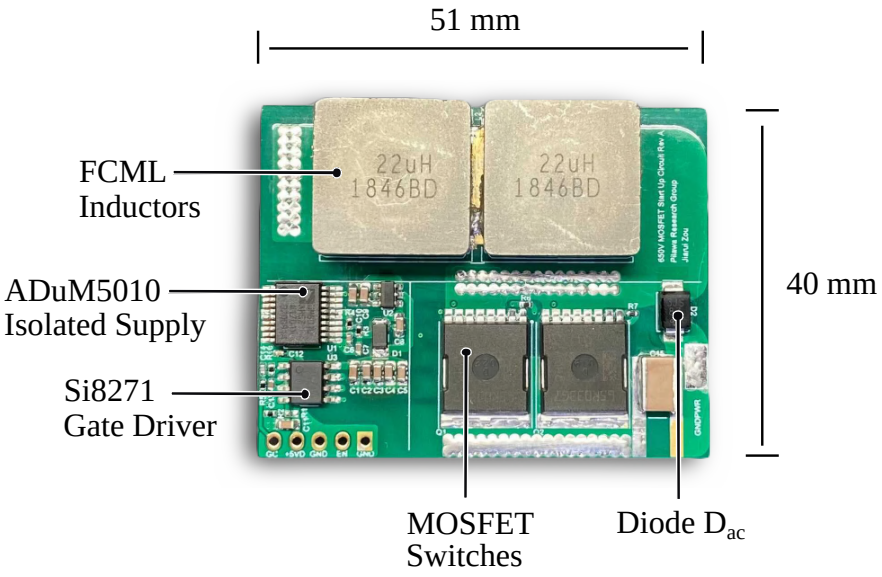


Figure 3.10: Modular start-up PCB daughter-board that is mechanically and electrically fitted to the EV charger system. (Figure created in collaboration with Ting Ge, Rahul Iyer, and Jiarui Zou.)

associated gate-drive hardware. Fig. 3.11 displays the schematic of the FCML with start-up components. The start-up module interfaces the active rectifier and the FCML converter's filter inductor. A PWM control signal from the microcontroller is fed to the gate driver IC. Since the source of S_{ac} floats above the system ground potential, an isolated supply is needed to deliver gate drive power. Four 650 V Silicon MOSFETs, two on each side of the module, are connected in parallel to increase the current handling capability of the series device S_{ac}. The control (shown in Fig. 3.12) and design of this daughterboard is adapted from [48] such that it could be mechanically and electrically connected to the second revision of the EV charging system, as shown in Fig. 3.9.

Cold Plate

Conventionally, a liquid cooling loop is utilized in electric vehicles to dissipate power loss through the indirect flow of water [49], [50]. In this work, two liquid cooling solutions for the thermal management of the EV charger system are proposed - a machine-drilled cold plate, shown in Fig. 3.13, and an additively manufactured (AM) cold plate, shown in Fig. 3.14. Machine-drilled cold plates are cost-effective solutions with quick manufacturing turnaround times. However, their internal liquid cooling channels have very restrictive designs; they specifically only permit paralleled and perpendicular channels due to their drilling manufacturing process, thus restricting a fully minimized differential pressure drop in the thermal management design [51]. Therefore, a second thermal management solution that examines

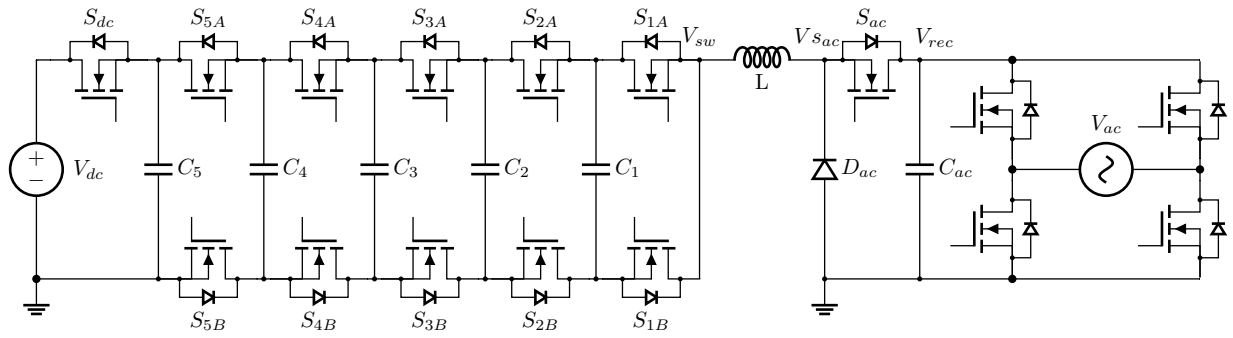


Figure 3.11: Schematic of the EV charger FCML equipped with start-up components S_{ac} and D_{ac}. (Figure made in collaboration with Sophia Chou.)

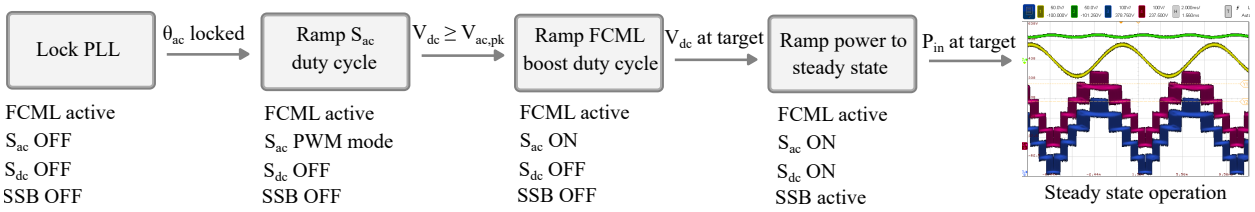


Figure 3.12: Flow diagram of the EV charger start-up control procedure adapted from [48]. (Figure made in collaboration with Sophia Chou.)

the design of an additively manufactured (AM) cold plate is explored in this work. Due to its 3D printing process, additive manufacturing doesn't restrict the shape or orientation of the internal channels of the cold plate, allowing for an even higher optimized liquid cooling design with a significantly lower pressure drop across the thermal management system and reduced mass [52]. However, the 3D printing manufacturing process can become expensive and thus prohibitive in this type of solution for large-scale EV manufacturing. With this in mind, the machine-drilled cold plate was used to showcase a power demonstration of the entire EV charger prototype in Section 3.4. In this section, only the design of the AM cold plate is discussed, and the reader is referred to [34] for a detailed design discussion of the machine-drilled cold plate.

Fig. 3.14 shows the custom AM cold plate used to liquid-cool the second revision EV charger electrical system. The cold plate used in this work incorporates a highly optimized fluid flow path to ensure efficient heat removal from the converter assembly. The pressure drop across the cold plate and its mass were considered optimization objectives in the design optimization process. An aluminum-silicon (AlSi10Mg) direct metal laser sintering (DMLS) additive manufacturing process was chosen for the cold plate construction to enable complex internal geometries needed for fluid flow and weight reduction. Additive manufacturing permits the design of a curved fluid flow path with a non-circular channel cross-section.

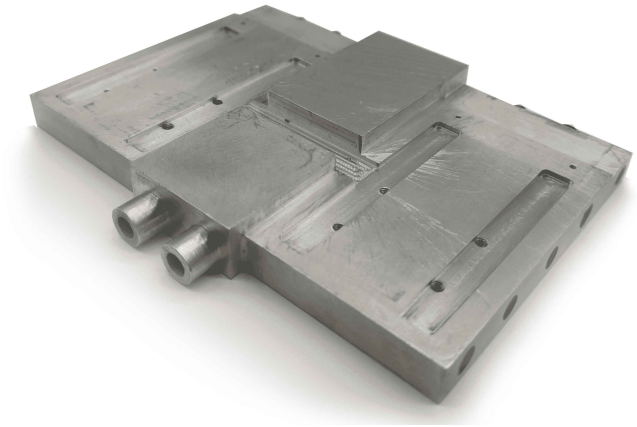


Figure 3.13: The machine-drilled manufactured cold plate, showing the side that interfaces with the electrical system. (Figure made in collaboration with Sophia Chou and Zitao Liao.)

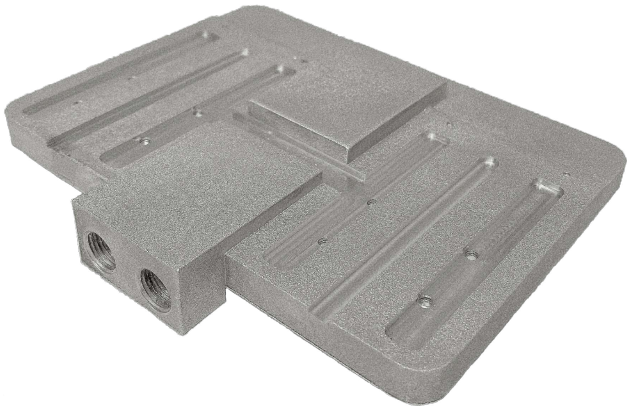


Figure 3.14: Custom additively manufactured cold plate, showing the side that interfaces with the electrical system. (Figure made in collaboration with Ting Ge and Rahul Iyer.)

This increases heat exchange between the inner fluid and the cold plate surface, significantly reducing fluid pressure loss over the liquid path length. The custom AM cold plate design has an approximate differential pressure drop of 4 PSI. The cold plate weighs approximately 240 grams and occupies a total volume of 7 cm^3.

The velocity of the coolant fluid (water in this design) and the estimated temperatures of the power switches and inductors on the charger PCBs are simulated in ANSYS IcePAK. The simulation results are shown in Fig. 3.15. Power switch and inductor losses are estimated based on LTspice simulation of the FCML converters in buck mode, representing the system operating as an inverter. Manufacturer GaN SPICE models are used for improved modeling of switching and conduction losses. The simulation reveals that the FCML converters' high-side switches demonstrate higher loss than their low-side counterparts due to

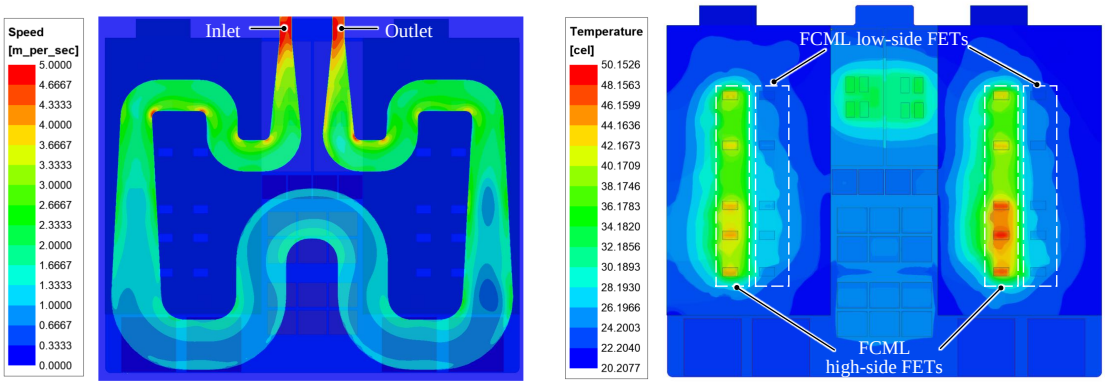


Figure 3.15: Simulated velocity magnitude of the coolant in the AM cold plate with a 3.3 LPM flow and corresponding temperature on the power stage operating at 4 kW. (Figure made in collaboration with Ting Ge and Rahul Iyer.)

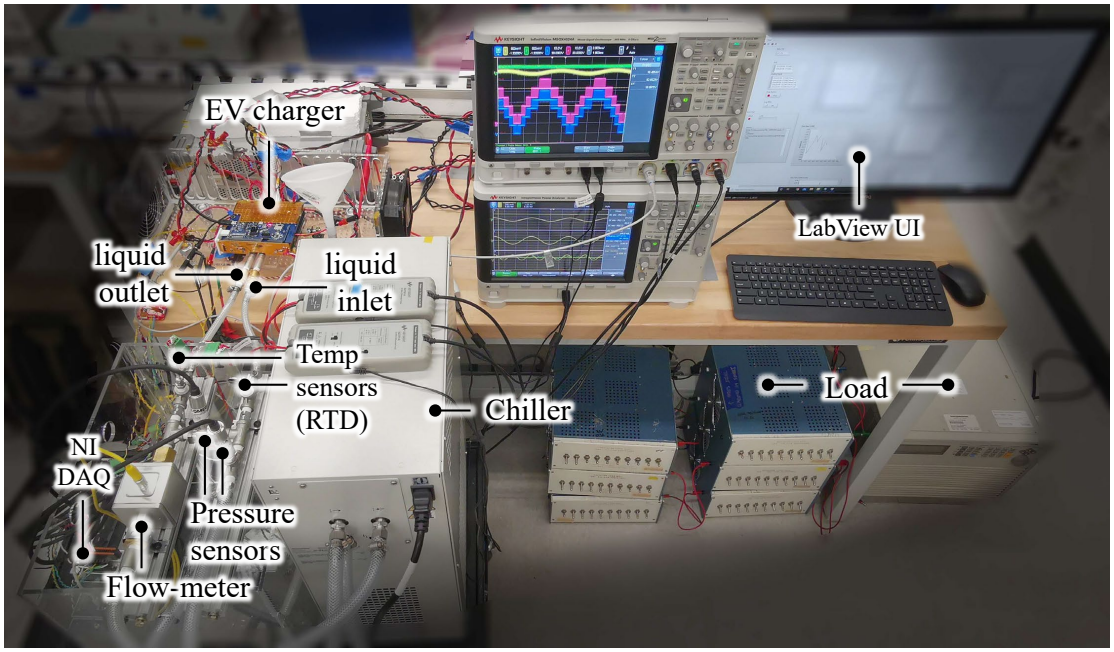


Figure 3.16: System test setup for high power inverter testing. (Figure made in collaboration with Sophia Chou and Zitao Liao.)

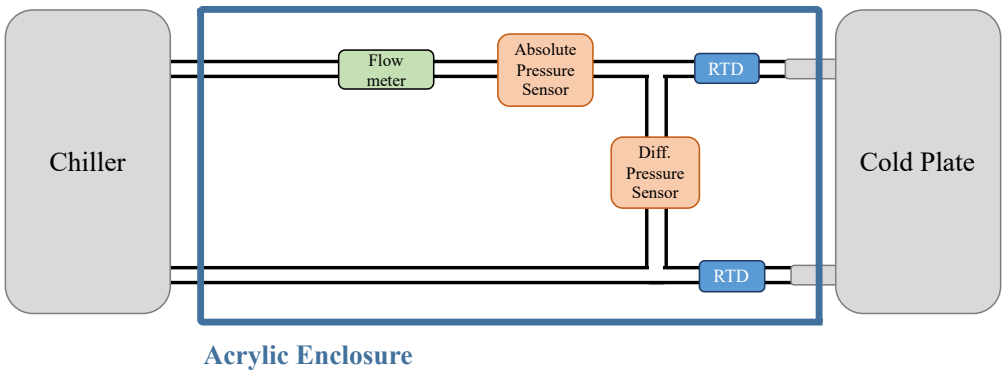


Figure 3.17: Diagram of liquid cooling loop used in high power inverter testing. Table 3.2 lists the equipment used for data measurement and acquisition of the cooling loop.

Table 3.2: Data acquisition and thermal management equipment for EV charger inverter testing

Equipment	Description	Part Number
Chiller	Thermo Scientific Polar Series Accel 500	223422800
Flow meter	Kobold MIM Series Electromagnetic Flow Meter	MIM-1215HG5C3T0
RTDs	REOTEMP RTDs	AT-PX1123YLR4S1T2T
Data Acquisition Chasis	NI cDAQ-9189 CompactDAQ Chassis	785065-01
Analog Data Module	NI 9201	779013-01
RTD Data Module	NI 9216	785186-01

their hard-switching operation and thus have more elevated temperatures. The difference in temperature between the low-side and high-side devices is highlighted in Fig. 3.15. The left-side FCML converter demonstrates a relatively lower temperature than the right-side one since the high-side FETs of the left-side FCML converter are closer to the fluid flow pipeline. This matches the findings in [34].

3.4 Experimental Results

This section gives experimental results for dc to ac high power inverter testing, ac to dc start-up validation, and preliminary electromagnetic interference results. The reader is referred to [33] for further details on the PFC and THD results for ac-dc validation and testing.

Inverter Testing

To validate the high-power handling capabilities of the EV charger system, the combined electrical and mechanical systems were tested in inverter mode, performing a 400 V_{dc} to

240 V_{ac} conversion up to levels in the kilowatts. The EV charger system was tested with a water cooling loop with the water temperature set to 25° C. Fig. 3.16 shows the inverter test setup, and Fig. 3.17 shows an annotated diagram of the liquid cooling loop with the equipment used for data measurement and acquisition of the cooling loop listed in Table 3.2. This test was performed for the system's first and second revision. Noted, the first revision of the system consists of the first revision of the FCML module and machine-drilled cold plate, while the second revision of the system consists of the second revision of the FCML module and the AM cold plate; the same revision of the SSB/Unfolder board, capacitor boards, logic connector board, and microcontroller are used in both inverter tests.

First revision inverter testing

Fig. 3.18 displays the efficiency of the first revision of the EV charger system for a 400 V_{dc} to 240 V_{ac} conversion with an input power ranging from 500 W to 6.1 kW. The peak efficiency of the system recorded is 99% at 1.1 kW, while the full-load efficiency is 97.7%. A high-precision Keysight PA2201 power analyzer was used to capture these efficiency measurements. Fig. 3.19 displays the system waveforms at 6.1 kW. Waveforms v_{C2} and v_{ab} are the voltage across the C_2 capacitor and the voltage produced by the interleaved full-bridge modules, respectively. Voltage v_{C2} demonstrates the validity of the loss compensation control that injects charge into capacitor C_2. In contrast, voltage waveform v_{ab} demonstrates the validity of the SSB - its proposed control to create a sinusoidal waveform with the full-bridge converters that cancel with the ac voltage ripple across C_1. Voltage waveforms v_{sw1} and v_{sw2}

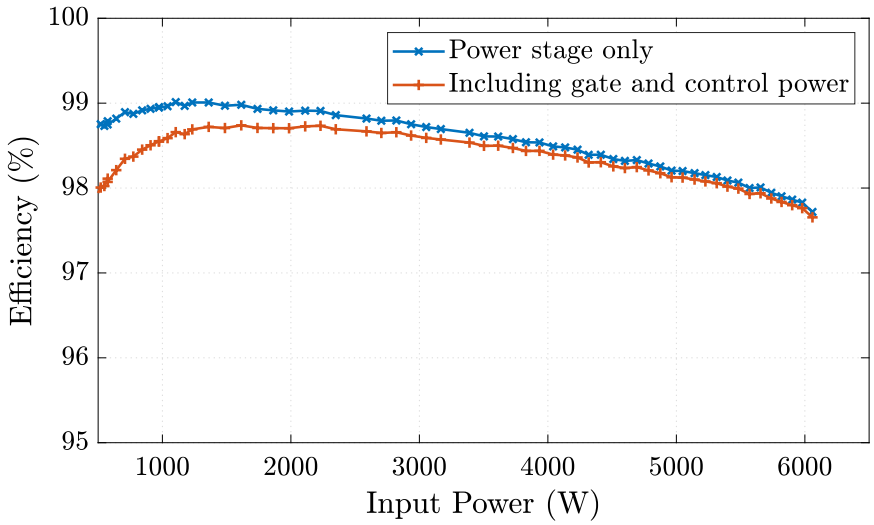


Figure 3.18: The efficiency of the 6.1 kW inverter test, 400 V_{dc} to 240 V_{ac} for the **first** revision of the EV charger system. (Figure made in collaboration with Sophia Chou and Zitao Liao.)

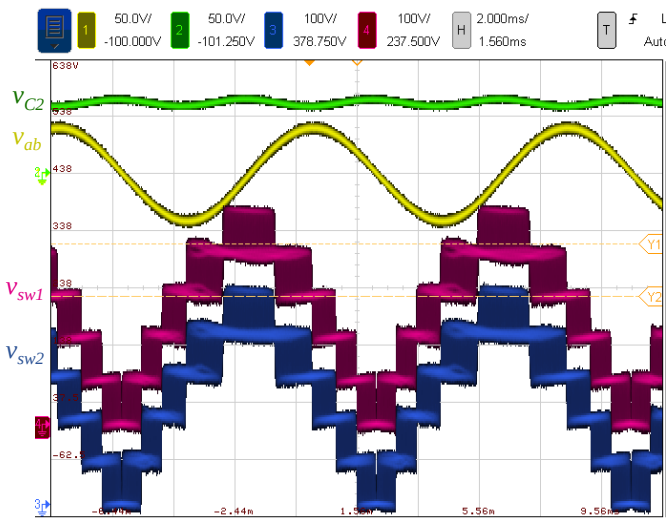


Figure 3.19: Typical SSB voltage waveforms for v_{C2} and v_{ab}, and FCML switching node voltages from 400 V_{dc} to 240 V_{ac}, 6.1 kW for the **first** revision of the EV charger system. (Figure made in collaboration with Sophia Chou and Zitao Liao.)

Table 3.3: Key performance specifications for the 6.1 kW inverter test for the **first** revision of the EV charger system

Parameter	Value
DC Voltage	400 V_{dc}
AC Voltage	240 $V_{ac,\ rms}$
AC Current	25 A
AC Power	6.1 kW
Peak Efficiency	99.01% at 1.1 kW
Full Load Efficiency	97.7% at 6.1 kW
Switching Frequency	150 kHz
Effective Frequency @ v_{sw}	750 kHz
PCBA Rect. Box Dimensions	5.1" × 4.6" × 1.0" (12.95 cm × 11.68 cm × 2.54 cm)
Cold Plate Dimensions	5.1" × 3.6" × 0.375" (12.95 cm × 9.14 cm × 0.95 cm)
Without cold plate	
Weight	0.8 kg
Volume	23.46 in^3 (384.4 cm^3)
Volumetric Power Density (w/o. cold plate)	260 W/in^3 (15.9 W/cm^3)
Gravimetric Power Density	7.6 kW/kg
With cold plate	
Weight	1.1 kg
Volume	30.35 in^3 (497 cm^3)
Volumetric Power Density	201 W/in^3 (12.3 W/cm^3) e
Gravimetric Power Density	5.5 kW/kg

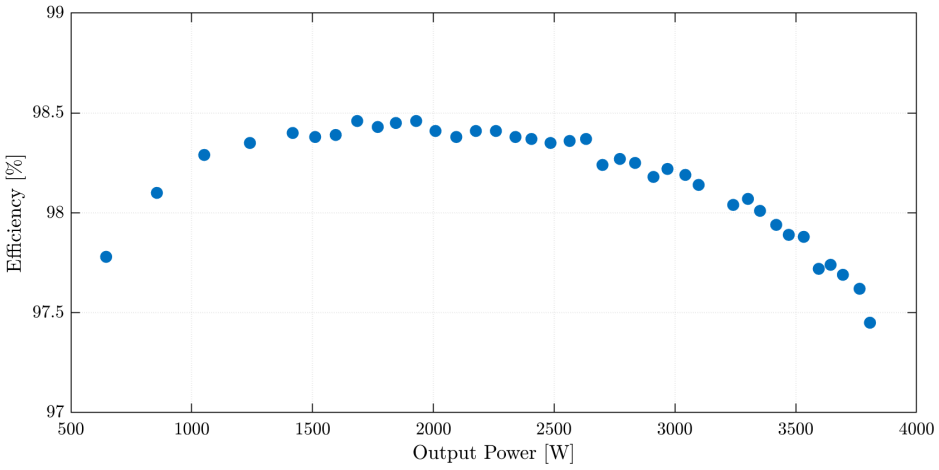


Figure 3.20: The efficiency of the **second** revision of the EV charger system in inverter mode from 400 V_{dc} to 240 V_{ac}. (Figure made in collaboration with Ting Ge and Rahul Iyer.)

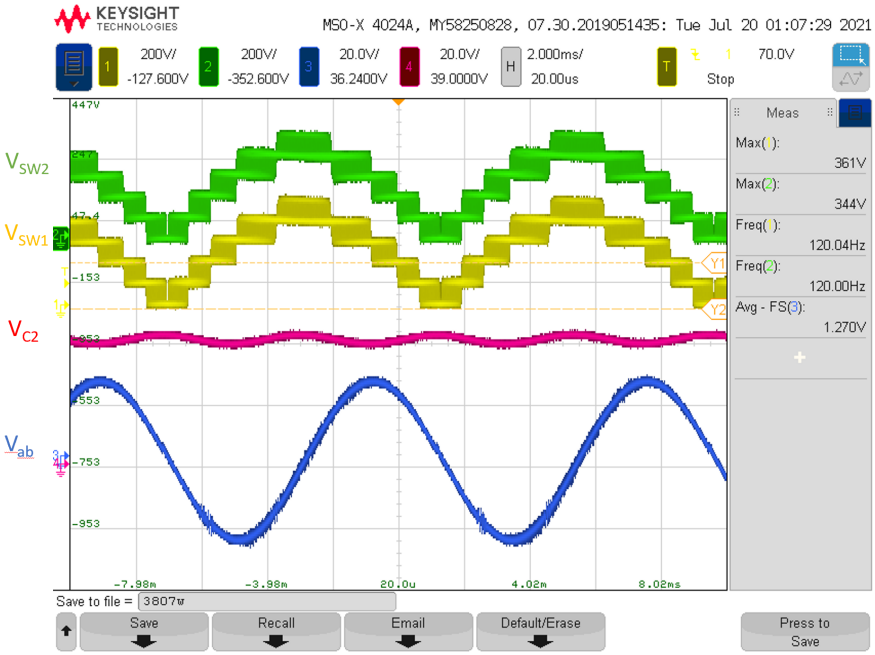


Figure 3.21: FCML switching waveforms measured at peak tested power (3.8 kW) for the **second** revision of the EV charger system. The measured switched-node waveforms indicate the natural balancing of the flying capacitor voltages. (Figure made in collaboration with Ting Ge and Rahul Iyer.)

are the measured voltages of the switched nodes of each FCML with respect to the ground of the system. Both v_{sw1} and v_{sw2} verify the ability of both FCMLs to produce a 6-level rectified voltage waveform. Table 3.3 shows the performance and testing specifications.

Second revision inverter testing

The second revision of the EV charger system was tested up to 3.8 kW operating as an inverter. The electrical system was connected to a 400 V_{dc} input source, producing a 240 V_{ac} RMS output. Fig. 3.20 shows the electrical system efficiency over a 500 W to 3.8 kW output power range. The peak efficiency of the system and corresponding power is 98.5% at 1.7 kW, while the efficiency at max power is 97.4%. A high-precision Keysight PA2201 power analyzer was used to capture these efficiency measurements. Fig. 3.21 displays switched-node voltage waveforms exhibiting stable balanced operation. Fig. 3.21 also shows the fundamental SSB voltage waveforms demonstrating twice-line-frequency energy buffering on the dc bus.

Start-up validation

The system is connected to an ac supply to test the proposed start-up circuit with the start-up procedure enabled. Fundamental waveforms during converter start-up with annotations highlighting the different phases of the start-up control are shown in Fig. 3.22. The system was connected to a 120 V_{ac} source and commanded a target dc output of 400 V_{dc}. The start-up control and hardware allow for the dc-side voltage V_{dc} to be ramped from 0 V to 400 V in a safe manner.

3.5 Conclusion

This chapter investigates a bidirectional EV charging system consisting of FCML and SSB stages. A second system revision was designed to offer improvements in the converter's design and component selection. Furthermore, an optimized additively manufactured cold plate enables the demonstration of a compact and lightweight prototype. The first revision of the system is tested up to 6.1 kW and obtains a 99% peak efficiency at 1.1 kW and a full-load efficiency of 97.7%. The second revision of the system was tested up to 3.8 kW and obtains a peak efficiency of 98.5% at 1.7 kW and a full-load efficiency of 97.4%. A reliable converter start-up from an ac source using a novel soft-start sequence for charging the flying capacitors is demonstrated. The start-up hardware and control can charge up the dc-side voltage from a 120 V_{ac} RMS supply.

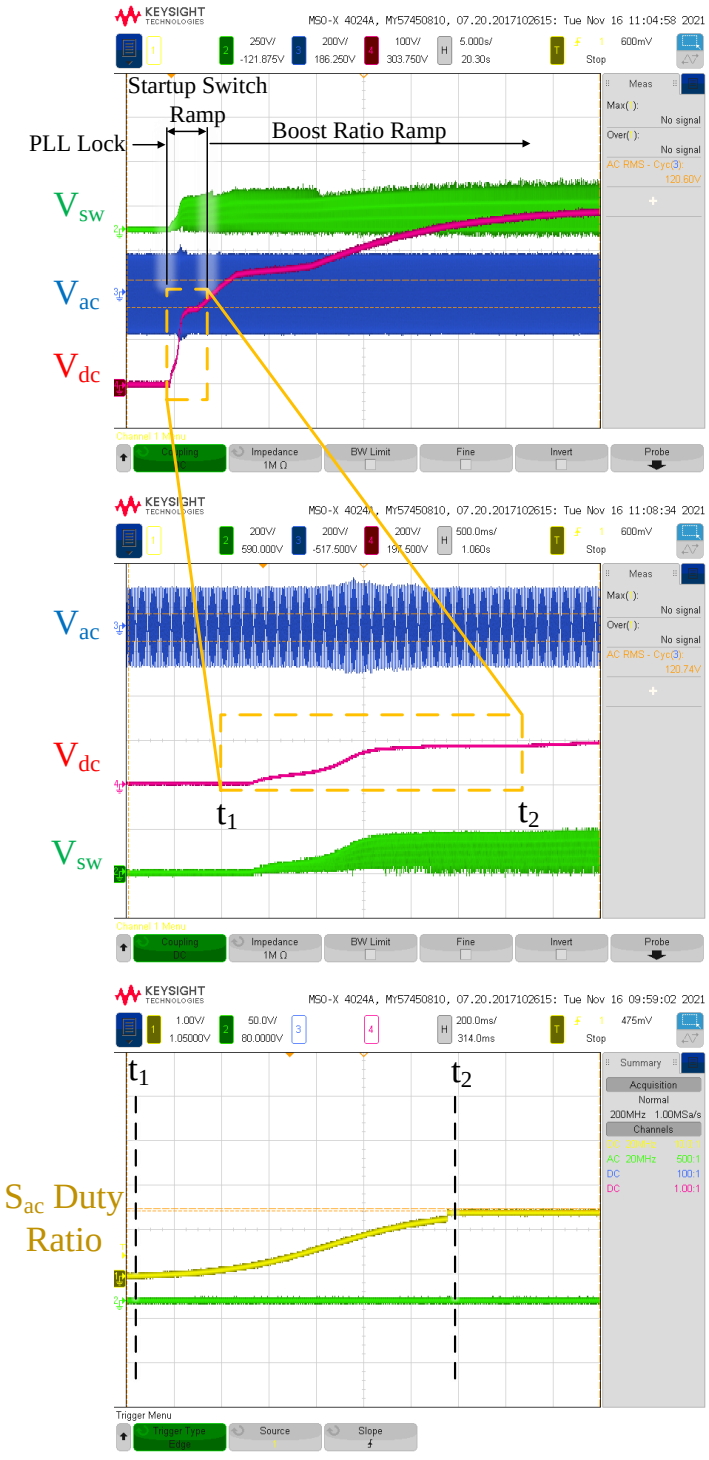


Figure 3.22: Annotated start-up waveforms showing start-up switch ramp phase and corresponding start-up switch duty ratio ramp. (Figure made in collaboration with Ting Ge, Rahul Iyer, and Jiarui Zou.)

Chapter 4

Series-Stacked Buffer with and without the Charge Injection Method

4.1 Introduction

In single-phase rectifier and inverter systems, twice-line frequency power pulsation present at the input port of the converter must be processed by an energy buffer to avoid large current ripple and associated losses in the dc-side supply. Traditionally, dc-link capacitors are employed as this energy buffering element [53]. However, in addition to processing twice-line-frequency power, the dc-link capacitors must be sized to ensure that the dc-link voltage meets tight voltage ripple requirements. Consequently, the dc-link capacitance is frequently oversized, contributing to a significant fraction of the overall system volume [54]. In order to overcome this limitation and further reduce the physical volume of the buffer stage, it is advantageous to separate the twice-line frequency buffering and voltage regulation requirements from one another.

Active buffers are becoming increasingly popular solutions due to their ability to decouple the system buffering and dc-link voltage regulation requirements, reducing the overall single-phase system volume and cost compared to bulky solutions that utilize electrolytic capacitors. [55]–[66]. Traditionally, active buffers have the active switching elements in the circuit connected directly to the dc bus [67]–[71]. As a result, the active devices of the circuit have to block the high dc voltage displaced across the dc-link. Therefore, the active buffer processes a non-negligible amount of energy, further undermining the efficiency of the single-phase converter. Moreover, the high voltage stress in the circuit necessitates more significant magnetic filtering elements to reduce high-frequency current ripple in the buffer, contributing to a larger overall physical volume of the converter. To reduce the amount of power processed in the active buffer, the voltage blocked by the active elements and displaced across the filtering elements must be reduced.

The Series-Stacked Buffer (SSB) is an active buffer topology that accomplishes this by placing a high-voltage capacitor between the dc bus and the active circuitry. As a result, the

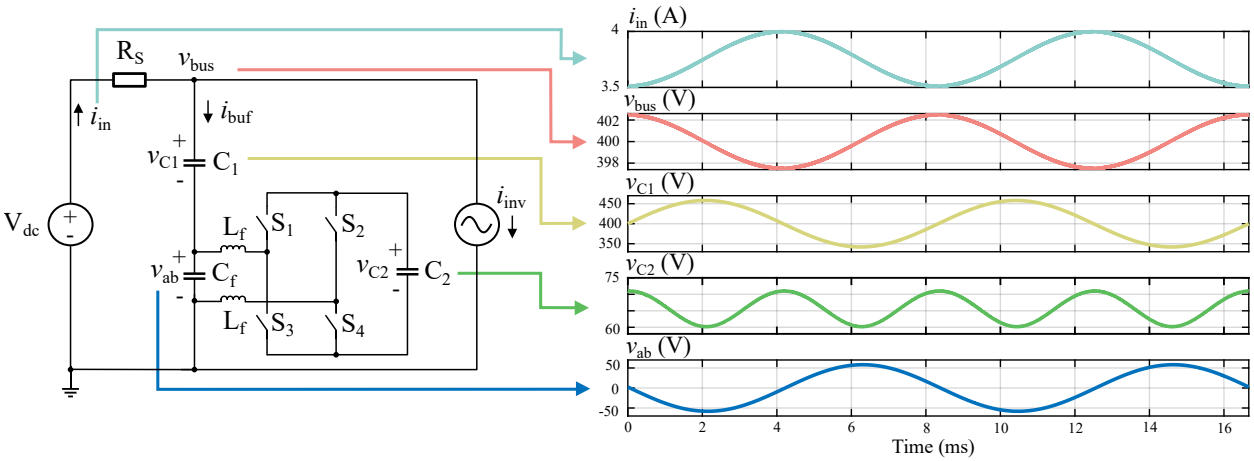


Figure 4.1: Schematic of a traditional Series-Stacked Buffer connected to a dc voltage source V_{dc} and an inverter modeled as a current load i_{inv}. Voltage and current waveforms of the system are displayed for a 1.5 kW system operation where $v_{bus,\,dc} = 400$ V, $i_{dc} = 3.75$ A, $C_1 = 80$ μF, $C_2 = 204$ μF, and $R_s = 10$ Ω.

high dc voltage is absorbed by the capacitor, reducing the voltage stress and power processed by the active circuitry [28]–[32]. Fig. 4.1 depicts a single-phase inverter system utilizing the SSB as the energy buffer. The SSB is connected to a dc input voltage source with source impedance R_s and an inverter whose input port is modeled with current

$$i_{inv} = i_{dc}\sin(\omega_{2L}t) + i_{dc}. \tag{4.1}$$

In (4.1), ω_{2L} is the system's twice-line angular frequency $2\cdot(2\pi f_L)$ and f_L is the nominal ac mains frequency of either 50 to 60 Hz, depending on the operating region. Assuming a near-lossless inverter, i_{dc} is the dc-offset of input current i_{in} and is also the magnitude of the twice-line ac current component. Exemplary waveforms of the modeled 1.5 kW, 400 V dc-bus-rated SSB with a source impedance of $R_s = 10$ Ω are also shown in Fig. 4.1.

Although the SSB buffers most of the dc-link twice-line frequency power pulsation, a drawback is the required loss compensation control [72]. The loss compensation control injects real power into the buffer branch to charge capacitor C_2, resulting in residual ac ripple that can be seen in the dc-link current and voltage waveforms i_{in} and v_{bus}. Fig. 4.1 shows this residual ripple, which is greater than 10% of the average dc-link current in this representative example. While this residual ac ripple is not a problem in systems with relatively large R_s, such as in a PV application presented in [28], in systems with small R_s (such as battery systems, where R_s can be less than 1Ω [73]), the corresponding ripple can be a limiting factor in the SSB's effectiveness in buffering energy and maintaining the dc-link's voltage requirement.

This chapter presents a new charge injection technique that provides loss compensation to the SSB, substantially reducing the twice-line ac ripple coupled to the dc-link. The new

charge injection method entirely removes the twice-line frequency power pulsation on the dc-link by adding another circuit branch and control loop. The remainder of this chapter is organized as follows: Section 4.2 discusses the control and theory of a traditional SSB and how its traditional loss compensation control introduces residual ac ripple coupled to the dc-link; Section 4.3 introduces the circuit operation and control of the proposed charge injection technique; Section 4.4 presents experimental results of a 1.5 kW, 400 V-rated SSB hardware prototype demonstrating improvements in the current ripple and its efficiency compared to the traditional control method; and lastly, Section 4.5 concludes this chapter.

4.2 Series-Stacked Buffer Principles of Operation

SSB Operation in Ideal Conditions

Fig. 4.1 shows an SSB connected in parallel with dc source voltage $V_{\rm dc}$ and a modeled inverter current load $i_{\rm inv}$ that is described in [54]. In the SSB branch, capacitor C_1 serves as the primary energy storage component and is allowed to have a relatively large ac voltage ripple. Assuming no power loss in the SSB converter and that the full ac current $i_{\rm dc}\sin(\omega_{\rm 2L}t)$ from the modeled inverter load flows fully through the SSB branch, the voltage across C_1 is

$$v_{\rm C1}(t) = v_{\rm bus} + \frac{i_{\rm dc}}{\omega_{\rm 2L}C_1}\cos(\omega_{\rm 2L}t) = v_{\rm bus} + v_{\rm C1,ac}(t). \tag{4.2}$$

A bidirectional full-bridge converter, with capacitor C_2 acting as its dc voltage source, is placed in series with C_1. Assuming that there are zero power losses in the SSB, the full-bridge converter can be controlled to produce the ac output voltage $v_{\rm ab}$ = -$v_{\rm C1,ac}(t)$ that exactly cancels the voltage ripple on C_1, making $v_{\rm bus}$ purely dc. Thus, in this ideal case, the power processed by the SSB is strictly reactive. In this ideal lossless buffer system, the full-bridge converter in the SSB operation can be controlled with the proposed control and sensing shown in the "Reactive Control" block of Fig. 4.2.

SSB in Real Conditions and Required Loss Compensation Control

In a practical hardware implementation, due to unavoidable power conversion losses in the SSB branch, the dc source capacitor C_2 continuously loses energy, and its dc-offset voltage $v_{\rm C2,dc}$ decays over time. When this occurs, the SSB does not effectively buffer the twice-line frequency power pulsation. Fig. 4.3 shows simulated waveforms for the SSB with losses modeled when it is controlled with only the Reactive Control block in Fig. 4.2 (i.e. when no loss compensation control is implemented). Before time $t = 0$ seconds, capacitors C_1 and C_2 are charged to their required steady-state voltages for a 1.5 kW system operation with a dc bus voltage of 400 V. The system turns on at $t = 0$ seconds, and $v_{\rm C2,dc}$ immediately begins to decay due to the real power dissipation in the SSB circuit branch. Consequently, $v_{\rm C2}(t)$ becomes strictly less than the peak ac voltage of C_1, $v_{\rm C1,ac,pk}$. Thus, the voltage produced by

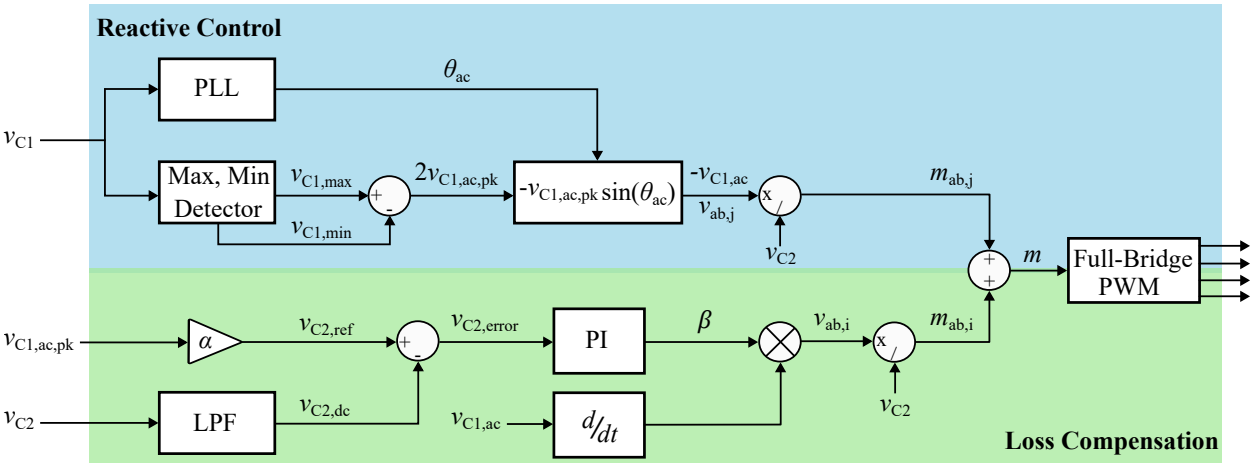


Figure 4.2: The reactive and loss compensation control blocks for a traditional SSB.

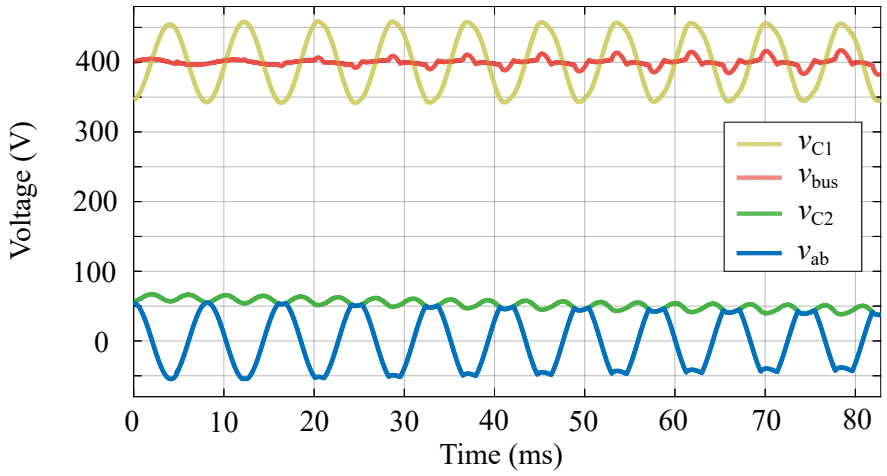


Figure 4.3: Voltage waveforms for a SSB when no loss compensation control is implemented. Before time $t = 0$, capacitors C_1 and C_2 are charged to nominal amounts for a 1.5 kW, 400 V system operation.

the full-bridge converter v_{ab} begins to saturate, which prevents the SSB from fully buffering the dc-link's ac ripple. To maintain the voltage on C_2, real power can be injected into capacitor C_2 through the SSB branch with additional loss compensation control, as described in [72].

Fig. 4.2 shows the SSB control diagram, including the "Loss Compensation" control block. As shown in [72], allowing real power to flow through the reactive buffer branch for loss compensation causes an undesirable phase shift between v_{ab} and $-v_{C1,ac}$. This can be better understood with the phasor diagrams shown in Fig. 4.4. In Fig. 4.4a, when the

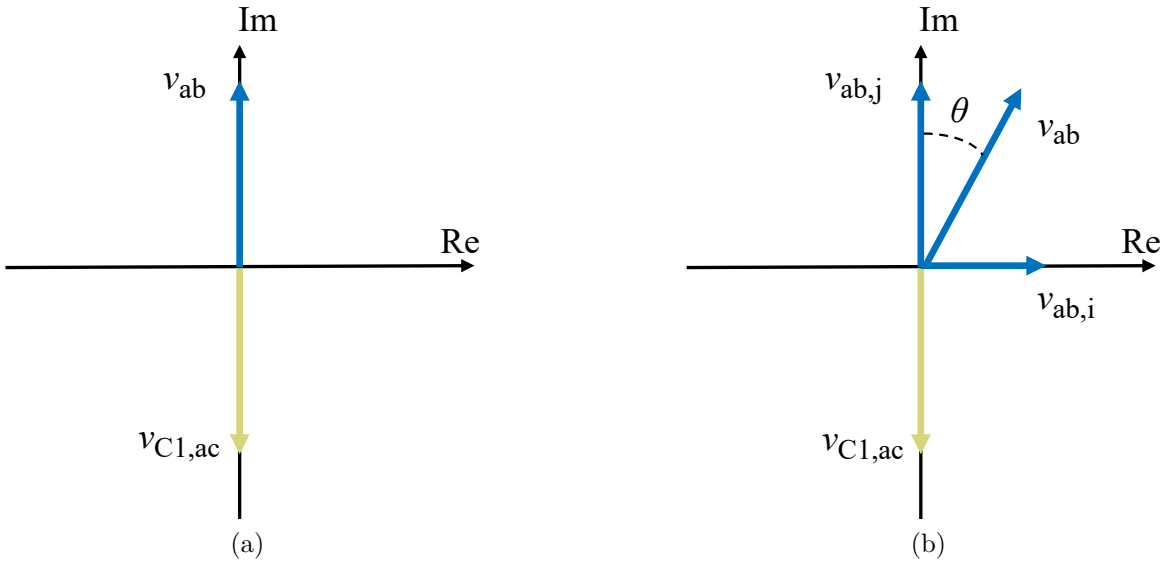


Figure 4.4: Phasor diagram of the voltages v_{ab} and v_{C1} based on (a) solely the reactive control diagram in Fig. 4.2 for a lossless SSB and (b) the combined reactive and loss compensation controls in Fig. 4.2

.

SSB generates zero power loss, no loss compensation control is required, and the phasors corresponding to voltages v_{C1} and v_{ab} are of the same magnitude and are 180° out of phase with one another. Conversely, in Fig. 4.4b the phasor corresponding to voltage v_{ab} is now the sum of reactive phasor component $v_{ab,j}$ and real phasor component $v_{ab,i}$, which are respectively generated from the reactive and loss compensation control blocks. Due to the change in phase and magnitude of the v_{ab} waveform compared to the lossless case, the sum $v_{C1} + v_{ab}$ is no longer strictly dc and leaves a residual amount of ac voltage ripple coupled to v_{bus}. This also causes ac current ripple coupled to i_{in}, negatively impacting system operation. If the load current i_{inv} is known, i_{in} can be approximated as follows:

$$\begin{aligned} i_{in}(t) &= i_{dc} + i_{dc}\frac{R_{ab}}{R_s + R_{ab}}\sin(\omega_{2L}t) \\ &= i_{in,dc} + i_{in,ac}\sin(\omega_{2L}t), \end{aligned} \tag{4.3}$$

where R_{ab} is the reactive branch's modeled resistance due to the branch's power loss. As shown in [74], an expression for the resistance modeled in the SSB branch can be derived based on the power loss inside the SSB branch. The impedance divider in (4.3) can be better visualized through conducting superposition ac analysis on the traditional SSB schematic shown in Fig. 4.1. To do so, the dc input voltage source V_{dc} is replaced with a short-circuit, and the dc component of the modeled inverter load current i_{dc} can be removed, resulting in an ac-only currently source. As shown in [72], capacitor C_1 and the SSB can be replaced with an equivalent RLC circuit, where the L and C resonate at the twice-line frequency

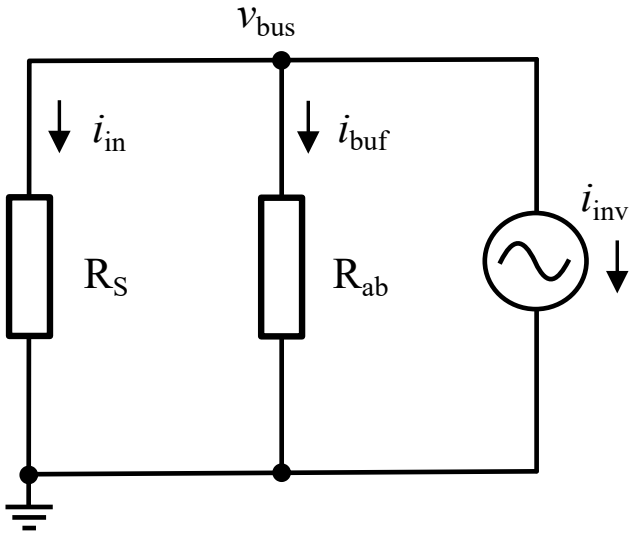


Figure 4.5: The SSB schematic is simplified as an impedance divider to estimate the ac current ripple coupled to the dc-link current.

ω_{2L}. Thus, the LC components can be simplified as a short circuit, leaving the SSB branch modeled solely with resistance R_{ab}. Fig. 4.5 shows the resulting impedance divider circuit.

As shown in (4.3), the ac ripple that is coupled to the dc-link current $i_{in,ac}$ is dependent on the dc voltage source impedance R_s and the power loss in the SSB branch. However, R_s is often a fixed parameter based on the input dc source that cannot be adjusted. In particular for sources with voltage-source behavior (e.g., batteries), the very low R_s makes the loss compensation technique challenging to utilize in practice due to the large ac ripple that couples to the dc-link.

4.3 Charge Injection

Figs. 4.6 and 4.7 display the schematic and the control diagram for the proposed charge injection method, respectively. The charge injection circuitry is an additional branch that periodically draws power from the dc bus onto capacitor C_2 to keep C_2 charged. The charge injection circuit consists of three components: switch S_{CI}, inductor L_{CI}, and diode D_{CI}. This loss compensation method injects real power into the SSB without compromising the phase shift and magnitude of v_{ab}. As a result, the phase shift and magnitude change of v_{ab} is eliminated, and the full-bridge converter can be modulated such that $v_{ab} = -v_{C1,ac}$. Consequently, the twice-line frequency voltage coupled to v_{bus} and the current coupled to i_{in} are further reduced. This is shown in the exemplary waveforms of Fig. 4.6, where $i_{in,ac}$ is reduced by a factor of five in comparison to the traditional loss compensation method simulation shown in Fig. 4.1. The y-axis limits for the voltage and current waveforms in

Fig. 4.6 are set equal to that in Fig. 4.1 to further demonstrate the reduction in dc-link ripple.

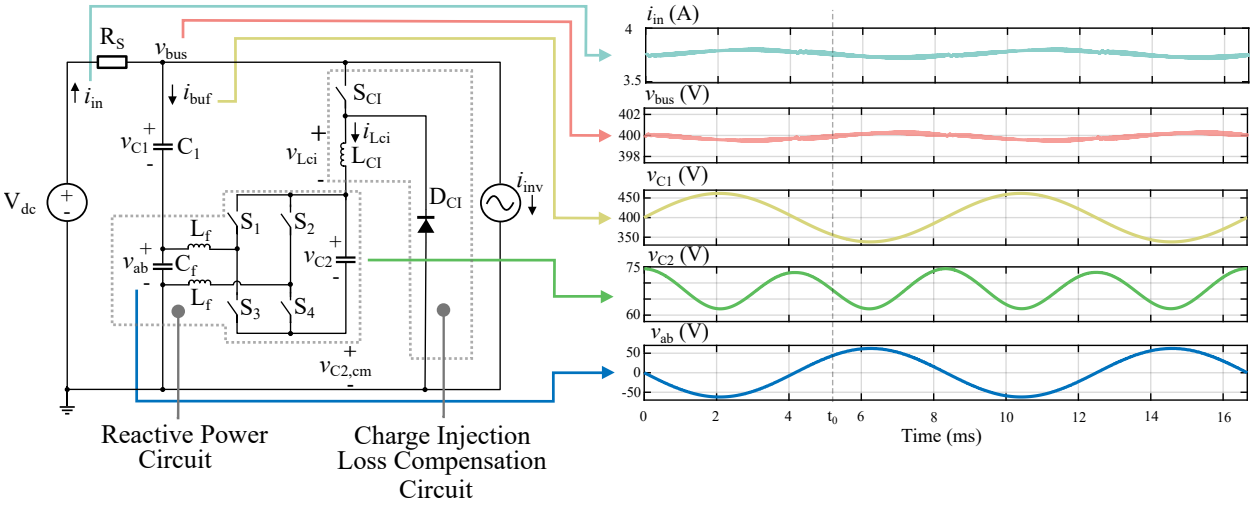


Figure 4.6: Schematic of a SSB with charge injection circuit connected to a dc voltage source and a modeled inverter current load. Voltage and current waveforms of the system are displayed for a 1.5 kW system operation where $v_{\text{bus,dc}} = 400$ V, $i_{\text{dc}} = 3.75$ A, $C_1 = 80$ μF, $C_2 = 204$ μF, and $R_{\text{s}} = 10$ Ω. Time t_0 is labeled for the switching period example of the SSB with charge injection converter explained in Section 4.3.

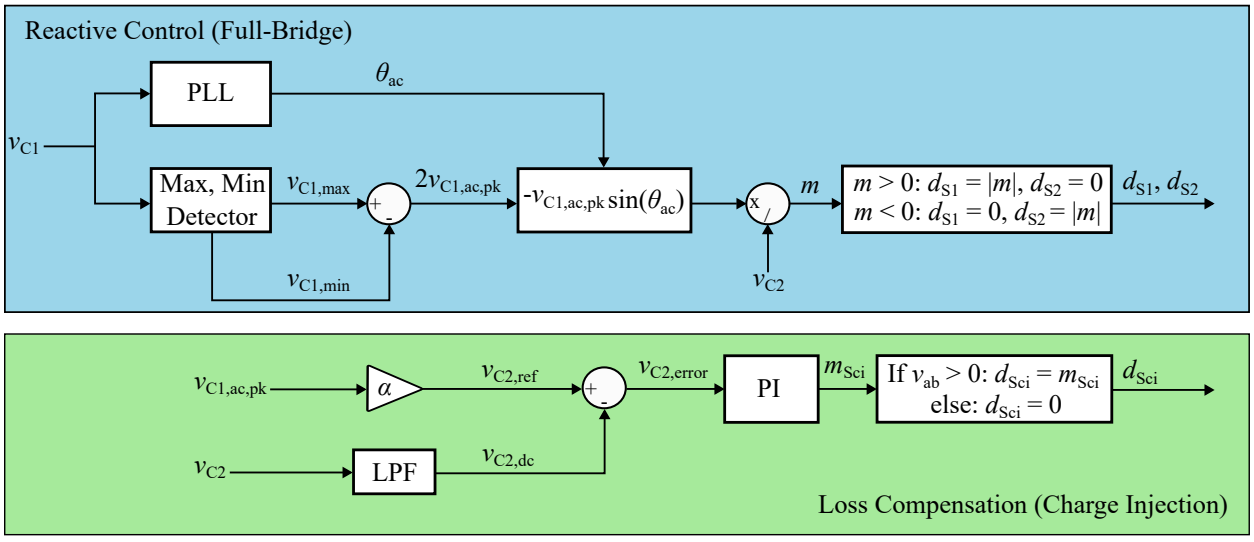


Figure 4.7: Reactive and loss compensation control diagrams for a SSB implemented with charge injection loss compensation control.

Reactive Power Control

The SSB with the charge injection method has the same reactive power control discussed in Section 4.2 with a modified unipolar modulation scheme to generate the PWM signals for the switches in the full-bridge. In the SSB with the traditional loss compensation control, a conventional unipolar modulation scheme is used as described in [75]. In the conventional unipolar modulation, the full-bridge converter shorts its ac output by simultaneously conducting switches S_1 and S_2, or by simultaneously conducting switches S_3 and S_4. However, it is undesirable to simultaneously conduct switches S_1 and S_2 in the charge injection method because when these switches are both on, the negative terminal of C_2 is left floating, consequently leaving no closed loop path for the charge injection circuit to deliver charge to C_2. Conversely, during the simultaneous conduction of switches S_3 and S_4, the negative terminal of C_2 is no longer left floating, and hence there is a closed loop path for C_2 to receive charge through the charge injection circuit. Therefore, to ensure that the charge injection circuit can deliver charge to C_2 each switching cycle, the modulation scheme was modified to eliminate the simultaneous conduction state of switches S_1 and S_2. The duty cycle for switches S_1 and S_2 are calculated from the modulation index m of the full-bridge converter as follows:

$$\begin{aligned} m > 0 \;\; (v_{\text{ab}} > 0 \text{ V}) : d_{\text{S1}} &= |m|, \; d_{\text{S2}} = 0, \\ m < 0 \;\; (v_{\text{ab}} < 0 \text{ V}) : d_{\text{S1}} &= 0, \; d_{\text{S2}} = |m|. \end{aligned} \tag{4.4}$$

When v_{ab} is larger than 0 V, S_4 is turned on and the half-bridge with switches S_1 and S_3 is modulated with duty cycle d_{S1} equal to $|m|$. During this (positive) half of the twice-line frequency cycle, only the simultaneous conduction of switches S_1 and S_4, and the simultaneous conduction of S_3 and S_4 are permitted. Similarly, during the (negative) half of the twice-line frequency cycle, when v_{ab} is less than 0 V, S_3 is turned on and the half-bridge with switches S_2 and S_4 are modulated with duty cycle d_{S2} equal to $|m|$. During this second half of the twice-line frequency cycle, only the simultaneous conduction of switches S_2 and S_3 and switches S_3 and S_4 are permitted. As a result, the undesired circuit state where switches S_1 and S_2 simultaneously conduct is avoided completely, and charge can be injected into C_2 through the charge injection circuitry over the entire twice-line period.

Charge Injection Loss Compensation Control

With the modulation technique proposed above, the charge injection methodology can be viewed as a buck converter with a voltage feedback loop that regulates $v_{\text{C2,dc}}$ and drives capacitive load C_2. To ensure that $v_{\text{C2,dc}}$ is at its desired value, and hence C_2 is charged sufficiently, a reference value for $v_{\text{C2,dc}}$ is obtained. As described in [76], the reference value for $v_{\text{C2,dc}}$ is the product

$$v_{C2,dc,ref} = \sqrt{\frac{2C_2 + C_1}{2C_2}} v_{\text{C1,ac,pk}} = \alpha v_{\text{C1,ac,pk}}, \tag{4.5}$$

where $v_{\mathrm{C1,ac,pk}}$ is the amplitude of the twice-line frequency ac ripple of v_{C1} and α represents the constant square root term shown in (4.5). The variable α is derived from the potential maximum peak values of v_{C1} and v_{C2}:

$$v_{\mathrm{C1,max}} = v_{\mathrm{bus}} + \frac{i_{\mathrm{dc}}}{\omega_{\mathrm{2L}} C_1}, \tag{4.6}$$

$$v_{\mathrm{C2,max}} = \sqrt{v_{\mathrm{C2}}^2 + \frac{i_{\mathrm{dc}}^2}{2\omega_{\mathrm{2L}}^2 C_1 C_2}}\ . \tag{4.7}$$

From this, an optimization constraint can be derived which determines the value of the peak value of C_2, or rather α:

$$\frac{i_{\mathrm{dc}}}{\omega_{\mathrm{2L}}} - C_1 v_{\mathrm{C2,dc}} \sqrt{\frac{2C_2}{2C_2 + C_1}} \leq 0. \tag{4.8}$$

It should be noted that $v_{\mathrm{C2,dc,ref}}$ is derived from the simplifying assumption that the total twice-line frequency current $i_{\mathrm{dc}}\sin(\omega_{\mathrm{2L}} t)$ is injected into the SSB branch and no fraction of the current transverses through the dc-link. Although not strictly correct, this assumption yields good results that have been validated in the hardware of this work and several others [30], [31], [74], [77]–[80].

With a dc reference obtained for v_{C2}, an error term is calculated and fed into a proportional-integral (PI) voltage compensator. The output of the compensator is the duty cycle for the charge injection switch $\mathrm{S_{CI}}$.

Charge Injection Hardware Operation

The proposed charge injection circuit and control technique are designed to operate in the discontinuous conduction mode (DCM) since the SSB branch has a small amount of power loss and thus $\mathrm{C_2}$ requires a small amount of charge delivery per switching period. When $\mathrm{S_{CI}}$ and $\mathrm{D_{CI}}$ are both off, there is no current flow through any of the charge injection components and hence no charge delivery to $\mathrm{C_2}$. The full-bridge converter continues to operate such that $v_{\mathrm{ab}} = -v_{\mathrm{C1,ac}}$ and to buffer the twice-line frequency power pulsation.

When $\mathrm{S_{CI}}$ turns on, the charge injection inductor current i_{Lci} begins to increase linearly from 0 A and inject charge into $\mathrm{C_2}$. The slope of i_{Lci} is based on the voltage across $\mathrm{L_{CI}}$:

$$v_{\mathrm{Lci}} = v_{\mathrm{bus}} - (v_{\mathrm{C2}} + v_{\mathrm{C2,cm}}), \tag{4.9}$$

where $v_{\mathrm{C2,cm}}$ is the common-mode voltage of $\mathrm{C_2}$, defined as the voltage of the negative terminal of $\mathrm{C_2}$ with respect to ground, which is dependent on the state of operation of the full-bridge circuit, therefore, although the control between the reactive and real branches of the SSB are decoupled from one another, the ac voltage v_{ab} that is produced by the full-bridge converter affects the rate of the charge delivered to $\mathrm{C_2}$. There are a total of twelve unique circuit states of the combined full-bridge and charge injection circuits that

Table 4.1: Series-Stacked Buffer with charge injection method circuit states of operation

State	v_{ab} Orientation	Full-Bridge Switches	Charge Injection Switch	v_{Lci}
I	positive	S_3 and S_4 on	S_{CI} and D_{CI} off	0 V
II	positive	S_1 and S_4 on	S_{CI} and D_{CI} off	0 V
III	positive	S_1 and S_4 on	S_{CI} on, D_{CI} off	$\frac{v_{\text{ab}}-v_{C2}+2v_{C1}}{2+\frac{L_f}{L_{CI}}}$
IV	positive	S_1 and S_4 on	S_{CI} off, D_{CI} on	$-\frac{\frac{1}{2}(v_{ab}+v_{C2})}{1+\frac{1}{2}\frac{L_f}{L_{CI}}}$
V	positive	S_3 and S_4 on	S_{CI} off, D_{CI} on	$-\frac{(\frac{1}{2}v_{ab}+v_{C2})}{1+\frac{1}{2}\frac{L_f}{L_{CI}}}$
VI	positive	S_3 and S_4 on	S_{CI} on, D_{CI} off	$\frac{v_{\text{ab}}-2v_{C2}+2v_{C1}}{2+\frac{L_f}{L_{CI}}}$
VII	negative	S_3 and S_4 on	S_{CI} and D_{CI} off	0 V
VIII	negative	S_2 and S_3 on	S_{CI} and D_{CI} off	0 V
IX	negative	S_2 and S_3 on	S_{CI} on, D_{CI} off	$\frac{v_{\text{ab}}-v_{C2}+2v_{C1}}{2+\frac{L_f}{L_{CI}}}$
X	negative	S_2 and S_3 on	S_{CI} off, D_{CI} on	$-\frac{\frac{1}{2}(v_{ab}+v_{C2})}{1+\frac{1}{2}\frac{L_f}{L_{CI}}}$
XI	negative	S_3 and S_4 on	S_{CI} off, D_{CI} on	$-\frac{(\frac{1}{2}v_{ab}+v_{C2})}{1+\frac{1}{2}\frac{L_f}{L_{CI}}}$
XII	negative	S_3 and S_4 on	S_{CI} on, D_{CI} off	$\frac{v_{\text{ab}}-2v_{C2}+2v_{C1}}{2+\frac{L_f}{L_{CI}}}$

provide distinct values for the slope of i_{Lci}. Table 4.1 displays the SSB circuit states and their effective voltage v_{Lci}. Note, not all of these circuit states listed in Table 4.1 occur in each switching period; the circuit state may or may not happen based on the location of the twice-line frequency period that the switching period occurs. The occurrence of the circuit state depends on the amount of the time that the charge injection circuit is on, which is dependent on the amount of charge injected into C_2 dictated by the closed-loop control. This is arithmetically complex to equate, not necessary to know for the charge injection circuit to function and to keep C_2 charged, and is therefore left out of this chapter.

When S_{CI} turns off, diode D_{CI} begins to conduct to freewheel the current through the inductor L_{CI} as well as the full-bridge filter inductors L_f. Inductor L_{CI} is connected to the ground, and the voltage across the inductor v_{Lci} is negative, causing the slope of i_{Lci} to be negative and hence i_{Lci} to decrease. When i_{Lci} reaches 0 A, all of the elements in the charge injection circuit are no longer conducting current, and the charge injection circuit is turned off until the next switching period.

Example of the SSB Charge Injection Operation

To demonstrate how the charge injection loss compensation method operates in tandem with the full-bridge converter, exemplary waveforms of currents i_{Lci} and i_{C2} throughout one

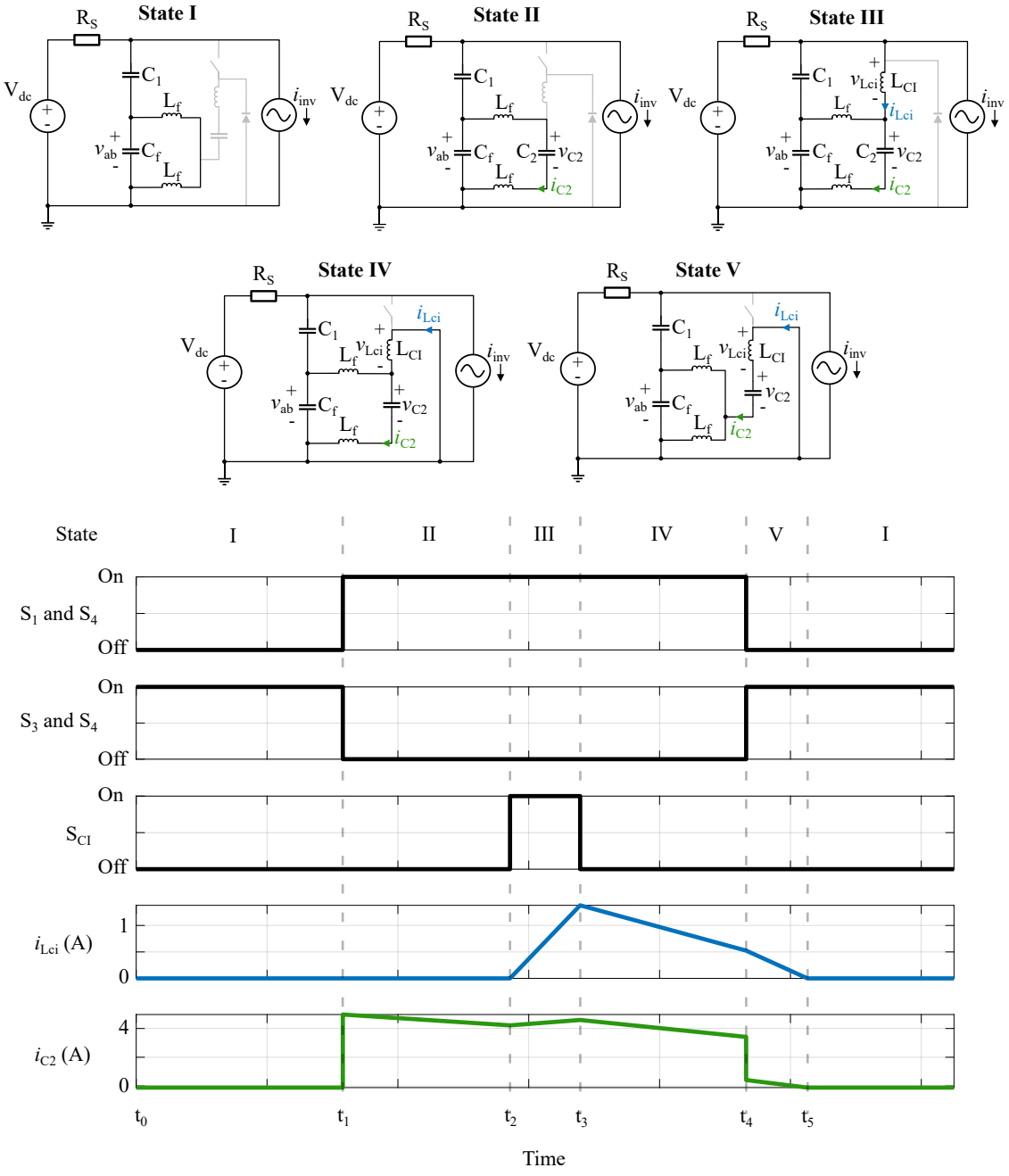


Figure 4.8: Simulated operation of the SSB with charge injection method during one switching period. Both the charge injection and full-bridge circuits are operated at 160 kHz where the PWM for S_{CI} is delayed by time t_2. The circuit states shown in this example are described in Table 4.1. Fig. 4.6 shows where time t_0 occurs in the twice-line frequency period.

switching period are shown in Fig. 4.8. In this example, the full-bridge and charge injection switch operate at the same frequency of 160 kHz. However, switch S_{CI} has a time delay of t_2 seconds. Moreover, this example takes place when the full-bridge converter is being modulated to produce an output voltage greater than 0 V (noted, $v_{ab} > 0$ V). As will be described in Section 4.3, the charge injection circuitry only operates when v_{ab} is positive. Therefore, this analysis only considers positive values of v_{ab}. The start time of this example is highlighted in system waveforms shown in Fig. 4.6. Moreover, as stated in the previous sub-section, not all of the circuit states listed in Table 4.1 occur in this example due to where it takes place in the twice-line frequency period. Specifically, State VI does not occur in this switching period example.

At time $t = t_0$, the charge injection circuit is off, and the full-bridge converter is modulated to shunt the ac output. At time $t = t_1$, switch S_1 turns on while switch S_3 turns off in order to connect C_2 to the the ac output of the converter. Then at time $t = t_2$, the charge injection switch S_{CI} is turned on to enable power delivery to C_2. The slope of i_{Lci} can be calculated from the voltage across L_{CI}:

$$v_{Lci} = \frac{v_{ab} - v_{C2} + 2v_{C1}}{2 + \frac{L_f}{L_{CI}}}. \tag{4.10}$$

In this state, v_{ab}, v_{C2}, and v_{C1} are all positive values. However, v_{C1} is sufficiently larger than $v_{ab} - v_{C2}$ and effectively, all of the solutions for (4.10) are strictly positive. Therefore, current i_{Lci} will only increase when operating in this circuit state. Once i_{Lci} begins to increase, the slope of i_{C2} also increases, and charge is injected into C_2.

At time $t = t_3$, switch S_{CI} turns off and diode D_{CI} turns on to freewheel the inductor current. The SSB is now operating in circuit State IV, and the voltage across L_{CI} is equal to

$$v_{Lci} = -\frac{\frac{1}{2}(v_{ab} + v_{C2})}{1 + \frac{1}{2}\frac{L_f}{L_{CI}}}. \tag{4.11}$$

Note, the forward voltage across D_{CI} is ignored in (4.11). In this state, both v_{ab} and v_{C2} are positive values and all possible solutions to (4.11) are negative. Therefore, the slope of i_{Lci} is now negative. Effectively, the slope of i_{C2} decreases from its previous value, and i_{C2} is now decreasing over time.

At time $t = t_4$, the state of operation of the full-bridge converter changes to shunt the ac output. This is done by switch S_1 turning off and switch S_3 turning on. The voltage across L_{CI} is now:

$$v_{Lci} = -\frac{(\frac{1}{2}v_{ab} + v_{C2})}{1 + \frac{1}{2}\frac{L_f}{L_{CI}}}. \tag{4.12}$$

Note, the voltage drop across D_{CI} is ignored in (4.12). In this state, both v_{ab} and v_{C2} are positive values and all possible solutions to (4.12) are negative. Therefore, the slope of i_{Lci} changes to a slightly more negative value than in (4.11), and the slope of i_{C2} also decreases.

At $t = t_5$, i_{Lci} has fully discharged to 0 A, D_{CI} stops conducting and the charge injection circuit is no longer in operation. The circuit has returned to the same state in sub-period

1, and the full-bridge continues to operate alone until the next switching period when the charge injection circuit turns on again.

Disabling Charge Injection Circuit when $v_{\mathbf{ab}} < \mathbf{0}$ V

The only circuit state that affects the charge injection circuit in an undesirable manner is State X in Table 4.1. As depicted in Fig. 4.9, this state occurs when the full-bridge converter is modulated to produce a negative output voltage of $v_{\mathrm{ab}} < 0$ V while diode $\mathrm{D_{CI}}$ is conducting. During this state, the voltage across inductor $\mathrm{L_{CI}}$ is

$$v_{\mathrm{Lci}} = -\frac{\frac{1}{2}(v_{ab} + v_{\mathrm{C2}})}{1 + \frac{1}{2}\frac{L_{\mathrm{f}}}{L_{\mathrm{CI}}}}, \tag{4.13}$$

where v_{ab} is less than 0 V and v_{C2} is strictly positive. As v_{ab} becomes more negative, the solution of (4.13) becomes less negative. As a result, the slope of the current becomes less negative and approaches a value of zero, preventing i_{Lci} from fully decreasing to 0 A. During this time, the charge injection circuit reaches an unstable continuous conduction mode (CCM) state where i_{Lci} continually increases each switching period to an uncontrollable amount. Fig. 4.10 shows this event in simulation.

The unstable CCM operation that occurs in State X can cause $\mathrm{L_{CI}}$ to saturate, prevent the charge injection circuit from delivering charge to $\mathrm{C_2}$, and potentially cause a system failure. To prevent this from occurring, the charge injection circuit is chosen only to operate when $v_{\mathrm{ab}} > 0$ V. This is shown in the charge injection control block in Fig. 4.7. Once the PI voltage compensator calculates the modulation index m_{Sci} for switch $\mathrm{S_{CI}}$, the modulation index for the full-bridge m is compared to the value 0 V. If m is greater than 0 V, voltage v_{ab} is greater than 0 V and the duty cycle for switch $\mathrm{S_{CI}}$ is set to m_{Sci}. Conversely, if m is less than 0 V, voltage v_{ab} is less than 0 V and the duty cycle for switch $\mathrm{S_{CI}}$ is set to 0 and the charge injection circuit is turned off.

By allowing the charge injection circuit to operate strictly during the positive half cycle of the twice-line period, the current ripple through $\mathrm{L_{CI}}$ will be doubled in comparison to allowing the charge injection circuit to operate throughout the entirety of the twice-line period. To reduce the current ripple, the charge injection circuit can be tuned to operate during a certain duration of the negative half-cycle period when $v_{\mathrm{ab}} < 0\ V$, as long as the charge injection circuit is turned off before the current i_{Lci} enters the boundary conduction mode. This will reduce the current ripple of inductor $\mathrm{L_{CI}}$.

4.4 Experimental Results

A 1.5 kW Series-Stacked Buffer with charge injection hardware prototype was designed and built to validate the charge injection loss compensation method. The control for the prototype was implemented digitally using a Texas Instruments F28379D ControlCARD. Fig. 4.11 displays the hardware prototype annotated with relevant charge injection and SSB

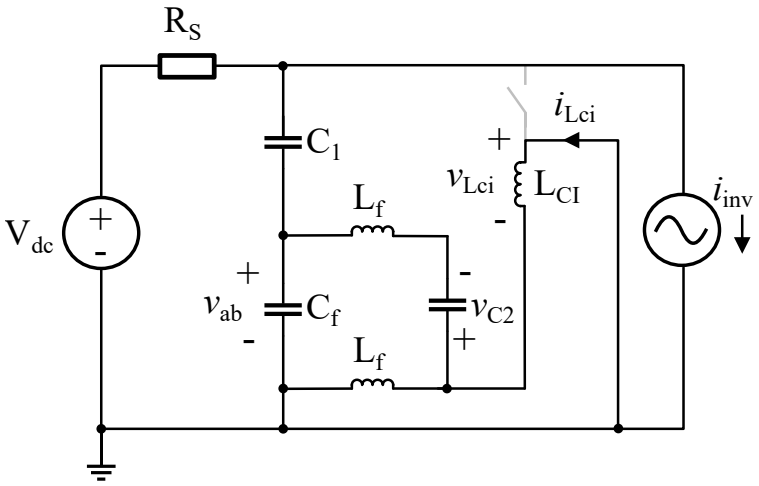


Figure 4.9: State X of the SSB and charge injection combined circuit.

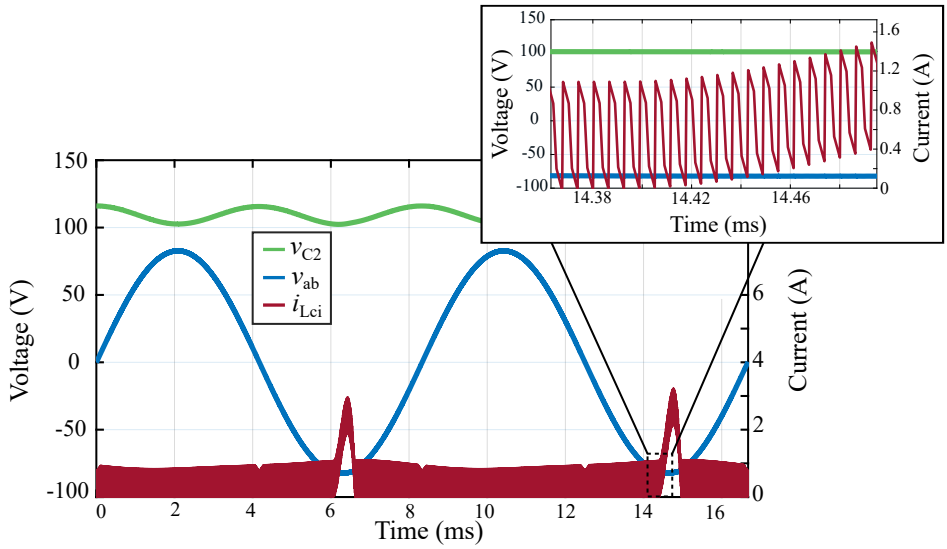


Figure 4.10: Simulated occurrence of the charge injection circuit entering CCM due to the voltage v_{Lci} in circuit state X.

components. The SSB switching cell comprises the four active switches and gate drive components for the full-bridge converter of the SSB. The components used in the hardware prototype are listed in Table 4.2. The prototype was tested using the charge injection method and the traditional loss compensation method up to 1.5 kW with a rated dc bus of $v_{\text{bus,dc}} = 400$ V. A MagnaPower TSD1000 was used for the dc source V_{dc} and a Chroma 63204 DC electronic load was used for the output inverter-modeled load i_{inv}.

Fig. 4.12 shows the steady state waveforms for the SSB with charge injection method at

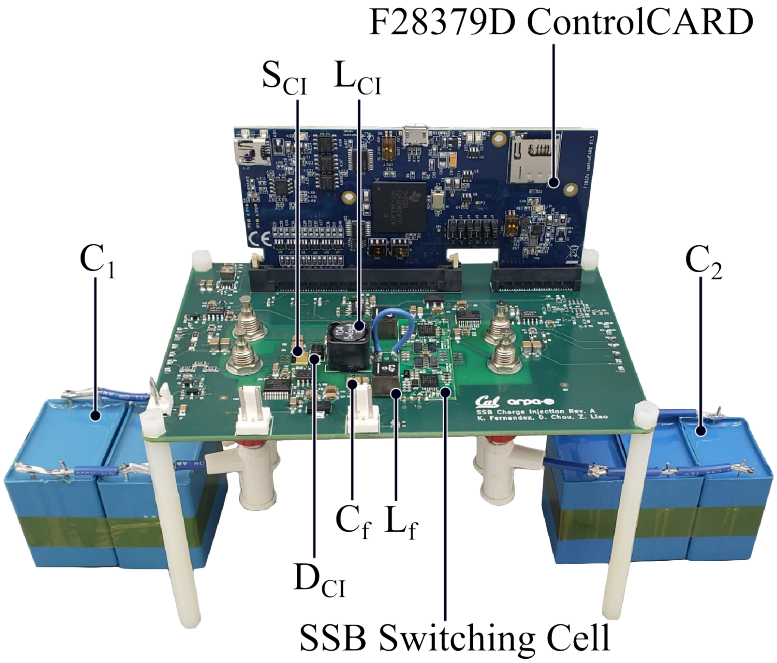


Figure 4.11: Hardware prototype of the SSB with charge injection method that is rated for 1.5 kW. A list of components used in the prototype can be found in Table 4.2.

Table 4.2: Component listing of the SSB with Charge Injection hardware prototype

Component	Part No.	Parameters
S_1, S_2, S_3, and S_4	EPC 2033	150 V, 7 mΩ
S_{CI}	GaN Systems GS66506T	650 V, 67 mΩ
D_{CI}	ON Semiconductor MURS160T3G	600 V, 2 A
L_{CI}	Coilcraft MSS1210-104	100 μH
L_f	Coilcraft XAL7070-473	47 μH x 2
C_1	TDK B32524Q1686K000	100 V, 68 μF x 3
C_2	TDK B32776G4406K000	450 V, 40 μF x 2

1.5 kW and $v_{\text{bus,dc}} = 400$ V. The waveforms for v_{C1}, v_{C2}, and v_{ab} are consistent with the simulated waveforms shown in Fig. 4.6. Fig. 4.13 shows the steady state waveforms for the SSB using the traditional loss compensation method at 1.5 kW and $v_{\text{bus,dc}} = 400$ V. Fig. 4.15 shows the system during a load step from 1.5 kW to 750 W with a rated dc bus of 400 V_{dc} at full load. These waveforms were recorded using a Keysight MSOX4024A oscilloscope. Figs. 4.12 and 4.13 both display the peak-to-peak current ripple for the dc-link current i_{in}. The charge injection method obtains a dc-link peak-to-peak current ripple of 300 mA, while the traditional loss compensation method obtains a dc-link peak-to-peak current ripple of 880 mA. Thus, at the full power and voltage rating, there is a 2.9× reduction in the dc-link

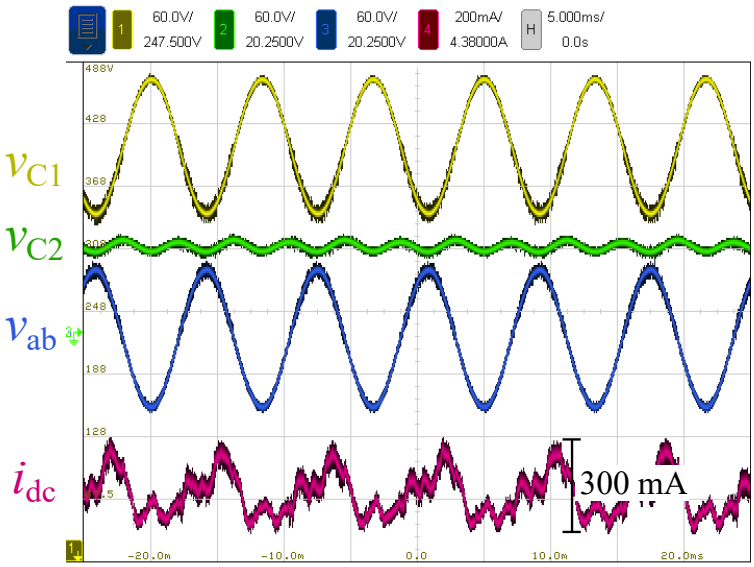


Figure 4.12: Steady state waveforms of v_{C1} (yellow), v_{C2} (green). v_{ab} (blue) and i_{in} (pink) for the SSB implemented with the charge injection loss compensation control at 1.5 kW with $v_{bus,dc} = 400$ V.

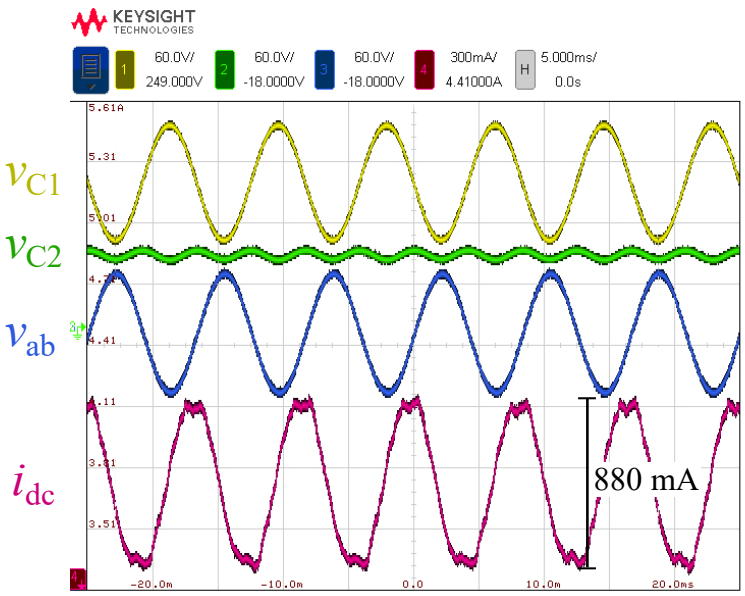


Figure 4.13: Steady state waveforms of v_{C1} (yellow), v_{C2} (green). v_{ab} (blue) and i_{in} (pink) of the SSB implemented with the traditional control proposed in [72] at 1.5 kW with $v_{bus,dc} = 400$ V.

current ripple when using the charge injection method. Note that the y-axis scaling for i_{in} in Fig. 4.12 is 200 mA/div while the y-axis scaling for the traditional loss compensation method in Fig. 4.13 is 300 mA/div.

The efficiency and peak-to-peak input current ripple of the charge injection method and the traditional loss compensation method over a power range from 500 W to 1.5 kW are displayed in Fig. 4.14. Voltage, power, and current measurements of v_{bus}, i_{in}, and i_{inv} were recorded with a Keysight PA2203A over a time span of ten twice-line frequency cycles. The input and output power of both methods was averaged over the ten twice-line cycles to calculate the efficiency of each method at different power levels. Efficiency measurements do not include the gate drive power loss since it is negligible, as shown in Fig. 4.16. The maximum and minimum input current i_{in} was recorded over ten twice-line cycles to calculate the peak-to-peak input dc current ripple.

The peak-to-peak dc current ripple measured in the charge injection method is consistently four times smaller than the ripple of the traditional loss compensation method over

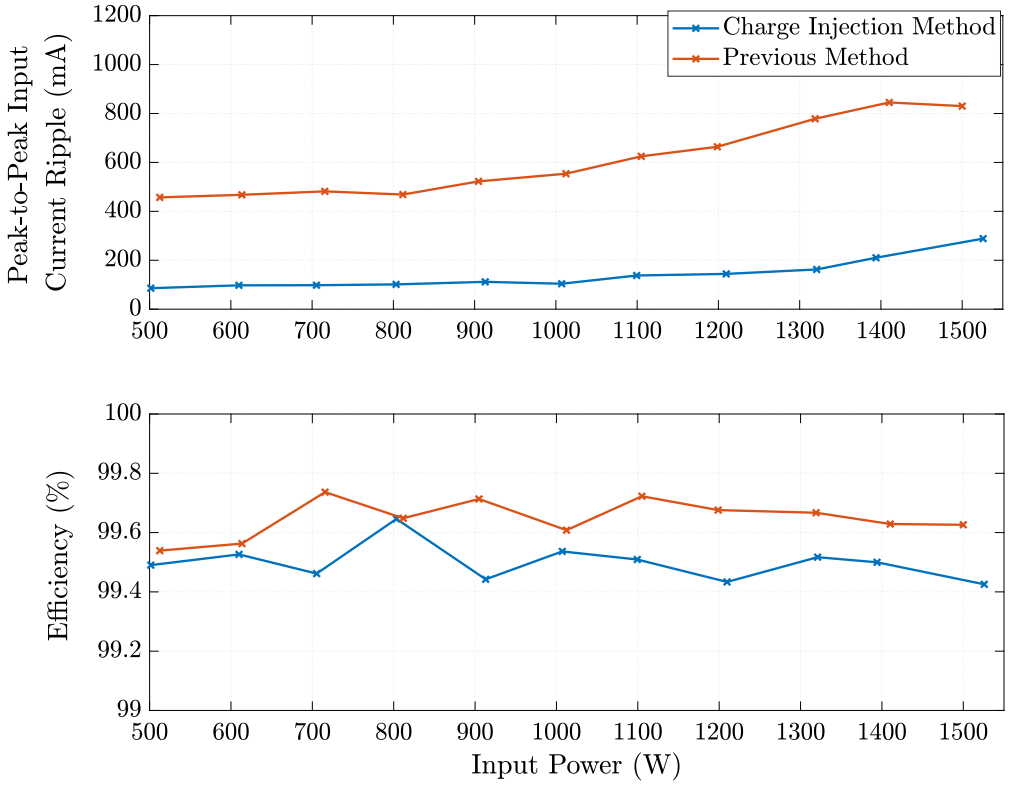


Figure 4.14: The peak-to-peak dc input current ripple and efficiency comparisons between the traditional loss compensation method highlighted in Section 4.2, and the charge injection method. Note, the efficiency curve does not include gate drive losses since they are negligible, as shown in Fig. 4.16.

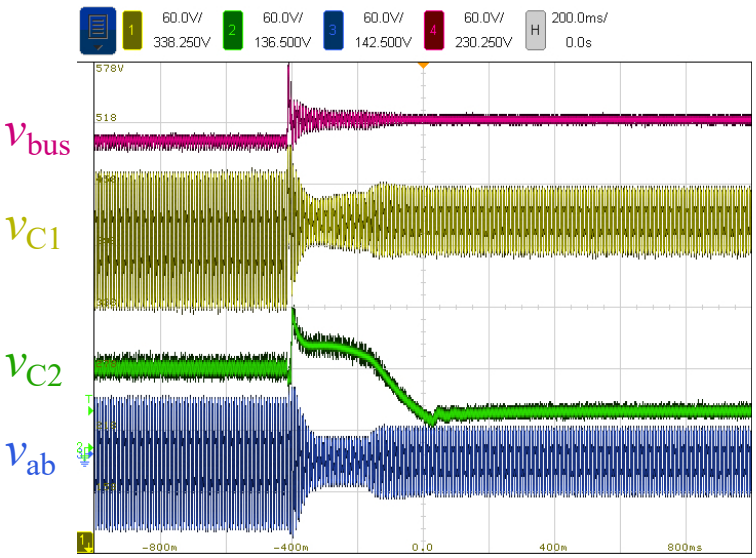


Figure 4.15: Waveforms of the SSB with charge injection method captured during a load step from 1.5 kW ($v_{\text{bus,dc}} = 400$ V) to 750 W.

the range of power levels from 500 W to 1.5 kW. The peak ripple reduction is achieved at 1 kW, where the peak-to-peak input current ripple of the charge injection method is more than five times smaller than the ripple of the traditional method. Moreover, the charge injection method significantly reduces the input current ripple with a negligible loss in efficiency in the buffer stage.

Although the charge injection method greatly reduces the peak-to-peak current ripple, i_{in} still contains some portion of the twice-line frequency ac ripple. This is partially due to a byproduct of errors associated with the analog to digital (ADC) sensing of v_{C1}, error in the PLL output θ, and the delays in the ADC sensing, MCU, and gate signal of full-bridge switches. The sensing circuitry can be improved further to reduce the peak-to-peak ripple of the dc input current, and a more advanced PLL such as the SOGI PLL [81] can be used. Even with perfect sensing control, and in the absence of delays, there will typically be a small amount of twice-line frequency ripple on the dc-link uncompensated losses in the SSB branch. These losses correspond to non-zero real impedance on the SSB branch that prevents the full ac current $i_{\text{dc}}\sin(\omega_{\text{2L}}t)$ from fully traversing through the SSB branch and partially flowing through the dc-link.

Fig. 4.16 displays the estimated loss breakdown of the SSB with the charge injection hardware at 1.5 kW and a dc bus voltage of 400 V. The reverse recovery and conduction losses for the charge injection diode D_{CI} are encompassed in the pie chart's hard switching and switch conduction loss categories, respectively. The most significant contributor to the power losses of the SSB hardware are the filter inductors L_{f}. This is due to the large DCR

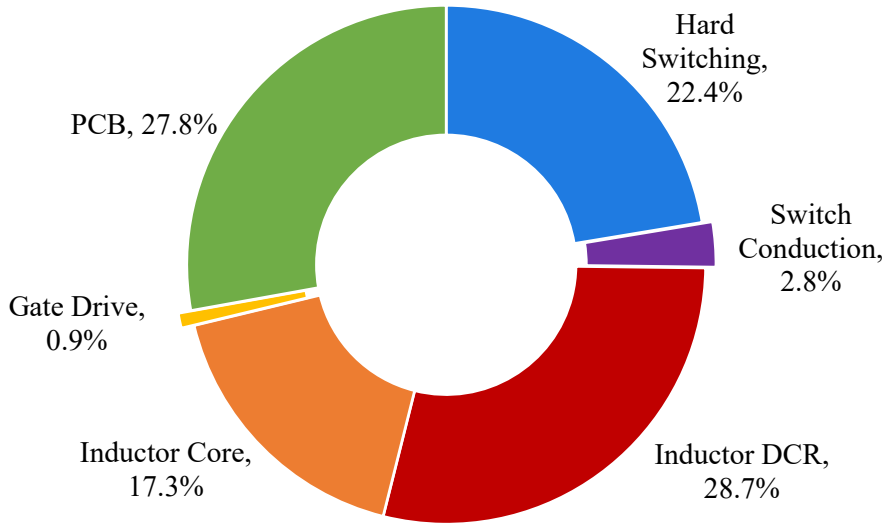


Figure 4.16: Estimated loss breakdown of SSB with charge injection circuit at 1.5 kW.

of the XAL7070-473 model, the large RMS currents of the filter inductors (due to the ac current $i_{dc}\sin(\omega_{2L}t)$, and the switching ripple of the combined full-bridge and charge injection circuitry). An inductor with a smaller DCR inductance can be selected for L_f to improve performance further. An example is the XAL7070-472 model used for the filter inductors in the SSB in [31].

4.5 Conclusion

This chapter describes how a Series-Stacked Buffer's traditional loss compensation control causes an undesirable, residual twice-line frequency current and voltage ripple on the dc-link. The charge injection method proposed in this work effectively decouples the reactive power buffering from the real power loss compensation and enables dc-link current and voltage ripple minimization. A proof-of-concept 1.5 kW, 400 V hardware prototype was built and tested to showcase the charge injection method. Experimental measurements at a power level up to 1.5 kW with a dc bus voltage of 400 V verify the ability of the charge injection method to reduce the twice-line frequency dc current and voltage ripple at the cost of a minor decrease in overall system efficiency. Suggestions to further improve the efficiency of the charge injection circuit are given.

Part II

Multi-Level Power Converters for Residential Solar Panel Microinverter Applications

Chapter 5

Residential Solar Panel Survey

5.1 Motivation for a Residential Solar Panel Survey

As residential photovoltaic (PV) panels have become increasingly popular as additional electrical energy-producing installments to residential homes, the advancement of microinverters, a sub-class of solar panel inverters specifically for residential applications, has become critical. A novel microinverter system topology is proposed in the second part of this thesis. The topology has three primary stages: a step-up dc to the converter, a high voltage (HV) energy buffer stage, and lastly, an inverting stage. This system solution was selected to evaluate what benefits and potential drawbacks a fixed-ratio resonant switched-capacitor converter (ReSC) converter can offer to the residential solar panel microinverter application space. The first stage of this solution is a ReSC that steps the input voltage up with a 1-to-N conversion ratio. A wide variety of residential solar panels were surveyed to select an appropriate step-up ratio and realize the required power handling capabilities of the converter.

5.2 Overview of Solar Panel Survey

In this survey, we wish to categorize anticipated voltage and power levels the proposed microinverter system should experience if connected to a residential solar panel. Therefore, the following seven solar panel manufacturers were chosen as a part of this survey:

- Jinko Solar
- JA Solar
- Trina Solar
- Longi Solar
- Canadian Solar

- LG
- Q-Cells

Each manufacturer's chosen datasheet for their residential solar panel products was studied. From each datasheet, the maximum power voltage V_{mp}, the open-circuit voltage V_{oc}, the short circuit current I_{sc}, and maximum rated power of the surveyed PV panel were recorded. Noted, the V_{mp}, V_{oc}, and I_{sc} under Standard Test Conditions (STC) were recorded as opposed to values under Nominal Operating Cell Temperature (NOCT) [82]. These parameters are defined as:

- Open-circuit voltage (V_{oc}) - the maximum voltage displaced across the solar panel, which occurs when no load is present.
- Short circuit current (I_{sc}) - the maximum current outputted from the solar panel when it experiences a shunt.
- Maximum power voltage (V_{mp}) - the voltage displaced across the solar panel when it is operating at its maximum power.

5.3 Findings of Solar Panel Survey

The open circuit voltage, short circuit current, and maximum power voltage are plotted versus the solar panel's maximum power and are shown in Figs. 5.1, 5.2, and 5.3, respectively. The data collected for each solar panel was averaged to select a nominal operating point for the proposed microinverter topology:

- Averaged open circuit voltage $< V_{oc} > = 43.4$ V,
- Averaged short circuit current $< I_{sc} > = 11$ A,
- Averaged maximum power voltage $< V_{mp} > = 36.3$ V,
- Averaged maximum power$< P_{max} > = 378$ W.

From the average surveyed results, the proposed microinverter system is designed to handle a 35 V_{dc} input. Because the microinverter must be equipped to 240 V_{ac} grid, the step-up converter is designed to step up the 35 V_{dc} input by a factor of ten such that HV dc bus of the system is rated for 350 V_{dc}. The inverting stage then inverts this dc waveform to create a 240 V_{ac} output. The microinverter must also be rated to have power-handling capabilities up to 400 W.

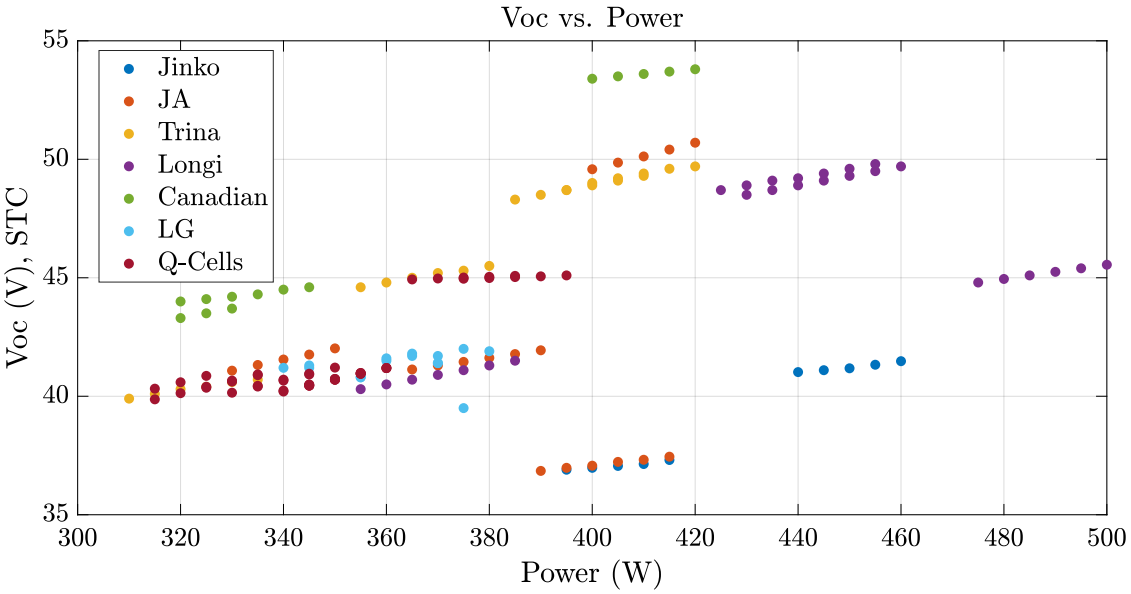


Figure 5.1: The open circuit voltage V_{oc} of various residential solar panels versus the rated power of the solar panel for standard testing conditions (STC). (Figure made in collaboration with Francesca Giardine.)

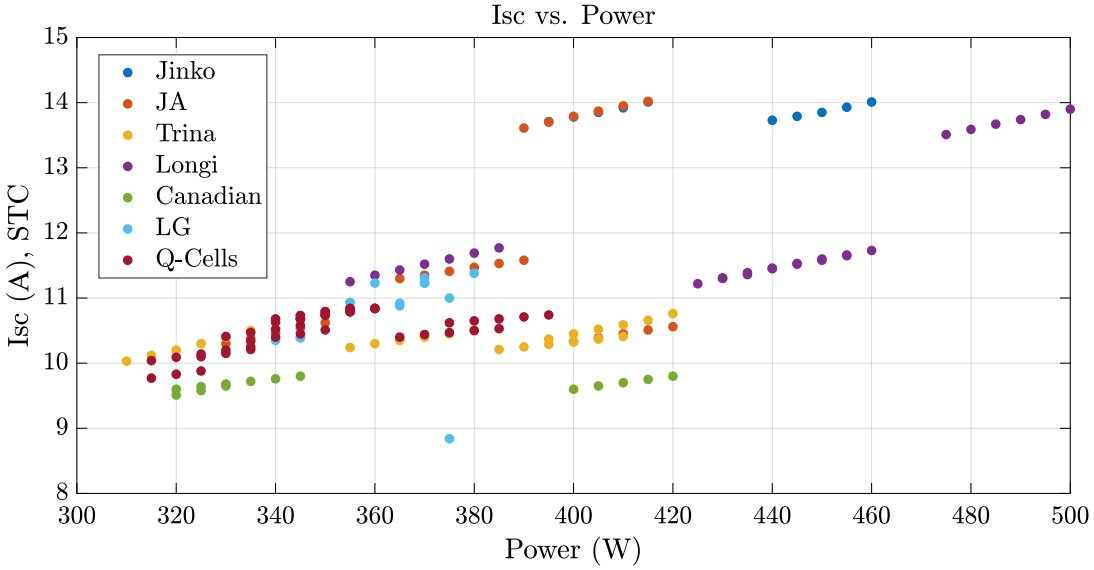


Figure 5.2: The short circuit current I_{sc} of various residential solar panels versus the rated power of the solar panel for standard testing conditions (STC). (Figure made in collaboration with Francesca Giardine.)

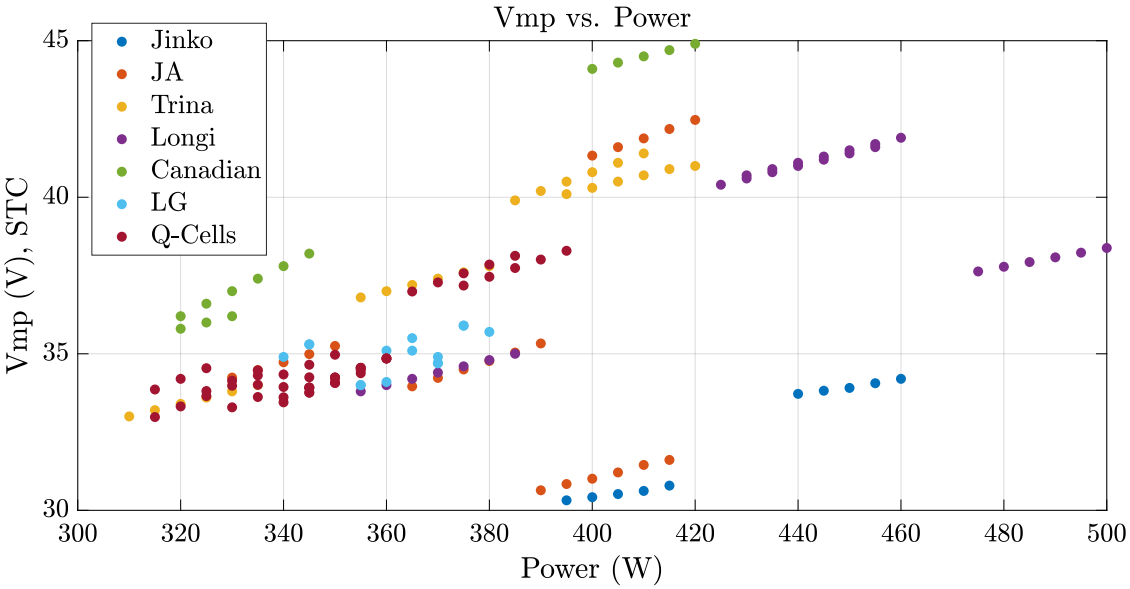


Figure 5.3: The maximum power voltage V_{mp} of various residential solar panels versus the rated power of the solar panel for standard testing conditions (STC). (Figure made in collaboration with Francesca Giardine.)

Chapter 6

A 1-to-10 Cascaded Series-Parallel Converter

6.1 Introduction

In many electrical systems, a low-voltage (LV) dc-source must be stepped up to a higher dc-voltage. Such areas include both commercial and residential photovoltaic inverters [7], [83], medical systems such as X-ray power generators and pulsed electric fields (PEFs) [84]–[86], fuel cell and lithium-ion battery applications such as dc microgrids [87], [88], and space exploration systems that utilize Hall-effect-propulsion (HEP) [89].

Typically, a conventional two-level boost converter can be used for step-up applications. However, two-level boost converters generally exhibit poor power densities as they rely primarily on inductors for energy transfer, which demonstrate energy densities up to 1000x smaller than those of capacitors [15]. Moreover, for high-voltage dc-dc step-up applications, the two-level boost converter requires a sufficiently large duty cycle to produce a high input-to-output voltage gain. Large duty cycles are undesirable since they impose significant reverse-recovery stress on the output diode, resulting in poor converter performance, low efficiency, and worsened electromagnetic interference (EMI) performance [90]. The implementation of gallium nitride (GaN) devices eliminates the reverse-recovery losses but still produces lower efficiency due to dead-time losses of the GaN devices [91]. Moreover, very high duty ratios also bring difficulty in control, where, for example, digital control requires very high-resolution pulse width modulation (PWM) resolution to achieve effective output voltage regulation. Transformer-based power converter topologies address the shortcomings of the two-level boost by utilizing a transformer to achieve a high dc-dc gain [92]–[94]. Still, the increase in converter performance and efficiency is undermined by the added physical volume of the transformer, resulting in poor power density metrics.

In the LV domain, resonant hybrid switched-capacitor converters (ReSCs) have overcome these shortcomings. Specifically, ReSCs have consistently demonstrated low physical volumes by using a combination of capacitors and inductors for energy storage and transfer. Addi-

tionally, ReSCs have demonstrated the ability to achieve high power-handling capabilities, ultra-high power densities, high efficiencies, and soft-switching abilities [95]–[100]. When implemented with GaN devices, soft-switching ReSCs do not exhibit the previously mentioned dead-time losses since the inductor current is discharged to 0 A before any switches transition from an ON to OFF state.

Conventional two-phase ReSC topologies have two circuit states of operation, each configured with a 50% duty cycle. At higher dc-dc gains, two-phase ReSC topologies, such as the Series-Parallel, Ladder, and Dickson converters, require a large number of active and passive devices [101], [102]. However, using multi-phase control schemes reduces the number of switches and capacitors required for a given dc-dc gain compared to two-phase control. These advanced ReSC topologies with more than two circuit states per switching period are often referred to as "multi-resonant topologies." One such multi-resonant converter is the Cascaded Series-Parallel converter (CaSP), which has been shown to have a much lower output impedance compared to other ReSC and non-ReSC converters [103]. This enables the CaSP converter to have high peak and full-load efficiencies while maintaining a compact physical volume due to its use of flying capacitors for energy storage.

Although much research has been done on further improving the performance of ReSCs, such as the CaSP converter, the work so far has mainly been applied to LV application areas. This work introduces ReSC converters to the high-voltage (HV), high dc-dc gain space by investigating a 1-to-10 CaSP converter. The 1-to-10 CaSP converter comprises a 1-to-5 Series-Parallel switched-capacitor (SC) stage followed by a 1-to-2 SC stage. Due to its multi-phase operation, the CaSP can achieve a 1-to-10 conversion ratio with a lower number of components compared to a standard two-phase SC converter [102], with a single inductor to provide soft-charging [98] operation, as well as soft-switching capabilities. The 1-to-10 step-up dc-dc ratio approximately corresponds to the dc voltage gain needed for a residential PV panel to supply power to an ac grid through a conventional source inverter [104]–[110].

The remainder of this chapter is organized as follows: Section 6.2 details a passive component volume and switching stress analysis that motivates the selection of the CaSP converter over standard, non-multi-resonant ReSC topologies for higher gain applications; Section 6.3 gives an overview of the principles of operation of the 1-to-10 CaSP; Section 6.4 showcases the hardware and experimental validation of the 1-to-10 CaSP, and lastly, Section 6.5 concludes this chapter.

6.2 Cascaded Series-Parallel (CaSP) Passive Component Volume and Switch Stress Analysis

Previous analysis of the CaSP converter has been restricted to comparisons to other types of power converters for distinct conversion ratios and operating frequencies. For example, in [111], the output impedance for an 8-to-1 CaSP is numerically evaluated and compared to the output impedance of other 8-to-1 ReSC converters. In [112], the peak and full-load

efficiencies of the demonstrated hardware for a 6-to-1 CaSP are used to compare to other 6-to-1 ReSC converters. In [103], the authors compare the passive volume and switch stress using the analytical technique presented in [113]. However, it only shows the numerical results for a 6-to-1 CaSP from the analysis and does not provide a more general framework for comparing the CaSP to other power converters for different conversion ratios. Without further investigation, it is not immediately apparent at what distinct fixed conversion ratios the CaSP might be a practical or advantageous converter choice. To enable such comparisons of value both to researchers and practicing engineers, this work provides a general analysis framework that allows the CaSP to be compared to other ReSC converters for any fixed conversion ratio.

Several ReSC analysis and modeling techniques have been presented in recent literature that further motivate ReSC topology choice based on specifications such as switching frequency, power level, and the energy densities of the topological passive components [113]–[118]. Because we wish to analyze a ReSC that operates at resonance and minimize both its volume and power losses, the analytical techniques presented in [113]–[115] are the most applicable to this work. In [115], a fixed box volume for a given converter topology is selected, and the power loss of the converter is minimized by optimizing the ratio between the inductive and capacitive volumes. In [113] and [114], the total passive volume for different topologies is minimized by observing the peak energy stored in both the inductive and capacitive components. Concerning the passive volume analysis while the converter is operating at resonance, using the analysis from either [113] or [114] will yield the same result. In this work, we take the passive volume and switch stress analysis in [113], apply it to the CaSP, and compare the results of the CaSP to the results of [113].

Fig. 6.1 displays generalized N-to-1 step-down ReSC converters that will be compared to one another in the remainder of this section. The passive volume and switch stress analysis for all the shown converters, except the CaSP, is given in [113]. To be consistent with the analysis in [113], the step-down versions of the topologies shown in Fig. 6.1 are analyzed as opposed to a step-up configuration. Nonetheless, the step-down analysis yields the same results for a step-up (i.e., 1-to-N) analysis because the peak energy in each flying capacitor and inductor for each topology stays the same for both step-down and step-up operations.

CaSP Passive Component Normalization

A generalized N-to-1 CaSP with the dc voltage ratings of the switches and flying capacitors annotated is shown in Fig. 6.2. The CaSP comprises a $\frac{N}{2}$-to-1 Series-Parallel converter stage in series with a 2-to-1 doubler converter stage. In the Series-Parallel stage, there are a total of $\frac{N}{2} - 1$ capacitors, all equivalent in capacitance C. Regardless of the output to input dc-dc voltage gain, the CaSP has three sub-period circuit states of operation. These states are depicted in Fig. 6.3a for the generalized N-to-1 CaSP, while Fig. 6.3b illustrates the capacitor and inductor current waveforms for each sub-period. For a generalized N-to-1 CaSP, circuit states 1 and 2 have a sub-period duration of $\frac{T}{N}$ seconds, where T is the length of the switching period, and circuit state 3 has a sub-period duration of $\frac{N-2}{N} \cdot T$ seconds.

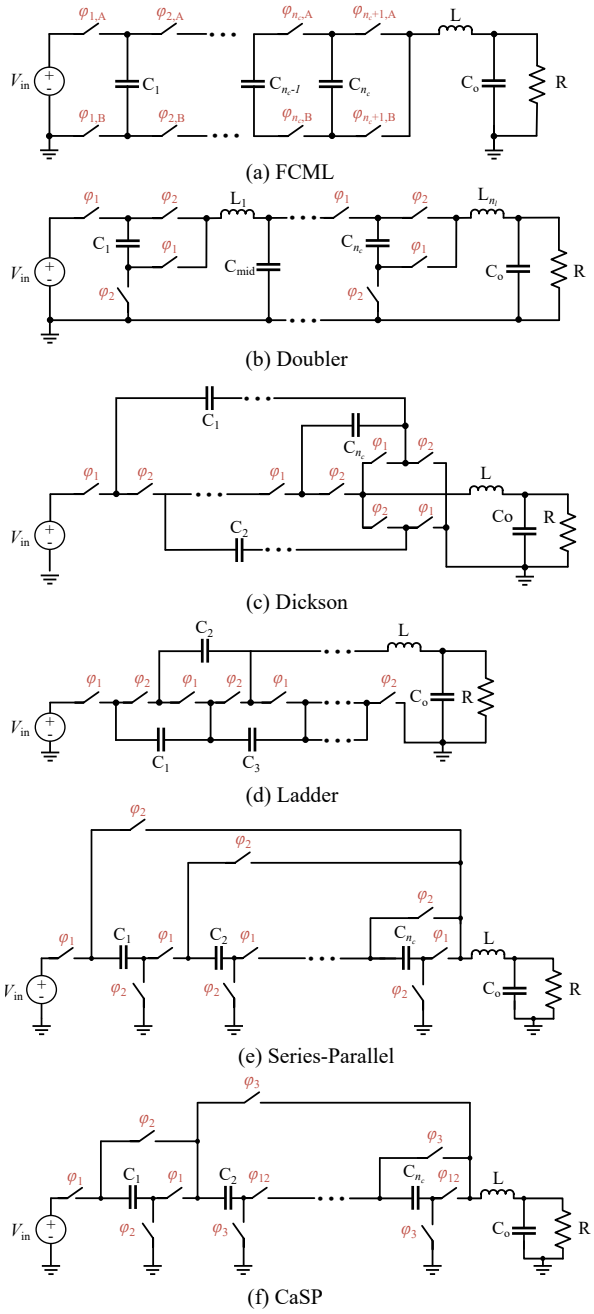


Figure 6.1: Schematic drawings of the various N-to-1 ReSC converter topologies considered for comparison in this analysis. Subscripts n_c and n_l denote the number of capacitors or inductors per topology, respectively, which are unique values per topology to achieve an N-to-1 conversion ratio. The gating signal for each switch is denoted by φ.

Passive Component Minimization Methodology

The total passive volume for any power converter can be determined by the total energy stored by all of the passive elements divided by the component energy density:

$$Vol_{\text{tot}} = \frac{E_{\text{C,tot}}}{\rho_{\text{E,C}}} + \frac{E_{\text{L,tot}}}{\rho_{\text{E,L}}}, \tag{6.1}$$

where $\rho_{\text{E,C}}$ and $\rho_{\text{E,L}}$ are the energy densities for the capacitors and inductors in the topology, respectively. In this analysis, the energy densities of all the passive components in each topology are assumed to be constant (i.e., all capacitors have the same energy density, and all inductors share the same energy density). As explained in [113], the minimized total passive volume can be derived from (6.1) by evaluating four necessary topology-dependent vector quantities, k, α, β, and γ. These vector quantities can be determined by the relationships

$$P_{\text{C},j} = k_j P_{\text{out}}, \tag{6.2}$$

$$V_{\text{C},j} = \alpha_j V_{\text{out}}, \tag{6.3}$$

$$\Delta V_{\text{C},j} = \beta_j \Delta V_{\text{C0}}, \tag{6.4}$$

and

$$P_{\text{L},j} = \gamma_j P_{\text{L0}}, \tag{6.5}$$

where k_j is the ratio of processed power (noted, the total energy absorbed and delivered in a switching period divided by the switching period duration T) by flying capacitor C_j to the converter's output power P_{out}; α_j is the ratio between the average dc voltage of C_j and

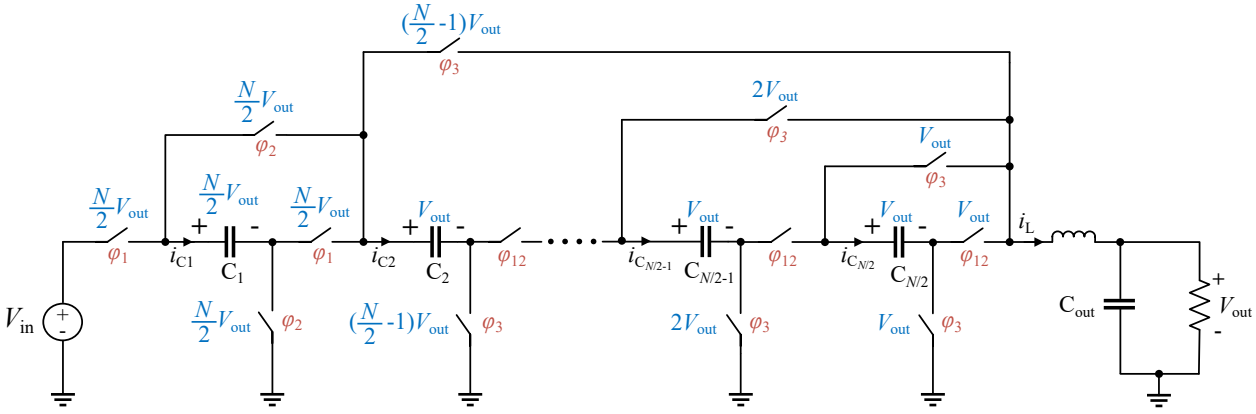


Figure 6.2: A schematic drawing of an N-to-1 CaSP. The dc ratings of the switches, flying capacitors, and the gate signals of the switches are provided.

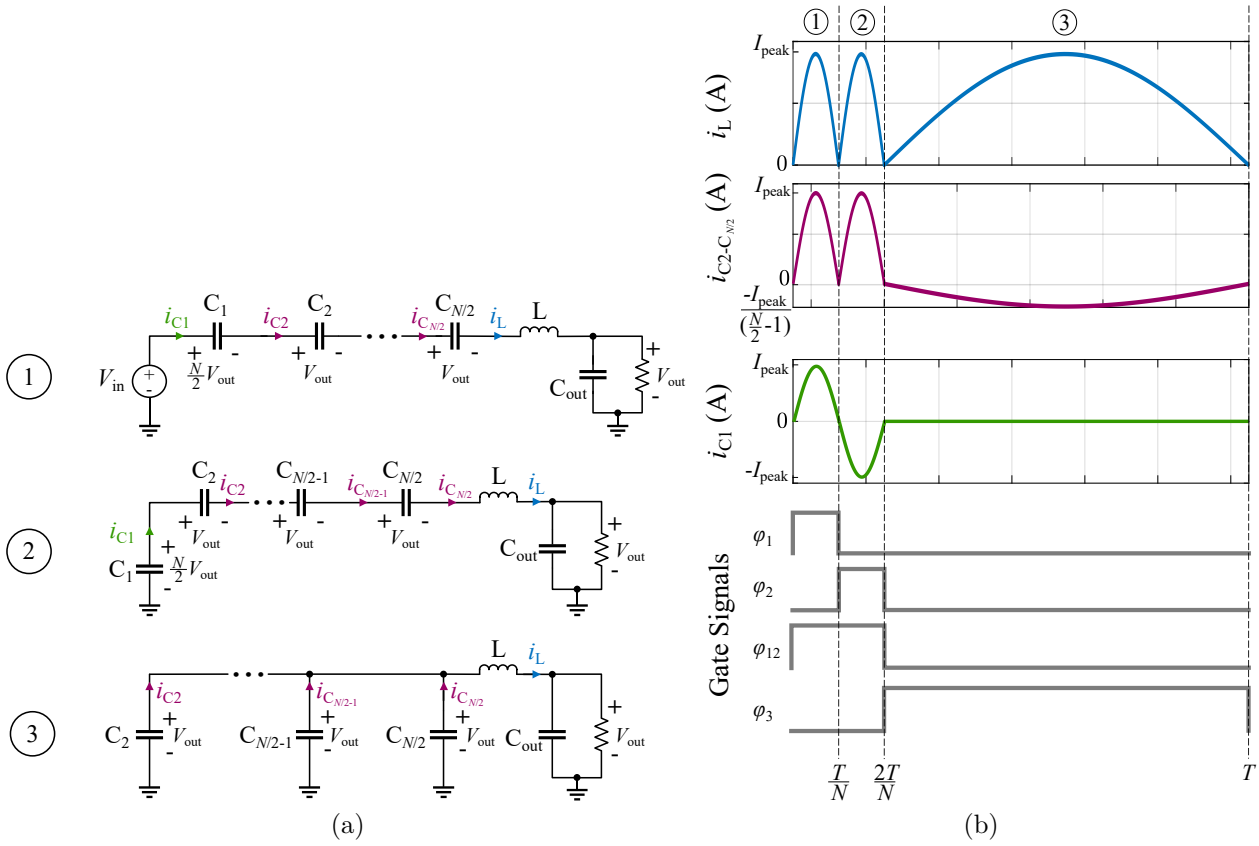


Figure 6.3: The N-to-1 CaSP: (a) The circuit states for each of the three sub-periods of the N-to-1 CaSP. (b) The inductor and flying capacitor current waveforms, along with gate signals for the N-to-1 CaSP during the entire switching period. Note that the average inductor current is equal to I_{out} for each of the three sub-periods, and thus for the entire switching period, leaving $I_{\text{peak}} = \frac{\pi}{2} I_{\text{out}}$.

the converter's output voltage V_{out}; β_j is the ratio of the ac ripple voltage of C_j to the ac ripple voltage V_{C0} of capacitor C_0 in a standard 2-to-1 ReSC converter; and γ_j is the ratio of the maximum reactive power stored in inductor L_j compared to the maximum reactive power stored in inductor L_0 of a 2-to-1 ReSC. Fig. 6.4 illustrates the 2-to-1 ReSC topology with the inductor current i_{L0} shown for an entire switching period.

When the vector quantities k, α, β, and γ are known, they can be substituted into the following expression for the minimized passive component volume:

$$\mathrm{Vol}_{\mathrm{tot,min}} = \frac{P_{\mathrm{out}}}{f_{\mathrm{sw}}\rho_{\mathrm{E,L}}}\left(\frac{\rho_{\mathrm{E,L}}}{\rho_{\mathrm{E,C}}}\left(K_{\mathrm{tot}} + A_{\mathrm{tot}}\frac{1}{r^*} + B_{\mathrm{tot}}r^*\right) + \frac{Y_{\mathrm{tot}}r^*}{16}\right), \tag{6.6}$$

where $K_{\mathrm{tot}} = \frac{1}{2}\sum_{j=1}^{n_c} k_j$, $A_{\mathrm{tot}} = \frac{1}{2}\sum_{j=1}^{n_c}\frac{k_j\alpha_j}{\beta_j}$, $B_{\mathrm{tot}} = \frac{1}{8}\sum_{j=1}^{n_c}\frac{k_j\beta_j}{\alpha_j}$, $Y_{\mathrm{tot}} = \sum_{j=1}^{n_l}\gamma_j$, and r^* is the optimal capacitor ripple ratio that yields the converter's minimized passive volume

$$r^* = \left(\frac{\Delta V_{\mathrm{C0}}}{V_{\mathrm{out}}}\right)^* = \sqrt{\frac{16A_{\mathrm{tot}}\rho_{\mathrm{E,L}}}{16B_{\mathrm{tot}}\rho_{\mathrm{E,L}} + Y_{tot}\rho_{\mathrm{E,C}}}} \quad . \tag{6.7}$$

The quantities n_c and n_l are the number of capacitors and inductors, respectively. To compare the passive volumes between different topologies, the minimized volume in (6.6) is further normalized to $\frac{P_{\mathrm{out}}}{f_{\mathrm{sw}}\rho_{\mathrm{E,L}}}$, and the final normalized passive volume expression that is used to compare the topologies in this analysis is

$$M_{\mathrm{p}} = \left(\frac{\rho_{\mathrm{E,L}}}{\rho_{\mathrm{E,C}}}\left(K_{\mathrm{tot}} + A_{\mathrm{tot}}\frac{1}{r^*} + B_{\mathrm{tot}}r^*\right) + \frac{Y_{\mathrm{tot}}r^*}{16}\right). \tag{6.8}$$

In this work, the N-level topologies shown in Fig. 6.1 are compared via (6.8) for different N-to-1 conversion ratios. For a more detailed description of this passive component volume minimization methodology and how to obtain the vector quantities of this method, the reader is directed to [113].

Deriving α

In each of the three sub-periods, the inductor current i_{L} of the CaSP is sinusoidal and has the same initial and final value of 0 A. Effectively, the dc voltage across L in each of the three sub-periods equals 0 V for resonant operation. By applying a KVL analysis to each of the circuit states in Fig. 6.3a, values for the dc voltages of the flying capacitors can be obtained, yielding the vector expression for α

$$\alpha = [\frac{N}{2} \quad 1 \quad ... \quad 1 \quad 1]. \tag{6.9}$$

The elements of the vector $V_{\mathrm{C}} = \alpha \cdot V_{\mathrm{out}}$ from (6.9) correspond to the dc voltages across the flying capacitors in Fig. 6.2.

Deriving k

As described in [119], the average power processed by a capacitor is

$$P_{\mathrm{C},j} = \frac{1}{2}\overline{|v_{\mathrm{C},j} i_{\mathrm{C},j}|}. \tag{6.10}$$

For ReSC converters, (6.10) can be further simplified to

$$P_{\mathrm{C},j} = \frac{1}{2}\overline{V_{\mathrm{C},j}}\ \overline{I_{\mathrm{C},j}}, \tag{6.11}$$

where $\overline{V_{\mathrm{C},j}}$ and $\overline{I_{\mathrm{C},j}}$ are the dc voltage and averaged charging (or discharging) current, respectively, of the flying capacitors. As discussed in [113], the average charging current, which is equal to the average discharging current to maintain charge balance, is defined as the total charge flowing into a capacitor per switching cycle then divided by half the switching period:

$$\overline{I_{\mathrm{C},j}} = \frac{Q_{\mathrm{C}j,\mathrm{in}}}{\frac{T}{2}} = \frac{Q_{\mathrm{C}j,\mathrm{out}}}{\frac{T}{2}}. \tag{6.12}$$

The average voltage across flying capacitor C_j is element j of the $V_{\mathrm{C},j}$ vector in (6.3), found by the analysis in the previous subsection.

As illustrated in Fig. 6.3b, the average current flowing through inductor L in each sub-period (and the entire switching period) is equal to the output current I_{out} of the converter and the peak value of the inductor current $I_{\mathrm{peak}} = \frac{2}{\pi} I_{\mathrm{out}}$. In sub-periods 1 and 2, capacitors C_2 through $\mathrm{C}_{\frac{N}{2}-1}$ are charged by current i_{L} for a time duration of $\frac{2}{N}T$. In sub-period 1, capacitor C_1 is charged by current i_{L} for a time duration of $\frac{T}{N}$. Therefore, the total amount of charge that flows into each of the flying capacitors is

$$Q_{\mathrm{C}_1,\mathrm{in}} = I_{\mathrm{out}} \cdot \frac{T}{N}, \tag{6.13}$$

and

$$Q_{\mathrm{C}_2,\mathrm{in}} = ... = Q_{\mathrm{C}_{N/2-1},\mathrm{in}} = I_{\mathrm{out}} \cdot \frac{2T}{N}. \tag{6.14}$$

To obtain the average charging current vector $\overline{I_C}$, (6.13) and (6.14) are then divided by $\frac{T}{2}$,

$$\overline{I_C} = \begin{bmatrix} \frac{2}{N} & \frac{4}{N} & ... & \frac{4}{N} & \frac{4}{N} \end{bmatrix} I_{\mathrm{out}}. \tag{6.15}$$

The vectors described in (6.3) and (6.15) can be substituted into (6.11), then divided by output power P_{out} in order to obtain the following result for vector k,

$$k = \begin{bmatrix} \frac{1}{2} & \frac{2}{N} & ... & \frac{2}{N} & \frac{2}{N} \end{bmatrix}. \tag{6.16}$$

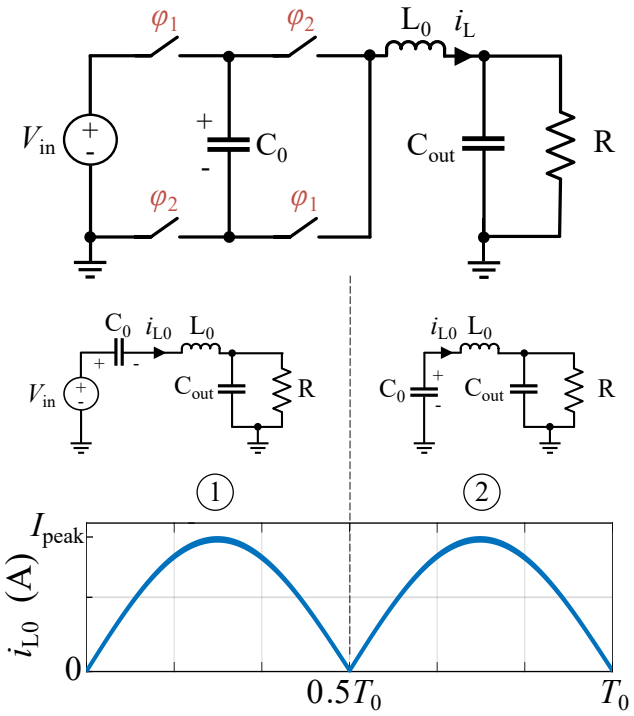


Figure 6.4: A schematic and principle functionality of a 2-to-1 ReSC converter. Inductor L_0 shares the same inductance L_0 as inductor L in the N-to-1 CaSP shown in Fig. 6.2. Similar to the CaSP, the average inductor current is equal to the output current I_{out} and therefore the peak inductor current is $I_{\text{peak}} = \frac{\pi}{2} I_{\text{out}}$. Noted, the switching period duration T_0 is not equal to the switching period T for the CaSP.

Deriving β

Fig. 6.4 shows the schematic of a standard 2-to-1 ReSC. The peak-to-peak voltage ripple across the flying capacitor C_0 in a 2-to-1 ReSC is

$$\Delta V_{C0} = \frac{\pi I_{\text{out}}}{C_0 \omega_{\text{res}}}, \tag{6.17}$$

where I_{out} is the average output current of the converter, C_0 is the capacitance of C_0, and ω_{res} is the resonant frequency of the LC tank in Fig. 6.4, which is $\omega_{\text{res}} = \frac{1}{\sqrt{L_0 C_0}}$. To relate the voltage ripple in (6.17) to the voltage ripple across all of the flying capacitors in the N-to-1 CaSP, the capacitance of the flying capacitors C_2 to $C_{N/2}$ are normalized to the capacitance in the 2-to-1 ReSC converter C_0 (noted, $C_2 = C_3 = \ldots = C_{N/2} = C_0$). Similarly, the inductances in both converters are normalized (noted, $L = L_0$).

To derive β, we examine circuit state 1 of the CaSP for analysis, though any of the three circuit states can be used. The peak-to-peak voltage ripple across each capacitor in the N-to-1 CaSP is

$$\Delta v_{\mathrm{C},j} = \frac{\pi I_{\mathrm{out}}}{C_j \omega_{\mathrm{res},1}}, \tag{6.18}$$

where C_j is the capacitance of capacitor C_j, and $\omega_{\mathrm{res},1}$ is the resonant frequency of the LC tank formed in circuit state 1. The resonant frequency of the LC tank is $\omega_{\mathrm{res},1} = \frac{1}{\sqrt{LC_{\mathrm{eq},1}}}$, where $C_{\mathrm{eq},1}$ is the equivalent capacitance of circuit state 1,

$$\frac{1}{C_{\mathrm{eq},1}} = \frac{1}{C_1} + \frac{1}{C_0} + ... + \frac{1}{C_0}. \tag{6.19}$$

Section 6.3 further explains how to obtain an expression for C_1 in terms of C_0. In a generalized N-to-1 CaSP, the expression for C_1 is $C_1 = \frac{C_0}{3(\frac{N}{2}-1)}$. By substituting this expression for C_1 into (6.19), $C_{\mathrm{eq},1}$ can be simplified to

$$C_{\mathrm{eq},1} = \frac{C_0}{4(\frac{N}{2}-1)}. \tag{6.20}$$

After substituting (6.20) into $\omega_{\mathrm{res},1}$ and (6.19), the peak-to-peak voltage across all capacitors in sub-period 1 is

$$\Delta v_{\mathrm{C1}} = \frac{3}{2}\sqrt{\frac{N}{2}-1}\; V_{\mathrm{C0}}, \tag{6.21}$$

and

$$\Delta v_{\mathrm{C2},...,\mathrm{C}_{N/2}} = \frac{V_{\mathrm{C0}}}{2\sqrt{\frac{N}{2}-1}}. \tag{6.22}$$

The total peak-to-peak voltage across capacitors C_2 through $\mathrm{C}_{N/2}$ over the whole switching period is twice the peak-to-peak ripple in sub-period 1 (6.22) because the capacitors are charged by the same quantity of charge in both sub-period 1 and sub-period 2. This allows us to complete a finalized expression of β:

$$\beta = \left[\frac{3}{2}\sqrt{\frac{N}{2}-1},\;\; \frac{1}{\sqrt{\frac{N}{2}-1}}, ...,\;\; \frac{1}{\sqrt{\frac{N}{2}-1}}\right]. \tag{6.23}$$

Deriving γ

Fig. 6.4 and Fig. 6.3b illustrate the current waveforms for the 2-to-1 ReSC converter and the N-to-1 CaSP, respectively. Both converters have the same average output current I_{out}. The 2-to-1 ReSC inductor L_0 and the N-to-1 CaSP inductor L see the entire output current, and therefore, the energy stored in inductor L_0 is equal to the energy stored in inductor L (i.e., $E_{\mathrm{L}} = E_{\mathrm{L0}}$). However, the switching period duration for each converter is different. Thus, γ can be solved by computing the ratio between the switching period duration for each converter $\gamma = \frac{T_0}{T}$. For the 2-to-1 ReSC converter, the switching period is

$$T_0 = 2\pi\sqrt{L_0 C_0}. \tag{6.24}$$

The switching period duration of the CaSP is the sum of the three sub-period durations, which are a function of the equivalent capacitance. For sub-periods 1 and 2, the sub-period duration is

$$T_1 = T_2 = \pi\sqrt{L\frac{C_0}{4(\frac{N}{2}-1)}}. \tag{6.25}$$

In sub-period 3, the equivalent capacitance changes to $C_{\text{eq},3} = (\frac{N}{2}-1)C_0$, and the sub-period duration is

$$T_3 = \pi\sqrt{L(\frac{N}{2}-1)C_0}. \tag{6.26}$$

Vector γ can then be derived as

$$\gamma = \left[\frac{4\sqrt{\frac{N}{2}-1}}{N}\right]. \tag{6.27}$$

CaSP Switching Stress Normalization

The total switch stress for a converter topology is commonly defined as the summation of the product of the peak dc blocking voltage of each switch, $V_{\text{ds},j}$ and the average current, $I_{\text{ds},j}$ that flows through each switch:

$$\text{Converter switch stress} = \sum_{j=1}^{n_{\text{sw}}} V_{\text{ds},j} I_{\text{ds},j}, \tag{6.28}$$

where n_{sw} is the number of switches in the converter. Both $V_{\text{ds},j}$ and $I_{\text{ds},j}$ can be expressed in terms of the converter output voltage V_{out} and output current I_{out}. We define the normalized switch stress for the converter as follows:

$$M_s = \frac{\text{Converter switch stress}}{V_{\text{out}} I_{\text{out}}} = \sum_{j=1}^{n_{\text{sw}}} \beta_{v,j}\beta_{i,j}, \tag{6.29}$$

where $\beta_{v,j}$ is the ratio between the dc blocking voltage of switch S_j and V_{out} (noted, $\beta_{v,j} = \frac{V_{\text{ds},j}}{V_{\text{out}}}$), and $\beta_{i,j}$ is the ratio between the average current through switch S_j and I_{out} (noted, $\beta_{i,j} = \frac{I_{\text{ds},j}}{I_{\text{out}}}$)[113]. As noted in [120], for converters with a duty cycle that deviates from 0.5, the rms current value as opposed to the averaged amount should be looked at instead to better correlate converter switching stress with loss. However, because most of the ReSC converters being analyzed in this work have a 50% duty ratio, the average current through each switch can be a good approximation for this analysis.

Fig. 6.2 details the dc-blocking voltages in terms of V_{out} for each of the switches in the N-to-1 CaSP, which were solved for after completing the analysis in Section 6.2. The $\beta_{v,j}$ for each switch is the integer multiple of V_{out} that each switch blocks. For example, the switches with the gating signal φ_{12} have the same value $\beta_{v,\varphi_{12}} = 1$, whereas the switches with gating signals φ_1 and φ_2 all have the value $\beta_{v,\varphi_1} = \beta_{v,\varphi_2} = \frac{N}{2}$.

The average current for each switch can be calculated from the current waveforms in Fig. 6.3b, which displays the current flowing through each of the flying capacitors and the inductor and the gating signals for each switch. The average current of the inductor in one switching period and each of the three sub-periods is equal to I_{out}. Due to this, $\beta_{i,j}$ is the gating signal duty ratio for each switch. For example, the switches with the gating signal φ_3 have the same value $\beta_{i,\varphi_3} = \frac{N-2}{N}$, whereas the switches with gating signal φ_{12} have the value $\beta_{i,\varphi_{12}} = \frac{2}{N}$.

Analysis Results

Fig. 6.5 shows the normalized passive volume M_{P} from the analysis for different ReSC converters and a buck converter across different N-to-1 conversion ratios. A lower M_{p} indicates a lower overall passive volume. Fig. 6.6 shows the normalized switch stress M_{s} from (6.29). A lower M_{s} value indicates smaller switching losses. Fig. 6.7 displays normalized passive volume vs. normalized passive switch stress for several ReSC topologies performing either a

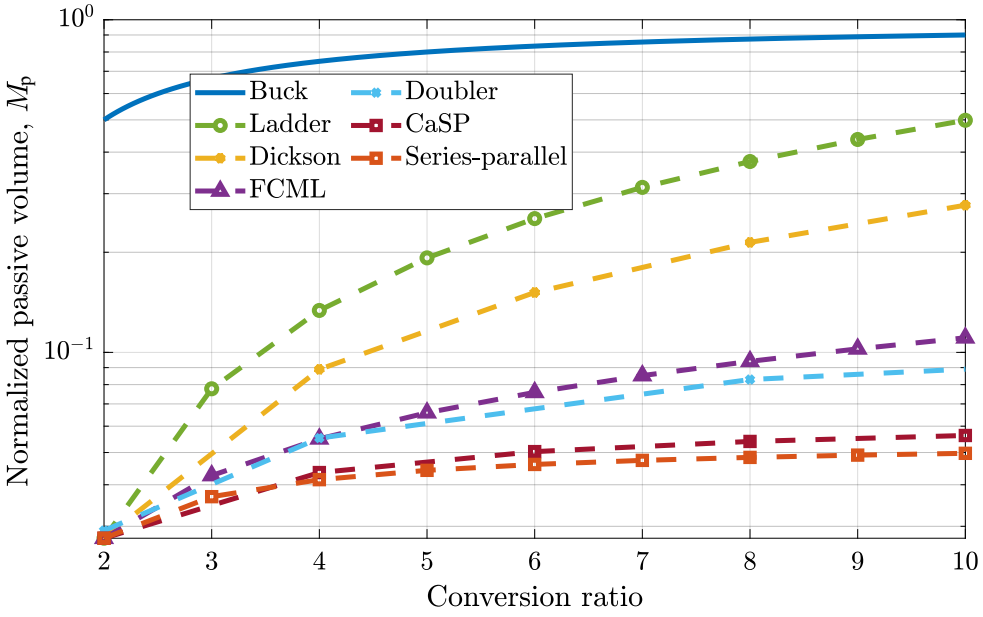


Figure 6.5: Normalized passive volume M_{p} for the buck converter and the ReSC topologies illustrated in Fig. 6.1, from a 2:1 to a 10:1 conversion ratio.

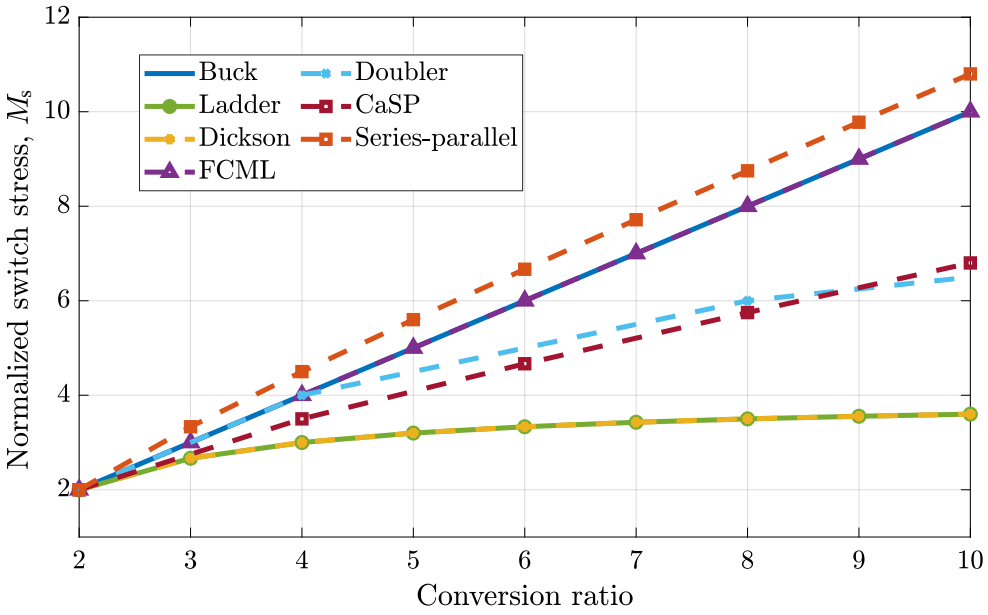


Figure 6.6: Normalized switch stress M_s for the buck converter and the ReSC topologies illustrated in Fig. 6.1, from a 2:1 to a 10:1 conversion ratio.

10-to-1 step-down or 1-to-10 step-up dc-dc ratio. A 1-to-10 step-up ratio was chosen in this work for investigation and, as shown in Section IV, to develop a hardware prototype for a residential PV panel application.

Across all conversion ratios, the CaSP has one of the lowest normalized passive volumes while maintaining relatively low switch stress compared to the other topologies. The Series-Parallel converter outperforms the CaSP for normalized passive volume; however, the CaSP has nearly two times better-normalized switch stress performance. In the 10-to-1 analysis, the 10-to-1 CaSP achieves a fairly similar normalized passive volume as the Series-Parallel converter while achieving more than a 30% reduction in normalized switch stress M_s. While the Dickson and Ladder topologies achieve the lowest normalized switch stress, they have a much larger normalized passive volume. From the analysis, it can be concluded that the 10-to-1 CaSP achieves a relatively low amount of power loss while maintaining a low passive volume for all conversion ratios in comparison to the other ReSC topologies previously analyzed in [113].

6.3 1-to-10 CaSP Principles of Operation

Fig. 6.8 displays the schematic drawing of the 1-to-10 CaSP with $V_{out} = 10 \cdot V_{in}$. The dc-voltage rating and polarity of the switches and the flying capacitors are shown. Fig. 6.9a shows the three different sub-period circuit states of the 1-to-10 CaSP while Fig. 6.9b shows

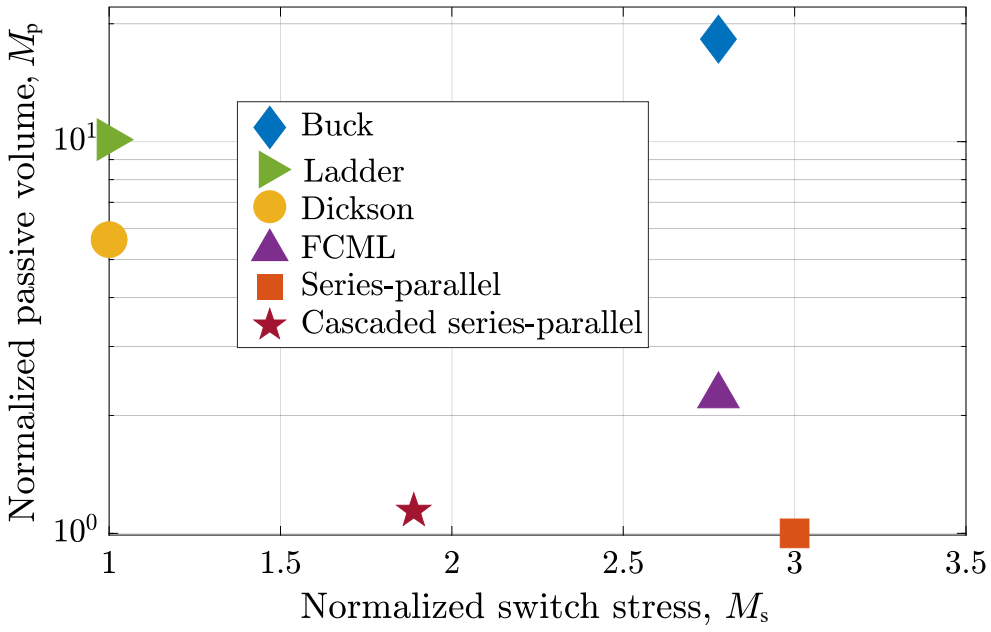


Figure 6.7: Normalized passive volume M_p vs. normalized switch stress M_s for the topologies considered in this analysis for a 10-to-1 (or 1-to-10) conversion ratio.

exemplar current waveforms for the flying capacitors and inductor. The duration of time for each sub-period is equal to the fraction of charge that flows through the LC tank in each sub-period compared to the total charge injected by the input source every switching period Q_{in}. By following the charge flow analysis presented in [116], a quantity $\frac{Q_{in}}{10}$ flows through the LC tank in sub-period 1, quantity $\frac{Q_{in}}{10}$ flows through the LC tank in sub-period 2, and quantity $\frac{8 \cdot Q_{in}}{10}$ flow through the LC tank in sub-period 3. Thus, sub-period 1 is a tenth of the full switching period T, i.e. $T_1 = \frac{T}{10}$, followed by sub-period 2: $T_2 = \frac{T}{10}$, and sub-period 3: $T_3 = \frac{8T}{10}$.

Sub-Period 1

From time $t = 0$ to $\frac{T}{10}$, the load is connected in a direct path to the input voltage source. Capacitors C_1 through C_5 are connected in series with inductor L and are discharged. Capacitors C_1 through C_4 have a dc-voltage equal to V_{in} across each capacitor, while capacitor C_5 has a dc-voltage equal to $5V_{in}$ across it. The equivalent capacitance of the corresponding LC tank can be calculated as

$$C_{eq,1} = \frac{1}{\sum_{j=1}^{5} \frac{1}{C_j}}. \tag{6.30}$$

The capacitance C_1 through C_4 can be set equal to a nominal capacitance C_o. From this,

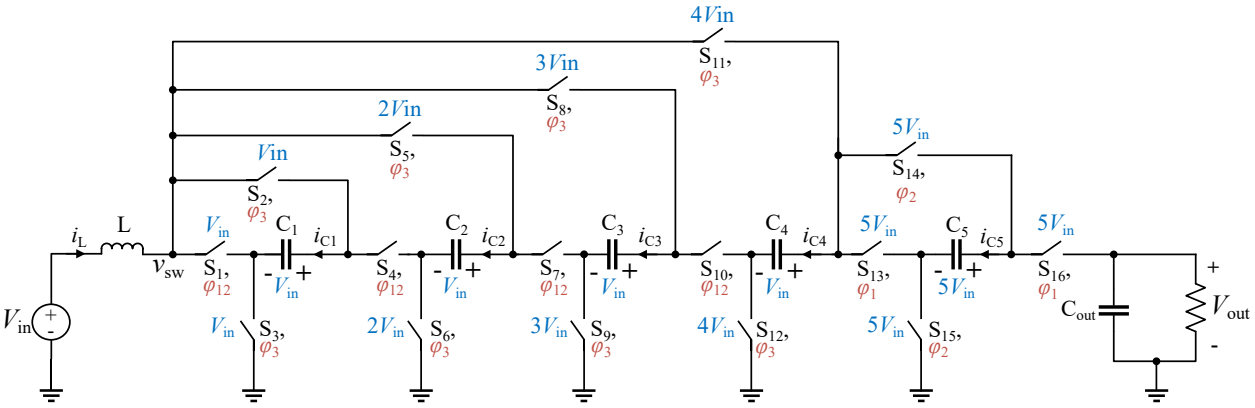


Figure 6.8: Schematic drawing of a 1-to-10 CaSP with switch and capacitor dc voltage ratings provided.

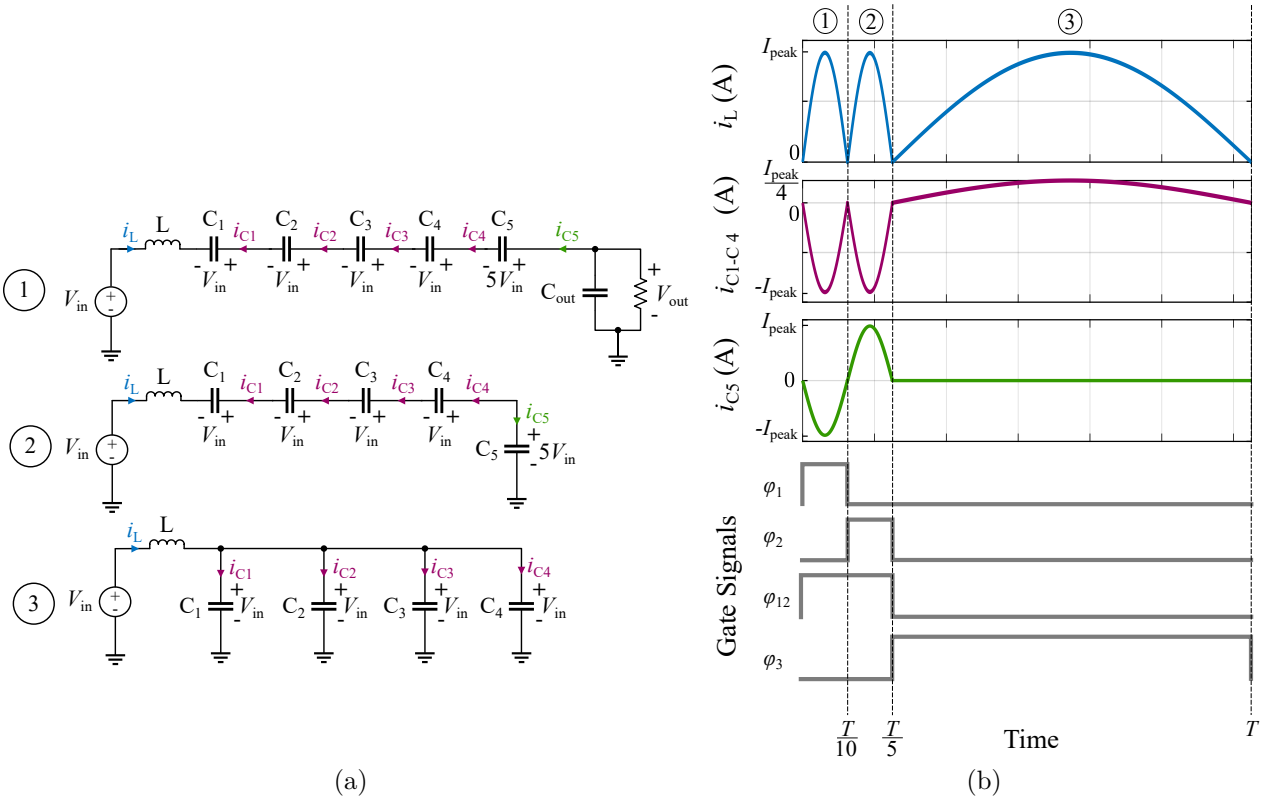


Figure 6.9: The 1-to-10 Cascaded Series-Parallel Converter: (a) The inductor and flying capacitor current waveforms for the 1-to-10 CaSP during the entire switching period. (b) The circuit states for each of the three sub-periods of the 1-to-10 CaSP.

the resonant frequency of sub-period 1 is equal to:

$$\omega_{\text{res},1} = \frac{1}{\sqrt{L\frac{C_\text{o}C_5}{C_\text{o}+4C_5}}}. \tag{6.31}$$

The duration of sub-period 1 is equal to half of the resonant period, i.e., $T_1 = \frac{\pi}{\omega_{\text{res},1}}$. By obtaining expressions for the duration of each sub-period in terms of L, C_o, and C_5, the capacitance C_5 can be calculated in terms of C_o. Specifically, we can relate sub-period duration T_1 and T_3 as $8 \cdot T_1 = T_3$, and an expression for C_5 can be obtained as $C_5 = \frac{C_\text{o}}{12}$.

Sub-Period 2

From time $t = \frac{T}{10}$ to $\frac{2T}{10}$, the load is disconnected from the CaSP and capacitor C_5 is now charging while capacitors C_1 through C_4 remain discharging. Flying capacitors C_1 through C_5 remain connected in series. Thus, the equivalent capacitance and resonant frequency of sub-period 2 can be set equal to the expressions in (6.30) and (6.31), respectively.

Sub-Period 3

From time $t = \frac{2T}{10}$ to T, capacitor C_5 is disconnected, and capacitors C_1 through C_4 are connected in parallel at the switch node and are charged by the input dc voltage source. Because the inductor current i_L has a sinusoidal shape, the average voltage across the inductor in each sub-period is 0 V. Consequently, through KVL analysis, it can be shown that in circuit state 3, capacitors C_1 through C_4 are charged to a dc-voltage equal to the input source voltage V_in.

Due to the change in configuration of the flying capacitors in sub-period 3, new expressions for the sub-period equivalent capacitance $C_{\text{eq},3}$, resonant frequency $\omega_{\text{res},3}$, and duration T_3 must be obtained. Since flying capacitors C_1 through C_4 are now connected in parallel and have the same nominal capacitance C_o, the equivalent capacitance for sub-period 3 is $C_{\text{eq},3} = 4C_\text{o}$, and the resonant frequency and time duration of sub-period 3 are $\omega_{\text{res},3} = \frac{1}{\sqrt{4LC_\text{o}}}$ and $T_3 = \frac{\pi}{\omega_{\text{res},3}}$, respectively.

6.4 Hardware Validation and Experimental Results

Fig. 6.10 shows an annotated photograph of the 1-to-10 CaSP hardware prototype. Fig. 6.11 depicts the active devices, which are all implemented with EPC Gallium nitride (GaN), and the passive components used in the power stage. As shown in Fig. 6.8, the dc voltage rating of each switch varies from V_in to $5 \cdot V_\text{in}$. Therefore, a variety of switches with different voltage ratings may be used to minimize the switching, conduction, and gate drive losses due to the active device circuitry. The $R_{\text{ds,on}}Q_\text{g}$ and $\frac{1}{\sqrt{R_{\text{ds,on}}C_\text{oss}}}$ figures of merit (FOMs) [21], [121] for

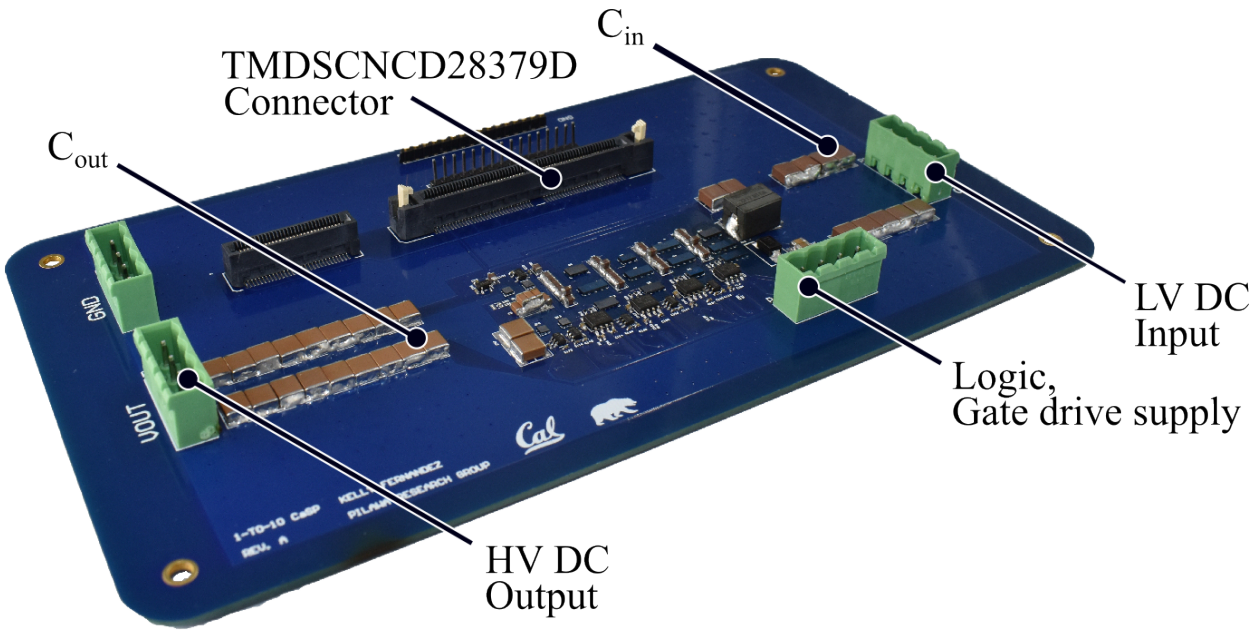


Figure 6.10: The CaSP hardware prototype rated for 300 W and a 35 V-to-350 V step-up ratio. Fig. 6.11 shows a detailed look of the power stage of the hardware, and Table 6.1 explains the detailed parameters for the annotated components.

Table 6.1: Components used in the 1-to-10 CaSP hardware prototype

Component	Device	Parameters
S_1-S_4, S_7, S_{10}	EPC2020	GaN, 60 V, 1.5 mΩ
S_5, S_6	EPC2053	GaN, 100 V, 3.1 mΩ
S_8, S_9	EPC2033	GaN, 150 V, 5 mΩ
S_{11}, S_{12}	EPC2034	GaN, 200 V, 7 mΩ
S_{13}-S_{16}	EPC2050	GaN, 350 V, 55 mΩ
C_1 - C_4	GRM21BR61H106KE43L	9 x 10 μF, 50 V, X5R, 0805
C_5	CGA5L3X7T2E224K160AA	8 x 0.22 μF, 250 V, X7T, 1206
L	PA5187.181HLT	180 nH, 55 A

GaN and Si switching devices were examined for individual blocking voltage categories. The switches with the best FOMs for each blocking voltage category were chosen and are shown in Table 6.1. Along with the passive components used in the hardware prototype (noted, the capacitance values depicted are without derating).

Fig. 6.12 illustrates the gate drive schematic used in the 1-to-10 CaSP hardware prototype. The majority of the switches in the CaSP have a source terminal that is not connected to ground, making power delivery to gate drivers more complicated. For this hardware prototype, the cascaded bootstrap techniques with LDOs method was chosen for power delivery to the gate drivers of the switches [122]. To protect the logic circuitry from any potential

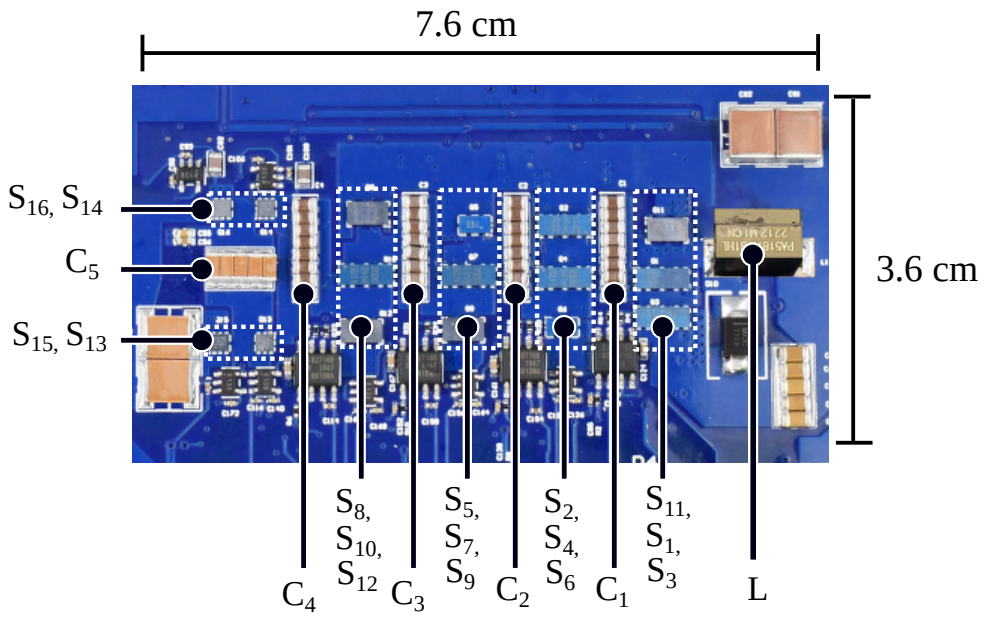


Figure 6.11: Power stage of the hardware prototype with passive storage elements and active devices labeled. Table 6.1 provides the detailed parameters for the annotated components.

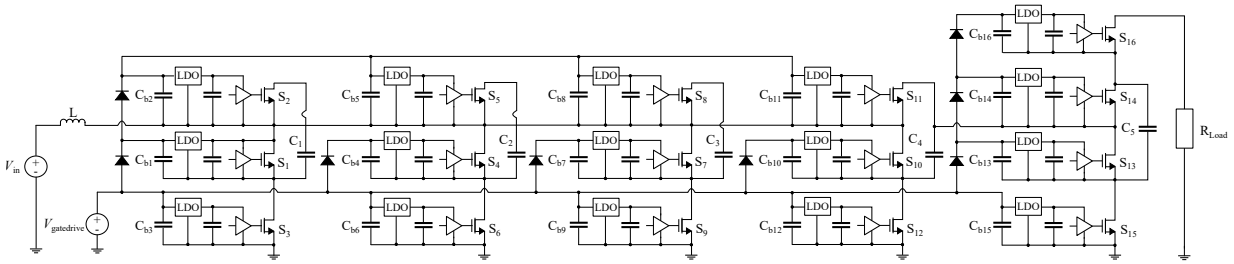


Figure 6.12: Gate drive schematic used for the 1-to-10 CaSP hardware prototype. A cascaded bootstrap methodology is used to deliver power to the switch side of the gate driver.

high voltage surges in the power stage while level shifting the gate control signals, Skyworks Si8271GB-IS isolated gate drivers were used. The same isolated gate drivers were used on the low-side switches to avoid any differences in propagation delay for the gate signals, which have been shown to be a cause of flying capacitor imbalance [35].

In the cascaded bootstrap method, bootstrap capacitors C_b provide power to charge and discharge the gate of each switch. A daisy-chain of diodes connected to $V_{gatedrive}$ allow charge to be delivered to C_b when the switch connected to the negative terminal of C_b is conducting. An example of this is illustrated in Fig. 6.13, where switch S_{15} is conducting, and charge is delivered to $C_{b,13}$ through the path depicted in red. The voltage across a bootstrap capacitor is

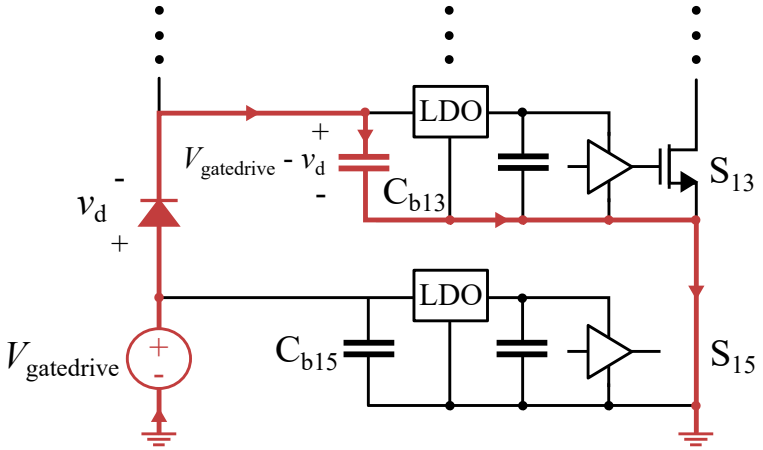


Figure 6.13: An example of the cascaded bootstrap circuit method for the 1-to-10 CaSP hardware prototype.

Table 6.2: Performance specifications of the 1-to-10 CaSP hardware prototype

Parameter	Value
V_{in}	35 V
V_{out}	350 V
P_{out}	300 W
f_{sw}	87 kHz
Peak efficiency	96.1%
Full-load efficiency	95.9%

$$V_{\text{Cb}} = V_{\text{gatedrive}} - n_{\text{d}} \cdot V_{\text{diode}}, \tag{6.32}$$

where V_{diode} is the voltage across the diode (assuming all diodes have the same voltage drop) and n_{d} are the number of diodes in the daisy-chain to which C_{b} is connected to. LDOs are used to maintain an amplitude of 5 V for each v_{gs} signal and keep the on-state resistance for all devices similar. During the hardware testing, a LV Rigol DP832 dc supply was used with a voltage set to $V_{\text{gatedrive}} = 8$ V, which is a sufficient voltage to supply the LDOs at the end of each diode daisy-chain. The efficiency of the gate drive circuit is approximately $100\% \cdot \frac{5\text{ V}}{V_{\text{gatedrive}}} = 62.5\%$.

The 1-to-10 CaSP hardware has been validated up to 300 W with an output voltage of 350 V. Table 6.2 lists the full-power specifications of the system validation test. Figure 6.14 demonstrates the efficiency versus output power for the 1-to-10 CaSP. The CaSP can achieve a peak efficiency of 96.1% and a full-load efficiency of 95.9%. An estimated loss breakdown of the 1-to-10 CaSP operating at its full-load operating point is given in Fig. 6.15. Fig. 6.16

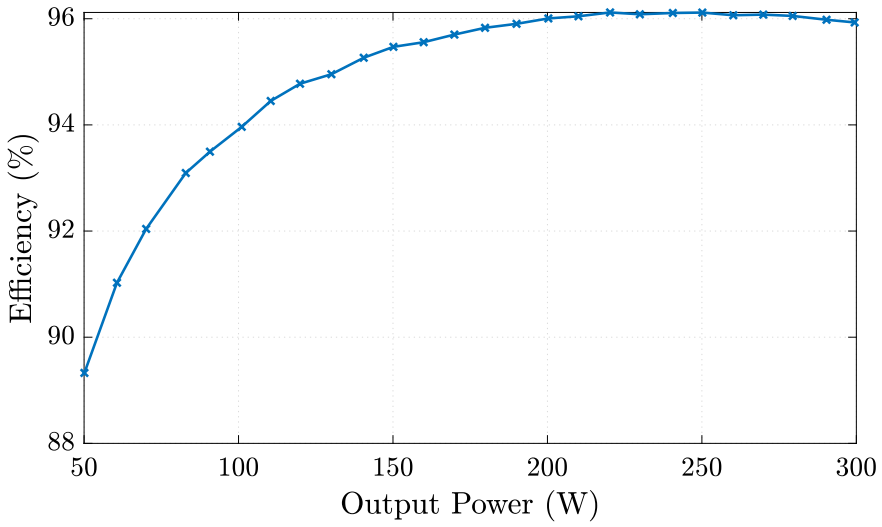


Figure 6.14: Efficiency vs. output power for the CaSP performing a 35-to-350 V step-up.

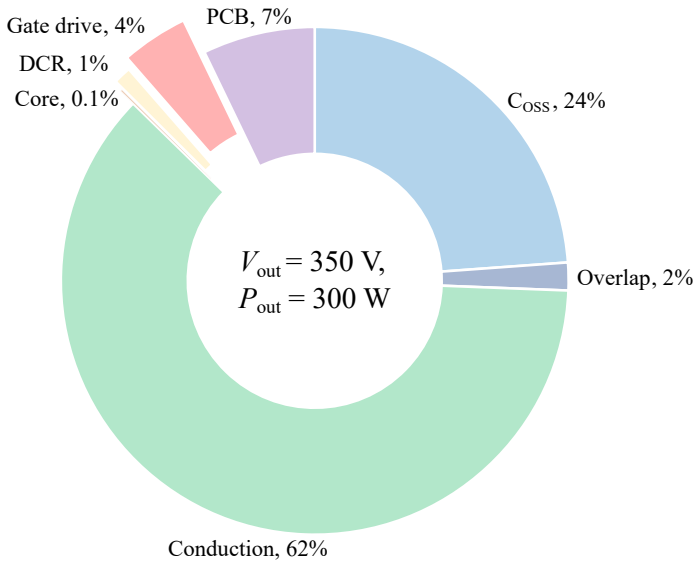


Figure 6.15: Loss breakdown of the 1-to-10 CaSP hardware prototype for a 35-to-350 V step-up operation with 300 W output power.

displays the load regulation of the 1-to-10 CaSP between an output power of 50 to 300 W. At full-load, the output voltage experiences a voltage droop $\Delta\ V_{\text{out}}$ of 8.4 V, corresponding to 2.4% of V_{out}. Lastly, Fig. 6.17 shows oscilloscope captures of the inductor current i_{L} and switch node voltage v_{sw} for $P_{\text{out}} = 300$ W. The inductor current waveforms validate the ability of the converter to achieve ZCS. It can be seen that ZCS is achieved during

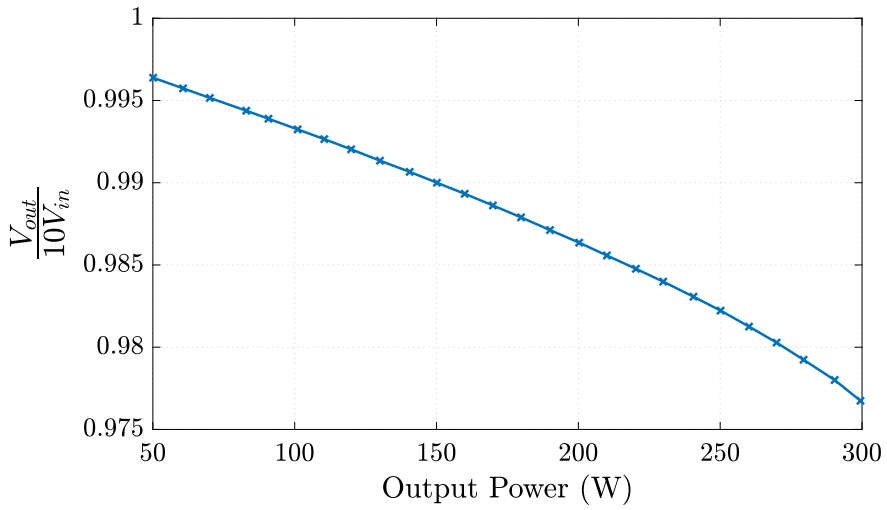


Figure 6.16: Load regulation of the CaSP performing a 35-to-350 V step-up.

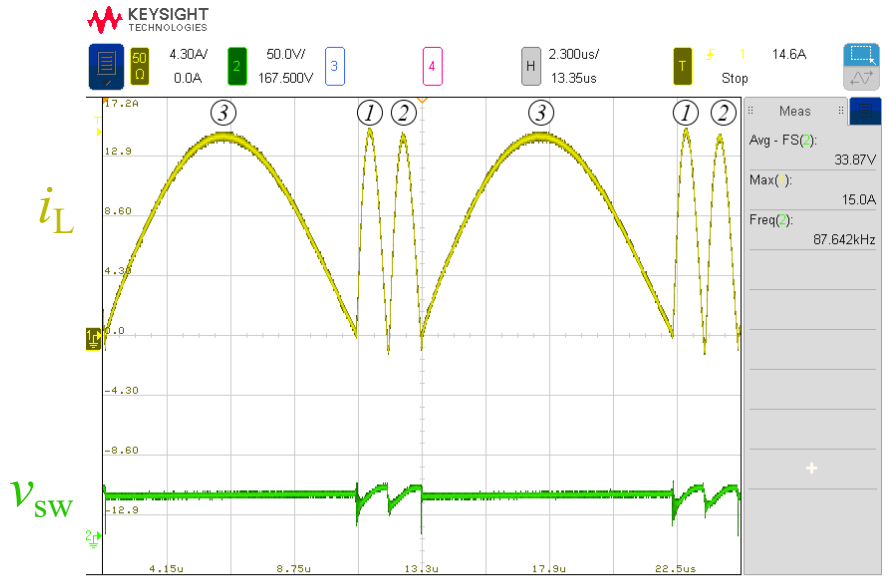


Figure 6.17: Inductor current and switch node waveforms validating the ZCS operation of the 1-to-10 CaSP for a 35-to-350 V step-up at 300 W of output power.

the turn-on and turn-off of stage 3 and the turn-on of stage 2. The 1-to-10 CaSP has the ability to achieve complete ZCS for every turn-on and turn-off transition between each sub-period. However, a trade-off was made in this hardware design between achieving ZCS for all transitions and handling thermal stress on certain devices. By reducing the dead time between the transitions of sub-periods 2 to 1, the converter is able to operate with

ZCS. However, due to the small amount of dead time, shoot-through may occur between complimentary devices and thermally stress the switches. To avoid this, the dead time was increased, resulting in slightly degraded ZCS performance. When prioritizing soft-switching, closed-loop control that adjusts the switching frequency and dead-time, such as in [123] and [124], could be applied to increase performance.

6.5 Conclusion

This chapter presents the operation of a high-voltage 1-to-10 Cascaded Series-Parallel converter. The CaSP converter achieves a relatively low passive component volume and switch stress for high-gain step-up and step-down dc-dc applications. The principle of operation of each sub-switching period is explained with expressions provided for the sub-period duration and resonant frequencies. The theory of operation is validated with a high step-up hardware prototype that can achieve a peak efficiency up to 96.1% and a full load efficiency of 95.9% efficiency.

Chapter 7

A Two-Stage Multi-level Hybrid Switched-Capacitor Microinverter

7.1 Introduction

Residential solar panel installation has become an increasingly widespread solution for consumers to generate and store their electricity to decrease their utility costs and carbon footprint [125]. Once electricity from the solar panel is generated, the power can be stored locally through battery storage or be inverted, transmitted to the grid, and sold to a local utility. Commonly, one microinverter is used per photovoltaic (PV) module to maximize the power output from the solar panel. At the same time, it steps up the low-voltage dc output from the solar panel and inverts the voltage and current waveforms to the required levels for the ac distribution grid [1], [2].

There are two classifications of microinverter topologies: single-stage microinverters and double-stage microinverters. Single-stage microinverters, as depicted in Fig. 7.1, consist of a low voltage (LV) energy buffer, followed by a compounded step-up and step-down stage, and lastly an ac unfolder stage [126], [127]. While the single-stage approach offers the most simplistic solution, the twice-line frequency energy buffer must be placed along the LV dc bus in parallel with the PV module. Because of the severe efficiency decrease of solar panels due to voltage ripple, the PV module requires a large amount of capacitance when tied to the LV dc bus to mitigate any power ripple and to tolerate large rms currents [128]–[130]. The most practical energy buffer solution for the single-stage approach is, therefore, an electrolytic capacitor bank, which suffers from large physical volumes, limited temperature ranges, and short lifetimes [131]–[133]. Moreover, the single-stage approach conventionally utilizes an inductor for energy transfer, further increasing the volume and weight of the converter due to its poor energy density.

The double-stage microinverter, showcased in Fig. 7.2, consists of a step-up converter, followed by a high voltage (HV) dc-link energy buffer stage, and lastly, an inverting stage. The double-stage approach eradicates the LV dc-link energy buffer problem by placing the

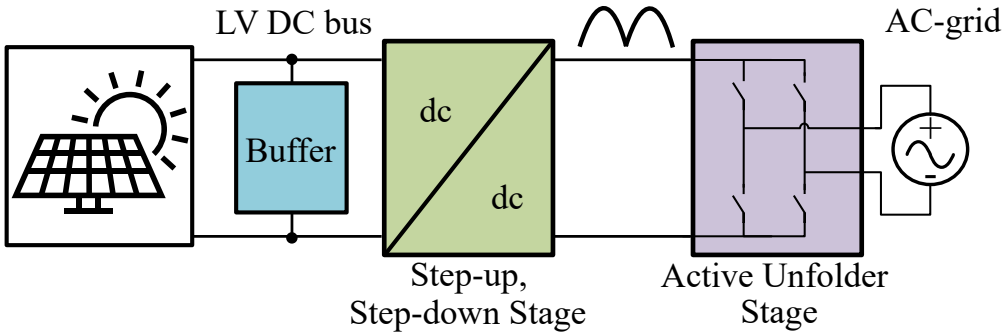


Figure 7.1: Diagram of a single-stage microinverter.

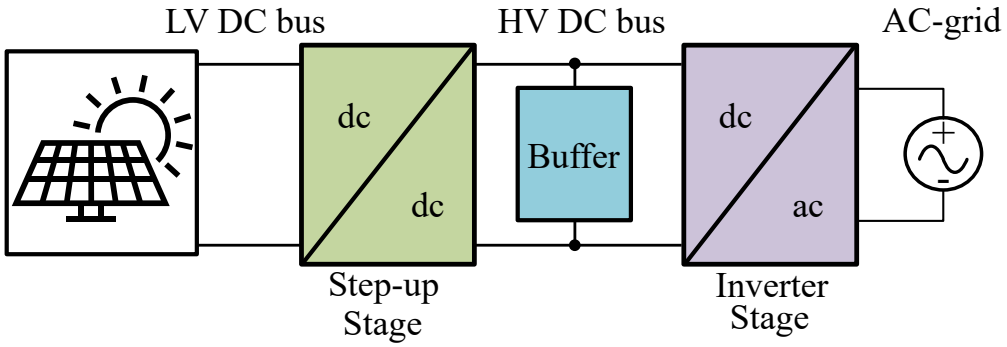


Figure 7.2: Diagram of a double-stage microinverter.

energy buffer on the HV dc bus, significantly decreasing the capacitance requirement. Thus, the energy buffer is more energy-dense as (1) the capacitance and current requirements of the buffer stage are much smaller and (2) HV capacitors, specifically electrolytic capacitors, showcase high levels of physical and gravimetric energy density at high voltage levels (e.g., around 400 V) [14], [15]. This can drastically decrease the microinverter's volume and weight, further reducing manufacturing, packaging, and shipping costs. To showcase the reduction in the volume of the buffer stage between a single-stage and a double-stage solution, Table 7.1 compares the volume between the buffer stage in the Enphase IQ6 microinverter, a single-stage solution, to the volume of a buffer for a double-stage solution. The Enphase IQ6 microinverter has four Nichicon UVZ1H332MHD electrolytic capacitors placed in parallel, totaling a full buffer capacitance of 13.2 mF and full physical volume of 36.1 cm^3. The voltage ripple across the electrolytic capacitor bank is:

$$\Delta v_{\mathrm{dc}} = \frac{P_{\mathrm{in}}}{2\pi f_{\mathrm{2L}} \cdot v_{\mathrm{dc}} \cdot C_{\mathrm{buff}}}, \tag{7.1}$$

where f_{2L} is the rated frequency of the ac power pulsation, v_{dc} is the averaged value of the HV dc bus voltage, and C_{buff} is the buffer capacitance. If the Enphase IQ6 microinverter

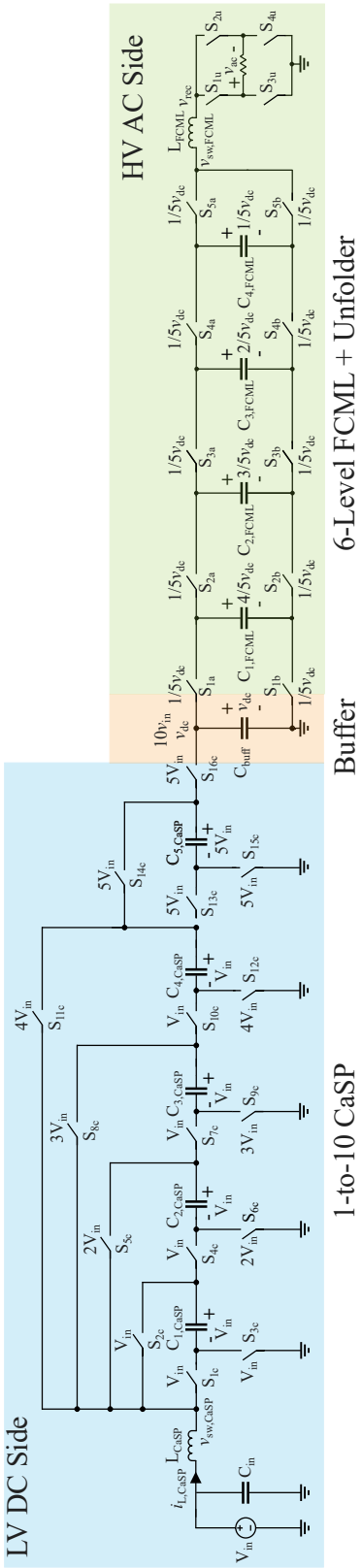


Figure 7.3: Schematic drawing of the proposed system architecture. A 1-to-10 CaSP converter is used to step up the LV dc input to a HV dc bus. A dc-link capacitor buffers the twice-line frequency power pulsation. A 6-level FCML converter with an active unfolder acts as the inverting stage.

operates with a 40 V LV dc bus with a power rating of 400 W, the voltage ripple across the Enphase IQ6 buffer can be approximated to be 1 V peak-to-peak from (7.1). For a double-stage microinverter solution with a 1-to-10 step-up stage, the HV dc bus is rated as 400 V and the HV buffer is allowed to have a 10 V peak-to-peak ripple. From (7.1), the required capacitance for the double-stage buffer is approximately 132.6 μF. An example of a capacitor that can be used for the double-stage solution is a single Nichicon LGW2G151MELZ35 electrolytic capacitor, which has a volume of 13.3 cm^3, approximately a third of the volume in comparison to the single-stage solution.

In addition to the volume reduction of the buffer stage, the two-stage solution uses a more significant amount of active components. As a result, the temperature and power stress of the system components are smaller than in the single-stage solution, which has been shown to sometimes even improve the reliability of the system [133], [134]. However, a drawback to the double-stage architecture topology is that it requires two separate power converter stages, which increase total component count, and, depending on the efficiency of each stage, can yield poorer efficiency metrics than the single-stage solution [8], [126], [133].

Hybrid switched-capacitor converters are becoming increasingly popular solutions for both dc-to-dc conversion and inverting applications as they allow for a significant reduction in passive component volumes by utilizing energy-dense capacitors [15], [135] and increased efficiency via the use of high figure-of-merit [19], [21] LV switches [13], [92], [97], [136], [137]. Resonant hybrid switched-capacitor converters (ReSCs), which are a resonant sub-class of hybrid switched-capacitor converters, further demonstrate extremely low physical volumes through the utilization of a combination of capacitors and inductors for both energy storage and transfer and the ability to achieve high power-handling capabilities, ultra-high power densities, increased efficiencies, and soft-switching [95]–[100].

In this chapter, a novel two-stage architecture is proposed in which a ReSC, the 1-to-10 Cascaded Series-Parallel converter, steps up a $35 - 40$ V photovoltaic (PV) module input to a $350 - 400$ V unregulated intermediate bus. The HV dc bus feeds a flying capacitor multilevel (FCML) inverter stage with a 240 V_{rms} ac output. The proposed microinverter solution, shown in Fig. 7.3, has the potential to be highly power-dense compared to current market solutions as it (1), can utilize HV energy-dense capacitors for the buffer stage, and (2), use several ceramic capacitors, which have up to $1000\times$ high energy densities than inductors, in the step-up and inverting stages. By reducing the volume and weight of the converter, the entire system's manufacturing, packaging, and shipping costs can be decreased. Noted, although the proposed method requires a more significant amount of active components than the conventional microinverter [7], the price and size of semiconductor devices have shown to only reduce over time and precisely when bought in large quantities for large-scale manufacturing [138]–[140].

The CaSP has previously demonstrated capabilities of high efficiency and low physical profiles [141]. However, ensuring its ability as the step-up stage, specifically its ability to handle the dynamics of the voltage and current ripples imposed by the grid-frequency inverting stage to an inverting stage, remains a critical step in validating its potential for adoption in microinverter applications. The FCML has previously demonstrated competitive

Table 7.1: Volume difference in the buffer stage between a single-stage and a double-stage microinverter solution

Parameter	Single-stage	Double-stage
Manufacturer	Nichicon	Nichicon
Part number	UVZ1H332MHD	LGW2G151MELZ35
Capacitance	4×3300 μF	150 μF
Volume	36.1 cm^3	13.3 cm^3
Volumetric energy density	456.6 $\mu J/mm^3$	901.9 $\mu J/mm^3$

efficiencies and low volumes in inverting applications [19], [28], [34], [80], [136]. In this two-stage conversion scheme, the FCML produces a rectified sine-wave output of the correct magnitude, which is then converted to a full-wave ac waveform through an active unfolded. Combined, the two stages form a fully hybrid switched-capacitor converter architecture, using multi-level topologies from input to output.

The rest of this chapter is organized as follows: Section 7.2 describes the operation of the combined 1-to-10 step-up CaSP stage, the HV energy buffer, and the FCML stage; Section 7.3 showcases the hardware and results of the proposed microinverter topology; lastly Section 7.4 concludes this chapter.

7.2 System Architecture

Fig. 7.3 illustrates the system architecture with the dc blocking voltages of switches and dc voltage ratings of capacitors provided. The system comprises two converter stages: a 1-to-10 CaSP stage that steps up the dc input voltage and a 6-level FCML with an active unfolder stage. In between the two stages, a buffer capacitor stores and releases power pulsated at the twice-line frequency. Exemplary waveforms of the system input dc voltage V_{in}, the CaSP inductor current $i_{\text{L,CaSP}}$, the HV dc bus voltage v_{dc}, the FCML switch-node voltage $v_{\text{sw,FCML}}$, and ac output v_{ac} for one line cycle during a 40 V_{dc} to a 240 V_{ac} conversion rated at 400 W are shown in Fig. 7.4.

CaSP Step-up Stage

For a given switching period, the CaSP converter undergoes three separate sub-period intervals, each with its own unique LC tank [103]. In [141], the time duration, equivalent impedance, and resonant frequency are derived for each sub-period interval. When operating at resonance, all of the switches in the CaSP are capable of zero current switching (ZCS), and a fraction of switches are capable of zero voltage switching (ZVS) for any step-up or step-down ratio. Noted when operating above resonance, ZCS is foregone to decrease con-

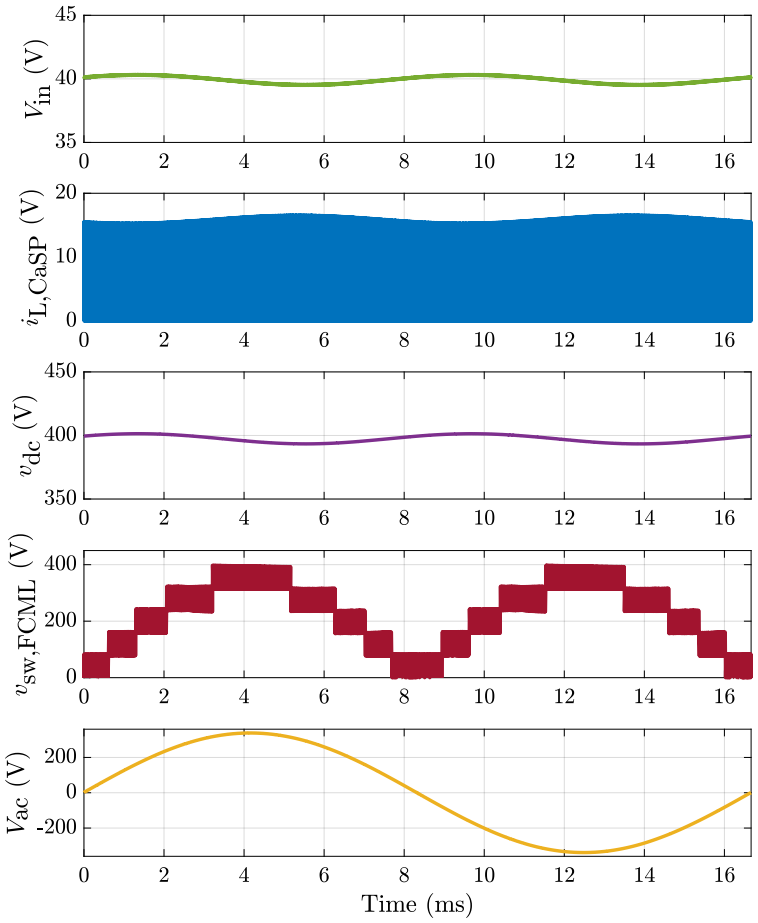


Figure 7.4: Exemplary waveforms of the low voltage dc bus V_{in} (which is internally modeled with some source impedance), the CaSP inductor current $i_{L,CaSP}$, the high voltage dc bus v_{dc}, the FCML switched-node voltage $v_{sw,FCML}$, and the ac output voltage v_{ac} during a 40 V to 240 V_{ac} conversion rated at 400 W.

duction losses; however, a fraction of the switches will still experience ZVS. Fig. 7.5 shows the three sub-period circuit states and the inductor current for a 1-to-10 step-up operation. As discussed in [141], the resonant frequency for each sub-period is:

$$\omega_{res,1} = \omega_{res,2} = \frac{1}{\sqrt{L_{CaSP}\frac{C_o C_{5,CaSP}}{C_o+4C_{5,CaSP}}}}, \text{ and} \tag{7.2}$$

$$\omega_{res,3} = \frac{1}{\sqrt{4L_{CaSP}C_o}}, \tag{7.3}$$

where $C_{5,CaSP} = \frac{C_o}{12}$ and C_o is the capacitance for capacitors $C_{1,CaSP}$ through $C_{4,CaSP}$. From (7.2) and (7.3), the time duration for each interval T_j can be derived as $T_j = \frac{\pi}{\omega_{res,j}}$.

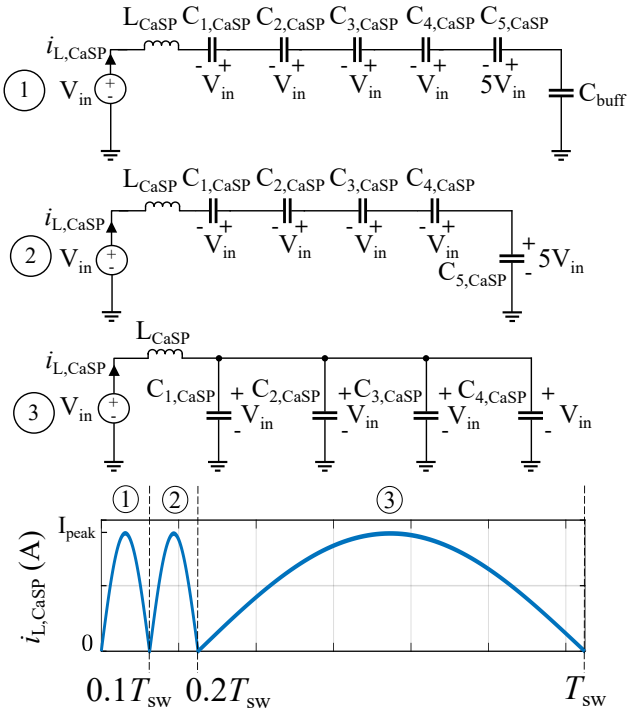


Figure 7.5: The three sub-period circuit states of the CaSP stage. Inductor current $i_{L,CaSP}$ is shown for each sub-period for a given switching period T_{sw}.

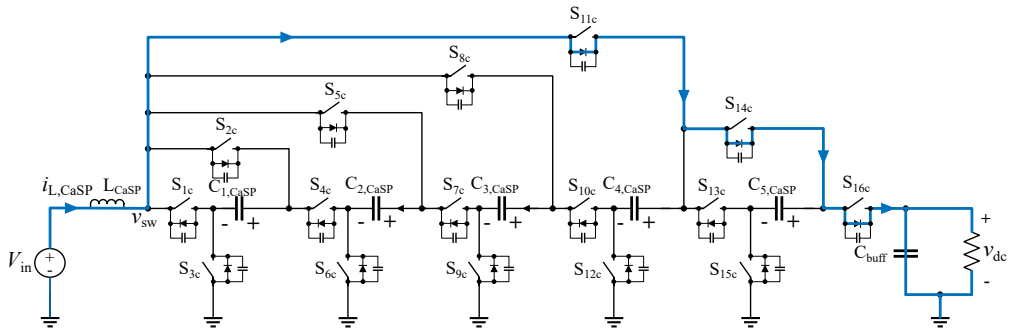


Figure 7.6: Direction of current flow when the $i_{L,CaSP}$ is not fully discharged to 0 A and the converter experiences a switching transition. The output capacitance in some switches will discharge, allowing some switches to reverse conduct and connect the switched-node to the HV dc bus v_{dc}.

As shown in Fig. 7.5, the current flowing through the conducting switches in sub-periods 1 and 2 is equal to inductor current $i_{L,CaSP}$. In sub-period 3, the current flowing through the switches that are ON is equal to one-fourth of $i_{L,CaSP}$. In each sub-period, the current $i_{L,CaSP}$ has the same averaged value and the same peak current value of the inductor L_{CaSP}, which

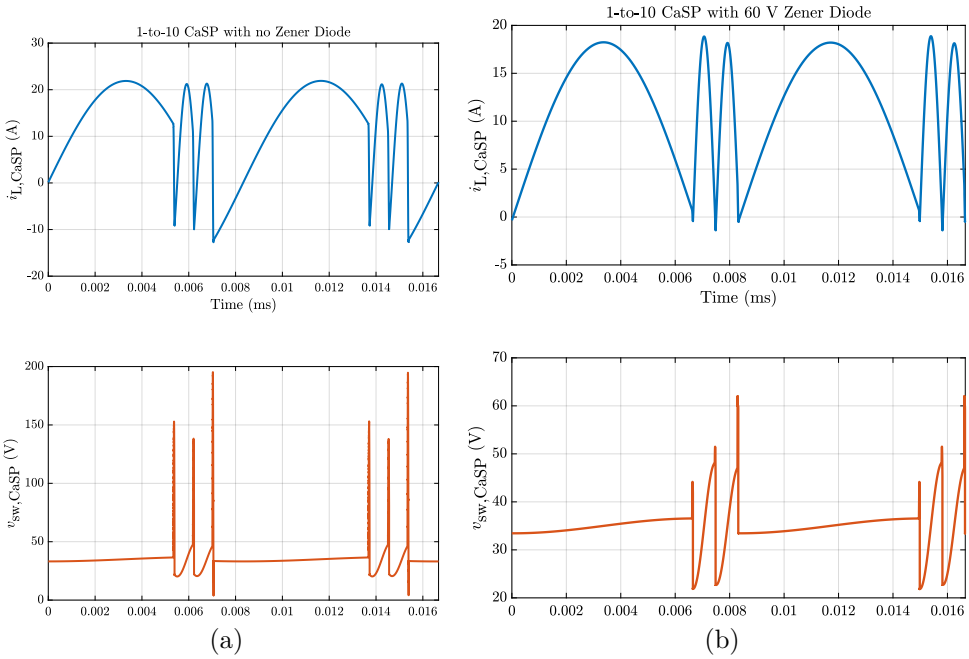


Figure 7.7: Exemplary waveforms of the inductor current $i_{\mathrm{L,CaSP}}$ and switched-node voltage $v_{\mathrm{sw,CaSP}}$ without and with a clamping circuit on the switched-node of the CaSP: (a) when there is no clamping mechanism in the CaSP circuit. The voltage transient along the switched-node can cause the voltage across some of the switches in the CaSP to exceed their blocking voltage, potentially causing catastrophic damage to the microinverter system. (b) When a 60 V Zener diode is placed along the switched-node in the CaSP circuit as a clamping mechanism. The voltage across the switched-node is clamped to prevent any switches in the circuit from experiencing an over-voltage condition.

can be derived based on the input power and voltage $I_{\mathrm{peak}} = \frac{\pi}{2} \cdot \frac{P_{\mathrm{in}}}{V_{\mathrm{in}}}$. At high power, the peak-to-peak value of the resonant current $i_{\mathrm{L,CaSP}}$ becomes quite substantial, requiring the input and output ports to have sufficient filter capacitance to moderate the current ripple at the switching frequency f_{sw}.

It is possible for the inductor current in the CaSP $i_{\mathrm{L,CaSP}}$ not to be fully discharged when a switching transition occurs in the CaSP. This possibility becomes more probable when no closed-loop control monitors the inductor current. If the inductor current $i_{\mathrm{L,CaSP}}$ is not fully discharged, the output capacitance in some of the switches will discharge to allow the internal body diodes in the switches to conduct, creating a path for $i_{\mathrm{L,CaSP}}$ to flow (shown in Fig. 7.6). As a result, the switched-node of the CaSP, $v_{\mathrm{sw,CaSP}}$, will become directly connected to the HV dc bus and experience a HV transient. This transient can cause the voltage across the switches in the CaSP to exceed their nominal dc blocking voltage rating (the dc rating for all switches is shown in Fig. 7.3), causing catastrophic damage to the

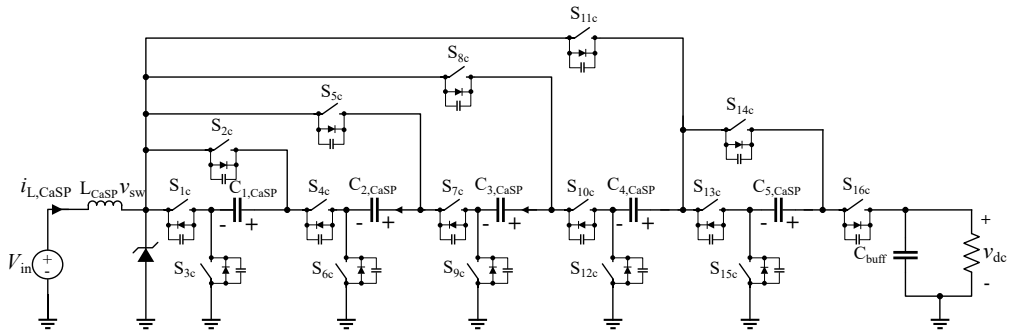


Figure 7.8: Circuit of the 1-to-10 CaSP with a Zener diode placed across the switched-node to prevent high voltage transients during switching transitions.

microinverter system and potentially the PV panel. Fig. 7.7a shows the inductor current and switched-node voltage during this hazardous condition. To protect the system from this harmful event, a Zener diode is placed on the switched-node of the CaSP to act as a clamping circuit. The Zener diode provides a path for current to flow when $i_{\mathrm{L,CaSP}}$ is not fully discharged during any dead-time duration and clamps the voltage on the switched-node to a safe value that doesn't exceed the dc voltage rating of the switches. Fig. 7.7b displays the inductor current and switched-node voltage waveforms when a 60 V Zener diode is placed across the switched-node. Fig. 7.8 shows the location of the Zener diode in the CaSP circuit.

Buffer Stage

The buffering stage for the step-up inverter system is placed on the HV dc bus between the output port of the CaSP stage and the input port of the FCML inverting stage. The buffer must store and release the twice-line frequency ($f_{2\mathrm{L}}$) pulsation due to the single-phase system architecture [54]. The required minimum capacitance value can be found by

$$C_{\mathrm{buff}} = \frac{P_{\mathrm{in}}}{2\pi f_{2\mathrm{L}} \cdot v_{\mathrm{dc}} \cdot \Delta v_{\mathrm{dc}}}, \tag{7.4}$$

where $f_{2\mathrm{L}}$ is the rated frequency of the ac power pulsation, v_{dc} is the averaged value of the HV dc bus voltage, and Δv_{dc} is the user's desired voltage ripple along the HV dc bus. As shown in (7.4), by placing the buffer capacitance across a bus with a higher dc voltage rating, the capacitance can be reduced due to the increase in the dc voltage and in the allowable ac ripple across the buffer capacitor v_{dc} and Δv_{dc}, respectively. Therefore, placing the buffer capacitance at the HV bus decreases the required buffer capacitance requirement, enabling the use of capacitors with higher lifetimes and lower physical volumes.

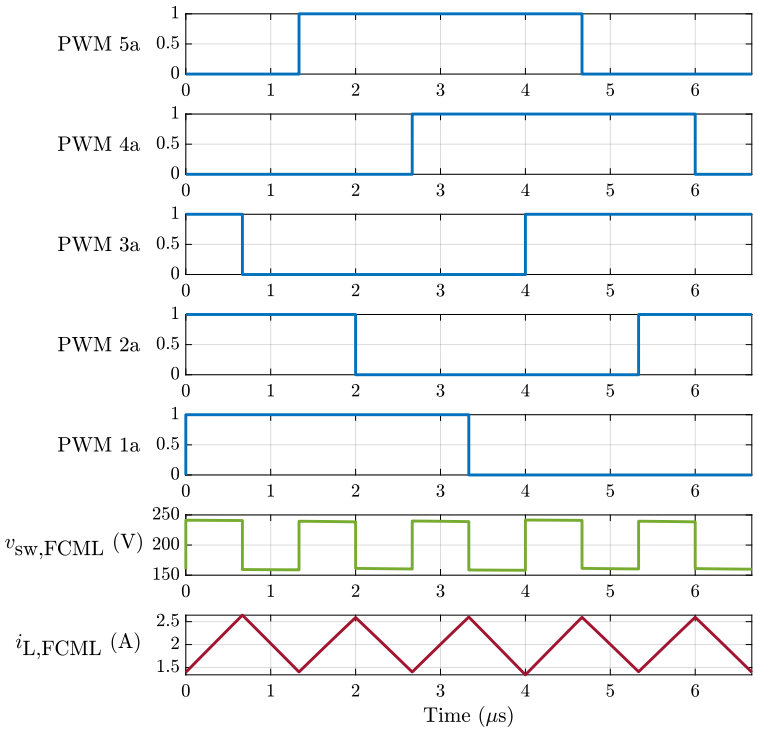


Figure 7.9: The inductor current i_L and switched-node voltage v_{sw} during one switching period for a 6-level FCML shown in the microinverter system topology in Fig. 7.3. The input voltage, output power, switching frequency, and duty cycle of the topology are $V_{dc} = 400$ V, $P_{out} = 400$ W, $f_{sw} = 150$ kHz, and $d = 0.5$, respectively.

The Flying-Capacitor Multi-level Converter

A Flying Capacitor Multi-level Converter (FCML) was chosen as the inverting stage in the proposed two-level microinverter system. A 6-level design was selected to invert a HV dc input between 350 V_{dc} to 400 V_{dc}, to a 240 V_{ac} single-phase output. An even level count was chosen based on the natural charge balancing between the flying capacitors in the FCML [35]. Moreover, a 6-level count offers an optimal balance in trade-offs between the power loss in the system, the physical volume, and the passive component mass [37], [41], [46].

A generalized N-level FCML consists of $N-1$ switch pairs, $N-2$ flying capacitors, and N dc voltages that the output can be connected to (noted, the dc input, the dc voltage across the $N-2$ flying capacitors and ground). In steady-state operation, the voltage across each capacitor is given by $v_{c,k} = v_{dc}\frac{k}{N-1}$, where $k = 1, \ldots N-2$, and each switch must block a dc voltage value of $\frac{v_{dc}}{N-1}$. For the proposed system, phase-shifted pulse width modulation (PSPWM) is used to control the switching operation of each FCML switching pair [17]. For a 6-level FCML, each PWM is phase-shifted by $\frac{360^\circ}{N} = 72^\circ$ [18], [38], [39]. As shown in Fig. 7.9, the PSPWM control scheme causes a frequency multiplication effect at the switched-node

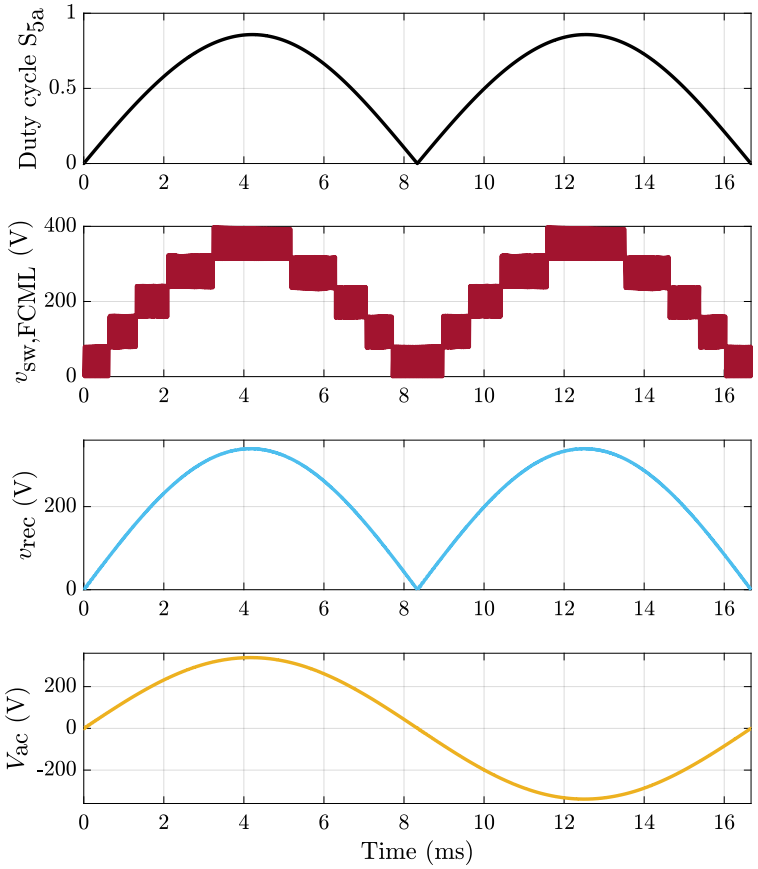


Figure 7.10: Exemplary waveforms of the duty cycle for switch S_{5a} (placement shown in Fig. 7.3), the FCML switched-node voltage $v_{sw,FCML}$, the voltage output of the low pass filter in the FCML v_{rec}, and the ac output voltage v_{ac}.

of FCML. For a 6-level FCML, the frequency at the switched-node is $(N-1) \cdot f_{sw} = 5 \cdot f_{sw}$, resulting in $(N-1)^2\times = 25\times$ reduction in the inductor filter, enabling a higher control bandwidth at this node, which is advantageous for fast inductor current control of the 60 Hz output. In an inverting operation, the duty cycle for each switching pair is in the shape of a rectified sinusoid, causing the voltage at the switched-node $v_{sw,FCML}$ to resemble a sine wave with a lower amount of harmonic components. The $v_{sw,FCML}$ waveform is then filtered by the FCML output inductor and capacitor L_{FCML} and C_{ac}, respectively, producing a rectified ac voltage v_{rec} that is then unfolded by the active unfolder stage as the ac output. Fig. 7.10 displays the duty cycle for the FCML switch S_{5a} alongside the FCML switched-node voltage $v_{sw,FCML}$ and the output ac voltage v_{ac} over one line cycle.

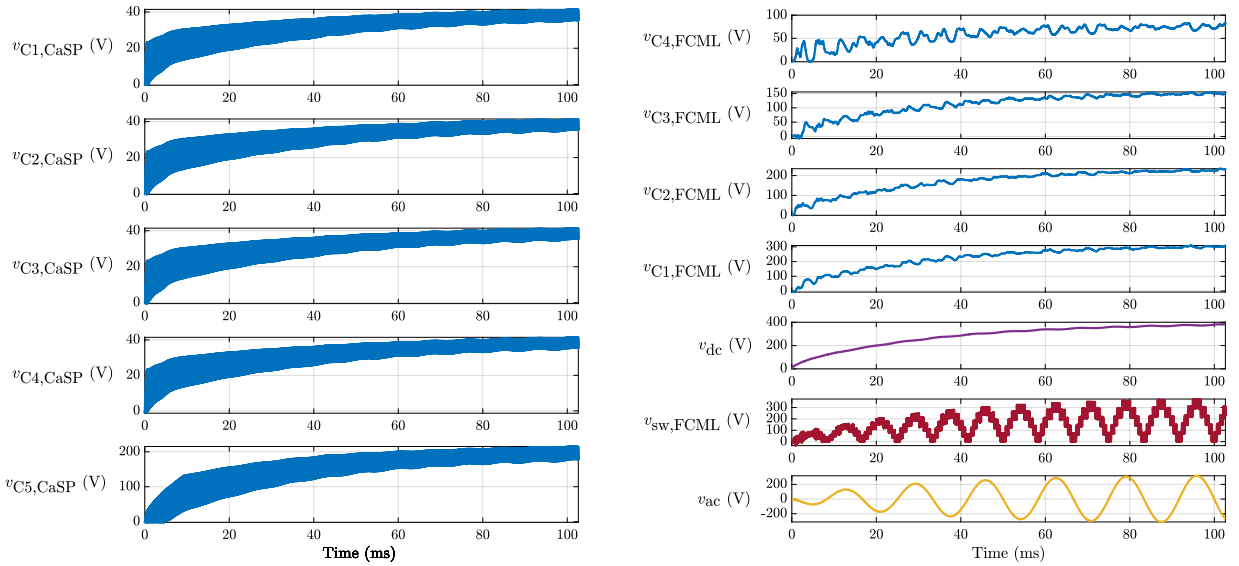


Figure 7.11: Exemplary voltage waveforms of the capacitors $C_{1,CaSP}$ through $C_{5,CaSP}$ in the CaSP stage, $C_{1,FCML}$ through $C_{4,FCML}$ in the FCML stage, the voltage across the HV energy buffer v_{dc}, the FCML switched-node voltage $v_{sw,FCML}$, and the ac output v_{ac}, during a system hard start-up from $V_{in} = 0$ V to 40 V at a rated power of $P_{in} = 400$ W.

System Start-up

The CaSP stage eliminates the need for any additional start-up circuity in either stage when an input voltage is instantaneously connected to the LV dc input port by inherently controlling the start-up behavior of the full system. As showcased in the system diagram in Fig. 7.3, the switches in the CaSP are rated to block a minimum dc voltage of V_{in}. Therefore, when a LV dc input is connected to the LV dc port of the system when all passive components in the system are not energized, the charge flow in each sub-period duration causes the dc voltages of the flying capacitors of the step-up and inverting stages to gradually increase over time without any detrimental voltage overshoot. Fig. 7.11 demonstrates a hard start-up event for $V_{in} = 40$ V and $P_{in} = 400$ W. With time, the capacitors in the microinverter system ramp to the desired dc voltage value until the output of the CaSP stage reaches an approximate value of $10 \cdot V_{in}$ and the system output is $v_{ac} = 240$ V_{ac}.

7.3 Hardware Implementation and Experimental Results

The step-up inverter system comprises two developmental board prototypes connected in series. The CaSP and FCML stages utilize only GaN components as active components, enabling further system savings in power loss. Table 7.2 lists the active and passive com-

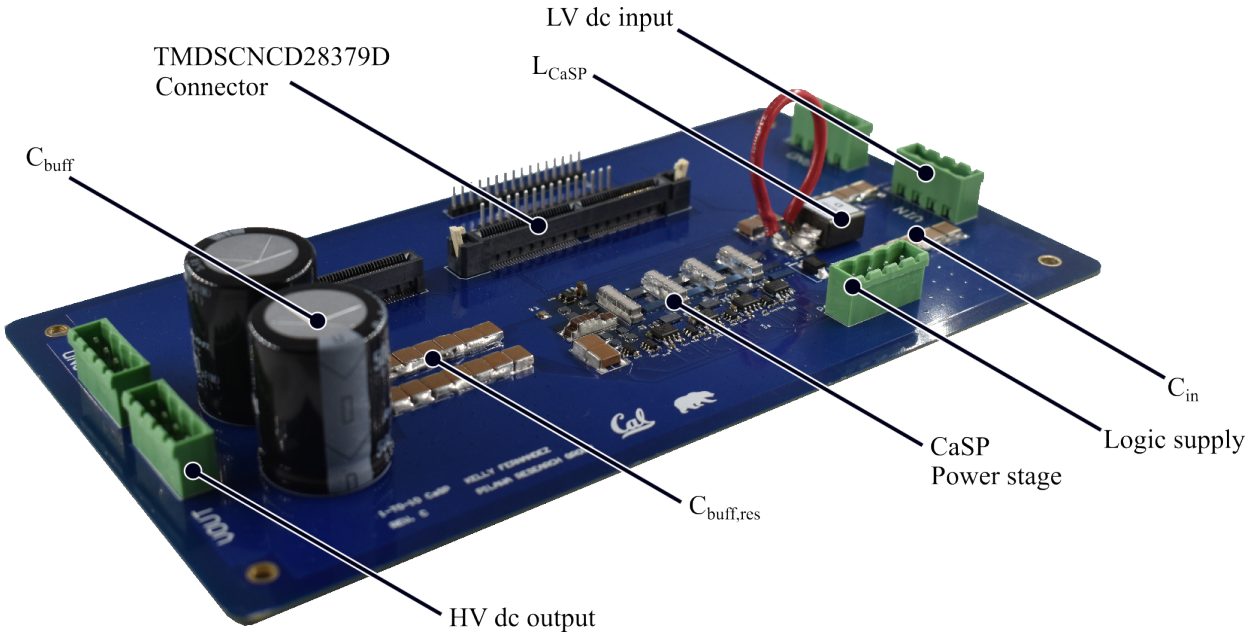


Figure 7.12: Developmental prototype of 1-to-10 CaSP stage for the proposed step-up inverter. Table 7.2 lists the part numbers and parameters of the major components of the full system.

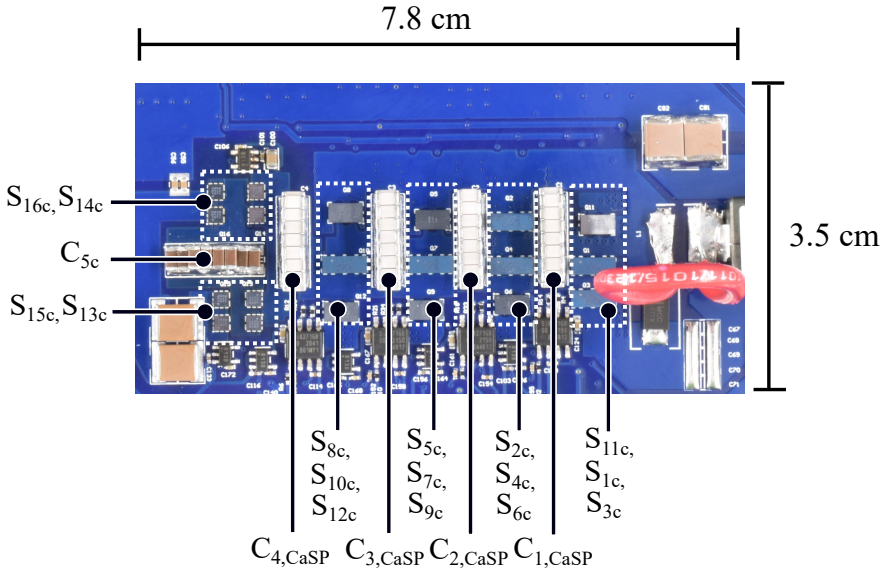


Figure 7.13: Annotated photograph of the power stage for the CaSP. Table 7.2 lists the part numbers and parameters of the major components of the full system.

Table 7.2: Component listing of the microinverter system hardware prototype

Subsystem	Component	**Part No.**	**Parameters**
1-to-10 CaSP	S_{1c} - S_{4c}, S_{7c}, S_{10c}	EPC2022	100 V, 3.2 $m\Omega$
	S_{5c}, S_{6c}	EPC2033	150 V, 7 $m\Omega$
	S_{8c}, S_{9c}, S_{11c}, S_{12c}	EPC2034C	200 V, 8 $m\Omega$
	S_{13c} - S_{16c}	EPC2050	350 V, 80 $m\Omega$ × 2 (parallel)
	C_{1c} - C_{4c}	Murata GRM31C5C1H224JE02L	0.22 μF × 15 (parallel), C0G
	C_{5c}	Murata GCM31C5C2E223JX03L	0.022 μF × 12 (parallel), C0G
	L_{CaSP}	Coilcraft SLC1480-321MLD	320 nH
6-level FCML	GaN FETs	EPC2033	150 V, 7 $m\Omega$
	Flying Capacitors	TDK C5750X6S225K250KA	2.2 μF × 2–5 (parallel, ∼2.6 μF effective)
	L_{FCML}	Vishay IHLP6767GZER220M51	22 μH
Unfolder	GaN FETs	GS66508T-MR	650 V, 30 A
Buffer Capacitors	C_{in}	Cal Chip Electronics GMC55X7R226M50NT	22 μF × 20 (parallel, ∼? μF effective at 40 V)
	$C_{buff,line}$	Rubycon 500USK180MEFCSN25X30	180 μF, 500 V
	$C_{buff,res}$	TDK C5750X6S225K250KA	2.2 μF × 26 (parallel, ∼11.2 μF effective at 400 V)
Control	Microcontroller	TI F28379D controlCARD	C2000 Series Microcontroller

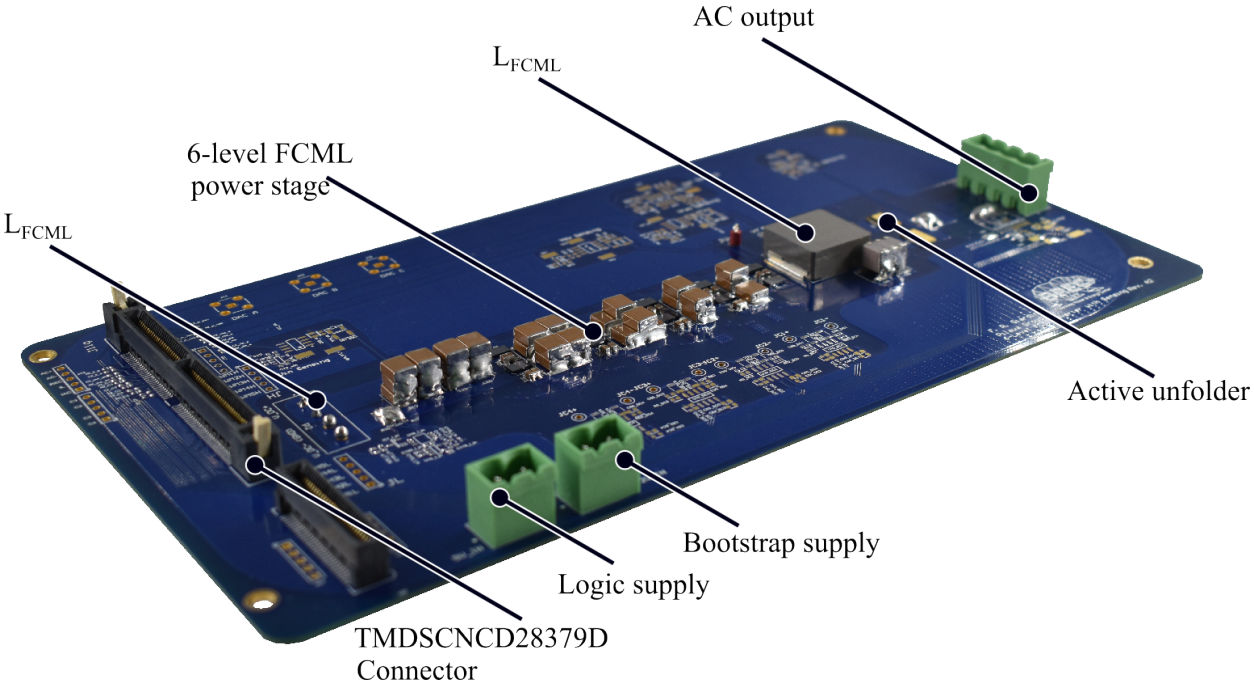


Figure 7.14: Developmental prototype of the inverting FCML stage for the proposed microinverter. Table 7.2 lists the part numbers and parameters of the major components of the full system. (Figure made in collaboration with Francesca Giardine.)

ponents used in the complete microinverter system. The total boxed volume of the power conversion portion of the step-up and inverting stages is 51.7 cm^3, amounting to a power density of 9.7 W/cm^3 (158.6 W/in^3), which excludes the volume from the buffer stage.

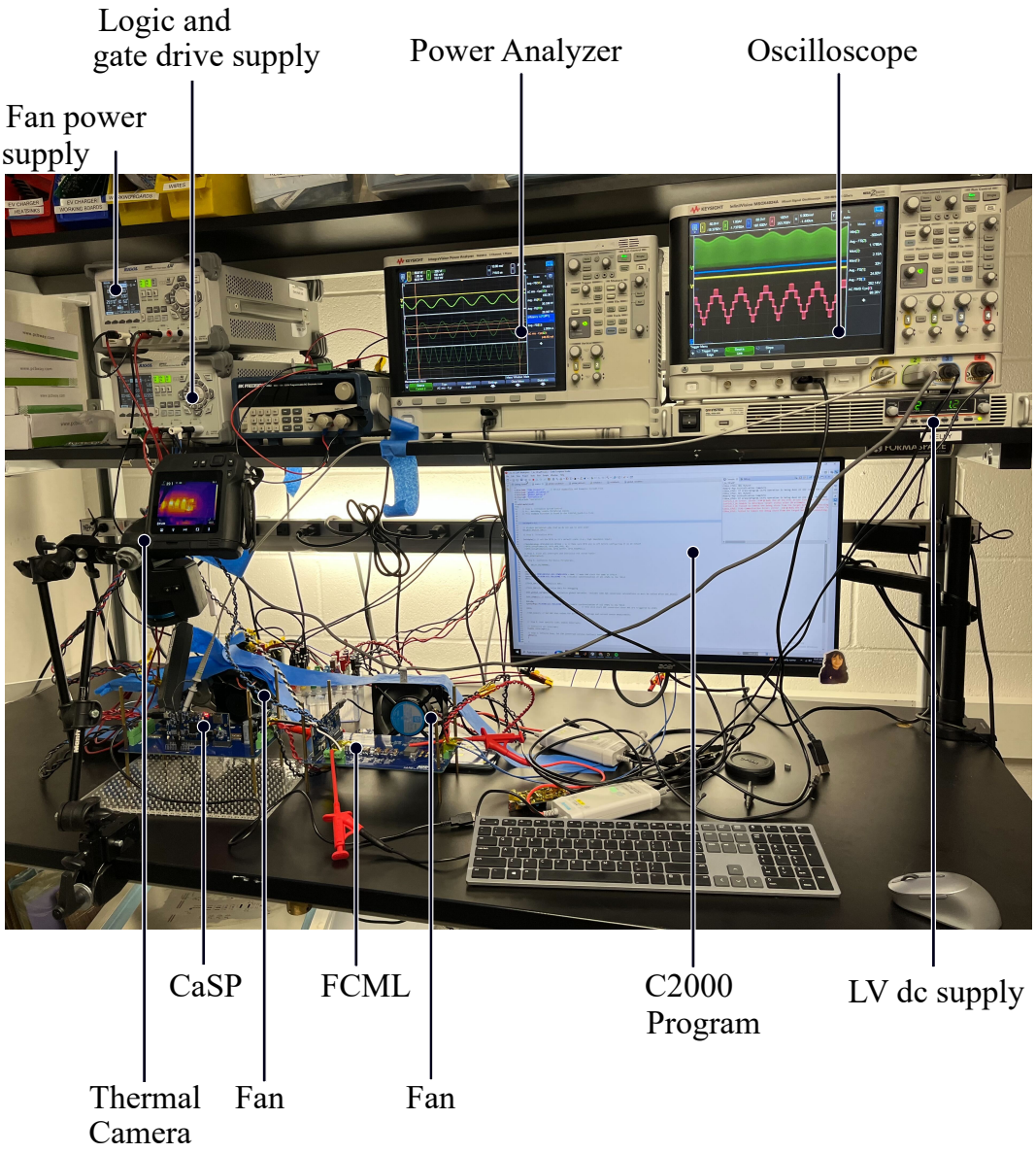


Figure 7.15: Test setup for the microinverter system prototype verification. The resistive load sits below the table of the shown test setup. (Figure made in collaboration with Francesca Giardine.)

The 1-to-10 CaSP and energy buffer stages are shown in Fig. 7.12. Fig. 7.13 displays a zoomed-in annotated photograph of the CaSP power stage. Class 1 MLCCs are used as the flying capacitors in the CaSP stage. In [141], it is demonstrated that a 1-to-10 conversion can be achieved using class 2 MLCCs. In this system prototype, class 1 MLCCs were chosen in mind that the voltage across a PV panel can change, affecting the capacitance

derating due to the voltage-capacitance dependence in class 2 MLCCs. Because there is no voltage-capacitance dependency, class 1 MLCCs can ensure that the system is capable of soft-switching techniques more reliably. A cascaded bootstrap methodology delivers charge to the individual gate drivers in the CaSP circuit [122].

Two electrolytic capacitors placed in parallel are used to buffer the twice-line frequency power pulsation (C_{buff}) in the system. Noted, although this system is designed to utilize capacitors with higher reliability, aluminum electrolytic capacitors were chosen to preserve space on the hardware prototype, as aluminum electrolytic capacitors offer the highest energy density around 400 V [14], [16]. Several paralleled class 2 MLCCs are also placed in parallel with the aluminum electrolytic capacitors; MLCCs have a broader tolerance to withstand high rms currents, and thus, they are used to decrease the rms current stress in the electrolytic capacitors that are caused by the sizeable resonant current exhibited at the input port of the CaSP stage.

As shown in Fig. 7.14, the FCML inverting stage is placed on a separate developmental board and has additional sensing circuitry to monitor the voltages across the four flying capacitors and the inductor current in the FCML system. The FCML stage has the power processing stage placed on the top side of the PCB, while the gate drive and sensing components are placed on the bottom side of the PCB. A cascaded bootstrap technique delivers power to the gate drive circuits in the FCML stage [122].

Fig. 7.15 displays the testing setup for the microinverter system hardware prototype. A GW Instek PSU 60-25 is used as the LV dc input supply for the system. The load, a resistor bank placed directly under the test setup, is not shown in the test setup figure. A Keysight PA2201A is used as a high-precision analyzer to collect the input and output power measurements, while a Keysight MSOX4024A oscilloscope is used to monitor the critical system voltage and current waveforms throughout testing. Two separate fans were used to provide air cooling to both boards. A Rigol DP832 is used as the LV dc supply for both boards' logic and gate drive supplies and to supply the fans with power. A FLIR thermal camera is used to monitor the system's thermal stresses.

Fig.7.16 shows the measured experimental waveforms for a complete system operation of 38 V to 240 V_{ac} with an output power rated at 500 W. As shown in the figure, some twice-line frequency ripple power pulsation remains coupled to the CaSP inductor current and the HV dc bus. The voltage at the switched-node of the FCML indicates that the flying capacitors can achieve passive charge balancing at the prototype's full rated power and voltage. Fig. 7.17 shows inductor current $i_{L,CaSP}$, and switched-node voltages $v_{sw,CaSP}$ and $v_{sw,FCML}$ during one switching period. The CaSP inductor current $i_{L,CaSP}$ can approximately discharge to 0 A at the end of each sub-period, allowing all switches in the CaSP stage to achieve ZCS. Fig. 7.18 shows the total system efficiency for a rated output power incremented from 50 W to 500 W. The system's peak efficiency, which occurs at $P_{out} = 340$ W, is 94.3% while the efficiency at full load is 93.8%. Fig. 7.19 shows the temperature of both the CaSP and FCML power stages at full load. The EPC2050 GaN devices generate the dominant source of heat. This is expected due to the small die volume of the devices, decreasing their ability to handle larger rms currents.

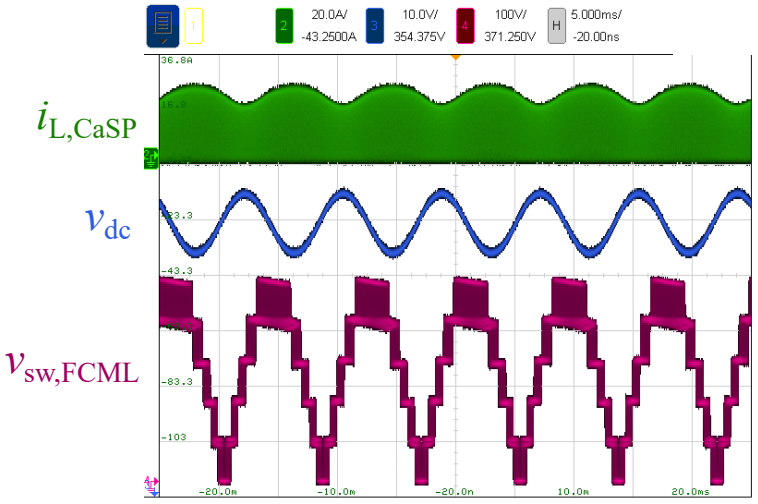


Figure 7.16: Experimental waveforms of CaSP inductor current $i_{L,CaSP}$, the HV dc bus voltage v_{dc}, and the FCML switched-node voltage $v_{sw,FCML}$ for a 38 V to 240 V_{ac} conversion at full load P_{out} = 500 W. (Figure made in collaboration with Francesca Giardine.)

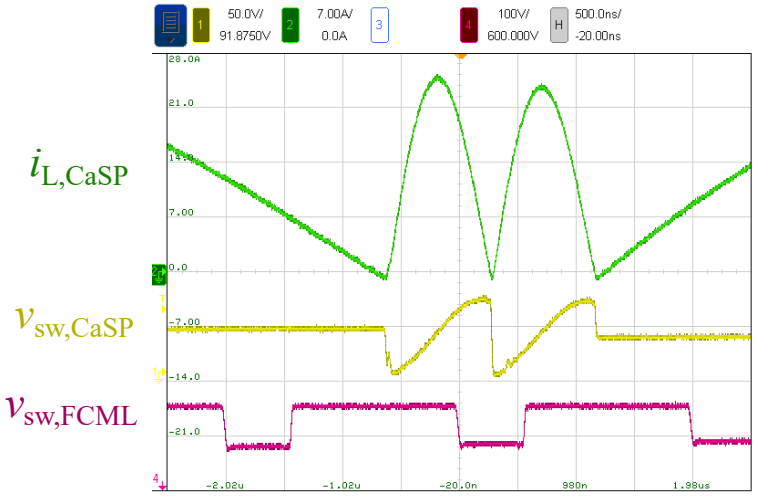


Figure 7.17: Inductor current of L_{CaSP}, and the CaSP and FCML switched-node voltage $v_{sw,CaSP}$ and $v_{sw,FCML}$, respectively, during ZCS operation for a 38 V to 240 V_{ac} conversion at full load P_{out} = 500 W for one switching period. (Figure made in collaboration with Francesca Giardine.)

To test the ability of the microinverter system to undergo a hard start-up at the LV dc input port, a 0 V to 36 V dc transient was inputted along the LV input port of the system. The output of the steady-state system is v_{ac} = 240 V_{rms} and P_{out} = 110 W. Fig. 7.20

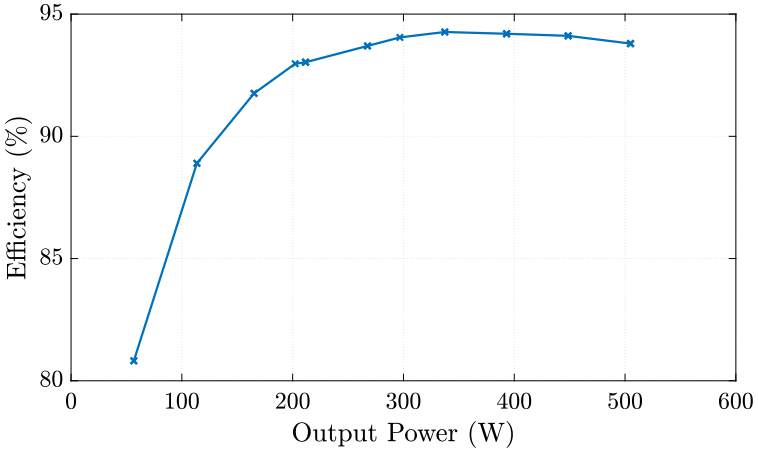
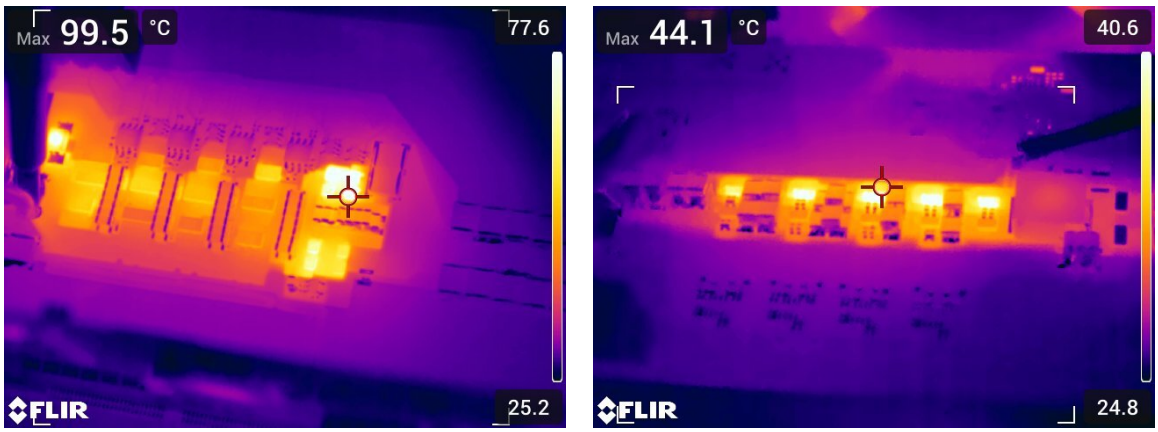


Figure 7.18: Efficiency of full system over an output power range from 50 W to 500 W for a 35 V to 240 V_{ac} system conversion. (Figure made in collaboration with Francesca Giardine.)



(a) (b)

Figure 7.19: Thermal temperature of system at for a 38 V to 240 V_{ac} conversion at full load P_{out} = 500 W: (a) the step-up CaSP stage; (b) the inverting FCML stage. (Figures made in collaboration with Francesca Giardine.)

shows the voltages across two of the flying capacitors, the switched-node, and the HV dc output of the CaSP stage over time when this transient occurs. Fig. 7.21 and Fig. 7.22 show the startup voltage waveforms across the flying capacitors in the FCML stage and relevant system voltage waveforms, respectively, when the transient occurs. As shown in the figures, the voltages passively and stably increase over time, verifying that the microinverter system can handle a wide range of transient steps at the LV dc input port of the system.

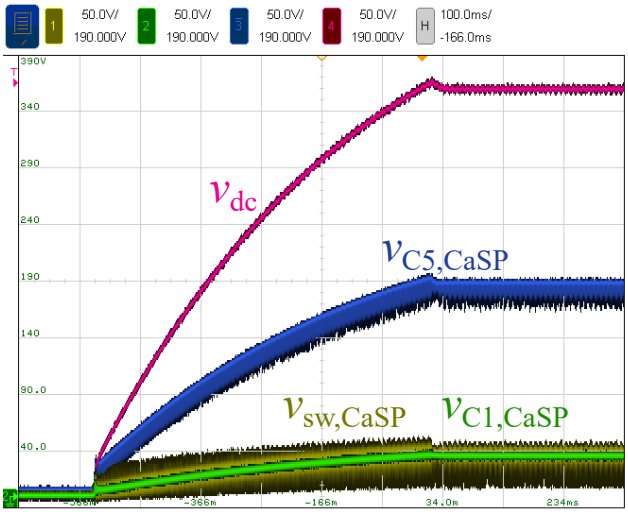


Figure 7.20: The CaSP voltage waveforms during a hard startup where the input of the system starts from $v_{in} = 0$ V to 36 V. The output when the system completes its startup is $v_{ac} = 240$ V_{rms} and $P_{out} = 110$ W. The CaSP waveforms shown are CaSP switched-node voltage $v_{sw,CaSP}$, the CaSP C_1 capacitor voltage $v_{C1,CaSP}$, the CaSP C_5 capacitor voltage $v_{C5,CaSP}$, and HV dc bus v_{dc}.

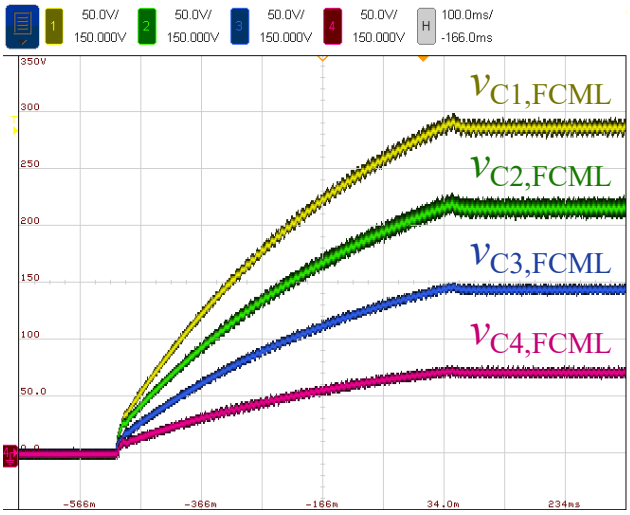


Figure 7.21: The FCML voltage waveforms during a hard startup where the input of the system starts from $v_{in} = 0$ V to 36 V. The output when the system completes its startup is $v_{ac} = 240$ V_{rms} and $P_{out} = 110$ W. The FCML waveforms shown are the FCML C_1 capacitor voltage $v_{C1,FCML}$, the FCML C_2 capacitor voltage $v_{C2,CaSP}$, the FCML C_3 capacitor voltage $v_{C3,FCML}$, and the FCML C_4 capacitor voltage $v_{C4,CaSP}$.

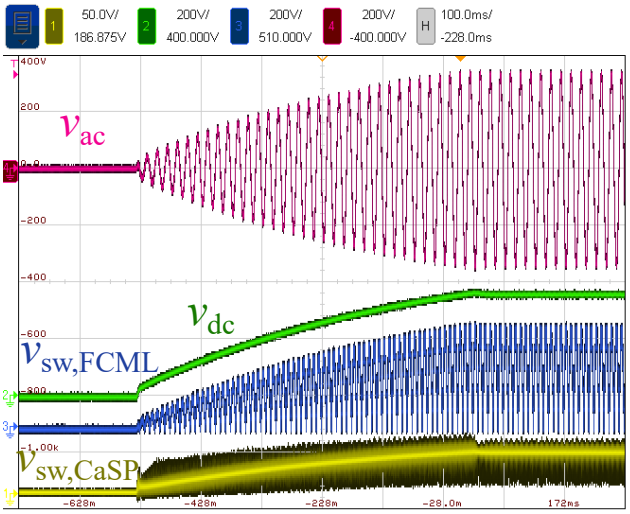


Figure 7.22: The system voltage waveforms during a hard startup where the input of the system starts from $v_{in} = 0$ V to 36 V. The output when the system completes its startup is $v_{ac} = 240$ V_{rms} and $P_{out} = 110$ W. The system waveforms shown are the CaSP switched-node voltage $v_{sw,CaSP}$, the FCML switched-node voltage $v_{sw,FCML}$, the HV dc bus v_{dc}, and the system's 240 V_{rms} system output v_{ac}.

7.4 Conclusion

As residential solar is becoming an increasingly widespread solution for people to provide electricity to their homes and the ac grid, there is a need for a reliable microinverter solution that has a long lifetime, is highly efficient, and has a low cost. This work demonstrates the feasibility of using a fixed-ratio 1-to-10 Cascaded Series-Parallel converter as a step-up stage combined with a 6-level Flying Capacitor Multi-Level inverter for a residential scale solar panel application. The intent behind this system design is to offer a two-stage solution that is highly efficient and increases the power density of the system to decrease manufacturing and shipping costs. Hardware results are shown up to an output power of 500 W, with a peak system efficiency of 94.3% and a full load efficiency of 93.8%.

Chapter 8

Conclusion

8.1 Concluding Remarks

In a conventional single-phase power converter, there are two stages. The first stage is the power factor correction and rectification stage that converts the ac power waveform sourced from the ac grid, to a dc power waveform that matches the demands of the dc load. In some applications, the first stage is operated in reverse, where the stage now acts as an inverter and converts the dc power supplied by the dc port to an ac waveform within ac grid regulations. The second stage is the energy buffer, which buffers the twice-line frequency power pulsation that inherently couples to the dc-link in single-phase systems.

Part I of this thesis studies the application area of electric vehicle (EV) on-board charging. In a conventional level-2 EV on-board charger system, a two-level step-up converter acts as the power factor correction/inverting stage, and a bank of electrolytic capacitors is used for the energy buffer stage. In this conventional solution, the inductor in the PFC stage and the bank of electrolytic capacitors in the buffer stage consume the overall system volume and weight. To increase the power density of the system, an N-level converter can be used as the PFC stage, while an active buffer solution can replace the electrolytic capacitor bank.

Chapter 3 introduces a novel level-2 EV charging solution, where a pair of interleaved 6-level Flying Capacitor Multi-level converters (FCMLs) are used as the PFC/inverting stage and a Series-Stacked Buffer (SSB) is used as the buffer stage. The 6-level FCML has a circuit topology construction similar to the two-level step-up converter. However, the 6-level FCML utilizes four "flying" capacitors that assist with energy storage and transfer, decreasing the inductance requirement in the stage. Moreover, capacitors contain orders of magnitude of higher energy density levels than inductors, significantly reducing the system's volumetric and gravimetric energy densities. Additionally, the phase-shifted pulse width modulation control of the FCML induces a higher effective frequency at the switched-node, further decreasing the size of the required inductive component and thus increasing the system's power density. The SSB utilizes a capacitor as the primary energy buffer. The capacitor is allowed to have a large voltage ripple, decreasing the capacitance requirement

of the buffer stage. The active and passive circuitry network placed in series with the buffer capacitor effectively cancels any twice-line frequency ripple along the dc-link. The reduction in capacitance enables higher energy densities in the overall system. Moreover, because the buffer capacitor blocks the high voltage of the dc port, the active circuitry processes only a small portion of the system's power; thus, it does not compromise the system's efficiency. The first hardware prototype revision of the proposed EV charger system achieves a 99% peak efficiency and a full load (P_{out} = 6 kW) efficiency of 97.7%. The volumetric power density of the system is 201 W/in^3, while the gravimetric power density of the system is 5.5 kW/kg.

Chapter 4 further expands upon the design and control of the SSB and explains how it is not a desirable buffer choice for systems with a low dc source impedance, such as EV batteries. This is due to the loss compensation control of the SSB, which induces a large residual twice-line frequency ripple along the dc-link for systems with low dc source impedance. This chapter proposes the Charge Injection method, which encompasses a novel hardware and control topology for the SSB. The Charge Injection method contains an additional path for current to flow outside the traditional SSB branch. As a result, real and reactive power handling are decoupled in the SSB, allowing the auxiliary active converter to be solely controlled to cancel the ripple voltage across the C_1 capacitor. A hardware prototype was built for the SSB with the Charge Injection method and verifies that the proposed system can reduce the dc-link current ripple up to 5× compared to a traditional SSB.

Part II of this thesis discusses the single-phase application area of microinverters. Microinverters are used to invert the dc power supplied by a residential solar panel, to required voltage and current levels for the ac distribution grid. Chapter 5 presents a survey of several residential solar panels and discusses conventional voltages and power levels that microinverters must endure. The survey concludes that microinverters must have capabilities to invert a 35 V_{dc} signal to extract the maximum power from the solar panel and be able to tolerate an open circuit voltage of the solar panel of up to 43 V. Moreover, microinverters must be able to tolerate power levels up to 400 W.

Microinverters are conventionally designed with just one stage for the inverting stage. The inverting stage both steps up and down the voltage the low-voltage solar panel provides to produce a rectified sine wave that is then unfolded. This approach forces the energy buffer to be placed on the low-voltage dc bus in parallel with the solar panel. As a result, the buffer must tolerate high rms currents, requiring a larger buffer capacitance such that only an electrolytic solution is sensible. To decrease the capacitance requirement such that more energy-dense and reliable capacitors can be used, a novel two-part inverting stage is proposed in Chapter 7; a 1-to-10 Cascaded Series-Parallel converter (CaSP) is used to step-up the voltage from the solar panel to a high voltage dc bus, where the energy buffer is placed, and a 6-level FCML inverts the large dc bus voltage. This two-stage inverter solution utilizes multi-level hybrid switched-capacitor converters to further reduce the entire system's volume and weight, reducing manufacturing and shipping costs for larger-scale manufacturing. Chapter 6 discusses the design of the 1-to-10 CaSP and how it is an optimal converter choice for a 1-to-10 step-up application. Alone, the 1-to-10 CaSP is able to achieve

a peak efficiency of 96.1% and a full load ($P_{\text{out}} = 300$ W) efficiency of 95.9%. The complete microinverter system is able to achieve a peak efficiency of 94.3% and a full load ($P_{\text{out}} = 500$ W) efficiency of 93.8%.

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