Joint LDPC Decoding and Timing Recovery Using Code Constraint Feedback

Dong-U Lee, *Member, IEEE,* Esteban L. Vallés, *Student Member, IEEE,*
John D. Villasenor, *Senior Member, IEEE,* and Christopher R. Jones, *Member, IEEE*

***Abstract*— Timing recovery and channel decoding are traditionally performed independently. However, we show here that the information generated during the iterative decoding of Low-Density Parity-Check (LDPC) coded data can be fed back to the timing recovery circuit to enable accurate estimation of frequency and phase errors without the need for any pilot symbols. We describe a method capable of handling large offsets with complexity that grows linearly with offset size. Combining the LDPC constraint node observations with a properly calibrated phase locked loop allows successful tracking of a constant time delay, a frequency offset and a random phase walk.**

***Index Terms*— Low-density parity-check codes, symbol timing synchronization.**

I. Introduction

LDPC codes have received significant attention due to their ability to operate at capacity-approaching SNRs [1]. Realizing the full potential of LDPC codes requires receivers in which the timing recovery process can successfully acquire and track symbols at these lower SNRs. Acquisition and tracking have traditionally been performed independently of channel decoding. However, the information generated for the constraint nodes during the LDPC decoding process provides information that can be fed back to the timing recovery circuit, allowing operation at very low SNRs where other timing synchronization methods typically fail. The number and nature of satisfied LDPC constraint node equations provides a measure not only of code convergence, but also of the underlying accuracy of the timing estimates used in acquiring the sampled data input to the LDPC decoder.

Previous treatments in the literature addressing joint LDPC decoding and timing recovery has focused on the use of output codewords produced as the iterations progress [2], [3]. By contrast, we exploit the information available from the metrics computed for the constraint nodes of an LDPC code during the decoding process. In addition, we use a waveform model that more directly captures the distortions induced by relative transmitter/receiver motion and other receiver-side timing errors.

Manuscript received September 24, 2005. The associate editor coordinating the review of this letter and approving it for publication was Prof. Marc Fossorier.

Dong-U Lee, Esteban L. Vallés, and John D. Villasenor are with the Electrical Engineering Department, University of California, Los Angeles, CA 90095-1594, USA (e-mail: {dongu, villa}@icsl.ucla.edu; evalles@ee.ucla.edu).

Christopher R. Jones is with the Jet Propulsion Laboratory, Pasadena, CA 91109-8099, USA (e-mail: christop@jpl.nasa.gov).

Digital Object Identifier 10.1109/LCOMM.2006.03003.

II. Timing Error Modalities

We consider an LDPC encoded BPSK signal comprised of a series of N root raised-cosine pulses $h_{RRC}(t)$, transmitted at integer multiples of a symbol interval T and scaled by a_i, where $a_i \in \{\pm 1\}$ is the BPSK modulated value of the i^{th} symbol: $s(t) = \sum_{i=0}^{N-1} a_i \, h_{RRC}\,(t - iT)$. In a system with no timing errors, $s(t)$ would be sampled at the receiver at multiples of a sampling interval T_s. This produces a sampled received sequence $r[k] = s(kT_s) + n(kT_s)$, where $n(kT_s)$ is AWGN noise introduced by the channel. When timing errors are present, the assumed time reference for the k^{th} sample at the receiver differs from corresponding time reference at the transmitter according to some function $\tau[k]$, giving $r[k] = s(kT_s + \tau[k]) + n(kT_s)$. Substituting in $s(t)$ gives

$$r[k] = \sum_{i=0}^{N-1} a_i \, h_{RRC}\,(kT_s + \tau[k] - iT) + n(kT_s).$$

Note that this representation alters the time instances at which samples are taken and appropriately avoids the introduction of inter-symbol interference (ISI) in the received waveform.

We consider the following timing error modalities.

Constant time offset. All sample times are offset by the same constant delay D with respect to the ideal sampling time, giving $\tau[k] = D$ for all k.

Random walk. The timing error at each sampling instant is given by the previous error further perturbed according to a zero mean Gaussian random variable with variance σ_d^2, denoted by $\mathcal{N}(0, \sigma_d^2)$. This gives $\tau[k] = \tau[k-1] + T_s \, \mathcal{N}(0, \sigma_d^2)$.

Constant frequency offset. A frequency offset F_{PPM} measured in parts per million, assuming an initial timing offset of zero for the first symbol, is described by $\tau[k] = \tau[k-1] + T_s \, F_{PPM}/10^6$.

In previous treatments of this topic, timing errors have been modeled as perturbations of the symbol (as opposed to sample) times of the individual pulses followed by superposition [2], [4]. However, applying differing timing shifts to individual pulses and then superimposing the shifted pulses gives rise to ISI. While this approach may be appropriate for transmitters exhibiting symbol clock jitter, it is not well suited for the present work, which assumes a correctly constructed ISI-free waveform at the transmitter and is concerned with receiver-side timing errors.

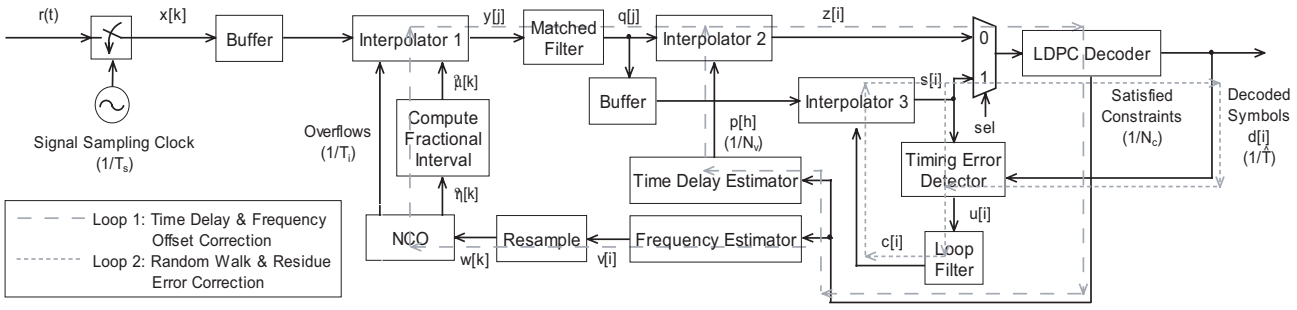

Fig. 1. Receiver model for timing recovery. Signal labels indexed with i, j, and k represent rate $1/T$, $1/T_i$, and $1/T_s$ respectively.

III. Receiver Model

Fig. 1 illustrates the receiver architecture which exploits feedback from the LDPC decoder to manage timing errors. The received waveform is initially sampled at intervals of T_s and stored into a buffer. The interpolator computes interpolants at intervals of T_i using linear interpolation, which are then used for the matched filtering process [5]. In this work, we use $T_i = \hat{T}/2$ and $T_s = \hat{T}/4$, where $\hat{T}$ is the receiver-side assumption of the transmitter symbol period T (i.e. the symbol period that would be seen by the receiver in the absence of any timing perturbations). Storage cost approximately equals NT/T_s or $4N$ samples. A few additional pre and post pended samples may be stored to accommodate potential fixed time delays.

Loop 1 in Fig. 1 is first executed to recover constant time phase and frequency offsets. The phase error estimator provides the interpolator (after the matched filter) with a time offset, which is used to correct the constant time delay. The frequency estimator provides a frequency control word which is resampled at a rate of $1/T_s$ and fed to the numerically controlled oscillator (NCO).

Both the phase and frequency offset estimation processes use feedback based on the percentage of satisfied LDPC constraints. The utility of this metric as a feedback mechanism is illustrated for the case of frequency offsets in Fig. 2, which shows the average percentage of satisfied constraints as a function of frequency estimation error for different SNRs (E_b/N_0) and numbers of LDPC iterations. A similar plot, with similar tradeoffs, can be constructed for the relationship between phase estimation error and satisfied LDPC constraints. The $(1944, 972)$ irregular LDPC code proposed for the IEEE 802.11n standard is used throughout this work [6]. Fig. 2 indicates the rate of falloff as the estimation error increases, and shows that the best frequency error discrimination occurs for errors within approximately 200 ppm. This information is used in determining the step size to use in the frequency offset search. Fig. 2 also indicates the costs (in computations) and benefits (in increasing the percentage of satisfied constraints) of increasing the number of iterations.

A search based on successively narrower search windows is used to determine the frequency offset. For each "search iteration", multiple LDPC decoding iterations are performed for each candidate frequency error at evenly spaced steps in the window. For the first search iteration, the frequency offset estimate giving the most satisfied constraints is found. In the case of ties, the midpoint is taken. The search window is

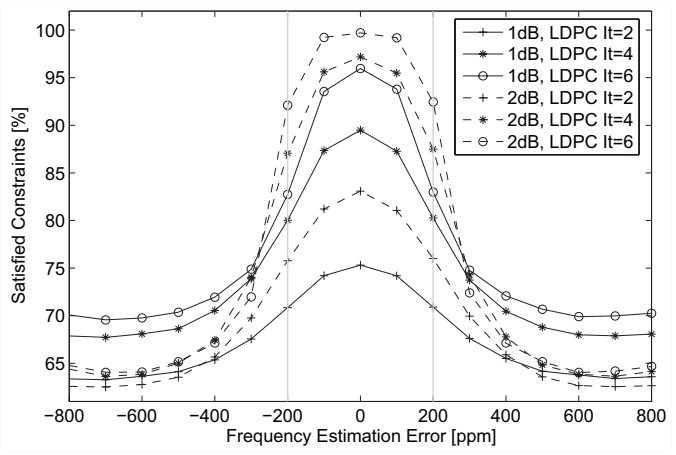

Fig. 2. Percentage of satisfied constraints as a function of frequency estimation error. Curves for 2, 4, and 6 LDPC iterations are shown for E_b/N_0 of 1 and 2 dB. An average of 500 trials were used for each data point.

recentered to this frequency offset, the search window and the step size are reduced by a factor of c_1 and c_2 respectively, and the next search iteration is performed. Based on extensive simulations, halving the window size and step size with each iteration (i.e. $c_1 = 2$ and $c_2 = 2$) has been found to be effective. As long as the the frequency offset is contained within the initial search window, the algorithm will converge with an accuracy that increases with increasing SNR. The accuracy of the receiver's estimate of the frequency offset is determined by the smallest search step size used (with diminishing sensitivity below 40 ppm). The complexity grows linearly with the width of the range of frequency offsets contained in the initial search window.

For the simulation results presented here, an initial window of width ± 2000 ppm (i.e. $\pm 0.2\%$), a step size of 400 ppm, three LDPC iterations per estimate and a total of three search iterations were used. Hence for these parameters, a total of 99 LDPC decoding iterations are needed per search iteration. Time delays can be tracked in the same manner. Based on experiments analogous to those used for frequency offsets, a step size of $0.2T$, one search iteration, and three LDPC iterations per estimate were chosen. It is possible to track waveforms where both time delays and frequency offsets are present at the cost of quadratic computational complexity. A two-dimensional search strategy is employed where for a given time delay candidate, the satisfied constraints of all frequency offset candidates are computed.

TABLE I

REDUCTION IN TIMING ERROR WITH SEARCH ITERATIONS USING A FREQUENCY OFFSET OF 1730 PPM INJECTED INTO THE TRANSMITTED WAVEFORM. THE RMS TIMING ERROR IS BASED ON THE NORMALIZATION σ_ϵ/T, WHERE σ_ϵ IS THE TIMING ERROR.

Search Iteration	1	2	3
Window Size [ppm]	4000	2000	1000
Window [ppm]	$[-2000, 2000]$	$[600, 2600]$	$[1300, 2300]$
Center Offset [ppm]	0	1600	1700
Step Size [ppm]	400	200	100
Offset Estimate [ppm]	1600	1800	1700
Estimation Err [ppm]	130	70	30
RMS Timing Err [%]	16.87	8.80	5.54

After large-scale phase and frequency errors have been identified in loop 1, loop 2 is utilized to handle random walks, correct residual phase and frequency errors, and perform the remaining LDPC decoding. A conventional first-order PLL-based circuit with a decision-directed Mueller-Müller timing error detector (M&M TED) [7] is used. After every LDPC iteration, the M&M TED is provided with the symbols decoded by the LDPC decoder, analogous to the approach used in the recent work of Barry *et al.* [2]. The number of iterations for loop 2 is set to be the same as for normal LDPC decoding.

IV. EXPERIMENTAL RESULTS

For all experiments, root raised-cosine pulse shaping with a roll-off factor of 0.3 and a 12-tap FIR filter for matched filtering were used. The loop gain of loop 2 was fixed to $Kp = 0.001$. For time delay and frequency offset simulations, random offsets over $\pm 0.5T$ and ± 2000 ppm were used.

Table 1 provides an example of how the timing errors decrease as a function of the number of search iterations using loop 1 only. An initial search window of ± 2000 ppm with an initial step size of 400 ppm were used. A frequency offset of 1730 ppm was injected to the transmitted waveform at $E_b/N_0 = 1$ dB. After the third iteration, the frequency estimation error has been reduced to 30 ppm and the RMS timing error to 5.54%.

While Table 1 illustrates the convergence of the frequency estimation for one particular example, Figure 3 shows the average behavior of the frequency error and the RMS timing error as a function of E_b/N_0 based on 500 trials. As would be expected, low E_b/N_0 values decrease the ability to accurately estimate frequency and phase errors. Above E_b/N_0 of 0.9 dB, both curves exhibit asymptotic-like behavior, flattening to 40 ppm and 7% respectively.

Figure 4 gives the bit error rate (BER) and frame error rate (FER) performance for different receiver architectures and timing offsets. For constant time delays and frequency offsets, the proposed model is able to get within $0.1 \sim 0.2$ dB of the ideal (i.e. perfect timing) code performance.

V. CONCLUSIONS

We have presented a pilotless symbol timing recovery architecture for tracking time delay, frequency offsets and random walks using LDPC feedback. A two-stage receiver architecture is proposed where the first stage corrects large-scale time delays and frequency offsets, and the second stage tracks random walks and corrects residual time and frequency offsets. The algorithm has complexity that grows linearly with the offset size. Performance within $0.1 \sim 0.2$ dB of the ideal code performance can be achieved for large phase and frequency offsets.

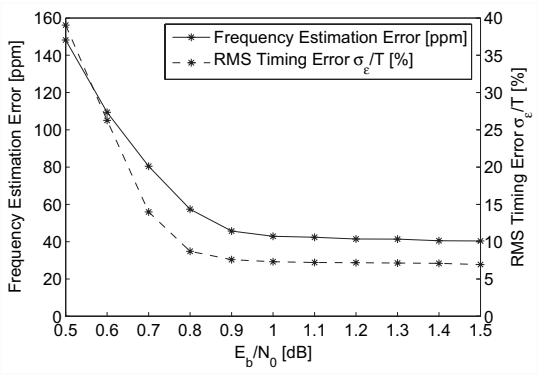

Fig. 3. Frequency estimation error and RMS timing error behavior with E_b/N_0. An average of 500 trials are used for each data point.

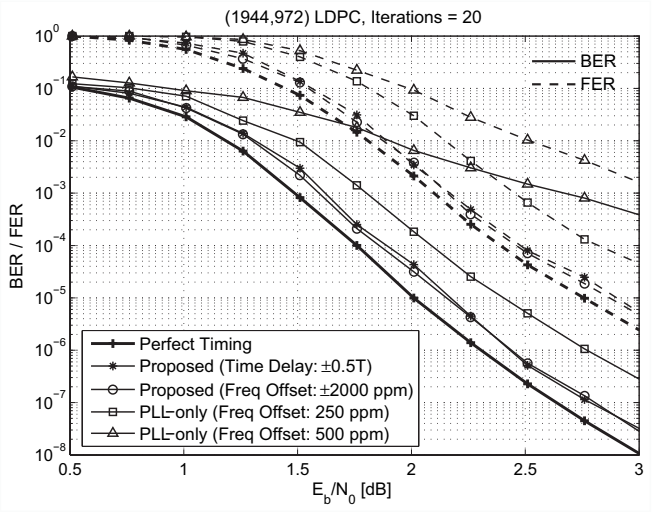

Fig. 4. BER/FER performance for different receiver architectures and timing offsets. The PLL-only architecture employs a second order loop filter with the loop gains optimized for each case.

REFERENCES

[1] R. G. Gallager, "Low-density parity-check codes," *IRE Trans. Inform. Theory*, vol. IT-8, pp. 21–28, Jan. 1962.

[2] J. Barry, A. Kavčić, S. McLaughlin, A. Nayak, and W. Zeng, "Iterative timing recovery," *IEEE Sig. Proc. Mag.*, vol. 21, pp. 89–102, Jan. 2004.

[3] J. Liu, H. Song, and B.V.K. Vijaya Kumar, "Symbol timing recovery for low-SNR partial response recording channels," in *Proc. IEEE Global Telecomm. Conf.*, 2002, pp. 1129–1136.

[4] L.E. Franks, "Carrier and bit synchronization in data communication - a tutorial review," *IEEE Trans. Comm.*, vol. 28, pp. 1107–1121, Aug. 1980.

[5] F. L. Gardner, "Interpolation in digital modems – part I: fundamentals," *IEEE Trans. Comm.*, vol. 41, pp. 501–507, Mar. 1993.

[6] A.I. Vila Casado, W. Weng, and R. Wesel, "Multiple rate low-density parity-check codes with constant block length," in *Proc. IEEE Asilomar Conf. on Sig., Syst. and Comput.*, vol. 2, 2004, pp. 2010–2014.

[7] K. Mueller and M. Müller, "Timing recovery for digital synchronous data receivers," *IEEE Trans. Comm.*, vol. 24, pp. 516–531, May 1976.