Switched Capacitor Quasi-Adiabatic Clocks

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***Abstract*—Clock Distribution Networks (CDNs) in high speed designs can consume 30-50% of the total chip dynamic power. Adiabatic clock circuits can save some of this power, but these depend on a time varying power supply which is difficult to implement in practice. In this paper, we present the first quasi-adiabatic clock circuit with a constant supply voltage at high speeds. Our proposed adiabatic clocks attain an average 23% clock power savings with better slew rate and the same skew compared to traditional buffered clocks.**

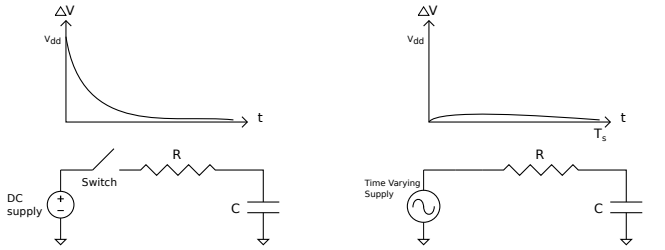
I. Introduction

Clock Distribution Networks (CDNs) synchronize most data signals by generating a common reference. Although clock signals seem like a simple control signal, they consume significant amounts of power and require high accuracy. In high-speed applications, CDNs have been shown to consume 30-50% of the total chip dynamic power. In modern technologies, power consumption has become a primary design issue that can affect circuit performance, reliability, and require bulky, expensive cooling systems such as heat sinks and fans. Reducing the power consumed in the clock network is highly challenging and is an actively researched area of circuit design and design automation [**?**].

Over the past decades, numerous effective techniques have decreased dynamic power consumption. Clock gating can reduce clock power, but active devices limit power savings since they cannot be disabled. Reducing the supply voltage decreases the dynamic power quadratically, however threshold voltage lower bounds limit potential scaling since $V_{dd}^2/V_{threshold}^2 \geq 10$ [**?**]. Frequency scaling is often used in conjunction with voltage scaling to achieve a cubic power reduction, but many high-performance applications require improvements in peak performance. Recently, distributed resonant clocking has reduced dynamic clock power by up to 90% in theory [**?**] and 30% in practice [**?**]. However, the passive component area overhead prevents adoption. While these techniques effectively reduce power, increased integration levels demand more techniques for power reduction.

Adiabatic circuits reduce dynamic power by recycling energy. Previously, adiabatic clocking circuits were differential with time-varying supplies that are hard to implement, and only practical at low-speeds. Quasi-adiabatic circuits with constant supplies, on the other hand, do not recycle 100% of the dynamic power, but often have simpler designs which make them more practical to implement. In this paper, we introduce the first quasi-adiabatic clock circuit with a constant supply that saves substantial dynamic power at high speeds.

The remainder of this paper proceeds as follows: Section II presents adiabatic circuit models and reviews adiabatic behavior. Section III proposes our quasi-adiabatic circuit and its clock distribution application. Section IV proposes the circuit design and implementation. Section V quantifies the major performance metrics of power, slew, and skew using industrial clock benchmarks through circuit simulations compared to buffered clocks. Section VI concludes the paper and discusses the remaining road map to integrate our quasi-adiabatic clock circuit.



(a) The potential difference across resistor R when using a constant supply starts at V_{dd} and decays approaching zero.

(b) When using a time-varying supply, charges are being spread evenly across the entire time available, leading to a huge reduction in the peak current.

Fig. 1. A time-varying supply results in a reduction in the current peak which reduces the dynamic power compared to constant supplies.

II. Adiabatic Circuits

The word adiabatic means *impassable* in Greek which is a thermodynamic term for changing the state of matter with no loss of heat. Adiabatic switching circuits recycle energy between clock cycles which decreases dynamic power dissipation.

There are two types of adiabatic circuits: *fully adiabatic* with asymptotically zero energy dissipation and *quasi-adiabatic* with non-zero energy dissipation [**?**]. Fully adiabatic circuits are impossible due to fundamental energy losses in devices, but are theoretically possible with ideal devices. Quasi-adiabatic circuits, on the other hand, cannot achieve zero energy consumption even with ideal devices. However, this concession can potentially enable simpler circuit implementations yet still recycle substantial energy in the system.

Many quasi-adiabatic circuits use differential logic and a time-varying supply voltage. The two halves of the differential circuit are doing opposite activities (receiving negated inputs and producing a negated output). When the supply is time varying, the differential circuit can operate with only one half, while the other half is off. In every supply clock cycle, we get an output and its negation. Even when the supply is low, the process completes with no loss of data. Usually, the power dissipated when using constant supply voltage is

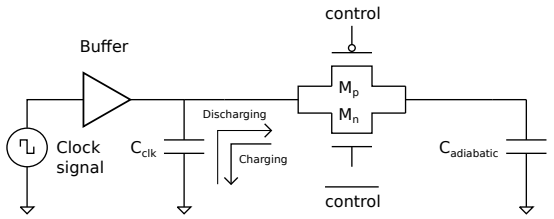


Fig. 2. Switching capacitor $C_{adiabatic}$ is responsible for charge recovery to reduce dynamic power in our proposed quasi-adiabatic clock circuit.

$(1/2)CV_{dd}^2$ as shown in Figure 1(a), but after using the time varying supply, the power dissipated can be calculated as $(RC/T_s)CV_{dd}^2$ where R is the driver resistance, C is the switching capacitor and T_s is the supply period [**?**]. This power reduction is due to spreading charge across time T_s as shown in Figure 1(b), which reduces the peak current. Increasing T_s allows more dynamic power savings. Examples of these types of quasi-adiabatic circuits are 2N-2P inverter logic, 2N-2N2P logic [**?**], Clock Adiabatic Circuits (CAL) [**?**], Pass-Transistor Adiabatic Logic (PAL) [**?**], Positive Feedback Adiabatic Logic (PFAL) [**?**], and the Differential Cascode Pre-resolve Adiabatic Logic (DCPAL) [**?**]

III. Proposed Quasi-adiabatic clock

Our quasi-adiabatic clock circuits use a switched capacitor as shown in Figure 2. Energy is recycled between the load capacitance (C_{clk}) and the extra storage element ($C_{adiabatic}$) to reduce overall power. The extra capacitor has two operating modes: First, it helps discharge the load capacitor, C_{clk}, from high to low while recovering some of the charge. Second, it aids the driving buffer by supplying charge to C_{clk} during the low to high transition. The amount of charge recovered and reused in $C_{adiabatic}$ determines the overall efficiency of the energy recycling. Our proposed clock is a switched-capacitor quasi-adiabatic circuit that does not recycle 100% of the energy, as it is active during only a limited part of the signal transition.

When two capacitors are in parallel at different potentials, current will flow from the higher potential to the lower potential until the two capacitors have the same potential. At this point, no current flow occurs and all nodes are in steady state. If $C_{adiabatic}$ is not disconnected during some portions of the cycle, the clock buffer will have to charge/discharge the total capacitive load $C_{clk} + C_{adiabatic}$ each cycle which would increase the overall power consumption to $(C_{clk} + C_{adiabatic})V_{dd}^2 f$. To avoid this, $C_{adiabatic}$ is switched into the circuit only during the charge recovery and reuse stages using a passgate as shown in Figure 2. The timing of the control signals, *control* and $\overline{control}$, determine the duration of the energy recovery and reuse.

Figure 3 illustrates the key idea of our quasi-adiabatic circuit which connects $C_{adiabatic}$ only when $V_{adiabatic} > V_{clk}$ and C_{clk} is charging, or when $V_{adiabatic} < V_{clk}$ and C_{clk} is discharging. If $C_{adiabatic}$ is sufficiently larger than C_{clk}, it will remain a steady-state voltage, $V_{steadystate}$, that is somewhere between V_{dd} and 0 as shown in Figure 3.

The control signals depend on the cross-over when $V_{clk} = V_{adiabatic}$, which in turn depends on the slew rate of the clock

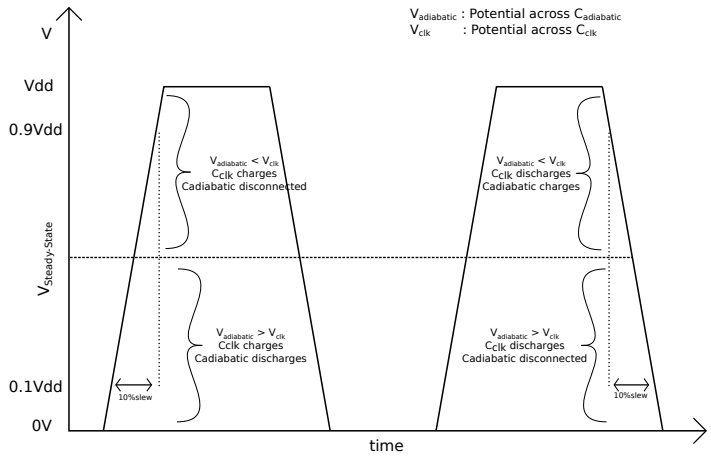


Fig. 3. Clock signal at C_{clk} with the help of $C_{adiabatic}$ switching activity, showing the different stages when $C_{adiabatic}$ is connected and disconnected.

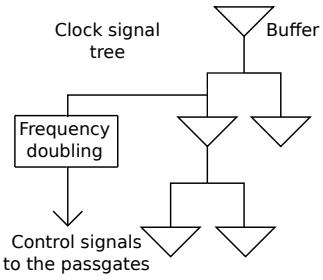


Fig. 4. Control signals are generated from a clock signal from an upper point in the CDN.

and any fluctuation in $V_{adiabatic}$. Typical clocks will have slew rates on the order of 10% of the clock period [**?**]. We size $C_{adiabatic}$ so its fluctuation can be neglected to the first order, but the amount of charging and discharging must be equal to maintain the steady-state voltage. The passgate control signals, *control* and $\overline{control}$, are double the clock frequency since they are required to enable $C_{adiabatic}$ twice per clock pulse for charging and discharging activities, respectively. For simplicity, it is assumed that both the recovery and reuse stages will be the same duration. Different recovery and reuse periods would require increasingly complex circuits potentially using voltage comparators. In addition, they wouldn't preserve a steady-state voltage on $C_{adiabatic}$.

IV. Circuit Implementation

The switched control signals must arrive before the clock transition so that the pass gate is properly enabled. This is done by supplying them from an upper point in the clock tree distribution as shown in Figure 4. Typically, the load on these control signals is much less than the clock and the remaining levels of the clock tree. Therefore, this timing is not difficult.

In order to double the control signal frequency, we use the proposed pulse generator circuit shown in Figure 5. The output from the NAND gate, a short pulse, will be the input to an even-number of series inverters to keep the same polarity while delaying the pulse. At the same time, the pulse from the

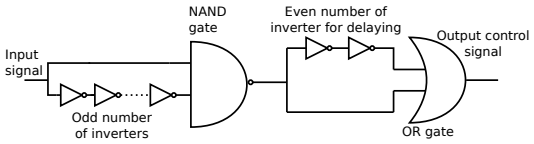


Fig. 5. The pulse generator circuit controls the pulse width and pulse separation to control the two phases of charge recovery and reuse.

NAND gate will be an input to an OR gate. This will result in two pulses at different times. The number of inverters used before the NAND gate determines the pulse width while the number of inverters before the OR gate determines the time gap between the two pulses. The output signal is $control$, inverting $control$ using a simple inverter will result in $\overline{control}$.

The sizes of the passgate and clock buffer transistors in Figure 2 determine the efficiency of our proposed system. The equivalent circuit of Figure 2 is shown in Figure 6. The current flowing into C_{clk} is the combination of the buffer current and the current from $C_{adiabatic}$ during the $0 \rightarrow 0.5Vdd$ transition and can be expressed by

$$i(t) = \frac{V_{dd}}{2R_p}(1 - e^{-t/R_pC_{clk}}) + \frac{V_{dd}}{R_{buf}}(1 - e^{-t/R_{buf}C_{clk}}) \quad (1)$$

where R_p is the passgate equivalent resistance, $(V_{dd}/2)(1 - e^{-t/R_pC_{clk}})$ is the change in potential from $C_{adiabatic}$ while from while $V_{dd}(1 - e^{-t/R_{buf}C_{clk}})$ is the change in potential from V_{dd} and the buffer. There is an additional current from V_{dd} to $C_{adiabatic}$ but this has no net effect on C_{clk}.

At the point where the clock voltage is $0.5V_{dd}$, the pass gate will be turned off and the C_{clk} is solely driven by the clock buffer during the remainder of a clock transition from $0.5V_{dd} \rightarrow V_{dd}$. The clock buffer must be sufficiently sized to satisfy a 10%-90% clock slew rate when it "takes over" midway through the transition. This can be expressed by

$$0.9V_{dd} = 0.5V_{dd}(1 - e^{-(0.5T_{slew})/R_{buf}C_{clk}}) \quad (2)$$

where R_{buf} is the buffer equivalent resistance and T_{slew} is the required slew rate. This assumes that the slew rate is constant during the entire transition which is an approximation. In reality, it is conservative since the slew rate of the first half of the signal transition is likely faster due to the adiabatic charging assistance. Solving Equation 2 using *Newton Raphson* obtains the required value for R_{buf}.

Since q=$\int i(t)dt$, the charge q can be expressed from Equation 1 as

$$q = V_{dd}(\frac{t}{2R_p} + \frac{C_{clk}}{2}e^{-t/R_pC_{clk}} + \frac{t}{R_{buf}} + C_{clk}e^{-t/R_{buf}C_{clk}}). \quad (3)$$

To get the voltage $V_{clk}(t)$, we can utilize $V_{clk}(t) = q/C_{clk}$, and since $V_{clk}(T_{CO}) = V_{dd}/2$, where T_{CO} is the cross over time when $V_{steadystate} = V_{clk}$. Now, we have one equation in one unknown, R_p, that can be obtained by

$$ln(R_p) + \frac{T_{CO}}{R_pC_{clk}} = ln(\frac{4T_{CO}^2e^{-T_{CO}/R_{buf}C_{clk}}}{R_{buf}C_{clk}^2}) \quad (4)$$

From Equation 2 and Equation 4, the buffer and the passgate sizes are of a known values that are used to maintain a $V_{steadystate}$ value of $V_{dd}/2$.

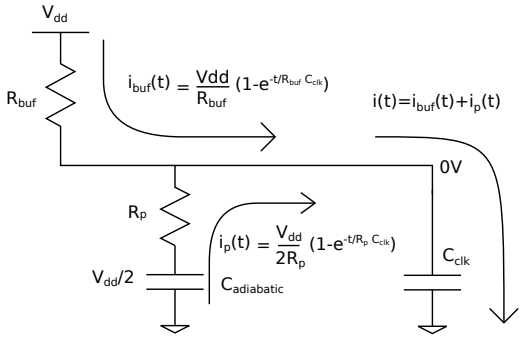


Fig. 6. While charging, during the $0 \rightarrow 0.5Vdd$ transition, the total current flowing to C_{clk} is the buffer current $i_{buf}(t)$. in addition to the current flowing from $C_{adiabatic}$ $i_p(t)$.

Now, the buffer and the passgate widths are obtained using R_{buf} and R_p respectively, with the help of the transistor ON resistance equation:

$$R_{on} = \frac{1}{\mu C_{ox}(W/L)(V_{GS} - V_{TH})} \quad (5)$$

where μ is the mobility, C_{ox} is the gate oxide capacitance per unit area, W/L is the aspect ratio, V_{GS} is the Gate-Source voltage and V_{TH} is the threshold voltage.

Sizing of $C_{adiabatic}$ is another important consideration. A bigger $C_{adiabatic}$ will save more power by avoiding a large voltage fluctuation. Based on our experiments, $C_{adiabatic}/C_{clk} = 10 \sim 100$, with varying efficiency, keeps the fluctuation minimal while reducing dynamic power without area overhead.

V. Experiments

A. Experimental Setup

Our simulations use an IBM 130nm technology and the ISPD2010 clock synthesis benchmarks in FreePDK 45nm for system-level analysis since we do not have benchmarks in the IBM technology. The supply voltages are 1.2V and 1V for the IBM and FreePDK technologies, respectively. The circuit simulations use operating frequencies of 1, 2 and 4 GHz while the system benchmarks are analyzed only at 1GHz.

B. Circuit Analysis

Figure 7 shows $C_{adiabatic}$ charging/discharging activity with respect to the output clock signal. $C_{adiabatic}$ discharges during the rising edge of the clock, until $C_{adiabatic}$ and C_{clk} have the same potential, then $C_{adiabatic}$ is disconnected. At the falling edge of the clock, $C_{adiabatic}$ charges from C_{clk} until they both have the same potential, then $C_{adiabatic}$ is disconnected. These simulations confirm at the fundamental level that our circuit recycles charge back and forth between C_{clk} and $C_{adiabatic}$. Experiments also show that our proposed quasi-adiabatic clock converges at steady state after 80nsec.

In IBM 130nm, we built a single buffer driving C_{clk} of 100fF at 2GHz frequency. We then added a passgate (8μm NMOS and 8μm PMOS) and $C_{adiabatic}$ of 100X (10pF). Simulation results show that the proposed clock circuit has less slew compared to a buffered clock with the same specifications.

TABLE I. USING THE SWITCHING CAPACITOR ADIABATIC CLOCK SHOWS A HIGH PERCENTAGE OF POWER SAVINGS BEFORE AND AFTER BUFFER REDUCTION. THE POWER CALCULATED IS THE TOTAL POWER CONSUMPTION INCLUDING THE PASSGATE SWITCHING POWER.

Frequency	Buffered Clock	QA[1] Clock	QA[2] Clock	QA[2] Saving
GHz	mW	mW	mW	%
1	0.241	0.197	0.182	24.8
2	0.482	0.396	0.371	23.2
4	1.290	1.150	1.060	18.0

QA[1] Clock: Total power consumption before buffer reduction.
QA[2] Clock: Total power consumption after buffer reduction.
QA[2] Saving: Percentage savings after buffer reduction.

TABLE II. ISPD2010 CLOCK SYNTHESIS BENCHMARKS IN FREEPDK 45NM FOR SYSTEM LEVEL ANALYSIS. ANALYSIS SHOWS AN AVERAGE OF 23% POWER SAVINGS WHEN USING THE SWITCHING CAPACITOR ADIABATIC CLOCK.

	Buffered Clock Network				Quasi-Adiabatic Clock Network		
	Sink	Cap	Chip Area	Pwr[1]	Pwr[2]	Skew	Pwr[2] Saving
	#	pF	mm^2	mW	mW	ps	%
03	1200	18.1	1.4	41.1	31.6	21	23.2
05	1016	5.2	5.8	47.8	36.5	12	23.7
06	981	12.6	1.5	33.2	23.2	16	30
08	1134	13.0	2.6	44	36.2	15	18
Avg.	1083	12.2	2.8	41.5	31.8	16	23.4

Pwr[1]: Buffered CDN power. Pwr[2]: Quasi-Adiabatic power in HSPICE.

Moreover the dynamic power consumption is reduced from $482\mu W$ (buffered clock) by 24% to $366\mu W$. The 24% saving uses the same buffer size of $6\mu m$ PMOS transistor and $3\mu m$ NMOS transistor. In order to duplicate the same signal performance (i.e., slew), the proposed clock buffer can be reduced to a $5\mu m$ PMOS and $2.8\mu m$ NMOS. This reduction in buffer size results in a dynamic power of $342\mu W$ which is almost 29% power savings. The total power consumption, including the passgate power consumption using ideal control signals, is shown in Table I for a range of frequencies. The dynamic power saving trend is consistent at nearly all frequencies. However, at higher frequencies the passgate control logic consumes more power, as power increases linearly with frequency, leading to an overall reduction in total power savings.

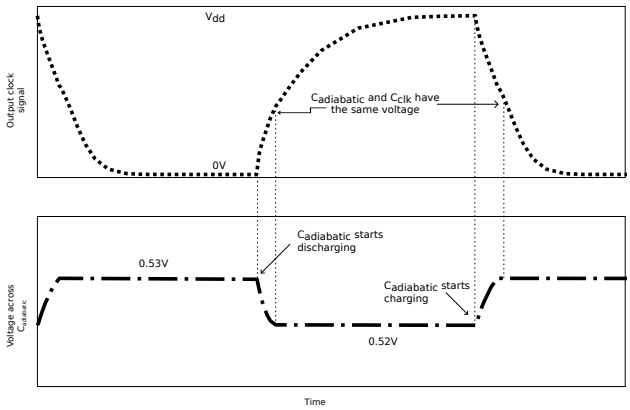


Fig. 7. Transient analysis shows the voltage across $C_{adiabatic}$ is discharging during the rising edge of the clock and charging during the falling edge of the clock, and in both cases it is disconnected when having the same potential.

C. Benchmark Analysis

In Table II, the results and simulations show the ability of the proposed adiabatic clock to reduce power consumption with an average of 23.4% in high-frequency systems at different chip sizes and different sink capacitances/placements. The high percentage of power savings is when using smaller benchmarks with higher capacitance per unit area. While using big benchmarks with small capacitance per unit area, the power savings drops to an average of 5% likely due to the interconnect parasitics decreasing the system efficiency.

VI. CONCLUSION

In this paper we presented the first quasi-adiabatic clock circuit with constant supply voltage at high speeds. Spice simulations and results show that using the proposed technique is a promising approach that can save on average 23% of clock power over a range of clock frequencies. In addition, the proposed circuit is easier to implement than existing adiabatic clock circuits, as our proposed circuit has a constant supply voltage, and can work at very high clock frequencies unlike previous adiabatic circuits.

Since the $C_{adiabatic}$ capacitors can be quite large, we plan to investigate integrated on-package capacitors, as they are of high density with small sizes. With the help of the proposed pulse generator, a complete clock design is ready for fabrication to be used at the system level.

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