Hybrid Silicon Photonic Integrated Circuit Technology

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(Invited Paper)

***Abstract*—In this paper, we review the current status of the hybrid silicon photonic integration platform with emphasis on its prospects for increased integration complexity. The hybrid silicon platform is maturing fast as increasingly complex circuits are reported with tens of integrated components including on-chip lasers. It is shown that this platform is well positioned and holds great potential to address future needs for medium-scale photonic integrated circuits.**

***Index Terms*—Hybrid silicon platform, integrated optoelectronics, optoelectronic devices, semiconductor lasers, silicon-on-insulator (SOI) technology, silicon photonics.**

I. Introduction

THE prospect of medium- and large-scale integration is a major driver for research on silicon photonics in the silicon-on-insulator (SOI) platform. The SOI fabrication infrastructure is compatible with CMOS technology and hence is highly accurate and mature, leading to a robust, high yield and reproducible technology and hence performance. Photonic integrated circuits (PICs) in the SOI platform can be and have been made on large 200-mm diameter wafers and this allows for low cost and high volumes. SOI-based PICs operate in the telecommunication windows around wavelengths of 1.3 and 1.55 μm, so prime application candidates are telecommunication and interconnects [1].

The SOI platform offers an almost complete suite of photonic components, including filters, (de)multiplexers, splitters, modulators, and photodetectors (PDs) [2]. Silicon modulators generally make use of the free-carrier plasma dispersion effect. Mach–Zehnder interferometric (MZI) and ring-based modulators have been reported [3]–[5]. Under forward bias, speeds of 18 Gb/s using pre-emphasis have been obtained [6], [7]. Under reverse bias, bandwidths up to 30 GHz were shown [8]–[10]. Strained germanium and silicon germanium are also compatible with the CMOS fabrication technology, and these materials further increase the possibilities. Since their bandgap can be pushed into the 1.55-μm wavelength regime, these materials enable electroabsorption modulators (EAMs) and PDs [11], [12]. By using band engineering, germanium can also be used as a laser gain medium. First results have been obtained with germanium-on-silicon lasers, but the efficiency is still too low to be of practical interest [13]. Electrically pumped efficient sources on silicon remain a challenge and an overview of the numerous efforts is presented in [14].

Heterogeneous integration of III/V materials such as indium phosphide (InP) gives the SOI platform access to the complete suite of high-speed and efficient III/V-based photonic components. These InP-based components include electrorefractive modulators that operate in the 40–80 Gb/s range at efficiencies of around 1 V·mm [15]–[17] and EAMs with bit rates well above 100 Gb/s [18], [19]. III/V PDs have shown operation bandwidths into the hundreds of gigahertz regime [20]. Laser diodes and semiconductor optical amplifiers (SOAs) finally have been widely available in various III/V material systems and have been the first choice for efficient and low-cost systems where single-mode or tunable sources are required.

The hybrid silicon platform heterogeneously integrates III/V functionality on the SOI platform by means of molecular wafer bonding [21]. Hybrid silicon III/V waveguides have the functionality of the III/V epitaxial layer, e.g., gain, high-speed modulation, or photodetection, but are still located on an SOI wafer. The active III/V components can be fabricated with lithographic precision and alignment accuracy, thereby enabling large-scale integration. This is done in a back-end process after the SOI fabrication at temperatures of 350 °C maximum. This means that contamination of a CMOS foundry is avoided and the III/V fabrication process is in principle fully compatible with the SOI CMOS fabrication process. The hybrid silicon platform combines the maturity and scale of CMOS processing and SOI photonics with essential III/V functionality and as such is unique and well positioned for medium-scale photonic integration, with tens to hundreds of integrated components.

The rationale for photonic integration is manifold. Integration offers a reduction in size, weight, and power consumption (SWaP), increases yield and reliability, and allows for

Manuscript received November 2, 2012; revised December 14, 2012; accepted December 14, 2012. Date of publication December 19, 2012; date of current version May 13, 2013. This work was supported in part by DARPA MTO (S. Raman, S. Rodgers, J. Shah, and J. Conway), in part by Intel, and in part by Hewlett Packard.

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Digital Object Identifier 10.1109/JSTQE.2012.2235413

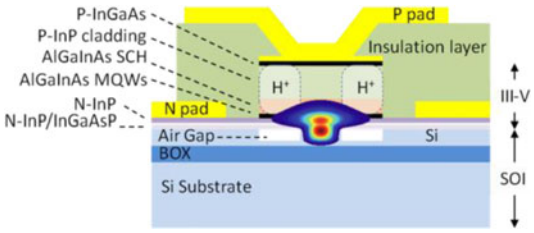

Fig. 1. (a) Cross section of the hybrid Si device.

large volume manufacturing at low cost. Packaging costs are reduced since optical and electrical interfaces are minimized. Telecommunications and interconnects are clear drivers for photonic integration for reasons of bandwidth and energy-efficient operation [22]. Photonic technologies have all but replaced electronics in the longer link lengths and are key enablers for future exascale datacenters. But photonic integration is also making an impact or has this potential in other fields. Ubiquitous sensor networks, point-of-care medical diagnostics, turn-key and compact instrumentation, spectroscopy and (biomedical) imaging solutions, and high-accuracy metrology will all benefit from photonic integration [23]–[25].

In this paper, we review the current status of the hybrid silicon platform. We focus on the potential for medium-scale integration and show that this platform is suitable and on track to meet current and future demands for medium-scale photonic integration. In Section II, we give an overview of the fabrication technology that enables heterogeneous integration of the required suite of components, such as passive and active silicon and hybrid silicon III/V components. In Section III, we review a set of basic components, such as lasers, SOAs, isolators, and passive components. These components are the building blocks for more complex and functional PICs. In Section IV, we show the current status of fully integrated PICs by reviewing a set of examples. We conclude this paper in Section V with a discussion on the current position of the hybrid silicon platform and the prospects for the future.

II. Technology Platform

The integration of active III/V-based components with silicon photonics on a silicon substrate requires an approach that accommodates the large mismatch in lattice constants and thermal expansion coefficients. Low-temperature wafer bonding techniques are a promising approach to overcome these issues [26], [27]. The hybrid silicon platform we developed makes use of covalent wafer bonding. Alternative approaches based on adhesive bonding [28] and bonding after silica planarization [29] show equally promising results. In these approaches, the additional thermal bottleneck can be circumvented by minimizing the thickness of the layer separating the III/V and the silicon. Techniques that make use of the epitaxial growth of III/V on silicon are an interesting option, but the required thick buffer layers are still a bottleneck for further integration [30].

A schematic of the hybrid waveguide cross section is shown in Fig. 1. The optical mode is laterally confined by the silicon waveguide and couples evanescently to the III/V slab. By decreasing the waveguide width, the mode is pushed up and the confinement within the active layer increases. For example, high-gain elements can be designed by decreasing the silicon waveguide width. High-saturation power gain elements on the other hand can be designed by increasing the waveguide width. This is a unique feature of the hybrid silicon platform as presented here. Further design and fabrication details can be found in [31] and [32]. Alternative hybrid waveguide designs can be found, e.g., in [33], where the optical mode almost fully resides in the III/V section. In this design, the mode and injection current are both guided by the relatively narrow p-InP mesa, thereby decreasing the threshold current. The hybrid waveguide designs presented here can in principle be as efficient as any monolithic single-mode InP-based laser diode, having topside n-contacts, if the buried-oxide thermal bottleneck can be minimized, as discussed later.

The optical properties of the hybrid waveguide depend on the bandgap of the III/V active region. SOAs and lasers can be made for both telecom bands centered around 1300 and 1550 nm using InP-based material. Both AlGaInAs- and InGaAsP-based quantum wells (QWs) have been considered [34]. By careful tuning of the bandgap, EAMs, phase modulators (PHMs), and passive waveguides can be made in this way. High-speed and high-responsivity PDs can be made using a bulk active layer.

Complex hybrid silicon PICs, however, will require any combination of such functionalities on a single silicon chip. A minimum required set would consist of sources (lasers or LEDs), SOAs, PHMs, PDs, and passive waveguide circuitry. EAMs can in principle be replaced by Mach–Zehnder modulators based on PHMs. There are several approaches available for the hybrid silicon platform, which can combine III/V photonics with silicon photonics. In the following, we discuss four approaches that were pursued to successfully integrate a combination of functionalities. First, we discuss tapered mode converters that allow for the combination of a hybrid waveguide with passive silicon waveguides and components. Second, we discuss briefly the possibilities of combining active silicon with hybrid silicon. Third, we discuss quantum-well intermixing (QWI) techniques that allow for the combination of multiple bandgaps in the hybrid section. And as a final technique, we briefly review the work on selective die bonding, where dies from different epitaxial wafers are bonded to the silicon wafer, for maximum flexibility and performance.

A. *Tapered Mode Converters—Integration With Passive SOI*

To integrate hybrid silicon components with passive SOI components, the optical mode as shown in Fig. 1 should be converted to a mode that resides solely in the SOI waveguide. Tapered mode converters can be used to adiabatically transform the mode, i.e., without exciting higher order transverse modes. These have been successfully implemented in various designs to combine, e.g., SOAs with arrayed waveguide grating multiplexers (AWGs) [35], [36]. It is not trivial though to evaluate taper performance, since part of the transition loss will be due to mode mismatch and radiation losses and part of the performance will depend on the electrical pumping, since it is part of an active section.

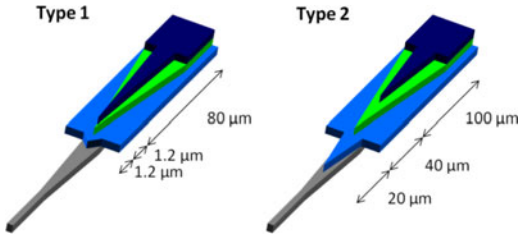

Fig. 2. Type 1 and Type 2 tapers showing the silicon waveguide (gray), n-InP (light blue), SCH layer containing QWs (green), and p-InP top cladding (dark blue). Taper start offsets are indicated.

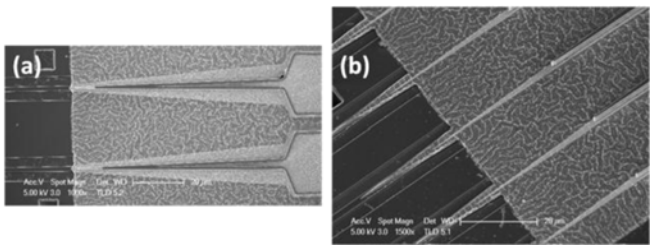

Fig. 3. SEM pictures of (a) Type 1 and (b) Type 2 tapers.

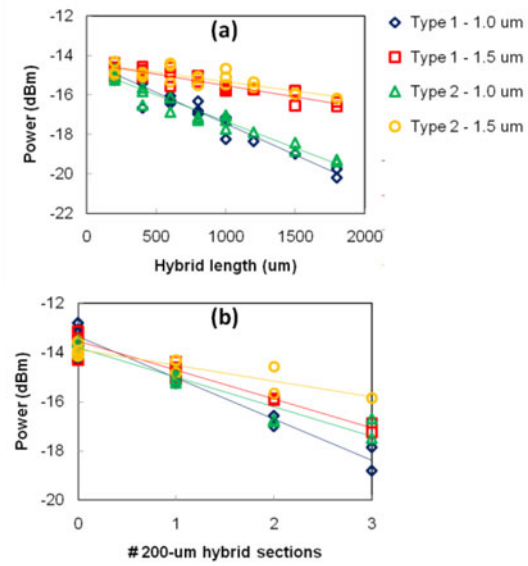

Fig. 4. Measured in-fiber output power after propagation through structures with (a) various hybrid waveguide lengths and (b) various number of 200-μm hybrid sections. Configurations are indicated as Type 1, 1.0 μm (blue diamonds); Type 1, 1.5 μm (red squares); Type 2, 1.0 μm (green triangles); Type 2, 1.5 μm (yellow circles).

To investigate taper performance in more detail, tapers were fabricated where the bandgap of the QWs was shifted to 1.40 μm, i.e., well below the wavelength of 1.55 μm used for characterization. By doing this, QW absorption and the need for electrical pumping were eliminated. Two taper designs were studied, each fabricated using three etch levels, as shown in Fig. 2. In Type 1 tapers, the silicon waveguide is tapered out to 2 μm where the III/V taper starts. Tapering of the p-InP layer starts almost immediately after the start of the other two taper levels, allowing a 1.2-μm margin of the n-InP and SCH levels for fabrication tolerance purposes. The designed taper tip width is 0.5 μm, as limited by lithographic resolution. This taper has been used in [35]. In [36], a Type 2 taper was used, where the mode is more gradually converted from the silicon mode to the hybrid mode. To vary the overlap of the hybrid mode with the QWs, two different widths of silicon waveguide in the hybrid section were used, namely 1.0 and 1.5 μm. This is realized by tapering the silicon width from 2.0 μm down over the length of the III/V taper. More details about the designs can be found in [37] and [38]. Fig. 3 shows top-view SEM pictures of the realized tapers.

Taper losses and mesa propagation losses are then extracted by measuring propagation losses through devices with varying lengths and repeats. In Fig. 4(a), the transmitted power as a function of hybrid device length is plotted. A linear fit through the data gives the hybrid waveguide loss. The offset in Fig. 4(a) and the slope in Fig. 4(b) give the taper losses. The tapers show losses of 0.5 and 0.3 dB per taper transition for the two taper designs presented. These losses are significantly lower than the 1–2 dB coupling loss values that are generally obtained in other hybrid integration approaches [39], showing the clear advantage of this integration approach. Taper reflections on taper Types 1 and 2 were measured to be below −41 dB in both cases.

When the taper is part of an SOA, as is the case in [35] and [36], the QWs inside the taper will have a bandgap with lower energy than the wavelengths of interest. An open question remains as to what extent electrical pumping of the taper can decrease coupling losses. The relatively narrow taper widths will lead to increased sidewall surface recombination, thereby decreasing the gain [40]. This would lead to additional absorption, which can be wavelength dependent. This subject remains under investigation.

B. *Integration of Hybrid Silicon With Active SOI*

Although III/V-based PHMs and PDs generally have superior performance over silicon- and germanium-based equivalents in terms of speed, there can be huge value in making use of the far more mature silicon CMOS-based fabrication infrastructure [41]. This is obviously the case for PICs where medium-scale integration is required. With the standardization and maturity of silicon photonics, it is an attractive option to combine hybrid silicon SOAs or lasers with active SOI components. This has been successfully realized [42], [43]. In this section, we review briefly some process considerations that were taken into account in the work in [42].

First of all, the process flow needs to be designed in such a way that the thermal budgets of all the steps are compatible. Silicon diodes to be used as PHMs were realized by ion implantation of phosphorus and boron. The doping has to be activated by a high-temperature anneal $> 900\ ^{\circ}$C, which is not compatible with III/V epitaxial material. So this anneal has to be done before wafer bonding.

Since the effect of ion implant on the silicon surface with respect to III/V wafer bonding was not known, implantation and contact formation were done in the etched slab next to the

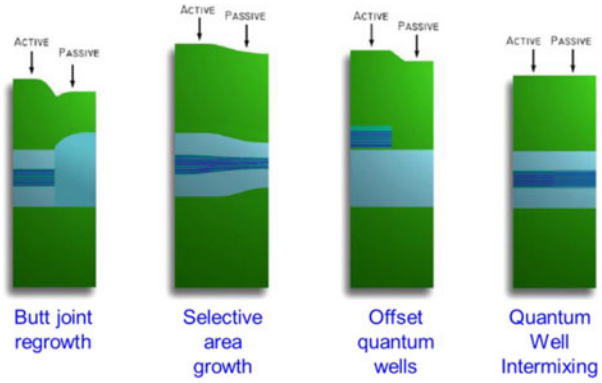

Fig. 5. Overview of different monolithic integration approaches [45].

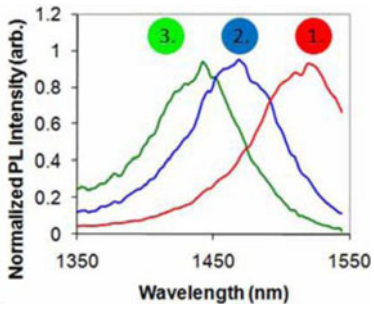

Fig. 6. Normalized PL spectra from the three bandgaps utilized in the work in [46].

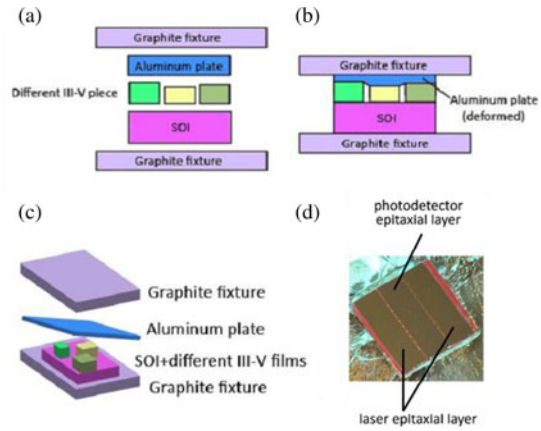

Fig. 7. (a)–(c) Selective area wafer bonding diagram. (d) Selective area wafer bonding results: two laser and one PD III/V films integrated on an SOI chip after substrate removal [50].

waveguide only. This means that implantation was only done on recesses in the top surface of the SOI wafer. Any additional roughness that the implantation might cause would thus not be detrimental for wafer bonding. Another way to mitigate this risk is to use selective area die bonding, as explained in [44]. In this approach, the III/V die is only bonded over the areas where SOAs and lasers are designed to be and not over the areas where, e.g., silicon PHMs are designed to be. Care was taken to protect the uncovered area during III/V processing, as explained in [44].

The approach of selective area bonding also allows for defining the silicon metal contacts before III/V bonding. This is especially important as the wafer can stay inside a silicon fab for all the silicon processing and the full III/V process flow can be added as a backend process.

C. QW Intermixing

Various techniques have been developed for InP-based monolithic integration of components that require different bandgaps, e.g., a laser integrated with an EAM. These techniques include butt-joint regrowth, selective area growth, and offset QWs [45]. Fig. 5 shows an overview of these techniques. It can be seen in this schematic that these techniques do not result in a flat wafer surface. This is prohibitive for wafer bonding. QWI on the other hand results in a flat top surface and wafer bonding to an SOI wafer is possible. With QWI a high-temperature anneal drives atomic interdiffusion across the well-barrier interface. The resulting change in concentration profile modifies the potential profile and hence the bandgap.

In [46], a QWI process was reported based on such implant enhanced intermixing in combination with selective removal of an InP buffer [47]. By selectively masking and implanting the QWs, three different bandgaps are created in the wafer. Fig. 6 shows photoluminescence (PL) spectra from the three bandgaps in this study, showing the feasibility of integration of, e.g., SOA, EAM (50 nm blue-shift), and PHM (80 nm blue-shift) components. In [48], a similar approach has been chosen for InGaAsP-based epitaxial material operating at wavelengths around 1.3 μm. Four bandgaps spread over 60 nm were generated across a single chip. Recent results have extended this range to over 100 nm [49].

The QWI is done before wafer bonding takes place, since the high-temperature anneals of around 700 °C would degrade the bonded interface. Bonding of the QWI III/V die to a patterned SOI wafer is then done with controlled alignment and devices can be fabricated as explained previously. The clear advantage of QWI is that different-bandgap components can be combined on a silicon wafer without the need for mode converters that can add losses to the circuit. The mode stays in the hybrid waveguide when, e.g., a laser and a modulator are combined.

D. Selective Die Bonding

Selective die bonding techniques give maximum flexibility as they do not only allow for the combination of different-bandgap hybrid waveguides, but also allow for a combination of components with completely different epitaxial layer stacks. This technique was successfully used to make a fully integrated hybrid silicon triplexer [50], where a 1310-nm laser and 1490 nm/1550 nm PDs were integrated on a single hybrid silicon chip.

The bonding process makes use of a thin and compressible aluminum foil in the bonding fixture to compensate for the thickness differences (typically tens of microns) between the different III/V dies. Fig. 7 shows an overview of the bonding process. Fig. 7(d) shows the successful bonding of two laser and one PD III/V dies onto a 1-cm^2 SOI chip. Ideally, the process flow of PDs and lasers is compatible with identical

parameters, such as etch depths, to minimize the total number of fabrication steps. Also during processing, protection of the uncovered SOI circuitry between the bonded III/V dies has to be taken into account [44]. The major drawback of this approach is that the combination of components requires mode conversion to the passive interconnecting silicon waveguide. This adds two (tapered) mode converters per transition and hence increases the link losses.

E. Summary

In the previous discussion, we have shown that medium-scale integration is in principle possible in the hybrid silicon platform. The combination of active and passive SOI components is enabled by tapered mode converters. The combination of different-bandgap components is enabled by QWI. And finally, the combination of components that require a different epitaxial layer stack is enabled by selective die bonding and with the help of interconnecting silicon waveguides. These techniques have all been successfully implemented to realize a large variety of hybrid silicon chips.

III. Hybrid Silicon Platform Building Blocks

Since the first report of the electrically pumped hybrid silicon laser [31], a full suite of hybrid silicon III/V components has been developed. For an overview, we refer to the work in [1], [32], and [51]. In the following, we report the most recent results on components that are made in the platform as described in Section II. Since these components have similar fabrication technologies, they can in principle be used to build larger-scale PICs. As such, these results are indicative for the near-future possibilities for hybrid silicon PICs.

The results reviewed here include the recent work on sources, amplifiers, and modulators. We also review results on platform compatible polarization components and optical isolators. Finally, we show that with a novel integration approach, silica-based components can be made compatible with the hybrid silicon platform.

A. Sources

On-chip sources need to be efficient, emit the optical power and wavelength required for the application, and ideally can operate uncooled in elevated-temperature environments, e.g., close to or on a CPU processor. Eliminating thermoelectric coolers significantly increases wall-plug efficiency. All-hybrid lasers have shown operation at temperatures up to 105 °C [52] and with output powers up to 45 mW [53]. Improved thermal impedance can be achieved by thermal shunts [54] and/or by silicon-on-diamond substrates [55]. Also, flip-chip bonding techniques can be considered.

1) DFB Lasers: Quarter-wavelength-shifted hybrid silicon DFB lasers operating at a single frequency with over 50 dB side-mode suppression ratio (SMSR) and a linewidth of 3.6 MHz were reported in [56]. However, the high intensity concentrated at the phase-shifted region of the cavity limits its performance because of spatial hole burning. To avoid this problem, DFBs

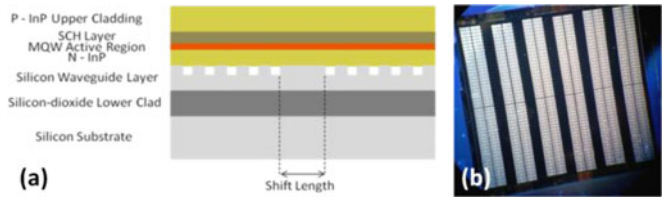

Fig. 8. (a) Symmetric phase-shifted DFB laser. (b) Hybrid silicon chip showing 300 DFB lasers with on-chip photodetectors.

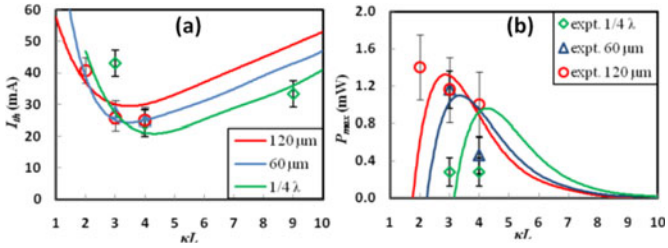

Fig. 9. (a) Threshold current and (b) maximum output power plotted against κL ($\kappa = 250\ \text{cm}^{-1}$) for three phase-shift lengths, one quarter wavelength (green line and diamonds), 60 μm (blue line and triangles), and 120 μm (red line and circles).

with longer phase shift lengths, i.e., 60 and 120 μm, were realized [57]. A schematic is shown in Fig. 8. The grating length L was also varied and hence the grating reflectivity as expressed by the κL product, where κ is the grating strength or coupling constant, i.e., the reflection per unit length.

Fig. 9 shows the theoretical and experimental values of threshold current and maximum output power versus κL. The threshold decreases to a minimum value and then grows with reducing total device length. Similarly, the output power increases at the optimum value and then falls off. These results indicate that higher power extraction and differential quantum efficiency can be achieved by having large phase-shift lengths and lower κL products. The SMSR in all these lasers was better than 40 dB. However, devices with increased phase shift length are more prone to mode hopping. The thermal impedance decreased for the longer phase shift lengths. Simulations using realistic parameters [58] show that sub-1 mA threshold currents at reasonable output power levels of $\sim$0.1 mW can be achieved when these lasers are reduced in length to about 10-μm length. This goes up to 1 mW at 3 mA injection current. High reflectivities can be obtained by using grating mirrors or ring or disk configurations. Critical design parameters are the minimization of free-carrier losses and diode electrical resistance, and the optimization of injection efficiency and confinement factor.

The question is then whether these hybrid silicon III/V lasers can have similar reliability as their III/V counterparts. A reliability study was done [59] using these quarter-wave-shifted DFB lasers. The effect of the superlattice between the III/V diode structure and the bonded interface was investigated. The superlattice blocks defects originating from the bonded interface from migrating to the QWs. These defects would create carrier recombination centers in the QWs, which in turn would degrade laser performance. Devices containing an unstrained and strained (-1% well, 1% barrier) superlattice were

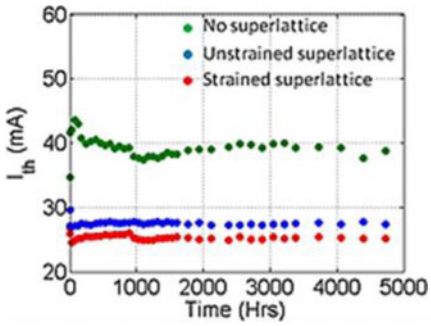

Fig. 10. Accelerated aging at 70 °C and 100 mA of three hybrid laser structures: no superlattice (green), strained superlattice (red), and unstrained superlattice (blue).

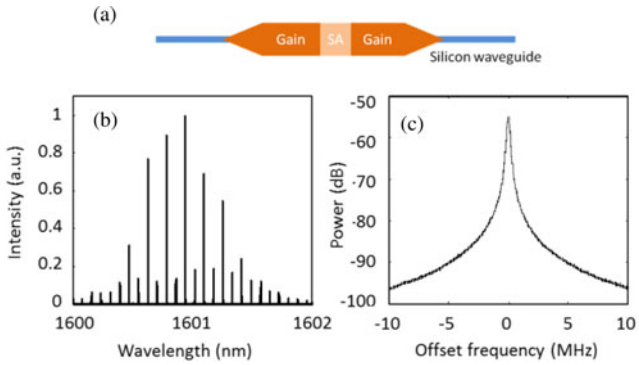

Fig. 11. (a) Top-view schematic of the device layout. (b) Optical spectrum obtained using a 20-MHz resolution high-resolution optical spectrum analyzer. (c) Electrical spectrum centered at 18.32 GHz. Resolution bandwidth is 20 kHz.

compared to control devices without a superlattice. Fig. 10 shows a typical aging result. The diodes with a superlattice showed no significant degradation in threshold current after 5000 h of aging even at 70 °C. On a couple of devices that showed degradation, a sublinear fit was used, and a degradation of 50% in threshold current at 70 °C is estimated to take ∼40 000 h. No significant difference between devices with and without strain in the superlattice was observed.

2) Extended-Cavity Hybrid Silicon Colliding-Pulse Mode-Locked Laser: Mode-locked lasers (MLLs) can be used as on-chip pulse or (WDM) comb sources. As such they complement single-wavelength DFB lasers in functionality. Extended-cavity designs, i.e., configurations where part of the lasing cavity is passive, have advantages over all active cavities in terms of low-noise performance and further integration on a PIC. An extended-cavity hybrid silicon MLL was reported in [60]. The design is a colliding-pulse MLL, which avoids having to place the saturable absorber (SA) at a facet or DFB mirror, as shown in Fig. 11. In this realization, the diced and polished silicon facets act as the laser mirrors.

The lasing spectrum in Fig. 11(b) shows colliding pulse operation. For this operating point, the single-sided output power is around 1 mW. The lasing modes are spaced at 18.32 GHz, which is twice the fundamental cavity roundtrip frequency. Analysis of the radio-frequency spectrum shows a 250-kHz 3-dB width of the 18.32 GHz peak. The fundamental frequency of the cavity at 9.16 GHz is suppressed to 30 dB below the second harmonic. No

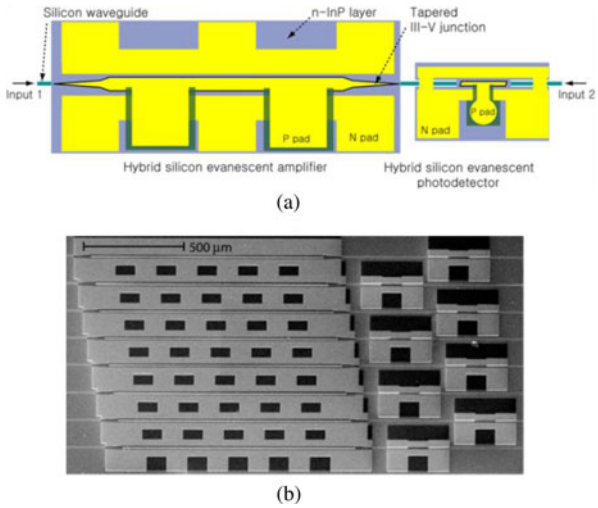

Fig. 12. (a) Top view of a hybrid silicon evanescent preamplified receiver. (b) SEM picture of eight integrated devices with amplifiers [61].

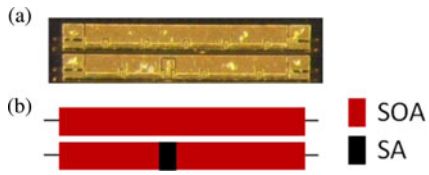

Fig. 13. (a) Optical micrograph image of the SOA and SOA with integrated SA. (b) Schematic diagram of the fabricated device.

direct evidence of reflection due to the tapers is observed. This approach will allow further integration of MLLs with passive silicon photonic devices, e.g., by using grating-based mirrors.

B. Optical Amplifiers

1) Hybrid Silicon SOA: An integrated SOA depends strongly on low-loss and low-reflection mode converters, as discussed previously. Reports on hybrid silicon SOAs have not been as extensive as the work on lasers. In [61], an SOA is used as a preamplifier, as shown in Fig. 12. The transition between the passive silicon waveguide and the hybrid waveguide of the amplifier is formed by tapers. For a 1.2-mm-long structure, the maximum gain is 9.5 dB at 300 mA. More recent work shows a significant improvement in SOA gain. A peak gain of 19 dB/mm at a wavelength of 1560 nm is observed at an injection current density of 5 kA/cm^2 [44].

2) Hybrid Silicon 2R Regenerator: As the serial integration of components in PICs increases, integrated optical regenerators become increasingly important. One interesting approach is a 2R regenerator based on an SOA in series with an SA. A concatenated array can be considered for improved performance [62]. The concept is based on the fact that the signal ("1") can saturate the SA while the noise in the "0" level will be absorbed by the SA. In the work in [63], an SA was formed by proton implant of the QWs with a dose of $\sim 10^{14}$ cm^{-2}. A picture and schematic of the device are shown in Fig. 13. It consists of a 1-mm-long hybrid SOA containing a 20-μm-long implanted SA section and

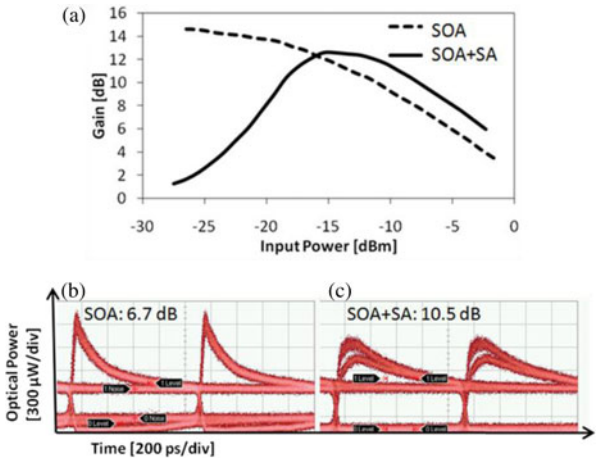

Fig. 14. (a) Transfer curves of the SOA (injected current 90 mA) and SOA with integrated SA (injected current 140 mA). (b) Eye diagram of the SOA output signal (injected current 100 mA). An extinction ratio of 6.7 dB is measured. (c) Eye diagram of the SOA with integrated SA (injected current 100 mA). The extinction ratio increased to 10.5 dB.

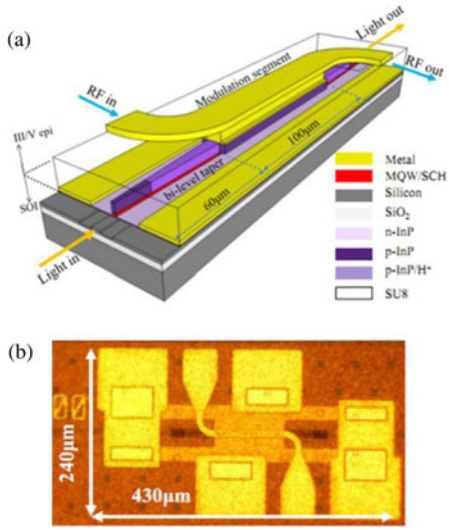

Fig. 15. (a) Schematic structure of a hybrid silicon TW-EAM. (b) Top-view photograph of a fabricated TW-EAM.

passive silicon input and output waveguides, which shows the promise for further integration.

The transfer curve of the 2R regenerator is shown in Fig. 14(a) with a 1-mm-long SOA curve for reference. As can be seen, the 2R regenerator should be able to suppress noise at the "0" level for signal input powers around −15 dBm. Eye diagrams for a 1 Gb/s predistorted input signal are shown in Fig. 14(b). A 3–4 dB improvement of the output extinction ratio was observed.

C. *High-Speed Electroabsorption Modulators*

High-speed modulators are key enablers for high-bandwidth interconnects and microwave photonics. In the following, we describe three realizations in more detail. In [64], an EAM with a traveling-wave (TW) electrode design operating at 1.55-μm wavelength was reported. The TW electrode design overcomes the RC-limit due to a distributed circuit configuration, as shown in the schematic in Fig. 15(a). This device has a compact footprint of 240 μm × 430 μm. The TW-EAM optical insertion loss is 5 dB. For wavelengths around 1550 nm, over 11 dB extinction ratio is achieved for a voltage change from −2 V to −4 V. A 3 dB bandwidth of 42 GHz was obtained, using a bias voltage of −3 V. Large-signal performance was evaluated using an NRZ-PRBS signal with a 2 V swing on the TW-EAM under a −3 V bias. As shown in Fig. 16, a clear open eye was observed at 50 Gb/s with a dynamic extinction ratio of 9.8 dB, which is sufficient for practical applications.

A distributed EAM based on an asymmetric segmented electrode was reported in [65] for wavelengths around 1.3 μm. The measured modulation response shows an (extrapolated) 3 dB bandwidth of 74 GHz, as can be seen in Fig. 17. Large-signal measurements showed open eye diagrams at 50 Gb/s. An extinction ratio of 9.6 dB for back-to-back transmission and an extinction ratio of 9.4 dB after 16 km transmission were obtained with a drive voltage of 2.2 V.

To achieve low-energy consumption, lumped modulators with high input impedances are preferable. Ideally, such modulators

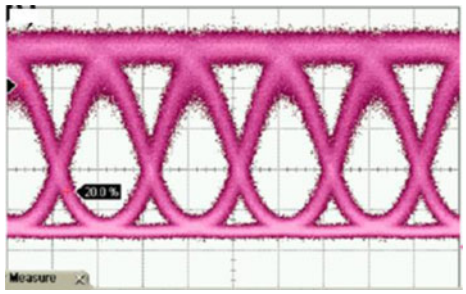

Fig. 16. 50 Gb/s NRZ eye diagram at $\lambda = 1550$ nm with $2^{31}-1$ PRBS pattern for a 100-μm-long hybrid silicon TW-EAM. The modulator was biased at –3 V with a driving voltage swing of only 2 V.

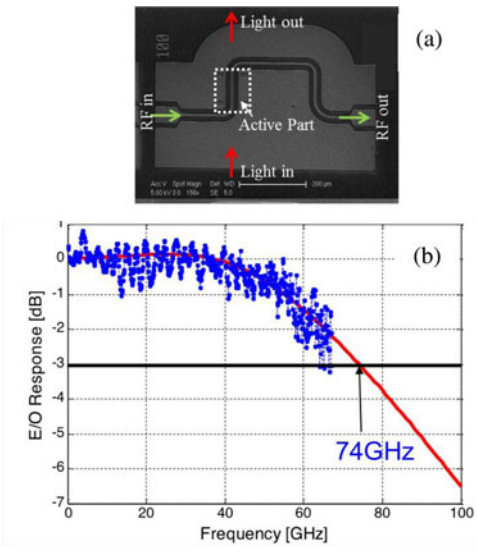

Fig. 17. (a) SEM picture of the realized distributed EAM. (b) Measured (blue) and calculated (red) modulation response [65].

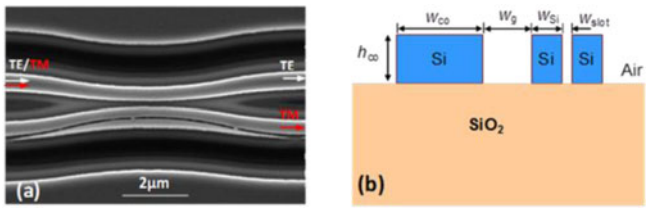

Fig. 18. PBS based on an asymmetrical coupler consisting of an SOI-nanowire and a nanoslot waveguide: (a) SEM picture; (b) cross section of the waveguides in the coupling region. The parameters are $w_{co} = 0.4\ \mu$m, $w_S i = 0.26\ \mu$m, $h_c o = 250$ nm, $w_{\rm slot} = 60$ nm, and $w_g = 100$ nm.

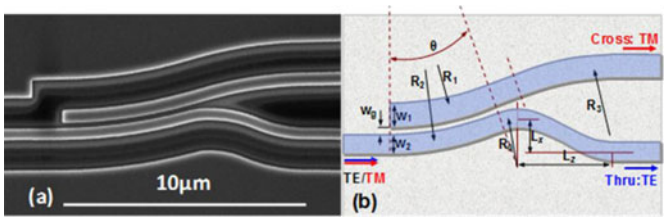

Fig. 19. Ultrashort PBS based on a bent DC: (a) SEM picture and (b) schematic configuration. The parameters are as follows: $L_{\rm dc} = 4.5\ \mu$m, $R_1 = 19.3\ \mu$m, $R_2 = 20.0\ \mu$m, $w_1 = 0.534\ \mu$m, $w_2 = 0.46\ \mu$m, and $w_g = 203$ nm.

have sub-1 V drive voltages and can be driven directly by the logical output of advanced CMOS drivers. Also for applications in high-temperature environments, uncooled operation is important to avoid energy-consuming thermoelectric cooling. In [66], a lumped hybrid silicon EAM was reported with a bandwidth of 30 GHz and 1 V operation. Uncooled operation up to 80 °C was shown at bitrates of 40 Gb/s and with an energy consumption of 112 fJ/bit.

D. Polarization Handling Components

Polarization multiplexing is an attractive way of doubling the capacity of a fiber-based network. For PICs to make use of this approach, on-chip polarization handling is required. But even when the polarization state of the signal is not used in this way, polarization handling can be used to make polarization-transparent PICs by using a polarization-diversity scheme. Recent work on silicon-based polarization components can bring this functionality to the hybrid silicon platform. This study includes polarization beam splitters (PBSs), polarization rotators (PRs), and polarization splitter–rotators (PSRs).

1) Polarization Beam Splitter: PBSs based on an asymmetrical coupling system were reported in [67], which allow for ultracompact, 6.9-μm-long, footprint and broad-band operation of over 160 nm. The asymmetrical coupling system consists of an SOI-nanowire and a nanoslot waveguide, as shown in Fig. 18. The S-bend section allows for a compact mode converter from the nanowire to the slot waveguide. TM polarization couples to the cross waveguide while TE polarization remains in the input waveguide. The extinction ratio is simulated to be over 10 dB.

An even more compact PBS was reported in [68], using a bent coupler, as shown in Fig. 19. Apart from decoupling the two bent waveguides, the S-bend also functions as a TE-pass polarization filter by using a small radius R_0 (see Fig. 19). This

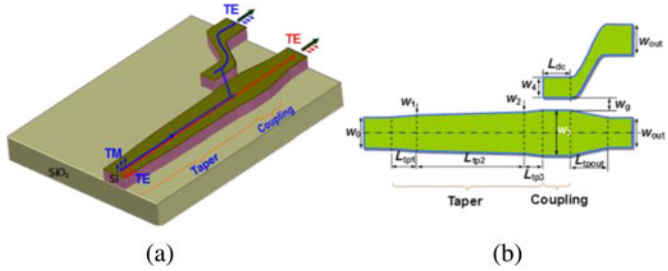

Fig. 20. PSR consisting of a taper and an asymmetrical directional coupler: (a) 3-D schematic and (b) top view.

device has a simulated extinction ratio of >10 dB over a broad, 200 nm wavelength range. The design is compact and has large fabrication tolerances of over 60 nm of the width.

2) Polarization Splitter–Rotator: PRs are key components for polarization diversity transmitters and receivers. However, fully integrated PRs are difficult to realize since planar waveguides are generally polarization maintaining. A compact silicon PR with a cut corner was proposed in [69]. This design uses a two-etch-step process. A simpler design using one etch step only was proposed in [70]. This design splits and rotates the polarization simultaneously, as shown in Fig. 20. It consists of an adiabatic taper and an asymmetrical directional coupler, with a total length of less than 100 μm. The adiabatic taper converts the fundamental TM mode to the first higher order TE mode, with an efficiency of close to 100%, using the mode hybridization in the SOI nanowire with air or silicon-nitride upper cladding [71]. The cascaded asymmetrical coupler then couples the first higher order TE mode to the fundamental TE mode in the adjacent waveguide. No mode conversion or coupling takes place for input fundamental TE light.

In summary, these results show that polarization handling on-chip is possible with these silicon-based PBSs, PRs, and PSRs. Their design is simple, their footprint is small, and the fabrication technology is compatible with the process outlined previously, which makes these components promising candidates for adding polarization management to the hybrid silicon platform.

E. Silicon Ring Isolators With Bonded Magneto-Optic Garnets

Integrated optical isolators are becoming increasingly important when larger scale serial integration is required. Reflections and spontaneous emission noise that can be generated further downstream in a circuit can destabilize a laser source. In applications like optical buffers, the unwanted counterpropagating field can be amplified to significant power levels and hence decrease optical gain and signal-to-noise ratio [89]. Integrated isolator concepts that have been reported make use of a magneto-optic material to create a nonreciprocal effect, for example in an MZI configuration [72]. Other options include a gated array of modulators, timed either by a phased drive signal or by self-saturation [73].

Practical ring-based isolators making use of the magneto-optic effect were proposed and realized in [74] and [75]. The isolator of [74] consists of a silicon ring resonator coupled to a

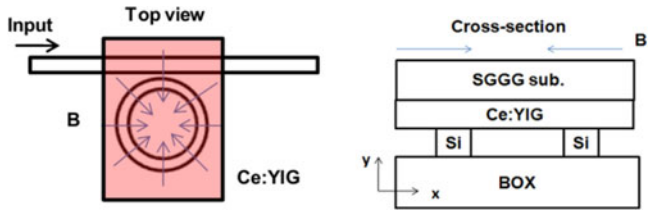

Fig. 21. Schematic of a ring isolator consisting of a ring resonator, a straight waveguide, and a bonded Ce:YIG layer as magneto-optic material: (a) top view and (b) cross section.

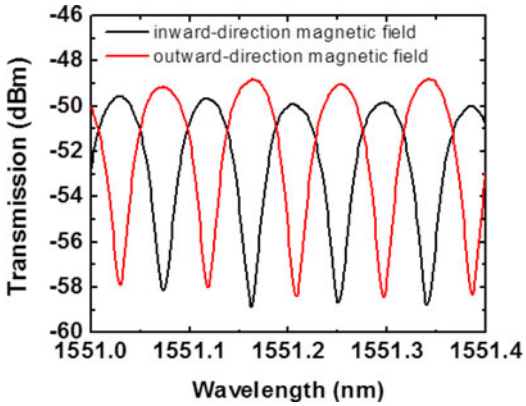

Fig. 22. Transmission spectra of the ring isolator with external radial magnetic fields in two different directions: inward (black) and outward (red) directed.

bus waveguide and a bonded magneto-optic cerium-substituted yttrium iron (Ce:YIG) garnet, which has relatively low optical loss in the 1500-nm wavelength regime. A schematic is shown in Fig. 21. An externally applied radial magnetic field breaks the ring symmetry and the passbands for clockwise and counterclockwise propagating TM fields shift in opposite directions, as shown in Fig. 22. When the signal is at an off-resonance wavelength and the counterpropagating reflection is at resonance, the device effectively works as an optical isolator for narrowband signals. An isolation ratio of 9 dB was experimentally obtained. Simulations of such isolators were presented in [76] and show the possibility of obtaining 20 dB isolation in a robust design. The magnetic garnet is bonded to the SOI ring by a low-temperature oxygen plasma-assisted technique [27]. This approach makes this isolator in principle compatible with the hybrid silicon platform.

Further integration will require polarization managing components, such as PRs as described previously, since on-chip lasers and SOAs tend operate with TE polarized light. Alternatively by growing Ce:YIG on the ring inner sidewall, a TE isolator can be made [77]. Another interesting application is to use the ring isolator as a circulator, by adding a second bus waveguide [78].

F. Ultralow Loss Waveguides and Components

Silicon photonics based on the SOI platform has some fundamental performance limitations. First, variations in top-silicon thickness introduce phase errors and will limit the performance of AWGs and ring-filter arrays. Second, the high index contrast between silicon and the cladding material maximizes waveguide scatter loss. And finally, the silicon material nonlinearities, most notably two-photon absorption and the resulting free-carrier absorption, limit the optical powers that the waveguide can handle.

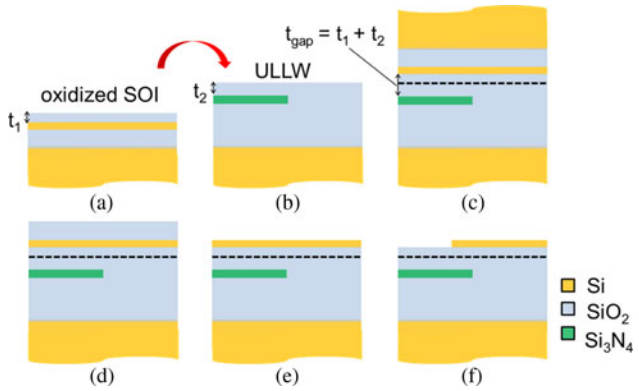

Fig. 23. Schematic overview of the back-end integration process used to integrate ULLWs on a silicon photonics platform [86].

Silica-on-silicon-based photonics, however, is less prone to these limitations. Recent work on Si_3N_4/SiO_2 high-aspect ratio waveguides has led to world-record low-propagation losses of less than 0.1 dB/m [79]. For more compact millimeter-bend radius waveguides, this value is around 3 dB/m [80]. This ultra-low loss waveguide (ULLW) platform enables long delay lines, low-loss AWGs [81], high-Q ring resonators [82], and high-extinction ratio waveguide polarizers [83]. Moreover, the low nonlinearity of SiO_2 and the relatively large mode sizes allow for high power handling [84].

It is clear that silica-based components would add significantly to the application possibilities of silicon PICs. However, existing integration approaches, such as those reported in [85], are not suitable to integrate ULLWs with silicon photonics. In the approach of [85], the silica waveguide films were deposited on an SOI wafer after the fabrication of silicon waveguides and devices on that wafer, which can, for example, include doping for PHMs. There are two main issues with this approach. First of all, the ULLWs require a thick cladding to avoid coupling to the silicon substrate, which means that coupling from the silicon to silica layer would become unfeasible. Second, ULLWs need to be annealed at temperatures over 1000 °C for several hours to drive out impurity hydrogen. These temperatures are not compatible with the SOI front-end process, e.g., because of dopant diffusion.

Fig. 23 shows the process flow for a novel integration approach that addresses these issues and allows for the integration of ULLWs on a silicon photonics platform [86]. ULLWs are fabricated, polished, and annealed. A thermally oxidized SOI wafer is then bonded using an oxygen plasma-assisted process and an anneal at 950 °C. Hereafter, the silicon substrate is removed using the buried oxide layer as an etch stop. Then, the buried oxide is also removed, leaving a crystalline and flat silicon film on top of the ULLW wafer. Further, SOI photonics processing is then done on a completely flat and clean surface. It should be emphasized that this process flow is fully compatible with the 8″ wafer CMOS fabrication infrastructure and

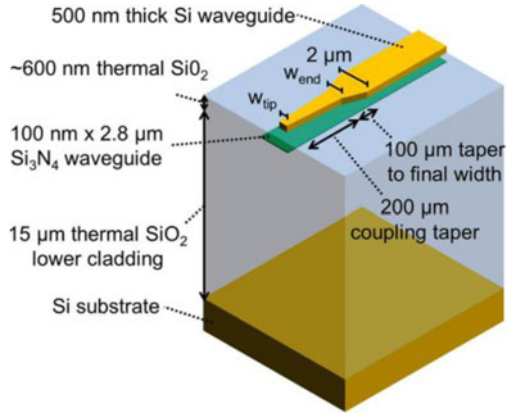

Fig. 24. Schematic of the structure used to couple light between ULLWs and silicon waveguide layers [86].

both ULLW and SOI photonics processing can be done in the same foundry. Coupling between the silicon and ULLW layers is achieved using tapers, as shown in Fig. 24. Coupling losses of (0.4 ± 0.2) dB per transition with a 20-nm 3-dB bandwidth and losses of (0.8 ± 0.2) dB per transition with a 100-nm 3-dB bandwidth for two different taper designs have been reported [86]. The ULLW loss for these 100-nm-thick Si_3N_4 waveguides was 1.2 dB/m at a wavelength of 1590 nm. In principle, this process is fully compatible with the hybrid silicon platform, although the thermal bottleneck is increased due to the thicker layer of oxide. Again, techniques like flip-chip bonding could be considered. Other options are microfluidic microchannel cooling.

IV. Hybrid Silicon PICs

In this section, we review the work on hybrid silicon PICs which combine a variety of components to make highly functional and integrated devices. These PICs are enabled by the technology platform as discussed in Section II and make use of the components, or building blocks, as reviewed in Section III.

A. AWG Multiwavelength Laser

The AWG-based multiwavelength or discretely tunable laser presented in [36] makes use of the integration of hybrid silicon actives with passive SOI-based circuitry. This is the first realization of a device where a silicon AWG is integrated with hybrid silicon SOAs. The mature CMOS technology allows in principle for high-quality and high-resolution AWGs, making this approach interesting for (D)WDM applications that require large channel counts. The layout of this laser is shown in Fig. 25(a) and (b). The AWG has eight channels with a channel spacing of 360 GHz. The 1 mm hybrid silicon SOAs are coupled to the silicon waveguides using a tapered mode converter. By biasing SOAs 1—4 above threshold, four lasing cavities are formed between (diced and polished) facets $f1-f4$ and the common output facet fc in Fig. 25(b). Lasing wavelength is determined by the AWG passband. An optical photograph of the fabricated device is shown in Fig. 25(c).

The AWG transmission spectrum in Fig. 26 shows slightly degraded passbands due to exposure of the silicon waveguides

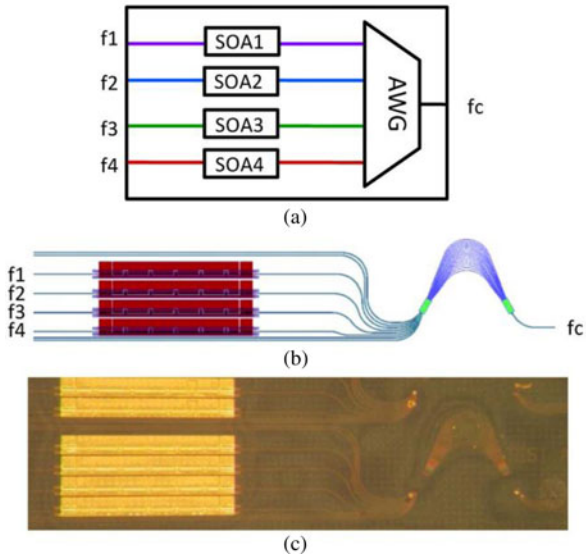

Fig. 25. (a) Schematic diagram of an AWG laser with four channels. (b) Schematic diagram of the fabricated chip. The AWG has eight channels. Four of the eight channels have hybrid silicon SOAs. (c) Optical photograph of the fabricated chip. The sample is covered with thick SU8 polymer that decreases the contrast of the image [36].

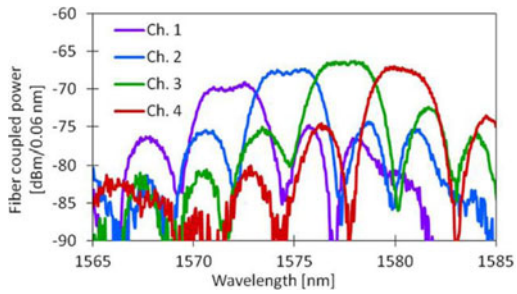

Fig. 26. ASE output of the common output waveguide for an SOA bias of 75 mA [36].

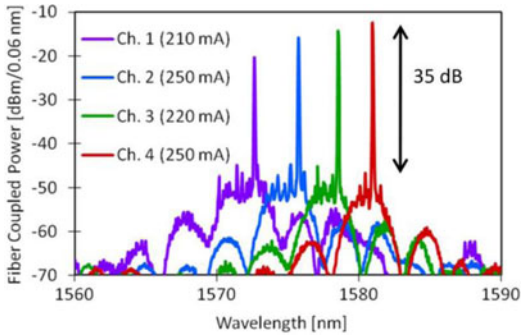

Fig. 27. Optical spectrum of the four channels optimized for the maximum SMSR [36].

to III-V etches, which slightly attacked the silicon, introducing phase errors. All four channels showed lasing, as depicted in Fig. 27, with output powers at the common facet of about 0.3 mW. This power can be almost doubled by applying a high-reflection coating on one side of the chip. Optimum SMSR was found to be 35 dB, as can be seen in Fig. 27. While this device is limited to four channels, it can be easily scaled up to several tens

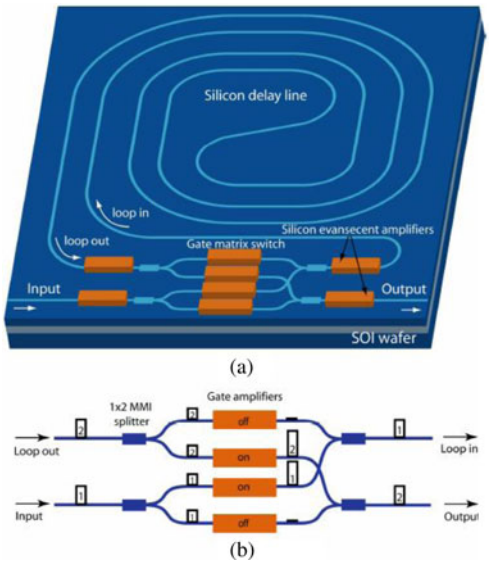

Fig. 28. Device layout: (a) integrated buffer and (b) gate matrix switch. The cross-over operation is illustrated as an example [89].

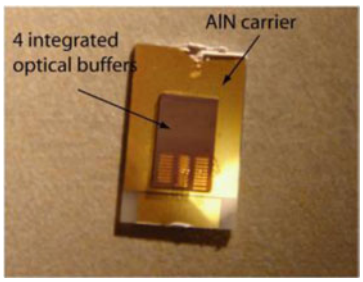

Fig. 29. Microscope image of the four integrated buffers mounted on an AlN carrier [89].

of channels as mature CMOS-manufacturing technology allows the fabrication of high-quality AWGs on SOI. Moreover, fast tuning, increased side-mode suppression, and decreased mode hopping can be achieved by similar designs that are compatible with this study [87], [88].

B. Optical Buffers

Silicon waveguides have relatively low loss, enabling PICs with relatively long delay lines. One such example is an integrated recirculating optical buffer. In [89], such a device is presented, integrating long passive silicon waveguides with hybrid silicon SOAs. A schematic of this device is shown in Fig. 28. The device has a 9-cm-long delay line and a hybrid silicon gate matrix switch. Optical packets were stored in the delay line until the gate matrix reroutes them to the output. Booster amplifiers in the delay line added gain to overcome the passive losses of the long silicon waveguides. Four buffers can be integrated on a 0.6×1 cm^2 chip by interleaving the four delay lines. An image of the mounted device is shown in Fig. 29.

The gain of the switch and booster amplifiers can overcome the 15 dB of passive silicon delay line loss. The crosstalk and dc extinction ratio of the gate matrix were measured to be -34 dB and 30 dB, respectively. The performance as a buffer was evaluated with a return-to-zero pseudorandom bit sequence at 40 Gb/s and at 1560 nm. The minimum power penalty with a 1.1 ns delay was 2.5 dB with an input dynamic range of 9 dB. Improved waveguide loss and amplifier gain were reported in [44], which allows for longer buffering times and increased packet size of 40 bytes at 40 Gb/s. Component yield needs to be increased for scaling to larger sizes. Such buffers will provide enough functionality as integrated optical buffers for all optical packet switched networks.

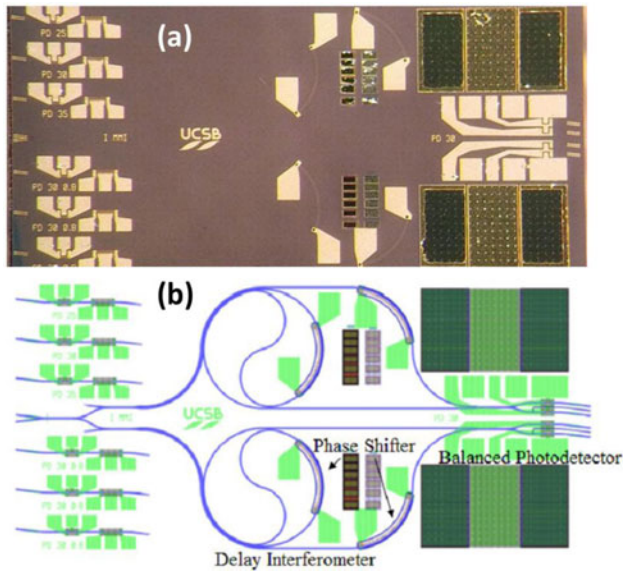

Fig. 30. (a) DQPSK receiver based on Mach–Zehnder delay interferometers and balanced detection. The footprint of the device is 1.8×3.5 mm^2. (b) Mask layout: waveguides are shown in blue, and metal contacts are light green. The layout includes stand-alone single PD test structures on the left.

C. 50 Gb/s DQPSK Receiver

The complexity and expensive implementation of advanced modulation methods for optical communication have limited their commercial development. One such technique is differential quadrature phase-shift keying (DQPSK). A DQPSK PIC-based receiver could provide a low-cost and compact solution to next-generation optical communication systems. Such a receiver based on the hybrid silicon platform was reported in [90].

The picture and corresponding mask layout are shown in Fig. 30. The receiver consists of two couplers, two 40 ps silicon delay interferometers including four thermo-optic NiCr phase tuners (one in each branch of the two delay interferometers), and two balanced InGaAs PD pairs. This design corresponds to 25 Gb/s operation for a single branch.

The III/V epitaxial layer stack has a 500-nm intrinsic InGaAs absorbing layer to optimize electrical bandwidth and responsivity [50]. The hybrid PDs have no tapered mode converters to limit the footprint and hence optimize the bandwidth. Instead, they have a 7° angled interface to minimize reflections. The optimum length of these PDs was found to be 30 μm. The responsivity is 0.64 A/W at wavelengths around 1550 nm and the electrical 3 dB bandwidth is over 20 GHz. Successful demodulation of a 25 Gb/s DPSK single-polarization TE signal by a

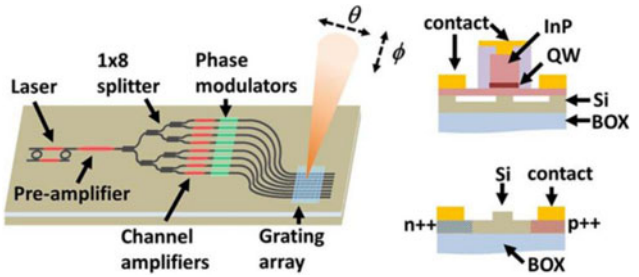

Fig. 31. Schematics (not to scale) of the overall device (left), cross section of the gain elements (right top), and cross section of the silicon PHMs (right bottom). QW: quantum wells, Si: silicon, BOX: buried oxide [42].

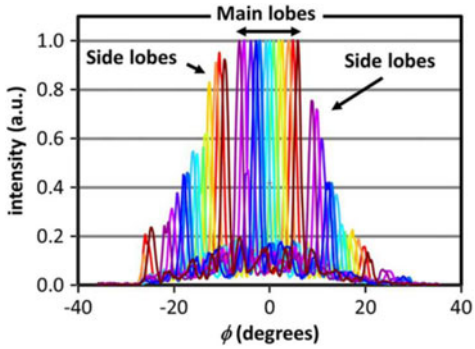

Fig. 32. Normalized far-field beam cross sections measured for beam positions from $\varphi = -6^\circ$ to $\varphi = 6^\circ$ at 1° increments [42].

single branch of the receiver demonstrates the working principle. The transmission results show a bit-error ratio of 10^{-9} for a received power of 13.8 dBm. Further integration of a PSR as proposed in [91] could enable a polarization-multiplexed (PM) DQPSK receiver at 100 Gb/s.

D. Beam Steering Chip

Fully integrated optical phased arrays can achieve fast nonmechanical free-space beam generation and beam steering for applications like free-space board-to-board adaptive optical interconnects and LIDAR (light detection and ranging). A silicon-based 2-D beam steering chip was presented in [92]. However, this chip has no source integrated. A hybrid silicon approach allows for the integration of the tunable laser source on-chip. Moreover to boost optical beam power for, e.g., LIDAR applications, booster SOAs can also be integrated. The first demonstration of such a chip is shown schematically in Fig. 31 [42]. An on-chip laser is coupled into a booster SOA followed by a 1 $\times$ 8 MMI-based splitter tree. Each channel has a separate SOA for further power boosting and equalization and silicon diode-based PHMs for phase tuning. These PHMs were operated in forward bias to make use of the thermo-optic effect by resistive heating. The light emits from a surface-grating array. By tuning and adjusting the PHMs, a beam in the far-field was shown to be formed and steered. The device footprint is 16 mm $\times$ 4 mm.

By tuning the phased array, a beam was formed having an angle of 1.8° along the steered axis and 0.6° along the nonsteered axis with 7 dB background suppression. By adjusting the PHMs, 12° beam steering was achieved, as shown in Fig. 32.

E. Hybrid Silicon CWDM Source Using QWI

The design of a WDM transmitter reveals a major limitation of most PIC platforms. The spectral range available for gain is restricted by the single bandgap QW design in the III/V layer stack. This can be a severely limiting factor in DWDM, especially in the case of coarse WDM transmitters where channel spacing is typically 20 nm. This limitation can be overcome in the hybrid silicon platform by either selective die bonding or QWI, as explained in Section II. QWI is the technique of choice for high density integration where devices with different bandgaps are closely interleaved. Moreover, selective die bonding becomes increasingly complex and hence costly when a larger number of bandgaps are required.

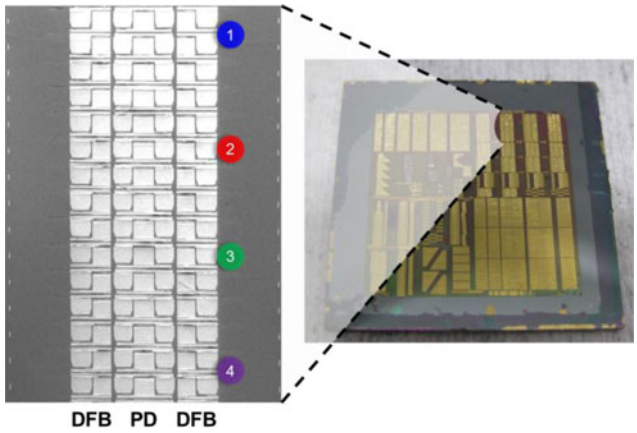

Fig. 33. (Right) Picture of the full QWI chip with (right) zoom in of the DFB laser array with backside PDs. The four bandgaps are indicated by numbers 1–4.

Using QWI, an array of distributed-feedback lasers (DFB) lasers for CWDM was reported [49]. Intermixing of InGaAsP QWs was used to generate four bandgaps spanning over 100 nm. This increase in gain bandwidth was then used to realize a broadband laser array on a single hybrid silicon chip. A picture of the full chip is shown in Fig. 33. The DFB lasers have lengths of 300 and 500 μm and have a quarter-wavelength shift. The grating pitch was varied from 185 to 230 nm to cover the optical spectrum from 1200 to 1500 nm. Backside PDs with the same cross section as the DFB lasers are integrated to allow for on-chip characterization.

Fig. 34 shows the lasing spectra of DFB lasers over all four bandgaps. Nine lasers spaced at $\sim$25 nm cover the entire O and E band from 1250 to 1450 nm. The DFB lasers exhibit a threshold current variation of 30–90 mA, which could be reduced by better control of bandgap placement during intermixing. At 20 °C, the maximum output power detected by on-chip PDs is about 2 mW. The SMSR is better than 30 dB. This approach could provide the spectral room necessary for scaling up of multichannel transmitters for terabit applications.

Arrays of eight EAMs integrated with DFB lasers and PDs were also integrated using QWI to shift the bandgap.

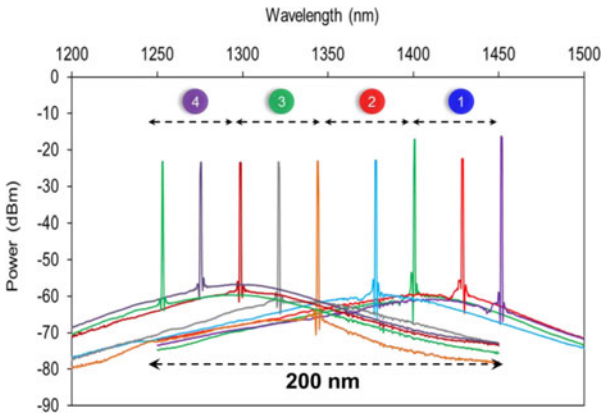

Fig. 34. Spectra of DFB lasers over four QWI bandgaps (1–4) operating at 150 mA.

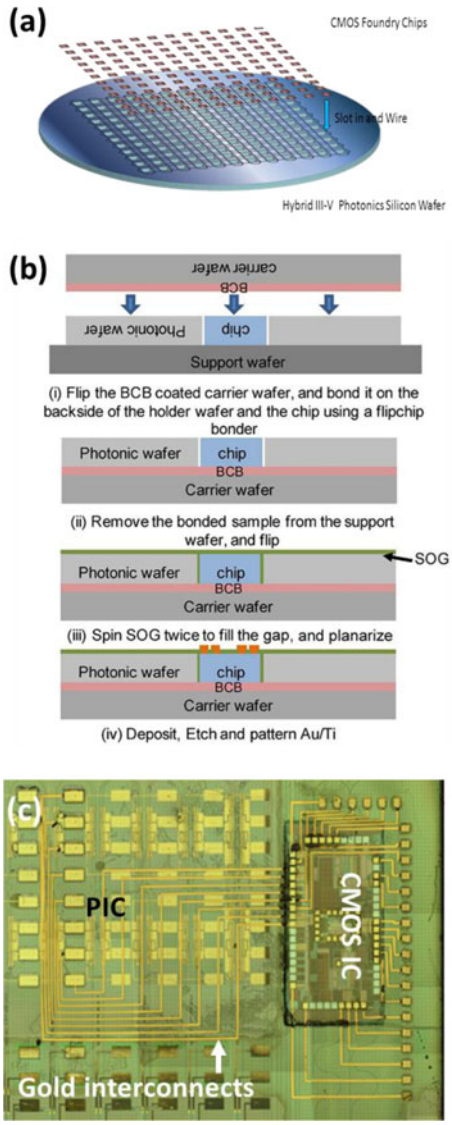

Fig. 35. (a) Schematic of the approach to integrate the CMOS IC with the PICs. (b) Process flow for the integration of the CMOS chip intimately with the photonics substrate [95], [96]. (c) Microscope picture of CMOS integration into a hybrid silicon PIC [97].

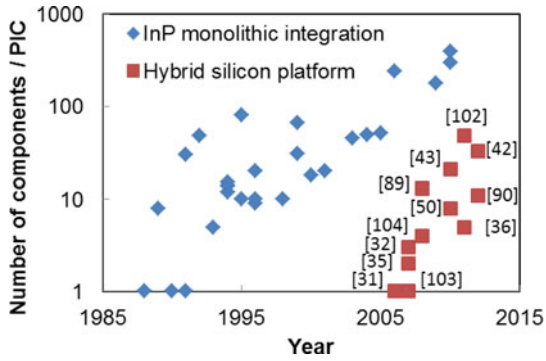

Fig. 36. Development of chip complexity measured as the number of components per chip. InP data (blue) taken from [101]. Hybrid silicon data taken from [31], [32], [35], [36], [42], [43], [50], [89], [90], [102]–[104].

Bandwidths over 30 GHz were measured across a 30-nm wavelength range with $V_{\rm pp}$ of 0.63 V at -2 V bias [93].

F. Integration With CMOS Electronics

To lower the cost and the energy consumption of PICs, close integration with CMOS driving electronics is required. In [94], a low-power high data rate optical packet switch for data center switching applications was reported. A hybrid silicon MZI-based optical chip was integrated side by side with a 0.13-μm CMOS driver IC. The PIC and electronic IC were connected by wirebonds and achieved 5 ns switching times at 250 μW power consumption.

Further integration can be achieved with the method presented in [95] and [96] and schematically shown in Fig. 35(a) and (b). A cavity was etched in the fully processed PIC and the electronic IC was placed in this cavity. The PIC wafer and the IC were then flipped on a support wafer to ensure that the processed surfaces were leveled. The chips were then bonded to a carrier wafer using benzocyclobutene. Electronic interconnects between PIC and electronic IC can now be defined lithographically on the flat surface. An example picture of CMOS integration into a hybrid silicon PIC is shown in Fig. 35(c). This approach overcomes the issue of PICs generally having a significantly larger footprint than electronic ICs, making monolithic integration on the same silicon substrate unattractive.

V. Conclusion

In this paper, we have reviewed the status of the hybrid silicon platform. The technology platform is well able to integrate silicon passives and actives with hybrid components using low-loss and low-reflectivity tapered mode converters and selective area bonding. Hybrid components that require different bandgaps, such as lasers, EAMs and PHMs, can be integrated using an additional QWI step, which is done prebonding. Finally, when completely different III/V epitaxial layer stacks are required, e.g., when lasers and SOAs have to be combined with high-speed and high-responsivity PDs, selective die bonding can be used. All these techniques are compatible with each other, meaning that the hybrid silicon platform has full access to all these components.

Recent developments show the future possibilities for complex hybrid silicon PICs. Broadband and reliable DFB laser arrays and MLL-based comb lasers enable high-capacity WDM transmitters in this platform, thus increasing the limits for parallel integration of components. SOAs and 2R regenerators are essential building blocks for serial integration, when losses have to be compensated while a signal travels through multiple components in a PIC. High-speed modulators are key enablers for applications of PICs in fields like advanced instrumentation and microwave photonics. Higher integration density will be enabled by miniaturization of components, such as microring lasers [98], [99], [103], [104]. Such lasers are expected to be able to operate at threshold currents below 1 mA [98]. For disk lasers, these low threshold currents have already been reported [100]. We further recognize that with increasing integration density, optical isolation becomes a necessity and we presented a compatible silicon ring-based isolator. Finally, the coupling of silicon to the ULLW platform will open up a plethora of possibilities where the hybrid silicon PICs can get access to meter-length delay lines, narrow-band filters in the megahertz range, and multiplexers with large channel count and narrow channel spacings.

The overview of medium-scale integrated PICs shows how the hybrid silicon platform has matured since its conception in 2006. To show the rate of progress more clearly, we plot in Fig. 36 the PIC complexity on a timeline, thereby following the outline and conventions laid out by Smit *et al*. [101]. It can be observed that InP-based monolithic integration has increased its complexity over the last two decades. Hybrid silicon PICs are catching up fast. There seem to be three major factors for this. First, hybrid silicon photonics can make use of the mature CMOS fabrication infrastructure for at least part of the process flow. Second, the hybrid silicon platform builds on the already existing knowledge of III/V-based photonics and rapidly incorporates that into the platform. And finally there is an early adoption by industry, with companies like Intel, HP, and Aurrion being active in this field and developing the technology. With these players, it seems likely that the first commercial implementation of hybrid silicon PICs will be in the field of optical interconnects, e.g., in datacenters [43].

Looking into the future, the question at hand is whether the hybrid silicon platform will be the platform of choice for complex PICs. Judging by an extrapolation of the data in Fig. 36, one can argue that the hybrid silicon platform will catch up with the monolithic InP-based PIC platform before 2020. Obviously, this is speculative and assumes that trends of increasing complexity will continue.

That will happen though if there are sufficient drivers. This seems to be the case since long-term requirements for cost, size, and power reduction of high-speed transceivers will lead to a broad demand for photonic integration [105]. In future terabit Ethernet applications, fully integrated solutions will become the technology of choice. Compared with InP-based PICs, hybrid silicon PICs offer the advantage of economies of scale. Current volumes do not seem to justify the choice for hybrid silicon PICs yet. However, when datacom, with volumes of 100 ks to 1 Ms per year, moves into the hundreds of gigabit or even terabit range, this volume increase of two orders of magnitude might well tip the balance toward hybrid silicon approaches, with their 300-mm silicon substrates and CMOS-compatible fabrication technology and the trends show that both academia and industry are well positioned to deliver.

ACKNOWLEDGMENT

The authors would like to thank B. Koch, G. Fish, E. Norberg, and A. Fang of Aurrion; M. Paniccia, R. Jones, and M. Sysak of Intel; D. Liang and R. Beausoleil of Hewlett Packard; A. Yariv of Caltech; D. Dai of Zhejiang University; L. Theogarajan, A. Sohdi, L. Chen, D. Blumenthal, L. Coldren, and J. Peters of UCSB for helpful discussions.

REFERENCES

[1] M. J. R. Heck, H.-W. Chen, A. W. Fang, B. R. Koch, D. Liang, H. Park, M. Sysak, and J.E. Bowers, "Hybrid silicon photonics for optical Interconnects," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 2, pp. 333–346, Mar./Apr. 2011.

[2] J. K. Doylend and A. P. Knights, "The evolution of silicon photonics as an enabling technology for optical interconnection," *Laser Photon. Rev.*, vol. 6, no. 4, pp. 504–525, Jul. 2012.

[3] A. Liu, R. Jones, L. Liao, D. Samara-Rubio, D. Rubin, O. Cohen, R. Nicolaescu, and M. Paniccia, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," *Nature*, vol. 427, no. 6975, pp. 615–618, 2004.

[4] D. Marris-Morini, X. L. Roux, L. Vivien, E. Cassan, D. Pascal, M. Halbwax, S. Maine, S. Laval, J. M. Fédéli, and J. F. Damlencourt, "Optical modulation by carrier depletion in a silicon PIN diode," *Opt. Exp.*, vol. 14, no. 22, pp. 10838–10843, 2006.

[5] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometrescale silicon electro-optic modulator," *Nature*, vol. 435, no. 7040, pp. 325–327, 2005.

[6] W. M. J. Green, M. J. Rooks, L. Sekaric, and Y. A. Vlasov, "Ultra-compact, low RF power, 10 Gb/s silicon Mach–Zehnder modulator," *Opt. Exp.*, vol. 15, no. 25, pp. 17106–17113, 2007.

[7] S. Manipatruni, Q. Xu, B. Schmidt, J. Shakya, and M. Lipson, "High speed carrier injection 18 Gb/s silicon micro-ring electro-optic modulator," in *Proc. 20th Annu. Meeting IEEE Lasers Electro-Opt. Soc.*, 2007, pp. 537–538.

[8] L. Liao, A. Liu, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, and M. Paniccia, "40 Gbit/s silicon optical modulator for high-speed applications," *Electron. Lett.*, vol. 43, no. 22, pp. 1196–1197, 2007.

[9] A. Liu, L. Liao, D. Rubin, J. Basak, Y. Chetrit, H. Nguyen, R. Cohen, N. Izhaky, and M. Paniccia, "Recent development in a high-speed silicon optical modulator based on reverse-biased pn diode in a silicon waveguide," *Semicond. Sci. Technol.*, vol. 23, no. 6, 064001, pp. 1–7, 2008.

[10] J. C. Rosenberg, W. M. J. Green, S. Assefa, C. L. Schow, A. V. Rylyakov, D. M. Gill, B. G. Lee, C. Jahnes, T. Barwicz, S. M. Shank, and Y. A. Vlasov, "High-speed and low-power microring modulators for silicon photonics," in *Proc. IEEE Photon. Conf.*, Oct. 9–13, 2011, pp. 256–257.

[11] J. E. Roth, O. Fidaner, R. K. Schaevitz, Y.-H. Kuo, T. I. Kamins, J. S. Harris, and D. A. B. Miller, "Optical modulator on silicon employing germanium quantum wells," *Opt. Exp.*, vol. 15, no. 9, pp. 5851–5859, 2007.

[12] D. Ahn, C.-Y. Hong, J. Liu, W. Giziewicz, M. Beals, L. C. Kimerling, J. Michel, J. Chen, and F. X. Kärtner, "High performance, waveguide integrated Ge photodetectors," *Opt. Exp.*, vol. 15, no. 7, pp. 3916–3921, 2007.

[13] J. Liu, X. Sun, R. Camacho-Aguilera, L. C. Kimerling, and J. Michel, "Ge-on-Si laser operating at room temperature," *Opt. Lett.*, vol. 35, pp. 679–681, 2010.

[14] D. Liang and J. E. Bowers, "Recent progress in lasers on silicon," *Nat. Photon.*, vol. 4, pp. 511–517, 2010.

[15] L. Zhang, J. Sinsky, D. Van Thourhout, N. Sauer, L. Stulz, A. Adamiecki, and S. Chandrasekhar, "Low-voltage high-speed travelling wave InGaAsP–InP phase modulator," *IEEE Photon. Technol. Lett.*, vol. 16, no. 8, pp. 1831–1833, Aug. 2004.

[16] H. N. Klein, H. Chen, D. Hoffmann, S. Staroske, A. G. Steffan, and K.-O. Velthaus, "1.55 μm Mach–Zehnder modulators on InP for

optical 40/80 Gbit/s transmission networks," in *Proc. Int. Indium Phosphide Related Mater. Conf.*, 2006, pp. 171–173.

[17] H. Ohe, H. Shimizu, and Y. Nakano, "InGaAlAs multiple-quantum-well optical phase modulators based on carrier depletion," *IEEE Photon. Technol. Lett.*, vol. 19, no. 22, pp. 1816–1818, Nov. 2007.

[18] M. Chaciński, U. Westergren, B. Stoltz, L. Thylén, R. Schatz, and S. Hammerfeldt, "Monolithically integrated 100 GHz DFB-TWEAM," *J. Lightw. Technol.*, vol. 27, pp. 3410–3415, 2009.

[19] S. Kodama, T. Yoshimatsu, and H. Ito, "500 Gbit/s optical gate monolithically integrating photodiode and electroabsorption modulator," *Electron. Lett.*, vol. 40, pp. 555–556, 2004.

[20] A. Beling and J. C. Campbell, "InP-Based high-speed photodetectors," *J. Lightw. Technol.*, vol. 27, no. 3, pp. 343–355, 2009.

[21] D. Liang, G. Roelkens, R. Baets, and J. E. Bowers, "Hybrid integrated platforms for silicon photonics," *Materials*, vol. 3, pp. 1782–1802, 2010.

[22] D. A. B. Miller, "Device requirements for optical interconnects to silicon chips," *Proc. IEEE*, vol. 97, no. 7, pp. 1166–1185, Jul. 2009.

[23] M. Iqbal, M. A. Gleeson, B. Spaugh, F. Tybor, W. G. Gunn, M. Hochberg, T. Baehr-Jones, R. C. Bailey, and L. C. Gunn, "Label-free biosensor arrays based on silicon ring resonators and high-speed optical scanning instrumentation," *IEEE J. Sel. Topics Quantum Electron.*, vol. 16, no. 3, pp. 654–661, May/Jun. 2010.

[24] M. Kuramoto, N. Kitajima, H. Guo, Y. Furushima, M. Ikeda, and H. Yokoyama, "Two-photon fluorescence bioimaging with an all-semiconductor laser picosecond pulse source," *Opt. Lett.*, vol. 32, no. 18, pp. 2726–2728, Sep. 2007.

[25] K. W. Holman, D. J. Jones, J. Ye, and E. P. Ippen, "Orthogonal control of the frequency comb dynamics of a mode-locked laser diode," *Opt. Lett.*, vol. 28, no. 23, pp. 2405–2407, Dec. 2003.

[26] A. Black, A. R. Hawkins, N. M. Margalit, D. I. Babic, A. L. Holmes, Y.-L. Chang, P. Abraham, J. E. Bowers, and E. L. Hu, "Wafer fusion: Materials issues and device results," *IEEE J. Sel. Topics Quantum Electron.*, vol. 3, no. 3, pp. 943–951, Jun. 1997.

[27] D. Pasquariello, C. Hedlund, and K. Hjort, "Oxidation and induced damages in oxygen plasma in situ wafer bonding," *J. Electrochem. Soc.*, vol. 147, pp. 2699–2702, 2000.

[28] S. Stankovic, R. Jones, M. N. Sysak, J. M. Heck, G. Roelkens, and D. Van Thourhout, "1310-nm Hybrid III–V/Si Fabry–Pérot laser based on adhesive bonding," *IEEE Photon. Technol. Lett.*, vol. 23, no. 23, pp. 1781–1783, Dec. 2011.

[29] B. Ben Bakir, A. Descos, N. Olivier, D. Bordel, P. Grosse, E. Augendre, L. Fulbert, and J. M. Fedeli, "Electrically driven hybrid Si/III-V Fabry–Pérot lasers based on adiabatic mode transformers," *Opt. Exp.*, vol. 19, no. 11, pp. 10317–10325, 2011.

[30] T. Wang, H. Liu, A. Lee, F. Pozzi, and A. Seeds, "1.3-μm InAs/GaAs quantum-dot lasers monolithically grown on Si substrates," *Opt. Exp.*, vol. 19, no. 12, pp. 11381–11386, 2011.

[31] A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia, and J.E. Bowers, "Electrically pumped hybrid AlGaInAs-silicon evanescent laser," *Opt. Exp.*, vol. 14, pp. 9203–9210, 2006.

[32] A. W. Fang, H. Park, Y.-H. Kuo, R. Jones, O. Cohen, D. Liang, O. Raday, M. N. Sysak, M. J. Paniccia, and J. E. Bowers, "Hybrid silicon evanescent devices," *Mater. Today*, vol. 10, no. 7–8, pp. 28–35, 2007.

[33] M. Lamponi, S. Keyvaninia, C. Jany, F. Poingt, F. Lelarge, G. de Valicourt, G. Roelkens, D. Van Thourhout, S. Messaoudene, J.-M. Fedeli, and G. H. Duan, "Low-threshold heterogeneously integrated InP/SOI laser with a double adiabatic taper coupler," *IEEE Photon. Technol. Lett.*, vol. 24, no. 1, pp. 76–78, Jan. 2012.

[34] X. K. Sun, A. Zadok, M. J. Shearn, K. A. Diest, A. Ghaffari, H. A. Atwater, A. Scherer, and A. Yariv, "Electrically pumped hybrid evanescent Si/InGaAsP lasers," *Opt. Lett.*, vol. 34, pp. 1345–1347, May 2009.

[35] H. Park, Y.-H. Kuo, A. W. Fang, R. Jones, O. Cohen, M. J. Paniccia, and J. E. Bowers, "A hybrid AlGaInAs-silicon evanescent preamplifier and photodetector," *Opt. Exp.*, vol. 15, no. 21, pp. 13539–13546, 2007.

[36] G. Kurczveil, M. J. R. Heck, J. D. Peters, J. M. Garcia, D. Spencer, and J. E. Bowers, "An Integrated hybrid silicon multiwavelength AWG laser," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 6, pp. 1521–1527, Nov./Dec. 2011.

[37] G. Kurczveil, P. Pintus, M. J. R. Heck, J. D. Peters, and J. E. Bowers, "Characterization of insertion loss and back reflection in Passive Hybrid Silicon Tapers," *IEEE Photon. J.*, vol. 5, no. 2, p. 6600410, 2013.

[38] P. Pintus, M. J. R. Heck, G. Kurczveil, and J. E. Bowers, "Low-loss hybrid silicon tapers," presented at the Group IV Photonics, London, U.K., 2011.

[39] A. Poustie, "Hybrid integration for advanced photonic devices," *Proc. SPIE*, vol. 7135, 713502, pp. 1–10, 2008, doi: 10.1117/12.803089.

[40] S. A. Moore, L. O'Faolain, M. A. Cataluna, M. B. Flynn, M. V. Kotlyar, and T. F. Krauss, "Reduced surface sidewall recombination and diffusion in quantum-dot lasers," *IEEE Photon. Technol. Lett.*, vol. 18, no. 17, pp. 1861–1863, Sep. 2006.

[41] M. Hochberg and T. Baehr-Jones, "Towards fabless silicon photonics," *Nat. Photon.*, vol. 4, pp. 492–494, 2010.

[42] J. K. Doylend, M. J. R. Heck, J. T. Bovington, J. D. Peters, M. L. Davenport, L. A. Coldren, and J. E. Bowers, "Hybrid III/V silicon photonic source with integrated 1D free-space beam steering," *Opt. Soc. Amer. Opt. Lett.*, vol. 37, no. 20, pp. 4257–4259, 2012.

[43] A. Alduino, L. Liao, R. Jones, M. Morse, B. Kim, W.-Z. Lo, J. Basak, B. Koch, H.-F. Liu, H. Rong, M. Sysak, C. Krause, R. Saba, D. Lazar, L. Horwitz, R. Bar, S. Litski, A. Liu, K. Sullivan, O. Dosunmu, N. Na, T. Yin, F. Haubensack, I.-W. Hsieh, J. Heck, R. Beatty, H. Park, J. Bovington, S. Lee, H. Nguyen, H. Au, K. Nguyen, P. Merani, M. Hakami, and M. Paniccia, "Demonstration of a high speed 4-channel integrated silicon photonics WDM link with hybrid silicon lasers," presented at the Opt. Soc. Amer. Tech. Dig. Integrated Photonics Res., Silicon Nanophotonics, Monterey, CA, 2010, Paper PDIWI5.

[44] G. Kurczveil, M. J. R. Heck, J. M. Garcia, H. N. Poulsen, H. Park, D. J. Blumenthal, and J. E. Bowers, "Integrated recirculating optical hybrid silicon buffers," in *SPIE Photonics West*. San Francisco, CA: SPIE, Jan. 2011.

[45] E. J. Skogen, J. W. Raring, G. B. Morrison, C. S. Wang, V. Lal, M. L. Masanovic, and L. A. Coldren, "Monolithically integrated active components: A quantum-well intermixing approach," *IEEE J. Sel. Topics Quantum Electron.*, vol. 11, no. 2, pp. 343–355, Mar./Apr. 2005.

[46] M. N. Sysak, J. O. Anthes, J. E. Bowers, O. Raday, and R. Jones, "Integration of hybrid silicon lasers and electroabsorption modulators," *Opt. Exp.*, vol. 16, no. 17, pp. 12478–12486, Aug. 2008.

[47] E. J. Skogen, J. S. Barton, S. P. Denbaars, and L. A. Coldren, "A quantum-well-intermixing process for wavelength-agile photonic integrated circuits," *IEEE J. Sel. Topics Quantum Electron.*, vol. 8, no. 4, pp. 863–869, Jul./Aug. 2002.

[48] S. R. Jain, M. N. Sysak, G. Kurczveil, and J. E. Bowers, "Integrated hybrid silicon DFB laser-EAM array using quantum well intermixing," *Opt. Exp.*, vol. 19, no. 14, pp. 13692–13699, 2011.

[49] S. R. Jain, M. N. Sysak, and J. E. Bowers, "Hybrid silicon CWDM source using quantum well intermixing," in *Proc. IEEE Int. Semicond. Laser Conf.*, San Diego, Oct. 10, 2012.

[50] H.-H. Chang, Y.-H. Kuo, R. Jones, A. Barkai, and J. E. Bowers, "Integrated hybrid silicon triplexer," *Opt. Exp.*, vol. 18, no. 23, pp. 23891–23899, 2010.

[51] H. Park, M. N. Sysak, H.W. Chen, A. W. Fang, D. Liang, L. Liao, B. R. Koch, J. Bovington, Y. Tang, K. Wong, M. Jacob-Mitos, R. Jones, and J. E. Bowers, "Device and integration technology for silicon photonic transmitters," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 3, pp. 671–688, May/Jun. 2011.

[52] H.-H. Chang, A. W. Fang, M. N. Sysak, H. Park, R. Jones, O. Cohen, O Raday, M. J. Paniccia, and J. E. Bowers, "1310 nm silicon evanescent laser," *Opt. Exp.*, vol. 15, no. 18, pp. 11466–11471, 2007.

[53] G. Fish, J. Roth, V. Kaman and A. Fang, "Advances in III–V heterogeneous integration on silicon," in *Proc. IEEE Photonics Conf. (IPC),* Sep. 23–27, 2012, pp. 747–748.

[54] M. N. Sysak, D. Liang, R. Jones, G. Kurczveil, M. Piels, M. Fiorentino, R. G. Beausoleil, and J. E. Bowers, "Hybrid silicon laser technology: A thermal perspective," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 6, pp. 1490–1498, Nov./Dec. 2011.

[55] D. Liang, M. Fiorentino, S. T. Todd, G. Kurczveil, R. G. Beausoleil, and J. E. Bowers, "Fabrication of silicon-on-diamond substrate and low-loss optical waveguides," *IEEE Photon. Technol. Lett.*, vol. 23, no. 10, pp. 657–659, May 2011.

[56] A. W. Fang, M. N. Sysak, B. R. Koch, R. Jones, E. Lively, Y.H. Kuo, D. Liang, O. Raday, and J. E. Bowers, "Single-wavelength silicon evanescent lasers," *IEEE J. Sel. Topics. Quantum Electron.*, vol. 15, no. 3, pp. 535–544, May/Jun. 2009.

[57] S. Srinivasan, A.W. Fang, D. Liang, J. Peters, B. Kaye, and J. E. Bowers, "Design of phase-shifted hybrid silicon distributed feedback lasers," *Opt. Exp.*, vol. 19, p. 9255, 2011.

[58] M. J. R. Heck, E. A. J. M. Bente, Y. Barbarin, D. Lenstra, and M. K. Smit, "Simulation and design of integrated femtosecond passively mode-locked semiconductor ring lasers including integrated passive pulse shaping

components," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 2, pp. 265–276, Mar./Apr. 2006.
[59] S. Srinivasan and J. E. Bowers, "Reliability of hybrid III-V on Si distributed feedback lasers," in *Proc. IEEE Int. Semiconductor Laser Conf.* , 2012, pp. 10–11.
[60] M. L. Davenport, G. Kurczveil, M. J. R. Heck, and J. E. Bowers, "A hybrid silicon colliding pulse mode-locked laser with integrated passive waveguide section," in *Proc. IEEE Photon Conf.*, 2012, pp. 816–817.
[61] H. Park, Y.-H. Kuo, A. W. Fang, R. Jones, O. Cohen, M. J. Paniccia, and J.E. Bowers, "A hybrid AlGaInAs-silicon evanescent preamplifier and photodetector," *Opt. Exp.*, vol. 15, no. 21, pp. 13539–13546, Oct. 2007.
[62] M. J. R. Heck, E. A. J. M. Bente, Y. Barbarin, A. Fryda, H.-D. Jung, Y. S. Oei, R. Nötzel, D. Lenstra, and M. K. Smit, "Characterization of a monolithic concatenated SOA/SA waveguide device for picosecond pulse amplification and shaping," *IEEE J. Quantum Electron.*, vol. 44, no. 4, pp. 360–369, Apr. 2008.
[63] G. Kurczveil, M. J. R. Heck, J. D. Peters, and J. E. Bowers, "An integrated and compact hybrid silicon 2R regenerator," in *Proc. IEEE Photon. Conf.*, 2012, pp. 751–752.
[64] Y. Tang, H.-W. Chen, S. Jain, J. D. Peters, U. Westergren, and J. E. Bowers, "50 Gb/s hybrid silicon traveling-wave electroabsorption modulator," *Opt. Exp.*, vol. 19, pp. 5811–5816, 2011.
[65] Y. Tang, J. D. Peters, and J. E. Bowers, "Over 67 GHz bandwidth hybrid silicon electroabsorption modulator with asymmetric segmented electrode for 1.3 μm transmission," *Opt. Exp.*, vol. 20, no. 10, pp. 11529–11535, May 2012.
[66] Y. Tang, J. D. Peters, and J. E. Bowers, "Energy-efficient hybrid silicon electroabsorption modulator for 40-Gb/s 1-V uncooled operation," *IEEE Photon. Technol. Lett.*, vol. 24, no. 19, pp. 1689–1692, Oct. 2012.
[67] D. Dai, Z. Wang, and J. E Bowers, "Ultra-short broad-band polarization beam splitter based on an asymmetrical directional coupler," *Opt. Lett.*, vol. 36, no. 13, pp. 2590–2592, 2011.
[68] D. Dai and J. E. Bowers, "Novel ultra-short and ultra-broadband polarization beam splitter based on a bent directional coupler," *Opt. Exp.*, vol. 19, pp. 18614–18620, 2011.
[69] Z. Wang and D. Dai, "Ultrasmall Si-nanowire-based polarization rotator," *J. Opt. Soc. Amer. B*, vol. 25, no. 5, pp. 747–753, 2008.
[70] D. Dai and J. E. Bowers, "Novel concept for ultracompact polarization splitter-rotator based on silicon nanowires," *Opt. Exp.*, vol. 19, pp. 10940–10949, 2011.
[71] D. Dai, Y. Tang, and J. E Bowers, "Mode conversion in tapered submicron silicon ridge optical waveguides," *Opt. Exp.*, vol. 20, no. 12, pp. 13425–13439, 2012.
[72] Y. Shoji, T. Mizumoto, H. Yokoi, I. W. Hsieh, and R. M. Osgood, "Magneto-optical isolator with silicon waveguides fabricated by direct bonding," *Appl. Phys. Lett.*, vol. 92, no. 7, 071117, pp. 1–3, 2008.
[73] M. J. R. Heck, A. J. M. Bente, Y. Barbarin, D. Lenstra, and M. K. Smit, "Monolithic semiconductor waveguide device concept for picosecond pulse amplification, isolation and spectral shaping," *IEEE J. Quantum Electron.*, vol. 43, no. 10, pp. 910–922, Oct. 2007.
[74] M.-C. Tien, T. Mizumoto, P. Pintus, H. Kroemer, and J. E. Bowers, "Silicon ring isolators with bonded nonreciprocal magneto-optic garnets," *Opt. Exp.*, vol. 19, no. 12, pp. 11740–11745, 2011.
[75] L. Bi, J. Hu, P. Jiang, D. H. Kim, G. F. Dionne, and L. C. Kimerling, "On-chip optical isolation in monolithically integrated non-reciprocal optical resonators," *Nat. Photon.*, vol. 5, pp. 758–762, 2011.
[76] P. Pintus, M.-C. Tien, and J. E. Bowers, "Design of magneto-optical ring isolator on SOI based on the finite-element method," *IEEE Photon. Technol. Lett.*, vol. 23, no. 22, pp. 1670–1672, Nov. 2011.
[77] P. Pintus, F. Di Pasquale, and J. E. Bowers, "Design of transverse electric ring isolators for ultra-low-loss Si_3N_4 waveguides based on the finite element method," *Opt. Lett.*, vol. 36, no. 23, pp. 4599–4601, 2011.
[78] P. Pintus, F. Di Pasquale, and J. E. Bowers, "Four-port integrated optical circulator based on ultra-low-loss Si_3N_4 waveguides for DWDM applications," *Opt. Lett.*, submitted.
[79] J. F. Bauters, M. J. R. Heck, D. John, J. S. Barton, A. Leinse, R. G. Heideman, D. J. Blumenthal, and J. E. Bowers, "Planar waveguides with less than 0.1 dB/m propagation loss fabricated with wafer bonding," *Opt. Soc. Amer Opt. Exp.*, vol. 19, no. 24, pp. 24090–24101, 2011.
[80] J. F. Bauters, M. J. R. Heck, D. John, D. Dai, M.-C. Tien, J. S. Barton, A. Leinse, R. G. Heideman, D. J. Blumenthal, and J. E. Bowers, "Ultra-low-loss high-aspect-ratio Si3N4 waveguides," *Opt. Exp.*, vol. 19, no. 4, pp. 3163–3174, 2011.
[81] D. Dai, Z. Wang, J. F. Bauters, M.-C. Tien, M. J. R. Heck, D. J. Blumenthal, and J. E. Bowers, "Low-loss Si3N4 arrayed-waveguide grating (de)multiplexer using nano-core optical waveguides," *Opt. Soc. Amer. Opt. Exp.*, vol. 19, no. 15, pp. 14130–14136, 2011.
[82] M.-C. Tien, J. F. Bauters, M. J. R. Heck, D. J. Blumenthal, and J. E. Bowers, "Ultra-high quality factor of Si3N4 ring resonators with integrated directional couplers," *Opt. Exp.*, vol. 19, no. 14, pp. 13551–13556, 2011.
[83] J. F. Bauters, M. J. R. Heck, D. Dai, J. S. Barton, D. J. Blumenthal, and J. E. Bowers, "Planar silica waveguide polarizers," *IEEE Photon. J.*, vol. PP, no. 99, pp. 1, doi: 10.1109/JPHOT.2012.2234095.
[84] M.C. Tien, J. F. Bauters, M. J. R. Heck, D. J. Blumenthal, and J. E. Bowers, "Ultra-low loss Si3N4 waveguides with low nonlinearity and high power handling capability," *Opt. Exp.*, vol. 18, pp. 23562–23568, 2010.
[85] T. Tsuchizawa, K. Yamada, T. Watanabe, S. Park, H. Nishi, R. Kou, H. Shinojima, and S. Itabashi, "Monolithic integration of silicon-, germanium-, and silica-based optical devices for telecommunications applications," *IEEE J. Sel. Top. Quantum Electron*, vol. 17, no. 3, pp. 516–525, May/Jun. 2011.
[86] J. F. Bauters, M. L. Davenport, M. J. R. Heck, J. K. Doylend, A. Chen, A. W. Fang, and J. E. Bowers, "Silicon on ultra-low-loss waveguide photonic integration platform," *Opt. Exp.*, vol. 21, no. 1, pp. 544–555, 2013.
[87] B. Docter, J. Pozo, S. Beri, I. V. Ermakov, J. Danckaert, M. K. Smit, and F. Karouta, "Discretely tunable laser based on filtered feedback for telecommunication applications," *IEEE J. Sel. Topics Quantum Electron.*, vol. 16, no. 5, pp. 1405–1412, Sep./Oct. 2010.
[88] M. J. R. Heck, A. la Porta, X. J. M. Leijtens, L. M. Augustin, T. de Vries, E. Smalbrugge, Y. S. Oei, R. Nötzel, R. Gaudino, D. J. Robbins, and M. K. Smit, "Monolithic AWG-based discretely tunable laser diode with nanosecond switching speed," *IEEE Photon. Technol. Lett.*, vol. 21, no. 13, pp. 905–907, 2009.
[89] H. Park, J. P. Mack, D. J. Blumenthal, and J. E. Bowers, "An integrated recirculating optical buffer," *Opt. Exp.*, vol. 16, no. 15, pp. 11124–11131, 2008.
[90] S. Faralli, K. N. Nguyen, J. D. Peters, D. T. Spencer, D. J. Blumenthal, and J. E. Bowers, "Integrated hybrid Si/InGaAs 50 Gb/s DQPSK receiver," *Opt. Exp.*, vol. 20, no. 18, pp. 19726–19734, Aug. 2012.
[91] D. Dai and J. E. Bowers, "Novel concept for ultracompact polarization splitter-rotator based on silicon nanowires," *Opt. Exp.*, vol. 19, no. 11, pp. 10940–10949, 2011.
[92] J. K. Doylend, M. J. R. Heck, J. T. Bovington, J. D. Peters, L. A. Coldren, and J. E. Bowers, "Two-dimensional free-space beam steering with an optical phased array on silicon-on-insulator," *Opt. Soc. Amer. Opt. Exp.*, vol. 19, no. 22, pp. 21595–21604, 2011.
[93] S. R. Jain, M. N. Sysak, M. Piels, and J. E. Bowers, "Hybrid silicon transmitter using quantum well intermixing," in *Proc. OFC*, 2013, to be published.
[94] L. Chen, Y. Tang, J.E. Bowers, and L. Theogarajan, "CMOS enabled silicon photonics for data center packet switching," in *Proc. IEEE Microwave Symp. Digest* , Jun. 2012, pp. 1–3.
[95] L. Chen, E. Hall, L. Theogarajan, and J. E. Bowers, "Photonic switching for data center applications," vol. 3, no. 5, pp. 834–844, Oct. 2011.
[96] A. Uddin, K. Milaninia, C.H. Chen, and L. Theogarajan, "Wafer scale integration of CMOS chips for biomedical applications via self-aligned masking," *IEEE Trans. Compon., Packag., Manuf. Technol.*, vol. 1, no. 12, pp. 1996–2004, Dec. 2011.
[97] L. Chen, J. Hulme, A. Sohdi, J. Roth, V. Kaman, G. Fish, J. E. Bowers, and L. Theogarajan, "Digitally tunable optical power equalization for large port count optical switches," in *Proc. OFC*, 2013, to be published.
[98] D. Liang, M. Fiorentino, S. Srinivasan, J. E. Bowers, and R. G. Beausoleil, "Low threshold electrically-pumped hybrid silicon microring lasers," *IEEE J. Sel. Topics Quantum Electron.*, vol. 17, no. 6, pp. 1528–1533, Nov./Dec. 2011.
[99] D. Liang, M. Fiorentino, S. Srinivasan, S. T. Todd, G. Kurczveil, J. E. Bowers, and R. G. Beausoleil, "Optimization of hybrid silicon microring lasers," *IEEE Photon. J.*,, vol. 3, no. 3, pp. 580–587, Jun. 2011.
[100] L. Liu, R. Kumar, K. Huybrechts, T. Spuesens, G. Roelkens, E.J. Geluk, T. de Vries, P. Regreny, D. Van Thourhout, R. Baets, and G. Morthier, "An ultra-small, low-power, all-optical flip-flop memory on a silicon chip," *Nat. Photon.*, vol. 4, pp. 182–187, 2010.
[101] M. K. Smit, J. J. G. M. van der Tol, and M. T. Hill, "Moore's law in photonics," *Laser Photon.*, vol. 6, no. 1, pp. 1–13, 2012.
[102] G. Fish, S. Nicholes, V. Kaman, and A. W. Fang, "Heterogeneous photonic integration for microwave systems applications," in *Proc. IEEE Photon. Conf.*, 2011, pp. 87–88.

[103] J. Van Campenhout, P. Rojo-Romeo, P. Regreny, C. Seassal, D. Van Thourhout, S. Verstuyft, L. Di Cioccio, J.-M. Fedeli, C. Lagahe, and R. Baets, "Electrically pumped InP-based microdisk lasers integrated with a nanophotonic SOI waveguide circuit," *Opt. Exp.*, vol. 15, no. 11, pp. 6744–6749, 2007.
[104] J. Van Campenhout, L. Liu, P. R. Romeo, D. Van Thourhout, C. Seassal, P. Regreny, L. Di Cioccio, J. M. Fedeli, and R. Baets, "A compact SOI-integrated multiwavelength laser source based on cascaded InP microdisks," *IEEE Photon. Technol. Lett.*, vol. 20, no. 16, pp. 1345–1347, Jul./Aug. 2008.
[105] C. Cole, B. Huebner, and J. E. Johnson, "Photonic integration for high-volume, low-cost applications," *IEEE Commun. Mag.*, vol. 47, no. 3, pp. S16–S22, Mar. 2009.

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