UCLA UCLA Previously Published Works

Title

Phase Change Random Access Memory for Neuro-Inspired Computing

Permalink

https://escholarship.org/uc/item/9377q0c8

Journal Advanced Electronic Materials, 7(6)

ISSN

2199-160X

Authors

Wang, Qiang Niu, Gang Ren, Wei <u>et al.</u>

Publication Date

2021-06-01

DOI

10.1002/aelm.202001241

Peer reviewed



Phase Change Random Access Memory for Neuro-Inspired Computing

Qiang Wang, Gang Niu,* Wei Ren,* Ruobing Wang, Xiaogang Chen, Xi Li, Zuo-Guang Ye, Ya-Hong Xie, Sannian Song, and Zhitang Song*

Neuro-inspired computing using emerging memristors plays an increasingly significant role for the realization of artificial intelligence and thus has attracted widespread interest in the era of big data. Thanks to the maturity of technology and the superiority of device performance, phase change random access memory (PCRAM) is a promising candidate for both nonvolatile memories and neuro-inspired computing. Recently many efforts have been carried out to achieve the biological behavior using PCRAM and to clarify the related working mechanism. In order to further improve device performances, it is helpful and urgent to summarize and discuss the PCRAM solution for neuro-inspired computing. In this paper, fundamentals, principles, recent progresses, existing challenges, and mainstream solutions are reviewed, and a brief outlook is highlighted and introduced, with the expectation to expound future directions.

1. Introduction

Artificial intelligence (AI) is leading a wave of unprecedented information technological revolution. As a promising route, hardware implementation of adaptive parallel processing in biological neural networks (BioNNs) by the means of neuro-inspired computing is proposed,^[1] which aims to eliminate the energy-intensive and inefficient transmission in von Neumann-based platforms.

Q. Wang, Prof. G. Niu, Prof. W. Ren Electronic Materials Research Laboratory Key Laboratory of the Ministry of Education and International Center for Dielectric Research School of Electronic Science and Engineering Xi'an Jiaotong University Xi'an 710049, China E-mail: gangniu@xjtu.edu.cn; wren@xjtu.edu.cn R. B. Wang, Dr. X. G. Chen, Dr. X. Li, Prof. S. N. Song, Prof. Z. T. Song State Key Laboratory of Functional Materials for Informatics Shanghai Institute of Microsystem and Information Technology Chinese Academy of Sciences 865 Changning Road, Shanghai 200050, China E-mail: ztsong@mail.sim.ac.cn Prof. Z.-G. Ye Department of Chemistry and 4D LABS Simon Fraser University Burnaby, British Columbia V5A 1S6, Canada Prof. Y.-H. Xie Department of Materials Science and Engineering University of California, Los Angeles Los Angeles, CA 90095, USA

DOI: 10.1002/aelm.202001241

The digital-bits encoded artificial neural networks (ANNs) and the spike-timing encoded spiking neural networks (SNNs) are the two main paradigms of neuroinspired computing. ANN, including deep neural networks (DNNs), convolutional neural networks (CNNs), recurrent neural networks (RNNs), etc., turn out to be successful in logical computing, machine vision, intelligent search, and automatic driving.^[2,3] More recently, thanks to the advantages to realize synapse–neuron architecture, SNN has been increasingly emphasized as a more promising candidate for neuro-inspired computing.

In the past decade, various hardware/ software strategies have been proposed for the implementation of neuro-inspired

computing. Based on the mainstream complementary metal– oxide–semiconductor (CMOS) technology, transistor-based chips such as BrainScaleS,^[4] TrueNorth,^[5] and Pohoiki Beach^[6] have executed SNN algorithms with reasonable classification accuracy and remarkable energy efficiency. However, the Moore's law constraint, complex peripheral circuits, and difficulties in 3D integration impede the achievement of more advanced transistor-based neuro-inspired systems.

As an alternative candidate, emerging nonvolatile memories (NVMs) are found to have virtues in eliminating the energyintensive and inefficient transmission. Based on the principle that the electric-induced conductance can mimic the biological synaptic weight, NVM exhibit excellent analogue conductance regulation, i.e., continuously multilevel conductance tuning, and thus are widely employed to emulate synaptic behaviors in both ANN and SNN neuro-inspired systems. As shown in Figure 1, two-terminal NVM devices can be categorized into ferroelectric random-access memory (FeRAM), resistive RAM (RRAM), phase change RAM (PCRAM), and magnetic RAM (MRAM). The analogue conductance regulation, the energy consumption, the intradevice reliability and the interdevice uniformity are key parameters to realize a high-performance neuro-inspired system. FeRAM with tunable and multilevel conductance states show challenges in intradevice reliability and energy consumption. MRAM has good uniformity and low energy consumption but has not yet been widely implemented in neuro-inspired computing due to the challenge in realizing the analogue conductance. RRAM is a strong candidate because it has excellent properties of analogue conductance regulation, low energy consumption, and good reliability and uniformity.







Figure 1. Introduction of neuro-inspired computing. Neuro-inspired computing based on memristors with integration of storage and computation avoids data traffic, becoming a promising alternative to emulate biological synapse, neuron, and BioNN.

Therefore, RRAM-based neuro-inspired systems have been intensively studied recently.^[7] PCRAM, as another strong candidate, has been widely demonstrated in various neuro-inspired systems with ANN and SNN, due to its good conductance controllability, intradevice reliability, and interdevice uniformity, as well as its good compatibility with the mature Si-based mass production technology. Intel has announced in 2018 the commercial Optane DC Persistent Memory.^[8]

A typical PCRAM has a metal-insulator-metal sandwich structure that is similar with a biological synapse component, and its conductance can be considered the same as the connection intensity between biological synapses. In PCRAM, the temperature-driven phase transition from the crystalline state to the amorphous state of the phase change material leads to the distinguishable high conductance state and low conductance state of the device, respectively. Therefore, analogue conductance, which depends on the volume ratio of crystalline/amorphous phase, can be obtained by applying a programmed electric excitation. This process is used to emulate the weight update of the biological synapse. With the aid of peripheral circuits and algorithms, the structure of BioNN composed of billions of interconnected neurons can be directly mapped by integrating PCRAM devices into a crossbar structure and thereby the functions of ANN and SNN can be executed. However, the technology roadmap from

prototype PCRAM to large-scale application of neuro-inspired computing has not been clarified. In this review, we interpret biological fundamentals and state-of-the-art of PCRAM implementing neuro-inspired computing. Considering aspect of device, the requirements, methods, challenges, and solutions as well as perspectives of PCRAM for neuro-inspired computing will be in-depth discussed and clarified. This review is expected to provide summary and feasible technical route for PCRAM in the field of neuro-inspired computing.

This review paper is organized as follows: Section 2 provides a comprehensive description of BioNN. Section 3 presents an overview of research progress of PCRAM in neuro-inspired computing. Section 4 discusses the challenges in the implementations of neuro-inspired computing and concludes effective solutions from the aspects of material science, PCRAM cell technology, and synaptic architectures. The final section summarizes the whole paper and points out potential research directions of PCRAM in neuro-inspired computing in future.

2. Fundamentals in BioNN

BioNN consists of billions of neurons interconnected through trillions of synapses, in which signals are transmitted by active potential (just as "spike") caused by ion transport and are then stored in synapse.^[9] The strength of the connection between neurons, known as weight, is related to processing and storage of information and determines whether the post neuron is fired or not. This section introduces BioNN biodynamics in synapses and neurons, as well as the behavior of synaptic plasticity and learning rules.

2.1. Neuron

DVANCED

www.advancedsciencenews.com

The neuron is the crucial information processing and transmitting unit component of a BioNN. A neuron consists of a cyton, dendrites, and axons. The cyton is covered by a lipid bilayer membrane and is responsible for metabolism and making a "decision" based on the incoming signals. Dendrite and axon are two types of extensions of the cyton, serving as signal input and output components, respectively. Once the synapse behavior occurs, the neuron makes self-adjusting activity to incoming potentials that are filtered and integrated through dendrites. Based on integrate-and-fire (LIF) mechanism, if the sum of the potentials (excitatory and inhibitory) exceeds the threshold value, the neuron cell will be eventually fired to export an update active potential to surround neurons by axons.^[10,11]

2.2. Electrical Synapse and Chemical Synapse

The synapse connects adjacent neurons. There are two types of synapses in the biological brain: the electrical synapse and the chemical synapse. An electrical synapse is constructed by two plasma membranes with an ultranarrow cleft (2–4 nm), as shown in **Figure 2**a, being able to simultaneously provide mechanical and electrical connections and allow fast bidirectional transmission through specific gap junctions.^[12,13] The functions of electrical synapse in biology are transiting arousal states and



regulating the sensitivity of the cortex to sensation as well as controlling the level of synchronization in neural networks.^[12,14] Differently, chemical synapse is more extensive in BioNN and more important for neuro-inspired computing. As shown in Figure 2b, the configuration of a typical chemical synapse has presynapse and postsynapse cells, as well as a wider synaptic cleft. Several receptors, such as N-methyl-D-aspartic acid receptor (NMDA) and a-amino-3-hydroxy-5-methyl-4-isoxazolepropionic receptor (AMPA) selectively provide molecular membrane channels when an active potential is triggered from presynapse, allowing or preventing synaptic vesicles that packing neurotransmitters (i.e., ionic and molecular) through the presynaptic membrane. Once the synaptic behavior occurs, vesicles fuse with presynaptic membrane and release neurotransmitters into synaptic cleft. A portion of neurotransmitters spreads to postsynaptic membrane to active corresponding receptors and bind to them, which contributes to the excitatory/inhibitory postsynaptic and potential (EPSP/IPSP) depending on the nature of neurotransmitters.^[13,15] These complicated dynamics can be executed by the electrical field-driven growth of the crystalline areas of phase change materials in PCRAM (see more discussion in Section 3.3).

2.3. Synaptic Plasticity and Learning Rules

The synaptic plasticity is essential for the formation of information storage, which refers to long-term changes of synaptic efficacy such as the enhancement and the reduction of the synaptic weight (known as "synaptic potentiation" and "synaptic depression").^[16] According to the duration of the synaptic behavior, the synaptic plasticity can be divided into long-term synaptic plasticity (LTSP) and short-term synaptic plasticity (STSP). Potency of brain's learning in cellular level is essential for BioNN to reach adaptive information processing. Hebbian learning and Bienenstock–Cooper–Munro (BCM) learning are two most popular theories in neuroscience.



Figure 2. Models of synapse and synaptic plasticity. a) Configuration of electrical synapse. The bidirectional ion channel between two membranes is formed through specific gap junctions specific gap. b) The components of chemical synapse are the presynapse (source of synaptic vesicles), the postsynapse (loading receptors), and the synaptic cleft. The ion diffusion model of LTSP indicates that Ca^{2+} concentration is key factor to form LTD/ LTP during synaptic behavior. c) Experimental LTD and LTP were induced by applying the repeated 1 Hz stimulation and the 100 Hz stimulation for 1 s, respectively. Reproduced with permission.^[19] Copyright 1993, The American Association for the Advancement of Science. d) Time course of STSP that includes four phases of facilitation, depression, stimulus ceases, and post-tetanic potentiation. Reproduced with permission.^[20] Copyright 2004, Sinauer Associates.



2.3.1. Long-Term Synaptic Plasticity

LTSP was discovered in 1970s. It was found that, in the hippocampus, continuous stimulation of excited synapses results in the increment of synaptic weight lasting for hours or even days.^[16-18] The intracellular concentration of Ca²⁺, which is affected by NMDA and AMPA receptor, plays a gating role to decide the formation of long-term potentiation (LTP), long-term depression (LTD). The process of LTSP is illustrated in Figure 2b. Once the low-frequency stimulus comes, Mg²⁺ blocks the Ca²⁺ channel that coupled to NMDA receptor (NMDA channel) due to the strong polarization therefore forming the low Ca²⁺ concentration in postsynapse. The weak depolarization inside postsynapse is mainly contributed by monovalent ions like Na⁺ and K⁺ that permeated by the channel coupled to the AMPA receptor (AMPA channel), resulting in LTD. Otherwise, the postsynapse membrane is strongly depolarized to impel Mg²⁺ blocking away, as the high-frequency stimulus occurs. NMDA channel opens leading to in surge of intracellular concentration of Ca²⁺ to form LTP. In terms of hardware, a good retention of the intermediate conductance is required to achieve LTSP. PCRAM exhibits advantages in terms of retention thanks to the thermal stability of phase change materials (see more discussion in Section 3.4).

2.3.2. Short-Term Synaptic Plasticity

STSP describes the phenomenon that the transmission signal (or synaptic weight) increases first right after activation occurs,



then nearly goes back to the initial state during tens of milliseconds to a few minutes (shown in Figure 2c).^[19] Figure 2d indicates that STSP contains four phases including facilitation (STF), depression (STD), stimulus ceases, and post-tetanic potentiation (PTP).^[20] STF refers to a transient increase that happens when several active potentials consecutively stimulate a presynapse in a short interval of tens of nanoseconds. Accumulation of Ca²⁺ ions in the synaptic cleft induces more synaptic vesicles to release neurotransmitters, ultimately resulting in a larger increment of membrane potential.^[21,22] According to this mechanism, a paired pulse facilitation (PPF) based on two short pulses has been widely demonstrated in synaptic simulation applications.^[23-26] After a period of stimulus ceasing, the presynapse restores the supply of vesicles to neurotransmitters, therefore the membrane potential can be enhanced again. This is another form of PTP.^[20,27]

2.3.3. Hebbian Learning

Hebbian learning plays an important role in biological learning and memory, which is born from Hebb's postulation in 1940s that elucidates the causality between the relative activity of neurons and the modulation of synaptic weight.^[28] Nowadays, Hebbian learning is mainly associated with the so-called spike-timing-dependent plasticity (STDP) that was proposed by bioneurologists at the end of the 20th century. As shown in **Figure 3**a,b, once both neurons are stimulated, if the presynaptic spike precedes the postsynaptic spike, LTP is formed



Figure 3. Biological learning rules. a) The model of neuron system in Hebbian learning rule. b) The shape of STDP observed by Bi and Poo. Reproduced with permission.^[29] Copyright 1998, Society for Neuroscience. c) The model of signal transmission mechanism in BCM learning rule. d) BCM learning rule introduces the sliding frequency threshold θ_{m} , which automatically adjust as a function of average activity of postsynaptic neuron. Reproduced with permission.^[37] Copyright 2012, Springer Nature.





2.3.4. Bienenstock-Cooper-Munro Learning

Hebbian learning illustrates that the modulation of the synaptic weight between two neurons arises from the order and the interval time of spikes, however, one imperative concern is that how such learning can be controlled and stable. BCM learning rule proposed in 1982 is a preferable solution that considers frequency-dependent plasticity and sliding modification threshold. Figure 3c schematically depicts the signal transmission mechanism under BCM learning rule.^[37–40] Its biggest difference from Hebbian learning in transmission is that, as a response, post-synaptic neuron exports an integrated postsynaptic spike-rate not only to the next neuron and but also to every presynapse.^[37] Mathematically, as shown in Figure 3d, BCM learning rule introduces the concept of sliding frequency threshold θ_m that just likes a turning point. If $c > \theta_m$, then $\phi(c) > 0$, and synaptic weight potentiates.

Otherwise, synaptic weight depresses. In BCM learning, synaptic weight tends to be stable and controllable due to the average activity of postsynaptic neuron automatically adjusts and limits the value of $\theta_{\rm m}$.^[37] This principle is also widely known as spike



rate-dependent plasticity (SRDP), which has been extensively demonstrated using memristors in experiments.^[41,42]

2.4. Other Advanced Synaptic Plasticity

Apart from the above-discussed synaptic plasticity, some other advanced ones have also been demonstrated in biology and electronic devices. Herein, we want to highlight three significant advanced synaptic plasticity that are of great potential to accelerate the development of neuro-inspired computing, being strongly associated with the regulation of synaptic plasticity, the expansion of encoding capability of 3D connectivity, as well as man-machine interaction implementation of ANN and SNN.

2.4.1. Intrinsic Plasticity

The ion channel is generally considered as a key in transmission by chemical synapses and exhibits manifold synaptic plasticity, like LTP, LTD, and STDP, thanks to the modulation of synaptic weight. In fact, during the signals transmission, the voltage-gated channel is another ubiquitous way situated near the input and output ends of neurons and has been demonstrated to be associated with intrinsic plasticity.^[43–46] Normally, as a function of emergency receptor, the intrinsic plasticity occurs in the hippocampus, amygdala, and prefrontal cortex, when in irritations, fear, skin injury, and it originates from the reduction of active potential threshold after learning.^[46] The schematic diagram for the intrinsic plasticity is shown in **Figure 4**a. Initially, the synaptic weight is potentiated to make



Figure 4. Schematic diagrams of recent advanced plasticity. a) Intrinsic plasticity. Reproduced with permission.^[46] Copyright 2018, Elsevier Ltd. b) Metaplasticity. Reproduced with permission. Copyright 2018, The Royal Society of Chemistry.^[51] c) Structural comparison of weight plasticity and wiring plasticity. Reproduced with permission.^[55] Copyright 2004, Spring Nature.



EPSP large enough to exceed the threshold (Step 1) during learning due to the increased density of neurotransmitters and receptors. After learning, EPSP is amplified because of the regulation of dendrite channels (marked in red, Step 2), and then threshold is lowered by the hyperpolarization caused by the regulation of voltage-gated channels, resulting in a larger spike firing (Step 3). Finally, neuron is depolarized to trigger an action potential by the EPSP (Step 4).^[46] To date, intrinsic plasticity has been widely applied in the field of sensors, such as in humanoid robots, nociceptor, built by CMOS devices, or nanometer memristors.^[47–49]

2.4.2. Metaplasticity

Preserving information of incoming signals is another important function of the biological synapse. The key concern is whether such synaptic weight plasticity like LTP and LTD could stay in dynamic balance within an appropriate range, to refrain from overpotentiation and overdepression.^[39,50] Metaplasticity is proposed by Abraham to eliminate this concern. It is high-order synaptic plasticity (known as "plasticity of synaptic plasticity") and often occurs after suffering from enriched environmental, stress events, visual stimuli, and so on.[39] An example of metaplasticity is illustrated in Figure 4b.^[51] It is clear that with the same plasticity-inducing stimulus, the synaptic response weakens once a priming stimulus is introduced before the plasticity-inducing stimulus (shown in the bottom panel), as compared to normal synaptic plasticity shown in the top panel. In recent years, metaplasticity also has been highly valued in the field of neuro-inspired computing using nanodevices.^[51-54] Typically, using a typical bismuth-based memristor, Mazur et al. verified that SRDP and STDP can be further modulated via metaplasticity to produce an amplification of synaptic weight.^[52]

2.4.3. Wiring Plasticity

Apart from the weight plasticity that illustrates the modification of connection strength in a given neuron system (wiring diagram is unchanged), the wiring plasticity that is mediated by the connectivity and structural alterations in spines, dendrites, and axons should also be highlighted. Evidences indicate that wiring plasticity not only partly affects the storage capacity of brain, but also is beneficial to the extension of advanced learning, such as perceptual learning, motor learning, and spatial learning. For example, rewiring diagram in sparse networks could dramatically improve the ability of encode learned information.^[55–57] The concept of wiring plasticity can be understood by considering a simple comparison shown in Figure 4c. Differing from weight plasticity with unchanged structure, the wiring diagram transforms when the system experiences wiring plasticity. However, the mechanism behind wiring plasticity is still unknown due to the underdeveloped imaging technology, which is insufficient to provide subcellular visualization of neural activities and morphological changes in brain. There is only an accepted speculation that there should be LTP-like and LTD-like mechanism to modify the formation or deletion



of the wiring plasticity. More detailed discussions about wiring plasticity are available in review by Chklovskii et al.^[55]

This plasticity is believed to be essential for the neuroinspired computing and has attracted intensive efforts in hardware implementation. The intrinsic characteristics and operation mechanism of different NVM devices determine their applications in realizing different plasticity. For example, LIF mechanism can be equivalent to the threshold effect of the (amorphous to crystalline) crystallization process in PCRAM. The characteristic conductance attenuation of RRAM makes it suitable for the realization of STSP, in which the rupture of the conductive filament results in the reduction of conductance in milliseconds or even nanoseconds. By contrast, PCRAM presents some disadvantages in STSP due to the nonspontaneous amorphization process. The STSP may be achieved by PCRAM only with the aid of programmed pulse excitations. Intrinsic plasticity, metaplasticity, wiring plasticity, and other advanced plasticity are important for high-performance neuroinspired computing. The state-of-the-art of PCRAM hardware applied to neuro-inspired computing will be presented in detail in Section 3.

3. Overview of Neuro-Inspired Computing Using PCRAM Technology

According to the dissection of BioNN, the essential tasks of neuro-inspired computing are mimicking fundamental synapses, neurons and their synaptic behaviors using hardware technology. Over decades, lots of implementations of neuroinspired computing based on PCRAM technology have been reported. In this section, we comprehensively discuss the implementation of neuro-inspired computing using PCRAM, including the fundamental electric-induced conductance mechanism, and advanced schemes to emulate biological components and behavior as well as the state-of-the-art in intelligent applications based on PCRAM integrated array.

3.1. Electric-Induced Conductance Controllability

Corresponding to the principles of biological synaptic behavior, the key precondition of implementing BioNN using hardware is the continuous regulation of conductance. The feasibility of PCRAM originates from the electric-induced controllable phase change occurred at the active region. As shown in Figure 5, crystalline and amorphous states in the active area can be bilaterally and continuously controlled by applying appropriate electrical excitation. The process of crystalline-to-amorphous change with prompt quenching is induced by high and narrow pulses, which equals to the process of synaptic depression (marked in dark blue). While the reverse process simulating synaptic potentiation (marked in dark red) is a thermal accumulation and requires long and moderate heating, which normally is carried out by applying lower and wider pulse. Consequently, with special programming pulses, PCRAM performs reliable bidirectional electric-induced conductance controllability, that is, multilevel reduced conductance and the cumulative enhanced conductance.[58-62]







Figure 5. Bidirectional electric-induced conductance controllability for synaptic simulation. Normally, synaptic potentiation is obtained by lower and wider pulse and synaptic depression is achieved using higher and narrower pulse.

3.2. PCRAM Neuron

The neuron dominates information transmission through the significant function of LIF mechanism in BioNN. LIF mechanism is driven by complex electrochemical mechanisms in conjunction with the feature of lipid-bilaver membrane, according Hodgkin-Huxley model and various threshold-based neuronal models.^[63-65] Membrane potential is regulated by stochastic incoming excitatory and inhibitory postsynaptic potentials from dendrites. It leads to fired neuron to export new potential via axons once the sum of potentials is high enough to exceed firing threshold.^[66] The idea of emulating artificial neuron is realizing dynamic updating of membrane potential using suitable hardware design. The electric-induced transformation in PCRAM with conductance threshold directly expresses the evolution of biological membrane potential. Figure 6a presents a typical stochastic PCRAM neuron system proposed by IBM team, which comprises dendrites (stochastic inputs), cyton (which performs function of integrate-and-fire event), and axons (output). The modification of conductance by pulses emulates the LIF mechanism in biological neuron, as shown in Figure 6b.^[66]

Thanks to the exploitation of the stochasticity and nonvolatility, this PCRAM neuron meets well the two requirements for neuroinspired computing, i.e., robustness and low energy. However, this comes at the expense of limited control of neuronal dynamics with minimal circuit requirements, because the intrinsic stochasticity of PCRAM is derived from physical crystallization. Further efforts may focus on using smaller nodes for more precise tuning of crystallization, and on more comprehensive design of accessory devices, peripheral circuits, and algorithms.

3.3. PCRAM Synapse

Electronic synapse is another crucial component to emulate biological behaviors. In practice, schemes of single PCRAM and 2-PCRAM per synapse are commonly employed for neuroinspired integrated circuits to simulate the potentiation and the depression. The single PCRAM scheme corresponds to bidirectional electric-induced conductance was described in Section 3.1. The disadvantage is that the subsequent reset pulse destroys the inherent state during amorphization. This means that the stored information is instantly forgot and has to be relearned. For the latter, the potentiation and the depression are implemented using "positive device" and "negative device," respectively, both of which exploit cumulativity in crystallization. The final synaptic weight can be expressed by differential conductance of two PCRAMs. This approach avoids using reset pulse to improve continuous value of weights but needs to periodically recover conductance to prevent saturation of positive and negative conductance. 2-PCRAM scheme has been widely employed for the construction of PCRAM-based neuro-inspired computing, although it comes at the cost of increasing complexity in design as compared to single PCRAM scheme.^[67,68]

3.4. PCRAM Synaptic Plasticity

Emulations of synaptic structure and synaptic plasticity are essential tasks for the realization of BioNN. However, the complex dynamic electrochemical models of synaptic plasticity make them be often necessary to be simplified into







Figure 6. PCRAM neuronal system and synaptic simulation. a) Schematics of PCRAM electronic neuron and b) corresponding update of conductance to mimic LIF rule in biological neuron. Reproduced with permission.^[66] Copyright 2016, Spring Nature. c,d) Four forms of STDP are simulated by regulating the intervals and amplitudes of programmable staircase pulse scheme in presynaptic spike. Reproduced with permission.^[6] Copyright 2011, American Chemical Society.

computation models for the emulation. Among the proven synaptic plasticity, synaptic potentiation and depression, as well as STDP are the most desired and emphasized in neuroinspired computing. PCRAM with a two-terminal structure allows these and has the advantage of structural similarity to biological synapse and bidirectional controllable conductance, and thus has been widely studied.^[35,69–71] Synaptic potentiation can be achieved using a uniform pulse train or a staircase pulse train comprising a number of wider pulses whose amplitude is below the Set voltage, while synaptic depression is achieved by staircase pulse train comprising a series of narrower pulses whose amplitude is slightly higher than Reset voltage.

For STDP, the programmable staircase pulse scheme and the square pulse scheme are the most popular.^[35,36,72-76] In the former approach, as shown in Figure 6c, the presynaptic spike consists of depression pulses with increasing amplitudes following potentiation pulses with decreasing amplitudes, whereas the postsynaptic spike only consists of a single and wider pulse. It is noticed that both amplitudes of depression pulses and potentiation pulses are initially below the corresponding threshold, which means that any pulse in presynaptic spike is not able to depress or potentiate the weight unless it overlaps the postsynaptic spike. Therefore, postsynaptic spike acts like a gate to control the synaptic weight to be increased or decreased, causing LTP or LTD, respectively. The net of arrival times of presynaptic spike and postsynaptic spike is defined as the spike timing (ΔT), and the net of the strength of two spikes is represented by the change of synaptic weight (ΔW). Thus, the correlation between time and

synaptic weight can be shown in Figure 6c, which is quite similar as the result reported by Bi and Poo for biological STDP rule. Furthermore, as shown in Figure 6d, the so-called four popular forms of STDP learning rules in biosome including asymmetric Hebbian, asymmetric anti-Hebbian, symmetric Hebbian, and symmetric anti-Hebbian, are obtained by regulating the intervals and amplitudes of presynaptic spike.^[36] In the latter approach, i.e., the square pulse scheme, pairs of mutual enhancing square pulse and mutual offsetting pulse are used to implement various STDP due to their perfect control of temperature in phase change area. It is more concise and has higher efficiency because two spikes contribute together to the regulation of synaptic weight, and may be easier to practice in large-scale integration circuits compared to the staircase pulses scheme due to the simple designs of square pulses. Nevertheless, the biological similarity of STDP achieved by square pulse scheme needs to be further improved and demonstrated, and thus it has not yet been widely used in practice.^[76]

The accumulative and controllable crystallization process makes it possible for PCRAM to achieve hardware neurons and synapses and to realize synaptic plasticity. The drawbacks of high-energy consumption and burst amorphization can possibly be overcome by optimizing the synapse architectures, circuits, and algorithms, although it is at the expense of increased system complexity. Furthermore, as a key figure of merit for storage application, high phase changing speed has been pursued in the past decades, which is in contrast to the requirement of the continuous multilevel conductance response in neuro-inspired computing. Improving the phase change controllability through material engineering may be considered as ADVANCED SCIENCE NEWS _____ www.advancedsciencenews.com



an alternative approach to simplify the circuits and minimize the system requirements.

3.5. Implementations of Neuro-Inspired Computing Using PCRAM Integrated Array

The implementation of hardware SNN using integrated synaptic devices array is essential to achieve neuro-inspired computing. In this section, we discuss fundamentals in PCRAM integration architecture and its applications in neuroinspired computing in both supervised learning and unsupervised learning manners.

3.5.1. PCRAM Integration Architecture

The powerful PCRAM-based SNN can be built layer by layer on integrated memristors structure by introducing the dense crossbar array structure and the 3D integration technology, as illustrated in Figure 7a,d, respectively.^[67,77] However, the sneak current as interpreted in Figure 7c is a serious challenge that may lead to confusion of high and low resistance devices, resulting in wrong interpretation of the storage bit.^[78] The selector is an effective component to cope with this problem. A variety of selectors have been developed, such as Si-based devices (i.e., threeterminal transistor and Si PN diode), oxide PN junction diodes, threshold switch devices (i.e., ovonic threshold switching (OTS) and threshold vacuum switching devices), as well as other novel devices.^[79-85] Transistor and OTS are widely accepted in PCRAM integration with configurations of 1T1R or 2T1R (in Figure 7e)^[85] and OTS-PCRAM (in Figure 7d),^[81] respectively, thanks to their good CMOS compatibility.

3.5.2. Learning Rules in Neuro-Inspired Computing

In terms of machine learning, neuron networks are trained either indirectly or directly, corresponding to supervised learning and unsupervised learning, respectively. The former manner requires training process to establish relation between inputs and outputs, and emphasizes the gradient descent-based error backpropagation algorithms.^[3,67] Supervised learning system usually takes thousands of training and thousands of labeled examples.^[3] For example, the famous MNIST contains 60 000 training samples. Many significant applications in the field of neuro-inspired computing, particularly in image classification and identification, have been successfully implemented by SNN supervised learning.^[60,67,85–89]

However, biological behaviors are more similar to unsupervised learning. Human beings or animals understand and create novelties by virtue of initiative learning from observations in practice rather than labeled training, although human experiences like labeled learning process in the youth period, for example, identifications of fruits, animals, and cars. Unsupervised learning with STDP requires underlining adaptively revealing, summarizing and analyzing latent connections and similarities in samples rather than onerous labeled training. In the BioNN topology, multiple presynaptic neurons are connected to a postsynaptic neuron, in accordance with the survival of the fittest, but only the strongest fired presynaptic neuron enables to transmitting information. In order to mimic this adaptive competition, unsupervised learning induces a winnertakes-all mechanism to screen out the winning neuron among all neurons that experience LIF mechanism.^[68] It is believed to be more promising to carry out adaptive tasks in the long term compared to supervised learning despite as the lightly lower performance than that of supervised learning.



Figure 7. 3D integration architecture of PCRAM. a) Schematic of multilayer perceptron and corresponding crossbar array designed by Burr et al. In this architecture, each subcell contains one selector and one PCRAM to address the sneak current issue. Reproduced with permission.^[67] Copyright 2014, IEEE. b) 3D integration schemes. Model 1: Stacked 3D horizontal crosspoint array. Model 2: 3D vertical crosspoint array. Reproduced with permission.^[77] Copyright 2016, IEEE. c) Interpretation of sneak path. Supposing that the targeting addressed unit in the center of the crossbar array is in the high resistance state (HRS) (marked in red) while surrounding units are in the low resistance state (LRS) (marked in yellow). Read current (marked in pink) may act on other devices (*I*_{sneak}, marked in brown) as it flows through the target device. d) Microstructure characterization of an OTS-PCM cell and the corresponding fully integrated array. Reproduced with permission.^[81] Copyright 2009, IEEE. e) TEM image of PCRAM-based 2T-1R configuration. Reproduced with permission.^[85] Copyright 2015, IEEE.





3.5.3. Neuro-Inspired Computing Networks Using PCRAM Hardware

PCRAM ANN: DNN, RNN, and CNN characterized by multiple iterations appear to be attractive to the communities of machine-learning, computer-vision, and speech-recognition, which, in turn, has incited numerous studies on the PCRAM hardware implementations. A fully connected multiple architecture is needed to map topological neuron networks. This can be achieved by integrating PCRAM synapses/neurons and combining the designs in selector components and synapse architecture. Then, hardware DNN (Figure 8a),^[90] RNN (Figure 8b),^[91] and CNN (Figure 8c)^[92] are created after training using such models as forward propagation, backward propagation, and Hopfield algorithms. Burr et al. proposed a large-scale 3-layer DNN hardware (containing 164 885 PCRAM synapses) and achieved a training accuracy of 82.2% using a 2-PCRAM synaptic architecture and backward propagation.^[67] As shown in Figure 8b, a Hopfield RNN used as an

accelerator was mapped by fully connected PCRAM synapses and neurons. $\ensuremath{^{[91]}}$

PCRAM SNN: IBM performs several pioneering works in PCRAM hardware SNN. In 2017, the team demonstrated spike-excited encoding information and supervised learning using multilevel cell (MLC) PCRAM technology along with an efficient comprehensive model.^[60] Most recently, a typical 132 × 168 PCRAM-SNN with supervised training was validated for high-accuracy speech recognition.^[93] Furthermore, unsupervised learning PCRAM hardware networks has progressed in the aspects of digit recognition, image recordings, spatiotemporal patterns learning, etc.^[64,94–98] Typically, using a 10 × 10 2D PCRAM SNN based on the Hopfield network, Eryilmaz et al. successfully achieved brain-like associative learning and pattern recognition by increasing the number of epochs of weight update.^[98]

PCRAM-based neuro-inspired networks have been demonstrated in experiments, however, more efforts are required for the large-scale applications and mass production. Low



Figure 8. PCRAM hardware neuron networks. a) DNN. Reproduced with permission.^[90] Copyright 2018, The Author(s). b) RNN.^[91] c) CNN.^[92] d) SNN.^[93] e) The training of supervised learning SNN. The audio signal of characters "IBM" (Eye..Bee..Em) was captured and then converted into 132 spike streams that were encoded in designed SNN. After supervised training, the objective images ("I," "B," and "M") can be recognized with high accuracy. Reproduced with permission.^[93] Copyright 2020, The Author(s).





intradevice and interdevice reliability and low-density integration are still problematic for high-accuracy recognition of PCRAM ANN. In addition, poor understanding of the principles of SNN algorithmic limits the development and implementation of its hardware. More studies on algorithms, circuits, synaptic architectures, and devices are urgently required to overcome the difficulties in PCRAM SNN.

4. Challenges and Solutions

Despite considerable advantages in neuro-inspired computing using PCRAM by booming neuroscience knowledge and mature large-scale integration technology, there are still some unsolved obstacles in aspects of devices, systems, and algorithms,^[90,92,99–104] which pose challenges to make further achievements in higher-level intelligent applications. We summarize here the challenges and solutions in terms of material engineering, programming stimulus, device technology, preparation technology, synaptic architecture engineering, as well as programming algorithms and circuits.

4.1. Reliability, Energy Consumption, and Multilevel Conductance

High reliability, low energy consumption and multilevel conductance are basic device requirements of PCRAM for an energy-efficient and high-performance neuro-inspired computing hardware. Device reliability primarily involves the stable write–erase operation, speed, retention, and endurance. Poor reliability of PCRAM normally results from the poor thermal stability and the unstable atomic rearrangement in active area after crystallization or amorphization. Energy consumption is a key concern for neuro-inspired computing hardware, which mainly results from the high-powered Reset operation due to the high melting point of phase change materials and is related to the power consumption of selective components in integration hardware. The capability of multilevel conductance change is associated with the continuous controllability of conductance for realizing reliable synaptic simulation.

Material engineering is beneficial for high crystallization temperatures, grain refinement, and stable lattice constant, which has played an essential role in these basic evaluations. It has been reported that PCRAMs based on Ga-Sb-Ge,^[105,106] Ge-Sb-Te (GST),^[107] are able to reach a high endurance of 10¹¹ cycles and a retention of more than 10 years. In addition, doping engineering leads to the suppression of nucleationseeds and the increase of defects, resulting in the slow and controllable crystallization. For example, C-doped GST,^[108] N-doped GST.^[109,110] O-doped Ti-Sb-Te,^[71] etc., were demonstrated to have the controllable multilevel conductance and good device reliability for neuro-inspired computing. Low energy consumption can also be achieved by optimizing the material composition to reduce melting point, [111] embedding 2D material as thermal barrier,^[112] as well as employing new materials like graphene and carbon nanotubes as electrodes.^[113,114]

Interface engineering, device structure design, and encapsulating are also employed to improve the storage reliability and synaptic performances. The nonconfined structure is the most appealing PCRAM structure for large-scale integrated device fabrication^[115] thanks to its easy doping and interface engineering as well as the low cost. The strategy using interfacial layer to impact the activation energies and bonds (as shown in **Figure 9**a) was widely accepted to reduce the energy consumption and increase the number of intermediate states of PCRAM.^[116,117] The design of GeTe/Sb₂Te₃ interface is helpful to achieve the low-energy consumption and the high reliability of write–erase.^[118] Moreover, it has indicated that stacks consisting of alloys with distinct crystallization behaviors, as named as "superlattice-like," show the low thermal conductivity, the limited active area, and the low heat dissipation as well as the formation of bond at interface as



Figure 9. PCRAM cell technology for enhancing performances in neuro-inspired computing. a) HfO₂ interface layer. Reproduced with permission.^[117] Copyright 2012, IEEE b) Metallic surfactant layer scheme in a confined PCRAM. Adapted with permission.^[123] Copyright 2013, IEEE. c) Elevated-confined structure. Reproduced with permission.^[126] Copyright 2010, The Japan Society of Applied Physics. d) PCH structure. Reproduced with permission.^[141] Copyright 2019, The American Association for the Advancement of Science. e) "Projected" PCRAM. Reproduced with permission.^[142] Copyright 2015, Macmillan Publishers Limited. f) Encapsulating schemes. Reproduced with permission.^[145] Copyright 2006, IEEE.



a barrier (i.e., TiN/W,^[119] GeTe/Sb₂Te₃,^[120] N-GST/GST,^[121] and Ti_{0.43}Sb₂Te₃/TiN^[122]), therefore significantly contributes to the reduced Reset voltage and higher device reliability. The confined cell design is the other practical structure (in Figure 9b), in which the phase change material is located in a hole.^[123] This structure was also suggested due to its advantages including failure avoiding, small footprint, limited active area, high reliability, and lower power consumption.^[61,123–125] A derivative design of elevated-confined structure (Figure 9c) has been demonstrated to provide effective thermal confinement to reduce the programming power.^[126]

In addition, the deposition techniques can ultimately determine the reliability and lifetime of prototype devices. For example, physical vapor deposition (PVD) technique is the most suitable method for large-scale integrated devices fabrication.^[115] However, the drawbacks like elemental segregation and void formation in active area threat the reliability of nonconfined PCRAM. Advanced deposition techniques such as atomic layer deposition, ion beam deposition, and sputtering could realize the high-quality film deposition but at the expense of high-cost and poor efficiency.^[127,128] A detailed discussion of deposition technology for PCRAM has been well-reviewed by Burr et al.^[115]

4.2. Nonlinear and Asymmetric Conductance Response

For nonvolatile memory implementation SNN, synaptic weights are referred to the conductance of devices. Linear and symmetric conductance response (conductance increases and decreases) are expected to achieve high-precision comparable to conventional computer-science-oriented ANN that contains weight matrix initialized by the mathematic model. The key requirement is the realization of the microcontrol of conductance. However, it is difficult due to the fast phase transition and unique asymmetric switching mechanism in PCRAM, that is, accumulation in Set and abruption in Reset. For PCRAM synapse, only the limited range with relatively linear and controllable conductance response can currently be achieved, resulting in strong degradation of accuracy.^[67]

Material engineering plays an essential role in slowing crystallization to improve the symmetry of electrical characteristic of PCRAM. For example, C dopant has been demonstrated to make the disorder of Ge–Te tetrahedral in GST thus retarding the formation of crystal grains.^[108] The O-doped Ti–Sb–Te performs a linear resistance modulation under identical pulses.^[71] These demonstrations perform the good potential of regulating conductance for synaptic simulation.

Programing stimulus engineering, such as programmable staircase pulse scheme^[36] and the square pulse scheme,^[76] has been proved to be an effective approach to improve linearity and symmetry of conductance response, even if material engineering sometime fails to meet expectations. However, it is increasingly reaching the bottleneck due to the imperfect devices. More efforts should focus on material engineering to improve phase change controllability and to reduce the complexity in programing stimulus engineering. Indeed, a synergistic approach of combined material engineering and programming engineering should be adopted.



Synaptic architecture engineering with the specific algorithm circuit is also widely used in neuro-inspired computing to circumvent tough challenges arising from electronic synapse. Analog PCRAM synapse and binary PCRAM synapse are basic synaptic architectures.^[129] The 2-PCRAM architecture described in Section 3.3, with differential circuits, is an available analog architecture that requires PCRAM itself to provide electric-induced conductance controllability. It has low power consumption and permits eliminating effects of asymmetric conductance response, because the update of synaptic weight is always realized in the crystallization process.^[68,130] The binary PCRAM synapse is driven by a crucial probabilistic rule rather than an electric-induced conductance controllability. It only employs binary representation of PCRAM (only HRS and LRS), in principle, which circumvents the issue of nonlinear and asymmetric conductance of PCRAM.^[131] At present, various probabilistic update schemes, such as fine-tuned probabilistic switching,^[132] pseudorandom number generators,^[129] and counter-based arbitration scheme,^[90] have been proposed both in supervised learning and unsupervised learning applications.

4.3. Intradevice and Interdevice Variabilities

Variability is a key obstacle for large-scale neuro-inspired computing using PCRAM technology and has been paid extensive attention for a long time. Generally, the variability occurs in both intradevice and interdevice.^[90] Both intradevice variability and interdevice variability in PCRAM restrict the accuracy of SNN, although it has tolerance to some extent for initial variations and is able to become more robust by increasing training epochs. However, it comes at the expense of undesired training complexity and increasing the power consumption.^[98]

Intradevice variability is believed to derive from inherent stochasticity in PCRAM. It is mainly because of the high atomic mobility and phase segregation in the molten state.^[101] It should be strictly avoided in implementing neuro-inspired computing as it may increase complexity of training and reduce system accuracy. Intradevice variability can be significantly relieved in general by high-thermal-stability composition like C-doped Sb-rich GST,^[133] N-doped Sb films,^[134] Mo-doped SbTe,^[135] etc. In addition, the encapsulating of device and the shielding of operation environment are friendly to reduce testing noises for the acquisition of low-variability data. Interdevice variability presents device-to-device differences in conductance response in the PCRAM array, which possibly originates from the poor consistency during film deposition. Furthermore, as IBM reported, synaptic architecture engineering like multi-PCRAM synapse together with iterative programming differential algorithms and circuits are necessary to further reduce both intradevice variability and interdevice variability in PCRAM integrated array.[136-138]

4.4. Resistance Drift

Resistance drift is a unique challenge in PCRAM. It refers to the phenomenon that the value of resistance spontaneously increases over time may due to the structural relaxation and



the increased activation energy for conduction. Such phenomenon is a major concern in HRS of amorphization while recent reports indicate that it also occurs in LRS of crystallization process.^[100,104] The slight resistance drift can be balanced with increasing training epochs and may facilitate the classification accuracy of SNN. However, it is dramatically happened when a pretrained SNN is used to identify incoming patterns without synaptic weight updating.^[92,103]

Some reports have verified resistance drift seems to be mitigated by material engineering. For example, N-doped Ge-rich GST^[139] or Ti–Sb–Te system.^[140] Indeed, an effective route is believed a comprehensive and systemic scheme that involves considerations of device structure, programming algorithms, and circuits.

From the device design point of view, the phase change heterostructure (PCH) (in Figure 9d) with a superlattice design of alternately stacked Sb₂Te₃/TiTe₂ effectively suppresses compositional and structural variability performs excellent immunity to noise and resistance drift.^[141] The specific thin conducting surfactant layers, serving as a resistance modulation component in amorphous state, have been widely verified to relieve the resistance drift in the confined structure and the "Projected" structure (in Figure 9e).^[59,123,142,143] Recently, a pair of confined PCRAM with a thin metallic liner as a synaptic element was demonstrated by IBM yielding a high test accuracy of 95% in MNIST simulation.^[144] The design of encapsulating layer (in Figure 9f) using SiO₂,^[145] TiN, or Al₂O₃, whose biaxial moduli is much different to that of the phase change materials, is demonstrated to block oxygen penetration and mitigate the resistance drift.^[145–148]

Recently, a number of advanced systematic R-drift mitigation approaches, such as reference-cell-based resistance tracking,^[149] DRAM-like refresh resistance drift,^[150] resistance drift compensation (RDC) scheme,^[151] and R-SET technique,^[139] have been verified by IBM, Samsung Electronics, Macronix, and CEA-LETI, respectively. These approaches have been successfully demonstrated in the application of multilevel cell PCRAM as storage, and are serving for high-precision neuro-inspired computing.

4.5. Nondegenerate Conductance

The characteristic of nondegenerate conductance, which means the conductance cannot decay naturally in a short time (i.e., tens of nanoseconds), is remarkable for PCRAM synapse due to the relatively stable rearrangements of atoms after electrical stimulation. It leads to the disadvantages of PCRAM synapse in short-term-related plasticity like STF, STD, PPF, and metaplasticity as compared to other RAMs that are driven by the migration and diffusion of charged ions.^[49,152–154] as well as ferroelectric polarization dynamics.[155,156] Thanks to the electric-induced conductance controllability for PCRAM, programming engineering can be viewed as a promising solution to overcome this issue. In addition, the inherent characteristic of resistance drift in PCRAM is a good representation of longterm degenerate conductance. It is anticipated that regulating the rate of resistance drift by material engineering, circuit compensation and programmable engineering is possible to achieve short-term conductance behavior.

4.6. Density

A high density is necessary for an energy-efficient and reliable PCRAM integration. As the developments of preparation techniques and new materials, the effective transformation region of PCRAM is shrinking and a ≈5 nm² contact area in a discrete PCRAM has been demonstrated using a carbon-nanotube electrode.^[157,158] However, as a key component to eliminate the sneak path issue in arrays, the transistor-based selector in industry always limits the chip density due to the lager demission of channel as compared to nanometer scale PCRAM. The emerging selector like OTS, and diode-based switch devices^[79-85] still need to overcome the issues of insufficient stability and preparation technology to mass production. Furthermore, the increase of throughput of neuro-inspired computing increasingly poses challenges in high-density and miniaturization of 3D hardware integration. As the number of layer increases, the conventional 3D vertical approaches like 3D stack with multiple layers of 2D crossbars^[159] and 3D vertical arrays using pillar vertical electrodes,^[160-163] normally forming a staircase interconnect outside the 3D array to CMOS layer, will be failure due to the increase of wire resistance and floor plan contributed by interconnect. The 4D address topology based on 3D CMOL (CMOS+Molecular) architecture,^[164] allowing CMOS circuits inside the 3D array, is a potential route to enhance ultrahigh density integration.

5. Conclusions and Perspectives

In conclusion, we have presented an overview of fundamentals in biological nervous system including biological compositions, plasticity (LTSP, STSP, STDP, intrinsic plasticity, metaplasticity, wiring plasticity, etc.), learning rules (Hebbian learning, BCM learning) for possible bridging the gap between neuro-inspired computing and PCRAM technology. Recent advances including principles and applications in neuro-inspired computing implemented by PCRAM have been comprehensively retrospected. PCRAM technique is capable to simulate biological neuron and synapse, Hebbian-based plasticity and is competent in fulfilling small-scale neuro-inspired computing tasks with ANN and SNN, such as MNIST digit recognition, speech identification, in manners of both unsupervised learning and supervised learning.

PCRAM technology is a very promising candidate to achieve the neuro-inspired computing. In the future, following perspectives can be predicted for PCRAM-driven neuro-inspired computing:

- 1. Explore the potentials of PCRAM to achieve higher-order plasticity such as intrinsic plasticity, metaplasticity, and wiring plasticity that are anticipated to intensify intellectual learning and promote the development of neuro-inspired computing. Meanwhile, occurrence of excessive simulation of biological synaptic plasticity should be avoided.
- 2. The mechanisms of neuro-inspired computing are still not well understood, at present, and the practical system capable of massive assignments are still lacking. We believe that the accommodation between ANN and SNN that combining the advantages of high precision, high data throughput, high processing speed, and low power consumption is a promising tradeoff to



solve complex tasks.^[165–167] The compatible system hierarchy allowing free communication between two paradigms in information representation, computing paradigm, weight updating, and storage architecture should be built. In addition, the high energy-efficiency and simplification should be considered in the future hybrid platform construction.

- 3. Innovations in material optimization and device technology are still an essential path to obtain high-density, energy-efficient and high-performance device. New material systems providing retardative and controllable phase transition and further shrinkage technology are supposed to be emphasized in future studies. On the other hand, we should be aware of potentials of algorithms for amending inherent flaws of PCRAM. The route of algorithm-hardware co-design is believed to be able to address variability and drift of PCRAM. In addition, researchers need to pay extra attention to selector devices that account for the vast majority of the energy consumption. They severely hamper high-density integration due to the relatively larger size as compared to memory devices. The miniaturization of existing selectors using transistor, diodes, OTS, etc., should be further investigated. Emerging self-selective techniques and some novel selector schemes need to be developed.
- 4. In view of the intricate challenges of PCRAM synaptic device, we deem synaptic architecture is an effective shortcut to evade nonlinear and asymmetric conductance response, as well as eliminate resistance drift and variations. Although a number of successful PCRAM synapse architectures have been demonstrated, the improvement of networks' ability is at the expense of increase in the number of devices per synapse, higher complexity, and higher power consumption. Furthering investigations on synaptic architecture may consider to embed multilevel PCRAM devices to balance complicated circuit configuration.

Finally, neuro-inspired computing is a systematic project involving disciplines of materials science, devices design, fabrication technologies, synaptic architectures, circuits, algorithms, and neuroscience. It has been driven by PCRAM technology to harvest preliminary benefits in energy-efficient nonideological intelligence. Now is the time to integrate crossdisciplinary efforts to realize the prospect of ideological and initiative AI.

Acknowledgements

The authors acknowledge the funding support from the Key R&D Program of Shaanxi Province of China (2020GY-271 and 2018ZDXM-GY-150), the Fundamental Research Funds for the Central Universities (xjj2018016), the "111 Project" of China (B14040), the Open Project of State Key Laboratory of Electronic Thin Films and Integrated Devices (KFJJ201902), the Open Project of State Key Laboratory of Information Functional Materials (SKL-201908), the Natural Sciences and Engineering Research Council of Canada (NSERC, Discovery Grant No. RCPIN-2017-06915), and the National Natural Science Foundation of China (91964204).

Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

G.N., W.R., and Z.T.S. supervised the project. Q.W., G.N., and S.N.S. designed the framework of review. Q.W. and R.W. contributed to collection of literatures. X.G.C., X.L., Z.-G.Y., Y.-H. X., and S.N.S. contributed to discussion and revision of review. Q.W. and G.N. drew the illustration figures and cowrote the paper. All authors discussed and gave approval to the final version.

Keywords

electronic synapses, neuro-inspired computing, nonvolatile memristors, phase change random access memory

Received: December 17, 2020 Revised: February 10, 2021 Published online:

- [1] A. M. Turing, Mind 1950, 236, 433.
- [2] G. E. Hinton, R. R. Salakhutdinov, Science 2006, 313, 504.
- [3] Y. LeCun, Y. Bengio, G. Hinton, Nature 2015, 521, 436.
- [4] S. Schmitt, J. Klaehn, G. Bellec, A. Gruebl, M. Guettler, A. Hartel, S. Hartmann, D. Husmann, K. Husmann, V. Karasenko, in 2017 Int. Joint Conf. on Neural Networks (IJCNN), IEEE, Piscataway, NJ 2017.
- [5] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S. K. Esser, R. Appuswamy, B. Taba, A. Amir, M. D. Flickner, W. P. Risk, R. Manohar, D. S. Modha, *Science* **2014**, *345*, 668.
- [6] R. Uhlig, Intel's Pohoiki Beach, https://newsroom.intel.com/ news/intels-pohoiki-beach-64-chip-euromorphic-system-deliversbreakthrough-results-research-tests/#gs.7ck8tt (accessed: July 2019).
- [7] W. Zhang, B. Gao, J. Tang, P. Yao, S. Yu, M.-F. Chang, H.-J. Yoo, H. Qian, H. Wu, Nat. Electron. 2020, 3, 371.
- [8] Y. Wu, K. Park, R. Sen, B. Kroth, J. Do, in DaMoN '20: Proc. of the 16th Int. Workshop on Data Management on New Hardware, ACM, New York 2020.
- [9] K. Roy, A. Jaiswal, P. Panda, *Nature* **2019**, *575*, 607.
- [10] D. Bucher, J. M. Goaillard, Prog. Neurobiol. 2011, 94, 307.
- [11] C. Grienberger, X. W. Chen, A. Konnerth, *Trends Neurosci.* 2015, 38, 45.
- [12] S. Koner, J. S. Najem, M. S. Hasan, S. A. Sarles, Nanoscale 2019, 11, 18640.
- [13] V. L. Tawfik, P. Flood, Anesthesiology 2016, 124, 13.
- [14] J. S. Haas, B. Zavala, C. E. Landisman, Science 2011, 334, 389.
- [15] C. Zamarreño-Ramos, L. A. Camuñas-Mesa, J. A. Pérez-Carrasco, T. Masquelier, T. Serrano-Gotarredona, B. Linares-Barranco, Front. Neurosci. 2011, 5, 26.
- [16] R. C. Malenka, R. A. Nicoll, Science 1999, 285, 1870.
- [17] T. V. P. Bliss, A. R. Gardner-Medwin, J. Physiol. 1973, 232, 357.
- [18] T. V. P. Bliss, A. R. Gardner-Medwin, J. Physiol. 1971, 216, 32.
- [19] R. M. Mulkey, C. E. Herron, R. C. Malenka, Science 1993, 261, 1051.
- [20] D. Purves, G. J. Augustine, D. Fitzpatrick, W. C. Hall, A.-S. LaMantia, J. O. McNamara, S. M. Williams, *Neuroscience*, 3rd ed., Sinauer Associates, Inc., Sunderland, MA 2004.
- [21] J. Tang, F. Yuan, X. Shen, Z. Wang, M. Rao, Y. He, Y. Sun, X. Li, W. Zhang, Y. Li, B. Gao, H. Qian, G. Bi, S. Song, J. J. Yang, H. Wu, *Adv. Mater.* **2019**, *31*, 1902761.
- [22] N. K. Upadhyay, S. Joshi, J. J. Yang, Sci. China Inf. Sci. 2016, 59, 061404.
- [23] J. Jiang, J. Guo, X. Wan, Y. Yang, H. Xie, D. Niu, J. Yang, J. He, Y. Gao, Q. Wan, Small 2017, 13, 1700933.

ADVANCED SCIENCE NEWS

www.advancedsciencenews.com

- [24] G. Wu, P. Feng, X. Wan, L. Zhu, Y. Shi, Q. Wan, Sci. Rep. 2016, 6, 23578.
- [25] G. Gou, J. Sun, C. Qian, Y. He, L. A. Kong, Y. Fu, G. Dai, J. Yanga, Y. Gao, J. Mater. Chem. C 2016, 4, 11110.
- [26] W. Xu, H. Cho, Y. H. Kim, Y. T. Kim, C. Wolf, C. G. Park, T. W. Lee, Adv. Mater. 2016, 28, 5916.
- [27] L. Wang, R. Lu, J. Wen, Nanoscale Res. Lett. 2017, 12, 347.
- [28] N. Caporale, Y. Dan, Annu. Rev. Neurosci. 2008, 31, 25.
- [29] G. Q. Bi, M. M. Poo, Annu. Rev. Neurosci. 2001, 24, 139.
- [30] C. C. Bell, V. Z. Han, Y. Sugawarat, K. Grant, Nature 1997, 387, 278.
- [31] V. Egger, D. Feldmeyer, B. Sakmann, Nat. Neurosci. 1999, 2, 1098.
- [32] D. E. Feldman, Neuron 2000, 27, 45.
- [33] H. Markram, J. Lübke, M. Frotscher, B. Sakmann, Science 1997, 275, 213.
- [34] L. I. Zhang, H. W. Tao, C. E. Holt, W. A. Harris, M. M. Poo, Nature 1998, 395, 37.
- [35] Y. Li, Y. Zhong, J. Zhang, L. Xu, Q. Wang, H. Sun, H. Tong, X. Cheng, X. Miao, *Sci. Rep.* **2014**, *4*, 4906.
- [36] D. Kuzum, R. G. D. Jeyasingh, B. Lee, H.-S. Philip Wong, Nano Lett. 2012, 12, 2179.
- [37] L. N. Cooper, M. F. Bear, Nat. Rev. Neurosci. 2012, 13, 798.
- [38] E. Bienenstock, L. Cooper, P. Munro, J. Neurosci. 1982, 2, 32.
- [39] W. C. Abraham, Nat. Rev. Neurosci. 2008, 9, 387.
- [40] L. N. Cooper, F. Liberman, E. Oja, Biol. Cybern. 1979, 33, 9.
- [41] N. Intrator, L. N. Cooper, Neural Networks 1992, 5, 3.
- [42] Z. Wang, T. Zeng, Y. Ren, Y. Lin, H. Xu, X. Zhao, Y. Liu, D. Ielmini, *Nat. Commun.* 2020, 11, 1510.
- [43] J. F. Disterhoft, D. A. Coulter, D. L. Alkon, Proc. Natl. Acad. Sci. USA 1986, 83, 2733.
- [44] B. G. Schreurs, D. Tomsic, P. A. Gusev, D. L. Alkon, J. Neurophysiol. 1997, 77, 86.
- [45] H. K. Titley, N. Brunel, C. Hansel, Neuron 2017, 95, 19.
- [46] D. Debanne, Y. Inglebert, M. Russier, Curr. Opin. Neurobiol. 2018, 54, 73.
- [47] R. S. Dahiya, D. Cattin, A. Adami, C. Collini, L. Barboni, M. Valle, L. Lorenzelli, R. Oboe, G. Metta, F. Brunetti, *IEEE Sens. J.* 2011, *11*, 3216.
- [48] Y. Kim, Y. J. Kwon, D. E. Kwon, K. J. Yoon, J. H. Yoon, S. Yoo, H. J. Kim, T. H. Park, J.-W. Han, K. M. Kim, C. S. Hwang, *Adv. Mater.* **2018**, *30*, 1704320.
- [49] J. H. Yoon, Z. Wang, K. M. Kim, H. Wu, V. Ravichandran, Q. Xia, C. S. Hwang, J. J. Yang, *Nat. Commun.* **2018**, *9*, 417.
- [50] G. Neves, S. F. Cooke, T. V. P. Bliss, Nat. Rev. Neurosci. 2008, 9, 65.
- [51] Q. Wu, H. Wang, Q. Luo, W. Banerjee, J. Cao, X. Zhang, F. Wu, Q. Liu, L. Li, M. Liu, *Nanoscale* **2018**, *10*, 5875.
- [52] T. Mazur, P. Zawal, K. Szacilowski, Nanoscale 2019, 11, 1080.
- [53] Z. H. Tan, R. Yang, K. Terabe, X. B. Yin, X. D. Zhang, X. Guo, Adv. Mater. 2016, 28, 377.
- [54] X. Zhu, C. Du, Y. Jeong, W. D. Lu, Nanoscale 2017, 9, 45.
- [55] D. Chklovskii, B. Mel, K. Svoboda, Nature 2004, 431, 782.
- [56] S. B. Hofer, T. D. Mrsic-Flogel, T. Bonhoeffer, M. Hübener, *Nature* 2009, 457, 313.
- [57] T. Xu, X. Yu, A. J. Perlik, W. F. Tobin, J. A. Zweig, K. Tennant, T. Jones, Y. Zuo, *Nature* **2009**, *462*, 915.
- [58] S. B. Eryilmaz, H.-S. P. Wong, in Neuro-Inspired Computing Using Resistive Synaptic Devices (Ed: S. Yu), Springer, Cham 2017, pp. 99–111.
- [59] I. Giannopoulos, A. Sebastian, M. Le Gallo, V. P. Jonnalagadda, M. Sousa, M. N. Boon, E. Eleftheriou, in 2018 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2018.
- [60] S. R. Nandakumar, I. Boybat, M. Le Gallo, A. Sebastian, B. Rajendran, E. Eleftheriou, in 2017 75th Annual Device Research Conf., IEEE, Piscataway, NJ, 2017.
- [61] J. Y. Wu, Y. S. Chen, W. S. Khwa, S. M. Yu, T. Y. Wang, J. C. Tseng, Y. D. Chih, C. H. Diaz, in 2018 IEEE Int. Electron Devices Meet., IEEE, Piscataway, NJ 2018.

- [62] S. Ambrogio, N. Ciocchini, M. Laudato, V. Milo, A. Pirovano, P. Fantini, D. Ielmini, Front. Neurosci. 2016, 10, 56.
- [63] A. L. Hodgkin, A. F. Huxley, Proc. R. Soc. London, Ser. B 1952, 140, 177.
- [64] T. Tuma, M. Le Gallo, A. Sebastian, IEEE Electron. Device Lett. 2016, 37, 1238.
- [65] H. M. Huang, R. Yang, Z. H. Tan, H. K. He, W. Zhou, J. Xiong, X. Guo, Adv. Mater. 2019, 31, 1803849.
- [66] T. Tuma, A. Pantazi, M. L. Gallo, A. Sebastian, E. Eleftheriou, Nat. Nanotechnol. 2016, 11, 693.
- [67] G. W. Burr, R. M. Shelby, C. di Nolfo, J. W. Jang, R. S. Shenoy, P. Narayanan, K. Virwani, E. U. Giacometti, B. Kurdi, H. Hwang, in 2014 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2014.
- [68] S. Sidler, A. Pantazi, S. Woźniak, Y. Leblebici, E. Eleftheriou, in Int. Conf. on Artificial Neural Networks, Springer, Cham 2017.
- [69] M. Suri, O. Bichler, D. Querlioz, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, B. DeSalvo, in 2011 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2011.
- [70] M. Suri, V. Sousa, L. Perniola, D. Vuillaume, B. DeSalvo, in 2011 Int. Joint Conf. on Neural Networks, IEEE, Piscataway, NJ 2011.
- [71] K. Ren, R. Li, X. Chen, Y. Wang, J. Shen, M. Xia, S. Lv, Z. Ji, Z. Song, Appl. Phys. Lett. 2018, 112, 073106.
- [72] B. L. Jackson, B. Rajendran, G. S. Corrado, M. Breitwisch, G. W. Burr, R. Cheek, K. Gopalakrishnan, S. Raoux, C. T. Rettner, A. Padilla, A. G. Schrott, R. S. Shenoy, B. N. Kurdi, C. H. Lam, D. S. Modha, ACM J. Emerging Technol. Comput. Syst. 2013, 9, 12.
- [73] Y. Li, Y. Zhong, L. Xu, J. Zhang, X. Xu, H. Sun, X. Miao, Sci. Rep. 2013, 3, 1619.
- [74] D. Kuzum, R. G. D. Jeyasingh, H.-S. Philip Wong, in 2011 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2011.
- [75] D. Kuzum, R. G. D. Jeyasingh, S. Yu, H.-S. Philip Wong, IEEE Trans. Electron Devices 2012, 59, 3489.
- [76] Y. Zhong, Y. Li, L. Xu, X. Miao, Phys. Status Solidi RRL 2015, 9, 414.
- [77] S. Yu, P.-Y. Chen, IEEE Solid-State Circuits Mag. 2016, 8, 43.
- [78] E. Linn, R. Rosezin, C. Kugeler, R. Waser, Nat. Mater. 2010, 9, 403.
- [79] G. W. Burr, R. S. Shenoy, K. Virwani, P. Narayanan, A. Padilla, B. Kurdi, H. Hwang, J. Vac. Sci. Technol. B 2014, 32, 040802.
- [80] M. C. Cyrille, A. Verdy, G. Navarro, G. Bourgeois, J. Garrione, M. Bernard, C. Sabbione, P. Noé, E. Nowak, in 2018 Int. Conf. on IC Design and Technology, IEEE, Piscataway, NJ 2018.
- [81] D. Kau, S. Tang, I. V. Karpov, R. Dodge, B. Klehn, J. A. Kalb, J. Strand, A. Diaz, N. Leung, J. Wu, S. Lee, T. Langtry, K. W. Chang, C. Papagianni, J. Lee, J. Hirst, S. Erra, E. Flores, N. Righos, H. Castro, G. Spadini, in 2009 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2009.
- [82] G. Navarro, A. Verdy, N. Castellani, G. Bourgeois, V. Sousa, G. Molas, M. Bernard, C. Sabbione, P. Noé, J. Garrione, L. Fellouh, L. Perniola, in 2017 Symp. on VLSI Technology, IEEE, Piscataway, NJ 2017.
- [83] Y. Shuang, S. Hatayama, J. An, J. Hong, D. Ando, Y. Song, Y. Sutou, Sci. Rep. 2019, 9, 20209.
- [84] L. Sun, Y. Zhang, G. Han, G. Hwang, J. Jiang, B. Joo, K. Watanabe, T. Taniguchi, Y. M. Kim, W. J. Yu, B. S. Kong, R. Zhao, H. Yang, *Nat. Commun.* 2019, 10, 3161.
- [85] S. Kim, M. Ishii, S. Lewis, T. Perri, M. BrightSky, W. Kim, R. Jordan, G. W. Burr, N. Sosa, A. Ray, J.-P. Han, C. Miller, K. Hosokawa, C. Lam, in 2015 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2015.
- [86] S. R. Nandakumar, I. Boybat, M. Le Gallo, E. Eleftheriou, A. Sebastian, B. Rajendran, Supervised Learning in Spiking Neural Networks with Phase-Change Memory Synapses, arXiv, 2019, preprint, arXiv: 1905.11929, https://arxiv.org/abs/1905.11929v1.
- [87] S. R. Kulkarni, B. Rajendran, Neural Networks 2018, 103, 118.
- [88] P. Yao, H. Wu, B. Gao, S. B. Eryilmaz, X. Huang, W. Zhang, Q. Zhang, N. Deng, L. Shi, H.-S. P. Wong, H. Qian, *Nat. Commun.* 2017, 8, 15199.



ADVANCED SCIENCE NEWS

www.advancedsciencenews.com



- [89] S. Kim, S. Park, B. Na, S. Yoon, Spiking-YOLO: Spiking Neural Network for Real-time Object Detection, arXiv, 2019, preprint, arXiv: 1903.06530, https://arxiv.org/abs/1903.06530v1.
- [90] I. Boybat, M. Le Gallo, S. R. Nandakumar, T. Moraitis, T. Parnell, T. Tuma, B. Rajendran, Y. Leblebici, A. Sebastian, E. Eleftheriou, *Nat. Commun.* 2018, 9, 2514.
- [91] G. Pedretti, P. Mannocci, S. Hashemkhani, V. Milo, O. Melnic, E. Chicca, D. Ielmini, *IEEE J. Explor. Solid-State Comput. Devices Circuits* 2020, 6, 89.
- [92] S. Oh, Y. Shi, X. Liu, J. Song, D. Kuzum, IEEE Electron Device Lett. 2018, 39, 1768.
- [93] S. R. Nandakumar, I. Boybat, M. Le Gallo, E. Eleftheriou1, A. Sebastian, B. Rajendran, *Sci. Rep.* 2020, 10, 8080.
- [94] P. U. Diehl, M. Cook, Front. Comput. Neurosci. 2015, 9, 99.
- [95] S. B. Eryilmaz, D. Kuzum, R. G. D. Jeyasingh, S. Kim, M. BrightSky, C. Lam, H.-S. Philip Wong, in 2013 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2013.
- [96] L. R. Iyer, A. Basu, in 2017 Int. Joint Conf. on Neural Networks (IJCNN), IEEE, Piscataway, NJ 2017.
- [97] S. Wozniak, T. Tuma, A. Pantazi, E. Eleftheriou, in 2016 IEEE Int. Symp. on Circuits and Systems, IEEE, Piscataway, NJ 2016.
- [98] S. B. Eryilmaz, D. Kuzum, R. Jeyasingh, S. Kim, M. BrightSky, C. Lam, H.-S. P. Wong, Front. Neurosci. 2014, 8, 205.
- [99] S. Balatti, S. Ambrogio, Z. Wang, D. Ielmini, IEEE J. Emerging Sel. Top. Circuits Syst. 2015, 5, 214.
- [100] M. Boniardi, D. Ielmini, Appl. Phys. Lett. 2011, 98, 243506.
- [101] M. Le Gallo, T. Tuma, F. Zipoli, A. Sebastian, E. Eleftheriou, in 2016 46th European Solid-State Device Research Conf., IEEE, Piscataway, NJ 2016.
- [102] T. Li, J. Shen, L. Wu, Z. Song, S. Lv, D. Cai, S. Zhang, T. Guo, S. Song, M. Zhu, J. Phys. Chem. C 2019, 123, 13377.
- [103] M. Suri, D. Garbin, O. Bichler, D. Querlioz, D. Vuillaume, C. Gamrat, B. DeSalvo, *Comput. Math. Appl.* 2013, 25, 59.
- [104] W. Zhang, L. Tao, in 2011 IEEE/IFIP 41st Int. Conf. on Dependable Systems and Networks, IEEE, Piscataway, NJ 2011.
- [105] H. Y. Cheng, W. C. Chien, M. BrightSky, Y. H. Ho, Y. Zhu, A. Ray, R. Bruce, W. Kim, C. W. Yeh, H. L. Lung, C. Lam, in 2015 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2015.
- [106] W. C. Chien, H. Y. Cheng, M. BrightSky, A. Ray, C. W. Yeh, W. Kim, R. Bruce, Y. Zhu, H. Y. Ho, H. L. Lung, C. Lam, in 2016 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2016.
- [107] S. Raoux, G. W. Burr, M. J. Breitwisch, C. T. Rettner, Y.-C. Chen, R. M. Shelby, M. Salinga, D. Krebs, S.-H. Chen, H.-L. Lung, C. H. Lam, *IBM J. Res. Dev.* **2008**, *52*, 465.
- [108] X. Zhou, M. Xia, F. Rao, L. Wu, X. Li, Z. Song, S. Feng, H. Sun, ACS Appl. Mater. Interfaces 2014, 6, 14207.
- [109] K. H. Song, J. H. Kim, J. H. Seo, H. Y. Lee, J. Optoelectron. Adv. Mater. 2009, 11, 1988.
- [110] K. Kim, J.-C. Park, J.-G. Chung, S. A. Song, M.-C. Jung, Y. Mi Lee, H.-J. Shin, B. Kuh, Y. Ha, J.-S. Noh, *Appl. Phys. Lett.* 2006, 89, 265.
- [111] S. Song, Z. Song, Y. Lu, B. Liu, L. Wu, S. Feng, Mater. Lett. 2010, 64, 2728.
- [112] C. Ahn, S. W. Fong, Y. Kim, S. Lee, A. Sood, C. M. Neumann, M. Asheghi, K. E. Goodson, E. Pop, H.-S. Philip Wong, *Nano Lett.* 2015, *15*, 6809.
- [113] A. Alpert, R. Luo, M. Asheghi, E. Pop, K. Goodson, in 2016 15th IEEE Intersociety Conf. on Thermal and Thermomechanical Phenomena in Electronic Systems, IEEE, Piscataway, NJ 2016.
- [114] A. Behnam, F. Xiong, A. Cappelli, N. C. Wang, E. A. Carrion, S. Hong, Y. Dai, A. S. Lyons, E. K. Chow, E. Piccinini, C. Jacoboni, E. Pop, *Appl. Phys. Lett.* **2015**, *107*, 123508.
- [115] G. W. Burr, M. J. Brightsky, A. Sebastian, H.-Y. Cheng, J.-Y. Wu, S. Kim, N. E. Sosa, N. Papandreou, H.-L. Lung, H. Pozidis, E. Eleftheriou, C. H. Lam, *IEEE J. Emerging Sel. Top. Circuits Systems* 2016, 6, 146.

- [116] M. Suri, O. Bichler, Q. Hubert, L. Perniola, V. Sousa, C. Jahan, D. Vuillaume, C. Gamrat, B. DeSalvo, in 2012 4th IEEE Int. Memory Workshop, IEEE, Piscataway, NJ 2012.
- [117] M. Suri, O. Bichler, Q. Hubert, L. Perniola, V. Sousa, C. Jahan, D. Vuillaume, C. Gamrat, B. DeSalvo, *Solid-State Electron.* 2013, 79, 227.
- [118] R. E. Simpson, P. Fons, A. V. Kolobov, T. Fukaya, M. Krbal, T. Yagi, J. Tominaga, Nat. Nanotechnol. 2011, 6, 501.
- [119] Y. Lu, S. Song, Z. Song, L. Wu, A. He, Y. Gong, F. Rao, B. Liu, Appl. Phys. Lett. 2012, 101, 824.
- [120] T. C. Chong, L. P. Shi, R. Zhao, P. K. Tan, J. M. Li, H. K. Lee, X. S. Miao, A. Y. Du, C. H. Tung, *Appl. Phys. Lett.* **2006**, *88*, 122114.
- [121] C. C. Tan, L. Shi, R. Zhao, Q. Guo, Y. Li, Y. Yang, T. C. Chong, J. A. Malen, W.-L. Ong, T. E. Schlesinger, J. A. Bain, *Appl. Phys. Lett.* 2013, 103, 133507.
- [122] L. Li, S. Song, Z. Zhang, L. Chen, Z. Song, S. Lv, B. Liu, T. Guo, Solid-State Electron. 2016, 120, 52.
- [123] S. Kim, N. Sosa, M. BrightSky, D. Mori, W. Kim, Y. Zhu, K. Suu, C. Lam, in 2013 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2013.
- [124] M. BrightSky, N. Sosa, T. Masuda, W. Kim, S. Kim, A. Ray, R. Bruce, J. Gonsalves, Y. Zhu, K. Suu, C. Lam, in 2015 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2015.
- [125] E. Small, S. M. Sadeghipour, L. Pileggi, M. Asheghi, in 2008 11th Intersociety Conf. on Thermal and Thermomechanical Phenomena in Electronic Systems, IEEE, Piscataway, NJ 2008.
- [126] H. K. Lee, L. Shi, R. Zhao, H. Yang, K. G. Lim, J. Li, T. C. Chong, Jpn. J. Appl. Phys. 2010, 49, 04DD16.
- [127] P. Lin, Q. Xia, J. Appl. Phys. 2018, 124, 152001.
- [128] J. Hao, Q. Xia, Appl. Phys. Lett. 2014, 104, 153505.
- [129] D. Garbin, E. Vianello, O. Bichler, Q. Rafhay, C. Gamrat, G. Ghibaudo, B. DeSalvo, L. Perniola, *IEEE Trans. Electron Devices* 2015, *62*, 2494.
- [130] M. Suri, O. Bichler, D. Querlioz, B. Traoré, O. Cueto, L. Perniola, V. Sousa, D. Vuillaume, C. Gamrat, B. DeSalvo, J. Appl. Phys. 2012, 112, 054904.
- [131] D. Garbin, M. Suri, O. Bichler, D. Querlioz, C. Gamrat, B. DeSalvo, in 2013 13th IEEE Int. Conf. on Nanotechnology, IEEE, Piscataway, NJ, 2013.
- [132] J. Bill, R. Legenstein, Front. Neurosci. 2014, 8, 412.
- [133] T. Li, L. Wu, Z. Song, S. Song, F. Rao, B. Liu, Mater. Sci. Forum 2017, 898, 1834.
- [134] Y. Hu, X. Zhu, H. Zou, J. Zhang, L. Yuan, J. Xue, Y. Sui, W. Wu, S. Song, Z. Song, *Appl. Phys. Lett.* **2016**, *108*, 6390.
- [135] W. Liu, L. Wu, T. Li, Z. Song, J. Shi, J. Zhang, S. Feng, Appl. Phys. Express 2018, 11, 041401.
- [136] A. Athmanathan, M. Stanisavljevic, N. Papandreou, H. Pozidis, E. Eleftheriou, IEEE J. Emerging Sel. Top. Circuits Syst. 2016, 6, 87.
- [137] H. Pozidis, T. Mittelholzer, N. Papandreou, T. Parnell, M. Stanisavljevic, IEEE Trans. Magn. 2015, 51, 3500107.
- [138] N. Papandreou, H. Pozidis, A. Pantazi, A. Sebastian, M. Breitwischt, C. Lamt, E. Eleftheriou, in 2011 IEEE Int. Symp. of Circuits and Systems, IEEE, Piscataway, NJ 2011.
- [139] A. Kiouseloglou, G. Navarro, V. Sousa, A. Persico, A. Roule, A. Cabrini, G. Torelli, S. Maitrejean, G. Reimbold, B. De Salvo, F. Clermidy, L. Perniola, *IEEE Trans. Electron Devices* 2014, *61*, 1246.
- [140] Y. Liu, Y. Chen, D. Cai, Y. Lu, L. Wu, S. Yan, Y. Li, Z. Song, Mater. Sci. Semicond. Process 2019, 91, 399.
- [141] K. Ding, J. Wang, Y. Zhou, H. Tian, L. Lu, R. Mazzarello, C. Jia, W. Zhang, F. Rao, E. Ma, *Science* 2019, *366*, 210.
- [142] W. W. Koelmans, A. Sebastian, V. P. Jonnalagadda, D. Krebs, L. Dellmann, E. Eleftheriou, *Nat. Commun.* 2015, *6*, 8181.
- [143] W. Kim, M. BrightSky, T. Masuda, N. Sosa, S. Kim, R. Bruce, F. Carta, G. Fraczak, H. Y. Cheng, A. Ray, Y. Zhu, H. L. Lung,

ADVANCED SCIENCE NEWS

www.advancedsciencenews.com

K. Suu, C. Lam, in 2016 IEEE Int. Electron Devices Meeting, IEEE, Piscataway, NJ 2016.

- [144] W. Kim, R. L. Bruce, T. Masuda, G. W. Fraczak, M. BrightSky, in 2019 Symp. on VLSI Technology, IEEE, Piscataway, NJ 2019.
- [145] Y. J. Song, K. C. Ryoo, Y. N. Hwang, C. W. Jeong, D. W. Lim, S. S. Park, J. I. Kim, J. H. Kim, S. Y. Lee, J. H. Kong, S. J. Ahn, S. H. Lee, J. H. Park, J. H. Oh, Y. T. Oh, J. S. Kim, J. M. Shin, J. H. Park, Y. Fai, G. H. Koh, G. T. Jeong, R. H. Kim, H. S. Lim, I. S. Park, H. S. Jeong, K. Kim, in 2006 Symp. on VLSI Technology, IEEE, Piscataway, NJ 2006.
- [146] B. Jin, J. Kim, D.-H. Pi, H. S. Kim, M. Meyyappan, J.-S. Lee, AIP Adv. 2014, 4, 127155.
- [147] M. Mitra, Y. Jung, D. S. Gianola, R. Agarwal, Appl. Phys. Lett. 2010, 96, 222111.
- [148] I.-M. Park, J.-K. Jung, S.-O. Ryu, K.-J. Choi, B.-G. Yu, Y.-B. Park, S. M. Han, Y.-C. Joo, *Thin Solid Films* **2008**, *517*, 848.
- [149] Y. N. Hwang, C. Y. Um, J. H. Lee, C. G. Wei, C. H. Chung, in 2010 Symp. on VLSI Technology, IEEE, Piscataway, NJ 2010.
- [150] G. W. Burr, M. J. Breitwisch, M. Franceschini, D. Garetto, K. Gopalakrishnan, B. Jackson, B. Kurdi, C. Lam, L. A. Lastras, A. Padilla, J. Vac. Sci. Technol., B: Microelectron. Nanometer Struct. 2010, 28, 223.
- [151] W.-S. Khwa, M.-F. Chang, J.-Y. Wu, M.-H. Lee, T.-H. Su, K.-H. Yang, T.-F. Chen, T.-Y. Wang, H.-P. Li, M. Brightsky, S. Kim, H.-L. Lung, C. Lam, *IEEE J. Solid-State Circuits* **2017**, *52*, 218.
- [152] Z. Wang, S. Joshi, S. E. Savel'ev, H. Jiang, R. Midya, P. Lin, M. Hu, N. Ge, J. P. Strachan, Z. Li, Q. Wu, M. Barnell, G.-L. Li, H. L. Xin, R. S. Williams, Q. Xia, J. J. Yang, *Nat. Mater.* **2017**, *16*, 101.
- [153] Q. Wang, G. Niu, S. Roy, Y. K. Wang, Y. J. Zhang, H. P. Wu, S. J. Zhai, W. Bai, P. Shi, S. N. Song, Z. T. Song, Y.-H. Xie, Z.-G. Ye, C. Wenger, X. J. Meng, W. Ren, J. Mater. Chem. C 2019, 7, 12682.
- [154] S. Roy, G. Niu, Q. Wang, Y. K. Wang, Y. J. Zhang, H. P. Wu, S. J. Zhai, P. Shi, S. N. Song, Z. T. Song, Z.-G. Ye, C. Wenger,



T. Schroeder, Y.-H. Xie, X. J. Meng, W. B. Luo, W. Ren, ACS Appl. Mater. Interfaces 2020, 12, 10648.

- [155] J. Li, C. Ge, J. Du, C. Wang, G. Yang, K. Jin, Adv. Mater. 2020, 32, 1905764.
- [156] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, M. Bibes, A. Barthélémy, J. Grollie, *Nat. Mater.* **2012**, *11*, 860.
- [157] F. Xiong, A. D. Liao, D. Estrada, E. Pop, Science 2011, 332, 568.
- [158] J. Liang, R. G. D. Jeyasingh, H.-Y. Chen, H.-S. Philip Wong, in 2011 Symp. on VLSI Technology, IEEE, Piscataway, NJ 2011.
- [159] C. Wu, T. W. Kim, H. Y. Choi, D. B. Strukov, J. J. Yang, Nat. Commun. 2017, 8, 752.
- [160] B. Gao, Y. Bi, H.-Y. Chen, R. Liu, P. Huang, B. Chen, L. Liu, X. Liu, S. Yu, H.-S. P. Wong, J. Kang, ACS Nano 2014, 8, 6998.
- [161] Z. Li, P.-Y. Chen, H. Xu, S. Yu, IEEE Trans. Electron Devices 2017, 64, 2721.
- [162] S. Yu, H.-Y. Chen, B. Gao, J. Kang, H.-S. P. Wong, ACS Nano 2013, 7, 2320.
- [163] H. Li, K.-S. Li, C.-H. Lin, J.-L. Hsu, W.-C. Chiu, M.-C. Chen, T.-T. Wu, J. Sohn, S. B. Eryilmaz, J.-M. Shieh, in 2016 IEEE Symp. on VLSI Technology, IEEE, Piscataway, NJ 2016.
- [164] D. B. Strukov, R. S. Williams, Proc. Natl. Acad. Sci. USA 2009, 106, 20155.
- [165] J. Pei, L. Deng, S. Song, M. Zhao, Y. Zhang, S. Wu, G. Wang, Z. Zou, Z. Wu, W. He, F. Chen, N. Deng, S. Wu, Y. Wang, Y. Wu, Z. Yang, C. Ma, G. Li, W. Han, H. Li, H. Wu, R. Zhao, Y. Xie, L. Shi, *Nature* **2019**, *572*, 106.
- [166] Y. Zhang, P. Qu, Y. Ji, W. Zhang, G. Gao, G. Wang, S. Song, G. Li, W. Chen, W. Zheng, F. Chen, J. Pei, R. Zhao, M. Zhao, L. Shi, *Nature* **2020**, *586*, 378.
- [167] B. M. Lake, T. D. Ullman, J. B. Tenenbaum, S. J. Gershman, *Behav. Brain Sci.* 2017, 40, e253.



Qiang Wang received his B.S. degree from North University of China in 2015 and obtained his master's degree from Central South University, China, in 2018. He is studying for a Ph.D. degree in the School of Electronic Science and Engineering, Xi'an Jiaotong University. His current research interest is nonvolatile memories and their application in neuro-inspired computing.



Gang Niu received a Ph.D. degree from Ecole Centrale de Lyon, France in 2010. He was a postdoc at CNRS, France and at the Leibniz Insitute for high performance microelectronics (IHP), Germany as a research scientist. He is now a research professor at Xi'an Jiaotong University, China. He is the author of one book chapter, more than 90 papers and 6 patents. Dr. Niu was a recipient of Alexander von Humboldt fellowship and DFG Mercator fellowship. His research interests consist in the monolithic integration of oxides with silicon for "more than Moore" devices, particularly non-volatile memories.







Wei Ren received his Ph.D. degree from Xi'an Jiaotong University (XJTU) in 1992. He is now the chair professor, the director of the Institute of Ferroic Materials and Integrated Devices and the executive director of the International Center for Dielectric Research, at XJTU. He has held visiting appointments at the Heinrich Hertz Institute, Germany, the Materials Research Laboratory of the Pennsylvania State University, USA, and the Department of Physics of the Royal Military College of Canada. Prof. Ren has published more than 290 papers and held 30 patents. His research interests include di-/ferro-/piezo-electric materials for novel device applications.



Zhitang Song received a Ph.D. degree from the Electronic Materials Research Laboratory, Xi'an Jiaotong University, Xi'an, China, in 1997. He has taken the lead in conducting research and development of phase change memory (PCM), and cultivated and organized a 100-person high-level research and development team, integrating industry, university, and research. He is currently the director of the State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology (SIMIT), Chinese Academy of Sciences (CAS), Shanghai, China.