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THE STRUCTURE OF GaAs/Si(211) HETEROEPITAXIAL LAYERS

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ABSTRACT

Gallium arsenide films grown on (211)Si by molecular-beam epitaxy have been investigated using transmission electron microscopy. The main defects observed in the alloy were of misfit dislocations, stacking faults, and microtwin lamellas. Silicon surface preparation was found to play an important role on the density of defects formed at the Si/GaAs interface.

Two different types of strained-layer superlattices, InGaAs/InGaP and InGaAs/GaAs, were applied either directly to the Si substrate, to a graded layer (GaP-InGaP), or to a GaAs buffer layer to stop the defect propagation into the GaAs films. Applying InGaAs/GaAs instead of InGaAs/InGaP was found to be more effective in blocking defect propagation. In all cases of strained-layer superlattices investigated, dislocation propagation was stopped primarily at the top interface between the superlattice package and GaAs. Graded layers and unstrained AlGaAs/GaAs superlattices did not significantly block dislocations propagating from the interface with Si. Growing of a 50 nm GaAs buffer layer at 505°C followed by 10 strained-layer superlattices of InGaAs/GaAs (5 nm each) resulted in the lowest dislocation density in the GaAs layer ($\sim 5 \times 10^7/\text{cm}^2$) among the structures investigated. This value is comparable to the recently reported density of dislocations in the GaAs layers grown on (100)Si substrates [8]. Applying three sets of the same strained layers decreased the density of dislocations an additional ~ 2 -3 times.

INTRODUCTION

Epitaxial growth of GaAs on Si has been the subject of increasing interest since such a system will provide the potential for utilizing the strength of GaAs (high mobility and direct gap/optical phenomena) in conjunction with advanced Si processes for integrated device structures [1-6]. However, the large misfit between GaAs and Si ($\sim 4\%$) and the growth of a polar crystal on a nonpolar one result in a high density of lattice defects and antiphase disorder, and can cause the formation of a very large intrinsic electric charge that can act as a sheet of very high doping. One solution to these problems may be the use of (211)Si substrates to grow GaAs [5]. The formation of a thick buffer layer and an intrinsic interface charge, as well as suppression of the antiphase boundary, can be avoided in this way. However, the high density of dislocations and stacking faults is not satisfactory for device applications and growth of low-defect density (below $10^5/\text{cm}^2$) in GaAs epitaxial layer on Si has not been successfully demonstrated yet. Reported low dislocation density ($10^3/\text{cm}^2$) seems to be underestimated [7]. Some discrepancies may come from using different techniques such as KOH etching and TEM studies. It was shown that values obtained from these two techniques can differ few orders of magnitude [8]. Some other differences estimated from TEM studies can come from the fact that dislocation density was estimated in different distances from the Si/GaAs interface on cross section micrographs, or for different foil thicknesses in plan-view micrographs. Suppression of dislocation propagation by using GaAs layers several μm thick does not appear to be a feasible

solution, as the differences in thermal expansion coefficients create wafer warpage problems. In this paper, the structure of GaAs/Si(211) hetero-epitaxial layers with GaP-InGaP graded layers, InGaAs/GaAs and InGaAs/InGaP strained layers, and AlGaAs/GaAs unstrained superlattice layers has been investigated by high-resolution electron microscopy.

EXPERIMENTAL

GaAs crystal growth on a Si(211) substrate was conducted in a molecular-beam epitaxy (MBE) system (Varian-360). Two different cleaning procedures, called A and B, were applied to the Si wafers to determine the importance of Si surface preparation on defect formation at the Si/GaAs interface. Method A followed the procedure described by Ishizaka [9], where four major steps were involved: degreasing, acidic oxidation, alkaline oxidation, and boiling in $\text{HCl}:\text{H}_2\text{O}:\text{H}_2\text{O}_2$ (3:1:1) for 5-7 min followed by DI water rinse. After this procedure the Si wafers were mounted to a molybdenum block with In where the Si wafer was dried with filtered nitrogen. In the MBE growth chamber the sample temperature was raised to 800°C for 10 min to desorb the SiO_x . After this procedure the Si surface was considered as oxide free.

Method B involved Ga reduction. In principle the procedure described above was repeated. Then, in the MBE chamber, the Si sample temperature was raised to 800°C , and a beam of Ga was simultaneously impinged on the sample surface. This "Ga-reduction" procedure lasted for ~10 min. Then, the Ga furnace shutter was closed, but the sample temperature was still kept at 800°C for one more minute to eliminate the excess Ga on the surface. After this procedure the surface was considered oxide free, and specific layers, shown in Fig. 1, were grown.

Two different structures shown schematically in Fig. 1a and b (samples 26 and 23) were grown on Si cleaned by method A. The purpose of those structures was to investigate how graded layers (GaP to InGaP) and different types (InGaAs/InGaP or InGaAs/GaAs) of strained-layer superlattices (SLSL) will influence defect propagation. Two other structures were grown to investigate the influence of the presence of a GaAs buffer layer and the temperature in which this layer was grown (Fig. 1c,d - samples 60 and 61). Subsequently the other structures were grown to check the influence of only one strained layer superlattice to stop the dislocation propagation (Fig. 1e - sample 62). On the basis of the experience gained by investigation of these five structures, a structure with three packages of SLSL was grown (Fig. 1f - sample 72).

RESULTS

All structures shown in Fig. 1 were investigated by transmission electron microscopy using a JEOL JEM 200CX electron microscope with a point-to-point resolution of a $2.4 \text{ \AA}$ and the Atomic Resolution Microscope (ARM) at Berkeley with its $1.7 \text{ \AA}$ point-to-point resolution. All samples were investigated in cross-sections prepared along Si[111] and Si[110] parallel to the electron beam. Studies of sample 26 show that the compositionally graded layers (GaP-InGaP) do not significantly reduce the high dislocation density. All dislocations formed on the interface propagate through the graded layer (Fig. 2). The dislocation density is reduced significantly, about two orders of magnitude by SLSL of InGaAs/InGaP. A very important feature of this blocking of dislocation propagation is that it does not occur gradually throughout all sets of strained superlattice layers but almost entirely at the uppermost interface between the strained layers and the final GaAs layer. Therefore, the reduction of dislocation density is only weakly dependent on the thickness of the strained-layer superlattices. Unstrained superlattices of GaAs/GaAlAs do not reduce the

a: Sample 26

(0.5 microns)	GaAs	600°C
(2.5 nm ea.)	20 per. GaAs/AlGaAs	600°C
(5 nm ea.)	50 per. In Ga As/In Ga P 25% In	450°C
(~0.3 microns)	In Ga P 0.49 0.51 GaP	580°C
	Si(211)	

b: Sample 23

(0.5 microns)	GaAs	600°C
(5 nm ea.)	50 per. InGaAs/GaAs 25% In	505°C
	Si(211)	

c: Sample 60

(1 micron)	GaAs 3 mins. growth inter.	600°C
(5 nm ea.)	InGaAs/GaAs	505°C
(50 nm)	GaAs	505°C
	Si(211)	

d: Sample 61

(1 micron)	GaAs	600°C
(5 nm ea.)	10 per. InGaAs/GaAs 3 mins. growth inter.	505°C
(10 nm)	GaAs 3 mins. growth inter.	300°C
	Si(211)	

f: Sample 72

(1 micron)	GaAs	600°C
(5 nm ea.)	10 per. InGaAs/GaAs	505°C
(50 nm)	GaAs	600°C
(5 nm ea.)	10 per. InGaAs/GaAs	505°C
(50 nm)	GaAs	600°C
(5 nm ea.)	10 per. InGaAs/GaAs	505°C
(50 nm)	GaAs increased growth rate from 200 nm/hr. to 500 nm/hr.	505°C
	Si(211)	

e: Sample 62

(1 micron)	GaAs	600°C
(30 nm)	InGaAs 3 mins. growth inter.	505°C
(50 nm)	GaAs	505°C
	Si(211)	

Fig. 1. Schematic description of particular layers grown on the (211)Si surface to block dislocation propagation into the GaAs epilayer.

Fig. 2. TEM cross-section micrograph of the GaAs layer grown on the (211)Si surface. Description of particular layers and the growth conditions shown in Fig. 1a. Note defects propagation through the graded layer and their very effective blocking by SLSL. Unstrained layers only weakly block dislocation propagation.

dislocation density occurring on the uppermost interface of SLSL. The dislocations density present in the top GaAs layer is in the range of $10^{10}/\text{cm}^2$, much too high for device applications.

Another type of strained-layer superlattice (GaAs/InGaAs - 25% In) was applied directly to the Si surface (sample 23), which was cleaned by procedure A. In this way the dislocations density was reduced drastically, to as low as $10^8/\text{cm}^2$ or even locally below this value.

Comparing these two structures, it was considered that InGaAs/GaAs strained-layer superlattices are more efficient in stopping dislocation propagation. However, in this sample many impurities were formed at the interface. The GaAs/Si interface was not flat, and many triangular crystalline precipitates (presumably SiAs or SiC) were present (Fig. 3). Formation of these precipitates was the source of stacking faults or twin formation. Therefore another cleaning procedure was applied (described earlier as B) for the following samples. In contrast to the previous structures, a buffer layer of GaAs was grown directly on the Si wafer. The temperature and the thickness of the buffer layer varied for samples 60 and 61 but the type of SLSL (InGaAs/GaAs, 5 nm each grown at 505°C) and the thickness and the growth temperature of the top GaAs layer (1 μm thick, grown at 600°C with 3 min. growth interruption) was the same for both of those samples.

Because it was recognized that the total thickness of the strained layer superlattices did not influence the reduction of dislocation propagation significantly, only 10 layers of InGaAs/GaAs (5 nm each) were grown to decrease total thickness of the epilayers. Sample 60, with a buffer layer grown at 505°C (a schematic drawing of this structure shown on Fig. 1c),

Fig. 3. TEM cross-section micrograph of the structure shown in Fig. 1b. Note low defect density in the GaAs layer, large number of stacking faults propagating through the SLSL of InGaAs/GaAs and a triangular protrusion of the Si interface. High resolution of this protrusion showed a crystalline structure.

Fig. 4. TEM micrographs of the structure shown in Fig. 1c. Note the SLSL grown on the GaAs buffer layer. There were found many dislocation free areas in the top GaAs layer (b), but there were some areas with higher dislocation density (a,c).

turned out to have large dislocation-free areas in the GaAs, and the average dislocation density was in the range of $10^7/\text{cm}^2$ at 150 nm from the Si interface (Fig. 4). Sample 61, grown with the buffer layer at 300°C (as shown in Fig. 1d), showed a slightly higher dislocation density than sample 60.

It was very interesting to observe that only one strain layer of InGaAs (sample 62, shown in Fig. 1e) was enough to bend many dislocations, but many of them still propagated to the GaAs. Bending of dislocations again occurred on the upper interface with GaAs (Fig. 5).

Because of the observation that the upper interface of strained layer superlattices is most efficient in the bending of dislocations, three sets of SLSL were grown on the Si separated by 50 nm of the GaAs buffer layer (sample 72, shown in Fig. 1f). It was expected that each set would reduce the dislocation density on the upper GaAs layer. Indeed, each set of SLSL caused additional dislocation bending, and there were many dislocation free areas ($3\text{--}5\text{ }\mu\text{m}$ long) (Fig. 6), but there were areas where additional dislocations were formed at the lower interface between the buffer layer and the SLSL. Therefore, in some areas the dislocation density was slightly higher.

Fig. 5. Dislocation bending by only one 30 nm thick layer of InGaAs (growth conditions shown on Fig. 1e).

Fig. 6. TEM micrograph of the structure shown on Fig. 1f. Note bending of dislocations by three sets of SLSLs.

DISCUSSION

Among all structures investigated, the largest dislocation-free areas were observed locally in samples 60 and in 72. In these samples (particularly in sample 60), the dislocations density dropped a few orders of magnitude and reached $10^7/\text{cm}^2$, as was reported for GaAs grown on a (100)Si substrate. This dislocation density is still too high for many device applications, particularly for minority-carrier devices. However, the misfit strain might prevent the glide of the total dislocation from the interface. Figure 7 shows that numerous stacking faults are formed lying on the (111) and $(\bar{1}\bar{1}1)$ planes, respectively. This can be explained by dissociations of the 60° misfit dislocations along $[01\bar{1}]$ of the following type: $a/2[\bar{1}01] = a/6[\bar{1}\bar{1}2] + a/6[211]$, creating a 30° Shockley partial on (111) and an edge Shockley partial dislocation at the interface; and $a/2[\bar{1}01] = a/6[\bar{1}\bar{2}1] + a/3[\bar{1}\bar{1}1]$, creating a Shockley partial on $(\bar{1}\bar{1}1)$ and an edge stair-rod at the interface. Both reactions leave edge misfit dislocations at the interface and produce Shockley partials that have no Burgers-vector component (for the $a/6[\bar{1}\bar{2}1]$ partial) or only a small component (for the $a/6[\bar{1}\bar{1}2]$ partial) along $[\bar{1}\bar{1}1]$, which is the direction of maximum misfit strain for a misfit dislocation along $[01\bar{1}]$. The partial dislocations gliding on (111), the plane perpendicular to (211), are often observed to stop at the top interface of the SLSLs. In some cases, reactions of such partial dislocations produce threading dislocations that extend through the top GaAs layer.

The reactions described above show the possibility that misfit dislocations at the (211)Si interface may dissociate, leaving a partial dislocation at the interface and allowing a threading partial to enter the epitaxial layer. The partial dislocation left at the interface can still release most of the interfacial strain. This mechanism might explain the extremely high density of dislocations propagating into the epilayer. Therefore, even a reduction of threading-dislocation density by several orders of magnitude by SLSLs does not reduce the dislocation density in the top GaAs layer sufficiently. For Si(100), two perpendicular $\langle 100 \rangle$ directions are lying on the interface, so that most misfit dislocations are of

the edge type, unable to glide into the epilayer. Only a small fraction of them ("type 2" [10]) has Burgers vectors inclined to the (100) plane, suitable to glide into the upper epilayers.

In view of the above discussion, it appears to be a notable achievement that the growth of 10 layers of InGaAs/GaAs SLSLs grown on (211)Si with a GaAs buffer layer (sample 60) or with three SLSL packages (sample 72) resulted in a dislocation density in the top GaAs layer in the $10^7/\text{cm}^2$ range, comparable to the recently reported dislocation densities for GaAs grown on (100)Si [11,12].

In addition to dislocations and stacking faults, the interfacial strain causes as well the formation of twins and twin lamellas. The number of these defects increases on impured and not atomically flat Si surfaces. The presence of microtwins and stacking faults seems to be very unfavorable to get dislocation free GaAs.

Fig. 7. Stacking faults formed at the Si/GaAs interface a) laying on the (111) plane, b) laying on the $(\bar{1}\bar{1}1)$ plane.

Another problem that needs to be solved for successful device application is a cracking of the GaAs layer.

CONCLUSIONS

Investigation of GaAs on (211)Si showed that all samples were free of antiphase boundaries. Misfit dislocations have Burgers vectors inclined to the interface, making them susceptible to dissociations and gliding into the GaAs layer. This was in contrast to the GaAs grown on a (100)Si surface, where a large fraction of the dislocations formed at the interface have Burgers vector parallel to the interface. Dislocations are not uniformly distributed at the interface. The average distance between them was ~ 8.1 nm. Many of the observed dislocations were dissociated, and stacking faults or microtwin lamellas were formed. Their number increased when some impurities or other imperfections were present on the Si surface. The dislocation density was reduced significantly by SLSL, but this reduction depended only weakly on the thickness of the SLSLs. It was interesting to observe that only one SLSL of InGaAs (30 nm thick) was enough to tangle the dislocations in the near interfacial area (Fig. 5).

In all observed cases blocking of dislocation propagation occurred almost entirely at the uppermost interface between SLSL and the final GaAs layer. Using SLSL's decreased the dislocation density at least two orders of magnitude or more. The use of ten periods of InGaAs/GaAs (5 nm each) led locally to a dislocation density of $\sim 5 \times 10^7/\text{cm}^2$, but three layers led to densities of $\sim 2 \times 10^7/\text{cm}^2$. These values are comparable to the reported dislocation density in GaAs grown on (100)Si [8,11-12]. The defects formed in the GaAs layer were not uniformly distributed. This observation was true for GaAs grown on (211)Si as well as on (100)Si [13].

In almost all structures investigated, some areas were dislocation free, but there were other areas of high dislocation density (to $10^9/\text{cm}^2$). Graded layers and unstrained superlattices did not significantly reduce the high dislocation density formed at the interface with Si.

Our observations show that the defect density in the top GaAs layers can be reduced drastically by suitable surface cleaning and the use of SLSLs. Further work appears to be necessary to reduce the dislocation density below $10^5/\text{cm}^2$, a value that is needed to allow use of such material for most device applications.

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