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A Wide-Band Frequency Domain Near Infrared Spectroscopy System on Chip

THESIS

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MASTER OF SCIENCE

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DEDICATION

To my family

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ABSTRACT OF THE THESIS

A Wide-Band Frequency Domain Near Infrared Spectroscopy System on Chip

By

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Master of Science in Electrical and Computer Engineering

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Professor Michael Green, Chair

In this thesis, the design procedure of a frequency-domain diffuse optical imaging system on chip is introduced. The objective of this design is to measure some optical properties of tissue. Using those measurement results, one can find out scattering and absorption coefficient of the tissue. These factors are used to compute the concentration of specific materials inside the human body. The proposed system must precisely compare the phase and amplitude difference between transmitted and detected optical signals. The first version of the chip, which was implemented in a 180 nm CMOS process, used a free-running voltage controlled oscillator (VCO) as the reference signal. In this version, a phase detector unit measures the phase difference between the transmitted and detected signal in the analog domain using a novel feedback system with an N-path filter. In addition, the circuit employed a logarithmic amplifier for amplitude detection. A second version of the chip was designed and fabricated using a 65 nm CMOS process. In this version, a number of changes and modifications were done. For better precision of the phase measurement and reducing jitter, a phase-locked loop (PLL) was designed instead of a free-running VCO. In addition, a down-conversion mixer was used for high-frequency noise filtering and ease of dealing with IF frequency in the phase measurement unit. In this version, phase measurement is done in the digital domain in which the time delay between two square wave signals is attained using a time-to-digital converter. In the third version, the system configuration was chosen to be a heterodyned

system. After completion of the whole system design, this version will also be fabricated in 65 nm CMOS. The PLL must provide modulation frequencies between 50 MHz to 500 MHz. In this version, a laser driver is added to be on chip. This circuit needs to provide large amounts of current for different kinds of laser diodes. In addition, this version is going to be less area consuming, with the pin count reduced by using serial-to-parallel converters. Some variations in the time resolution and clocking is done in this version, too. This work can show reasonable results for future operations in wearable optic sensing systems based on frequency-domain near-infrared spectroscopy (fd-NIRS).

Chapter 1

Introduction

1.1 Spectroscopy and Applications

The need for wearable, low-power, and cost-effective devices and detectors for healthcare and monitoring cases has been growing in the last few decades. There has been a large investment in digital health since one of the most important objectives of the health science field is identifying important events inside of the body where treatments should be done [1].

Among all of strategies used for characterizing molecular compositions, tissue optical spectroscopy has been in the center of attention due to its non-invasive and ease of use for bio-medical operations such as cardiology, neurology, and cancer [2].

Spectroscopy is the field of study that measures and interprets the electromagnetic spectrum resulting from the interaction of electromagnetic radiation with materials as a function of the wavelength or frequency of the radiation. Because this field is so broad, there are many sub-fields, each having produced significant results for specific spectroscopic techniques [3].

The focus of this work is on near-infrared spectroscopy. This system utilizes near-infrared

light (optical wavelengths from 650 nm to 1000 nm) to obtain information from the tissue inside the body. In this range of optical wavelengths, due to the low absorption of light by water, several centimeters of tissue can be probed. Therefore in this range of wavelength, loss decreases and penetration deep down in the tissue can be done.

A CMOS integrated circuit implementation of a broad-band transceiver was used to perform this measurement. Thus, the applicability and scalability of quantitative diffuse optical imaging (DOI) technology increases, while the cost reduces and it will be more accessible for any purpose.

New human and animal studies, including assessing brain activation, treatment of breast cancer, muscle composition, and metabolism use this imaging system as well. DOI systems are already widespread in commercial health-care devices such as Apple Watch for purposes like oximetry and continuous blood pressure monitoring [4].

As with any optical imaging structure, DOI employs two major components: the source of light and the detector. The principle function of this setup, which is shown in Fig. 1.1, is that the light is transmitted through fiber into the tissue. When the optical signal's characteristics are changed by the tissue, the modified signal is applied to a photodetector that is placed a certain distance from the source. These modifications depend on the interactions between the incident photons and the molecular structure of the tissue. The most important factors that describe these interactions are known as the absorption and scattering coefficients.

The absorption coefficient determines how far the light at a particular wavelength can penetrate into a material before it is absorbed. The material with a low absorption coefficient at a particular wavelength will appear transparent at that wavelength. As a result, each material has its own characteristics for absorption that can be used to determine compound structures [5]. The scattering coefficient, is defined to be a measure of the ability of particles

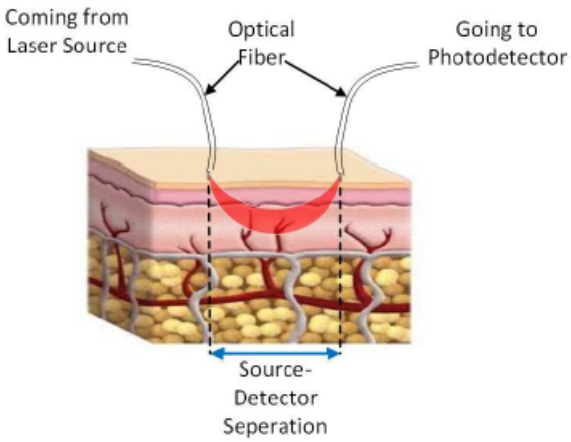


Figure 1.1: DOI system configuration.

to scatter photons out of a beam of light. Both of these parameters are proportional to the number of photons scattered or absorbed per distance (mean free-path). The objective of the whole system is to measure these two factors accurately.

DOI systems can be classified based on their top-level operation. The simplest form of a DOI system is continuous-wave DOI (CW-DOI). A fixed intensity source projects light into the tissue and a photodetector detects the light and compares its intensity with the input. The absorption rate of the medium can be calculated based on the amount of measured attenuation. This system is the least expensive, but incapable of measuring the attenuation of different components of the tissue since it is unable to take the scattering factor into account.

Another method is called time-domain DOI (TD-DOI). In the time-domain approach, a pulse signal modulates the light source. On the detector side, a delayed, attenuated version of the pulse is detected. The quantities of attenuation and pulse widening provide important information about the absorption and scattering coefficients. The drawback of this method is the need for photon counting photodetectors and finer resolution time, which makes the structure's design complex and power-hungry.

A good compromise between the accuracy of TD-DOI and simplicity of CW-DOI is a method

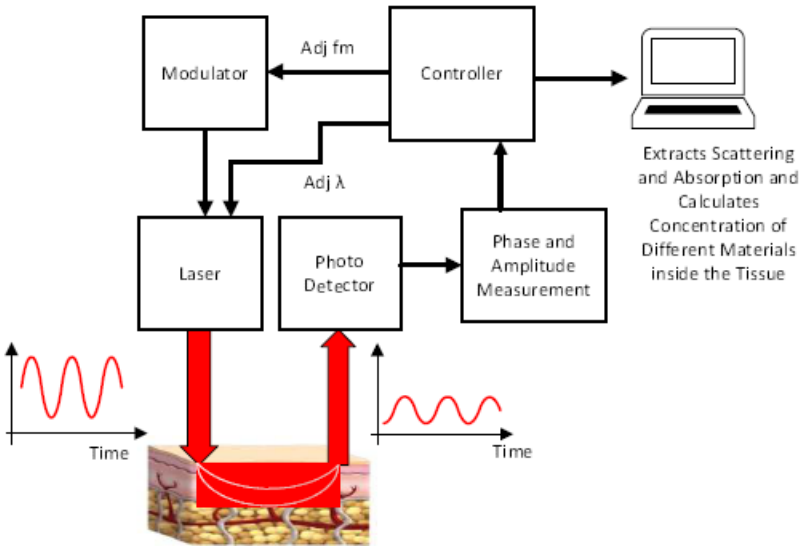


Figure 1.2: fd-NIRS system block diagram.

known as frequency-domain DOI (FD-DOI). As shown in Fig. 1.2, the laser is modulated by laser driver. Following the photodetecor, there is a phase and amplitude measurement block. The analog ouputs of this block are applied to a data acquisition system that is responsible for processing the data coming from measurement units. The results from measurement at different modulation frequencies are applied to analytical formulas [6] in order to determine the absorption and scattering factors at a specific wavelength. This measurement can also be repeated for multiple wavelengths of light. Based on these calculated values, the absolute concentration of different absorbers inside the tissue (e.g. fat, oxygenated, and deoxygenated hemoglobin) can be calculated.

1.2 fd-NIRS Principles

According to FD-DOI principles, photons projected into the tissue have a specific direction. They are scattered by interaction with the tissue, thereby losing their direction and increasing their diffusivity. Fick's first and second laws of diffusion explain and formulate the diffusive flux in steady state and changes in concentration with respect to time.

We assume that the input power source amplitude is sinusoidally modulated:

$$P(t) = P_0(1 + m_0 \sin \omega t) \tag{1.1}$$

where P_0 is the average optical power in [Watts], m_0 is the dimensionless modulation depth and ω is the angular modulation frequency of the source in [rad/sec].

By using the the results coming from differential equations of Fick's laws, the fluence rate at distance r from the sinusoidal source will be [7]:

$$\phi(t) = P_0 \frac{(\exp -r/\delta)}{4\pi D r}[1 + m_0 \exp(-r(k'' - 1/\delta)) \sin(\omega t - k'r)] \tag{1.2}$$

where ϕ denotes the fluence rate in [W/cm^2], r is the distance from origin in [cm], δ is the optical penetration depth in [cm], and D is the diffusion length in [cm]. It can be observed from (1.2) that the modulation amplitude and modulation phase are functions of $\exp(-r(k'' - 1/\delta)$ and $k'r$, respectively. Also k' [cm^{-1}] and k'' [cm^{-1}] are defined to be:

$$k' = \frac{1}{\delta\sqrt{2}} \left[\left(1 + (\frac{\omega}{\mu_a c}) \right)^{\frac{1}{2}} - 1 \right]^{\frac{1}{2}} \tag{1.3}$$

$$k'' = \frac{1}{\delta\sqrt{2}} \left[\left(1 + (\frac{\omega}{\mu_a c}) \right)^{\frac{1}{2}} + 1 \right]^{\frac{1}{2}} \tag{1.4}$$

where μ_a is the absorption coefficient in [cm^{-1}] and c is the speed of light in [m/s]. On the other side, $\delta = \frac{1}{\sqrt{3\mu_a(\mu_a+\mu_s)}}$, where the μ_s is the scattering coefficient. As a result, these two factors can be found by simply solving (1.3) and (1.4).

It is obvious that these two coefficients are dependent on the frequency of the modulation

and the distance between source and the detector. Thus, there are two methods used for measuring the optical properties of the sample in fd-NIRS: multi-distance (MD-FD) and multi-frequency (MF-FD). The first method performs amplitude and phase measurements with multiple source-detector spacing at a single modulation frequency. The trends of these changes in the macroscopic environment are used to determine the optical properties. The multi-frequency method measures alternating attenuation and phase using multiple modulation frequencies at a single source detector distance.

Chapter 2

1st Version Chip

2.1 System Operation

The block diagram of the first version of the chip [8] is shown in Fig. 2.1. A free-running quadrature ring VCO (QRVCO) is used as a frequency synthesizer. The in-phase output of the VCO is filtered by a Gm-C low-pass filter (LPF) to remove harmonics and give a nearly sinusoidal waveform. This signal is applied to an external laser driver, whose emitted light signal reaches the tissue. An attenuated and phase-shifted version of the signal is captured by an avalanche photodiode (APD), which converts optical signals into current. Since the amplitude of this current is very small (in the μA range), it must be amplified and converted to voltage in a transimpedance amplifier (TIA). There is also a variable gain amplifier (VGA) for further amplification. The output of the VGA is fed to the phase detection and amplitude detection units. Finally, the output data is processed by an external controller [9].

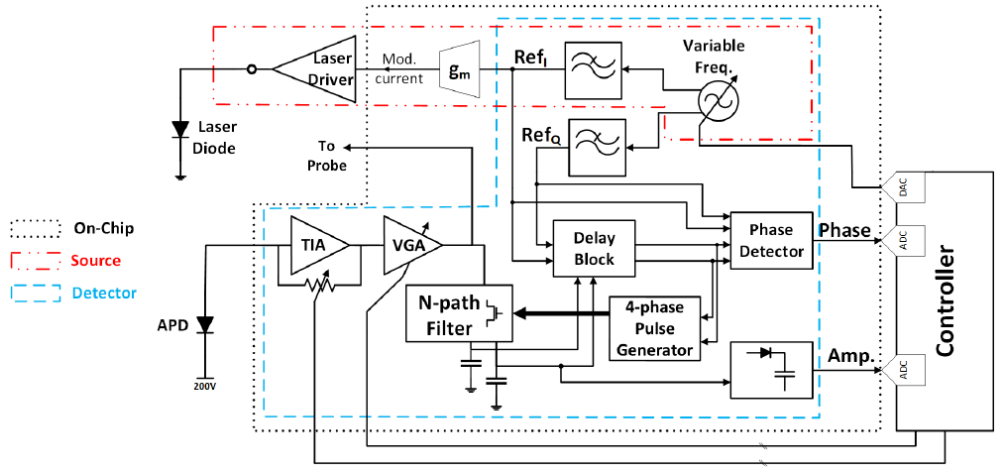


Figure 2.1: 1st version chip's block diagram.

2.2 Frequency Synthesizer

The circuit diagram of QRVCO is shown in Fig. 2.2. This oscillator contains four back-to-back current-starved inverters that act as a bistable circuit. Four feedforward inverters are added to the circuit to prevent latch-up and provide negative transconductance to force the circuit into oscillation. PMOS and NMOS transistors at the top and bottom of the circuit control the total amount of current. The total current determines the delay of each inverter, and thus the frequency of the oscillator. This VCO must cover frequencies from 50 MHz to 1 GHz. The frequency versus control voltage characteristics of this oscillator is shown in Fig. 2.3. According to this curve, K_{VCO} is approximately 1 GHz/V.

This structure was chosen instead of multiple LC oscillators. Although LC oscillators have better harmonic response and phase noise than ring VCOs, they consume more area, which makes them unsuitable for portable applications.

The output of the ring oscillator resembles a square wave, especially at low frequencies. A 4th-order low-pass filter consisting of two 4-stage 2nd-order Gm-C filters is selected to generate a nearly sinusoidal signal for the laser modulation. The corner frequency of this filter can be adjusted between 20 MHz and 1 GHz by adjusting the biasing current of the

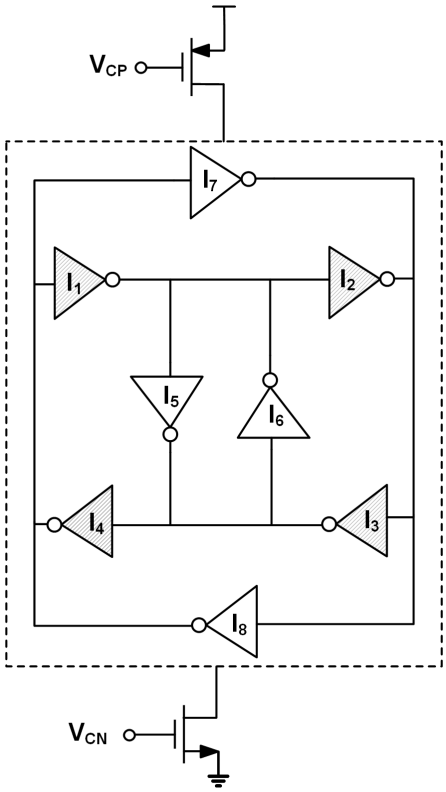


Figure 2.2: QRVCO's schematic.

Gm-C circuit. The 80 dB/decade roll-off provides sufficient attenuation of harmonics to enable clean sinusoidal modulation of the light.

2.3 Receiver

Receiver components include an APD, a TIA, a VGA, and a band-pass filter (BPF). The external APD detects the optical signal and converts it to current. APD selection is determined by the desired wavelength, sensitivity, and speed. There is also an internal amplification function to reduce photodiode noise current. That flows through the TIA. The APD has a large internal capacitor that is connected to the input of the TIA [10]. Therefore, the input resistance of the TIA must be small to provide a bandwidth close to 1 GHz. This block determines the overall sensitivity of the receiver, so it must also have good noise performance.

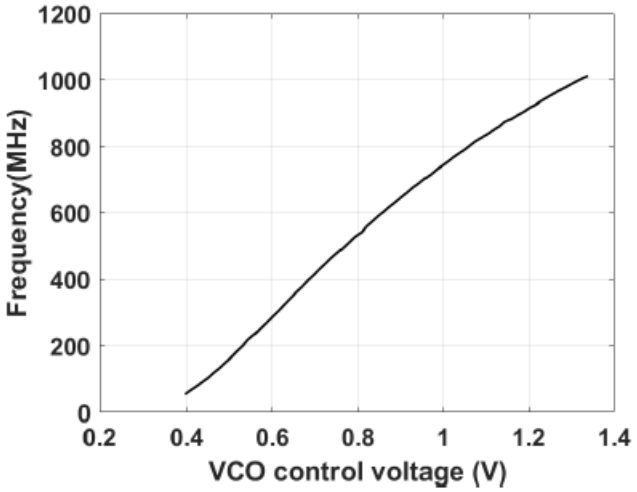


Figure 2.3: Frequency vs. control voltage curve.

To accommodate all these trade-offs, a regulated cascode followed by a simple feedback TIA was chosen [11]. The circuit diagram is shown in Fig. 2.4. The output resistance of M_2 does not affect the overall gain as long as it is large compared to the input resistance of the feedback TIA (i.e. $\frac{R_{fb}}{1+A}$). The input resistance is given by:

$$R_{in} \approx \frac{1}{gm_1(1 + gm_B R_B)} \tag{2.1}$$

As this resistance decreases, the second pole is shifted to a higher frequency, which increases stability (the dominant pole is at the input node). The transimpedance gain is adjusted by the value of the resistor bank, which is adjusted via three switches. The frequency response of the TIA at four gain settings is shown in Fig. 2.5. The highest gain mode is equal to 10 kΩ, which corresponds to all of the MOS switches being open.

Following the TIA, additional amplification is required to bring the detected signal level to values suitable for amplitude and phase measurements. The block diagram of the VGA is shown in Fig. 2.6. As shown in this figure, this block has a variable gain between 8dB and 32dB, which can be set in 8dB steps via two external control bits. It also includes an offset cancellation feedback loop that uses a low-pass filter [12].

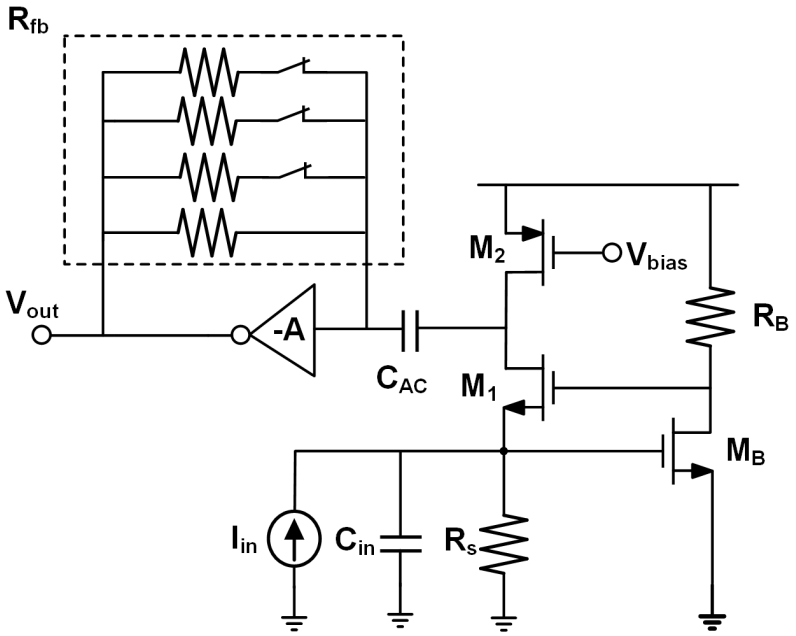


Figure 2.4: Schematic of the TIA.

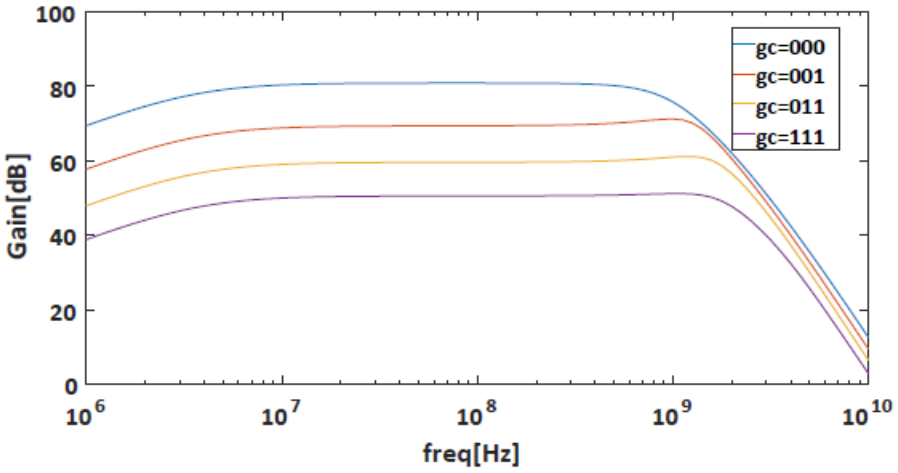


Figure 2.5: Frequency response of the TIA for four gain settings.

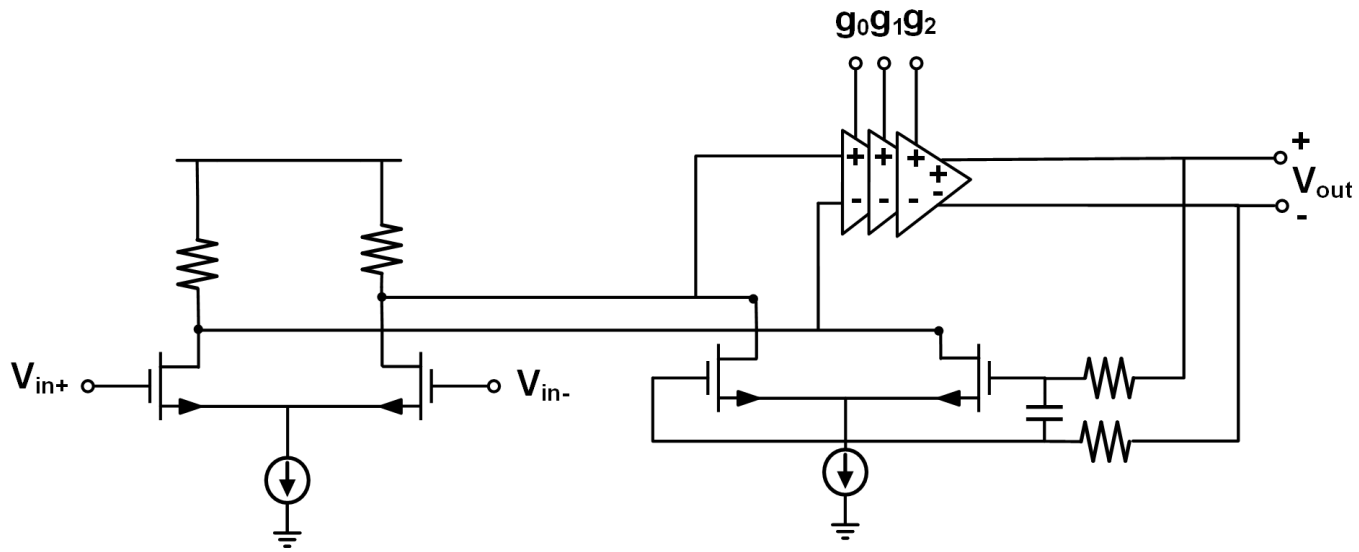


Figure 2.6: Schematic of the VGA.

2.4 Phase Detector

The phase detector architecture is shown in Fig. 2.8(a) [13]. Four orthogonal clock signals are applied to a variable delay circuit whose delay is controlled by a differential voltage V_C. The resulting output signal is applied to a series of AND gates to generate four non-overlapping clock pulses. These pulses are applied to a series of switches connected to capacitors $C0$ and $C90$, forming a 4-path differential filter. Fig. 2.8(b) shows the waveforms of the clock and pulse signals. The effect of the feedback loop is to make the average difference between the two capacitor voltages equal to zero. A voltage-controlled delay cell (VCD) takes the four phases of a clock signal generated by the QRVCO as the inputs and provides four outputs that are delayed versions of each input. The delay can vary over one clock period and is set by the differential control voltage $V_{C+} - V_{C-}$. If the relationship between the control voltage V_C and the VCD delay is known, V_C provides an accurate measurement of phase shift.

To gain better insight into how the circuit works, a simplified form of this filter with two single-ended stages is shown in Fig. 2.9(a). Assuming $R_{in}C$ is much bigger than the clock period, in steady state V_0 (or V_{90}) will be a dc voltage that is very close to the average

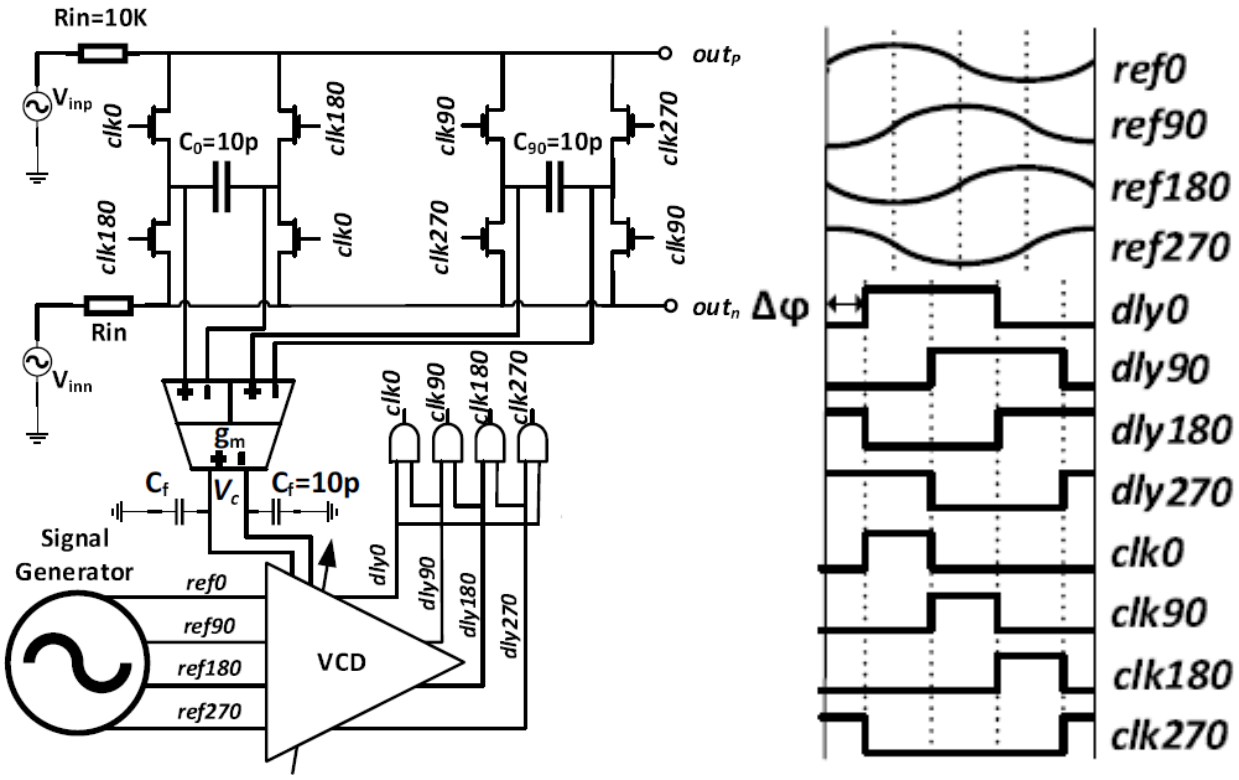
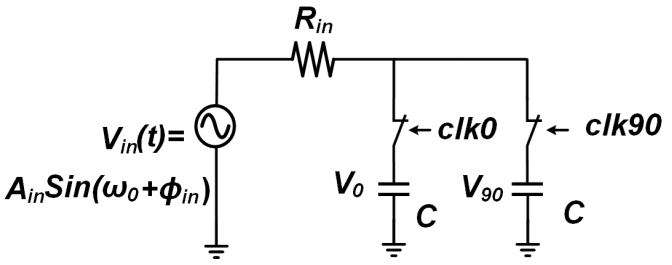


Figure 2.7: (a) Block diagram of the phase detector; (b) clock and pulse signals.

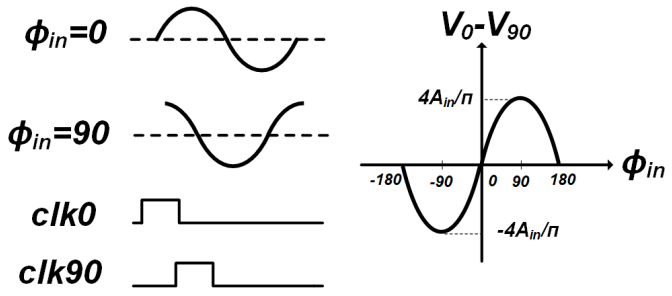
value of V_{in} when $clk0$ (or $clk90$) is high. Fig. 2.9(b) shows two different values of ϕ_{in} and $(V_0 - V_{90})$ vs. ϕ_{in} characteristic. From this figure, it can be seen that equilibrium occurs when the phase difference between the input clock waveform and the delayed clock signal is 0° or 180°. Moreover, the only stable equilibrium corresponds to a phase difference of 0°. Given this equilibrium condition, the phase difference between $ref0$ and $V_{inp/n}$ must be the same as that between $ref0$ and $clk0$.

2.5 Amplitude Detector

To measure amplitude attenuation, a rectifier is required to convert the amplitude to a dc level. Because there is an exponential relationship between the detected amplitude and the sample path length, a logarithmic amplifier whose output is proportional to the logarithm of



(a)



(b)

Figure 2.8: (a) Simplified behavioural model of 4-path filter; (b) two different input phases with $(V_{C0} - V_{C90})$ vs. ϕ_{in} characteristics.

the input is used [14]. The input to this stage is the voltage across one of those capacitors in the 4-path filter, which is proportional to the input amplitude. Therefore, a rectifier is not needed in this case. The outputs of a series of identical saturated amplifiers are summed, as shown in Fig. 2.9. To extend the dynamic range and enable measurement of high amplitude inputs, an attenuation stage is added that saturates after all other blocks saturate.

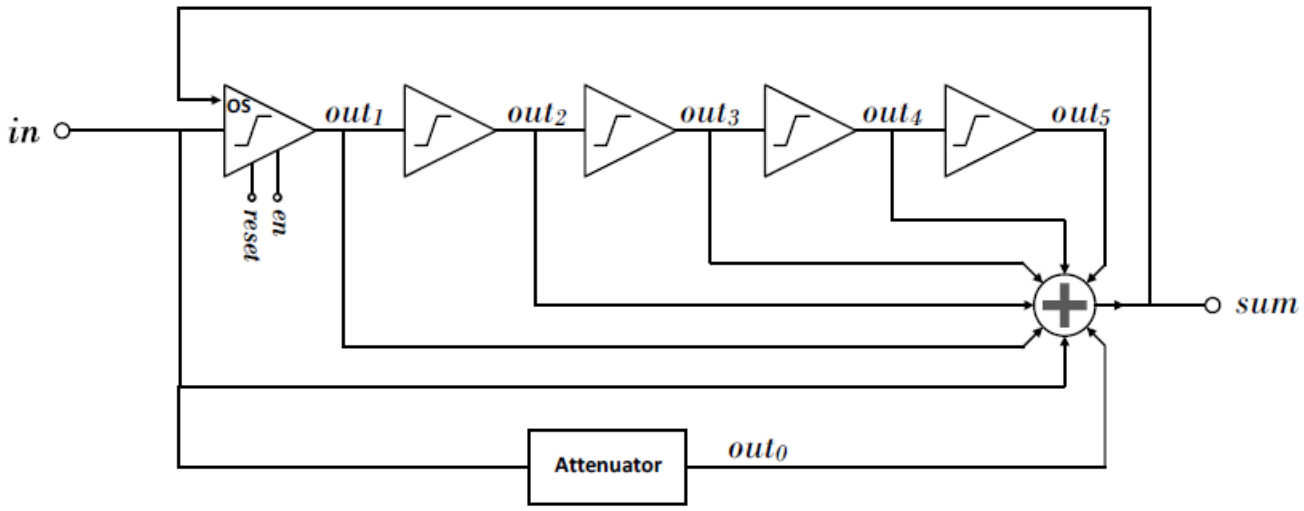


Figure 2.9: Block diagram of the amplitude detector.

Chapter 3

2nd Version Chip

3.1 System Operation

As explained in the previous sections, the main purpose of the fd-NIRS system is to measure the differences in phase and amplitude between the output signal of the laser driver and the signal detected by the photodiode after passing through the tissue. The sensitivity of the system depends on the accuracy of the phase and amplitude measurement units. In the first version of the chip, measurements showed a detection range of more than 60 dB. Meanwhile, the root mean square (RMS) phase error was 2.1°. Therefore, it is necessary to modify the phase measurement unit to improve the accuracy to less than 1°.

The most difficult task of the chip is processing two signals with large differences in amplitude. The phase difference between these two signals cannot be detected by traditional architectures such as simple XOR gates. On the other hand, the same principle can be used for the time interval of zero crossing points. For this reason, the second version uses an heterodyned architecture [15].

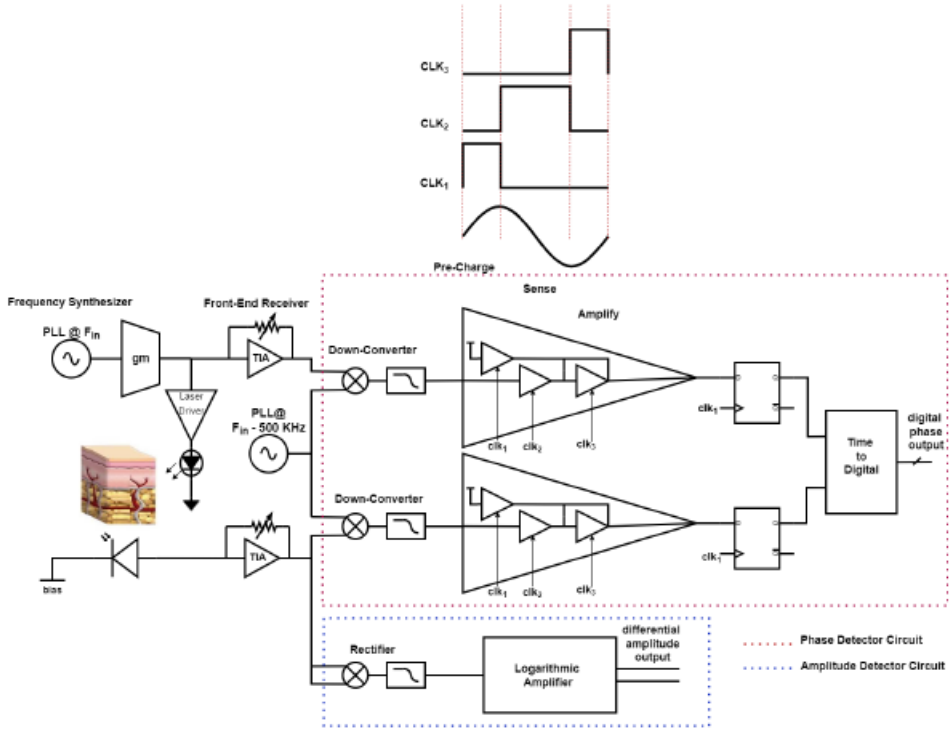


Figure 3.1: 2nd version chip's block diagram.

The block diagram of the system is shown in Fig. 3.1 [16]. The frequency synthesizer consists of a phase-locked loop rather than a free-running VCO for modulating the laser driver. To amplify the received signal, the receiver front end has a wide-band differential feedback TIA. It then passes through a down-conversion mixer and low-pass filter. The reason for down-converting the signal will be discussed shortly. An innovative limiting amplifier is used in the phase measurement section. This limiting amplifier consists of three stages. During the first phase of the clock, the signal is pre-charged to 0.5 V and the drain-source voltage of the transistors reaches the edge of saturation. In the second and third phases of the clock signal, the signal is amplified. During the last phase of the clock, the limiting amplifier's latch mode is activated and a rail-to-rail signal is provided at the output. The reason for using such a structure is that it is difficult to design a limiting amplifier without introducing amplitude-dependent offsets. This behavior is illustrated in Fig. 3.2 for two in-phase signals with different amplitudes. This limiting amplifier has a fixed delay over a two-decades range

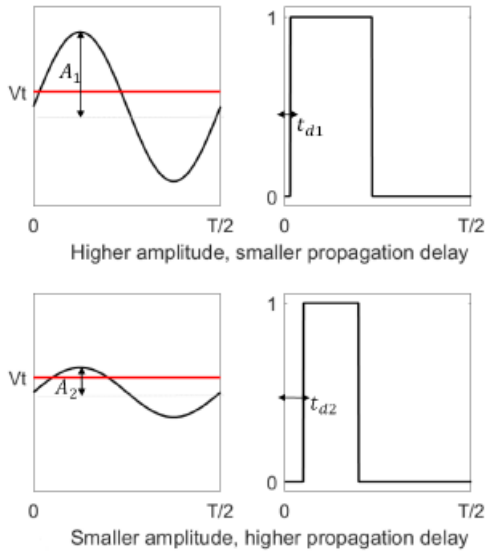


Figure 3.2: Amplitude dependent time-offset of limiting amplifier.

of input amplitude.

The amplitude-dependent phase error introduced by the limiting amplifier determines the overall system phase error and depends on the input signal frequency (f_{in}) and its own clock frequency (f_{clk}):

$$Maximum\ phase\ error\ of\ the\ limiting\ amplifier = 360° \times \frac{f_{in}}{f_{clk}} \tag{3.1}$$

To obtain measurements of better than 1° accuracy at the maximum input frequency of 1 GHz, the clock signal would need to be 360 GHz, which is impractical for the CMOS process being used. For this reason, a down-conversion part is proposed that allows the design and functionality of this limiting amplifier feasible.

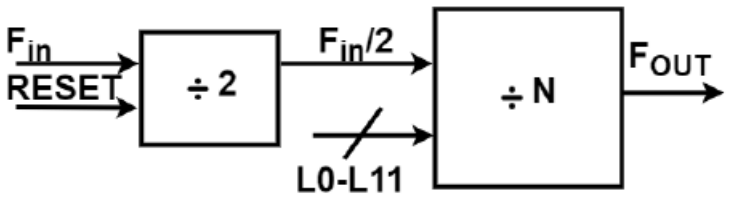


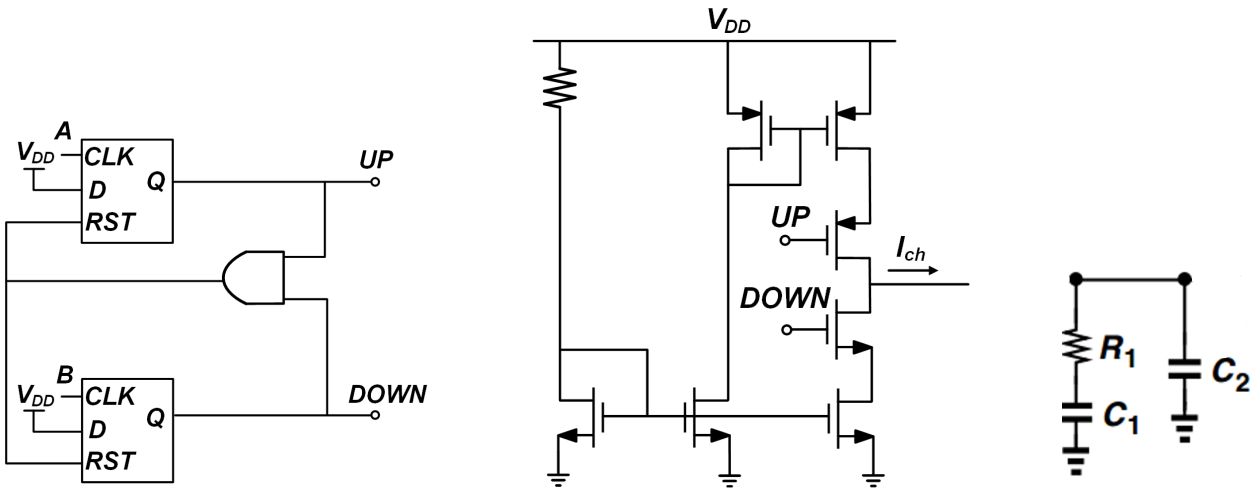
Figure 3.3: Frequency divider building block.

3.2 Frequency Synthesizer

As in the first version, a frequency synthesizer is required for laser driver modulation. However, there is significant difference between the first and second versions of the frequency synthesizer. In the second version, the free-running QRVCO used in the first version was replaced with a phase-locked loop. This VCO is used inside the PLL loop because the measurements of the previous version showed large amount of jitter at the output of the free-running QRVCO [17]. A rigorous analysis on this circuit was done in [18]. This VCO has a tuning range from 50 MHz to 1 GHz.

Since optical measurements of the tissue require a resolution of 500 kHz, the frequency divider of this PLL must be programmable and the maximum reference frequency provided by an off-chip crystal oscillator is limited to 250 kHz. Therefore, the minimum and maximum values of the divider ratio are $\frac{50MHz}{2\times250kHz} = 100$ and $\frac{1GHz}{2\times250kHz} = 2000$, respectively. A block diagram of this circuit is shown in Fig. 3.3. As shown in this figure, this block contains a divide-by-2 circuit with reset and an 11-bit synchronous down counter.

The PLL's phase-frequency detector (PFD) block is shown in Fig. 3.4(a) and consists of a positive edge-triggered D flip-flop with an asynchronous reset. The charge pump circuit shown in Fig. 3.4(b) is used to convert the delay-dependent output voltage of the PFD into a current that drives a second-order loop filter which is illustrated in Fig. 3.4(c). PLL loop stability and trade-off analyses are discussed in detail in the next chapter. The optimized



(a) (b) (c)

Figure 3.4: (a) Block diagram of the PFD; (b) charge-pump circuit; (c) loop filter.

loop parameters of the wide-band low jitter PLL are shown in Table 3.1.

parameters	optimum value
I_{ch}	15 μA
K_{VCO}	1 GHz/V
R_1	10 kΩ
C_1	8 nF
C_2	4 pF
Power consumption	3.51 mW @ 500 MHz

Table 3.1: PLL's final specifications.

3.3 Receiver

The receiver part of the chip consists of an off-chip APD and an on-chip TIA. The optical signal is detected and converted to current by a photodiode, which is then amplified and converted to voltage by a TIA. The structure of this differential TIA is shown in Fig. 3.5. Use of a differential circuit topology suppresses common-mode noise.

This structure uses two gain modes (1 kΩ and 10 kΩ) for an input range of 1 μA to 100 μA to avoid non-linear behavior. As previously mentioned, the TIA must be designed to

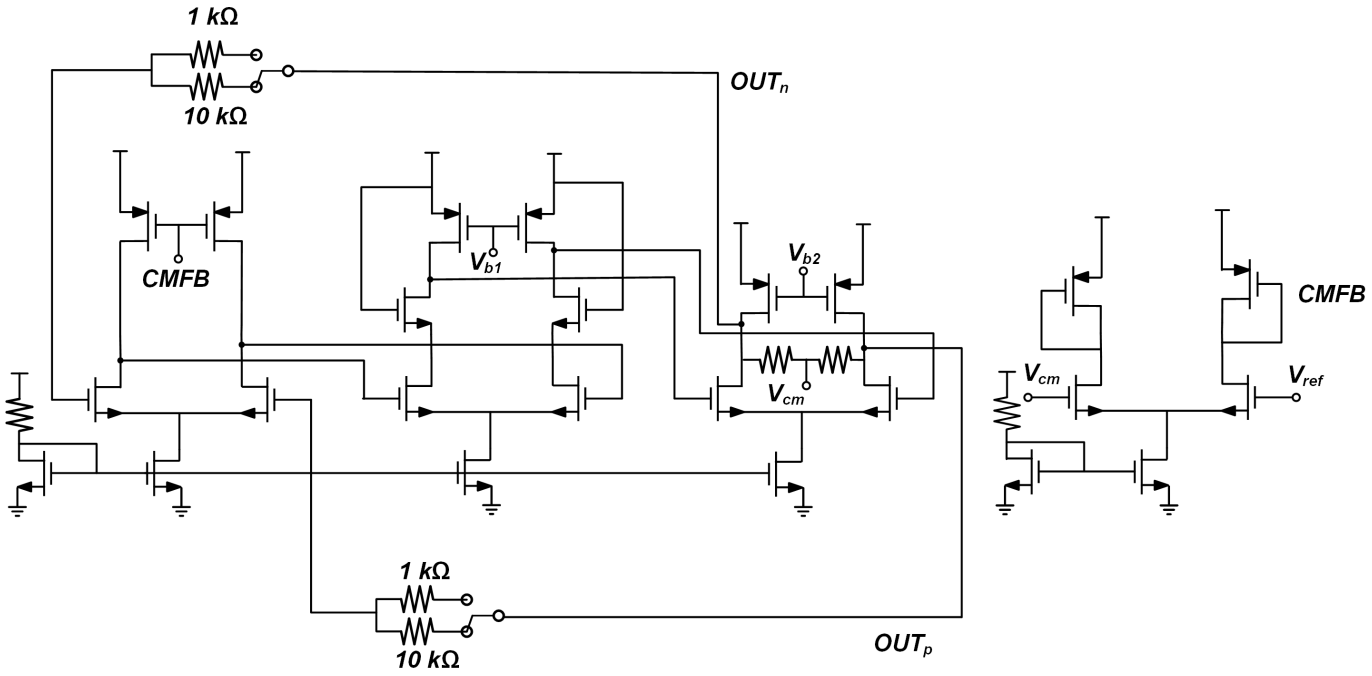


Figure 3.5: Schematic of the TIA.

meet the bandwidth and sensitivity requirements of the fd-NIRS system. Due to the large parasitic capacitance of the APD which is around 2 pF according to the Hamamatsu S12023 series Si-APD datasheet, the input impedance of the TIA must be set to a low value. To handle bandwidths up to 1 GHz, the maximum input resistance of the TIA is calculated as follows:

$$R_{in} = \frac{1}{2\pi C_P f} = \frac{1}{2 \times \pi \times 2 \times 10^{-12} \times 10^9} \approx 80\Omega \tag{3.2}$$

For the highest gain mode with $R_F = 10$ kΩ, the open-loop gain must be greater than 124. The first stage of the TIA utilizes small transistors in order to provide the required bandwidth. The second stage provides most of the required gain, and the third stage can provide up to 100 μA of output drive current.

Fig. 3.6 shows the Bode plot of the open-loop TIA response for both gain modes. The phase margins are 47.6° and 66.4° in low-gain and high-gain modes, respectively.

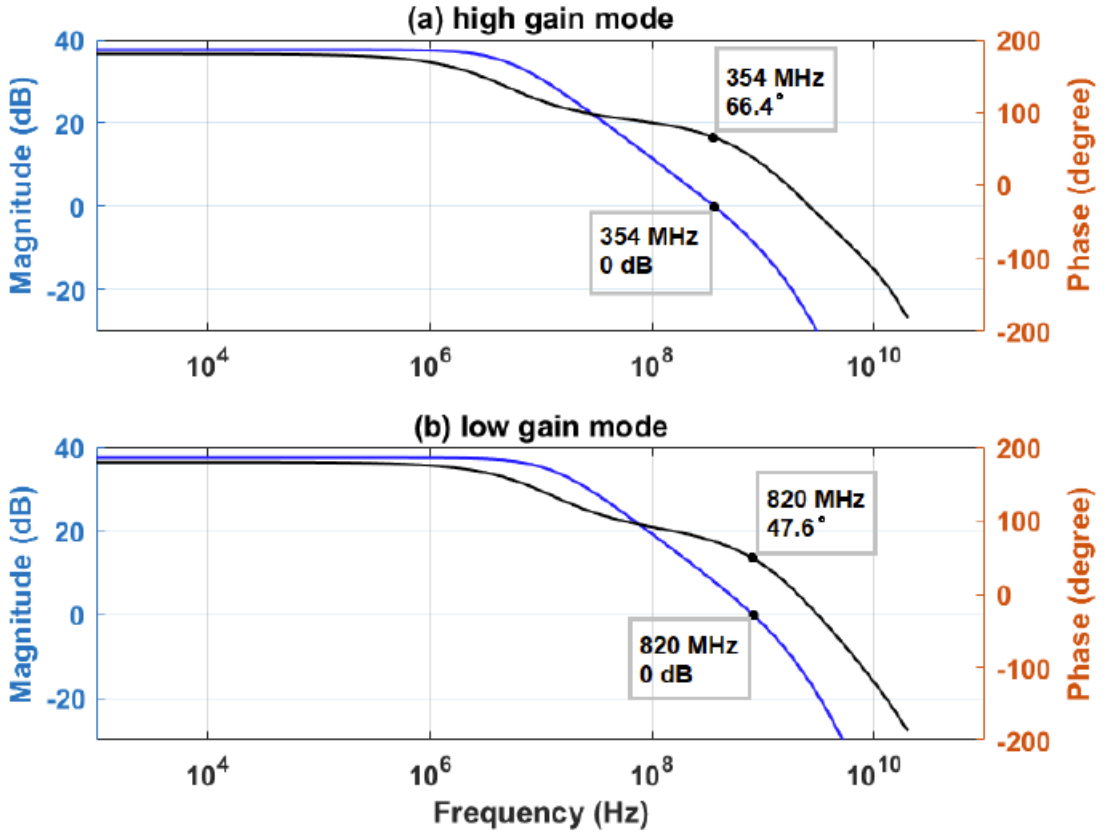
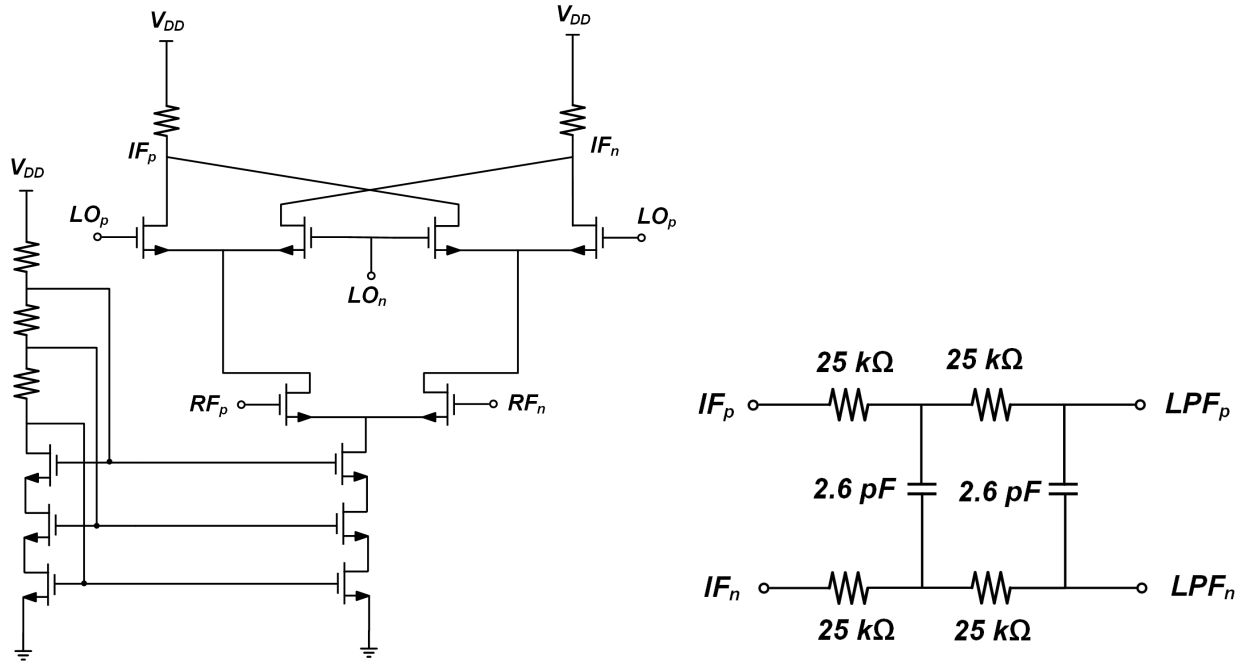


Figure 3.6: Bode plot of the open-loop TIA.

In terms of noise performance, the TIA's input-referred noise is 2.4 μA. However, the down-conversion mixer and LPF reduces this level.

The down-convertion mixer is used to down-convert the RF signal to an IF of 500 kHz at the output. As mentioned earlier, this stage is intended to enable the design of limiting amplifier for accurate phase measurements. The schematic of a double-balanced active mixer, whose tail current is 40 μA, with triple cascode current mirror is shown in Fig. 3.7(a). The triple cascode current source has a very high output impedance, which reduces the modulation effects of the second harmonic of the input signal.

The mixed IF signal is filtered by the on-chip second order passive low-pass filter shown in Fig. 3.7(b). This LPF further improves the overall sensitivity of the system.



(a) (b)

Figure 3.7: (a) Schematic of the mixer circuit; (b) on-chip LPF.

3.4 Phase Detector

Phase measurement between the reference and the detector outputs requires amplifying the down-converted sinusoidal signal to rail-to-rail levels and measuring the time interval (or phase difference) with an accuracy of less than 1°. For this purpose, a limiting amplifier that is independent of the input amplitude for two decades is designed and shown in Fig. 3.8(a).

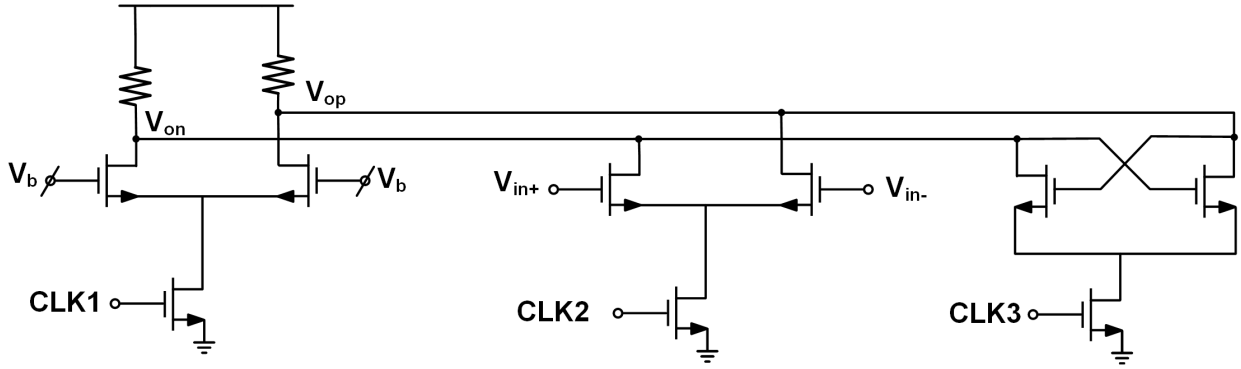
Based on the simulations, one quarter of the clock cycle is allocated to the first and third stages. To achieve input-independent time-delay operation, the other half period of the clock signal is applied to the second stage. For generating non-overlapping clock signals, a three-phase clock circuit is used. The circuit diagram is shown in Fig. 3.9(a). The reference clock is obtained from a separate PLL with a fixed output frequency of 1.44 GHz. As a result, each phase has $\frac{1.44\,GHz}{4} = 360$ MHz frequency. Fig. 3.9(b) shows the results of a transient simulation of the three-phase clock circuit.

This limiting amplifier has three stages for pre-charging the input signal, amplifying (sensing), and generating a full swing square wave signal (latching) at the output. The simulation results of this circuit are shown in Fig. 3.8(b).

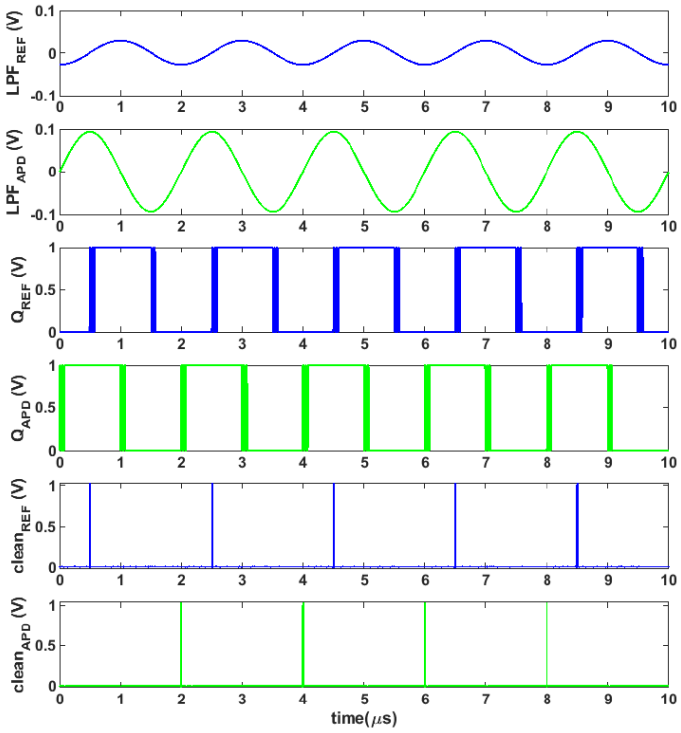
To remedy the bouncing edges, a debounceing circuit was designed. Then, a time-to-digital unit comes after it to generate the digital phase output.

3.5 Amplitude Detector

This chip's amplitude detector has the same architecture as the first version and it was discussed in Section 2.4.

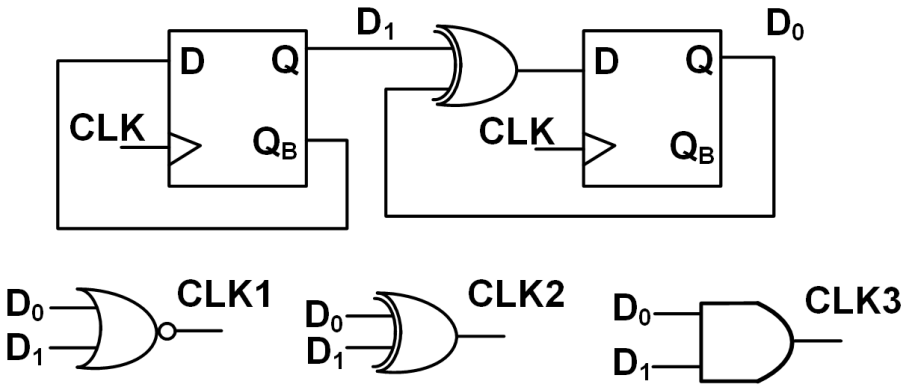


(a)

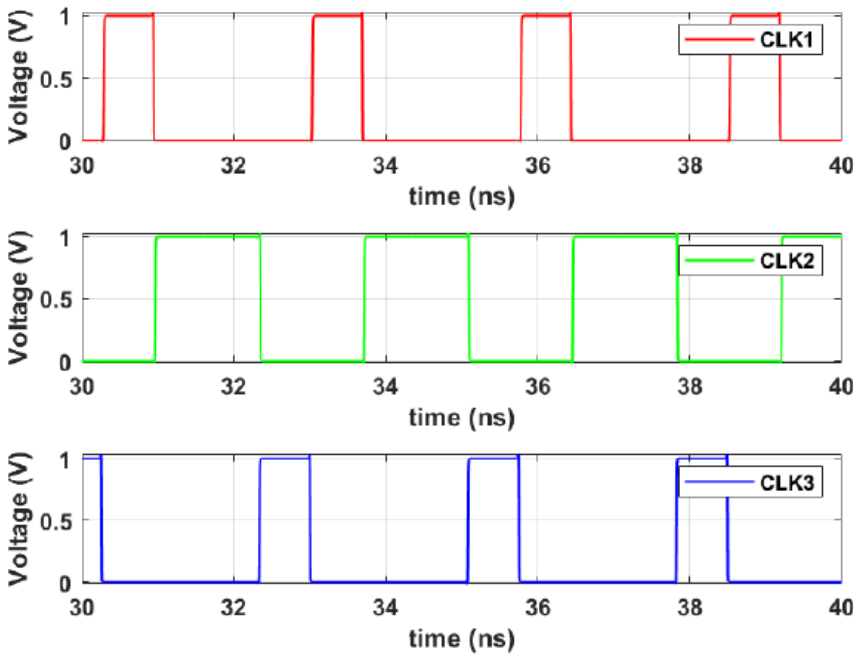


(b)

Figure 3.8: (a) Schematic of the limiting amplifier circuit; (b) transient response of the limiting amplifier circuit.



(a)



(b)

Figure 3.9: (a) Schematic of the three-phase clock circuit; (b) transient response of the three-phase clock circuit.

Chapter 4

3rd Version TX Design

4.1 System operation

One can see the gradual changes from the first version to the second version. For example, a PLL was used in version 2 instead of a free-running VCO, which was used in version 1 to significantly reduce the jitter of the reference signal. In the third version, the main goals are to enhance the portability of the system, implement the laser driver on the chip, which in the previous versions was an external block, and to change the structure of the second version according to different frequency ranges and resolution. This chapter describes transmitter chain design and its simulation results.

The block diagram of the TX chain is shown in Fig. 4.1. The sine wave comes from the PLL, whose output frequency range is from 50 MHz to 500 MHz. A source follower and a VGA are then designed to make the dc and amplitude levels of the signal large enough to drive the input differential pair of the laser driver. It is important to modulate the laser diode with a well-shaped sine wave whose first harmonic is at least 20 dB higher than other harmonics. The optical signal that is the output of the laser diode is transmitted through the tissue and

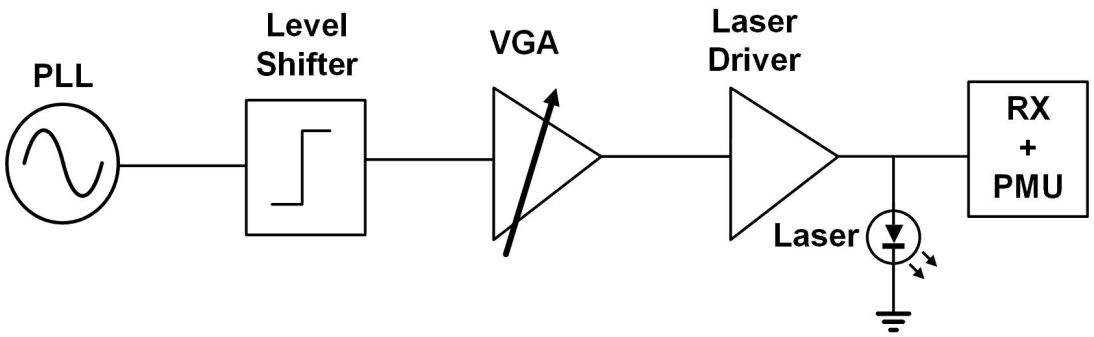


Figure 4.1: TX chain.

detected by the APD. As shown in Fig. 4.1, the front-end and phase measurement unit are also located in the TX section of this optical transceiver, similar to the structure of version 2 which was depicted in Fig. 3.1. The reason is that all these blocks cause an additional phase shift at the RX chain, and this replica compensates for the delay added to the detected signal. It is noteworthy that only the phase shift due the molecular composition of the tissue must be measured and there shouldn't be any additional delay due to the proceeding blocks. Also note that in this version, the output of the laser driver is a current-mode signal and can be applied directly within the TIA, thus the g_m block in the second version block diagram (Fig. 3.1) is no longer needed.

This version has some changes to reduce the number of pins compared to the previous chip to make the device wearable. For this reason, instead of having multiple input pins and connecting them to ground or V_{DD}, a serial-to-parallel converter programs the divider's division ratio with just one signal from the micro-controller. The laser driver is used to control five laser diodes, each with different characteristics. But only one laser will be connected to the board for each measurement. These lasers require different dc and ac current to properly emit optical power. This was the most challenging part of the blocks' design, as it allowed us to meet all the laser diode specifications which will be studied later.

The design procedure and post layout simulations of these circuits will be discussed in detail

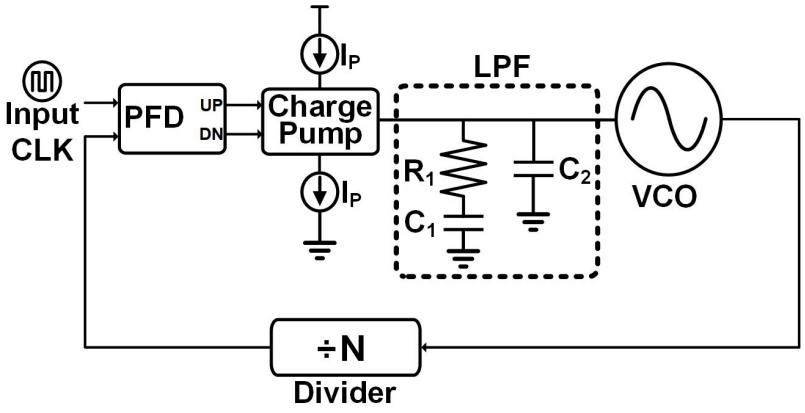


Figure 4.2: Traditional Type-II PLL.

in the next sections.

4.2 PLL Design Procedure

The block diagram of a traditional Type-II PLL is illustrated in Fig. 4.2. In the third version chip, the amount of resolution is coarser and instead of a 11-bit divider, an asynchronous 8-bit divider is used. As a result, the reference crystal oscillator's frequency is 8 times higher than that of the previous chip and is a 2 MHz square-wave signal.

The first block in the PLL system is PFD. The block diagram of the PFD was shown before in Fig. 3.4(a). The resettable DFF circuit is shown in Fig. 4.3 [19]. This circuit has some speed limitations. But this is a minor problem since ω_{in} is much lower than ω_{out} in this integer-N PLL. The simulation result for this PFD is shown in Fig. 4.4 (before lock). The reference signal comes from the crystal oscillator and feedback signal comes from the output of the divider. The AND gate resets the DFFs if up and down signals are logic one. The output of the PFD is directly applied to the charge-pump circuit in Fig 3.4(b). The amount of output current is 57 μA.

The ring VCO block in this design has the same structure as previous chips and was discussed

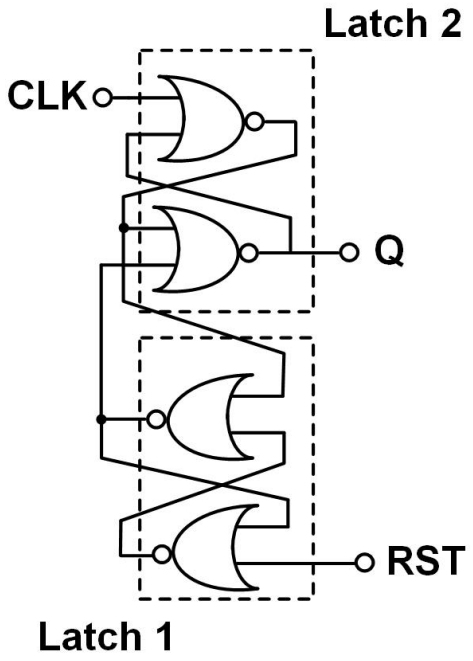


Figure 4.3: Resettable DFF.

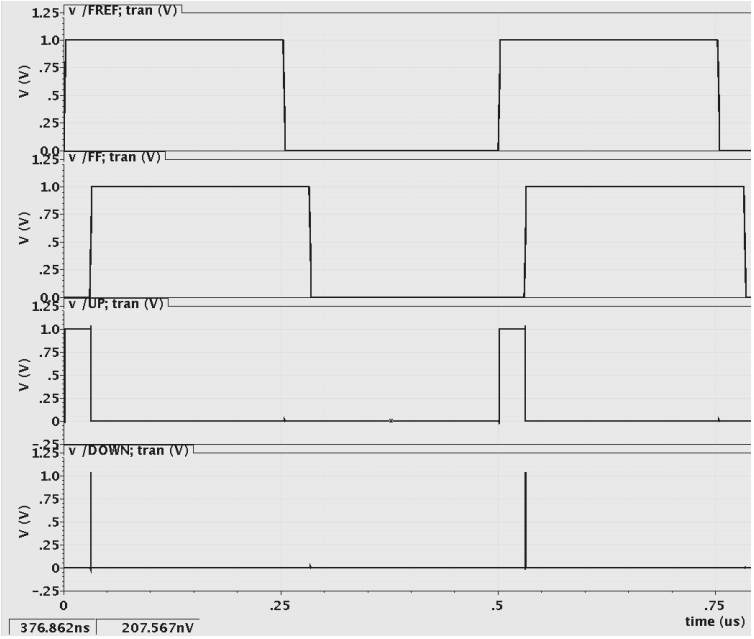


Figure 4.4: Transient response of the PFD.

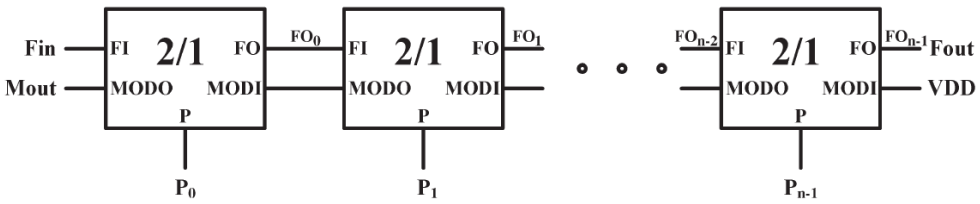


Figure 4.5: Proposed N-stages programmable frequency divider

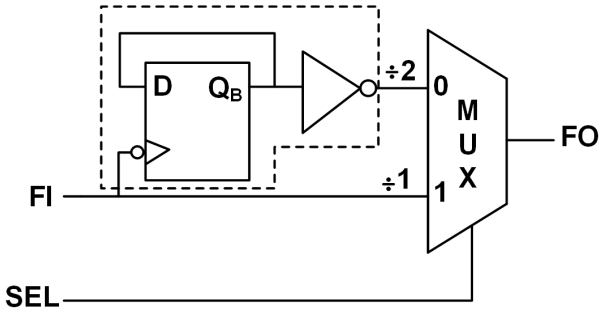


Figure 4.6: Concept of a (2/1) divider cell.

in detail in the previous chapters.

The N-stage programmable frequency divider, which is shown in Fig. 4.5, is proposed in [20]. This structure receives input signals F_{in}, V_{DD}, and programmable values (p_{n-1}, ..., p_1, p_0). The output signals are F_{out} and M_{out}. Note that the $MODO$ signal is active only once per F_{out} division period in each cell. Therefore, the divider provides an output signal F_{out} with a period of:

$$T_{out} = (2^n - 2^{n-1}p_{n-1} - 2^{n-2}p_{n-2} - ... - 2^1 p_1 - 2^0 p_0) \times T_{in} \tag{4.1}$$

As the name suggests, the (2/1) divide cell contains both a divide by 2 function and a divide by 1 function. Fig. 4.6 shows a simple 2/1 cell where a multiplexer (MUX) uses its SEL signal to select a divide ratio of either 1 or 2. The (2/1) frequency divider cell block diagram in Fig. 4.7, receives three input signals FI, $MODI$, and P and produces two output signals $MODO$ and FO. A master-slave DFF is used in this design.

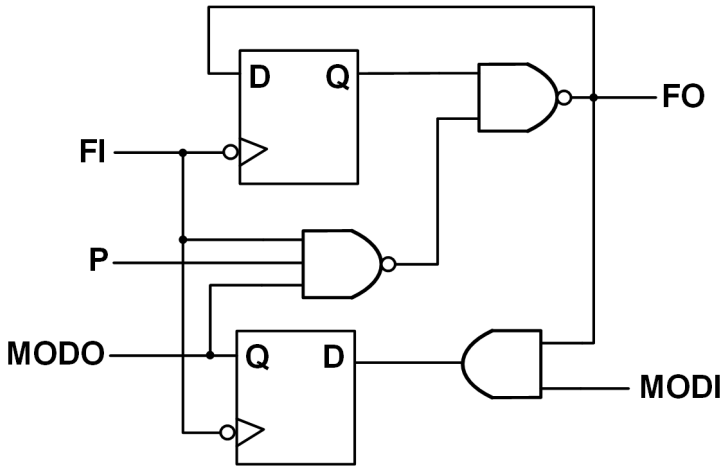


Figure 4.7: Proposed (2/1) divider's block diagram.

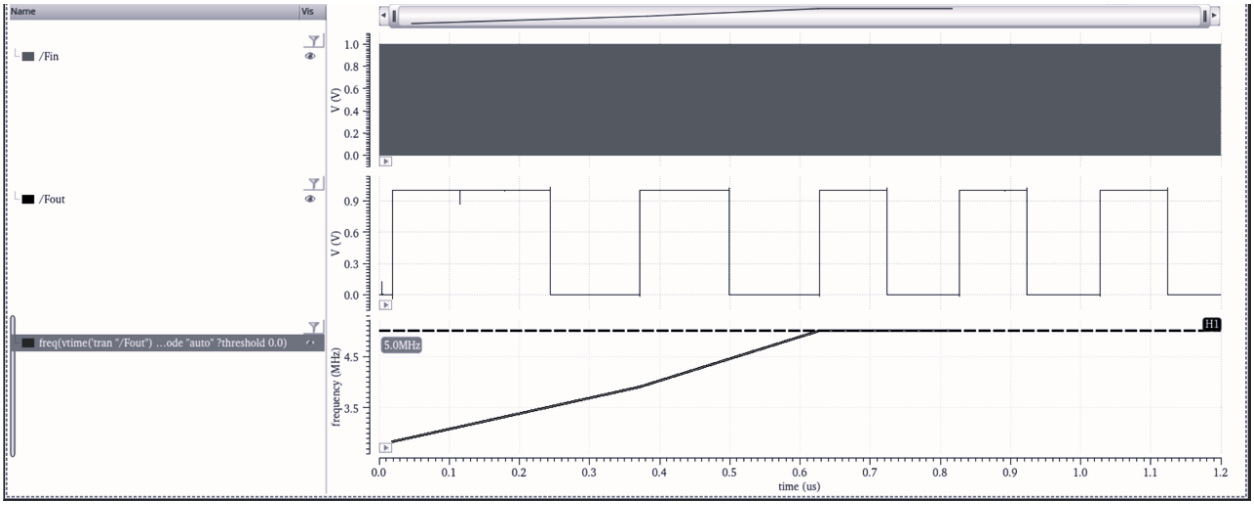


Figure 4.8: Simulation results of the divider with F_{in} = 500 MHz and N=100 and its output transient response with time dependent frequency of the output.

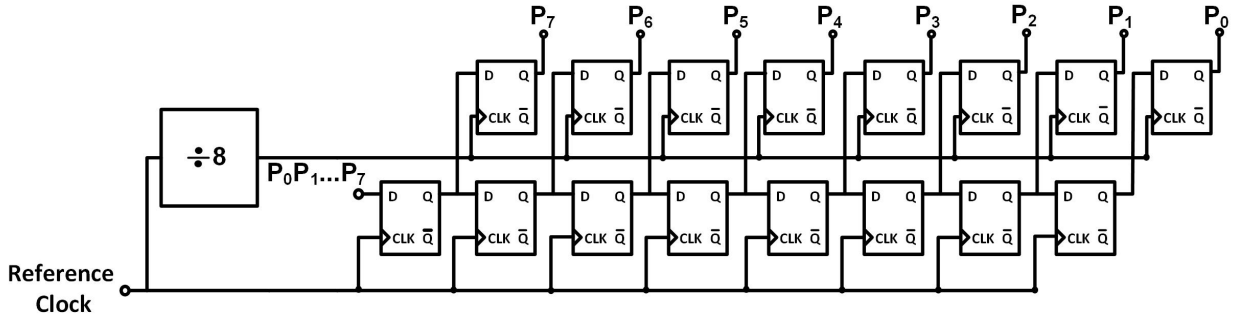


Figure 4.9: 8-bit serial-to-parallel converter's schematic.

Simulation results for the highest input frequency which is 500 MHz in our case, with $P_7P_6...P_0 = 10011100$ (translated to N=100 according to (4.1)) is illustrated in Fig. 4.8. At steady state, 5 MHz can be seen at the output.

To reduce the number of pins compared with the previous version, an 8-bit serial-to-parallel converter (Fig. 4.9) was designed to obtain a specific sequence of bits ($P_0P_1...P7$) serially from a hardware microcontroller [21, 22] and then apply it to the selection bits of the divider in parallel. This sequence of bits determines the divide ratio.

In order to arrive at a stable and low-jitter PLL design, we must properly select the loop filter components. The loop filter consisting only of R_1 and C_1 proves to be insufficient as it does not sufficiently suppress the ripple even when the loop is locked. The reason is when the charge pump current, due to propagation mismatches within the PFD, flows through R_1, instantaneous changes occur in the control voltage. A common approach to reduce this ripple is to connect a capacitor (C_2) directly from control voltage line to ground. To ensure the stability of the PLL, the open loop transfer function is derived as:

$$H(s) = \frac{I_{ch}K_{VCO}}{N} \cdot \frac{1}{s^2(C_1 + C_2)} \cdot \frac{1 + RC_1 s}{1 + R\frac{C_1C_2}{C_1+C_2}s} \tag{4.2}$$

The Bode plot of this transfer function is illustrated in Fig. 4.10. In order to have a stable loop, the phase margin must be at least 60°. The best way to ensure the stability of this

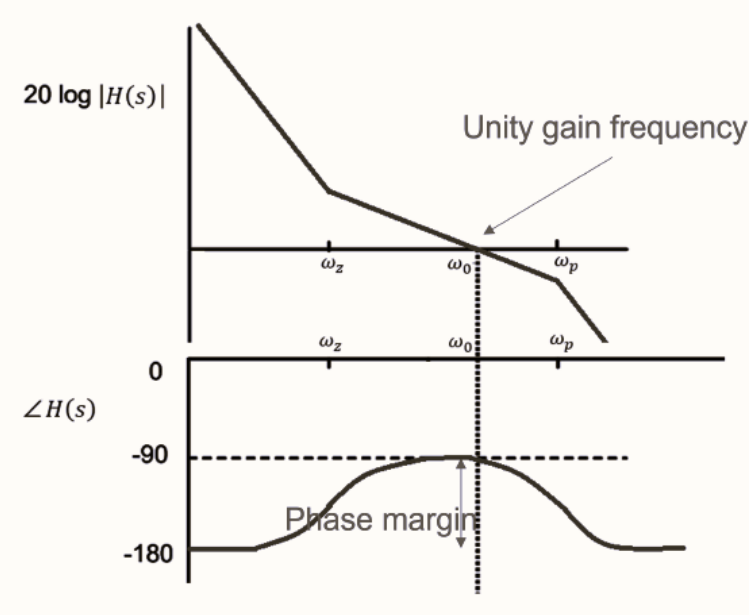


Figure 4.10: Bode plot of the open loop transfer function of the PLL.

loop is to put at least one decade distance between ω_z (zero frequency) and ω_0 (unity-gain frequency), and ω_0 and ω_p (pole frequency). As a result the stability criteria is going to be:

$$\omega_z << \omega_0 << \omega_p \tag{4.3}$$

In this case, the unity-gain frequency will be calculated by setting the magnitude of (4.2) with $s = j\omega_0$ equal to unity which is derived to be:

$$\omega_0 \approx \frac{I_{ch} K_{VCO} R}{N} \tag{4.4}$$

Combining (4.3) and (4.4), we have:

$$\frac{1}{RC_1} << \frac{I_{ch} K_{VCO} R}{N} << \frac{1}{R\frac{C_1 C_2}{C_1+C_2} s} \tag{4.5}$$

Equation (4.5) determines a minimum value for C_1 and maximum limit on C_2.

There is a trade-off between stability and timing jitter. If we choose $C_2 << 0.01C_1$, we

can clearly see that there is a phase margin near 90°. On the other hand, if C_2 is chosen to be too small, the control voltage ripple cannot be filtered out and jitter will appear at the output. With these design compromises taken into account, the loop filter components were chosen as shown in Table 4.1. Note that the third version has a smaller divide ratio and larger loop bandwidth, which removes unwanted components from the VCO, especially those that contribute to high-frequency phase noise [23].

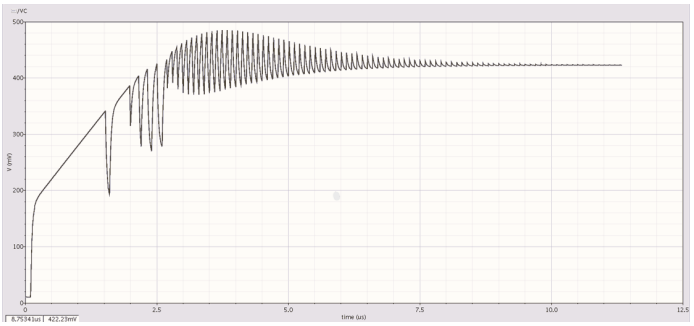
The PLL simulation results are shown in Fig. 4.11. This simulation result applies to f_{out} = 500 MHz. The transient response of the control voltage in Fig. 4.11(a) shows that in steady state, the control voltage remains nearly constant, with ripple no more than few milivolts. Although the amount of ripple in this condition is small, it will cause deterministic jitter at the output of the VCO. For instance, the duty cycle distortion in the feedback signal can be observed in the Fig. 4.11(b) waveform. Duty cycle distortion is a special type of deterministic jitter caused by circuit mismatches. In the PLL loop, it can originate from charge-pump non-idealities or divider based on the divide ratio. The differential output of the VCO is also shown in the Fig. 4.11(c).

parameters	optimum value
R_1	3 kΩ
C_1	450 pF
C_2	10 pF

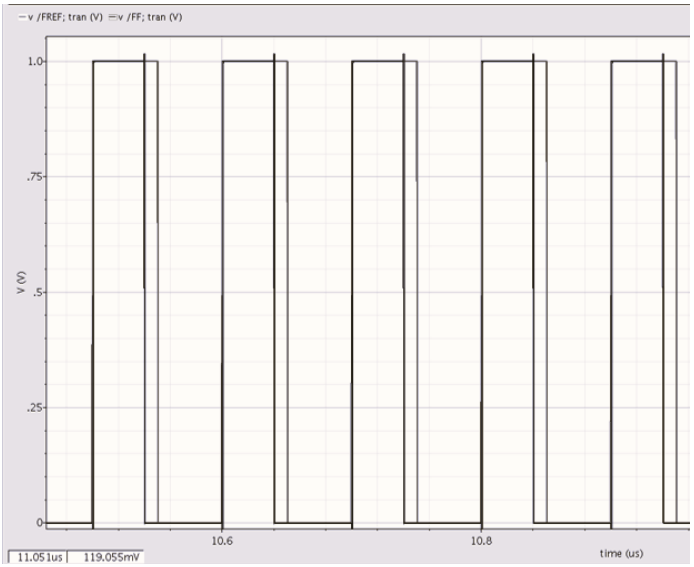
Table 4.1: Loop filter components

4.3 Intermediate stages between PLL and laser driver

The intermediate stages contain a source follower, which functions as a level shifter, and a VGA whose gain is manually controlled off-chip. The output of the PLL is a signal containing



(a)



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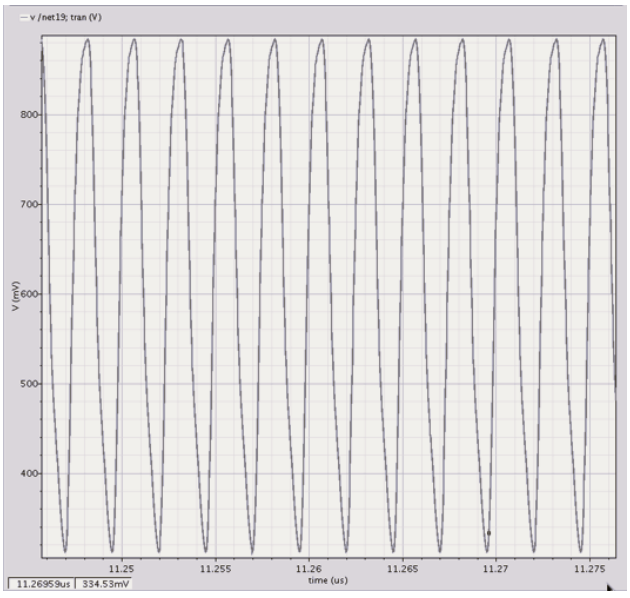
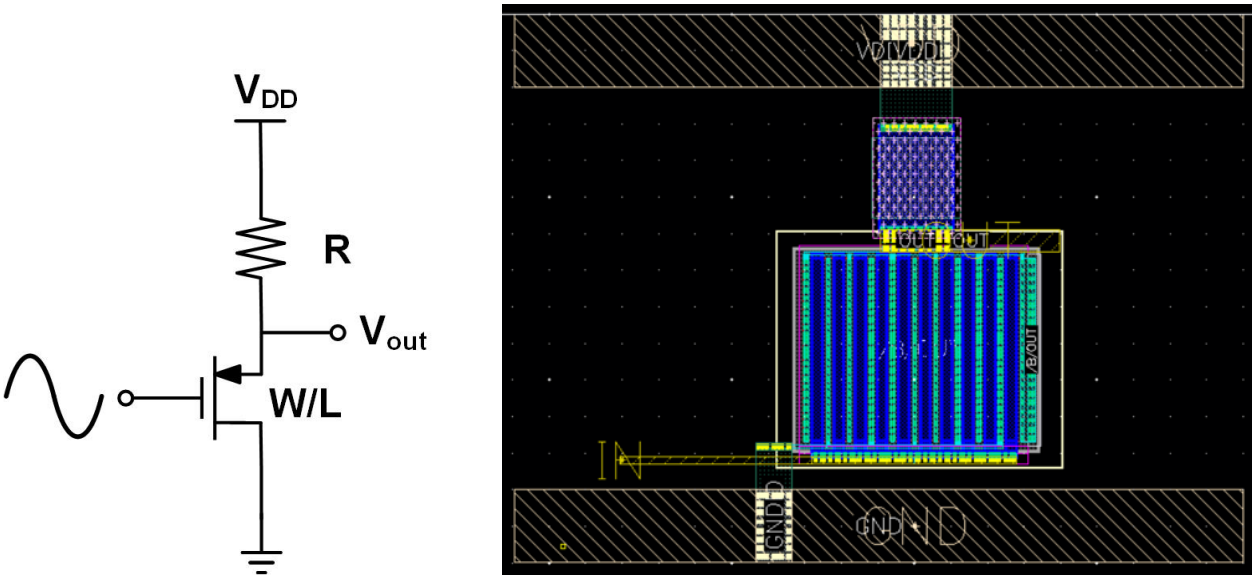


(c)

Figure 4.11: (a) Control voltage; (b) reference and feedback signals; (c) differential output of the VCO.



(a) (b)

Figure 4.12: (a) Schematic of the source follower; (b) layout of the source follower.

a fixed dc level, but with different amplitudes at different frequencies. The laser driver must conduct a large amount of current on the order of tens of mA. Thus, all the transistors in these stages are thick oxide 2.5 V transistors rather than standard 1 V MOSFETs. These high-voltage transistors have higher threshold voltages as well. Therefore, high dc and ac levels are required to turn on and off the input differential transistors of the power stage. A source follower, whose schematic and layout are shown in Fig. 4.12, is used to increase the dc level of the PLL output from 0.6 V to 1.5 V. To achieve the correct level shift, a dc sweep was performed from which the correct resistor value was determined. The simulation results in Fig. 4.13 show that the resistance value needs to be 687.4Ω to obtain a 1.5 V dc voltage at the output node.

The output amplitude of the VCO depends on its frequency. The frequency range for this application is 50 MHz to 500 MHz. Furthermore, the VCO's output amplitude varies according to the frequency of operation. Thus, the amplitude must be sufficiently amplified to certain values based on the characteristics of the laser diodes. This is why the VGA, whose schematic and layout are shown in Fig. 4.14 was implemented. The role of the n-channel

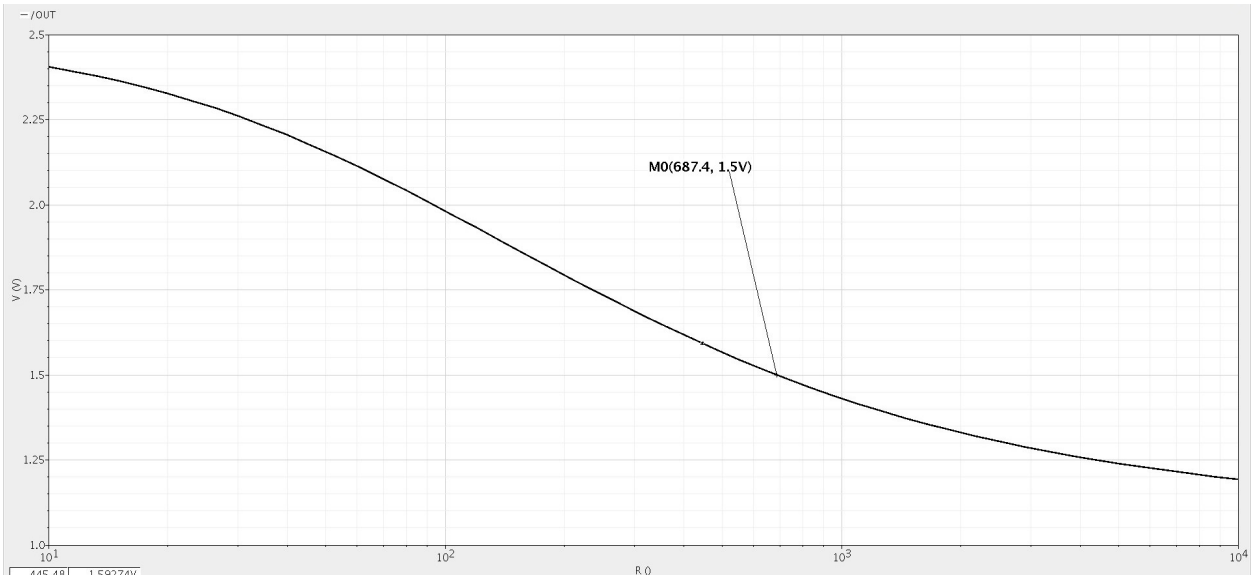
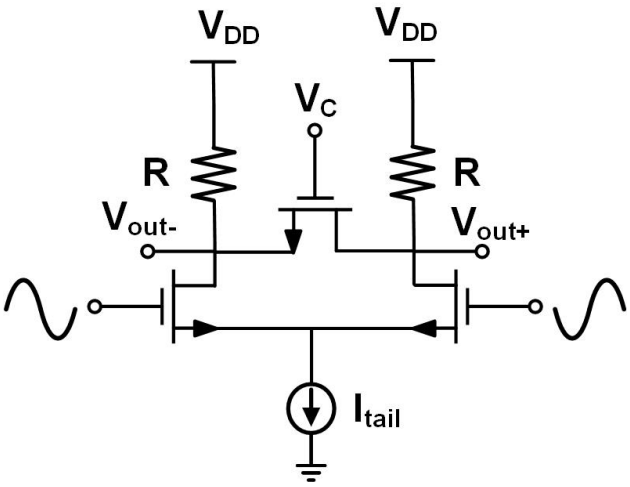


Figure 4.13: Output node's dc value vs. the resistor value at the source.

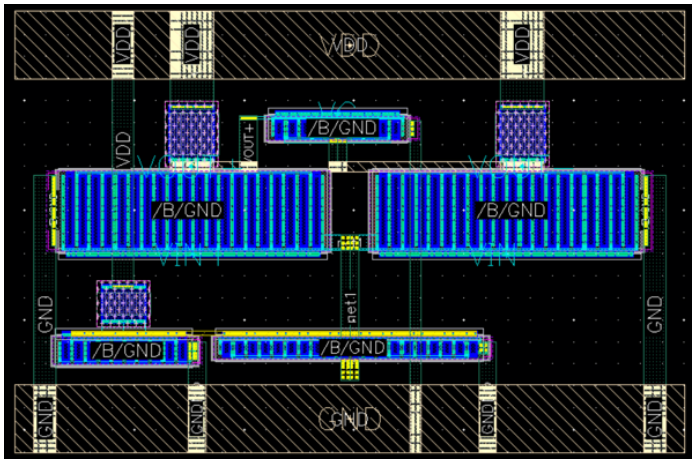
transistor between the drains of the differential pair is to provide another path for ac current and adjust the overall resistance. This VGA is required to have sufficient gain and bandwidth that is higher than the circuit's maximum operating frequency. As shown in Fig. 4.15, the bandwidth of the circuit with three different control voltages is larger than 500 MHz.

4.4 Laser driver

The last stage before the replica of the phase measurement unit on the TX side is a power stage called laser driver. In some applications, this block can be considered as a simple power switch that responds to an input signal modulated by a data stream. However in our case, rather than a bi-level signal, a sinusoidal waveform is applied into this block. Differential drivers have many important advantages over single-ended circuits [24]. They maintain a relatively constant supply current despite large current variations, resulting in low switching noise across the package inductor. Even if the output voltage fluctuates widely, crosstalk between V_{DD} metal lines will be low if the signal symmetry is maintained. Moreover, the presence of package parasitics make them less susceptible to oscillations due to their lower



(a)



(b)

Figure 4.14: (a) Schematic of the VGA; (b) layout of the VGA.

common mode gain.

This stage controls a laser diode. There is a special type of laser diode called a vertical cavity surface emitting laser (VCSEL). In a VCSEL, the axis of the optical cavity runs along the direction of current flow, rather than perpendicular to it as in traditional laser diodes. The radiation comes from the surface of the cavity, not from its edges. The reflector at the end of the cavity is a dielectric mirror, known as distributed Bragg reflector. Such dielectric mirrors provide highly wavelength-selective reflectivity at the required free-space wavelength λ [25, 26].

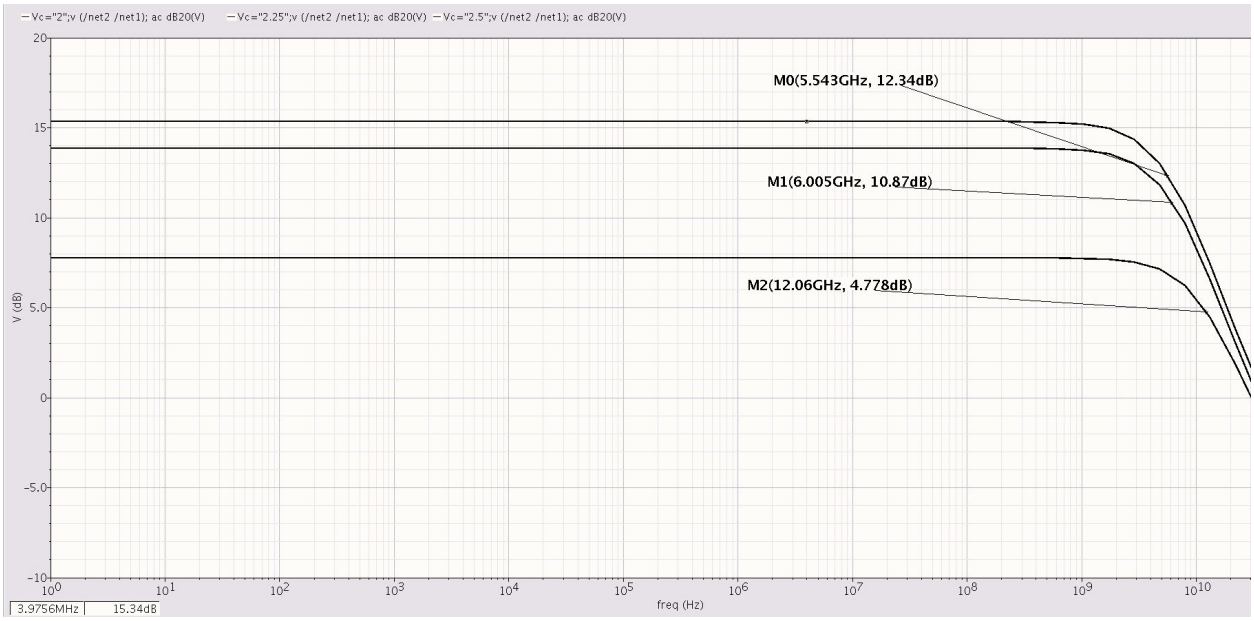
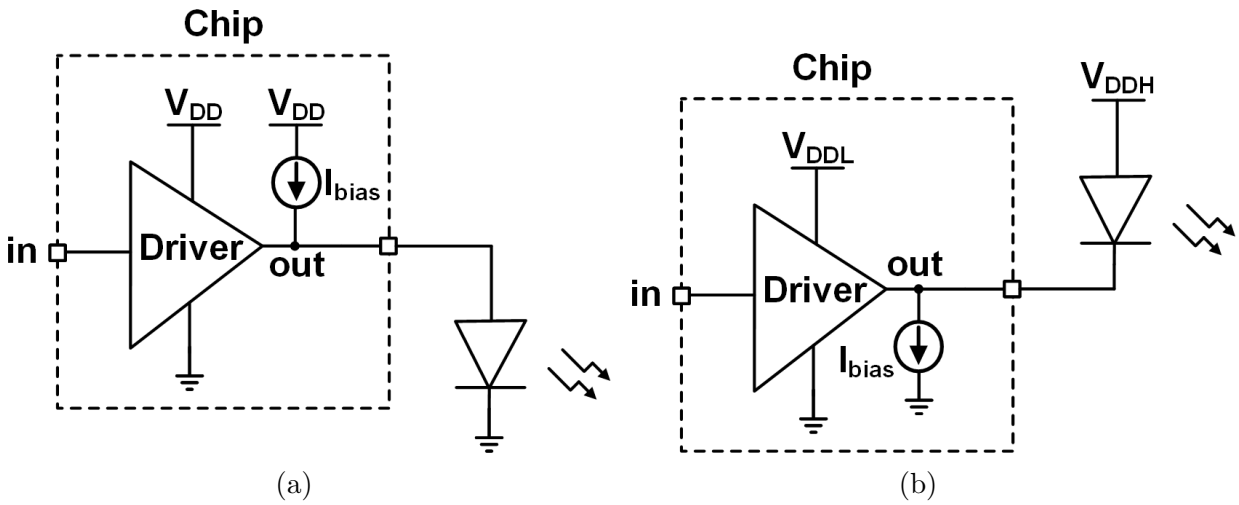


Figure 4.15: Ac response of the VGA for $V_C = 2.5V$, $V_C = 2.25V$, and $V_C = 2V$.

There are two types of VCSELs: common cathode and common anode. Fig 4.16 shows traditional drivers for two different types of VCSELs [27]. Because the turn-on voltage of a VCSEL is high (above 1.5 V), the supply voltage (V_{DD}) of a common cathode VCSEL driver must be set high enough to ensure robust operation of the VCSEL, and the design of the VCSEL driver can be difficult. However, for VCSELs with a common anode, the chip supply voltage (V_{DDL}) can be lowered by externally biasing the VCSEL anode to a higher voltage. This configuration reduces power consumption and allows the VCSEL to be driven more efficiently. However, using common anode VCSELs requires the use of additional supply voltages. Therefore, common-cathode VCSEL drivers are preferred in many applications.

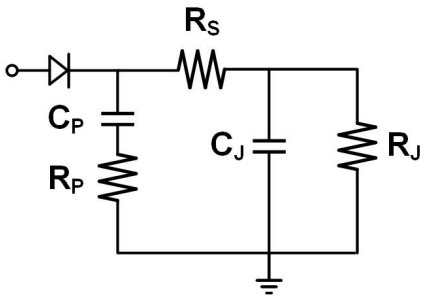
Circuit simulation requires a VCSEL electrical model. This model was extracted from [28] and is shown in Fig. 4.17. Since that electrical model is sufficient only for modeling small-signal behavior, a diode with certain relationship between current and voltage is modeled in Verilog-A and added to this R-C parasitic model of the VCSEL.

The most difficult part of the design is that the circuit must handle large dc and ac currents. Five types of lasers are available in the laboratory. Their specifications are shown in Table



(a) (b)

Figure 4.16: (a) Common-cathode driving topology; (b) common-anode driving topology.



Parameter	Value
Junction Capacitance (C_j)	110-117fF
Junction Resistance (R_j)	180-150Ω
DBR Resistance (R_s)	50Ω
Pad Capacitance (C_p)	10fF
Pad Resistance (R_p)	1Ω

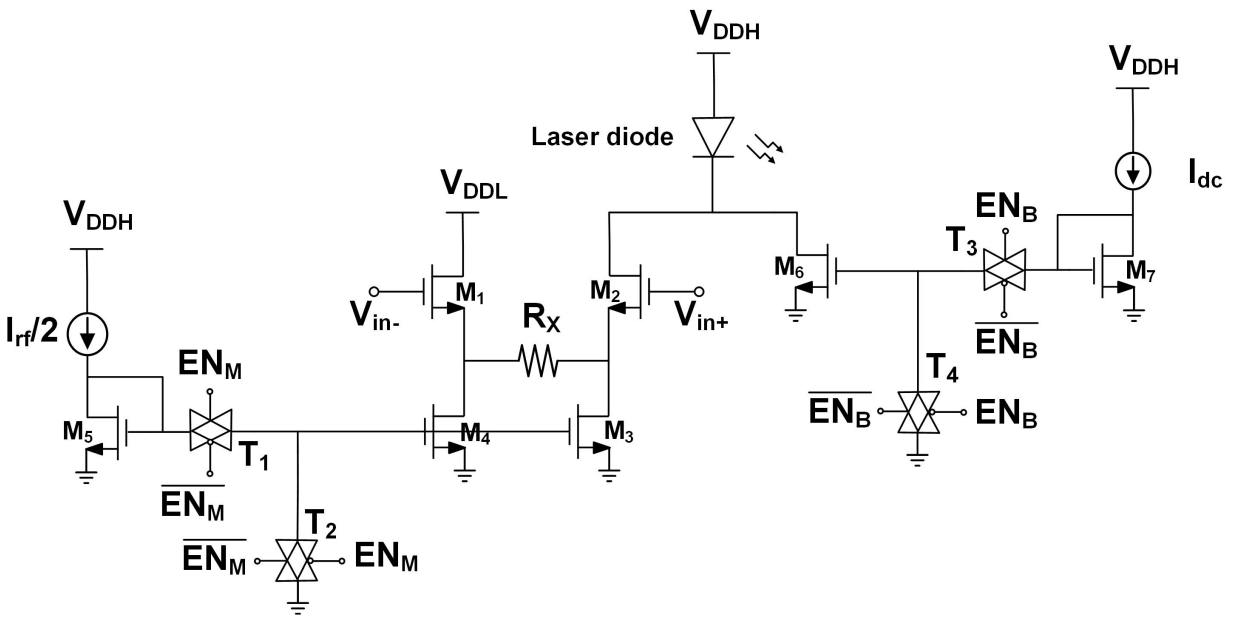
Figure 4.17: VCSEL electrical model.

4.2. After connecting each of these laser diodes to the chip, the laser driver must function properly. Therefore, the design requires adjustable current sources.

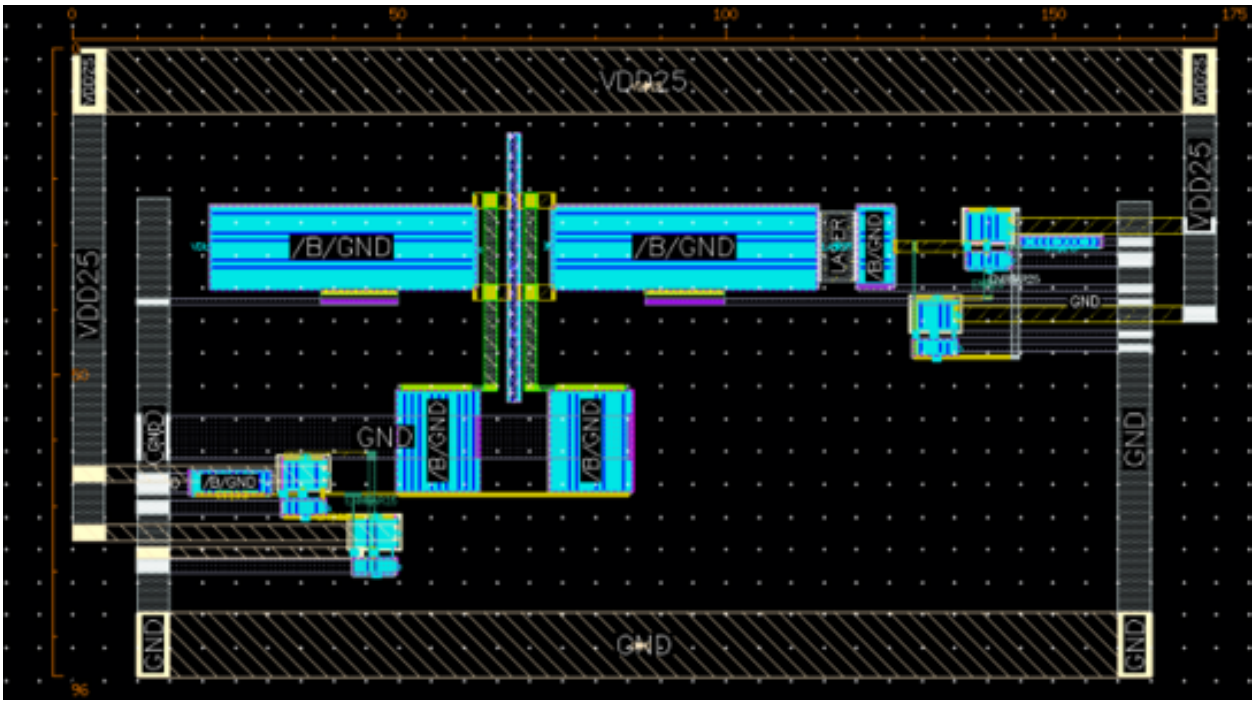
Serial Number	Wavelength	Max DC Current	Max AC Current
1	660 nm	79.27 mA	22.858 mA
2	689 nm	51.04 mA	28.545 mA
3	782 nm	69.19 mA	17.723 mA
4	828 nm	54.59 mA	18.24 mA
5	849 nm	61.81 mA	40.976 mA

Table 4.2: Laser diode's specifications

The schematic and layout of the differential laser driver are shown in Fig. 4.18. This circuit has several important nodes that require large amounts of current to flow. Therefore, these nodes with multi-layer metal lines must have sufficient thickness to ensure low parasitics



(a)



(b)

Figure 4.18: Laser driver's (a) schematic; (b) layout.

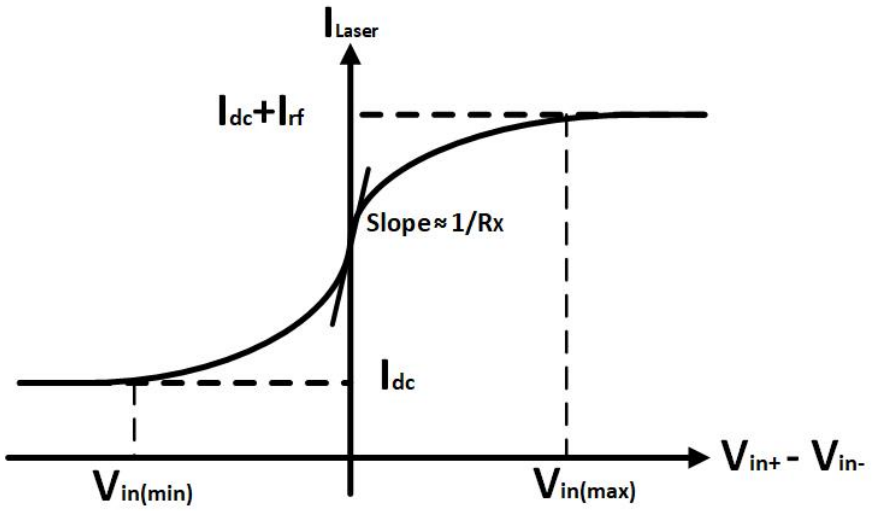


Figure 4.19: I-V Characteristics.

(low IR drop) and withstand the flow of such large currents.

Fig. 4.19 shows the output current versus input differential voltage characteristics. For abrupt switching (assuming same W/L ratios for current mirrors) we have:

$$I_{max} = I_{dc} + I_{rf} \tag{4.6}$$

$$I_{min} = I_{dc} \tag{4.7}$$

In this circuit, when transistor M_1 is off, the laser conducts its $I_{dc} + I_{rf}$. But when M_2 is off, only I_{dc} is conducted through the laser diode. In this application, there is no hard switching due to the sinusoidal input signal. In this case:

$$I_{max} = I_{dc} + (1 - \alpha)I_{rf} \tag{4.8}$$

$$I_{min} = I_{dc} + \alpha I_{rf} \tag{4.9}$$

where α is a coefficient between 0 and 0.5. For hard switching, α equals to 0.

Let's assume small-signal operation:

$$G_m = \frac{I_{laser}}{V_{in+} - V_{in-}} \approx \frac{g_{m1,2}}{1 + g_{m1,2} R_X} \rightarrow I_{laser} = (V_{in+} - V_{in-}) \times \frac{g_{m1,2}}{1 + g_{m1,2} R_X} \tag{4.10}$$

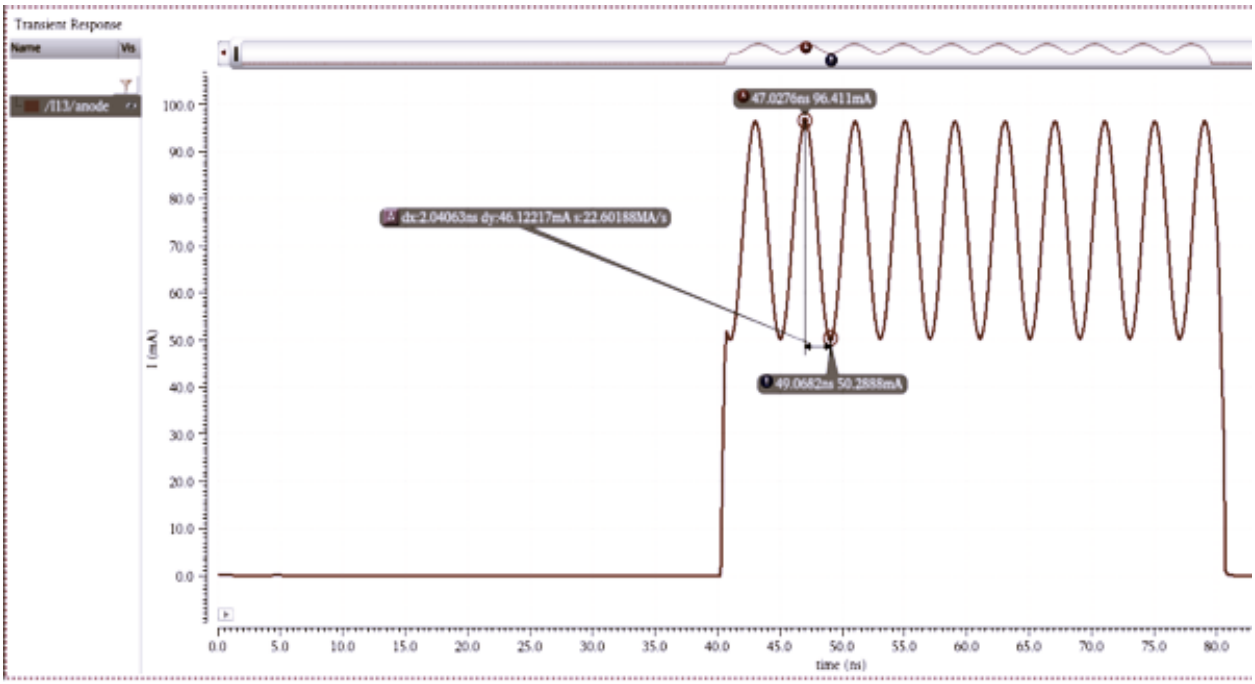
It is clear that there is a linear relationship between the input differential voltage and the output current (laser current). Choosing an appropriate value for the degeneration resistor can result in nearly linear behavior between the differential signal and the laser current.

This part of the TX consumes a large amount of power. The two switching pairs (T1-T2 and T3-T4) are configured to disable the power supply after a while to allow the chip to cool down.

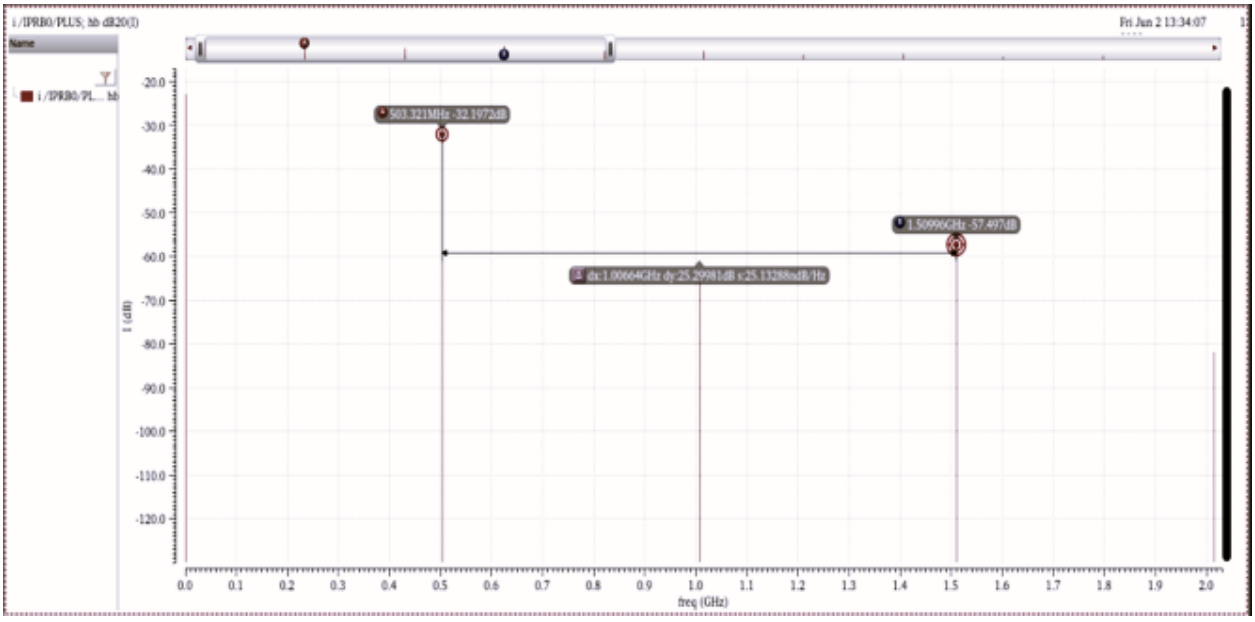
The W/L ratios of transistors in the current mirrors are all set to 5, which allows sufficient current to be generated. Currents I_{dc} and I_{rf} are supplied from outside the chip through a variable resistor connected to $V_{DDH} = 2.5V$

The post-layout simulation results for the entire TX chain of two lasers (serial numbers 1 and 3 from Table 4.2) are shown in Fig. 4.20 and Fig. 4.21. The frequency of the input signals is 250 MHz. It can be observed that, the peak-to-peak amplitudes and dc levels match the specifications. The transmission gates enable the laser driver's operation for 10 periods and then disable it for the same periods of time. The harmonic response for the switched-on transient current also shows a difference of more than 20 dB between the first and third harmonics. Therefore, a well-formed sinusoidal shape is concluded. It is also worth mentioning that due to time and hardware constraints, only the PLL's output (VCO)

is configured for the post-layout simulations.

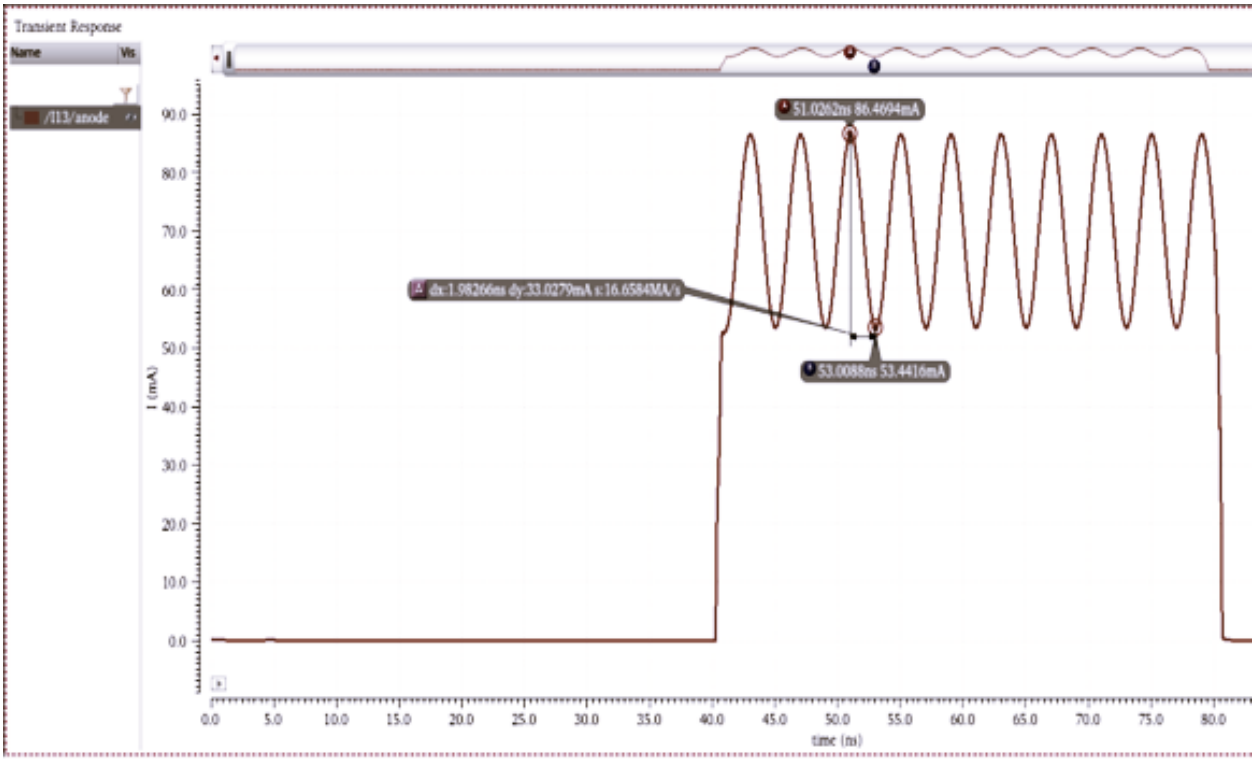


(a)

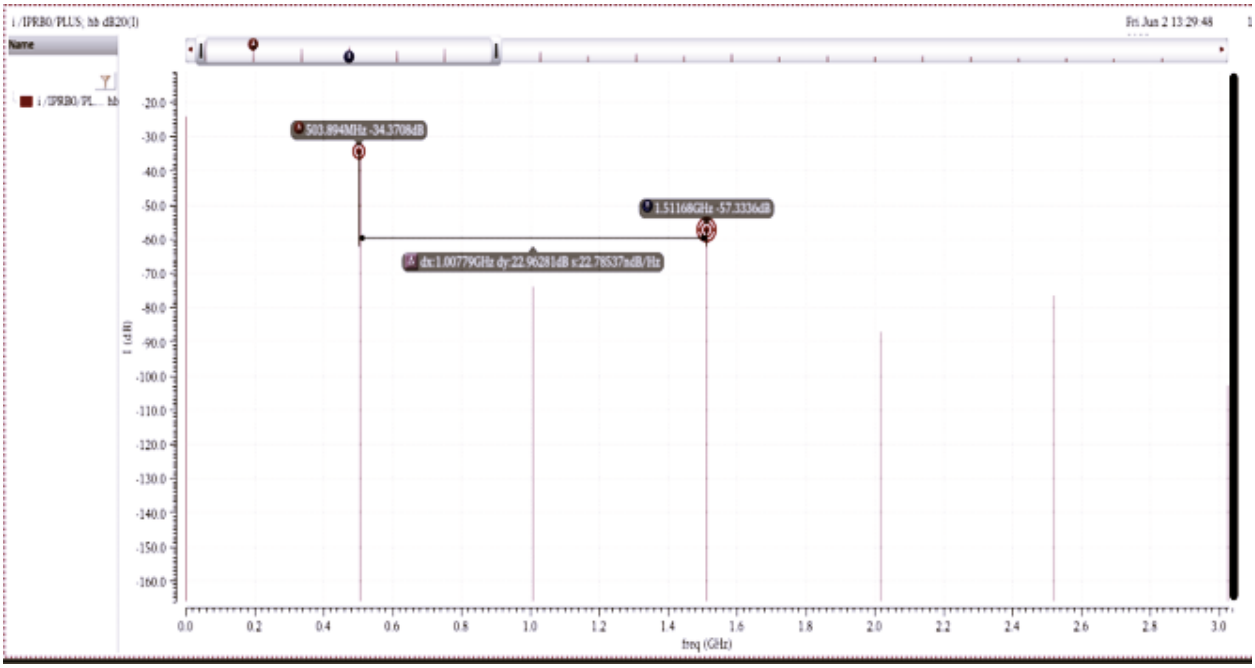


(b)

Figure 4.20: Laser number 1 current's (a) transient; (b) harmonic responses.



(a)



(b)

Figure 4.21: Laser number 3 current's (a) transient; (b) harmonic responses.

Chapter 5

Conclusion

In this thesis, several fd-NIRS systems on a chip have been discussed. The block diagram and circuit implementation of the first and second version chips were described. Transmitter chain design and post-layout simulation results of the third version system were reported. The third version has some changes compared to the previous versions. This version has a PLL instead of a free-running VCO in the first version as the reference signal. The digital blocks of the reference PLL are also fully asynchronous and consume less area compared to the second version. To reduce the number of pins, a serial-to-parallel converter was used. The laser driver is on the chip in this version, whereas it was external in the previous versions. This laser driver requires a large amount of current to flow. Thus, there are some switches that disable the circuit for a period of time to prevent the chip from overheating.. This laser driver meets the specifications of the five laser diodes expected to be used in this application. Post-layout simulations of the entire TX chain are shown. This circuit operates over a frequency range of 50 MHz to 500 MHz with a resolution of 2 MHz. This design was implemented in a 65 nm CMOS process. Our group is working on the receiver, phase, and amplitude measurement units as the future goal.

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