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BIAS STRESS EFFECTS IN ORGANIC THIN FILM TRANSISTORS

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ABSTRACT

Device instability and limited lifetime have been the hurdles to commercialization of organic electronics. Through electrical characterizations and microscopy techniques, much progress has been made in understanding gate bias stress that limits the stability of organic field-effect transistors. The kinetics and mechanisms of charge trapping in organic semiconductors are examined to explain the bias-stress behaviors. The external processing factors, such as dielectric treatments and environmental conditions that affect the severity of bias stress, are also investigated to enable controllable and reproducible device fabrication. [Keywords: Bias stress, organic semiconductors, charge trap, field-effect transistors.]

INTRODUCTION

The performance of solution-processible organic semiconductors has reached the benchmark mobility ($1 \text{ cm}^2/\text{Vs}$) of amorphous silicon and is adequate for many types of electrical circuits. Additionally, organic semiconductors can be processed cheaply over large areas at low temperature on flexible substrates. While active-matrix backplanes using organic thin film transistors (TFTs) have been demonstrated to drive flexible electronic paper displays [1, 2], the main hurdle to commercialization is their stability during operation and their shelf life. Organic TFTs have shown instability under continuous applied gate bias; gate bias stress causes changes of the output current of a TFT with operation time [3, 4] and is frequently due to a shift in threshold voltages V_T [5–9] (Fig. 1). Organic TFTs are frequently unstable in the ambient environment due to absorption of impurities such as water. Therefore, it is important to choose organic semiconductors that are inherently stable under operating conditions within practical limits of air, moisture, and light exposure; in addition, good understanding and control of the fabrication processes are also required to ensure reproducible manufacturing.

Because most solution-processible organic semiconductors form films that are disordered or poly-crystalline, the chemical structures of the carrier traps that cause device instability are difficult to identify and are still under debate [10]. We focus here on the mechanisms of bias stress in polymeric TFTs and its impact on circuits for active-matrix display backplanes. The mechanisms discussed are also important for understanding operation in rf-id circuits, but a detailed discussion is outside of the scope of this work. In this proceeding, we will first discuss the characteristics of bias stress in organic semiconductors, such as the distribution of trap states [11–13] and the mechanisms of charge trapping [4, 14, 15]. Then we will examine the external processing factors, such as dielectric treatments [16–21] and environmental conditions [5, 22–27], that affect the severity of bias stress.

CHARACTERISTICS OF BIAS STRESS

Gate bias stress is generally caused by mobile carriers being trapped at the dielectric/semiconductor interface or possibly inside the dielectric. The trapped carriers reduce the output current of a TFT as the total number of carriers stays constant at a given gate voltage.

Fig. 1. Gate bias stress in an annealed PQT-12 TFT, indicated by (a) decreasing current vs time and (b) threshold-voltage shift after consecutive current-voltage measurements (first measurement: Open circle; second measurement: filled circles). The TFTs discussed here are in the bottom gate coplanar configuration on substrates with 100 nm layer of thermally grown silicon oxide.

Thus, the main effect is a shift in the threshold voltage of the device without a change in carrier mobility. It is also possible that defects are created during operation, but we have observed that these effects are minimal under short term operation. Typically if a stressed polymeric TFT is illuminated by light with energy above the bandgap [28, 29] of the semiconductor, photogenerated electron-hole pairs recombine with the trapped charges to release mobile carriers and recover the shift in threshold voltage. The following bias stress measurements are done in the dark to exclude the light effect, and we have examined two polymeric semiconductors, regioregular poly(quarterthiophene) (PQT-12) and poly(9-9'-dioctyl-fluorene-cobithiophene) (F8T2).

In most semiconducting polymers, we expect that the trap states have a distribution of energies due to disorder in the semicrystalline film. For example, in PQT-12 different trapping regimes are observed due to broadly two types of trap states characterized by their time constants. As seen in Fig. 1(a), once a gate bias is applied, the current shows a fast initial decrease and then a slow drop at extended time without establishing a steady state. Similarly, after the gate bias is turned off, the current recovers rapidly in the first few seconds but slows down subsequently. Thus the mobile carriers are

trapped either in “fast” reversible or “slow” long-lived trap states. The concentration of mobile carriers [3] N can be inferred from the linear current I_{sd} by using the gradual channel approximation $I_{sd}/V_{sd}=W/L\mu Nd$, where W/L is the ratio of channel width to channel length, μ is the mobility measured from the transfer and output characteristics of the TFTs, and d is the effective width of the accumulation layer, assumed as 1 nm [30] here. The above approximation assumes that the source-drain bias V_{sd} is small relative to the effective gate voltage V_g-V_T . At time $t=0$, the inferred N agrees with the total charge concentration $C_g(V_g-V_T^0)$, where $C_g=30\text{nF/cm}^2$ here. The density of trapped charges at a given time is obtained from $N(0)-N(t)$. We have found that in polymeric TFTs the bias stress depends on the magnitude of the applied gate voltage and therefore the carrier concentration in the channel (Fig. 2(a)).

Since charge trapping is a competing process between the capture and the release of mobile charges, bias stress is dependent on the gate-on and gate-off time. Both “fast” and “slow” traps are filled during the gate-on state. In the gate-off state, the charge trapped in “fast” reversible traps is quickly de-trapped, leading to partial recovery of the current or threshold-voltage shift. Assuming ideal transfer characteristics in the linear regime of operation, the current is related to the threshold-voltage shift [11] by $\Delta V_T(t)=[1 \cdot I(t)/I_0](V_g \cdot V_T^0)$, where I_0 and V_T^0 are the current and threshold voltage at $t=0$, respectively. The lifetime of a TFT in a backplane circuit is limited by the current drop of the TFT and can be estimated based on the maximum tolerable threshold voltage shift [11]. During operation of a display, the pixel transistors are kept in their on-state for a time at most equal to the frame time divided by the number of lines in the display, but typically for substantially less time [31]. The TFTs are held in the off-state in depletion for

significantly longer times than the on-state. Thus, reversible traps play a minor role in the long term behavior and the shift in threshold voltage is dominated by “slow” trapping in irreversible traps. As the long-lived traps are increasingly occupied at high carrier densities, applications that require particularly high gate voltage will have much shorter lifetime.

KINETICS AND MECHANISMS OF CHARGE TRAPPING AND RELEASE

The kinetics of trap formation is studied by observing the change in mobile-carrier concentration. In general, we obtain the time decay of mobile carriers dN/dt by linear fits to the mobile carrier concentration derived from the current through the TFT after the gate voltage is turned on (Fig. 2(a)). The linear fit is done on data from 5 to 15 ms, and the values of N at 10 ms are used below. The use of this timescale minimizes variations due to capacitive charging, and we assume that trap release is negligible. The values of N at 10 ms are used below. The rate constant of trap formation is inferred from a linear fit to dN/dt against N (first-order reaction) or N^2 (second-order reaction), as shown in Fig. 2(b) and 2(c). The rate constants of trap formation are summarized in Table I. It has been suggested that, during bias stress, hole pairs bind together to become bipolarons (second order) in F8T2 and PQT-12 [3, 4]. However, charge modulation spectroscopy [14, 15] on F8T2-based TFTs suggests that the carriers are isolated polarons instead (first order), even in the strong accumulation regime. For our F8T2 and PQT-12 TFTs studied in vacuum, it is not possible to distinguish whether the bipolaron or the polaron model is dominant, because the residuals (not shown) are similar in the fits to N or N^2 . Although the reaction mechanism is not conclusively determined, the rate constants of trap formation are still useful for comparing the bias stress due to different materials and process parameters. For instance, the trapping rate constants of F8T2 TFTs are consistently larger than those of PQT-12, indicating that F8T2 is more susceptible to bias stress.

The kinetics of trap release has also been observed by electric force microscopy (EFM) [13, 28, 32–36]. EFM is a non-contact scanning probe technique that allows for imaging charge density variations in a thin film by measuring the local electrostatic potential between the tip of the cantilever and the sample. Images in Fig. 3, taken at the same area, illustrate the release of long-lived trapped charges with time. Compared to the initial image taken before stress bias is induced, the channel region in the stressed device ($V_g = -10$ V) exhibits a large frequency shift due to trapped charges. As time passes, the charges are released and the image gradually reverts back to its initial state. The trap distribution in F8T2 is relatively

Fig. 2. (a) Free carrier concentration N as a function of time and gate voltages $V_G=-20$ to -65 V in steps of 5 V. The carrier concentration decays faster with more negative gate voltage. Fits of dN/dt are shown in white. This plot is taken with an annealed F8T2/OTS device. Time decay of mobile carriers as a function of (b) N or (c) N^2 for annealed F8T2 devices. Untreated oxide interface: open triangles, linear fit shown by dashed line. OTS-treated interface: solid circles, linear fit shown by solid line. Data taken from Ref [20].

Fig. 3. Electric force microscopy images ($10 \times 10 \mu\text{m}^2$) of an annealed F8T2/OTS device, with cantilever bias $V_{tip}=1$ V. The images are taken at the same location, with the channel region in the middle and electrodes on both sides. (a) Before stress. (b) and (c) Time evolution of cantilever frequency shift $(f-f_0)/f_0$ after bias stress of $V_G=-10$ V. The line profiles are taken at the location indicated by the white lines. Data taken from Ref [20].

homogeneous, in contrast to the inhomogeneous trap distribution seen in pentacene thin-film transistors. The differences in trap distribution between our images and those of [33–36] are mainly due to the semiconductor (polymeric versus polycrystalline) film morphology.

The local electrostatic potential ϕ is inferred from the frequency shift of the cantilever by $f - f_0 = -(f_0/4k_0)(\partial^2 C/\partial z^2)(V_{\text{tip}} - \phi)^2$, where f_0 is the intrinsic cantilever resonance frequency (typically 25 ± 5 kHz), $k_0 = 1 \pm 0.5$ N/m is the intrinsic cantilever spring constant, C is the tip-sample capacitance, z is the tip-sample separation, V_{tip} is the applied tip voltage. At a given location inside the channel, the measured potential decreases with time and is fitted to a simple exponential $\phi(t) = \phi_{\Delta} \exp(-t/t_r)$, where ϕ_{Δ} is the potential change after the gate bias is removed, and t_r is the exponential decay time. Similar to other amorphous systems [37, 38], the potential decay actually follows a stretched exponential behavior, and therefore the exponential decay rates found in Table I are only approximations. Nevertheless, they are still valid metrics for relative comparisons.

FABRICATION PROCESSES THAT AFFECT CHARGE TRAPPING

From the kinetic studies of trap formation and dissociation, both trap capture and release (see Table I) are slower in devices with untreated dielectric interfaces than in devices whose dielectric surface has been modified with hydrophobic alkyl chains [16–18, 21], such as a cross-linked monolayer of octadecyl-trichlorosilane (OTS). This difference implies that the trap states in untreated interfaces have higher barriers than in modified interfaces. In untreated interfaces, a high barrier requires more time for a charge to fall into the trap state from a mobile state, but once a charge is in the trap state, it also takes longer for it to be released due to the same high barrier. Compared to a modified interface, the untreated interface eventually develops larger bias stress at the long time scales (Fig. 4), due to the high barrier to trap release. Thus, hydrophobic surface treatment improves the device bias stress by minimizing the time charge carriers spend in traps. While most structural analyses suggest that hydrophobic surfaces lead to lamellar stacking perpendicular to the surface and that hydrophilic ones lead to a mixture of orientations in polymers such as regioregular poly-(3-hexylthiophene) (P3HT) [39], the preference is not absolute [21], as x-ray scattering patterns of films of poly(2,5-bis(3-alkylthiophen-2-yl)thieno[3,2-*b*]thiophene) (PBTTT) spun on bare SiO_2 are similar to those observed for films on OTS/ SiO_2 [40]. The microstructure in a

film is strongly affected by processing conditions as well as interfacial interactions. The casting solvent, drying conditions, and thermal annealing steps can all have an impact on the final structure [41, 42].

Thermal annealing has increased rate constants for trap formation (Table I) on both OTS-treated and untreated interfaces. According to the percolation model in [43], charge carriers are transported through a mixture of ordered and disordered regions in polymers. Surface modification and annealing could align molecules in the disordered regions, so that the barriers of trap states are lowered and the trap states are more frequently occupied (but also quickly released) than before the treatments. Similar to [29], the device mobility is observed to remain the same after bias stress, further showing that charge trapping does not necessarily affect the mobility of the TFTs. This demonstrates that mobility and bias stress are two different device parameters.

Table I. Best-fit values for the rate of trap formation and trap release. In part (a), k_p corresponds to first-order reaction and k_{bp} to second-order reaction. The mobility μ is measured from transfer-output characteristics (error=20%). Part (b) gives the exponential decay times for different dielectric interfaces.

(a)	k_p (s^{-1})	k_{bp} ($10^{-19} \text{ cm}^3/\text{s}$)	μ (cm^2/Vs)
F8T2-oxide, annealed	6.4 ± 0.2	2.04 ± 0.17	1×10^{-5}
F8T2-OTS, annealed	17.8 ± 0.8	8.79 ± 0.42	0.006
PQT-oxide, as spun	5.1 ± 0.2	0.56 ± 0.03	0.010
PQT-oxide, annealed	6.4 ± 0.4	1.29 ± 0.07	0.006
PQT-OTS, as spun	8.5 ± 0.4	1.41 ± 0.07	0.008
PQT-OTS, annealed	10.9 ± 0.9	2.77 ± 0.14	0.055
(b)	ϕ_{Δ} (V)	t_r (min)	
F8T2-oxide, annealed	0.39 ± 0.05	63 ± 23	
F8T2-OTS, annealed	1.36 ± 0.09	33 ± 6	

ENVIRONMENTAL EFFECTS ON BIAS STRESS

It is highly desirable to process organic semiconductors in the ambient environment, but exposure to an uncontrolled atmosphere has detrimental impact on the electrical characteristics of TFTs [22–27]. The highest device performance in polymeric TFTs is usually achieved after a thermal annealing step in a controlled environment such as dry nitrogen. If the device is subsequently exposed to the ambient, the device characteristics will frequently degrade. Although in finished electronic devices the TFTs will be encapsulated, it is important to understand the effects of absorbed impurities and how to control them. Two of the most common ambient species that are considered important are water and oxygen.

The effects of water on organic TFTs have been examined by a number of groups and it is generally found to lower the mobility of TFTs. We performed a detailed study of the effects of adsorption of water molecules in PQT-12 and found that it affects both the field effect mobility and the rate of charge trapping [23]. Gate bias stress has been shown to increase during operation under humid

Fig. 4. Relative current vs time for PQT-12 TFTs with unmodified (solid line) and OTS-treated (crosses) dielectrics at $V_G - V_T = -10\text{V}$ and $V_{SD} = -3\text{V}$.

Fig. 5. Mobility (left axis) and rate constant for bipolaron formation (right axis) of an annealed PQT-12/OTS TFT as a function of relative humidity in nitrogen.

environments [5, 23–25]. In contrast to the kinetic studies done in vacuum, the bipolaron mechanism dominates when moisture is present. The observed increase in rate constant for the formation of bipolarons (Fig. 5) suggests that water molecules reduce the coulomb barrier in the approach of two positively charged species. It is difficult to determine if the absorption of water causes structural changes in the semiconducting material or simply, causes dipolar disorder [18]; in either case, the presence of water can substantially change the electrical characteristics.

The TFTs in backplane circuits must have very low leakage current (typically $< \sim 1$ pA) to store charge at the pixel during the refresh cycle [44]. Exposure to ambient atmosphere that has been stripped of moisture still leads to increasing off-current and sub-threshold slope of polythiophene-based TFTs. This degradation has generally been attributed to doping of the semiconductor by molecular oxygen, O_2 [26, 27], but we have [45] shown that, in the absence of light, it has little effect on the electrical characteristics of several polythiophenes. We believe that ozone, O_3 , is a more likely cause of the rapid doping observed in the ambient, (Fig. 6), which is partially reversible upon thermal annealing. While indoor ozone concentrations are relatively low (typically 1–10 ppb), calculations suggest that it is energetically favorable for an intact O_3 molecule to bind to the polymer backbone, such that the structure is stable with respect to a free O_3 molecule by -1.07 eV. This structure puts an acceptor state 0.3 ± 0.1 eV above the valence band maximum. With a relatively strong interaction between ozone and the semiconducting polymer, the films will continually absorb ozone from the environment until saturated, thus causing the slow (> 30 minutes) observed changes in the TFTs studied in the ambient. There have been several reports of the stabilization of TFTs using thin organic encapsulation layers [46] or for devices in a top-gate geometry [47]; these barrier layers are unlikely to prevent oxygen from reaching the semiconducting layer, but would prevent ozone exposure as it would likely react with the barrier before reaching the semiconductor.

CONCLUSION

In the attempt to maintain stability and extend device lifetime, the insights above have been accumulated to facilitate control over the critical materials and fabrication parameters that affect bias stress. Finally, smart pixel design is incorporated to mitigate bias stress by increasing the transistor geometric ratio W/L to keep the carrier concentration low while simultaneously maintain enough current ($\sim 1 \mu A$) to drive the pixel. This approach was taken by Phillips

Fig. 6. Current-voltage characteristics of annealed PQT-12/OTS TFTs measured in the linear regime with $V_{SD} = -5$ V under (a) an ambient of purified, dry air. The initial characteristics are given by the solid line and those after 5 and 10 days respectively are given by the squares. (b) Another device was measured after fabrication (black line), after brief exposure to ~ 1 –10 ppm ozone in dry air (grey line), and after annealing at $100^\circ C$ in nitrogen (black squares). Data taken from Ref [45].

Research in their polymer TFT circuits [1, 2]. With the current understanding and availability of stable materials and fabrication processes, commercial organic electronics should be realized in the near future.

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