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Process Development, Optimization, and Characterization of Sn Electroplating for Advanced Packaging Interconnection

A thesis submitted in partial satisfaction of the requirements for the degree Master of Science in Materials Science and Engineering

by

Shaurya Seth

2023

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ABSTRACT OF THE THESIS

Process Development, Optimization, and Characterization of Sn Electroplating for Advanced Packaging Interconnection

by

Shaurya Seth

Master of Science in Materials Science and Engineering

University of California, Los Angeles, 2023

Professor Subramanian Srikanteswara Iyer, Chair

Sn is an important material in the microelectronics industry. Electroplating of Sn for depositing pure Sn at low temperatures was done using acidic bath. This setup can have one application for the integration of chiplets onto a substrate. The Sn required is 99.999999% pure with primary impurity being Pb, and is chosen as the befitting material because of its excellent solderability as microbumps for fine pitch interconnection.

Since, the Sn needed for bonding should be dense, uniform, 2-4 μm in thickness and smooth, the acidic baths have been more developed and studied than alkaline baths [1] for microelectronic applications. Furthermore, recently, methanesulfonic acid based systems have grown and taken a good standing because of their eco-friendly nature [2] and good adhesion and uniform coatings.

The JM6000 LS bath was developed for low temperature Sn coating to have higher grain sizes for a better electrical conductivity even though the bath has grain refiners, the grain size distribution reached about the desired thickness. The aim of the research was to optimize the electroplating process parameters and investigate the effect of various parameters on the quality of the electroplated tin layer. The study provides valuable insights into the effect of process parameters such as temperature, current density, and plating time on the quality and properties of the electroplated Sn layer. The results suggest that the Sn electroplating process can be optimized to obtain a uniform, adherent, and defect-free Sn layer with desired properties.

The thesis of Shaurya Seth is approved.

Aaswath Pattabhi Raman

Jaime Marian

Subramanian Srikanteswara Iyer, Committee Chair

University of California, Los Angeles

2023

Dedicated to my parents

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Chapter 1

Introduction

1.1 Sn electroplating: bath types, preferred bath

Electroplating of tin is widely utilized in the microelectronics packaging and we attempted to coat the tin in-house because of its cost-effectiveness and excellent solderability required for tighter bonding pitches between the die and substrate [3]. Sn has a widespread use in the industry for bonding because of the solderability property mentioned above.

Sn setup requires different components for electroplating. The process involves having an electrolyte bath for ion transport, a Sn anode for the oxidation of Sn metal to Sn^{+2} ions and a cathode as a target material for Sn deposition [4]. Both the electrodes are immersed in the electrolyte to form a closed circuit. A direct current

is provided to the electrodes. Anode gives off the electrons and the water soluble

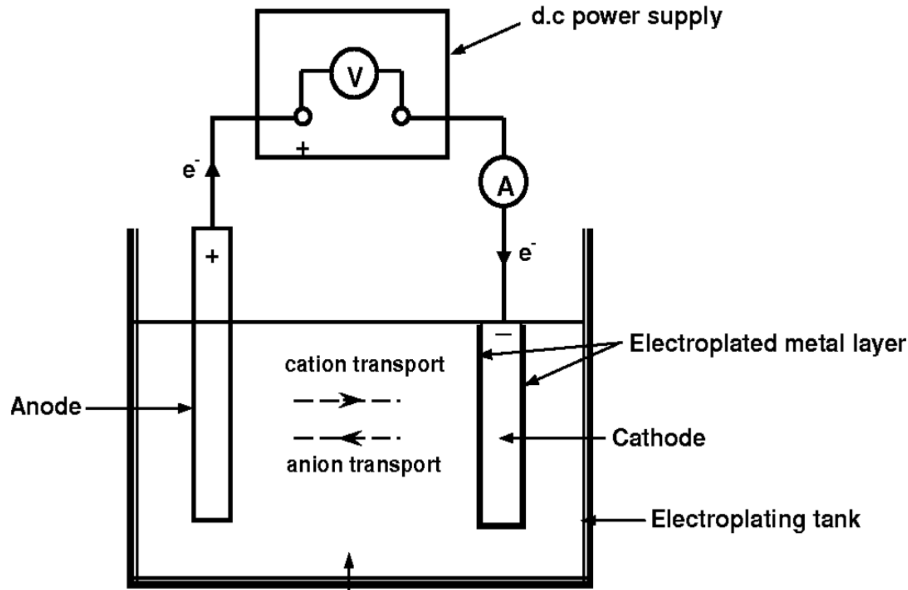
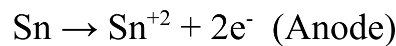
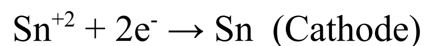


Fig. 1.1 Electroplating schematic [4]

Sn^{+2} ions dissolve in the electrolyte to maintain charge neutrality. The electrons are then consumed at the cathode, which is a 4" silicon wafer seeded with Ti/Cu, to reduce the Sn^{+2} ions from the bath to the Sn metal.



$$Sn \rightarrow Sn^{+2} + 2e^{-} \quad \text{(Anode)}$$



$$Sn^{+2} + 2e^{-} \rightarrow Sn \quad \text{(Cathode)}$$

Tin can be electroplated in acidic as well as alkaline baths [5]. The bath used for performing the experiments in this thesis is acidic in nature with methanesulfonic acid (MSA), as the electrolyte. Sn^{+2} ions are used for electrodeposition in the acidic

bath [6]. The acidic baths are complicated to maintain, and therefore require additives to stabilize the electrolyte [6]. Although, the Sn can get electroplated in acidic baths without the use of additives as well, because of lower activation potential, but it is not recommended as it produces coarse grained coatings which have a bad adhesion to the substrate and do not provide uniformity at all [7]. The acidic baths in presence of additives not only provide adhesion and uniformity, but also faster deposition rates in comparison to the alkaline baths. Additionally, applications in general for microelectronic packaging and for our application, there is limited use of alkaline baths as they have a higher pH (~14) requirement, which is detrimental to the photoresist. Moreover, alkaline baths use up a lot of power because of the presence of tetravalent Sn against what the acidic baths have to offer [8]. The MSA based bath system is preferred, because of its relatively eco-friendly nature [2] in comparison to other previously used systems. Furthermore, it is less harmful to the equipment used for the plating experiments because of its less oxidizing nature, therefore the conversion of Sn^{+2} to Sn^{+4} is inhibited to a great extent, which allows for the usage of insoluble anodes [6]. The MSA bath only has 3 types of ions present, the hydrogen ions, the Sn^{+2} ions and the methanesulfonic acid ions which carry current [6]. The current to the cathode is delivered by the hydrogen and Sn^{+2} ions. Subsequently, the current to anode is carried by the methanesulfonic acid ions. For application purposes the important concerns are

plating rate, coating uniformity, coating adhesion, coating thickness and lastly, surface roughness. Sn coating is being preferred for the bonding because of excellent solderability in the sub 5 micron region. Since, we need greater control over the tin plating process to achieve the coating characteristics as described above, the rack plating process is preferred [4]. The rack plating process involves hanging the cathode on a rack and immersing it in the plating solution.

1.2 Film nucleation and growth in presence of no additive and HQ

The mechanism of Sn nucleation and growth also varies in presence of no additives and different additives in the bath. In case, when there are no additives present, the grains in the electroplated Sn coating appear to be highly irregular and have a rough surface morphology [7]. The grain size distribution is uneven. The uneven texture is resultant from the fact that the smaller grains may or may not attract the charged Sn^{+2} ions while the other sites have a higher nucleation rate. The edges tend to be dendritic in nature due to concentration of electric field. This changes in presence of additives. The use of hydroquinone (HQ) as an antioxidant is extensive. Furthermore, hydroquinone is used to relatively smoothen the coating and narrow down the grain size distribution. The texture becomes more uniform and a better packing of grains is achieved [7]. HQ helps with the reduction of hydrogen evolution [7] as well, which leads to passivation of films and eventually

results in no plating at higher current densities. HQ can modify the electric field and ionic concentrations in the vicinity of cathode so as to provide more rounding of the grains and a better coalescence [7].

1.3 Objective of the research:

The purpose of this work is to electroplate Sn on Cu seeded or electroplated Si wafer samples and optimize the coating finish. The main contributions of this thesis are:

1. Setting up the lab owned Sn plating bath system in the wet room of UCLA CHIPS Lab.
2. Develop and optimize a process for 2-4 μm thick Sn plating over 500 μm thick Si wafers coated with 300 nm Cu seed layer or 1 μm electroplated Cu.
3. Performing surface profilometry (Dektak) technique for measurement of the thickness of the coating.
4. Performing X-ray Diffraction Analysis, for grain size measurement and determination of crystal lattice structure.
5. Performing 1 μm AFM scans on different spots on the wafer for short-wavelength surface roughness measurement.
6. Performing SEM for surface morphology characterization including grain geometry and size on samples plated at different temperatures.

7. Performing Adhesion test using the CGOLDENWALL Cross Hatch Adhesion Tester blade.
8. Develop the Standard of Procedure for using the Sn electroplating system.
9. Check whether the electroplated Sn can be used for attaching Cu pads through thermal reflow of Sn pillars ~2µm thickness

1.4 Organization of thesis:

The organization of the thesis is as follows. Chapter 2 will talk about the set up, operation and the maintenance of the Sn electroplating bath and system. Chapter 3 will talk about the process development for electroplating, characterization and metrology. Chapter 4 will present all the collected data, mainly plating rate, uniformity, adhesion, appearance, grain size, crystal structure. The discussion will include grain size variation with temperature, current density, surface roughness and coating thickness, surface roughness variation with thickness and appearance with grain size and roughness pertinent to the results and the conclusions will be elicited based on those in Chapter 5.

Chapter 2

The Makeup & Operation of Lab-Owned Sn Electroplating Bath

2.1 Overview & setting up of the Sn electroplating bath

To setup this electroplating bath, the following components were required:

1. Anode: 99.9% pure tin
2. Cathode: 4” Si wafer, with a Cu seed layer or electroplated Cu
3. Electrolyte: JM 6000 LS (a methanesulfonic system)
4. Hot plate
5. Thermometer
6. Power supply machine
7. Polypropylene tank
8. Deionised (DI) water filter
9. Cathode holder (wafer holder)

Except the DI filter, everything else until part (7) is located inside the fume hood to avoid chemical contamination of the bath by protecting the bath for instance, from water vapors. The DI filter is located beside the sink for water source.

Fig. 2.1 DI water setup

The lab owned equipment by Technic Inc. consists of a 6” x 10” x 9” (width by length by height) polypropylene (chemically inert to the Sn plating bath) tank for holding the electrolyte, cathode placed on the wafer holder and the anode. The anode is 17” x 4” x 1” (length by width by thickness) in dimensions and 99.9% pure tin metal as-casted from HallMark Metals**.** The cathode holder is obtained for a 6” wafer based on the availability at the Technic Inc. Anaheim office. The cathode is a 4” silicon wafer which is seeded with Ti/Cu layer of about 300 nm thickness. The bath is heated with the help of a 110V 800W LED Microcomputer

Electric Hot Plate used as a soldering station which can range from 0-300°C. It has temperature read-out which is digital and makes it easier to vary and gain control. The temperature for operation of the electroplating is kept between 44-48°C, and the current density is varied from 1.5-3.5 ASD (Amps per decimeter square) for coating comparison studies at different plating times ranging from 15-60 min. The hot plate and the power source is plugged to the power outlet located right outside the fume hood. The tank is placed over the hot plate for heating up the bath. The temperature of the bath is measured using a digital laboratory thermometer with 8” long steel probe and temperature measuring range between -50°C to 150°C. The thermometer is mounted using a steel clamp in the bath throughout the entirety of plating to check for stability in temperature during the process.

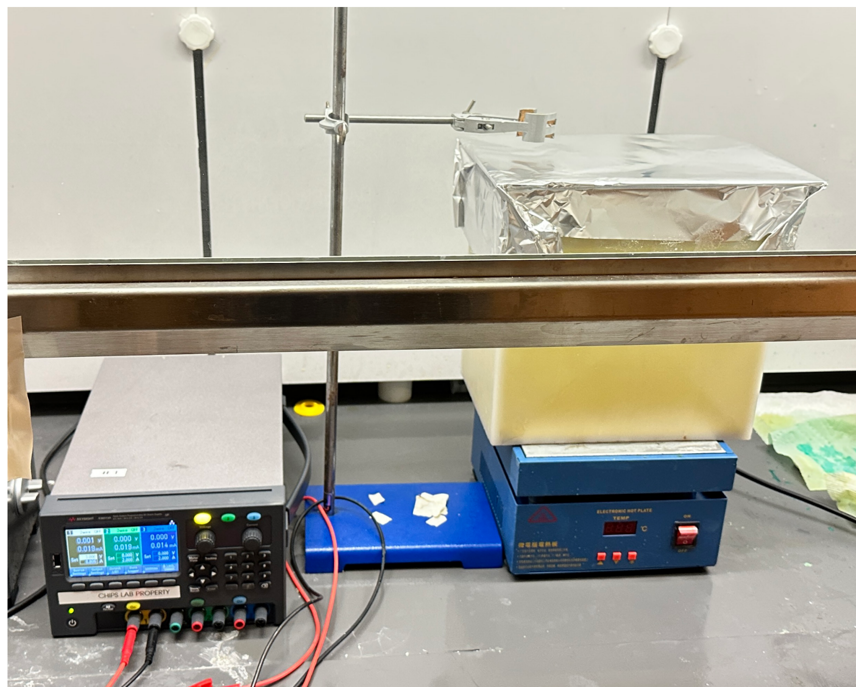
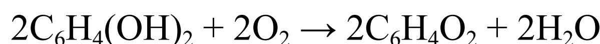


Fig. 2.2 The setup of lab owned Sn electroplating bath

The bath consists of various chemicals including additives for enhancing the ion transport and improving the film quality and uniformity. Aside from MSA which provides the bath its conductivity and drives the metal deposition on the cathode during plating , the bath consists of tin sulfate which acts as a grain refiner to deposit the metal in a controlled manner [8]. Furthermore, the bath consists of hydroquinone, an antioxidant, which reduces the rate of oxidation of stannous ion which is soluble in nature, into a sludge form, stannic ion [8]. Hydroquinone antioxidation reaction is as follows. [6]



$$2C_6H_4(OH)_2 + 2O_2 \rightarrow 2C_6H_4O_2 + 2H_2O$$

Setting up the plating system consists of cleaning the tank first. The tank needs to be leached and then cleaned. For leaching, 3% KOH is utilized, doing so takes away the contaminants such as dust or other organics. Moreover, this process is followed up by adding a 3% sulfuric acid necessary to clean out the KOH. The order of steps followed to clean the tank is given below:

1. The tank is washed and cleaned with DI water for 5 min.
2. The water is discarded into the sink.
3. The KOH was added into the tank for a quantity of 3 oz per gallon (199g in the tank) in the tank filled with two-thirds of DI water.
4. The DI water was added to the tank volume and stirred well.

5. The tank was heated to 55 – 60°C and kept to leach the tank for about 6-8 hours.
6. The solution was drained and the tank rinsed with DI water.
7. The tank was filled completely with DI water for about 30 min, and then drained and rinsed again.
8. The leaching solution was added to the tank by filling the tank to two-thirds, mixing it slowly with acid to make 3% solution by volume and constant stirring. This is an exothermic process.
9. The solution was left in the tank for a minimum of 8 hrs.
10. The solution was drained and the tank rinsed again with DI water. Step 7 was repeated again.

Once the leaching procedure was complete, the bath was made by pouring the chemicals in the following order [8]:

1. DI water up to 300 ml/liter (3 liter for the tank)
2. 1 liter MSA added slowly to the tank with constant mixing
3. 667ml of tin sulfate as the tin concentrate with proper mixing
4. 500ml of makeup solution with proper mixing
5. 150ml of Secondary A solution with proper mixing
6. 200ml of hydroquinone as the antioxidant with proper mixing

7. DI water was filled up to the mark on the tank so that the bath level is maintained between the marks on the tank.

2.2 Operation Manual of Electroplating System

The operation flow for the tin plating bath is as follows:

1. Prior to using the electroplating system, ensure that the solution level is below the lower marker. If not, pour DI water up to a level below the lower marker so that once the electrodes are input, the solution level stabilizes between the two markers.
2. Turn on the hot plate and insert the thermometer, after cleaning it with DI water, into the bath using the steel clamp.
    a. The hot plate should be set to:

Hot plate Temperature	**Bath Temperature**
100℃	44℃
110℃	45℃
125℃	46℃
130℃	47℃
135℃	48℃

Table 2.1 Hot plate temperature vs Bath Temperature values

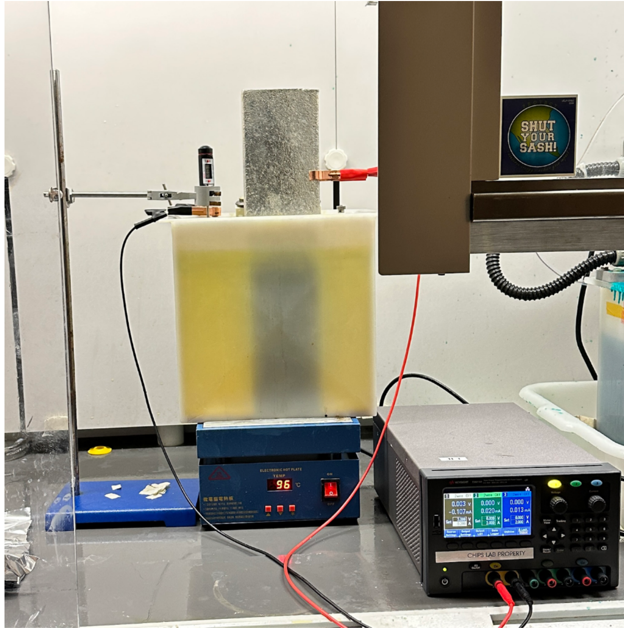
b. The hot plate to bath temperature variation depends upon the environmental conditions such as weather, and whether there are disturbances in the wet room.
c. The thermometer switches off about every 15 min, which needs to be switched on for temperature monitoring.
d. Once switched on, the hot plate takes about 3-6 min to attain the temperature and the bath correspondingly takes about 6-8 hrs to match the temperature as given above (subject to change depending upon the environment of the wet room) post heat loss by the tank.

3. After the bath reaches a close enough temperature, clean the Sn anode with DI water for about 4-5 min and insert it along the length of the tank, as shown in the figure 4.
4. The huge surface area from the anode displaces the solution increasing in height to maintain it between the two markers.
5. Meanwhile, check the conduction on the wafer before selecting it and thoroughly clean it and the cathode holder with DI water for about 3-4 min.
6. Place the cathode on the green area marked on the cathode holder.
7. The wafer needs to be connected electrically to the holder using copper tapes between the contacts on the holder and the wafer. The copper tapes need to be held in place using kapton tape (chemically inert) as shown in figure 5.

8. Rinse the cathode holder with DI water again and check for electrical conduction between the wafer and the holder using a multimeter. Ensure that the multimeter reads below 5Ω, otherwise, the resistance is getting contributed by improper connection with the contacts. Hence, either re-tape improper contact (if visible) or everything.
9. Calculate the exposed area of the wafer in cm^2 using a ruler. Multiple it with the current density (usually 0.5-2 ASD) to obtain the value of current.
10. Set the value of the current on the keysight power supply machine, using the knob which says current, for finer adjustments. For larger adjustments, simply input the number using the given number pad, and press "Enter". This sets the current value and thus the current density one wants to use to plate.
11. Place the cathode in the bath, so that the front side of the wafer faces the anode.
12. Connect wires to the power supply machine. The positive or the power gets clipped to the anode, and the negative or ground chord gets clipped to the cathode with the help of crocodile clips.
13. Once the bath reaches the desired temperature, switch on the power button on the machine to start the plating.

14. Write down the time and the voltage on the plating record sheet kept on the table in the wet room, along with bath temperature, plating time and the current.
15. Switch off all the lights in the room, and close the room shut for the entire duration of plating.
16. Once done, switch off the power button, make note of the end time and the voltage at the time of ending.
17. Remove the crocodile clips, and the electrodes one at a time. Use a glass beaker, to put beneath the electrodes while transferring them from the fume hood to the sink for post plating rinse out.
18. Use DI water to rinse off the acid on the electrodes for about 4-5 min. Keep the anode in the drawer labeled "Tin Anode" across the fume hood.
19. Rinse the cathode holder as well using DI water in the sink, and gently blow air using the valve labeled "air" in the fume hood to dry it off completely after removing the tapes.
20. Use tweezers to handle the wafers and place them in their respective box.
21. Keep the cathode holder in the drawer across the fume hood labeled "Sn cathode holder".
22. Turn off the hot plate, remove and rinse the thermometer, cap it and keep it on the table.

23.Cover the bath with aluminum foil.



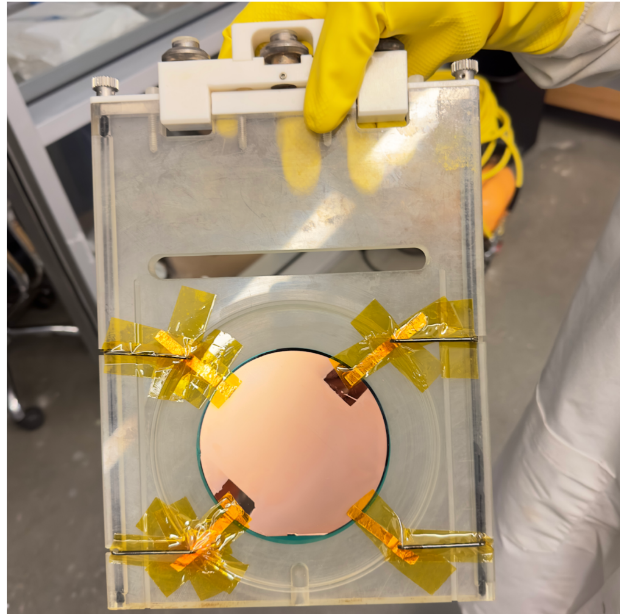


Fig. 2.3 (left) Placement of Sn anode in the bath
Fig. 2.4 (right) Fixing the cathode (4” Si wafer) on the cathode holder

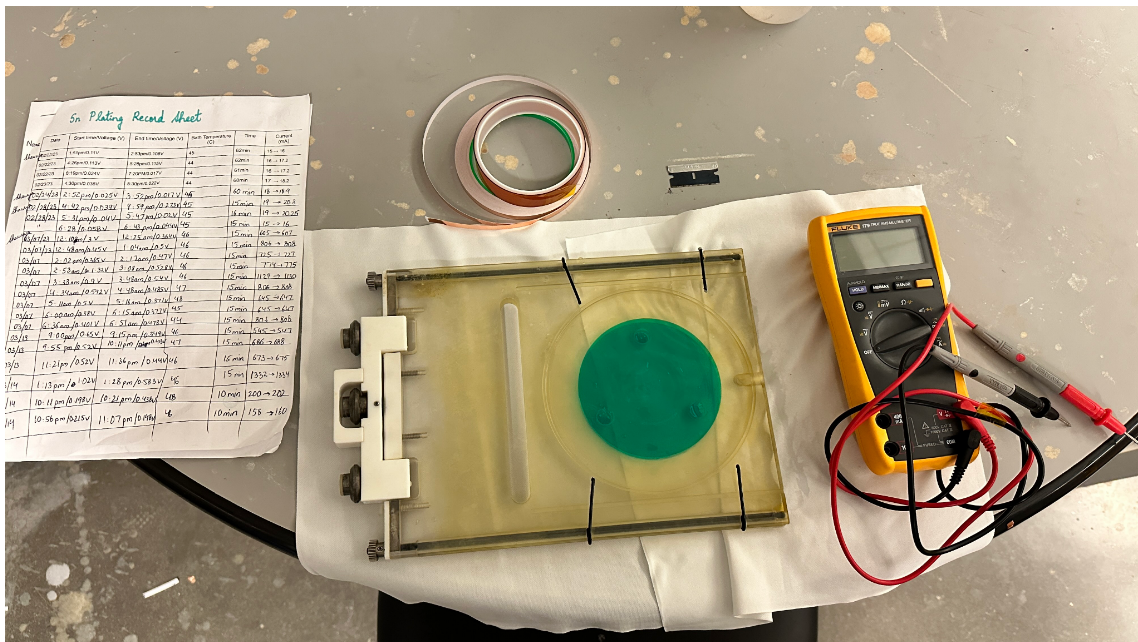


Fig. 2.5 Cathode Accessories; from left to right: Sn plating log sheet, (top) Cu tape and kapton tape, (bottom) Cathode holder, multimeter

2.3 Management of Electroplating System and Chemicals in Wet Bench

The lab-owned electroplating system needs to be used at least once every week to keep the bath activated. Furthermore, the system also needs to undergo maintenance on an annual basis. It is imperative to perform this task, as the system is located inside the fume hood which evaporates the electrolyte, water and other additives in the bath every day by a small amount which changes the concentration of chemicals inside the bath, that will change the quality of the electroplating system, changing the quality of the coated Sn. Therefore, it needs to be ensured that the solution level is either between the markers or just below the lower marker, and if not, then DI water needs to be added using a clean beaker, itself rinsed with DI water.

As part of annual maintenance, the tank needs to be fully drained out of the electrolyte, rinsed with DI water and then undergo the cleaning and leaching procedures as mentioned in section 2.1, cleaning steps 3 through 10. Since it takes a substantial amount of time to complete the maintenance, the system cannot be used for a while and the procedure therefore, needs to be planned accordingly.

The acids and other chemicals used during the process may be hazardous in nature, hence, it is suggested to wear the safety equipment which includes a lab coat, nitrile gloves and a visor. Moreover, the disposal along with the storage of

chemicals is crucial for our safety as well as the lab mates. The EHS, therefore, has set certain guidelines for chemical waste collection on Tuesdays. The waste is transferred into a large vessel and some unused empty chemical bottles and kept separately. The acid bottles are kept in the corrosion-free plastic cabinet and the organic chemicals are kept in the steel cabinet.

Fig. 2.6 Necessary safety measures for performing the electroplating process

From left to right: visor, yellow nitrile gloves, lab coat

Fig. 2.7 Acid bottles go in the plastic cabinet (left) and organic bottles stored in steel (right) [9]

Chapter 3

Process Development for Electroplating, Metrology and Characterization of Sn coating

3.1 Tools Used

In this chapter, I will be discussing the process development, observations, results and finally the discussions pertinent to the results.

The process was developed with the help of Technic Inc. and HallMark Metals in securing all the components desired for the building of the lab-owned Sn electroplating bath. After discussing the process development on Sn electroplating, I will present visual observation on the coating appearance, adhesion, results from the AFM performed in UCLA CNSI Nano Pico Laboratory, followed by XRD performed in Prof. Mark Goorsky's lab and lastly uniformity performed on surface profilometer.

Deposition	Denton Discovery Sputterer
Electroplating	Lab owned Sn plating equipment
XRD	Bede D1
AFM	Bruker Dimension FastScan SPM microscope
Thickness	Veeco Dektak 8 Profilometer
Adhesion Test	CGOLDENWALL Cross Hatch

	Adhesion Tester
SEM	Zeiss Supra 40VP SEM
Patterning	Miva

Table 3.1 Tools used for characterization & optimization of Sn plating

3.2 Electroplating

The Sn was plated onto a p-type Boron dopant 4" silicon wafer with <100> crystal orientation of thickness 500 µm. The wafer was sputtered with 350 nm Ti/Cu seed layer using the Denton Discovery Sputterer. The titanium was used for Cu adhesion on the Si wafer surface. Furthermore, the Sn electroplating was performed on 9 samples.

Sample SNo.	Temperature	Current Density
1	44℃	20mA/cm^2 (2.0 ASD)
2	45℃	20mA/cm^2 (2.0 ASD)
3	46℃	15mA/cm^2 (1.5 ASD)
4	46℃	20mA/cm^2 (2.0 ASD)
5	46℃	25mA/cm^2 (2.5 ASD)
6	46℃	30mA/cm^2 (3.0 ASD)
7	46℃	35mA/cm^2 (3.5 ASD)
8	47℃	20mA/cm^2 (2.0 ASD)
9	48℃	20mA/cm^2 (2.0 ASD)

Table 3.2 Electroplating conditions of various samples

The data for choosing the current density range and the temperature range was obtained through the technical data sheet provided by Technic Inc. for the JM6000 LS bath (MSA system) [8]. After sputtering, the Sn was electroplated on a 2.5” by 2.5” square box on every wafer as shown in figure.

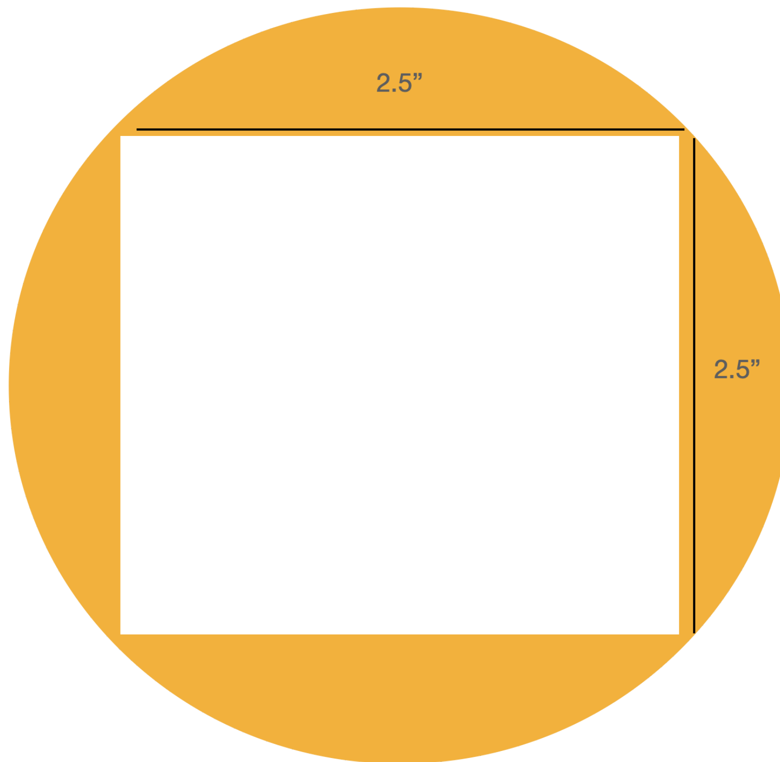


Fig. 3.1 Sn plated Si wafer schematic

3.3 Surface Roughness

Atomic Force Microscope (AFM) uses a small probe to scan over the surface and has feedback associated with it. The probe tip is usually a silicon tip which connects to the surface of the sample through Van Der Waals forces and oscillates

at a frequency just below the natural frequency of the probe. The Z height changes are addressed through a feedback loop which adjusts the amplitude of the tip from the surface accordingly and we get the topography of the surface measured.

We used the AFM for measuring the surface roughness over a 1µm by 1µm area. We took 4-5 spots per wafer before and after plating to check whether the roughness is coming from the wafer topography or the plated film. We measured surface roughness at the top, bottom, center, left and right.

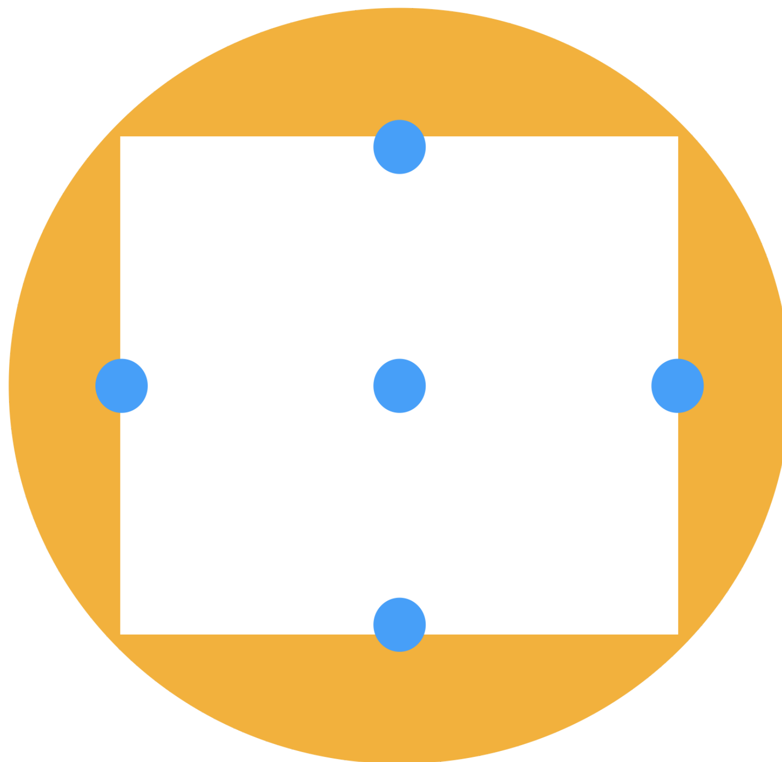


Fig. 3.2 Schematic of AFM spots represented by blue on the wafer

3.4 Thickness Measurement

The metrology on the wafer particularly i.e. thickness measurement to calculate the thickness as well as the plating rate (thickness/unit time) and figure out the trend of plating rate with respect to plating temperature and the current density. As the area of plating varied slightly, the plating rate was also calculated as thickness/unit area/unit time.

Thickness measurement was carried out using the surface profilometer, which is a topography measurement tool for the sample's uppermost layer [10]. With the help of kapton tapes, part of Cu seed layer was covered for creating a step, the height for which was calculated with respect to the Cu seed layer to get the thickness.

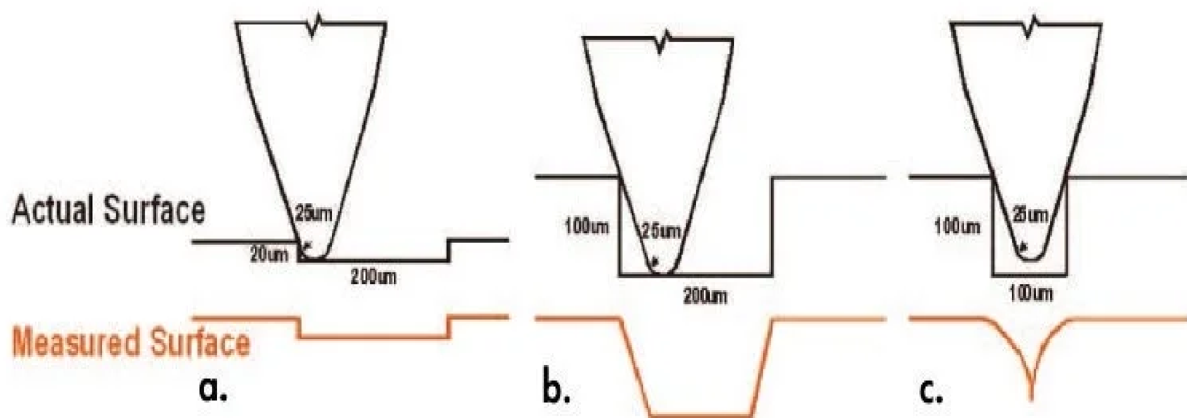


Fig. 3.3 Schematic representation of step height measurement using a stylus [11]

3.5 Crystal Phase and Grain Size variation

X-ray Diffraction (XRD) is a material characterization technique which uses monochromatic X-rays with a parallel beam on crystalline samples to find out crystalline phases and grain size estimation. XRD uses X-rays to diffract through crystallographic planes on which the beam is incident at an angle called Bragg angle. The constructive interference of the diffracted beams through a particular plane, also called as Bragg's law, gives the interplanar distance between two atomic planes and becomes the base for figuring out the miller indices of the plane, leading to peak referencing and crystalline phase determination. Bragg's law is the working principle for XRD.

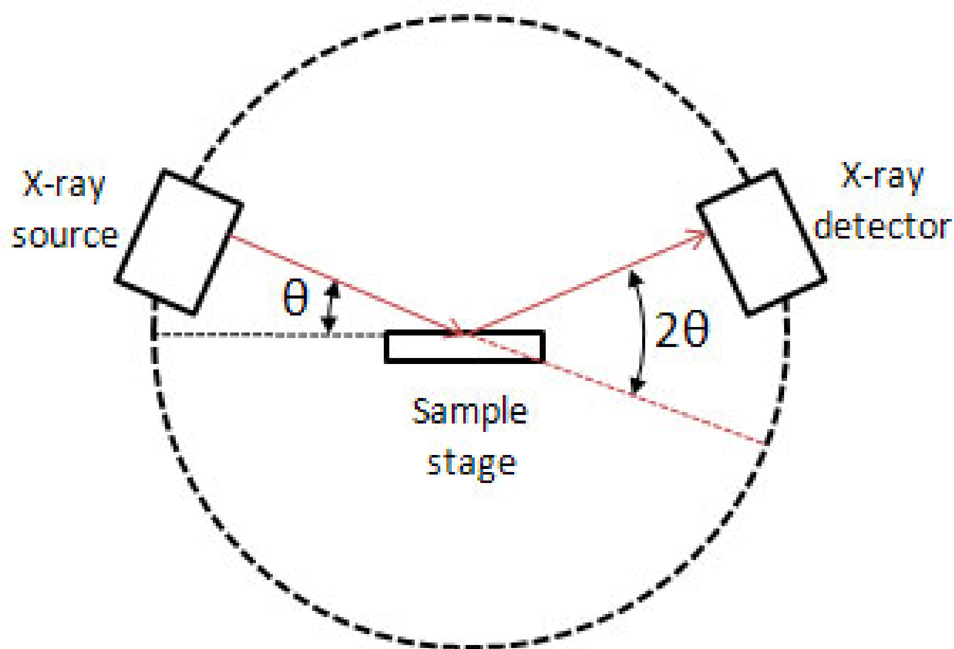


Fig. 3.4 XRD schematic [12]

XRD was used for grain size variation with respect to temperature and current density. Furthermore, to check the crystalline phase of Sn present in the coating. The scan size was about 2.5”, across the coating.

$$\text{Bragg's Law: } n\lambda = 2d\sin\theta$$

where λ is the wavelength of diffracted beam, d is the interplanar spacing and θ is Bragg angle.

3.6 Surface Morphology

Scanning Electron Microscope (SEM) is a material characterization technique used for mapping the surface morphology. It uses the kinetic energy of electrons as the working principle to give out various signals which are used to map the surface of the sample with up to 4 nm resolution. Zeiss Supra SEM uses a thermal emission gun to draw out electrons and accelerate them to a conductive sample for secondary electrons signals which is the best signal with ~5 nm penetration for surface characterization detected by an Everhart Thornley detector. This machine was used for grain size and geometry measurements to classify the use of 46℃ as

the electroplating temperature on samples plated for 1.5hr at a current density of 0.5mA/cm^2.

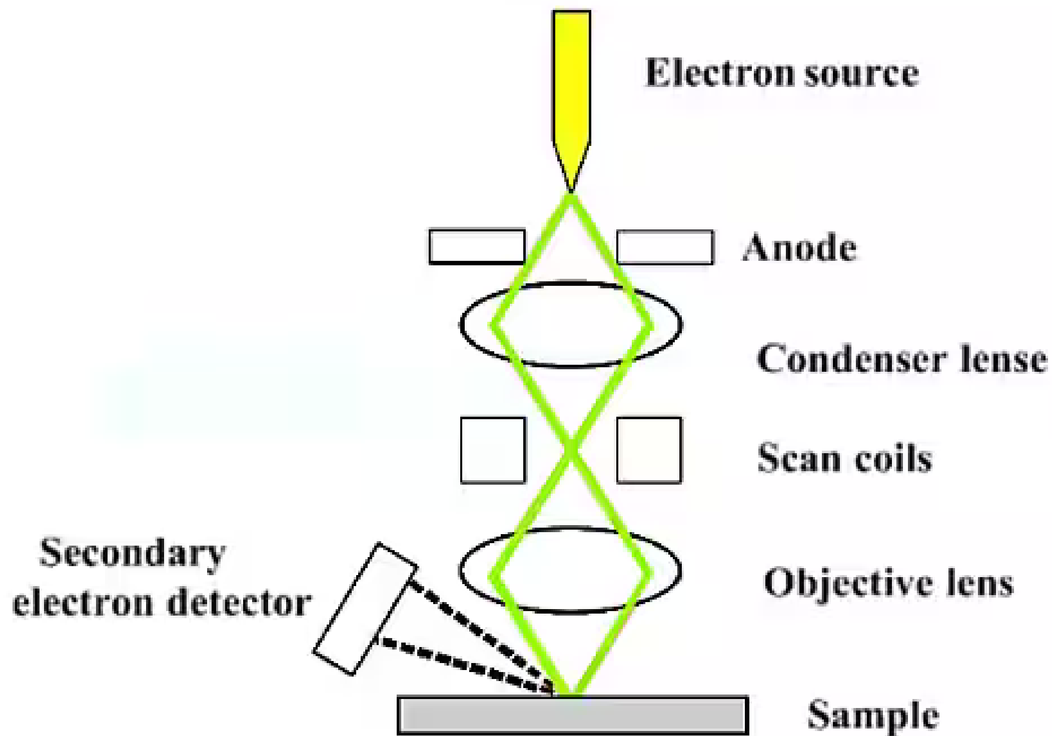


Fig. 3.5 SEM schematic [13]

3.7 Patterning

Using software called klayout, a 50x50 array of squares (areas for plating Sn) with dimensions 50x50 μm^2 was created with pitches as 10μm, 20μm, 40μm, 80μm and 160μm as shown in fig. 3.7 .

A photoresist mask (AZ-5214) was deposited throughout the wafer using spin coating and exposed using MIVA at the square regions on the wafer to create an opening for Sn to be plated as pillars of ~1.5-2μm.

Fig. 3.6 MIVA tool

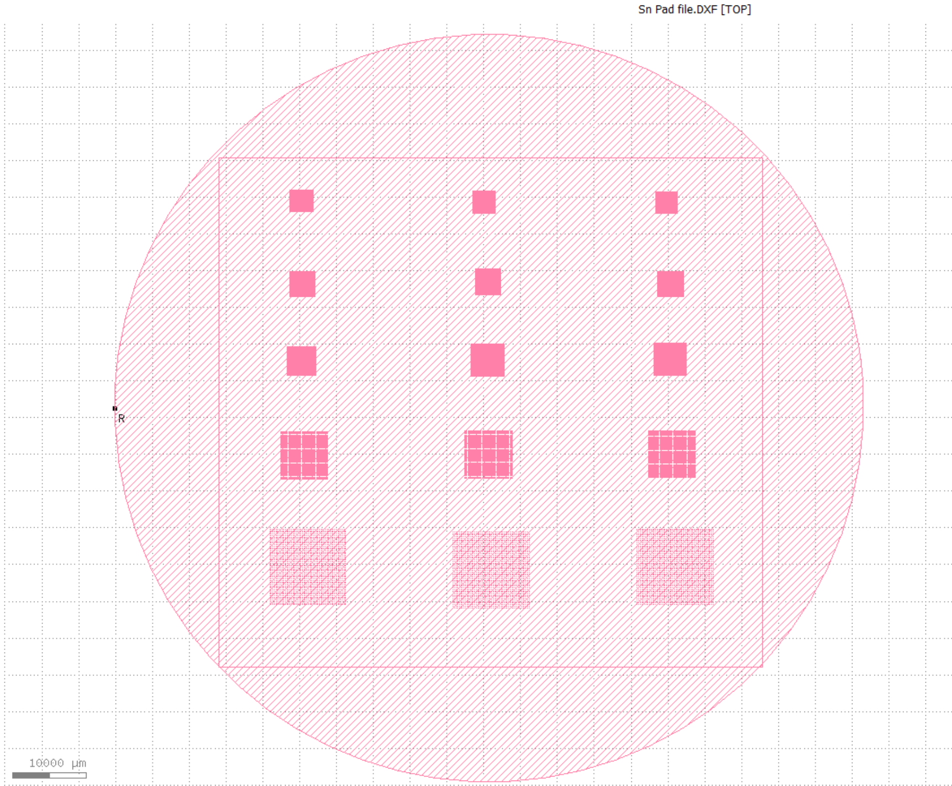


Fig. 3.7 Layout of squares for Sn pillar formation in a 50x50 array with different pitches

3.8 Thermal Reflow

The reflow oven is configured for a process called reflow soldering, which connects the die to the substrate both electrically and mechanically. The die is held in place on top of the Sn pillars electroplated on a Cu seeded Si wafer using a flux which is slightly adhesive in nature. The primary use of the flux is to evaporate the oxide in the reflow on and close to the pillars. To help with better contact, a bare wafer is placed on top of the inverted pads along with a weight.

The reflow oven has multiple sections set to different temperatures for heating and cooling. The reflow temperature is set to 265℃ (more than the melting point of Sn i.e. 232℃). The reflow is done to melt the electroplated Sn pillars and obtain microbumps for attachment of Cu pads laser drilled from other Cu seeded blanket wafer.

Fig. 3.8 Thermal Reflow Oven

Chapter 4

Optimization of Parameters for a uniform, dense and smooth Sn coating

4.1 Introduction

In this chapter, I will present the characterization and metrology data collected for the Sn electroplated Cu seeded Si wafers or coupons of Si wafers using SEM, XRD, AFM, Dektak and Adhesion tester and discuss the relation of crucial parameters like thickness, surface roughness, grain size.

4.2 SEM

SEM was performed on tin electroplated samples at 4 different temperature ranges as shown in the micrographs below to check the optimum temperature range at which the electroplating should be performed for obtaining a smooth uniform finish & optimum grain size of about 2-4µm for a desired coating thickness of 2-4µm to reduce the number of grain boundaries which ultimately increases the material resistivity [14]. As evident from fig.16b and 16c, the coating seems quite uniform with the grain size distribution in the desired range which is not the case in fig.16a and 16d. Therefore, a temperature range of 46-47℃ should be marked as optimum for performing Sn plating.

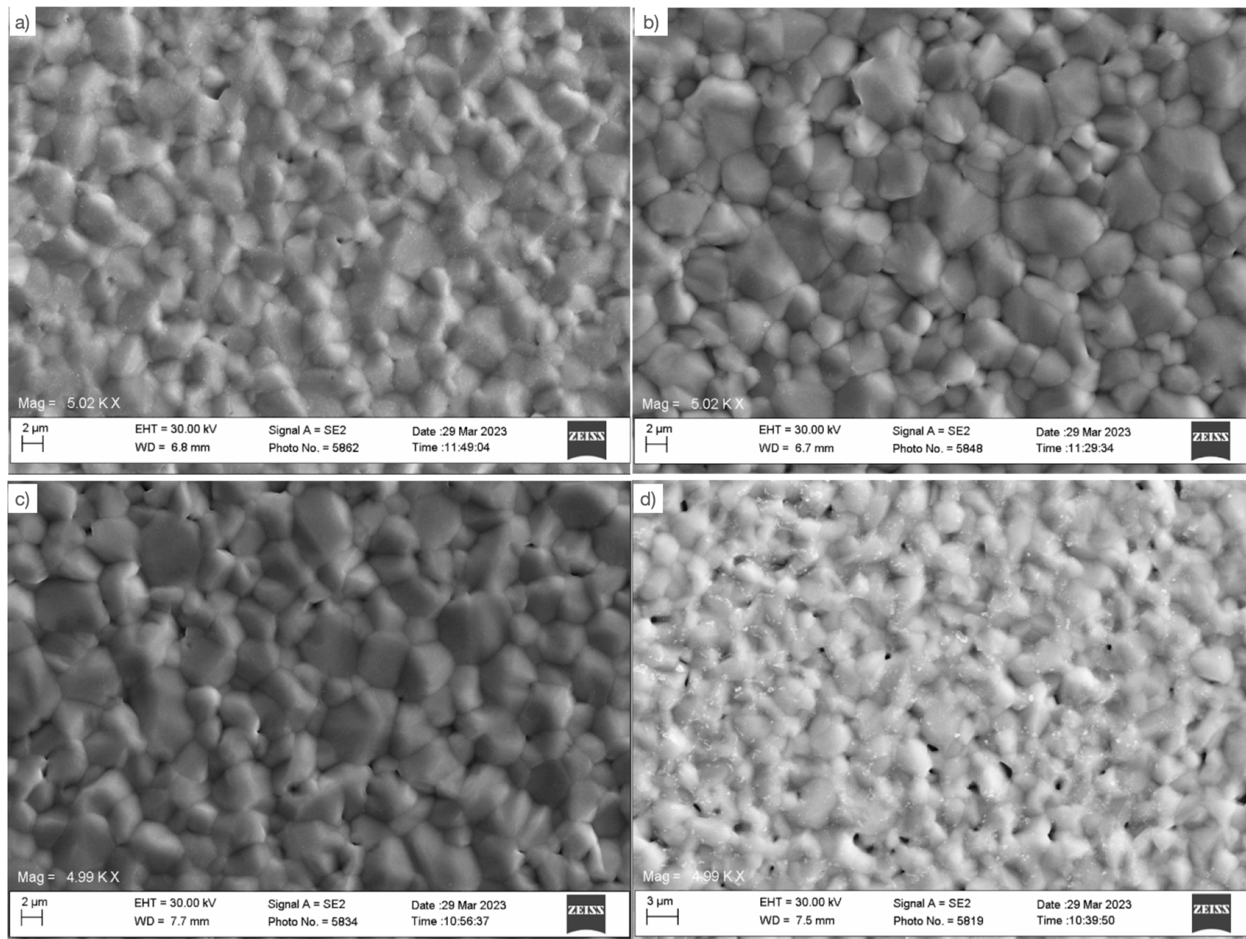


Fig. 4.1 SEM micrographs taken at 5X magnification for Sn coated samples at 0.5mA/cm^2 current density for 1.5hr to obtain the desired thickness with temperature variations:

a) 44±0.5℃ b) 46±0.5℃ c) 47±0.5℃ d) 50±0.5℃

4.3 Plating Rate

Plating rate was calculated for various current densities at a constant temperature range of 46-47℃.

4.3.1 Plating Rate v/s Temperature, Current Density, Plating Time

As the current density increases, naturally the plating rates were observed to increase as well. However, at higher current densities in the range of 15 to 35 mA/cm^2, not much variation was observed i.e. between 1.1 to 1.4 µm/min and the rate of change of plating rates with current densities seemed to slow down as evident from fig. 18.

Current Density (mA/cm^2)	Plating Rate (µm/min)
0.2	0.0025
0.5	0.028
1.5	0.099
8	0.534
15	1.184
20	1.38
35	1.35

Table 4.1 Plating rate w.r.t different current densities at a constant temperature range of 46-47℃

At 35 mA/cm^2, the coating was found to have Sn precipitates in the form of a powder enveloping the coating beneath as shown in fig. 17. The powder increases the surface roughness. Furthermore, some amount of Sn is wasted as it precipitates

out and can be wiped off. A detailed discussion can be found in an upcoming section.

The plating rate saturates above 20 mA/cm^2 and starts to decrease post 30 mA/cm^2 as is visible from fig. 19. This dip can be attributed to this system being acidic that leads to hydrogen evolution [15] which can lead to passivation of the cathode and non-uniform Sn coatings [16].

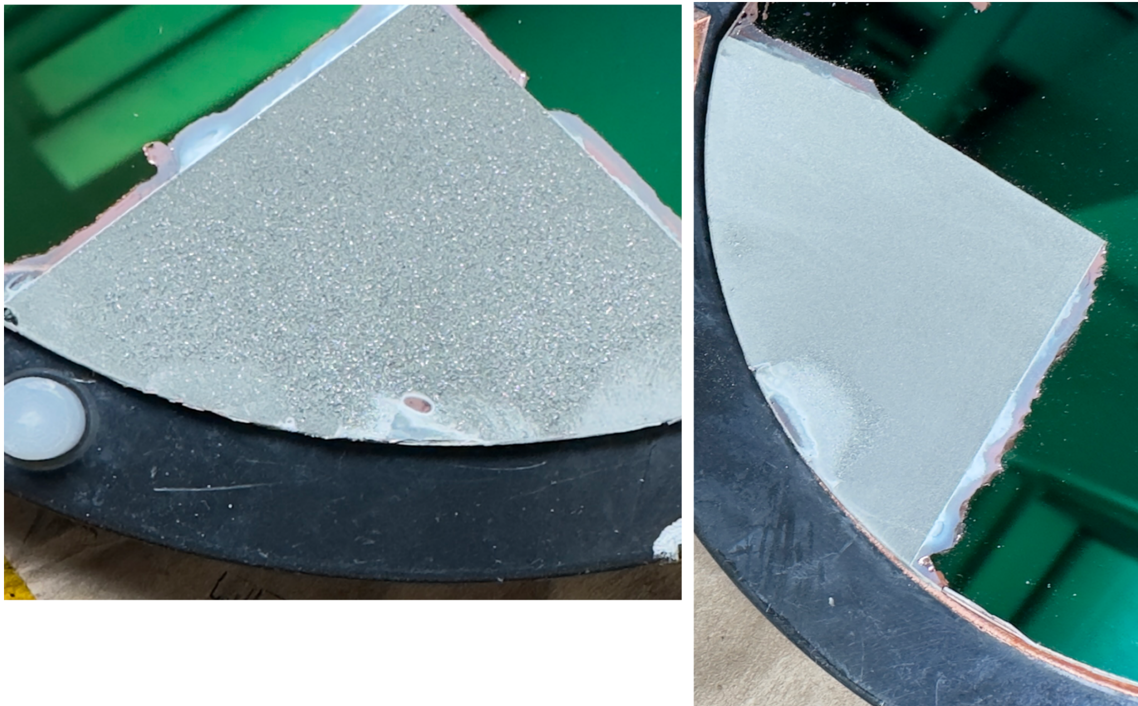


Fig. 4.2 35 mA/cm^2 at 46-47℃ a) after plating as-plated condition b) after wiping off the powder seen in 17a

In fig. 18, the plating rate was calculated while keeping the required thickness of 2-4μm as constant and varying the plating time. Similarly, fig. 19 was elicited keeping the plating time constant to 15 min. At higher current densities, I measured

the trend in differences in current densities w.r.t the plating times, varying the parameter as 15 min, 25min, 35min. Further increase in plating time

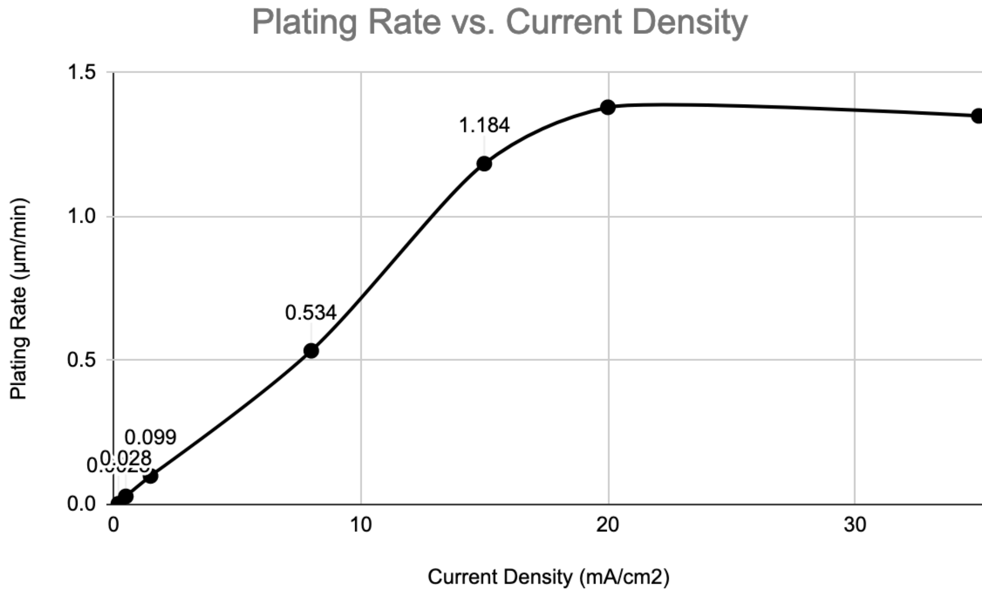


Fig. 4.3 Plating Rate vs Current Density at 46-47℃ at constant coating thickness

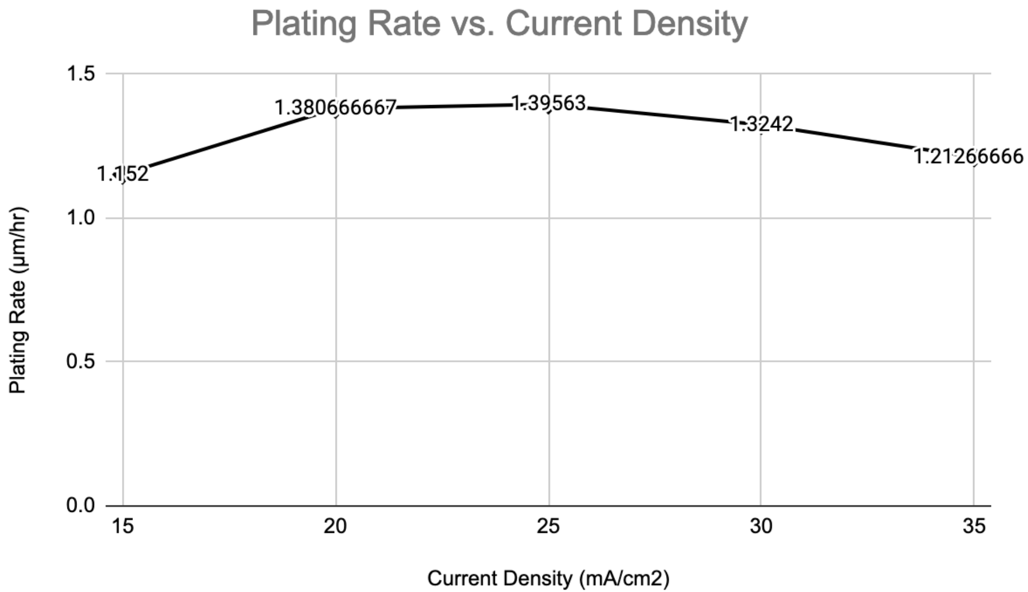


Fig. 4.4 Plating Rate vs Current Density at 46-47℃ for current density range 1.5-3.5 ASD at constant coating thickness

would result in an increase in the non-uniformity in the coatings. Furthermore, as shown in fig. 20, the plating rate slightly decreases with the plating time because of the fact that more the thickness or more Sn that gets deposited on the cathode, the number of active nucleation sites slightly increase, produced influencing a slightly higher nucleation rate, which can be attributed to the fact that the grain size decreases with increase in plating rates. Since, Sn grain growth is a three-dimensional diffusion limited grain growth [17], the rate of grain growth is more in the normal direction to the substrate than parallel to it. Besides, since the process is temperature controlled, as the plating rate increases with temperature and then nearly saturates beyond 46℃ implies diffusion limited growth.

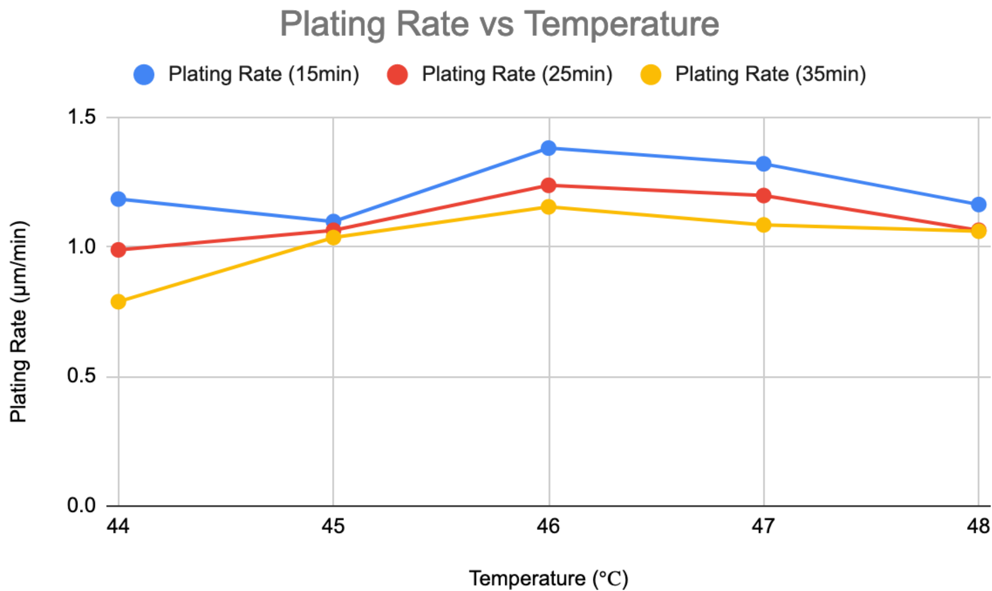


Fig. 4.5 Plating Rate v/s Temperature at 20mA/cm^2 current density at constant plating times

Furthermore, the general trend at a constant plating time shown is an increase in plating rate up to 46℃ as that is when the maximum number of Sn ions breach the kinetic barrier [19].

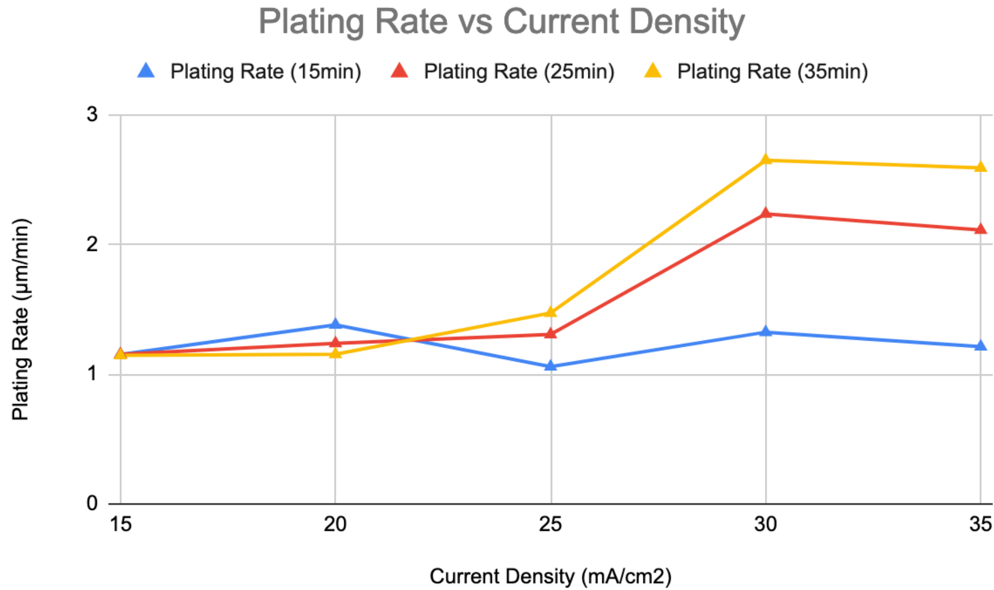


Fig. 4.6 Plating Rate v/s Current Density at 46℃ at constant plating times

The plating rates increase after 25mA/cm^2 because of the onset of nucleation of surface protrusions [18] which perhaps look like but are not single crystal Sn whiskers, which increase the surface area and hence the density of nucleation sites.

4.3.2 Grain Size and Crystal Phase

As the plating rate increases, the time for nucleation is less, which increases the nucleation rate and therefore the grain growth or the size reduces. First of all,

plating rate is primarily influenced by the current density, therefore an increase in current density should reduce the grain size. Secondly, temperature, which also determines the plating rate also influences the grain size. Normally, the temperature and grain size have a direct relationship, where as temperature increases, the grain size increases [18]. However, due to the bath consisting of grain growth inhibitors, the grain size doesn't increase. The grain size variation can be found in fig. 22 and 23.

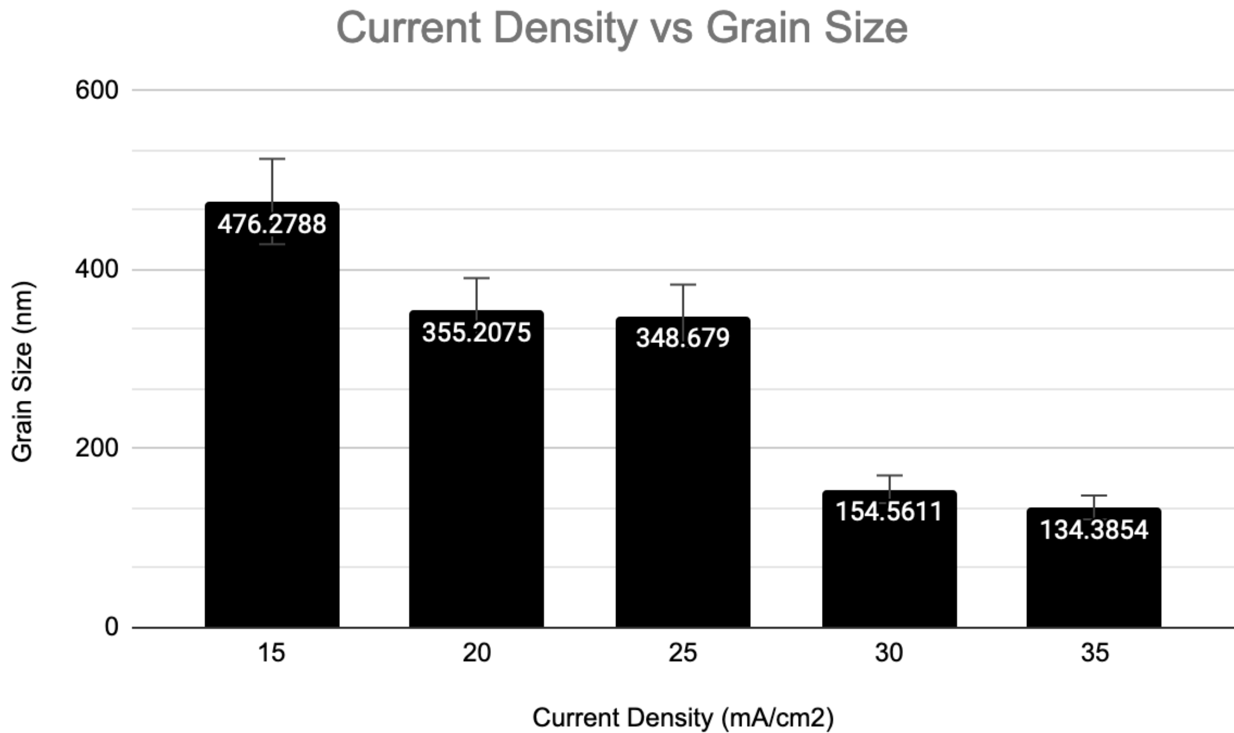


Fig. 4.7 Current Density v/s Grain Size at 46℃

There is a great variation in the grain size at same temperature across different current densities in comparison to the plating rate change (slope) in fig. 21.

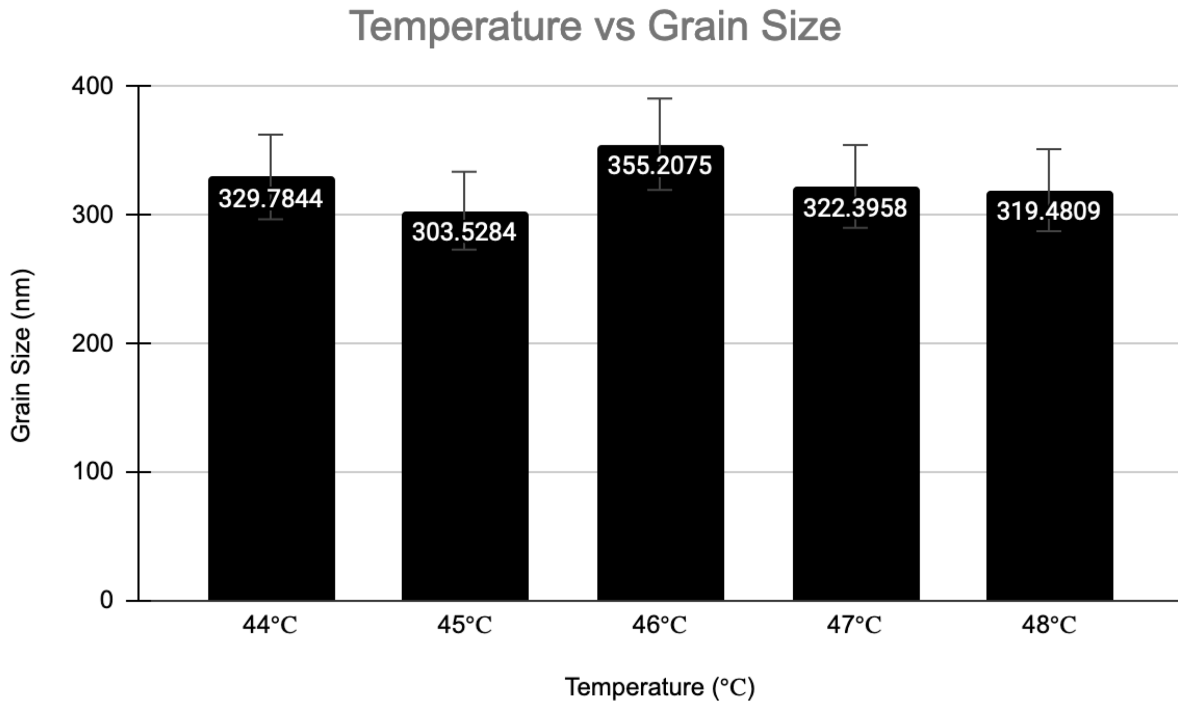


Fig. 4.8 Temperature v/s Grain Size at 20mA/cm^2 current density

The grain size variation across temperature is nearly the same in comparison to the plating rate change (slope) in fig. 20.

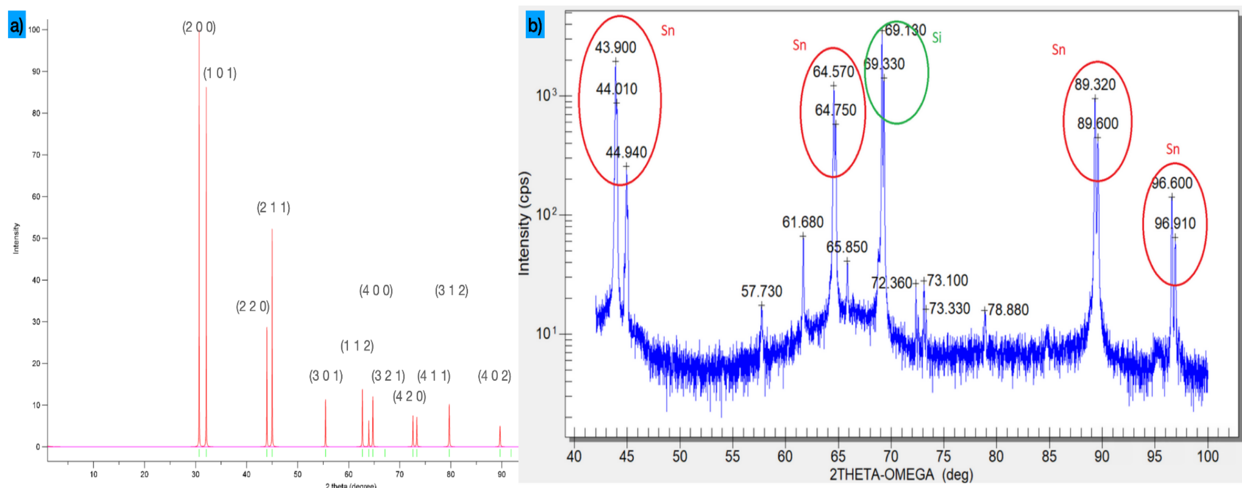


Fig. 4.9 XRD Peaks of a) reference **β**-Sn sample b) Sample 4

In fig. 24, the XRD data from sample 4 is compared against the reference **β**-Sn sample. As evident, the peaks are located exactly at the same 2θ values for the electroplated sample as the reference **β**-Sn data, which was generated by Vesta. The intensity values are different because the electroplated sample is not a homogeneous powder. The peak matching shows the presence of **β**-Sn with the body centered tetragonal crystal lattice in the electroplated sample, also known as white Sn which is metallic form of Sn and the desired phase. The other phase called gray Sn or α-Sn is non-metallic and brittle in nature which is highly undesirable for microelectronic applications. Upon performing XRD on all the samples, it was found that the presence of gray Sn was nil or negligible.

4.3.3 Plating Rate v/s surface roughness

The short wavelength surface roughness was measured using AFM. The wafers had non-uniformity in the Sn coating, as the roughness varied from as low as 2nm on one end of the wafer to 30nm on the other end. I used AFM to measure surface roughness near the edge where kapton tape was peeled off from and 1cm away from it to find similar roughness values, implying thickness doesn't have an effect on the surface roughness for such high plating rates of ~1μm/min. However, the substrate surface roughness along with the shape and area of the plated region definitely has an impact, which was studied.

The surface roughness majorly varied with respect to plating rate as it was found that the coating grew rougher with increase in the plating rate. Surface roughness was also influenced by the grain size. With increasing plating rate, the surface roughness increases with increasing plating times as the grain size decreases & the surface grew rougher with the introduction of more grain boundaries.

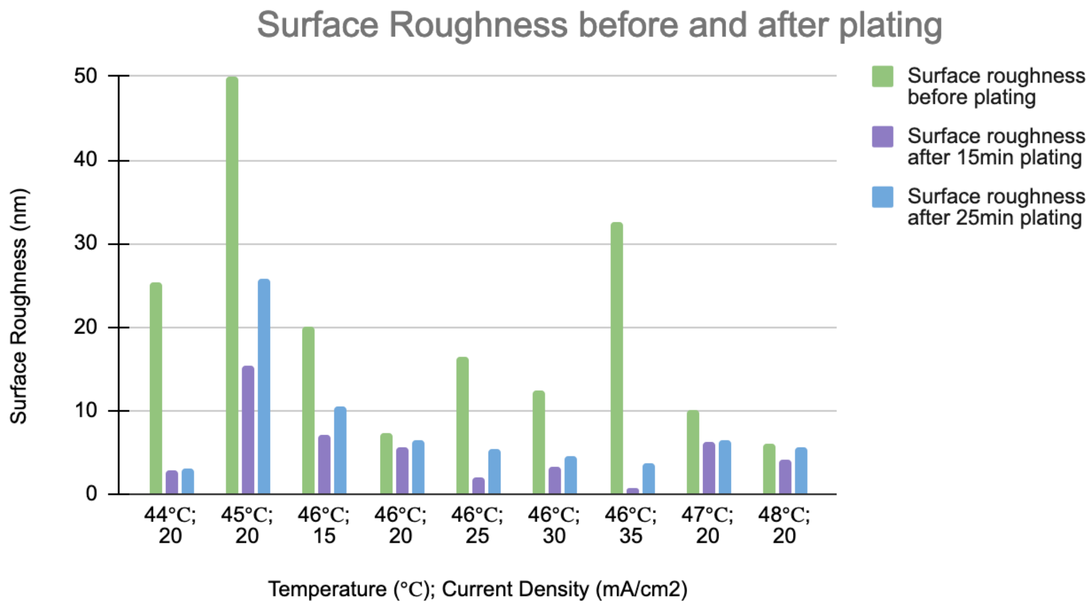


Fig. 4.10 Short wavelength surface roughness values in nm for substrate and after plating for 15 and 25 min

While there is no correlation between surface roughness across constant plating times of 15min and 25 min, the surface roughness is increasing as the plating time is increasing from 15 to 25 min. The surface roughness for Sn decreases from that of the substrate. However, long wavelength roughness revealed very high overall roughness ~4-5µm for 25 min plating beyond the substrate roughness.

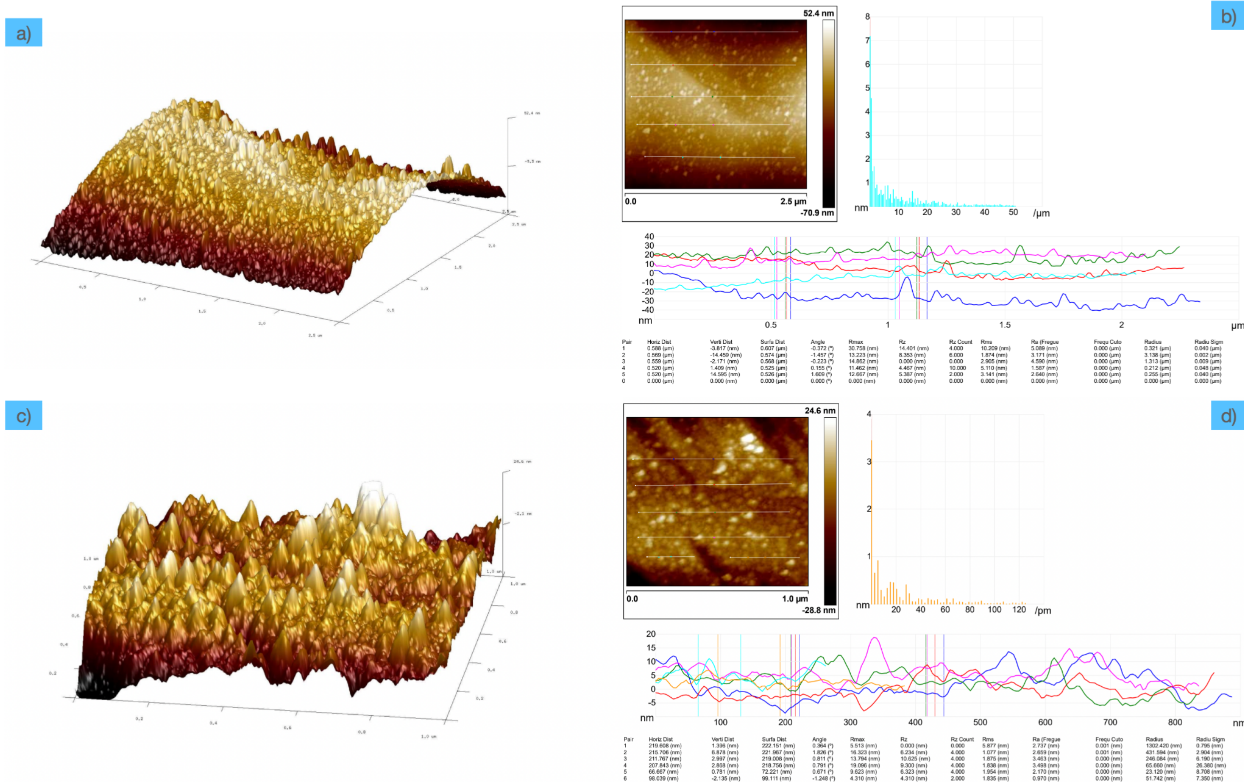


Fig. 4.11 1µm AFM Scans for surface roughness at 15 min plating rate (a and b); 25min plating rate (c and d) a) and c) 3D image b) and d) surface roughness section scans

4.3.4 Appearance v/s Surface Roughness

The change in surface roughness is visible through the differences in appearances of electroplated Sn coatings of various thicknesses. In fig. 27b the square is plated further hence a change in appearance on top of the square itself with 4 small rectangles. There are 3 finishes, a) bright finish, b) satin bright finish and c) matte finish [20].

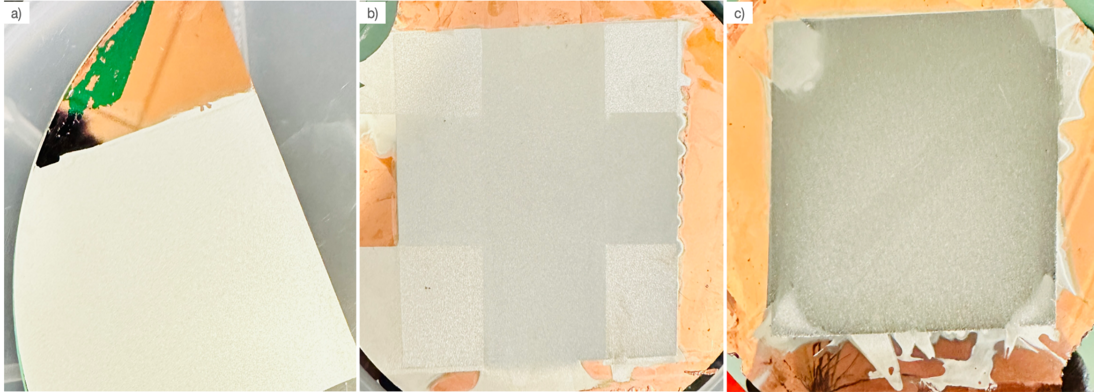


Fig. 4.12 Appearance of the Sn electroplated films of various thicknesses a) 2-4µm b) 10-25µm c) >25µm

4.4 Uniformity

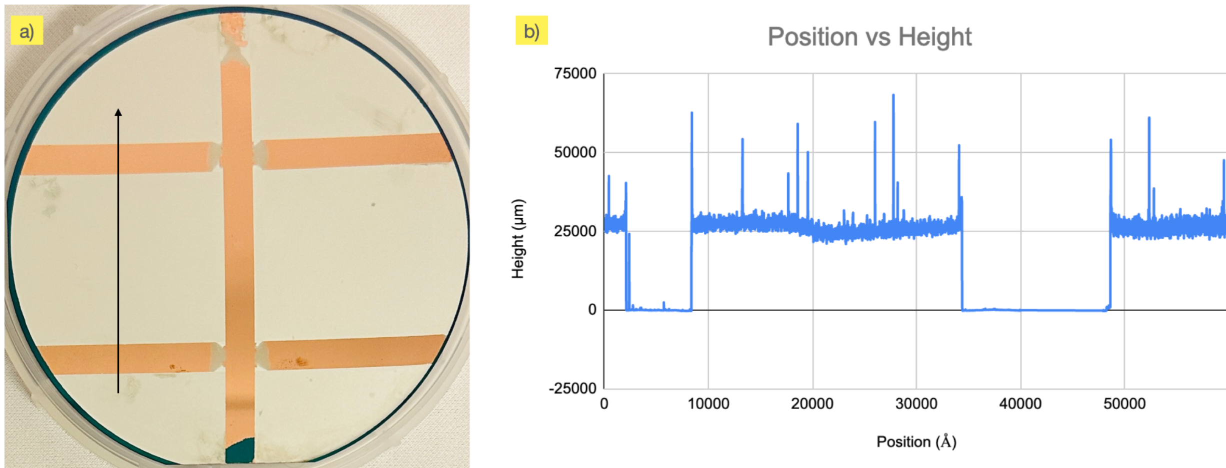


Fig. 4.13 Uniformity measurement through Dektak a) Wafer designed for uniformity measurement with the vertical measurement arrow on the wafer b) Position v/s Height Dektak measurement

The parameters were optimized for a uniform Sn coating. The vertical measurement shows coating uniformity with the long wavelength surface roughness around 5-10 nm in fig. 28, 29, 30.

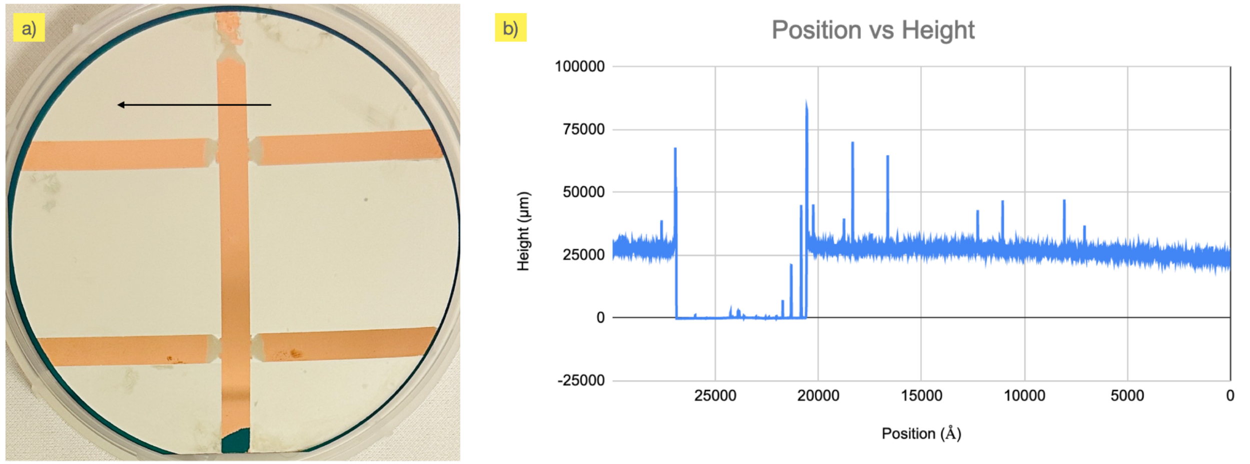


Fig. 4.14 Uniformity measurement through Dektak a) Measurement arrow on the wafer left to right b) Position v/s Height Dektak measurement

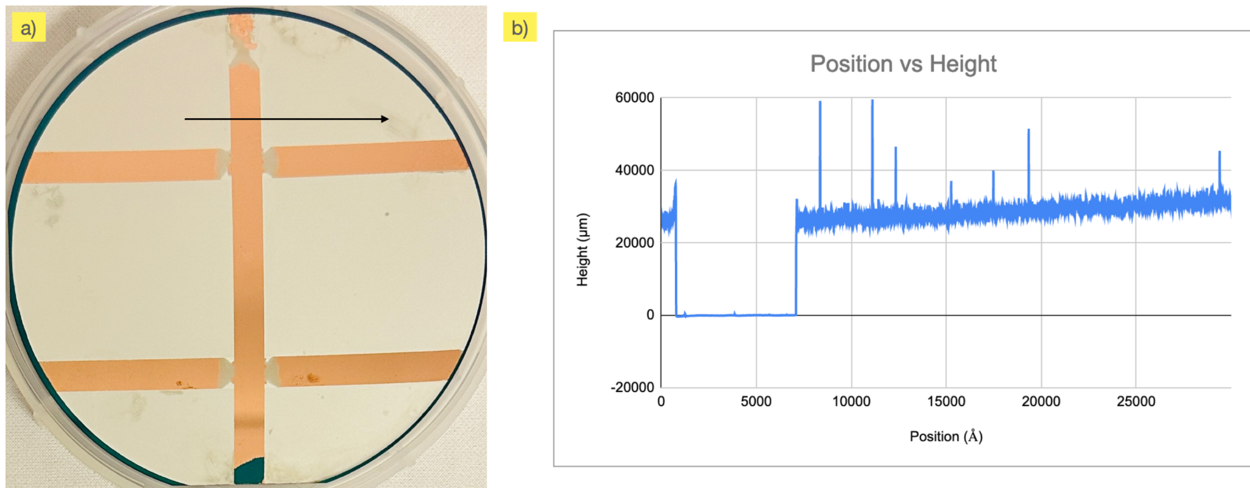


Fig. 4.15 Uniformity measurement through Dektak a) Measurement arrow on the wafer right to left b) Position v/s Height Dektak measurement

4.5 Surface Protrusions in high thickness coatings

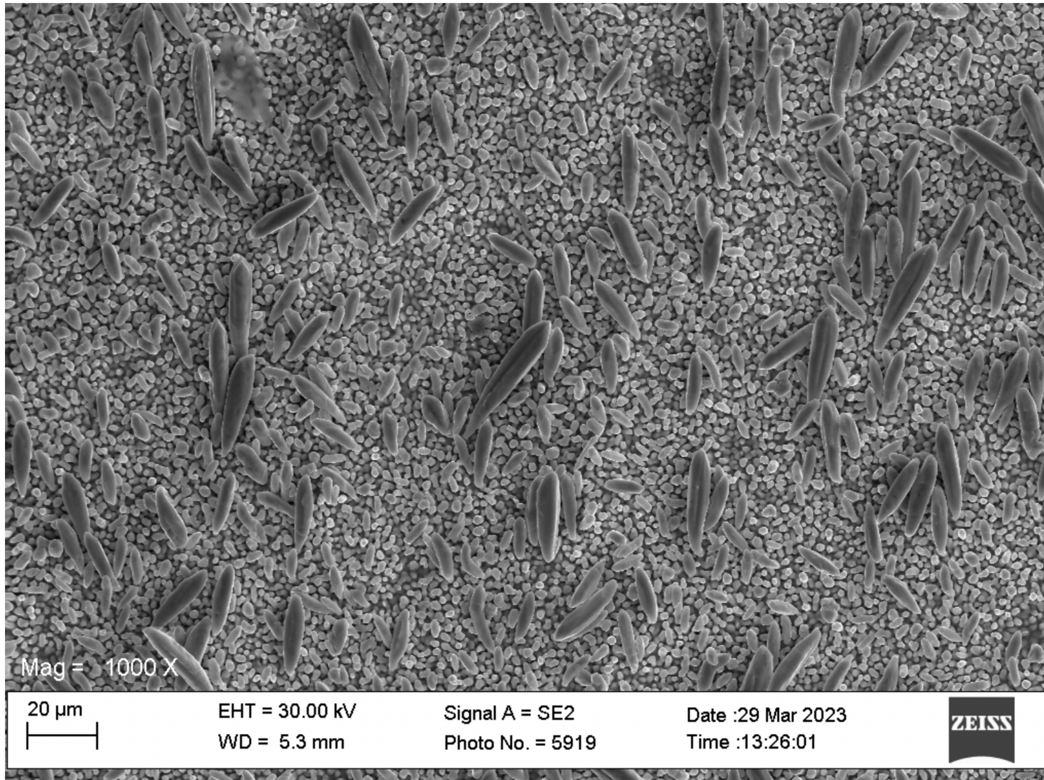


Fig. 4.16 SEM micrograph at 1000X magnification for sample electroplated at 30mA/cm^2 current density at 46℃ for 25 min.

The SEM micrographs on and above 30 mA/cm^2 current density start showing surface protrusions [18] and are only visible after a certain critical thickness is reached (>40μm) because of accumulation of the discharged metal ions. Initially, metal ions are distributed uniformly over the substrate, but as plating continues, a metal-ion denuded layer (MIDL) forms, which is thicker in some areas than others [21]. Metal ions are preferentially supplied to the thinner regions of the MIDL, resulting in the nucleation of surface protrusions.

The surface becomes increasingly smooth with temperature, which decreases the number of sites where adatoms (atoms that land on the surface) can be adsorbed. As a result, the number of nucleation sites and the nucleation rate of the pyramid-shaped features decrease with an increase in plating temperature. However, the protrusions that have already nucleated continue to grow, and new metal ions are preferentially discharged at their tips due to the local increased current density. As a result, the size of the pyramid-shaped surface features increases with plating temperature while their density decreases. The formation of pyramid-shaped protrusions helps minimize the overall surface energy by exposing the lowest energy plane of Sn (tin) i.e. {101} planes [22][23].

4.6 Adhesion Test

A tape test was used to analyze the adhesion of Sn electroplated coating over the Cu seed layer or electroplated layer using a CGOLDENWALL Cross Hatch Adhesion Tester and a 3M scotch tape. In the ASTM adhesion test Method-B [24], a specialized tool with 11 blades 2mm apart is used in the front head to make a scratch on the coating surface twice. Once, one set of scratches is implemented, the coating is turned by 90° and then another set of scratches are implemented. Finally, a 3M scotch tape given in the testing kit is used to stick on the scratches. After

keeping it adhered for some time, it is peeled off within 1-2 sec, with slight pull at a 60° angle.

The test was performed on coatings of different thicknesses ranging from too thin about 100 nm, followed by our desired thickness of 2-4µm, next 10-25µm and finally, >25µm.

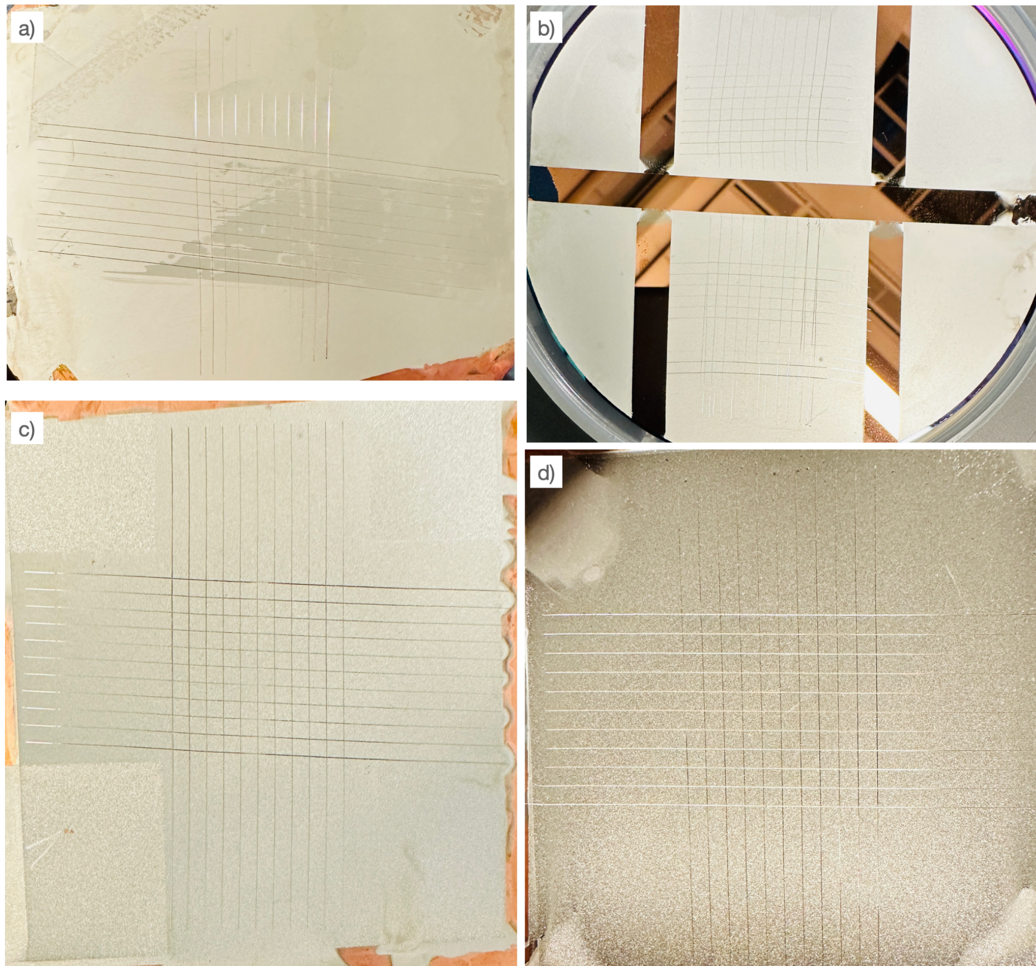


Fig. 4.17 Scratch marks for adhesion test on a) 100 nm thick coating b) 2-4µm coating on wafer designed for uniformity test c) 10-25µm coating d) >25µm coating

The test revealed peeling off of the very thin 100 nm thick coating as it was found to be extremely thin for proper adhesion. 2-4µm thick coating did extremely well, with no flaking in the form of filaments and the scotch tape was devoid of any particles. The 10-25µm thick coating showed minor particle removal on the scotch tape and lastly the >25µm thick coating had majority shiny Sn particles removed off the top of the scratches onto the tape. Therefore, the coating was optimized for adhesion for the desired thickness of 2-4µm.

4.7 Die attachment

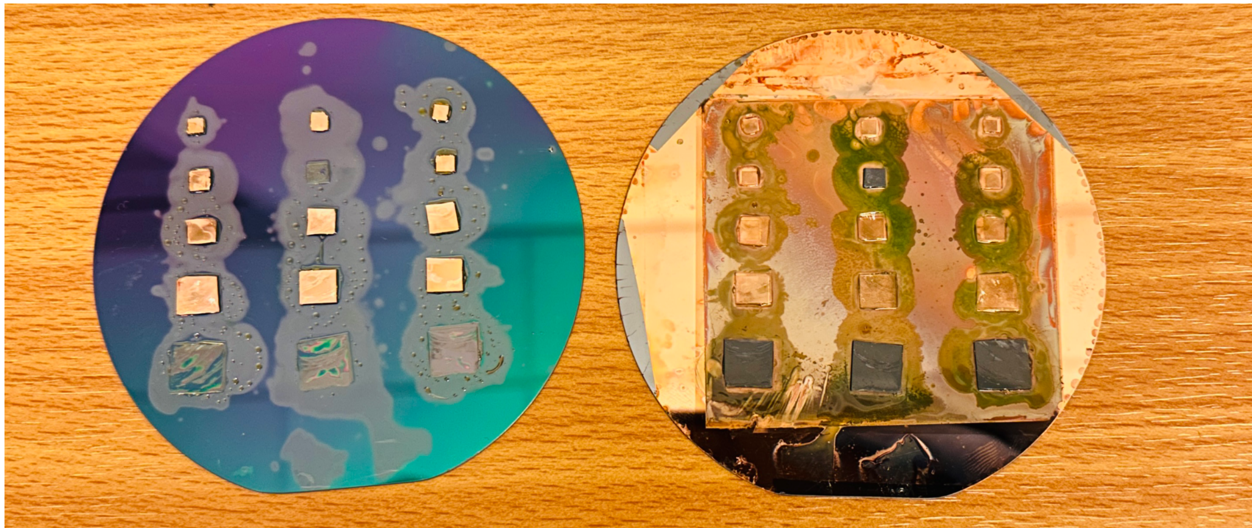


Fig. 4.18 (left) Wafer on top during reflow acting as weight; (right) Cu seeded wafer with electroplated Sn pillars in 50x50 square arrays with 10µm, 20µm, 40µm, 80µm, 160µm pitches from 1st to 5th row respectively having dies attached on top after reflow

After optimizing the parameters, the Sn pillars were plated using the parameters procured through the series of experiments and attached to Cu dies using thermal reflow. In fig. 4.18, the left wafer was on top of the right wafer (with Sn pillars), and due to improper contact the other dies could not attach well. However, 20µm pitch (2nd row middle die) and 160µm (5th row) dies are attached as well as they made more contact. Therefore, a shear test was performed using Dage Shear Tester on dies from both the pitches to find the breaking points at 28.26N and 47.37N.

Fig. 4.19 Microstructure of non-bonded die on the top wafer post reflow at 300x

Fig. 4.19 shows contact of the non-bonded die with the reflown Sn pillars, however it came off with the top wafer because of presence of some flux on top of the die additional to the fact that the overall contact area with the pillars was less, as

visible on the left side of the image. The pillar marks seem to fade away, because of non-planarity induced due to laser drilling of Cu square dies.

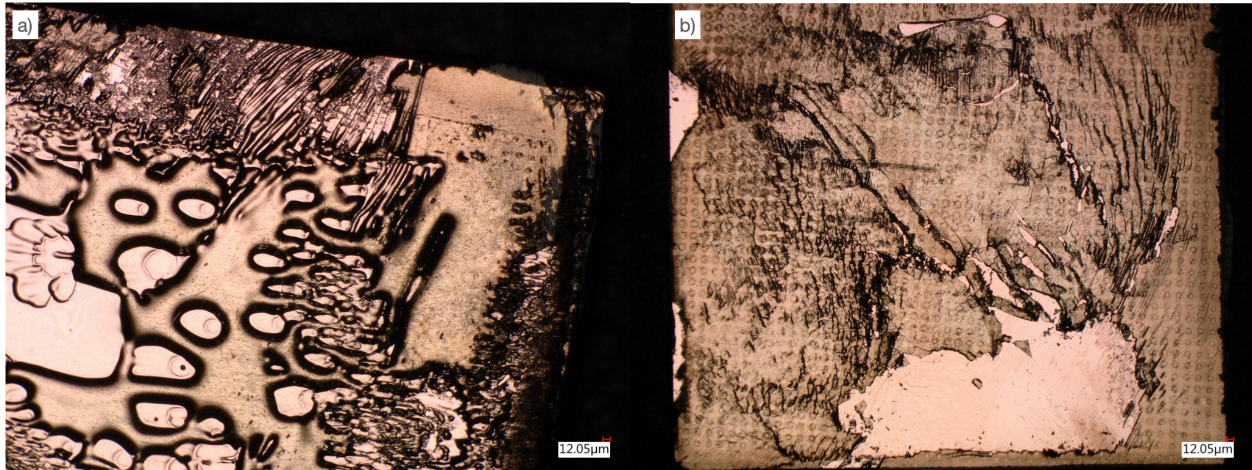


Fig. 4.20 Microstructure of bonded dies at 300X for a) 20µm pitch b) 160µm pitch

The problem lies with the presence of too much flux, and not the hypothesis that the Sn got smeared due to excessive weight put on top as is visible through the cross section of the interface taken for the 160µm pitch die in fig. 4.20. The marked region is perhaps the Sn microbump which only makes the issue of having too much flux and unknown pressure on top hindering a good bond between the Sn pillar and Cu die for dies with other pitches.

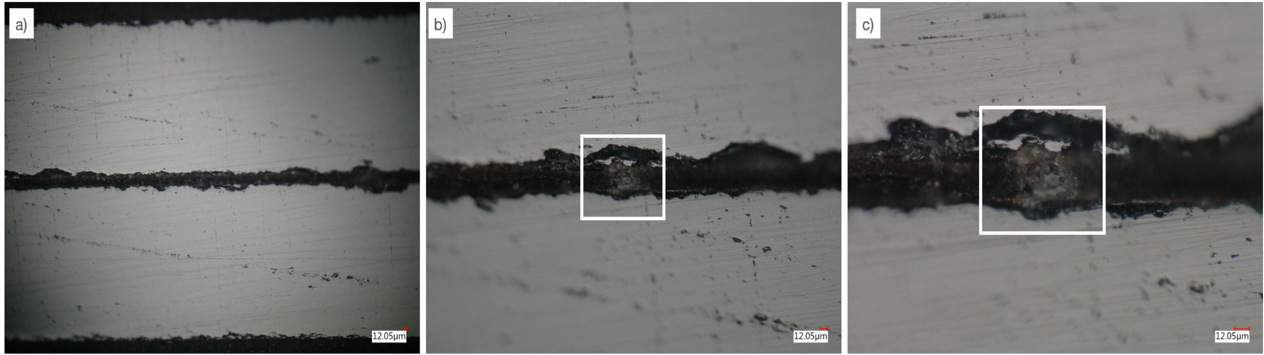


Fig. 4.21 Microstructure of substrate with Sn pillars (bottom) and Cu die (top) with marked region defining what maybe the Sn microbump at a)200X b)300X and c)500X magnifications

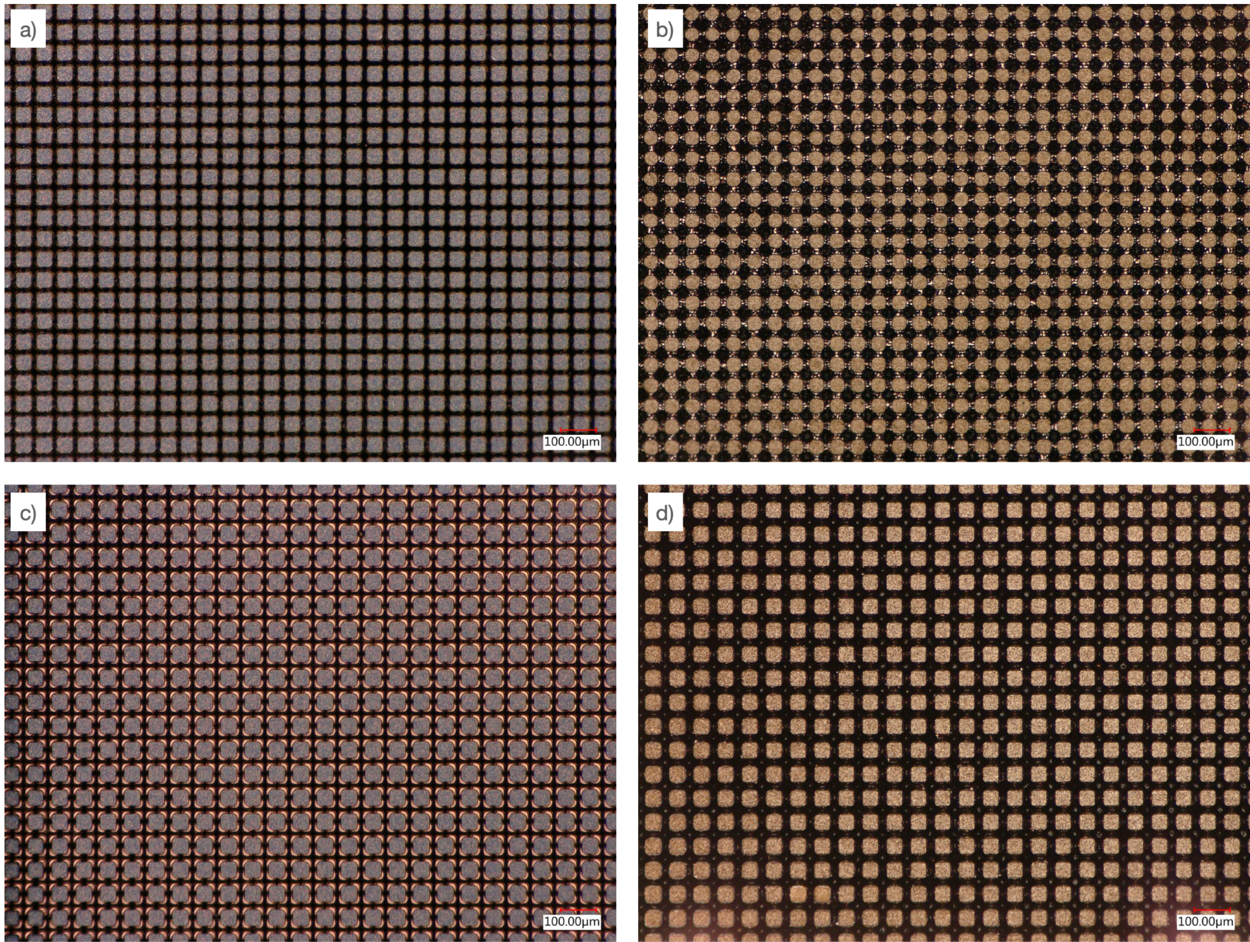


Fig. 4.22 Top down microstructure of Sn plated pillars with a) 10µm pitch with photoresist b) 10µm pitch without photoresist c) 20µm pitch with photoresist d) 20µm pitch without photoresist

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this thesis, the electroplating process of pure Sn for solder applications was developed and the coating characterized for optimization.

The objective was to achieve a dense, smooth, uniform Sn coating over a Cu sputtered/electroplated 4” Si wafer. An acidic bath was preferred over alkaline baths because of their lower power consumption and lower pH (<7) value which does not negatively impact the photoresist. Therefore, acidic baths are most common in microelectronics applications.

First of all, the temperature range was optimized using different plating rates for the desired thickness range of 2-4μm. It was evident from SEM images in fig. 16, that 46-47℃ is optimum for good quality coatings with desired grain size of 2-4μm to increase the bulk conductivity and reduce grain boundaries. The plating rate was calculated using the thickness measurements from Dektak, the relation for which was procured with respect to other plating parameters such as temperature, current density and plating time. The plating rate varies the most with current density at the optimum temperature range. With temperature, the plating rate nearly remains constant with the maximum at the optimum range among the accepted

temperature range of 43-48℃ as proposed in the data sheet by Technic Inc for the JM6000 LS MSA based electroplating bath. The increase in plating time reduces the plating rate. Hence, by adjusting the current density to 0.5 mA/cm^2, the plating rate was optimized for a uniform, good quality Sn coating. At the chosen plating rate, the sample was kept for 90 min. Because of the grain refiner in the solution, at the large grain size distribution of 2-4μm, the surface roughness achieved was also about 5-10 nm thereby producing a smooth coating. Furthermore, the sample at the desired thickness also passed the tape test which is the initial test for adhesion. Therefore, the objective of the thesis to obtain a dense, uniform, smooth pure Sn electroplated coating was achieved at 46-47°C temperature range and 0.5 mA/cm^2 current density.

The Sn electroplated was tested for bonding strength as well using thermal reflow, however, using APAMA tool for D2W metal-metal TCB seems a better option as we would need to know the pressure applied from the top for keeping the die aligned during bonding.

5.2 Future Work

The future work can be to study the Sn whisker growth [22] and formation through the presence of intermetallics which induce internal stress in the lattice [25]. The

whisker growth can be reduced by additions of Bi in small amounts [25] and Indium as well [26].

Furthermore, an extension to this project is to break the uniformity wafer into small pieces for APAMA tool bonding and characterize the bump formed electrically for better conductivity and its optimization.

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