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Development and Optimization of Electron Transport Layers for Perovskite Solar Cells using Physical Vapor Deposition

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Development and Optimization of Electron Transport Layers for Perovskite Solar Cells using
Physical Vapor Deposition

A Thesis submitted in partial satisfaction of the requirements
for the degree Master of Science

in

Nanoengineering

by

Apoorva Gupta

Committee in charge:

Professor David P. Fenning, Chair
Professor Darren J. Lipomi
Professor Oscar Vazquez-Mena

2023

The Thesis of Apoorva Gupta is approved, and it is acceptable in quality and form for publication on microfilm and electronically.

University of California San Diego

2023

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LIST OF ABBREVIATIONS

PSK   Perovskite

PVD   Physical Vapor Deposition

ETL   Electron Transport Layer

HTL   Hole Transport Layer

SAM   Self-Assembled Monolayer

BCP   Bathocuproine

PASCAL   Perovskite Automated Solar Cell Assembly Line

HOMO   Highest Occupied Molecular Orbital

LUMO   Lowest Unoccupied Molecular Orbital

PSC   Perovskite Solar Cells

TCO   Transparent Conducting Oxide

ALD   Atomic Layer Deposition

PSC   Perovskite Solar Cells

$FAPbI_3$ Formamidinium lead iodide

PbI_2 Lead Iodide

ACKNOWLEDGEMENTS

ABSTRACT OF THE THESIS

Development and Optimization of Electron Transport Layers for Perovskite Solar Cells using
Physical Vapor Deposition

by

Apoorva Gupta

Master of Science in Nanoengineering

University of California San Diego, 2023

Professor David P. Fenning, Chair

Perovskite Solar Cell (PSC) technology has gained a lot of interest in the photovoltaics community due to their excellent opto-electronic properties. The inverted architecture (p-i-n) PSCs are especially promising from a commercialization point of view. Herein, we developed an automated deposition process for Electron Transport Layer (ETL) C60 and interfacial buffer layer BCP using a scalable deposition technique, physical vapor deposition (PVD), to establish a baseline for p-i-n devices based on a wide bandgap Perovskite composition. With the help of

a Perovskite Automated Solar Cell Assembly Line (PASCAL) robot and with multiple iterations on devices, we were able to show reproducibility in the fabrication process of single-junction devices, which is typically one of the main advantages of adopting a scalable technique such as PVD. Additionally, devices showed reasonable performance, with a PCE of 17%, V_{oc} of 1.02 V, and J_{sc} of 20 mA/cm^2. To implement these devices into tandems, which require a transparent top cell and therefore a sputtered transparent conductive oxide top contact which necessitates a sputter buffer layer, we investigated PVD SnO_x as a replacement ALD SnO_x (difficult to commercialize). However, it was shown that the as-deposited SnO_x isn't dense enough to act as a protection layer, requiring an alternative buffer layer and/or alternate TCOs which have a soft-landing deposition process. Lastly, using implied V_{oc} calculations, it is shown that much of the PSC performance is lost at the interfaces due to extensive non-radiative recombination. In this direction, a Lithium Fluoride buffer layer showed promising passivation effect at the PSK/ETL interface and could be the next step towards optimization.

INTRODUCTION

Motivation

In modern society, humans are dependent on energy harvest and conversion for almost everything. Fossil fuels have led to the advancement of many industries and technology but are not a viable option for the future. A transition to sustainable energy is much needed as we see an increase in energy demand with the continuous rise in population worldwide. It is believed that tackling this 'energy problem' is the most pressing challenge that mankind faces in the near future. In addition to the increasing population, the living standards of many countries is also improving which means higher energy demand in the future. The atmospheric content of CO_2 has been increasing over the past several years and we can already feel the impacts of the resultant climate change. Amongst all these issues, the good news is that the sun provides more energy to the earth per day than the world consumes per year. However, there are roadblocks to effectively harnessing this energy. A lot of work has paved the way to achieve more efficient and cheap photovoltaic (PV) technologies like Cadmium Telluride, Crystalline Si, GaAs etc, thereby enabling wider spread adoption of the technology. A major milestone was recently achieved: March 15, 2022 marked 1 TW of PV installed worldwide [20]. Additionally, in 2011 the Solar Energy Technologies Office (SETO) launched the SunShot initiative [1] with a goal to get solar electricity costs competitive with conventionally generated electricity without subsidies. Since then, there has been a lot of progress and the goals have been increased to get the Levelized Cost of Electricity (LCOE) of Solar PV reduced by 50% to 0.03 per kWh for utility scale.

Recently Perovskites, namely any chemical that crystalizes in the structure shown in Fig A, have gained a lot attention in the PV industry. They have a chemical formula of ABX_3 where A is a monovalent cation, B is a divalent cation, and X is an anion that bonds to both. This

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compositional flexibility gives rise to many different Perovskite compositions with wide ranging opto-electronic properties. Additionally, they have sharp optical absorption, tunable bandgaps, high charge carrier mobilities and lifetimes and have potential to be cheaper than the existing technologies that currently dominate the market (like Silicon, CdTe etc). Primary challenges that Perovskite Solar Cells (PSC) faces include [2]:

Methyl ammonium lead triiodide (CH₃NH₃)PbI₃, or MAPbI₃, is one of the perovskites we are exploring.
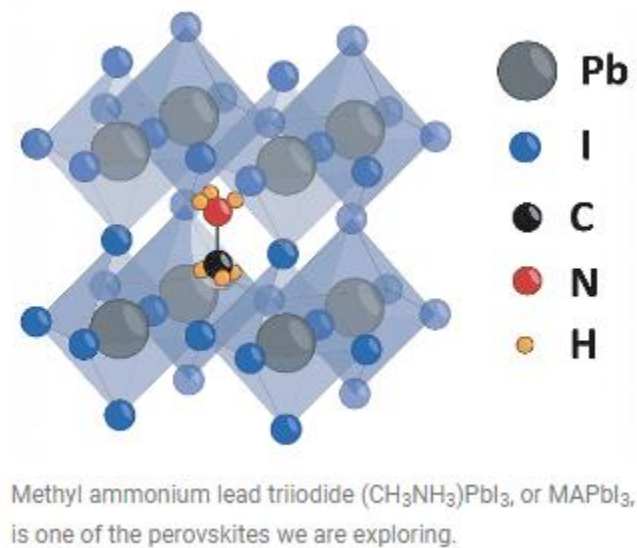
Figure A: Perovskite ABX3 crystal structure [2]

- Stability: Perovskites degrade on exposure to moisture/oxygen or prolonged exposure to light, heat, or/and applied bias

- Durability: Perovskites have limited operational lifetimes

- Scale: Perovskites have seen remarkable progress in small area cell efficiency, but large-area modules still lag behind

- Manufacturability: Perovskite fabrication process need increased scale and improved reproducibility for market penetration

CHAPTER 1

Photovoltaics Fundamentals

1.1 Bandgap

Solids can be classified into three main groups based on their electronic behavior: conductors, insulators, and semiconductors. The valence band (VB) and conduction band (CB) describe the allowed energy states that electrons can occupy in a solid. The VB consists of the atom's outermost electrons and the CB, which consists of higher energy states. The forbidden region between the VB and CB is called the Bandgap (E_g) and is the minimum energy required to excite an electron from a bound state in the VB to free state in the CB.
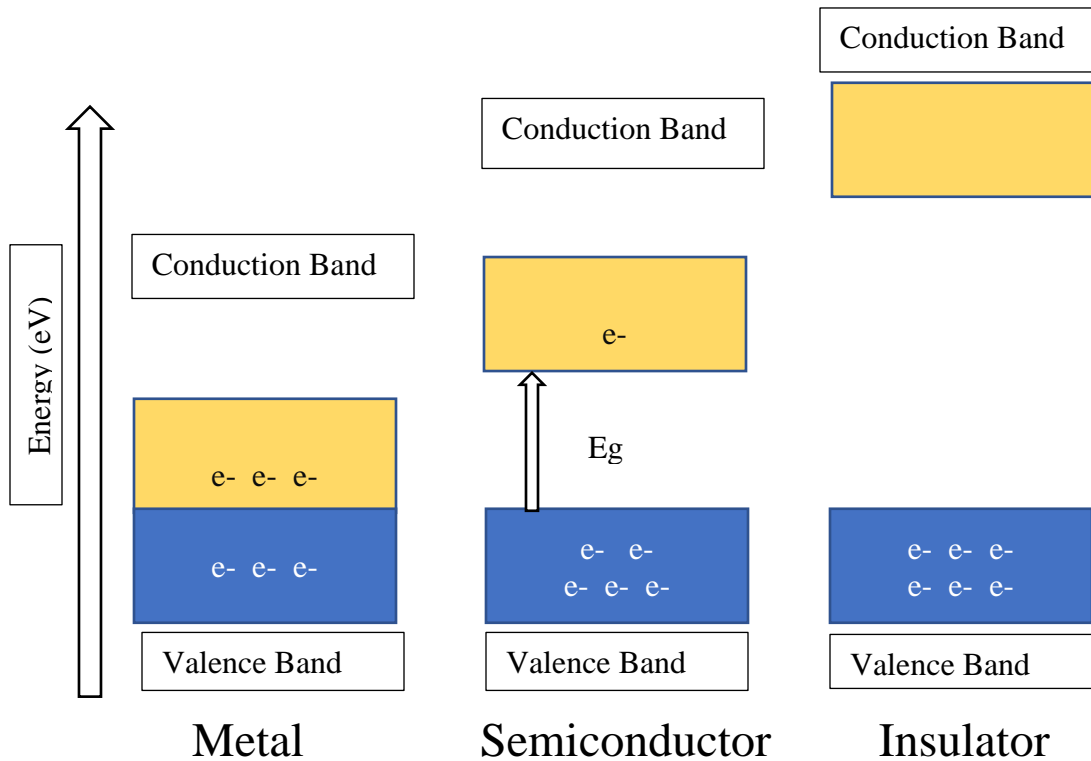
Figure 1.1 Illustration of bandgap for metals, semiconductor and insulators

1.2 Charge carriers

When a semiconductor is excited with energy higher than the bandgap, electrons are excited from the VB to the CB, where they become free and available for conduction. This creates an electron vacancy in the VB called a hole. While these holes are not real particles, they are typically considered as quasi-particles for conceptualization and to calculate interaction with electrons and the crystal's incomplete lattice. They have a positive elementary charge, an effective mass, and participate in conduction. Together with electrons, they form the charge carriers in semiconductors [3].

1.3 Carrier Concentration

Operation of any semiconductor device depends on the concentration of charge carriers and hence transport of electrical currents. In order to determine the carrier concentration, two things must be known: 1) the density of allowed energy states (DOS) of electrons g(E), and 2) the occupation function f(E). The DOS function describes the number of allowed states per unit energy and volume. The occupation function is the famous Fermi-Dirac distribution function that describes the ratio of states filled with an electron to total allowed states at a given energy. The following two equations [3] can be used to calculate DOS in the CB and VB respectively excluding the forbidden region i.e., the bandgap E_g.

$$g_c(E) = \left(\frac{4\sqrt{2}\pi m_n^*}{h^3} \right)^{\frac{3}{2}} \sqrt{E - E_C}, \qquad \boxed{\text{For } E \geq E_C} \qquad (1)$$

$$g_v(E) = \left(\frac{4\sqrt{2}\pi m_p^* t}{h^3} \right)^{\frac{3}{2}} \sqrt{E - E_V}, \qquad \boxed{\text{For } E \leq E_V} \qquad (2)$$

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Where m_n^* and m_p^* are effective masses of hole and electron respectively. This assumes that the band edges are parabolic in shape (known as Parabolic Band Approximation) and the curvature of the bands is inversely proportional to the effective mass of electrons (high dispersion curve → low effective mass → fast conduction of electrons). This mass takes account of a periodic force into account as the charges traverse the crystal. The Fermi-Dirac distribution function is given by [3]:

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)}, \tag{3}$$

Both electrons and holes are responsible for conduction. The total concentration of electrons in the CB (n) and holes in VB (p) can be calculated by integrating the product of DOS function g(E) and F(E) across the whole energy band [3].

$$n = \int_{E_C}^{E_{top}} g_c(E) f(E) \, dE, \tag{4}$$

$$p = \int_{E_{bottom}}^{E_V} g_v(E) \left[1 - f(E)\right] dE, \tag{5}$$

$$n = N_C \exp\left(\frac{E_F - E_C}{kT}\right) \quad \text{for} \quad E_C - E_F \geq 3kT, \tag{6}$$

$$p = N_V \exp\left(\frac{E_V - E_F}{kT}\right) \quad \text{for} \quad E_F - E_V \geq 3kT, \tag{7}$$

Where N_c and N_v are the effective densities of the CB and VB states respectively.

1.3.1 Intrinsic and Extrinsic Semiconductors

For an intrinsic semiconductor at equilibrium at 0 K, the number of electrons is equal to the number of holes. Multiplying equation (6) and (7), we can calculate the Fermi Energy as in equation (8) [3] below:

$$E_{Fi} = \frac{E_C + E_V}{2} + \frac{kT}{2} \ln \left(\frac{N_V}{N_C} \right) \tag{8}$$

At 0 K, it is evident from equation (8) that Fermi energy lies in the middle of the bandgap for intrinsic semiconductors.

In the case of extrinsic semiconductors, the concentration of electrons and holes can be manipulated by doping or can arise naturally due to crystal defects. Based on the type of majority charge carrier, semiconductors can be classified as either n-type or p-type. N-type materials are made by adding donor atoms into its crystal structure (e.g. P for Si). These donor atoms donate extra electrons to the lattice which become part of the delocalized electron population while the atom itself becomes ionized (positively charged) fixed center. Typically, the extra electrons do not truly lie in the CB but if the donor level is near enough to the CB than at room temperature (eg. In case of P), they are fully ionized. Doping introduces allowed energy states in the bandgap region close to the CB. This raises the Fermi energy. Similarly, introducing acceptor atoms (e.g. B for Si) increases hole concentration as they accept electrons from the crystal lattice and make it p-type. This would lower the fermi energy closer to the VB.

1.4 Working Principle of a Solar Cell

Solar cells work on the principle of Photovoltaic effect i.e., generation of current and voltage. This process can be broken down into three steps as shown in Fig 1.2. These steps include

1) generation of charge carrier due to absorption of photons, 2) separation of carriers by a built-in electric field, and 3) collection of the charge carriers. The main absorber layer serves the purpose of absorbing photons. When an incoming photon has energy equal to or greater than the semiconductors band gap, an electron gets excited from VB to CB. However, this electron in the CB has a limited lifetime and tends to either fall back to VB and recombine with a hole, leading to release of energy as a photon (Radiative Recombination), transfer energy to other electrons/holes or lattice vibrations (Non-radiative Recombination). To prevent this recombination and instead harness the charge carriers, there is a need for suitably doped (n- and p-type) semi-permeable membranes on both sides of the absorber such that they can selectively extract electrons from one side and holes from the other.
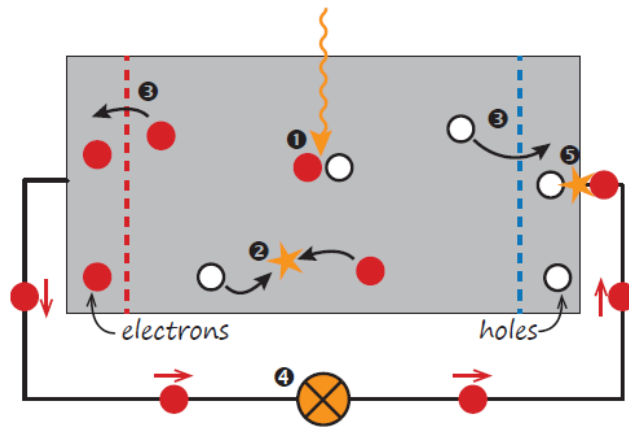
Figure 1.2 Schematic of working principle of solar cells [3]

1.5 AM1.5 Reference Solar Spectrum

Approximated as a perfect black body, the sun would be expected to emit a spectrum as shown by the black curve in Fig 1.3. However, as light travels across space various elements absorb and scatter (Rayleigh Scattering) light, causing losses which result in lower intensity and various absorption lines. At the edge of our orbit, AM0 (blue line in Fig 1.3) remains. Once the solar

radiation passes through the Earth's atmosphere, it gets attenuated substantially more due to the atmosphere. The degree of this attenuation is highly dependent on latitude as well as atmospheric conditions. In order to have a standard spectrum for PV testing, AM1.5 spectrum having an intensity of 1000 W/m^2 was adopted as the reference solar spectrum by the industry [3][4].

1.6 Current-Voltage (JV) Characteristics

Measurement of the current-voltage response of a solar cell under illumination is one way of extracting some of the most important metrics of a solar cell performance. For this measurement, the cell is illuminated with a simulated solar spectrum and the resulting current is measured as the voltage is swept across an appropriate range.
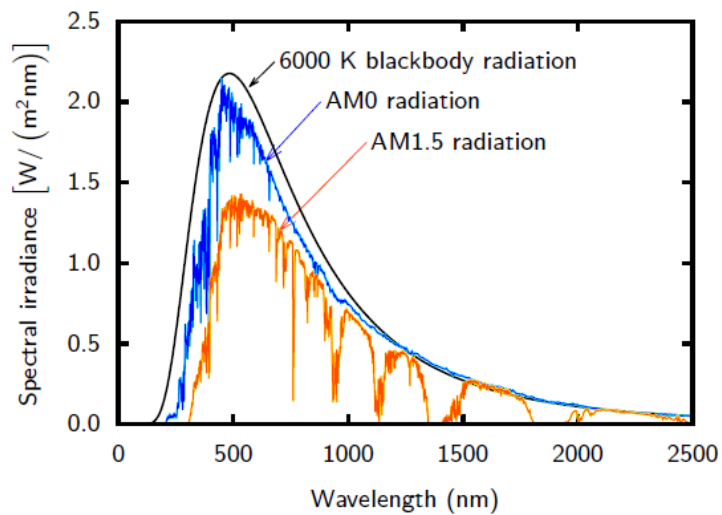
Figure 1.3 Spectral Radiance of AM0 and AM1.5 Solar Spectrum [3]

Fig 1.4 depicts a typical JV characteristic curve. This curve can be analyzed to extract performance metrics which tell us how efficiently the device is in converting solar to electricity. These parameters are discussed in the next several subsections.

1.6.1 Open Circuit Voltage (V_{oc})

The maximum possible voltage that can be generated from a device is its open circuit voltage. At this voltage, there is zero current flowing though the circuit.

1.6.2 Short Circuit Current Density (J_{sc})

The maximum current that a solar cell can deliver is related to its short circuit current density. It strongly depends on the optical properties of the absorber like absorption and reflection losses.

1.6.3 Fill Factor (FF)

Both V_{oc} and J_{sc} represent a state of device with no power delivered. FF is a parameter that determines the maximum power delivered. It is the ratio of the cells' Maximum Power Point (MPP) to the product of J_{sc} and V_{oc}. This determines how close the device is to ideal behaviour.

1.6.4 Power Conversion Efficiency (PCE)

PCE is the ratio of power output from a device to the power input from the sun and can be used to evaluate how efficient the device is in converting incident light into electricity. This metric can be used to cross compare solar cells and is calculated as following [3]:

$$\eta = \frac{P_{max}}{P_{in}} = \frac{J_{mp} V_{mp}}{P_{in}} = \frac{J_{sc} V_{oc} FF}{P_{in}}.$$

For standard AM1.5 spectrum, $P_{in} = 1000$ W/m^2.

1.6.5 Shunt (R_{sh}) and Series Resistance (R_s)

A shunt is an alternate low resistance pathway in the device that can emerge mostly due to manufacturing defects. This leads to losses in current and voltage. Additionally, high series resistance indicates a barrier to electron transport hindering current extraction in solar cells. Losses due to series resistance mainly occur due to energetic barrier at an interface or bulk resistance within the material. An ideal solar cell would have infinite R_{sh} and zero R_s.
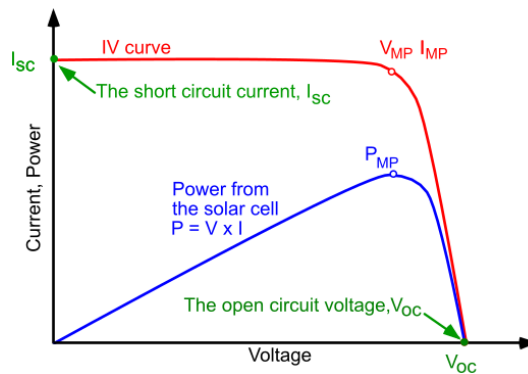
Figure 1.4 Typical JV characteristics curve [4]

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CHAPTER 2

Electron Transport Layer for Perovskite Solar Cells

2.1 Introduction

Typically, PSC are thin film systems in which a perovskite absorber layer is sandwiched between n-type and p-type doped contacts called the ETL and HTL, respectively. Depending on which contact layer is on the illumination side, they are categorized into n-i-p (HTL on top) and p-i-n (ETL on top) architecture. The front contact is typically a Transparent Conducting Oxide (TCO) like ITO or FTO sputtered on glass. The back contact is thermally evaporated metal like Gold or Silver.
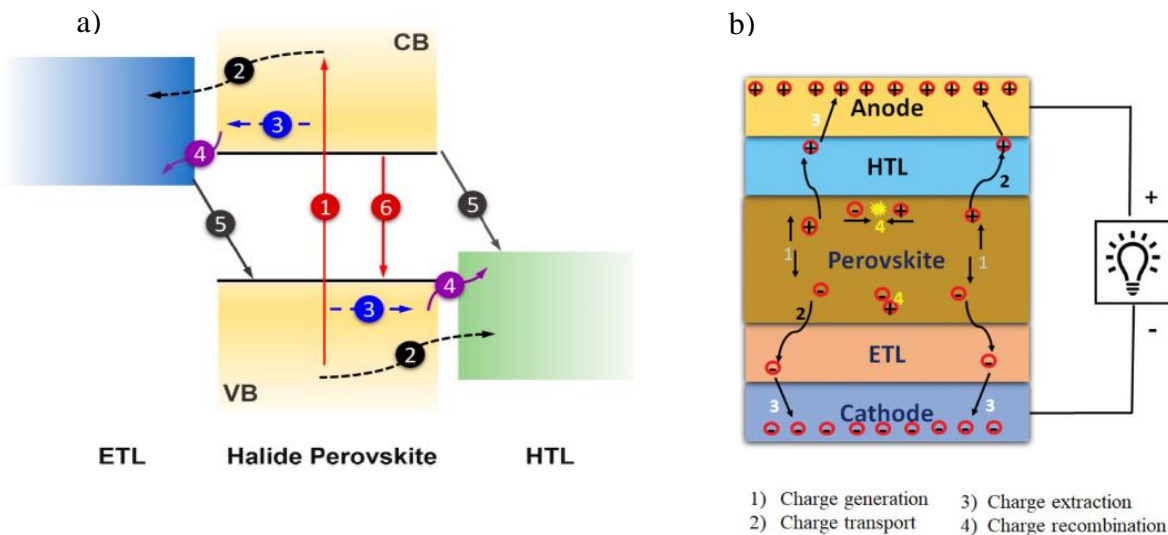
Figure 2.1 a) Schematic of carrier dynamics in PSC on illumination (1)carrier excitation (2)hot carrier cooling and extraction (3)diffusion of carrier from bulk to interface (4)charge transfer from interface to ETL and HTL (5)charge trapping in defect and backward charge recombination (6)band-to-band recombination; b)Working principle of PSC [5]

Fig 2.1 illustrates the working mechanism of a PSC. Incident photons excite electrons from the VB to the CB. Carriers with energy greater than the bandgap quickly thermalize to the band edge where they diffuse to the interface for extraction. In this process, some charges tend to get lost in the traps/defect states at the interface or they non-radiatively recombine through backward

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charge transfer. Additionally, if the lifetime of the free carriers in CB is too short, they end up falling back to VB and are lost through radiative recombination.

2.2 C60 as ETL

Buckminsterfullerene, also known as C60 is a spherical carbon allotrope with 60 carbon atoms arranged in hexagons and pentagons. It is widely used in organic PV devices as an ETL owing to its excellent electron mobilities and electron affinities. Its cage-like structure and polyaromaticity enable formation of displaced electron cloud that justify its electron selective nature. Since the CB of C60 aligns well with almost all PSK systems, it is very common in p-i-n PSC whereas in n-i-p configuration, its spin-coated counterpart PCBM is used. Additionally, its spherical shape facilitates good vertical charge transport regardless of the processing conditions.
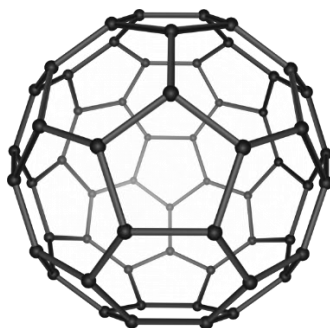
Figure 2.2 Cage-like structure of C60

Liu. Et al. [9] were able to show that an ultrathin 1 nm C60 can extract electrons from the PSK while reducing space charge accumulation at the interface, thereby suppressing photocurrent hysteresis. With ~ 1 nm thick C60, devices achieved a PCE of 18.2% with negligible hysteresis even though the C60 film had incomplete coverage. In contrast, devices with no C60 barely worked and even a 1 nm monolayer of C60 was sufficient to turn on the device. Although the

best devices had 20 nm thick C60 due to complete coverage whereas in 1 nm C60 based devices, incomplete coverage leads to a reduced effective mobility and hence less efficient electron transport. A thicker C60 shortened carrier lifetime and enhances charge extraction.

2.3 Non-radiative Recombination

Even the best performing p-i-n devices are limited by the PSK/ETL interface. Fig 2.3 [8] summarizes almost all the PSK systems and their Photoluminescent Quantum Yield (PLQY) values under 1 sun for the bare PSK, PSK/C60 and full devices stack. Irrespective of the bandgap, there is a 1-3 order of magnitude difference in PLQY from the addition of the C60 layer. This indicates severe quasi-Fermi level clamping, which will negatively affect open circuit voltage.
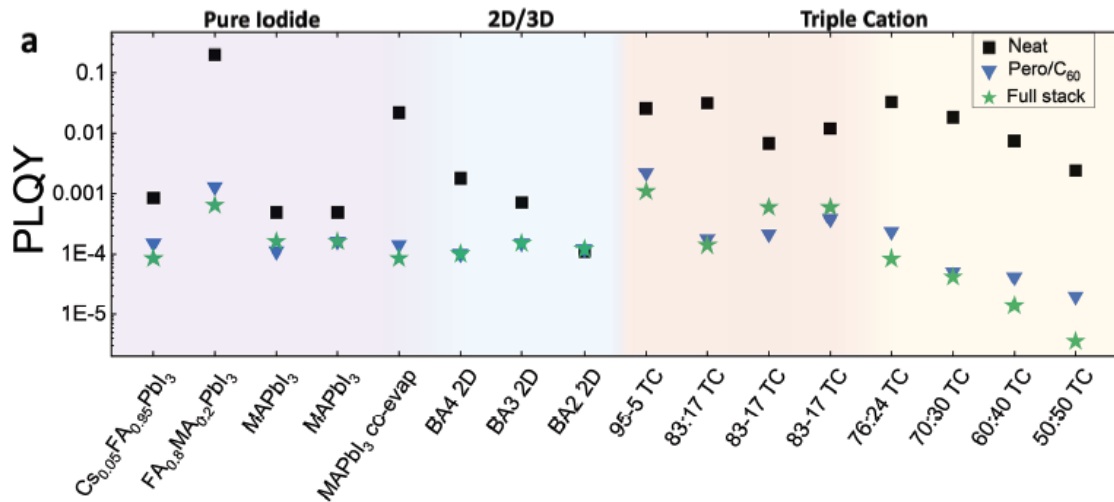
Figure 2.3 C60-induced recombination losses in different PSK systems, triple cation perovskite $(Cs_{0.05}FA_xMA_yPb(I_xBr_y)_3)$ is abbreviated as "TC," where the $x{:}y$ ratio reflects the molar ratio of $FAPbI_3$ versus $MAPbBr_3$ [8]

With an extensive set of EQE measurements, Warby, J. et al [8] were able to show that thermal evaporation of C60 atop PSK introduces a number of sub-gap states into the PSC that predominately form in the first nm itself. This is where most of the critical losses in device

performance occur. The traps originate either from the LUMO of C60 pinning down below the CB

of the PSK, giving rise to large DOS at the interface, or from the charge transfer states.

Additionally, the C60/Metal contact interface acts as a region of intense recombination too.

On thermally evaporating Ag directly on C60, the metal can penetrate into the C60, creating a

Schottky barrier for electron transport [10]. Hence there is a need for an additional buffer layer at

this interface. Addition of BCP layer (Fig 2.4 a) at the C60/Ag interface changes it from a Schottky

contact to an Ohmic contact by reacting with the Ag to form a BCP-Ag complex that has good

alignment with that of C60, as shown in Fig 2.4 b) and c), thereby enhancing charge collection [11].
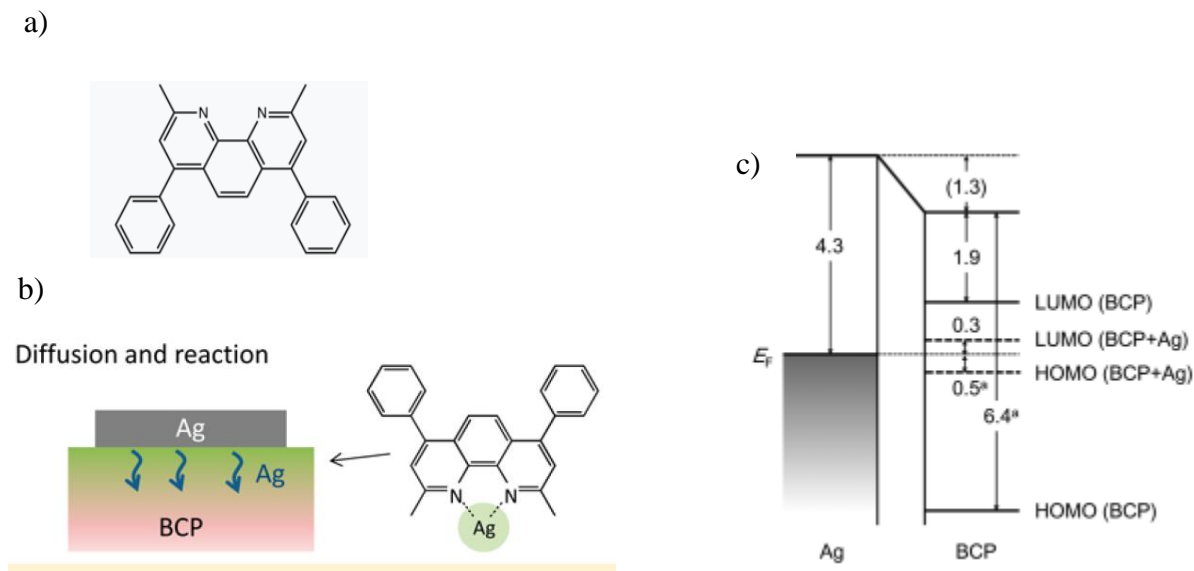
Figure 2.4 a) BCP: 2,9-Dimethyl-4,7-diphenyl-1,10-phenanthroline; b) schematic showing diffusion and reaction of Ag with BCP; c) Energy level diagram of Ag/BCP interface [11]

2.4 Towards scalable processing of PSC: Physical Vapor Deposition (PVD)

Most of the high-efficiency PSC reported in the field are solution processed at a research

lab-scale. For Perovskites to invade the PV market and show their full potential, they need to show

compatibility with industrial manufacturing techniques. Herein, we develop PVD processes for

ETLs to establish a baseline for our p-i-n devices. The advantages of thermally evaporated ETLs

in devices are excellent thickness control, better reproducibility, and low temperature processing (crucial to the fact that the films are to be deposited on top of PSK). Additionally, PVD enables pinhole free, uniformly deposited films without involving any toxic solvents.

2.4.1 Vacuum Thermal Evaporation

During thermal evaporation, material is resistively heated on a refractory metal-based (Tungsten, Molybdenum, Tantalum etc.) evaporation boat in a high vacuum environment. When it starts to vaporize, the vapor stream travels to the surface of the substrate where it condenses to form a thin film. High vacuum (<1E-8 mbar) reduces collision of the material vapors with other molecules in the chamber environment. Substrates are rotated at a fixed rotation speed to maintain homogeneity of films. A deposition rate sensor with a gold coated crystal oscillator (quartz crystal monitor) is placed near the substrate holder to monitor the rate of deposition and thickness. Z factor which converts the quartz crystal monitors vibrational frequency to the respective material's deposition rate. For materials whose Z factor values are not available, it is typically assumed as 1.
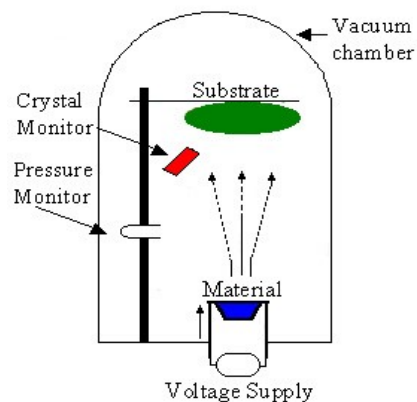
Figure 2.5 Basic set-up for thermal evaporation [12]

CHAPTER 3

Experimental (Baseline)

3.1 Photovoltaic Device Fabrication

3.1.1 Substrate Preparation

Pre-etched Indium Tin Oxide (ITO) substrates were used as substrates. Prior to fabrication, they were cleaned by a series of washing and sonication steps as follows: sonicate in 2 vol% Hellmanex III in DI water for 15min, rinse with DI water, sonicate in DI water for 15 min, sonicate in Ethanol for 15 min, rinse with water, sonicate in Acetone for 15 min, rinse with water, sonicate in IPA for 15 min, rinse with water and then blow dry. The substrates were then UVO treated for 30 min and then moved to PASCAL (Perovskite Automated Solar Cell Assembly Line) for automated or hand-spin coated HTL and Perovskite deposition.

3.1.2 HTL and Perovskite deposition (Half Stack)

A 0.6 mg/mL (1.8 mM) solution of MeO-2PACz in dry EtOH was dropped onto the substrate, let it sit for 5 s, spun at 3000 rpm with 500 rpm/s ramp for 30 s, and then annealed at 100 C for 10 mins. For wide bandgap devices, a triple halide triple cation wide bandgap PSK $Cs_{0.22}MA_{0.03}FA_{0.75}Pb_{1.010}I_{2.48}Br_{0.446}Cl_{0.0877}$ was dissolved in 3:1 volume:volume DMF:DMSO, spun coat, and annealing at 100 C for 10 mins. For $FAPbI_3$ based devices, a 1.33 M solution of $FAPbI_3$ was dissolved in 2-Methoxyethanol, added to 0.2 M of MACl and 7.5 volume % NMP, spun coat at 8000 rpm with 2000 rpm/s ramp for 30 s, and annealed at 150 C for 10 mins.

3.1.3 ETL and Top Metal Contact deposition by Thermal Evaporation

The vacuum chamber was pumped down to high vacuum levels (<1E-8 mbar). Alumina crucibles were used as the evaporation source and the low-temp thermal evaporation source was ramped up to 350 C and 150 C for C60 (Lumtec) and BCP (TCI) respectively to achieve a suitable rate of deposition (0.1 A/s for both). Temperature was incremented by 50 C every 5 mins until some rate was registered on the QCM after which it was ramped 5 C every 5 min until desired rate of deposition was achieved. Lastly, 100 nm of Silver (Kurt J. Lesker) was evaporated (0.5 A/s for first 0.5 nm of adhesion layer followed by 2 A/s for the remaining thickness) in a tungsten boat and using a shadow mask. Quartz Crystal Microbalance (QCM) sensors were used to monitor the rate of deposition and thickness deposited. The substrate holder was rotated continuously at a fixed speed (10-12 rpm) to ensure homogeneity of films. Dektak surface profilometry was used to measure the actual thickness and calibrate the tooling factor for each of the materials.

a)

Figure 3.1 a) schematic of baseline p-i-n device architecture [13]; b) picture of final devices
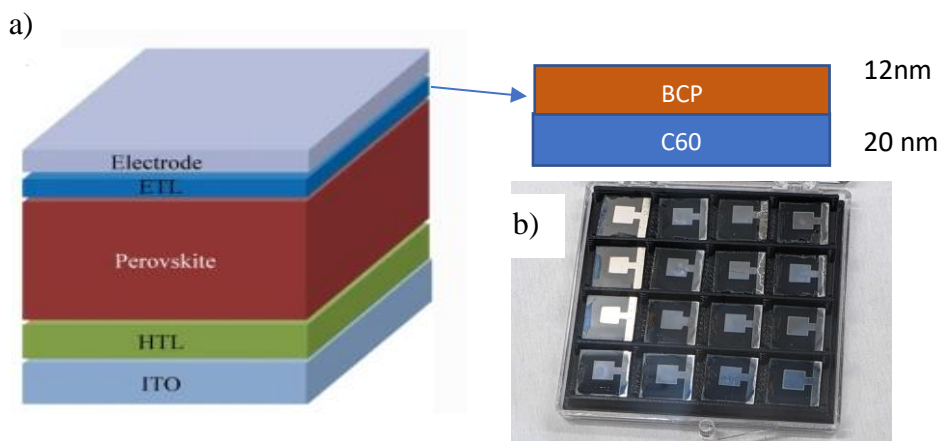
3.2 Characterization

3.2.1 Current-Voltage (JV) Measurements

After device fabrication was completed, the cells were tested inside Nitrogen environment. Solar cell performance was measured by sweeping the voltage from −0.1 to 1.2 V at a scan rate of

50 mV/s using a Keithley, with cells under an irradiance of 100 mW/cm^2 using an ABET Mondel 11002 SunLite solar simulator from a 150 W Xe short-arc lamp filtered to better match AM 1.5G. Spectral intensity was calibrated for each set of measurements using a silicon reference cell with a KG5 filter. The Ag and TCO sections were contacted via microprobes to ensure non-damaging device contact. The defined active area tested on each device was 0.07 cm^2, determined by an aperture mask.

3.2.2 Ellipsometry

Tooling factor calibration was done for each of the PVD processed materials. A J.A. Woollam M-2000D Ellipsometer at the UC San Diego Nano3 facility was used to measure the actual thickness of the films. These films were deposited on polished Silicon wafer for characterization. This technique measures the change in polarization of light as it gets reflected from or transmitted through a sample. This change in polarization depends on the material's complex dielectric function and dispersion index. Data acquisition and model fitting was done with CompleteEASE software to generate thickness and mean square error results. Tooling factor is the ratio of actual thickness of films to the thickness registered by QCM sensors. Lastly, a linear equation is fitted to the calibration curve (S1 and S2) to extract Tooling factor.

3.2.3 Scanning Electron Microscopy (SEM)

SEM images were taken on a Zeiss Sigma 500 SEM in Nano3 and Apreo FESEM in the UC San Diego NanoEngineering Materials Research Center.

3.3 Results and Discussion

Fig 3.2 a) and b) report the first pass results for device performance of two iterations of the same experiment. The half stacks (ITO/OMeO-2PACz/WBG PSK) for both the iterations were made on the same PASCAL run but split into two runs for ETL deposition keeping all conditions same. In Fig 3.2 a), we observe a lot of performance variation, notably in J_{sc} ranging from 9 mA/cm^2 to 17 mA/cm^2. Iteration 2 showed a tighter distribution in J_{sc} and a better yield. There seems to be a lot of intra batch variation (from PASCAL) and/or batch-to-batch variation (from evaporator). Additionally, the overall device yield was low and we suspect it to be due to shunting. A potential cause of many devices being totally shunted could be rooted in the way C60 and BCP films get deposited. This experiment was insightful in indicating the possibility of non-uniform evaporation of the layers (C60 and/or BCP) causing Ag contact to directly come in contact with the Perovskite and cause shunting.
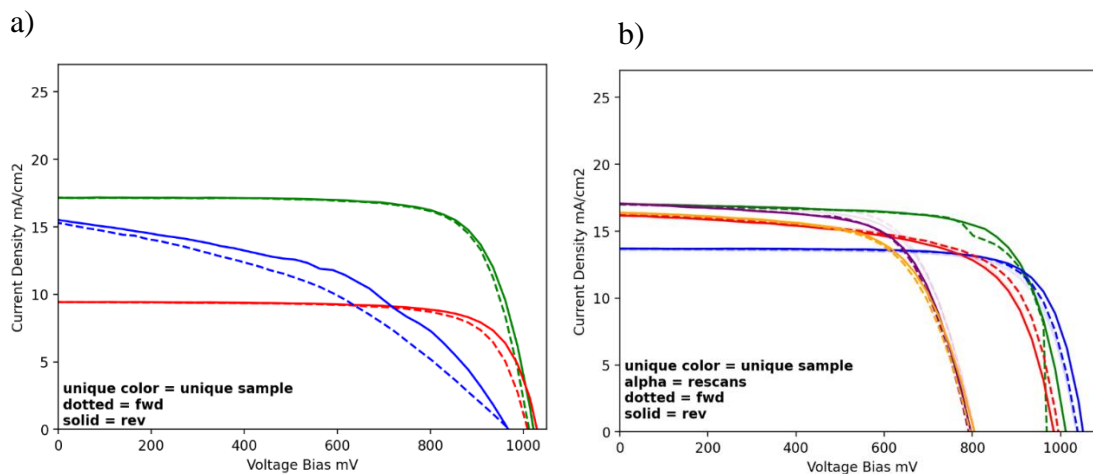
Figure 3.2 J-V sweeps for Iteration a) 1 and b) 2

SEM micrographs of device cross-sections in Fig 3.3 a) show Ag chipping off from a certain region on the device. This confirms our initial suspicion of inconsistency in the coverage of the ETLs.

The morphology of thermally evaporated films is mainly affected by the substrate/underlying layer and the rate of deposition. Therefore, C60 is typically evaporated at a slow and stable rate of 0.1-0.2 A/s onto the Perovskite.

a)   b)
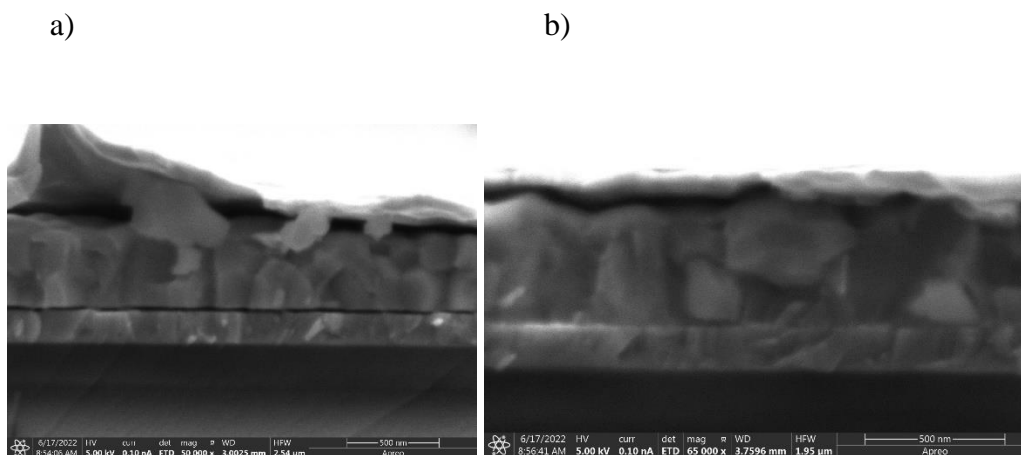
Figure 3.3 Cross-sectional SEM images of two different regions of the same device

Fig 3.4 a) and b) show a cross-sectional SEM of a thermally evaporated C60 onto polished Silicon wafer. This kind of a bumpy morphology seems to be due to spitting which is a very common phenomenon in thermal evaporation processes. The top part of the material inside the crucibles is exposed and as and when each particle gains sufficient energy during ramping up of the source, they sublimate to get deposited on the substrate. These spit particles solidify on the substrate and get embedded. This would explain the bumps observed in the SEM images and would affect the morphology of the next layer i.e., BCP as well. BCP layer would not be as conformal as it should be.

a)   b)   c)
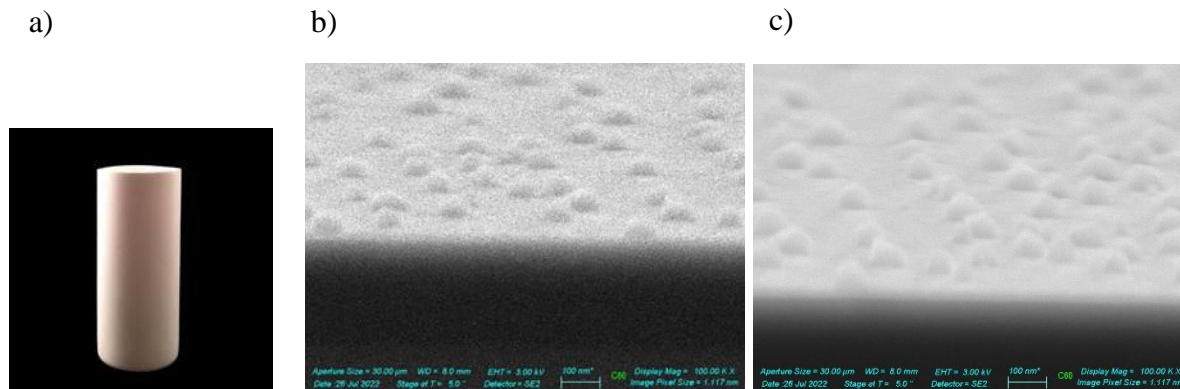
Figure 3.4 a) Alumina Crucible [19] b,c) SEM images of C60 deposited on polished Si wafer

3.4 Changing the evaporation source to Tantalum Box

In order to solve the issue of spitting as mentioned in section 3.2, we shifted to the use of tantalum boxes (Fig 3.5) for evaporating the ETL stack. Baffles tend to minimize the particulates in the vapor stream. For these boats, precursor is loaded into the side slots. On resistively heating the box, vapor stream develops on the side slots and travels to the mid portion before escaping out through the baffles. This controlled method of evaporation enables a stable rate and avoids spit.

3.4.1 Automating Recipe

We performed 3 manual runs by filling up fresh precursor each time to establish Pre-conditioning steps i.e. consistent Ramp Power, Time and Soak time across all the runs. Power is incremented by 0.5 % in intervals of 30 sec (depending on the thermal budget of the material) until the first pressure spike is noted i.e., chamber pressure suddenly increases from <1E-8 mbar to 1E-7 to 1E-6 mbar levels. This spike is an indicator of the material outgassing and we want to get rid of such spikes so that a stable deposition rate can be achieved. After the chamber pumps back to <1E-8 mbar, we increased the power again by 0.5 % every 30 sec until second pressure spike. After this, when we increase power to the electrodes, a stable rate of deposition was noted which marks the beginning of deposition phase. Fig 3.6 a) and b) represents a plot of the Pre-conditioning

settings for C60 and BCP respectively. After establishing pre-conditioning and PID parameters, we tuned these settings into the controller and ran automated depositions. We noted that color of C60 in the boat after evaporation changed to light brown from its original black-brown color indicating thermal degradation. In order to minimize the extent of thermal degradation, the preconditioning step of C60 was kept as short as possible.
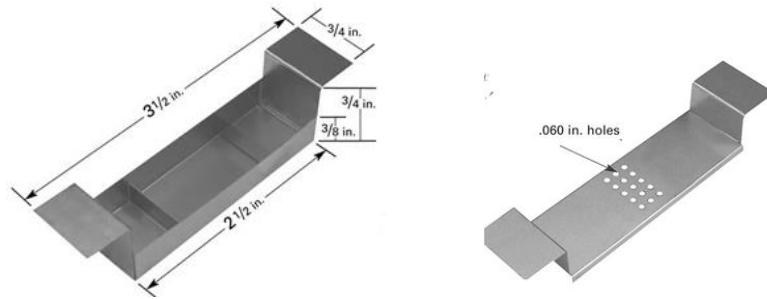
Figure 3.5 Tantalum Box Boats [21]
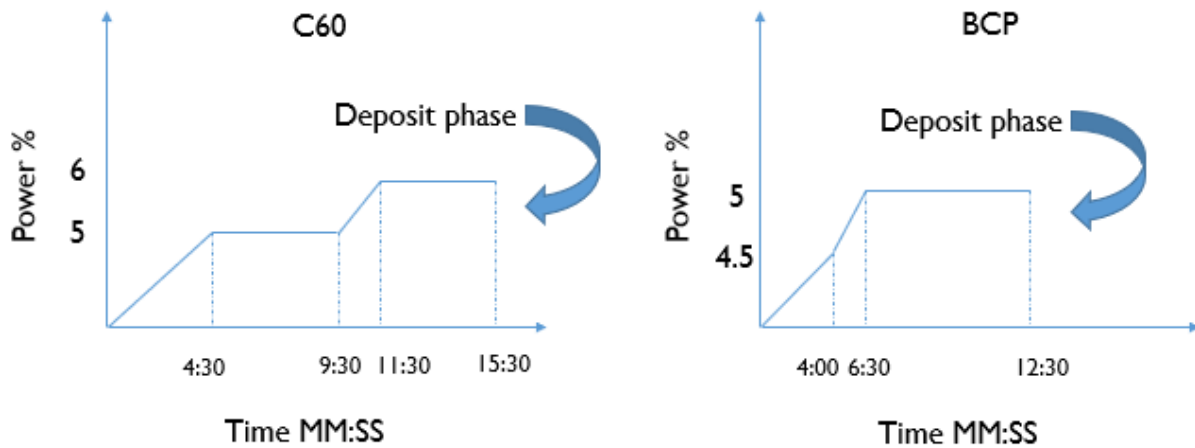
Figure 3.6 Pre-conditioning Steps for C60 and BCP evaporation recipes

3.5 Results and Discussion

We fabricated a batch of devices and tested the automated processes for ETL depositions. Fig 3.7 contains the JV sweeps and the box plot analysis of the device statistics. From the box plot

in Fig 3.7d) we can conclude an apparent improvement in reproducibility which can be attributed to automated deposition on PASCAL coupled with automated ETL evaporations. The next point of interest is the tight distribution of V_{oc} with a mean value of 1.02 V as well as tight spread in J_{sc}. The current density improved a lot from the 15 mA/cm^2 previously to 20 mA/cm^2 for this batch. Average PCE of these cells lies at 15.6 % with a champion being 17.02% efficient (reverse scan). Additionally, the yield drastically improved up to 100 % for this set of devices.
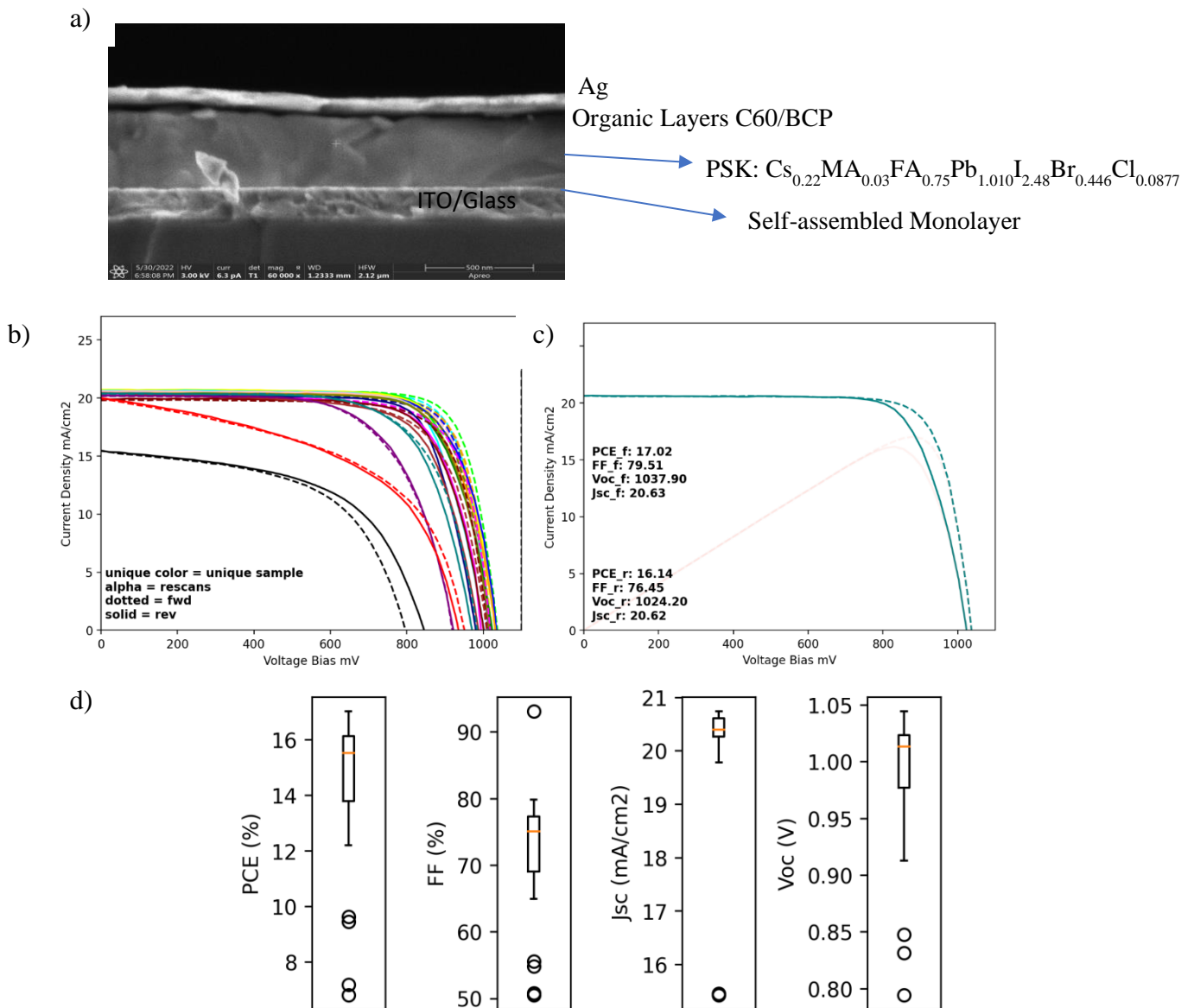
Figure 3.7 a) Cross-sectional SEM image of one of the devices; b) JV sweeps; c) Champion device; d) Batch statistics

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3.5 Conclusion and Future Work

In conclusion, PVD is an effective method to produce large area ETLs. Automated spin coating on PASCAL coupled with evaporated ETL stack enables an assembly line for baseline device optimization. Promising initial experimental results illustrate the potential for PSC optimization through ETL fabrication and characterization. Switching to the tantalum box boats boosted the ETL optimization process a lot. All in all, we can further improve PSCs through transport layer fabrication and interfacial trap recombination mitigation.

CHAPTER 4

Tin Oxide Buffer Layer

4.1 Introduction

4.1.1 Perovskite/Silicon Tandem Solar Cells

With the advent of improved manufacturing techniques and economies of scale, Silicon photovoltaics have seen a significant decrease in manufacturing costs. However, the technology has also reached very close to its detailed balance limit (thermodynamic limit) in terms of power conversion efficiencies. One way to break this single junction limit is to stack multiple absorbers of different bandgaps together to form a multi-junction device [14]. This helps in reducing thermalization losses (cooling off of high energy carriers because they can't be collected) to a great extent. Lately, organic-inorganic lead halide perovskites have emerged as a promising and cheaper top cell alternative for Silicon bottom cells. This is where Monolithic Perovskite/Silicon Tandems come in. Perovskites enable tunability in bandgap as well as offer great optoelectronic properties. They have a sharp optical absorption edge, a reported a high PCE of up to 25.7 %, [2] and an ideal bandgap range of 1.5-1.8 eV for Silicon based tandems. A common challenge faced in the community is related to the fabrication of Perovskite top cell on top of textured Si cells. The purpose of texturing i.e., micrometer sized pyramids on c-Si cells is to increase light trapping in the infrared. General Perovskite fabrication techniques like spin coating have been unable to achieve a conformal coating on the textured substrates as it results in accumulation of c-Si valleys while the pyramids remain bare leading to shunting of the device [14]. Hence, an alternate hybrid deposition approach is being studied. Fig 4.1 illustrates a typical Perovskite-Silicon tandem cell architecture. PVD processing of the ETLs, TCO and the top contact enable low temperature processing steps for the tandems and prevent degradation of the bottom Si cell.

4.1.2 Tin Oxide Buffer Layer

Perovskite-Si tandems require a Transparent Conducting Oxide (TCO) at the top since they are illuminated from the top side. TCOs such as Indium doped Tin Oxide (ITO) and Indium doped Zinc Oxide (IZO) have been widely studied as top electrodes in these configurations. Typically, these layers are deposited via RF sputtering. However, there are some challenges when these have to be sputtered on top Perovskite top cell. Specifically, the high energy of the sputtered atoms, ions, electrons and UV light during sputtering may change the chemical bonding of the Perovskite and the organic layers (C60, BCP) underneath damaging the top cell. Additionally, the sputtering processes may involve a large temperature range and a potential mismatch between the thermal expansion coefficient between TCO and underneath film could cause peeling-off issues [15]. Our typical p-i-n device architecture for Perovskite top cell in single junction configuration is Glass/ITO/MeO-2PACz/PSK/C60/BCP/Ag. Replacing the thermally evaporated Ag electrode with sputtered ITO poses issues as BCP is a soft organic material that suffers from sputter damage. Hence, a more robust inorganic material is required to protect against the sputter damage. Atomic Layer Deposition (ALD) processed Tin Oxide is widely used in this context. Since SnO_x and TCOs of interest (ITO) are both metal oxides, they have a better affinity for each other as opposed to contact between BCP and ITO which is based on Van der Waals forces and is weaker. Liu et al [15] were able to confirm this hypothesis by using a tape test Fig 4.1 b) wherein ITO could be peeled off easily from BCP as compared to SnO_x.

ALD is a much complicated and expensive method of deposition and not very promising from a scalable point of view. Instead, we tried to test PVD SnO_x as a buffer layer for tandems. An ideal buffer layer should be able to protect against sputter damage without impeding charge
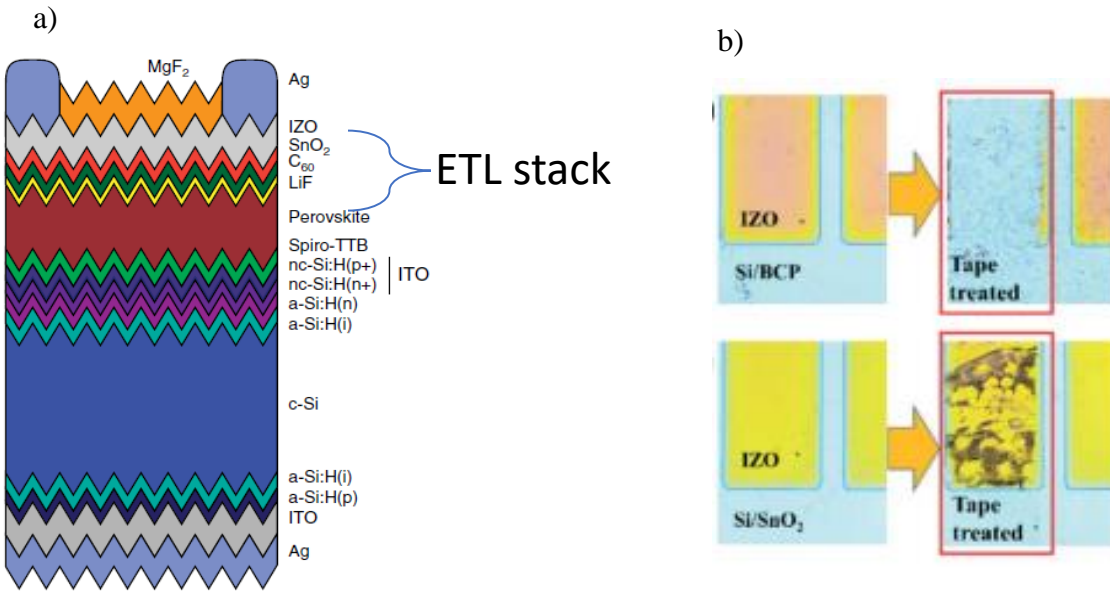
Figure 4.1 a) Device Architecture of PSC on doubly sided textured Silicon [14]; b) Tape Test results from peeling off tape from IZO deposited on BCP and Si respectively [15]

transport in the devices. Hence, we fabricated p-i-n devices with the given configuration: FTO/MeO-2PACz/PSK/C60/SnO$_x$ (10nm)/Ag as a comparison to the baseline p-i-n devices FTO/MeO-2PACz/PSK/C60/BCP/Ag.

4.2 Experimental

SnO$_x$ nanopowder was thermally evaporated in high vacuum (1E-6 mbar) condition from an Alumina-coated Tungsten boat at a rate of 0.1 A/s to deposit a 10 nm (nominal) film. Other layers were processed using the steps indicated in Section 3.1.

4.3 Results and Discussion

Devices with evaporated SnOx and Ag appeared promising. As can be seen in Fig 4.2, both the configurations show comparable performance with the baseline condition being slightly better on average. Additionally, champion devices were slightly better: the champion baseline condition

demonstrated a PCE of 17.02%, a V_{oc} of 1.038 V, J_{sc} of 20.63 mA/cm^2, and a great Fill Factor of 79.5% while the champion for the devices with SnO_x had a PCE of 15.62 % with a V_{oc} 1.02 V, J_{sc} 20.38 mA/cm^2 and a FF of 75.11 %. Both V_{oc} and J_{sc} had a tight distribution for both the conditions. PVD SnO_x has been studied widely as an ETL in n-i-p architectures. However, there is an added processing step which involved annealing it to 200 C. As-deposited films are under-stoichiometric containing variable valence states like Sn^{2+} which can be easily converted to Sn^{4+} by annealing. When used in the inverted configurations, we had to let go of the annealing step in order to protect the Perovskite and the underling organic layers from thermal degradation. Thus, from initial results, the as-deposited SnO_x looks promising in terms of selectivity towards electrons. Next, we fabricated semi-transparent devices to check how protective it is against sputter damage.
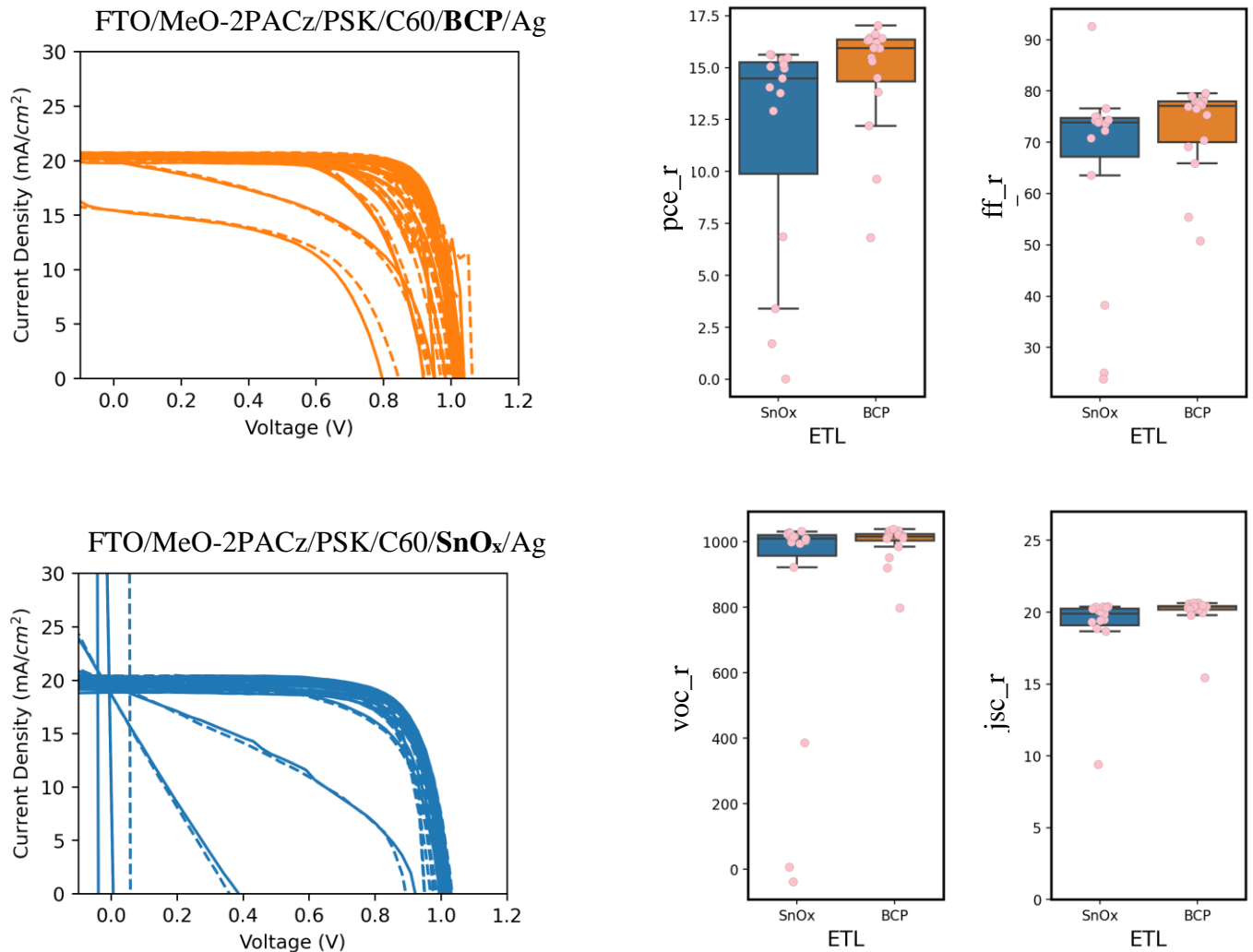
Figure 4.2 JV characteristics and device statistics for baseline and SnO_x buffer layer based devices for comparison

4.4 SnO_x in semi-transparent devices

Three categories of devices were fabricated with a bottom half stack consisting of FTO/MeO-2PACz/PSK and the following ETL stacks:

- C60 (20 nm) / BCP (12 nm) / Ag (100 nm)

- C60 (20 nm) / SnO_x (10 nm) / Ag (100 nm)

- C60 (20 nm) / SnO_x (10 nm) / ITO (100 nm)

4.5 Experimental

ITO was sputtered at a power of 80 W and 60 mTorr pressure under an Argon flow of 8 sccm. The rate of sputtering was maintained at 0.6 A/s with a source-target distance of about 20 cm. Sheet resistance of ITO on glass was measured using a four-point probe.

4.6 Results and Discussion

Sheet resistance of the ITO was found to be 350 ohm/sq. The JV curves and the device statististics are as shown in Fig 4.3 where both the C60/BCP/Ag and C60/SnO$_x$/Ag devices are comparable in performance. However, the semi-transparent ones (C60/SnO$_x$/ITO) have an S-shaped curve with too low shunt and too high series resistance. We note that the yield as well as performance of the control devices (C60/BCP/Ag) was relatively poorer than previous iterations. The half stacks were spin coated by hand and there were obvious surface coverage issues/pinholes on some of them which could be be linked to loss in yield.
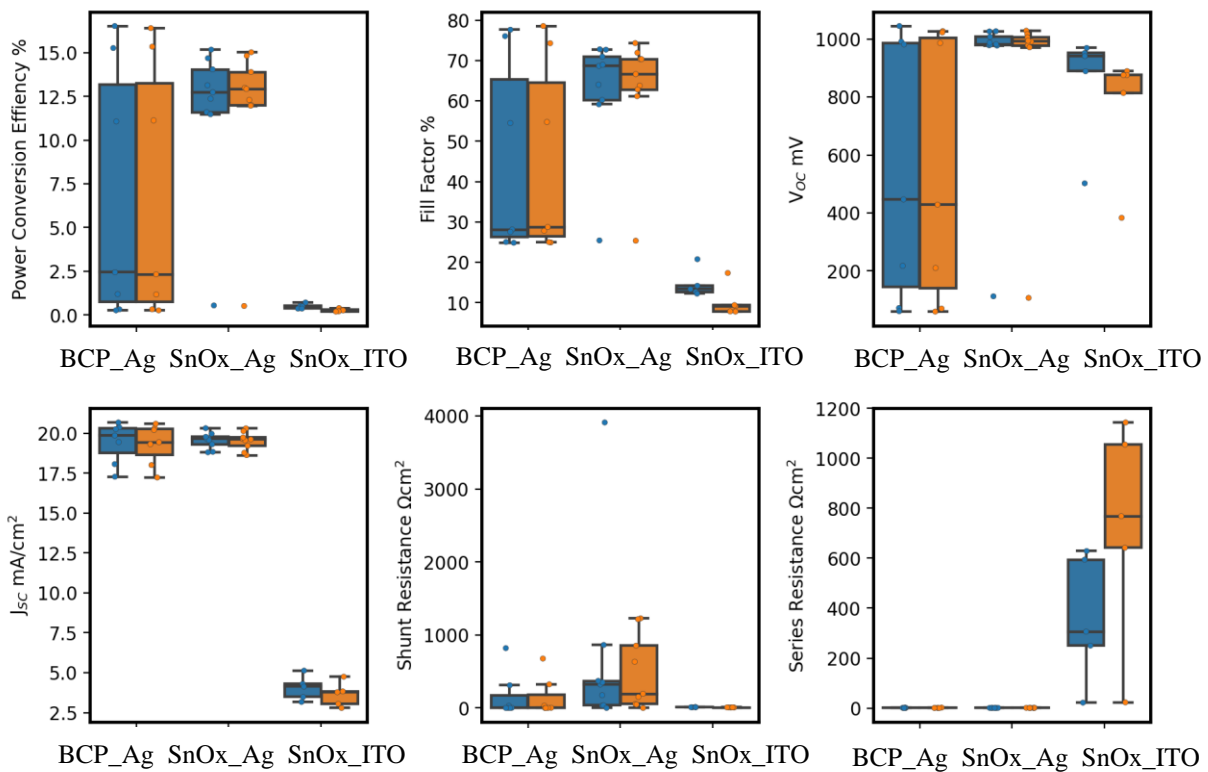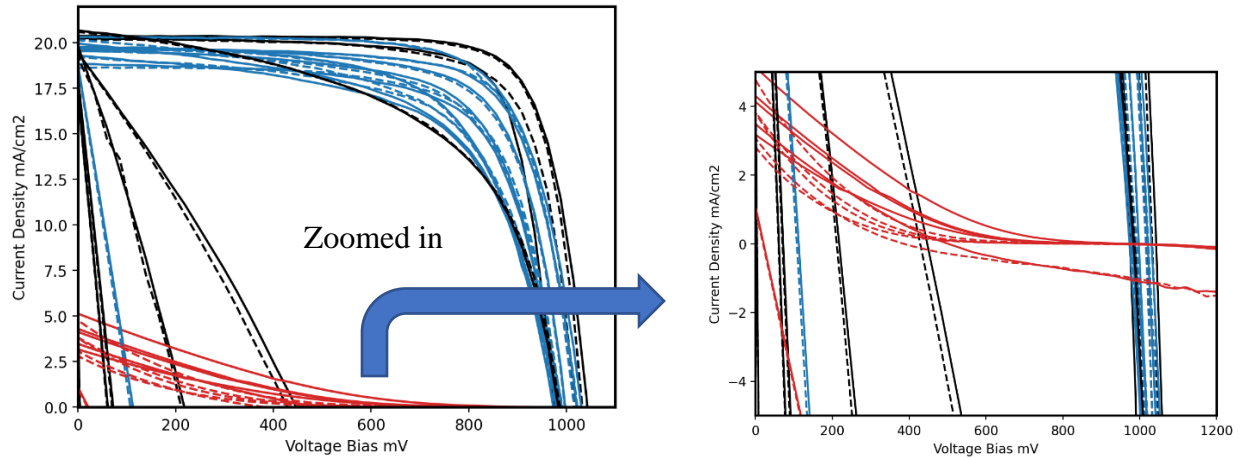
Figure 4.3 JV characteristics and device statistics for BCP/Ag (black), SnO$_x$/Ag (blue)and SnO$_x$/ITO (red) based devices for comparison where orange and blue represent forward and reverse scans respectively.

The origin of this S-shaped behaviour can be attributed to damage caused during ITO sputtering. Next, to see if we could protect the film with a thicker layer, we increased the SnO$_x$ layer thickness by 3 times i.e. 30 nm. At this thickness we observe a double diode in the C60/SnO$_x$/Ag devices, but reasonable Voc, suggesting we are at the upper limit of thickness of device functionailty.

However, even at these thicknesses the ITO-based devices were completely shunted, suggesting insufficent protection. We suspect that the root cause of this failure lies in the deposition condition of SnO_x. Specifically, SnO_x evaporates at about 1000 C at a rate of 0.1 A/s. There is some level of radiative heat transfer by which the substrates tend to get heated up too. As we aim for higher thicknesses at the same rate of deposition, prolonged exposure of the cells to higher temperatures causes a change in surface energetics and potentially work function of the layer too, making it less selective for electron transport. Additionally, a 30 nm thick SnO_x film does not seem to be dense enough to be shielding from oxyiodo species (formed from the interaction of radicalized Oxygen during ITO sputtering and Iodide in PSK layer) penetrating through the SnO_x layer, getting to the surface of PSK, damaging it and shunting the device.

4.7 Conclusion and Future Work

PVD SnO_x is not an adequate buffer layer for application in Perovskite-Silicon tandems. However, the as-deposited SnO_x does show electron-selective nature. There are two paths that can be taken: looking for alternate metal oxide buffer layers like ZnO or using alternate TCOs that are processed using other methods apart from sputtering. Conducting polymers like PEDOT:PSS, ultra-thin film of metals like Ag, Au etc. are some more alternatives to sputtered TCO. Currently we are exploring several of these options as well as a solution processed SnOx layer that may provide more conformal coverage.

CHAPTER 5

Fluoride Interfacial Buffer Layer

5.1 Perovskite/C60 Interface

State of the art p-i-n devices have been able to mitigate non-radiative recombination at the PSK/HTL interface using Self-Assembled Monolayers (SAM) like MeO-2PACz or molecular passivation with NiO_x [18]. However, there is still a large voltage loss at the ETL side caused by significant charge carrier recombination and energy level mismatch at the PSK/C60 interface. A ~1 nm ultrathin MgF_x or LiF layer when inserted at the ETL interface, displaces C60 density of states from the PSK mitigating recombination and facilitating efficient electron extraction [17]. Additionally, the dipole of these fluorides helps repel holes at this interface making the ETL stack more hole blocking.
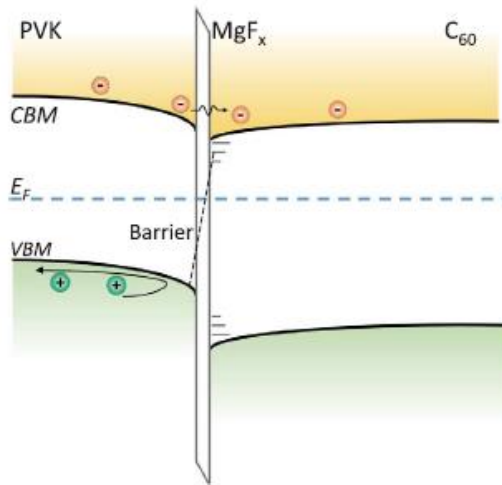

Figure 5.1 Band Bending due to MgF_x at the PSK/C60 interface [17]

Fluoride buffer layers tend to facilitate band bending at the PSK surface as illustrated in Fig 5.1. The Lowest Unoccupied Molecular Orbital (LUMO) of C60 bends downward towards the PSK making this interface more electron-selective with low resistance [17]. Since these interlayers

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are extremely thin, the mechanism with which electrons can reach C60 is either through quantum mechanical tunnelling or via pinholes. A brief literature review showed that mainly MgF_x and LiF interlayers have been successful in enhancing wide bandgap PSK based p-i-n device voltage by about 50 mV with a significant improvement in FF [17].

5.2 Experimental

We made ITO/MeO-2PACz/PSK/MgF_x (<1 nm)/C60(20 nm)/BCP(12 nm)/Ag as well as control devices without MgF_x. SAM and wide bandgap PSK was deposited on PASCAL. Magnesium Fluoride pellets (3.5 mm random pieces, Plasma Materials) were evaporated from a Molybdenum boat at high vacuum (<1E-8 mbar). Since the evaporator control panel provides a precision of 1 A, for the purpose of better thickness control when working with sub monolayers, we timed the deposition from opening the substrate shutter to closing it after achieving a stable rate of 0.1 A/s. Rest of the layers were deposited following the same steps as for the baseline devices as in section 3.1.

5.3 Results and Discussion

The MgF_x based devices (shown in Fig 5.2) have a slightly better champion PCE of 15.76% due to an increase in V_{oc} from 1.025 to 1.05 V, an increase of FF of 72.1% to 74.2 %, and a decrease of J_{sc} from 20.01 to 19.76 mA/cm^2 Thus, it appears that while the MgF_x does passivate the interface, it may be too thick, leading to a drop in current density. In order to inspect this and find the optimized MgF_x condition, we iterated on the thickness by aiming for a slightly lower and higher thickness than the current condition. However, no significant trend was observed. Additionally, all MgF_x based devices had hysteresis (scan-direction dependent JV characteristics)

that are generally attributed to mobile ions at the interface and are not great for long term device performance and stability. To better understand the origins of this peak, XRD was performed. Results show a massive PbI_2:PSK peak ratio, indicating that there is currently a significant amount of unconverted PbI_2 at the interface. Typically, a continuously PbI_2 rich interface tends to have a passivation effect itself and many works have reported great performing devices with excess PbI_2 in their composition. It also displaces the C60 DOS from the PSK DOS sufficiently shielding the PSK top interface from the Fermi level pinning defect in C60. However, it does not absorb light and is resistive. This explains the low J_{sc} in our devices and provides a plausible explanation for why any impact from Fluoride interlayers would not be observable anymore.
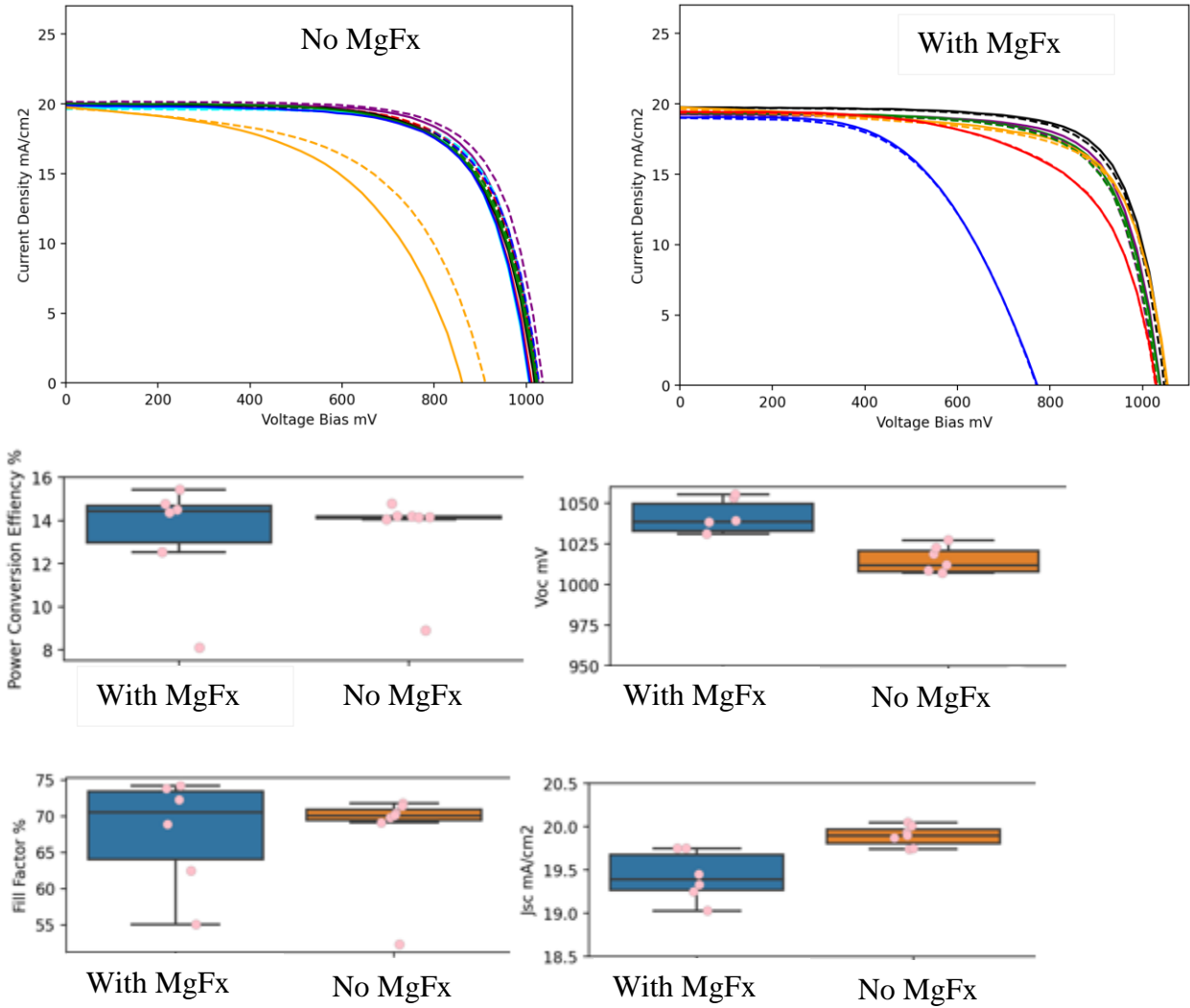
Figure 5.2 JV scans and device statistics for devices with and without MgF_x passivation

To better understand how the PSKs composition affected the MgF_x layers passivation effects, we switched to the prototypical and more stoichiometric $FAPbI_3$ composition and tested the passivation of MgF_x vs LiF. LiF is reported to work better with under-stoichiometric surfaces. As shown in Fig 5.3, interestingly the control devices without passivation were not great and had low voltages but still a relative comparison shall be valid.
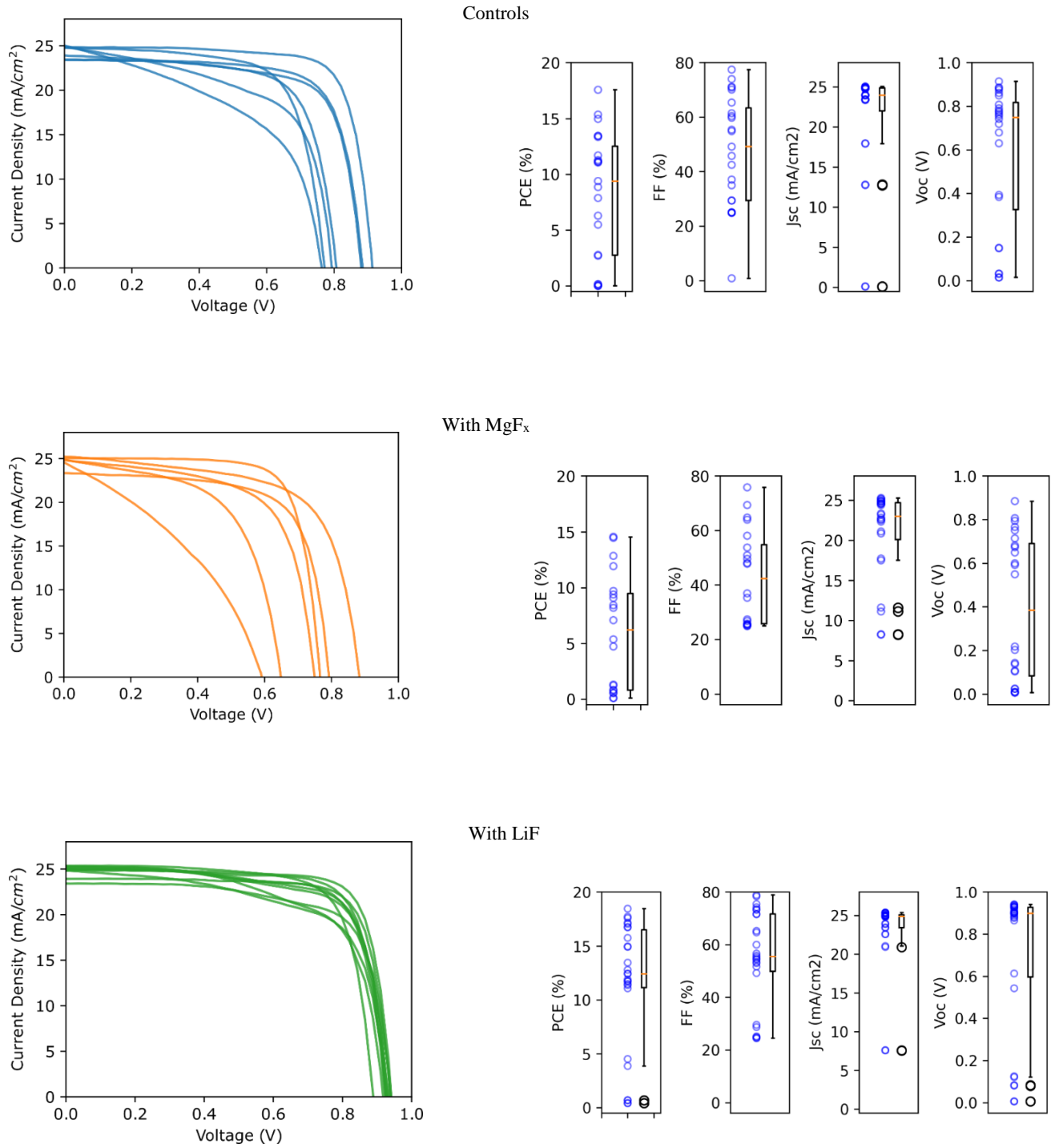
Figure 5.3 JV scans and device statistics for baseline devices as well as with MgF_x and LiF passivation for relative comparison

Clearly LiF worked much better in passivating the FAPbI$_3$ top interface as compared to MgF$_x$. LiF-based devices had at least 100 mV of enhancement in V$_{oc}$ as well as lower hysteresis than baseline devices or the ones with MgF$_x$.

5.4 Photoluminescence Characterization with Absorber (FAPbI$_3$)

To fully utilize the thermodynamic potential of the perovskite absorber, there is a need for both the electron and hole transport layers (ETL and HTL respectively) to be as selective as possible. In all high efficiency devices, V$_{oc}$ is limited by the quasi-fermi level splitting (QFLS) in the absorber layer. However, if the contact layers aren't sufficiently selective, there is a loss in V$_{oc}$ due to non-radiative recombination at that interface. This could be due to improper energy level alignment between Perovskite and the charge transport layer (CTL) and/or trap states defects at the interface. Hence, there is a need to decouple V$_{oc}$ losses in the bulk of the absorber, Perovskite/CTL interfaces and/or at the metal contacts.

5.4.1 Experimental

All samples were made on PASCAL by spin coating SAM and FAPbI$_3$ onto glass substrates followed by transfer into thermal evaporator for LiF, C60, and BCP evaporation. The PL spectra were taken with a 635nm laser at an intensity of approximately 0.1 suns. The collected fraction was coupled into an optical fiber and passed through a 650nm long pass filter of O.D. 4. The spectrum was collected using a Stellar Net Silver Nova CCD spectrometer. Dwell times were varied in the range of [0.1 to 20] seconds in order to maximize signal while not overloading the detector. PL counts were converted to PLQY estimate by assuming that PL counts per second collected by the spectrometer is directly proportional to PLQY. Several films with high PL

intensity were measured on a calibrated absolute PLQY spectrometer (Hamamatsu™ Quantaurus-QY™ C11347) to determine the absolute PLQY. The counts per second PL intensity measured on the PASCAL CCD spectrometer combined with the PLQY values allowed us to draw a line of best fit to extrapolate PLQY values well below that attainable using an integrating sphere.

5.4.2 Results and Discussion

Results are summarized in Fig 5.4. As suspected, and also seen in the literature, addition of C60/BCP quenched the PL by more than 2 orders of magnitude indicating extensive recombination due to trap states introduced by C60. However, when there is a fluoride interlayer displacing C60 from the PSK surface, we note an increase in PL intensity by about half an order of magnitude. Thus, LiF is able to passivate the trap states. This PL intensity was used to calculate PLQY which in turn was used to get the implied V_{oc} (iV_{oc}) values. We found that our FAPbI$_3$ with a bandgap of 1.542 eV has a thermodynamic limit of 1.25 eV. Addition of C60 to the absorber adds about 120 mV loss. However, with LiF passivation, there is comparatively lesser deficit of 100 mV indicating scope of future work in the direction of optimizing PSK/LiF interface.

Figure 5.4 PL intensity, Approximate PLQY and iV$_{oc}$ of interface for SAM/PSK, SAM/PSK/C60/BCP and SAM/PSK/LiF/C60/BCP stacks
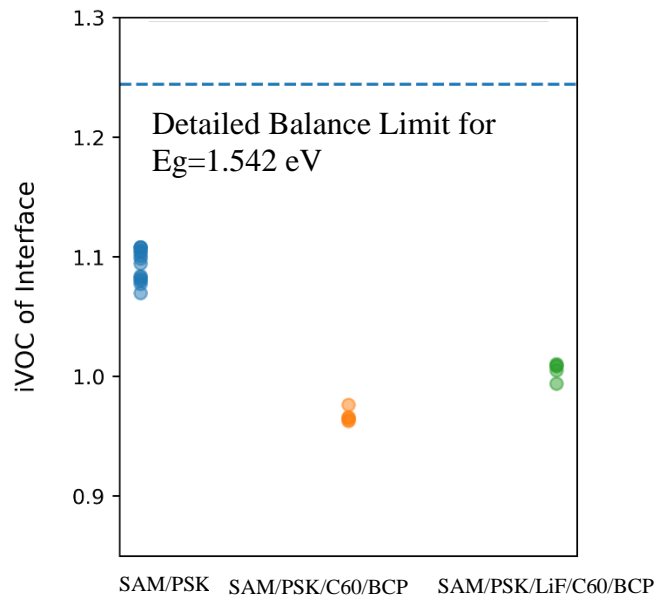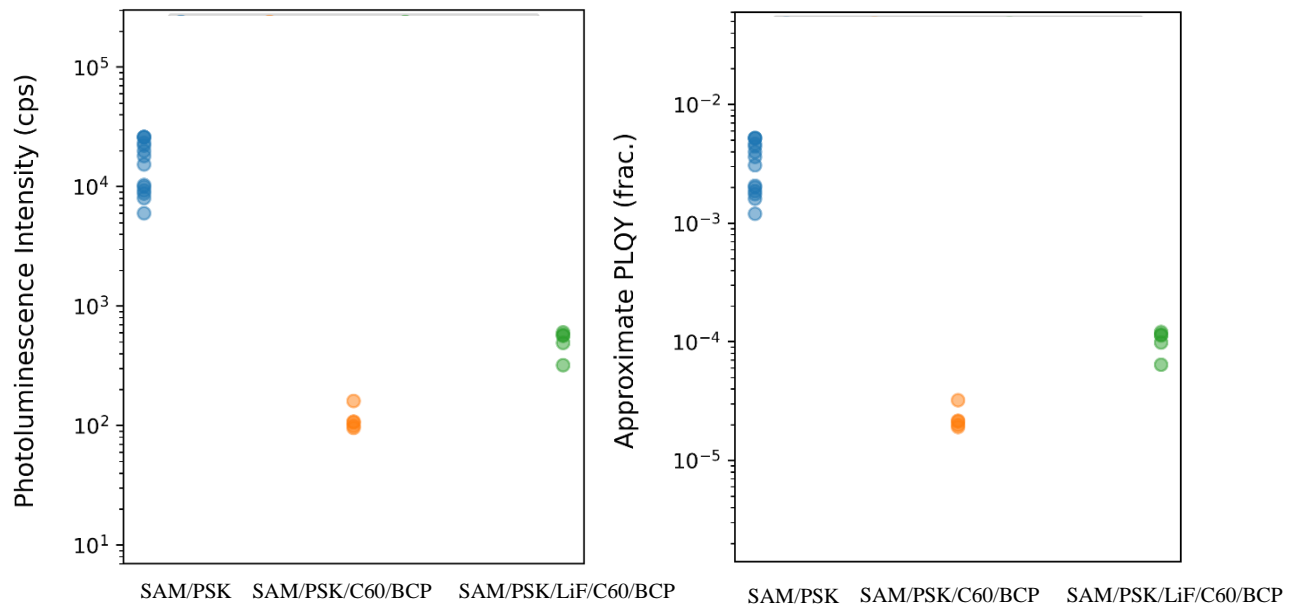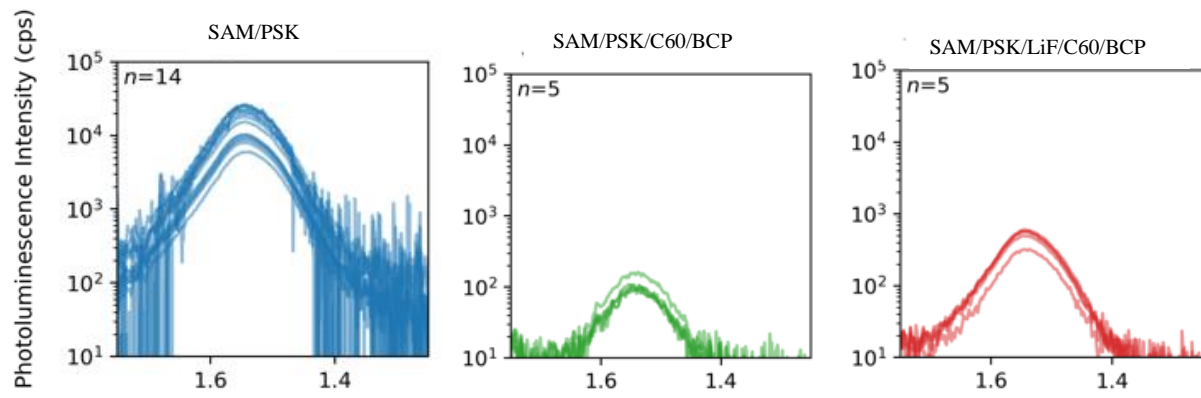
5.5 Conclusion and Future Work

In conclusion, the maximum losses are incurred at the ETL and HTL interface. First pass results from LiF passivation look promising on $FAPbI_3$ and further optimization could help mitigate recombination on the ETL side. Further, it would be interesting to see synergistic effect of a passivating agent called 3-(aminomethyl)pyridine (3-APy) with that of LiF. 3-APy bonds with the FA cation on the PSK surface reducing roughness and surface potential fluctuations associated with steps and terraces on the PSK surface. Most importantly, it affects the energetics, creating a built-in electric field that favors electron extraction and mitigates recombination [22] It would be interesting how this effect would couple with (if at all) LiF passivation which essentially is displacing C60 DOS from PSK DOS.

CONCLUSION

Overall, this thesis work demonstrates a baseline for p-i-n PSCs using PVD processed ETLs. Prior to device fabrication, the deposition process for each of the materials was first established on the thermal evaporator followed by tooling factor calibration. The impact of the evaporation source on the morphology of films can be noted through the vast difference in device results on switching to Tantalum boats which helped in preventing spitting of the material during thermal evaporation. By using a suitable evaporation source and manual evaporation recipes dialed in for each of the materials, we were able to make our fabrication process more repeatable and attain reproducibility. The best devices had a V_{oc} of 1.038 V and J_{sc} 20.67 mA/cm^2 and a great FF of 78.4 % (reverse scan). Additionally, we tested PVD SnO_x as a buffer layer against sputter damage during ITO deposition for applications in Perovskite-Silicon tandems. Although as-deposited SnO_x works great as an ETL buffer layer, it fails to protect the underlying organic layers from damage. A buffer layer would need a denser morphology to prevent high energy sputtering atoms from penetrating. Lastly, we developed PVD processes for two of the fluoride passivation layers (LiF and MgF_x) for testing their passivation effect on the baseline devices. First pass results show that LiF buffer layer was promising with slight enhancement in both V_{oc} and FF. The performance losses in the baseline p-i-n devices were uncoupled by characterizing the SAM/PSK, SAM/PSK/C60/BCP and SAM/PSK/LiF/C60/BCP stacks. Implied V_{oc} calculations tell us that 120 mV are lost just at C60 interface due to non-radiative recombination. However, the deficit isn't that much when LiF is inserted between PSK and C60. Hence, further optimization on LiF deposition could yield better results and help mitigate extensive recombination due to C60 trap states which seems to be one of the main limiting factors to the device performance. Table 1 summarized the best device performance for all the conditions tested.

Table 1: Champion Devices from all the conditions tested (statistics for reverse scan)

	Voc (V)	Jsc (mA/cm2)	FF (%)	PCE (%)
WBG Baseline p-i-n	1.038	20.67	78.4	17.02
FAPbI$_3$	0.914	24.82	77.42	17.56
FAPbI3 with LiF passivation	0.94	24.87	78.83	18.45
FAPbI$_3$ with MgFx passivation	0.766	25.04	75.82	14.55
WBG with SnOx as buffer layer	1.02	20.38	75.11	15.62

$$y = 1.9871x + 3.6439$$
$$R^2 = 0.8602$$
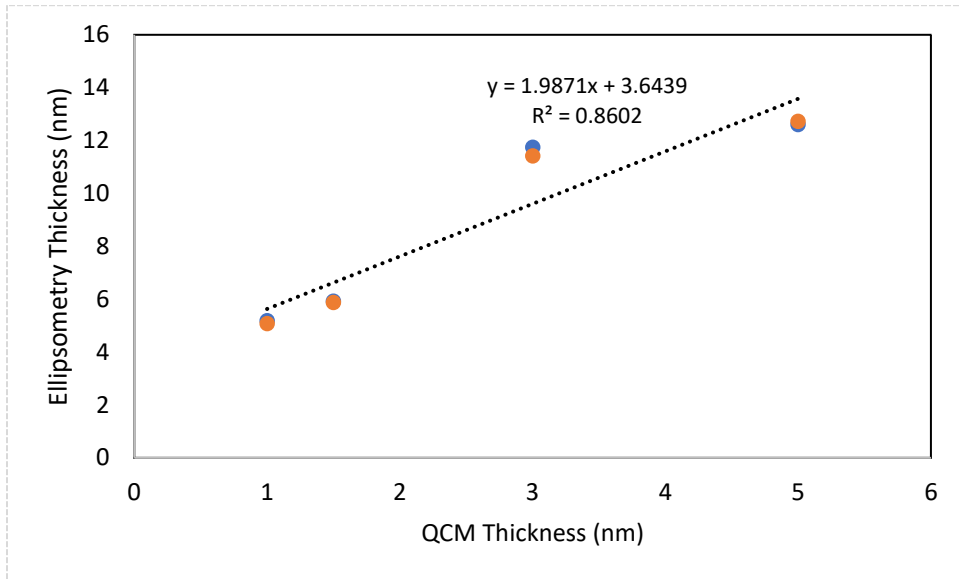
Fig S1: Tooling Factor Calibration of BCP

$$y = 0.869x + 6.1517$$
$$R^2 = 0.9892$$
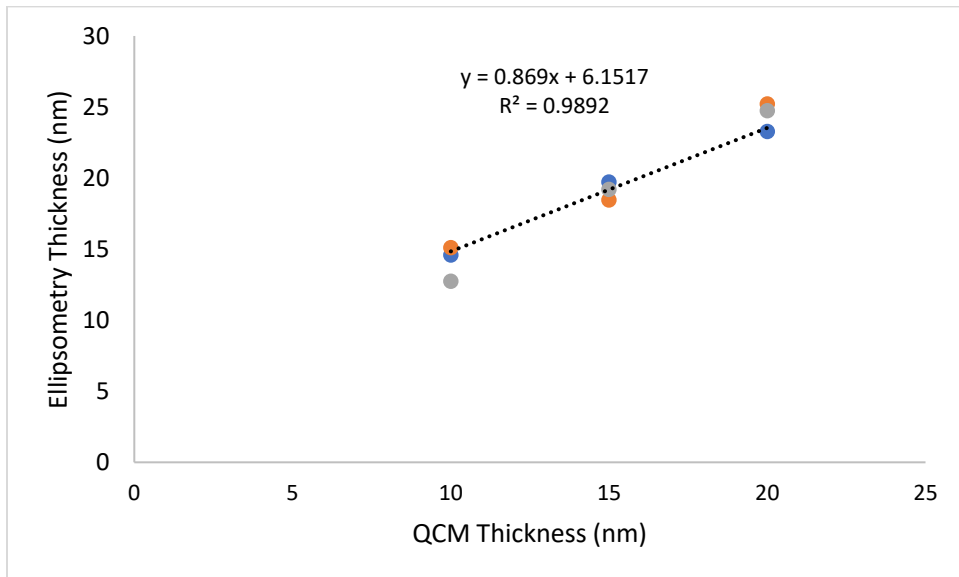
Fig S1: Tooling Factor Calibration of C60

Note the discrepancy between the 0 nm reading on QCM to the corresponding ellipsometry

thickness in both the cases. One of the potential reasons behind this offset could be the fact that

the material evaporation isn't perfectly line of sight. This can be investigated further by

evaporating with the substrate shutter closed and then measuring thickness by ellipsometry.

Table 1: PID settings for automated depositions

Material	P	I	D
C60	30	2.5	1
BCP	25	2.5	0
LiF	40	3	0

First pass attempts at depositing ETL stack on PSK deposited by hybrid method (PVD+spin conversion) for Perovskite top cell on textured Silicon cells
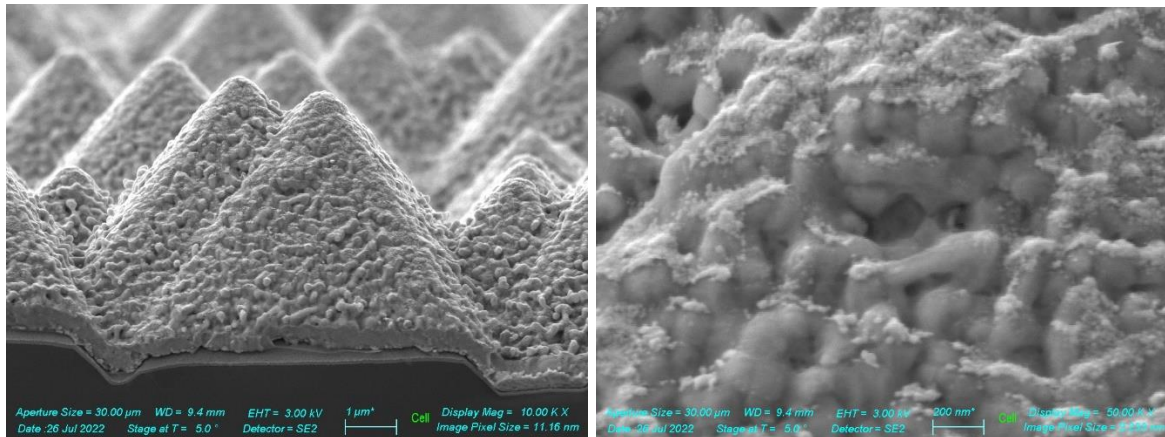
S3: Cross section SEM images of Perovskite-Silicon tandem cell where WBG Perovskite was deposited using a 2-step method (Co-evaporation of PbI_2 and CsBr scaffold followed by spin-coated conversion using FAI). Top cell configuration: Textured Si/Poly-TPD/PSK/C60/SnO_x/Ag (10nm)/Ag (100 nm). All the cells were shunted and evidently, the resulting morphology from hybrid deposition of PSK isn't conformal. This affects the morphology of the next layers as well. The ETLs seem to have been 'snowed' onto the PSK instead of uniform coverage.

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