UNIVERSITY OF CALIFORNIA, SAN DIEGO

Design Implementation and Channel Equalization of Double-Edge Pulsewidth Modulation Signaling

A dissertation submitted in partial satisfaction of the
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by

Wei Wang

Committee in charge:

Professor James F. Buckwalter, Chair
Professor Peter Asbeck
Professor Gert Cauwenberghs
Professor Lawrence Larson
Professor Steven Swanson

2014

The dissertation of Wei Wang is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2014

DEDICATION

To my family.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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VITA

1999-2003	B. S. in Electrical Engineering, Chang Gung University
2003-2005	M. S. in Electronics Engineering (Integrated Circuits and Systems), National Taiwan University
2007-2010	M. E. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego
2007-2013	Graduate Research Assistant, University of California, San Diego
2010-2014	Ph. D. in Electrical Engineering (Electronic Circuits and Systems), University of California, San Diego

PUBLICATIONS

W. Wang and J. F. Buckwalter, " Source Coding and Pre-emphasis for Double-Edge Pulsewidth Modulation Serial Communication, *submitted for review to IEEE J. Solid-State Circuits*, Jan. 2014.

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ABSTRACT OF THE DISSERTATION

Design Implementation and Channel Equalization of Double-Edge Pulsewidth Modulation Signaling

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Wei Wang

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Professor James F. Buckwalter, Chair

A 10-Gb/s serial link transceiver is demonstrated using double-edged pulse width modulation (DPWM) to overcome frequency-dependent losses in electrical interconnects. Time domain modulation is discussed as a means to enhance the spectral efficiency in channels with sharp frequency roll-off similar to multilevel voltage-domain modulation such as 4-PAM. The transmitter and receiver are high-speed programmable digital-to-time and time-to-digital converters that adapt to channel bandwidth characteristics with a timing resolution of 40 ps. This thesis presents a low-jitter, phase rotation architecture for cycle-to-cycle transmit pulsewidth control. The transceiver includes an elastic buffer to move data between synchronous and plesiochronous clock domains and is implemented in 45-

nm CMOS SOI. Transmitter and receiver functionality is demonstrated to 10 Gb/s at a BER of under 10^{-12} and is compared against NRZ schemes at the same rate. The inductor-less transmitter and receiver active circuitry respectively occupy an area of 93x94 and 218x160 μm^2, and consume a total 107 mW from a 1.2 V supply.

DPWM is less sensitive to frequency-dependent losses in electrical chip-to-chip interconnects. However, the DPWM scheme instantaneously transmits information at a different rate than a synchronous source. For the second-generation DPWM transceiver, this thesis presents an 8b/9b line coding scheme to compensate for the timing skew between the DPWM and synchronous clock domains while limiting the size of buffering required in the transmitter and receiver. Furthermore, pre-emphasis is introduced and analyzed as a means to improve the signal integrity of a DPWM signal. A multiphase-based, time interleaving receiver architecture using a sense amplifier is presented for high-speed data recovery. The second-generation DPWM transceiver is also implemented in 45-nm CMOS SOI and operates at 10 Gb/s with 10^{-12} BER and consumes 94 mW. The power consumption of the 8b/9b coding hardware is 1.5 mW at 10 Gb/s demonstrating low power overhead.

Chapter 1

Introduction: Multi-GS/s Electrical Interconnects

Chip-to-Chip memory links have faced substantial scaling problems to satisfy per-pin data rate requirements. Low-cost backplanes support modular memory interfaces to expand capacity and flexibility. Data rates beyond a few gigahertz are limited by FR4 laminates and aggravated by the expansion of the link over multiple memory modules, which introduce impedance discontinuity and crosstalk. The frequency response of an interconnect on printed circuit board (PCB) is degraded by many factors such as plated-through-hole vias, connectors and multi-drop bus configurations [1], [2]. Vias form open stubs that cause notches in the insertion loss, especially in multi-layer boards but can be mitigated with back-drilling but at higher fabrication cost. Multidrop configurations, such as stub-series-terminated-logic bus and doubled-data-rate (DDR) memory busses enlarge the total storage capacity. As the drop number (the number of slave modules) increases, multiple impedance discontinuities at each connector introduce reflections which incur dips in the frequency response that limit the data rate and degrade signal integrity [3].

In a multidrop memory bus, capacity expansion comes at the expense of signal reflections at T-junctions as illustrated in Fig. 1.1. The controller and slave module represent the memory controller and dual-in memory modules in DDR memory systems. The T-junctions in a multi-drop memory bus reduce incident signal power received by slave modules and deteriorate the signal integrity. As the

slave number increases, multiple impedance discontinuities at each drop incur an accumulated attenuation dip in the channel [4]. The slot connectors (Conn) are another constraint when memory modules are unpopulated [2], [3]. For example, when one slave module is not populated, the unterminated connector incurs signal reflections to the main channel and the other slave modules.

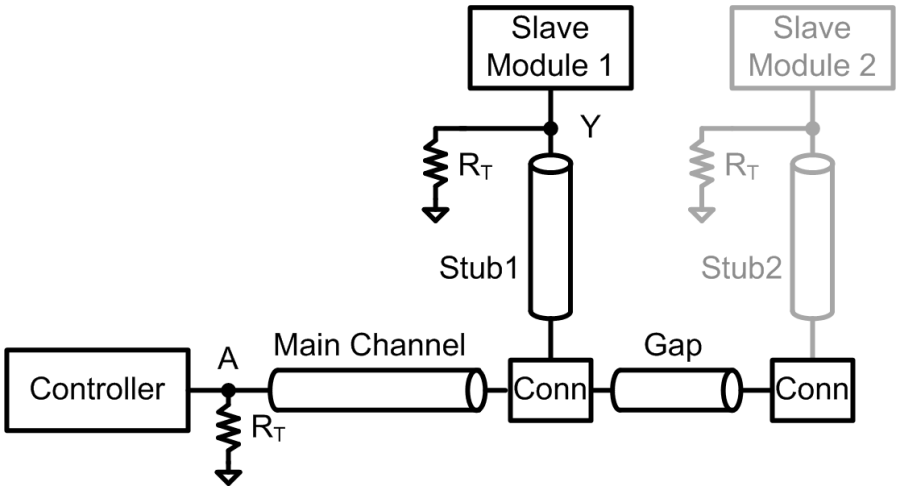


Fig. 1.1: A 2-slot DDR memory bus configuration

These issues can be mitigated through equalization if the channel response is not severely degraded (e.g. features nulls). Transmitter feed-forward pre-emphasis and receiver equalization can compensate channel loss and have demonstrated bit rates above 10 Gb/s using NRZ signaling across the copper backplanes [5], [6]. In general, intersymbol interference (ISI) in lossy channels is counteracted by incorporating a larger number of equalization taps into the equalizer. Severely stressed channels have sharp frequency response and the equalization circuitry demands high power consumption. Consequently, NRZ signaling becomes less attractive as significant equalization is demanded at the transmitter and receiver [3]. A resonance mitigation technique is proposed with excessive PCB area in [7].

Channel coding approaches can alleviate some of the issues of the channel response. Multilevel modulation such as 4-PAM and duobinary signaling have been proposed to improve the data rate in ISI-limited channels [4], [8], [9], [10]. Multi-level signaling enhances the spectral efficiency over such channels but often imposes higher voltage swing requirements which suggest high supply voltages and hence

higher power consumption. With multilevel signals, the front-end receiver requires a linear amplifier and a 4-PAM receiver necessitates an AGC to control the signal swing [10], [11]. Furthermore, the reduced dynamic range complicates the design of equalizers capable of compensating the severe attenuation of backplane transmission lines. A technique of mixing PWM/PAM reduces the channel bandwidth requirement but necessitates the use of dual supply voltages, i.e., a low supply voltage for PWM and a high supply voltage for PAM in [12], [32]. Alternative modulation approaches have been suggested that are suited to high frequency-dependent attenuation including discrete multitone and CDMA [13], [14].

This thesis presents an approach to multi-level signaling based on double-edge pulsewidth modulation (DPWM) to encode information into pulsewidth intervals. Previously, DPWM has been reported for high-frequency channels and the trade-offs between the timing parameters has been discussed [2], [15]. This thesis reviews the timing parameters and their influence on the data rate and signal integrity of the signal. Moreover, the low-jitter implementation of these parameters is demonstrated for the first time in a CMOS SOI technology. The pulsewidth modulation transmitter and receiver benefit from the scaling of devices through higher f_T, which can be leveraged for finer timing resolution. DPWM has been previously investigated for asynchronous memory links where several issues were encountered [16]. First, data rates were limited due to the architecture of the DPWM digital-to-time converter (DTC). Positive and negative pulses were alternatively generated by RS-latches resulting in high random and deterministic jitter due to propagation delay mismatches. A DTC for single-edge PWM improved the jitter performance by utilizing multiphase clocks but achieves half the bit rate of DPWM [17]. Second, asynchronous links are not feasible in many serial link applications where synchronous operation is desired. This thesis addresses each of the challenges of DPWM communication through electrical interconnects.

1.1 Dissertation Organization

Chapter 2 discusses the timing parameters of DPWM and compares this to NRZ signaling. The temporal and spectral characteristics of DPWM are related to the channel characteristic.

Chapter 3 discusses the circuit implementation of a DTC in a 45-nm SOI CMOS process. A DTC architecture is proposed that allows accurate, low-jitter control of the timing properties of the DPWM modulation. An elastic buffer interface concept for synchronous data links is introduced. A section of this chapter introduces a multiphase-based time-interleaving time-to-digital converter (TDC) architecture of high conversion rate and fine timing resolution. The final section presents measured performance of the DPWM transmitter over a DDR channel emulator. Similar to the voltage-domain modulation schemes, such as PAM-4 and Duobinary, time-domain modulation scheme DPWM also presents enhanced spectral efficiency compared to NRZ in the channels of sharp frequency rolloff.

Chapter 4 describes the frequency drift issue using DPWM for synchronous data links and discusses 8b/9b encoder to realize a low-power EB that prevents excessive long-term frequency skew.

Chapter 5 addresses pre-emphasis parameters to improve signal integrity.

Chapter 6 demonstrates 8b/9b hardware designs and measures the second-generation transceiver performance in both temporal and spectral domains. This chapter also introduces the transceiver architecture for synchronous data links.

Chapter 7 concludes the dissertation.

The dissertation author would like to acknowledge Prof. Buckwalter for his revision of this chapter. This chapter, in full, is a reprint of the material as it appears in IEEE Transactions on Circuits and Systems: I - Regular Papers, 2013, Wei Wang; James F. Buckwalter. The dissertation author was the primary investigator and author of this paper.

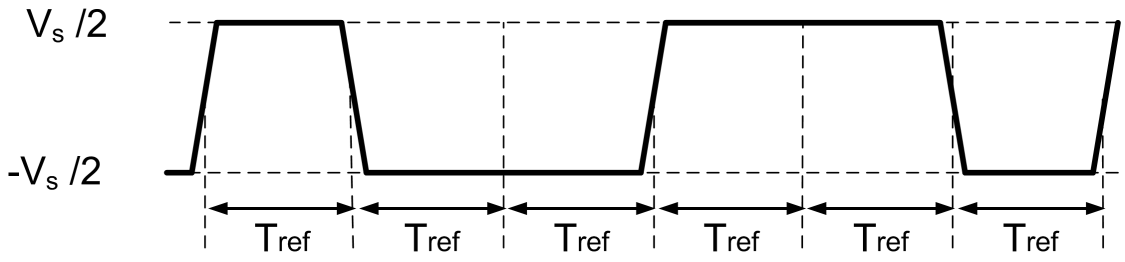
Chapter 2

Non-Return-to-Zero and Pulsewidth Modulation

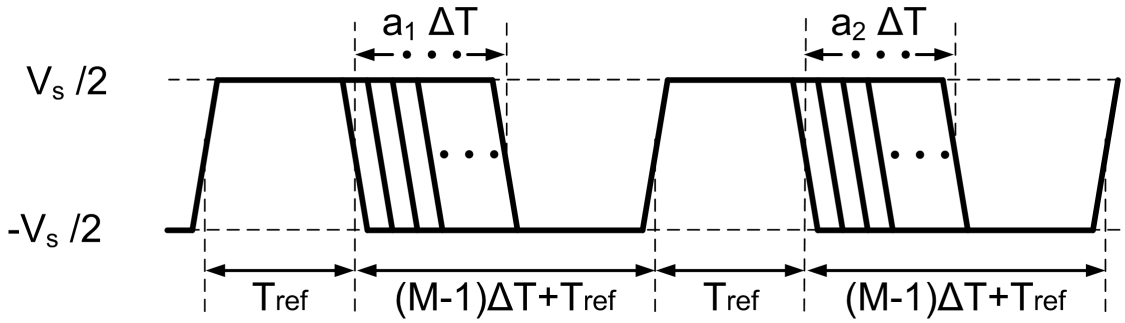
To understand the advantages of a DPWM scheme, it is useful to compare this signaling to the more conventional NRZ scheme. The proposed modulation schemes are illustrated in Fig. 2.1 to define the voltage and timing parameters. Two timing parameters are available in the design of the pulsewidth modulation scheme; a minimum pulsewidth that is chosen based on the channel bandwidth and a discrete timing interval that is chosen based on the receiver timing resolution. Encoding $\log_2(M)$ bits into M pulsewidths as opposed to the M amplitude levels theoretically approaches the spectral efficiency of M-ary PAM without increasing the voltage swing and, therefore, increasing the power consumption of the line driver. However, there is a circuit overhead to efficiently convert digital values to a time encoding and then recover these values in the receiver. Therefore, DPWM takes advantage of the scaling of CMOS transistors to encode information into timing resolution.

2.1 Non-Return-to-Zero Signaling

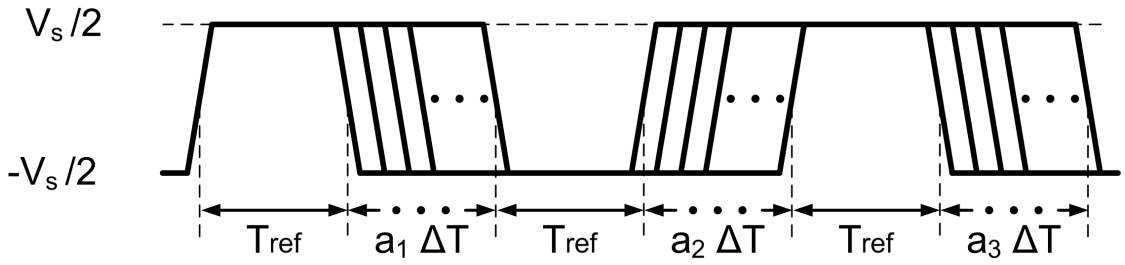
Fig. 2.1a illustrates the amplitude and timing of an NRZ signal. Each transmitted bit is encoded into two amplitudes separated by V_s during each symbol period, T_{ref}. The bit rate $f_{b,NRZ}$ of NRZ is $1/T_{ref}$ and the maximum bit rate



(a) NRZ



(b) Synchronous falling-edge M-PWM signaling



(c) Double-edge M-PWM signaling

Fig. 2.1: Pulse amplitude and pulsewidth modulation.

is related to the channel bandwidth since the channel bandwidth must be great enough to allow the propagation of data pulses of width T_{ref}. Equalization is widely used to compensate the intersymbol interference and timing jitter introduced by the channel bandwidth. M-ary pulse amplitude modulation increases the spectral efficiency over NRZ signaling by $\log_2(M)$, since more symbols exist in a given symbol period. This approach typically requires higher power consumption for a given signal to noise ratio (SNR).

2.2 PWM Signaling

Fig. 2.1b depicts PWM signaling where $\log_2(M)$ bits are encoded into M pulsewidths on the falling-edge (or rising edge). Symbol $a[k]$ takes values from 0 to M-1 during the k_{th} period. The positive pulsewidth of the k_{th} symbol period is

$$T_{PWM,p}[k] = T_{ref} + a[k]\triangle T, \tag{2.1}$$

where T_{ref} is the minimum pulsewidth and $\triangle T$ is the minimum timing resolution between each symbol. These timing parameters play an important role in defining spectral characteristics of the PWM signaling scheme. The PWM symbol period is

$$T_{PWM} = 2T_{ref} + (M\text{-}1)\triangle T. \tag{2.2}$$

The PWM scheme is synchronous since the period is constant. Therefore, the bit rate for PWM is

$$f_{b,PWM} = \frac{\log_2 M}{T_{PWM}} = \frac{\log_2 M}{2T_{ref} + (M\text{-}1)\triangle T}. \tag{2.3}$$

2.3 DPWM Signaling

To enhance the spectral efficiency in PWM, DPWM modulates the signal pulsewidth during both positive and negative excursions as shown in Fig. 2.1c. Each positive and negative pulsewidth is encoded with different symbols.

$$T_{DPWM,p/n}[k] = T_{ref} + a[k]\triangle T \tag{2.4}$$

As opposed to the PWM approach where the instantaneous period was fixed, the instantaneous period in DPWM deviates each clock period. However, the average period converges to

$$T_{DPWM} = E[T_{DPWM,p} + T_{DPWM,n}] = 2T_{ref} + (M\text{-}1)\triangle T, \tag{2.5}$$

where $E[\,]$ is the expectation. Finally, the bit rate of DPWM signaling can be calculated as

$$f_{b,DPWM} = \frac{2\log_2 M}{T_{DPWM}} = \frac{2\log_2 M}{2T_{ref} + (M\text{-}1)\triangle T}. \tag{2.6}$$

Most importantly, the DPWM bit rate is twice the PWM bit rate in (2.3). The increasing of M results in the increasing of the number of bits transmitted during each period but the average symbol period increases linearly with M. Since T_{ref} and$\triangle T$ contribute to the symbol period, this suggests an optimal data rate for PWM and DPWM.

2.4 Timing comparison of NRZ and DPWM signaling

An analysis of the relationship between timing parameters required for a particular bit rate is discussed here to motivate the specification for the circuit implementation. Here, the channel bandwidth is related to T_{ref} and $\triangle T$ to provide a rule of thumb for timing parameter of the DPWM signaling. The relationship between the channel bandwidth and T_{ref} significantly affects the channel deterministic jitter (DJ) and limits the tolerable random jitter (RJ) in the receiver for a given bit error rate.

To compare the different modulation schemes, Fig. 2.2 plots the bit rate of each modulation scheme as a function of M under the conditions described in Table 2.1. The bit rate of NRZ is 10 Gb/s for T_{ref} = 100 ps. For PWM, there

are several combinations of T_{ref} and $\triangle T$ that will result in 10 Gb/s signaling. To quantify the combinations of T_{ref} and $\triangle T$, we define the parameter, r, as $\triangle T/T_{ref}$. These design parameters allow us to trade-off the minimum pulsewidth and the timing resolution. Based on T_{ref} = 80 ps, the timing resolution at the receiver is $\triangle T$= 20 ps. This fine timing resolution must be considered in terms of a SNR that considers various sources of timing jitter and requires accurate sampling to reach the desired bit error rate [15].

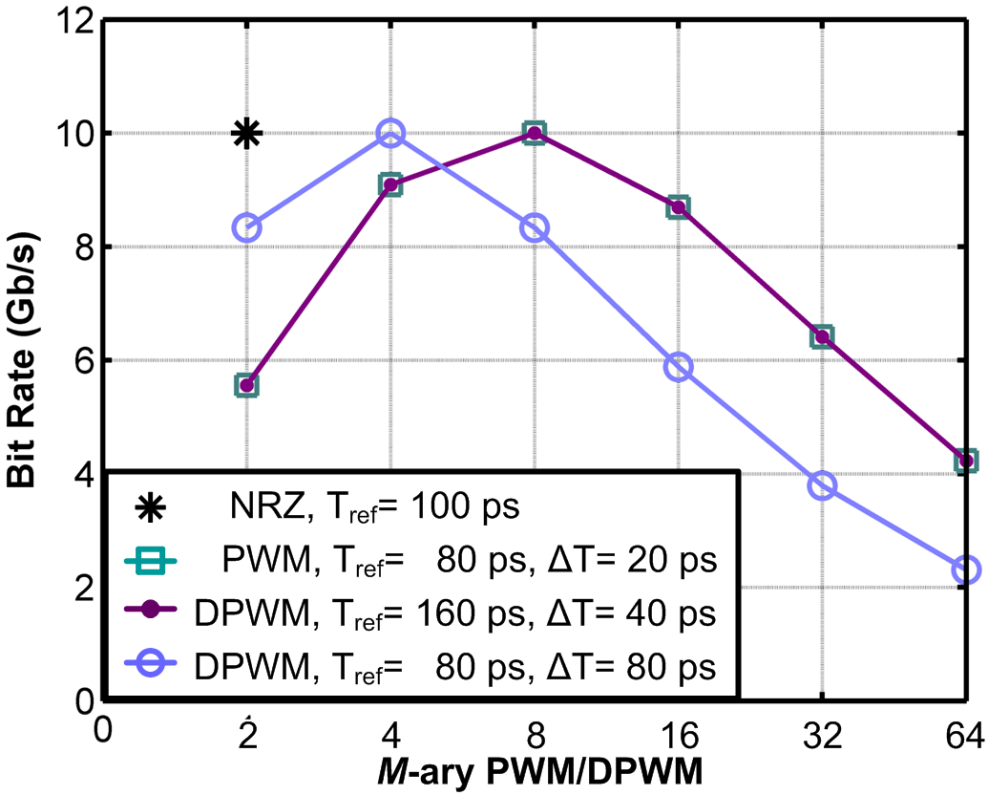


Fig. 2.2: Bit rate versus M-ary signaling based on the parameters shown in Table 2.1

For DPWM, two combinations of T_{ref} and $\triangle T$ are demonstrated in Table I that allow different minimum pulsewidths. The data rate is plotted as a function of M in Fig. 2.2. First, a longer minimum pulsewidth of T_{ref} = 160 ps and $\triangle T$ = 40 ps reaches 10 Gb/s and the optimal bit rate occurs at M = 8 for r of 0.25. The minimum pulsewidth is relaxed at the expense of finer timing

Table 2.1: Timing parameters for each 10-Gb/s modulation scheme

Modulation	T_{ref}	$\triangle T$
NRZ	100 ps	N/A
8-PWM ($r = 1/4$)	80 ps	20 ps
8-DPWM ($r = 1/4$)	160 ps	40 ps
4-DPWM ($r = 1$)	80 ps	80 ps

resolution. This combination would benefit relatively low channel bandwidth but excellent timing discrimination in the receiver. On the other hand, a bit rate of 10 Gb/s is achieved for $T_{ref} = 80$ ps and $\triangle T = 80$ ps, e.g. r is 1, at $M = 4$. The shorter T_{ref} allows coarser timing resolution in the receiver in the presence of high channel bandwidth. The trade-off between the minimum pulsewidth and the timing resolution is described by rewriting (2.6) as follows,

$$T_{ref} = \frac{\log_2 M}{f_b} - \frac{(M\text{-}1)}{2}\triangle T. \tag{2.7}$$

This illustrates that for a fixed bit rate (i.e. 10 Gb/s) M-ary DPWM approaches the performance of M-ary PAM ($^{\log_2 M}/_{f_b}$) for sufficiently fine timing resolution. Therefore, DPWM becomes attractive given sufficiently fast CMOS devices that allow fine timing resolution.

The bit rate of DPWM can be determined from

$$f_{b,DPWM} = \frac{1}{T_{ref}} \frac{2\log_2 M}{2 + (M\text{-}1)r}. \tag{2.8}$$

Fig. 2.3 illustrates the bit rate as a function of the ratio r. When r is larger than 0.4, 4-DPWM achieves the highest data rate. When r is less than 0.12, 16-DPWM achieves the highest data rate. In other words, the ratio r determines the optimal M-ary DPWM regardless of the choice of T_{ref}. The optimal r choices for three different DPWM schemes are summarized in Table 2.2. As finer timing resolution

is available, the use of higher order DPWM modulation can approach data rates of 20 Gb/s.

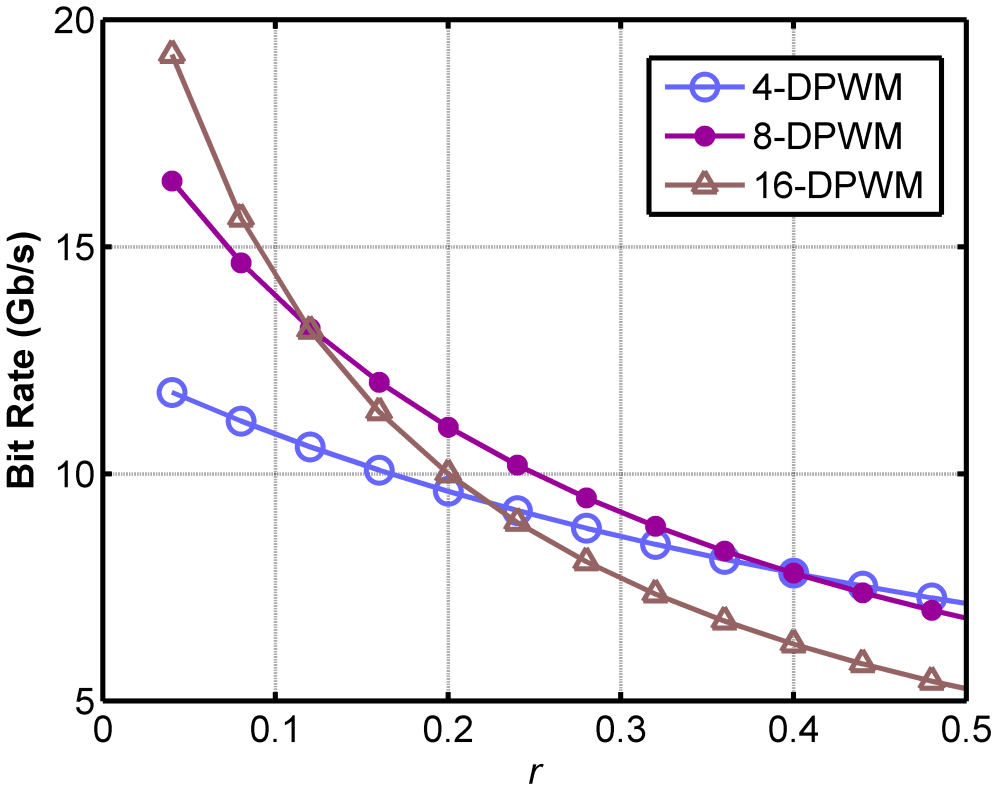


Fig. 2.3: Bit rates versus r among DPWM schemes where T_{ref} =160 ps

Table 2.2: r choices for optimal bit rates using different DPWM schemes

Modulation	16-DPWM	8-DPWM	4-DPWM
Optimal f_b condition	$r < 0.12$	$0.12 \leq r < 0.4$	$0.4 \leq r$

The channel bandwidth determines the minimum T_{ref} adopted in DPWM to avoid substantial intersymbol interference. Previous work has demonstrated that PWM symbols are non-uniformly impacted by deterministic jitter due to the different pulsewidth intervals [18]. Instead, T_{ref} is proposed here as a parameter which can be chosen to be long enough to avoid the need for equalization of the

deterministic jitter. If the channel bandwidth is 3.125 GHz, T_{ref} is 160 ps. From (6), the bit rate of 10 Gb/s can be actually achieved by multiple schemes, e.q. 4-DPWM, 8-DPWM, and 16-DPWM, by adjusting $\triangle T$. Fig. 2.3 depicts the bit rates achieved by the three DPWM schemes versus the ratio r. Using 8-DPWM requires a timing resolution of 40 ps (r= 0.25) while 16-DPWM and 4-DPWM require timing resolutions of 32 ps and 27 ps (r= 0.2 and 0.17), respectively. To choose the appropriate timing resolution, the signal-to-noise ratio defined at the receiver should be considered:

$$SNR_t = \frac{\Delta T}{\sigma_{RJ}}, \tag{2.9}$$

where σ_{RJ} is the standard deviation of the random timing jitter seen at the receiver. To choose the appropriate timing resolution, the channel timing jitter must be estimated. For a BER of less than 10^{-12}, $\Delta T > \alpha\sigma_{RJ}$ where α is 14. If the random jitter is constrained to 3 ps, the timing resolution should be around 40 ps. Therefore, 8-DPWM was selected for a bit rate of 10 Gb/s. Generally, bit rates between 8 Gb/s and 13 Gb/s suggest that the combination of 8-DPWM and moderate r provides the best performance. For lower bit rates under 8 Gb/s, 4-DPWM and larger choices of r can suffice. These timing parameters will be translated into the implementation of the DPWM circuit.

2.5 Spectral comparison of NRZ and DPWM signaling

Another consideration in the choice of the modulation scheme is the power spectral density (PSD). The PSD is compared to illustrate the anticipated benefit for bandwidth limited channels. According to the parameters summarized in Table 2.1, Fig. 2.4 plots the PSD of the NRZ, PWM, and DPWM schemes at 10 Gb/s.

For a bit rate of 10 Gb/s, the NRZ period is 100 ps. Typically, a channel bandwidth greater than 50% of the bit rate is required to prevent substantial ISI. In (4.1), T_{ref} determines the highest frequency component of $1/(2T_{ref})$ in signal power main lobe. For DPWM, $\triangle T$ is determined by the amount of tolerable

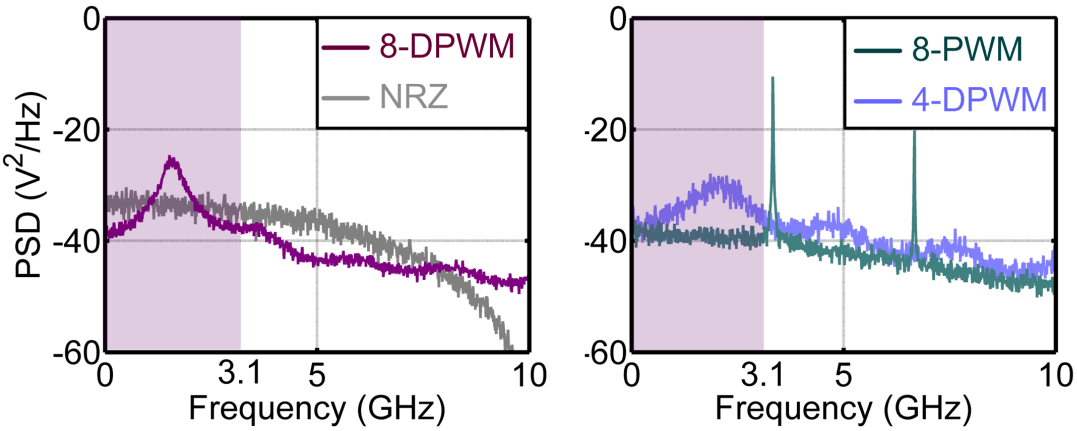


Fig. 2.4: Simulated power spectral density of 8-DPWM, NRZ, 8-PWM and 4-DPWM for a data rate of 10 Gb/s (Parameters are described in Table I.)

random jitter and deterministic jitter. For 8-DPWM ($r = 1/4$), the minimum pulsewidth T_{ref} and the timing resolution$\triangle T$ are 160 ps and 40 ps. Since T_{ref} is larger for 8-DPWM relative to NRZ, 8-DPWM concentrates the signal power at lower frequencies as plotted in Fig. 2.4. The peak signal energy of 8-DPWM is located under $1/2T_{ref}$, just under 3.125 GHz, and thus 8-DPWM requires a lower channel bandwidth. For 4-DPWM ($r = 1$), T_{ref} and $\triangle T$ are both 80 ps. The 4-DPWM T_{ref} is smaller than the minimum pulsewidth for NRZ. The shorter T_{ref} results in signal power distributed more broadly in spectrum and incurs the higher energy loss compared to 8-DPWM in Fig. 2.4. On the other hand, 8-PWM requires half of the minimum pulsewidth of the 8-DPWM signaling and this pushes the harmonics to higher frequencies. The PWM PSD exhibits harmonics at the average symbol period, 2 T_{ref} +7$\triangle T$, in this case at 3.3 GHz.

Fig. 2.5 plots the integrated signal power based on a brick-wall frequency response. Because 8-DPWM utilizes the longest minimum pulsewidth, 77% of the signal power is located below 3.125 GHz. This suggests that 8-DPWM is the best choice for the lowest bandwidth. The total signal power of 4-DPWM, NRZ, 8-PWM and at a brick-wall cutoff of 3.125 GHz are respectively 64%, 56%, and 9%. Therefore, 8-DPWM provides the greatest benefit by concentrating signal power at lower frequencies. Most importantly, DPWM outperforms NRZ when the T_{ref}

of DPWM can be increased at the expense of narrower timing resolution $\triangle T$ in the receiver. In essence, as the timing resolution becomes narrower the DPWM signal approximates the phase noise around a fixed carrier frequency.

While equalization techniques could be introduced to reduce ISI and data-dependent jitter (DDJ), the approach taken in this chapter is to increase T_{ref} to mitigate the DDJ contribution to the total jitter. Nonetheless, equalization could be implemented for DPWM to improve signal integrity based on both ISI and DDJ.

The dissertation author would like to acknowledge Prof. Buckwalter for his revision of this chapter. This chapter, in full, is a reprint of the material as it appears in IEEE Transactions on Circuits and Systems: I - Regular Papers, 2013, Wei Wang; James F. Buckwalter. The dissertation author was the primary investigator and author of this paper.

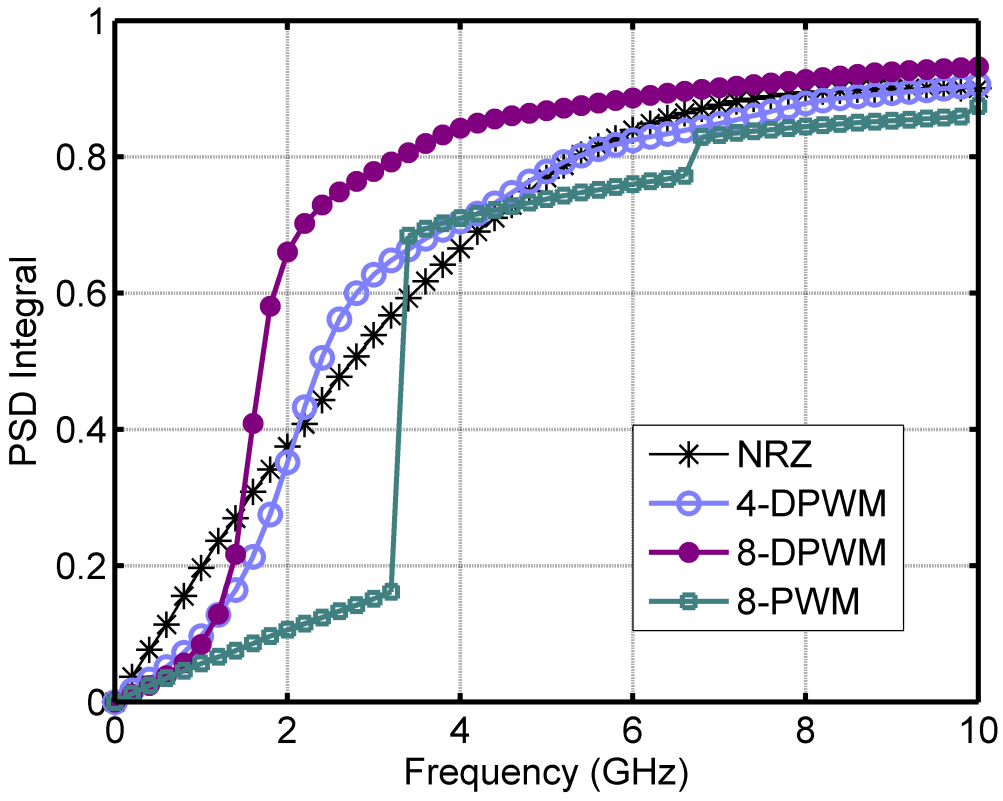


Fig. 2.5: Integrated signal power for a brickwall filter

Chapter 3

DPWM Transceiver Architecture

3.1 DPWM Transmitter Architecture

Previously, transmitters using DPWM and PWM for memory applications were introduced in [16] and [17]. Fig. 3.1 shows the conventional DTC block diagram for falling-edge PWM. The incoming clock first sets the RS latch output to high and generates delayed clock edges through a buffer and a delay chain consisting of M-1 stages. The buffer (BUF) assures a sufficient propagation delay, T_{ref}, for generating the first delayed clock. Based on the transmitted symbol value $a[k]$, the phase selector dynamically selects one of the delayed edges to reset the latch and, equivalently, generates the pulsewidth from T_{ref} to T_{ref} + (M-1)$\triangle T$. In addition, the delayed clocks are obtained from regular phase-locked loop or a delayed-lock loop. The condition $T_{ref} = \triangle T$ is obtained using a five-phase VCO in the PLL design [17]. Fig. 3.1 also depicts the conventional DPWM DTC block diagram. This transmitter utilizes an RS latch incorporating two replica delay circuits to alternatively generate positive and negative pulses. The upper and lower delay circuits control the set and reset cycles of the RS latch. Each delay circuit consists of a buffer to assure the minimum pulsewidth and a multiplexer chain for pulsewidth modulation. Each multiplexer includes an extra gate realized by NOR-AND or NAND-OR gates to contribute to a propagation delay difference, $\triangle T$, between two multiplexer inputs [16]. The transmitter dynamically adjusts signal propagation delay in the multiplexer chain and, consequently, modulates

the pulsewidth of positive and negative pulses. Both of these design approaches present potential problems for a high-speed DTC that must generate low-jitter. First, the T_{ref} is fixed in the design without allowing adaptation to different channel characteristics. Second, longer T_{ref} requires more buffers to increase the minimum delay which increases the power consumption and the jitter generation. Third, these architectures require more delay or multiplexer stages to increase the number of modulation levels. Not only does this impact the highest operating frequency but also raise the bandwidth requirement in the circuit design of phase selector output of PWM DTC and of delay chain input of DPWM DTC.

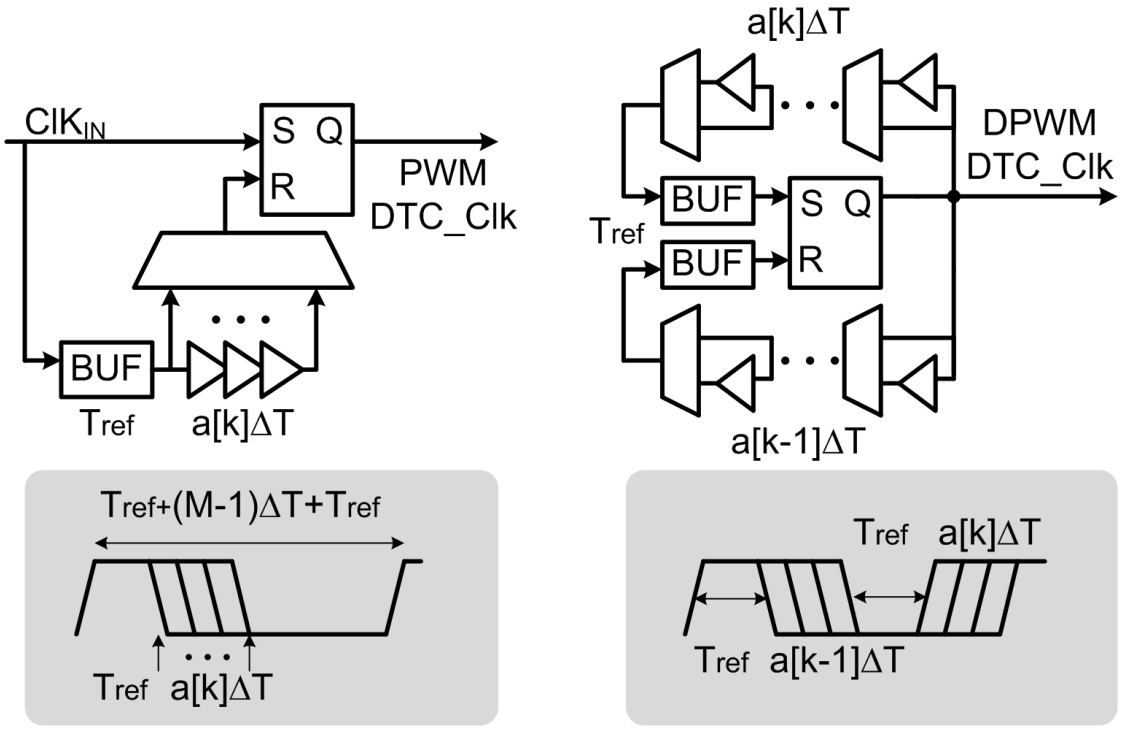


Fig. 3.1: Conventional PWM DTC (left) and DPWM DTC (right).

The proposed DPWM transmitter circuit design focuses on combining the high-speed operation with a low-jitter architecture. The schematic of the proposed DPWM transmitter is shown in Fig. 3.2. It consists of an elastic buffer (EB), a DTC, a multiphase clock generator, and a 50 Ohm driver. Additionally, the chip includes test interfaces for random word generation (PRWG) in the synchronous and plesiochronous clock domains.

The elastic buffer maintains a timing margin between the DPWM plesiochronous domain and synchronous clock domain. The head and tail pointers direct the read and write data access. For DPWM with T_{ref}= 160 ps, the EB must operate up to 6.25 GHz. High-speed pointers are implemented by shift registers incorporating a one-hot coding to replace conventional binary counter. The important constraint with the elastic buffer is the size of the buffer. Depending on how many consecutive identical digits are transmitted, the required buffer size can grow tremendously. For testing the DPWM system, the EB can be circumvented by using two different PRWG generators are provided on chip for testing in the plesiochronous and synchronous clock domains. $Data_SEL$switches testing between different clock domains. For plesiochronous data links, the DPWM transceiver does not require the use of EB and a random DPWM signal is generated by triggering the plesiochronous PRWG (Plesioc PRWG) with rising and falling edges of the DPWM signal. L_CK denotes the DPWM signal transitions. For synchronous data links, the synchronous PRWG (Sync PRWG) is written to the EB by the synchronous clock and read by DPWM clock. Additionally, a 3-bit interface ($Data$[2:0]) provides an external data interface. EB_SELswitches testing between on-chip and off-chip input symbol streams. For 10 Gb/s, the D_CK period is 300 ps (10 GHz/3) since DPWM transmits three bits in one symbol.

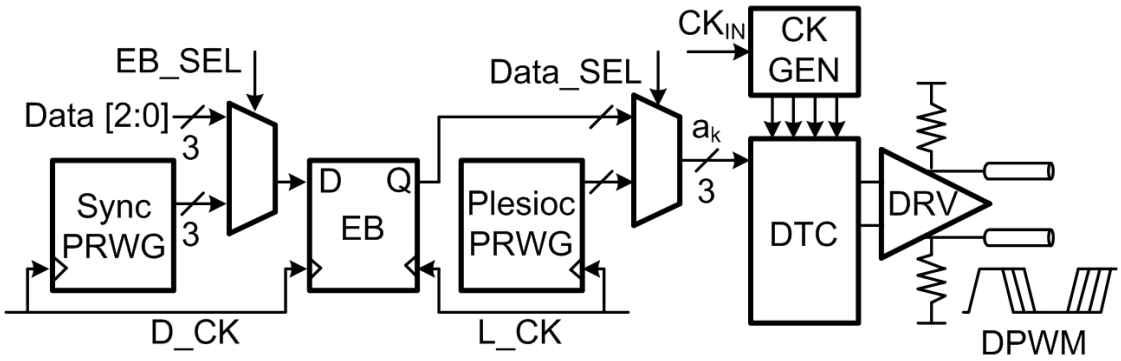


Fig. 3.2: Digital-to-time transmitter architecture and testing configuration

3.2 Digital-to-time Converter

Fig. 3.3 shows the diagram of the proposed DTC circuitry. A digitally programmable input, P, adjusts T_{ref} from 4 to 7$\triangle T$ to adapt to different channel bandwidth characteristics. Therefore, $T_{DPWM}[k]= P\triangle T + a[k]\triangle T$. The integrator records all prior pulsewidth values, i.e. $s_k = \sum(a_k + P)$, and computes a modulo operation to three bits since eight clock phases are utilized in the phase rotator (PR). The DTC uses input digital symbols to dynamically select a phase of a clock to determine the timing transitions of adjacent symbols. Using phase selection instead of delay elements reduces the jitter associated with delay stages, and allows simple implementation of long clock pulses by skipping cycles. Phase jumps among the eight clock phases of the PR are computed by the integrator and controlled by the finite state machine (FSM).

The decoder (DE) determines one of 8 clock phases in the PR to generate the trigger signal (M_CK). M_CK is regulated by a latch that is clocked by the output of a FSM to prevents timing glitches. When a large phase jump caused by a large symbol value occurs, the FSM regulates the PR by disabling the control latch in PR.

For instance, if $a_k + P$ exceeds a threshold TH, the FSM temporarily disables the PR by skipping its input pulses and re-enables it after 8$\triangle T$. This approach to the implementation of the FSM offers the capability for converting the extra delay stages to a state transition control and substantially improves the signal integrity, especially when desiring to extend T_{ref} or to increase the signal level, M. In the disabled state, the divider is not triggered and the pulsewidth is prolonged. Finally, L_CK denotes the regulated M_CK pulses and triggers a frequency divider which alternately generates positive and negative pulsewidths. Using the frequency divider to generate both pulsewidth intervals prevents duty-cycle distortion (DCD) between the positive and negative pulsewidth encoding. The integrator and decoder are also triggered by L_CK. A timing diagram is illustrated in Fig. 3.4 for $T_{ref} = 4\triangle T$ when consecutive zero symbols are transmitted.

An on-chip multiphase clock generator consists of 2 CML DFFs and forms divided-by-four frequency divider as shown in Fig. 3.5. With the matched latch fan

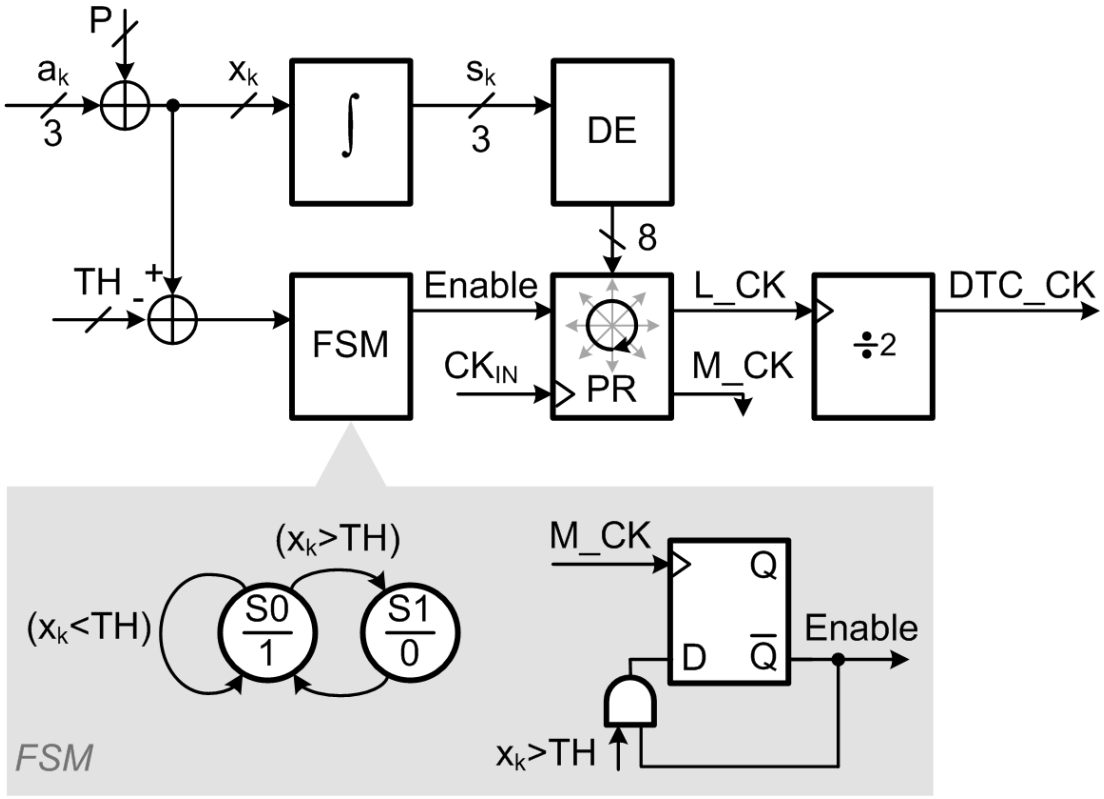


Fig. 3.3: The DTC block diagram and FSM schematic.

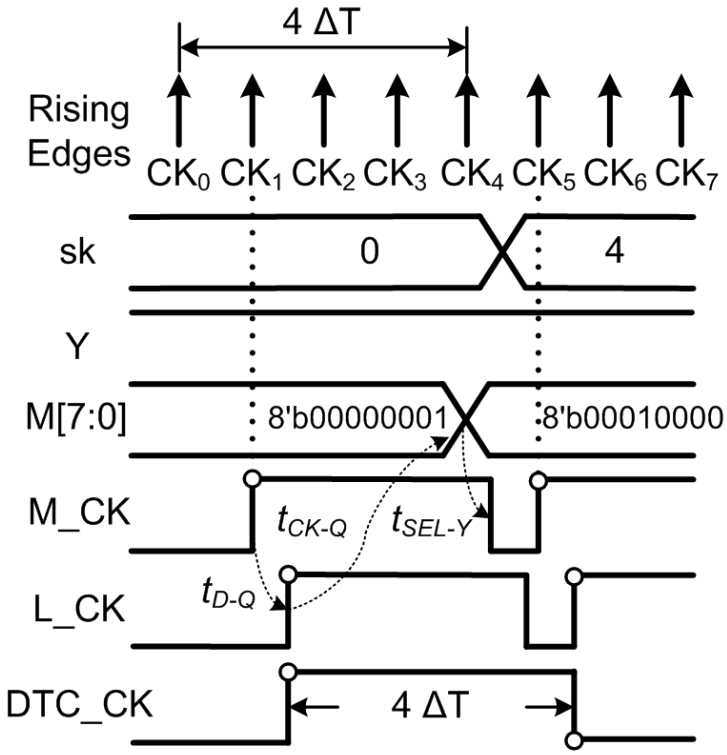


Fig. 3.4: DTC Timing diagram.

outs, quarter-rate differential clocks are sequentially generated to create 8 phases where CK4-CK7 are inverted phases of CK0- CK3. Notably, the jitter performance of a high-speed DTC based on the multiphase generator will be limited to the jitter of the reference clock rather than a chain of delay stages. The divide-by-4 circuitry for the eight multiphase clock generations can be replaced by regular PLL and DLL when clock generation circuitry is integrated in transmitter.

Because the DTC must map the binary word into discrete time intervals over short time period, the DTC circuitry requires a short critical timing path to convert each data symbol to a pulsewidth at a data rate of 10 Gb/s. The critical path determines the shortest achievable T_{ref} and, consequently, the maximum data rate. The critical path consists of three propagation delays through t_{D-Q} of latch, t_{CK-Q} of decoder and t_{SEL-Y} of MUX. CML gates are introduced where timing and jitter are critical, namely for the MUX, latch, divider, and FSM. Other DTC circuits are implemented in standard CMOS logic to reduce power consumption. Simulation of the extracted circuits in a 45-nm CMOS SOI process predicts t_{D-Q}= 10 ps, t_{CK-Q}= 105 ps and t_{SEL-Y}= 15 ps. Note that t_{CK-Q} includes delays of a CML-to-CMOS converter and 8-bit register.

$$t_{critical\,path} = t_{D-Q} + t_{CK-Q} + t_{SEL-Y}. \tag{3.1}$$

This critical path requires T_{ref} larger than 130ps (3.25 $\triangle T$) and therefore P is at least 4. Hence, the bit rate is constrained to 10 Gb/s for the DTC. Conversion from CML-to-CMOS potentially introduces jitter into the loop but facilitates standard-cell implementation of an 8b DFF and reduces the static power consumption. DTC trades jitter performance with power consumption in this building block. Fig. 3.6 depicts the schematic of MUX and CML-to-CMOS converter. Therefore, a critical feature of this architecture is the need for an advanced CMOS process to provide devices which can switch fast enough to generate the high-speed timing decisions required to generate a DPWM signal.

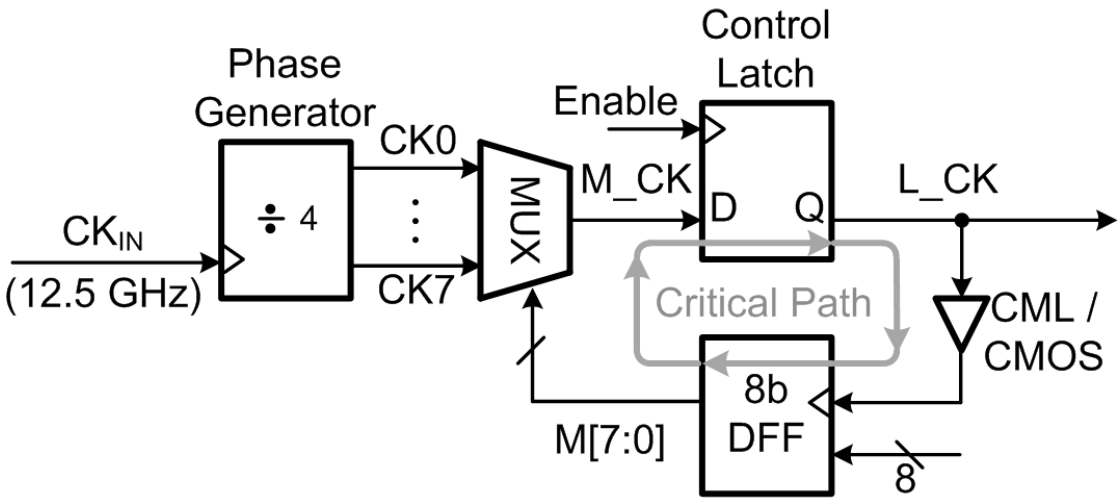


Fig. 3.5: Phase rotator and critical path for digital-to-time conversion.

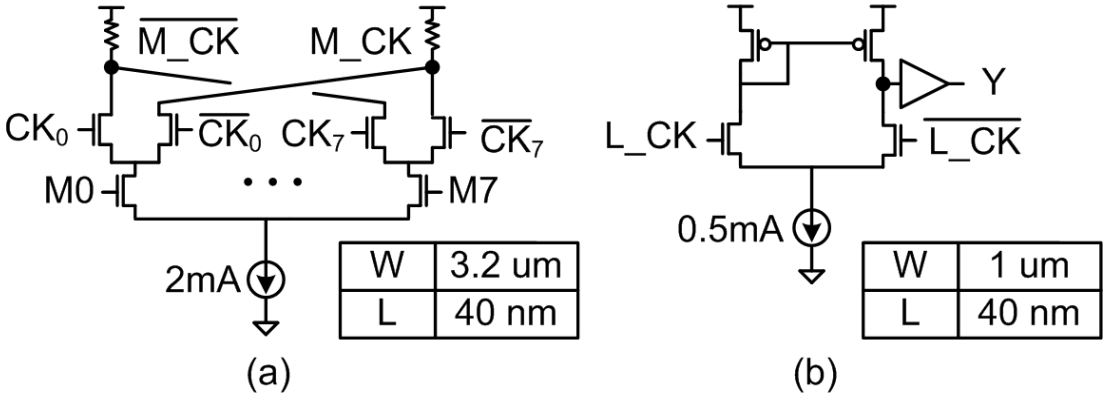


Fig. 3.6: 8-to-1 phase selector and CML-to-CMOS converter.

3.3 Channel Bandwidth Adaptation and Low Jitter Control

Two main benefits are outlined for this architecture. First, the proposed DTC architecture allows a programmable T_{ref} by incorporating a static parameter, P from 4 to 7. If T_{ref} is adjusted from $4\triangle T$ through $7\triangle T$ (or T_{ref} = 160, 200, 240, and 280 ps), then the bit rates are 10, 8.8, 7.9 and 7.1 Gb/s and the corresponding channel bandwidth requirement is 3.1, 2.5, 2.1 and 1.8 GHz (or Channel BW = 0.5/160ps, 0.5/200ps, 0.5/240ps, and 0.5/280ps), shown in Fig. 3.7.

Second, the architecture features low random and deterministic jitter generation. Jitter generation due to random jitter is minimized by the use of the multiple clock phases. For instance, to transmit 8-DPWM with T_{ref} of $7\triangle T$, a DPWM DTC requires a maximum pulsewidth generation of $[(8-1)+7]\triangle T$. For a conventional PWM and DPWM DTCs, fourteen delay stages are required. However, the proposed transmitter only uses eight clock phases and the potential jitter penalties that were previously described are avoided.

However, this architecture also limits the generation of DCD through the use of the final divider. In Fig. 3.1, the conventional DPWM DTC exhibits DCD in the absence of supply noise. Fig. 3.8 simulates the DCD when $T_{ref} = 4\triangle T$ for conventional and proposed DPWM DTCs in a 45-nm CMOS SOI process. The conventional DPWM DTC presents a peak DCD of 5.5 ps between positive and negative pulsewidth in the beginning of symbol transmission, caused by the propagation delay asymmetry between set and reset paths of RS-Latch. The positive pulses are longer than the negative pulses within four-hundred symbol transmissions when the nominal pulsewidth of T_{ref} is $4\triangle T$. The positive pulses gradually shrink afterwards due to the rise/fall time imbalance in the replica delay circuits. The pulsewidth distortion incurs timing jitter as well as degrades the achievable timing resolution. For the proposed DTC, the initial static DCD offset induced by RS-Latch signal paths is mitigated by using the frequency divider at the output. In addition, the proposed architecture utilizes the multiphase periodic clocks and eliminates the dynamic DCD contributed by the delay circuits.

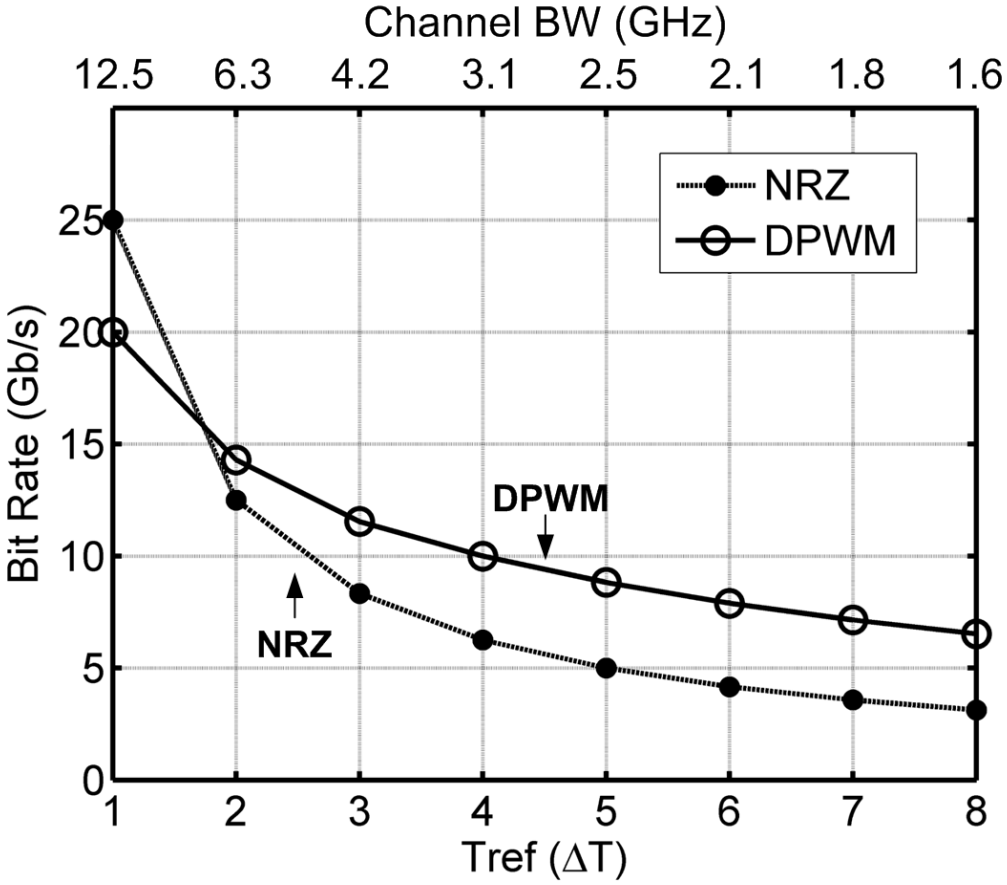


Fig. 3.7: Bit rate and Nyquist frequency versus T_{ref} ($\triangle T = 40$ ps)

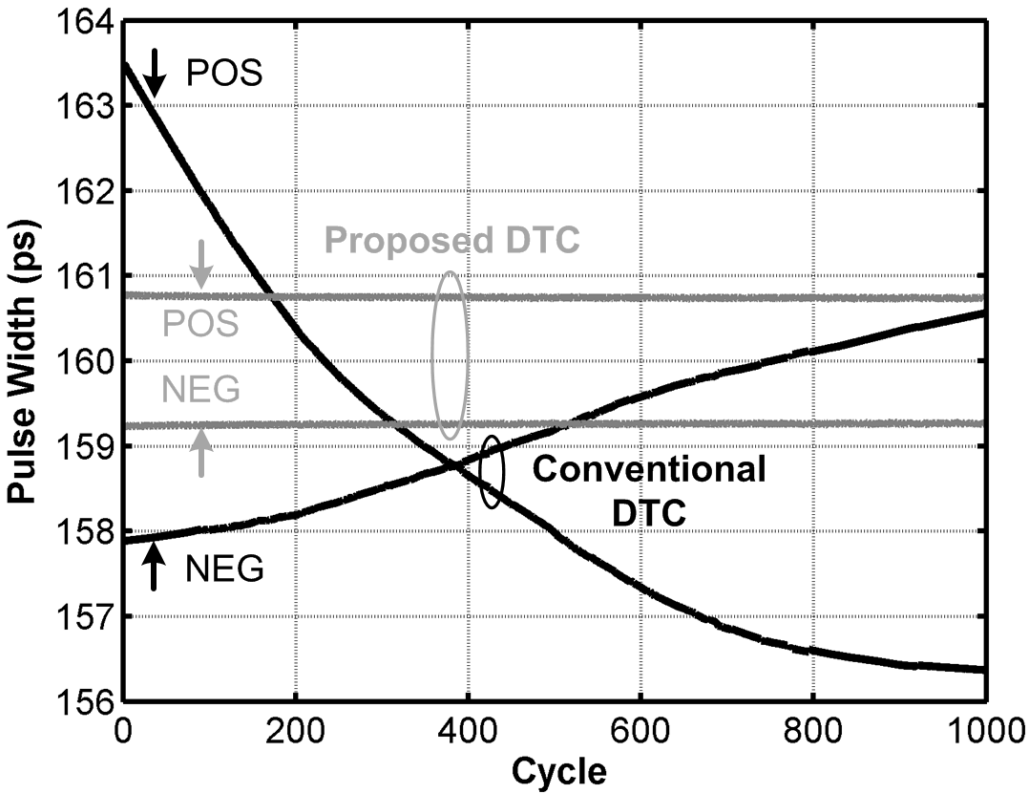


Fig. 3.8: Simulated duty cycle distortion of DPWM DTCs ($T_{DPWM} = 4\triangle T$, $\triangle T$=40 ps)

3.4 Transmitter Signal-to-Noise Ratio

The timing resolution $\triangle T$ is degraded by the deterministic jitter penalties from transmitter circuit. In the presence of deterministic jitter, the SNR from (2.9) should satisfy

$$SNR_{TX} = (\triangle T - DJ_{PP,TX})/RJ_{RMS}. \tag{3.2}$$

where $DJ_{PP,TX}$ reflects the peak-to-peak deterministic jitter contributed by the DTC circuit.

Fig. 3.9 compares the possible BER as a function of the random jitter for a timing resolution of $\triangle T = 40ps$ in the presence of the simulated DCD contributions presented in Fig. 3.8. The DCD reduces the transmitted timing resolution and degrades the BER tolerance to RJ. For a given BER, the proposed DTC circuitry tolerates a RJ_{RMS} of 2.73 ps (38.4 ps/14) while the conventional DTC circuitry tolerates a RJ_{RMS} of 2.45 ps (34.5 ps/14). While this analysis has been limited to the transmitter, additional sources of deterministic jitter due to the channel response such as data-dependent jitter will further degrade the tolerance to RJ at the receiver. The conventional DTC presents a reduced RJ tolerance of 14% compared to ideal tolerance, while in the proposed DTC the tolerance is reduced by only 4%.

3.5 DPWM Receiver Architecture

The receiver is based on a TDC which has previously been utilized in measurement systems, e.g. logic analyzers, time-of-flight detection and jitter emulators. TDC designs are evaluated against several performances metrics such as the timing resolution, linearity, complexity, range, and conversion rate. Vernier-delay-line architectures are based on propagation delay differences in buffers to achieve timing resolution under a gate delay [19, 20]. A cyclic vernier-delay-line TDC converts the linear delay elements into a periodic relationship and substantially reduces the area penalty [21, 22]. A TDC using periodic multiphase sampling clocks eliminates the requirement for a delay line [23]. Here the TDC must be capable of

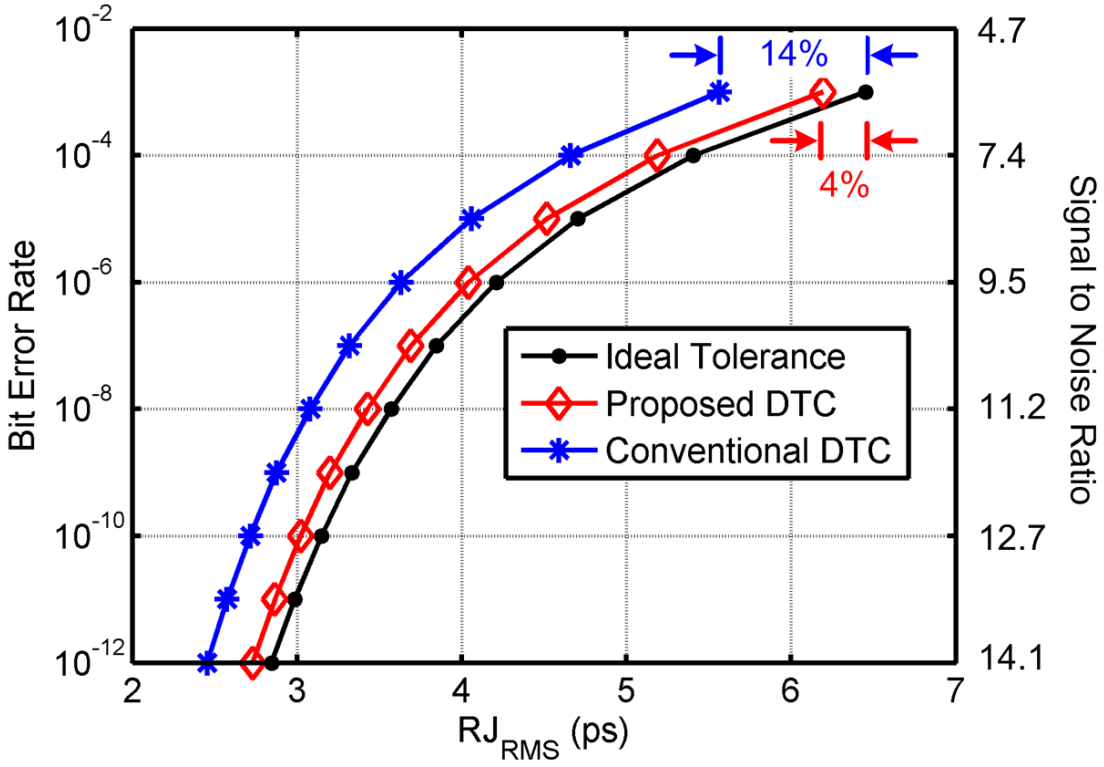


Fig. 3.9: Simulated BER versus the tolerable random jitter with presence of DCD.

high-speed operation to recover the 40 ps ($\triangle T$) symbol intervals with low additive receiver jitter.

One important feature is the DPWM RX demodulates the symbol in time domain rather than in voltage domain. Therefore, DPWM RX front end differentiates two signal voltages and resembles a NRZ RX front end. The proposed receiver employs a multiphase-based TDC for DPWM demodulation because it provides high conversion rate, sufficient timing resolution, and low power consumption. Fig. 3.10 depicts the proposed DPWM receiver. The time-interleaved architecture includes a 50 Ohm driver, dual TDCs, a data switch and an EB. TDC_{POS} and TDC_{NEG} perform positive and negative pulsewidth conversions, respectively. Based on the current DPWM signal polarity, the switch alternatively fetches the conversion results from TDC_{POS} or TDC_{NEG} to the buffer. The elastic buffer provides the interface between the plesiochronous DPWM signal domain and the local synchronous clock domain. TDC_{POS} utilizes two slicer-integrator pairs sampled by the differential sampling clocks. Each slicer-integrator pair determines the logic level of current symbol stream and records the conversion results. A CML-to-CMOS converter converts the slicer logic decision to rail-to-rail levels. The integrator and subtractor are implemented by digital standard cell logic. When the DPWM signal switches from high to low, the summation of the integrator outputs reflects the positive pulsewidth in terms of the timing resolution, $\triangle T$. The output of the integrators are held to assure the timing constraints of digital logic while the TDC is resetting for the next rising edge of DPWM signal. The write clock of EB, L_CK triggers upon every transition of DPWM signal and the $Dump$ signal detects the falling-edge transitions.

A timing diagram is illustrated in Fig. 3.11 to show the receiver timing. The integrator utilizes shift registers for high-speed accumulation. The proposed TDC circuits operates above a conversion rate of 3.1 GHz ($8\triangle T$), enables the timing resolution of 40 ps, and provides the measurement range of 4 to $14\triangle T$. The programmability of minimum pulsewidth, P, in the transmitter is also featured in the receiver. The receiver architecture implemented here uses a half-rate clock with 80 ps period but also supports 1/4- and 1/8-rate sampling clocks by increasing the

number of slicer-integrator pair. Performance tradeoffs between power consumption and mismatches in higher-order multiphase system are discussed in [24, 25]. The proposed receiver retains flexibility for different sampling architectures. This receiver focuses on verifying the operation of a DPWM receiver and ideally phase interpolator should be incorporated to adjust the sampling clock for the optimal BER performance over different channels and PVT variations.

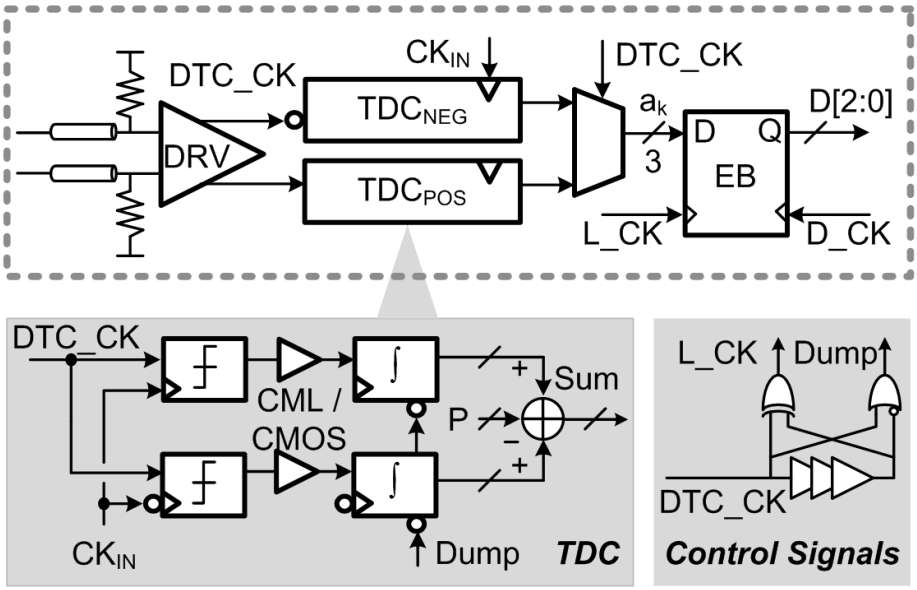


Fig. 3.10: TDC receiver block diagram.

3.6 DPWM Transceiver Measurements

The transmitter and receiver are shown in the chip microphotographs in Fig. 3.12. The area of the transmitter and receiver are roughly 0.9 mm by 1.1 mm including the pads. The active area of the transmitter is 93x94 um^2 while the area of the receiver is 218x160 um^2. A breakdown of the power consumption for the transmitter and receiver is provided in Table 3.1. The power consumption of DTC is 30 mW and driver is 14 mW, respectively, for a total transmitter power consumption of 44 mW. Any choice of T_{ref} from 4 to 7 $\triangle T$ exhibits comparable power consumption but the bit varies from 10 to 7.1 Gb/s, respectively. The

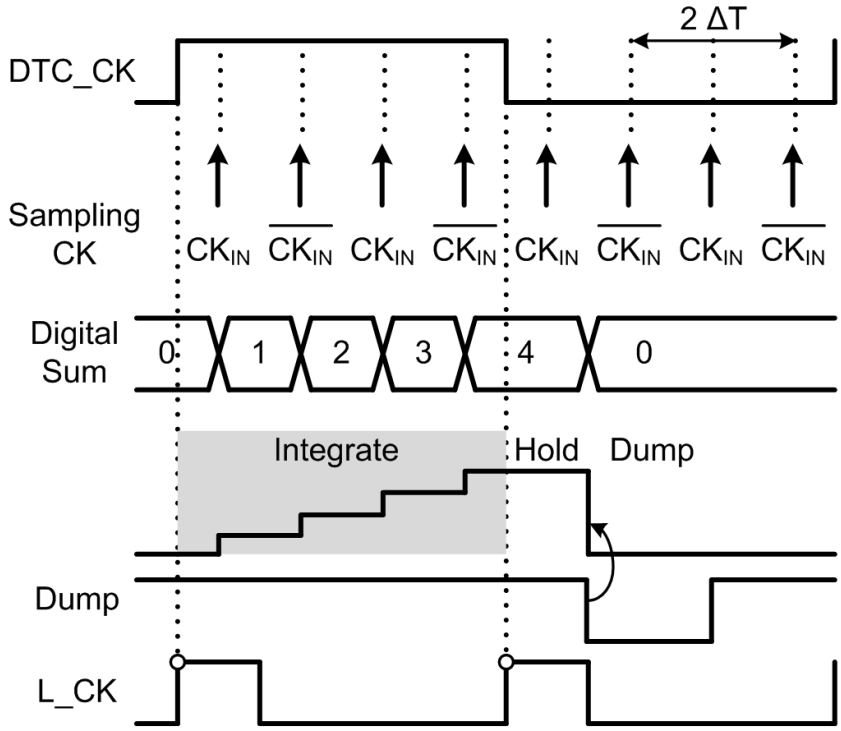


Fig. 3.11: TDC timing diagram.

power consumption of the receiver circuitry is 38 mW. The clock circuitry for the multiphase generation and sampling adds 25 mW. Therefore, the total power consumption is 107 mW and the transceiver energy efficiency varies from 10.7 pJ/b at 10 Gb/s to 14.9 pJ/bit at 7.1 Gb/s. The power consumption remains basically unchanged at different data rates due to the use of CML logic for low jitter.

The DPWM transceiver was measured with probing and the voltage supply was applied through a DC Tungsten probe. During the measurements, the probe resistance was found to be around 1 Ohm and the supply was raised to 1.2V to overcome the IR drop to the integrated circuit.

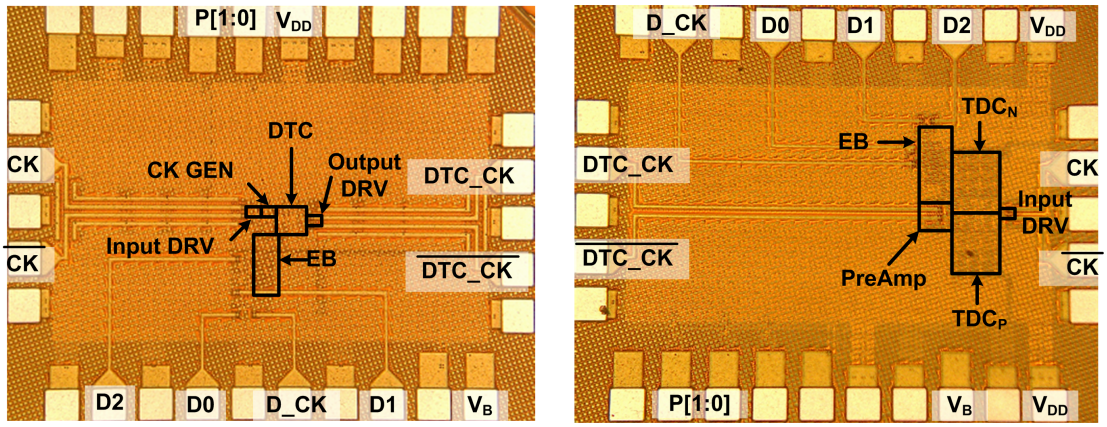


Fig. 3.12: Chip microphotograph of the transmitter (left) and receiver (right) circuits

3.7 Transmitter Performance

The PSD and integrated power spectrum of the modulated DPWM signal is described previously. The DPWM scheme is measured in the frequency and time domain. An on-chip PRWG-7 is used for symbol generation for transmitter measurements. For $T_{ref} = 4$ and $7\triangle T$, 77% of signal power occupies a bandwidth of 3.1 and 1.8 GHz, respectively. The measured PSD verifies the simulated PSD and demonstrates energy concentrations for four T_{ref} cases in Fig. 3.13.

The data eyes of the transmitter are plotted in Fig. 3.14 for 4 to 7 $\triangle T$. Since $T_{DPWM}[k]= P\triangle T + a[k]\triangle T$, the eye diagram is plotted with integer

Table 3.1: DPWM transmitter and receiver performance summary

Timing Resolution, $\triangle T$	40 ps
Programmable T_{ref}	4 to 7
Data Rate	10, 8.8, 7.9 and 7.1 Gb/s for T_{ref} = 4 to 7 $\triangle T$
Technology	45nm CMOS SOI
Supply Voltage	1.2V
DTC Driver Transmitter Total	30 mW 14 mW 44 mW
TDC Driver Receiver Total	27 mW 11 mW 38 mW
TX Clock Generator/Buffer RX Clock Buffer	18 mW 7 mW
Transceiver Total	107 mW
Energy per Bit	10.7-14.9 pJ/bit for T_{ref} = 4 to 7 $\triangle T$
Tx Output Jitter	1.3 ps
RX Input Sensitivity	50 mV/ 0.7 UI (Simulated) 200 mV/ 0.625 UI (Measured)

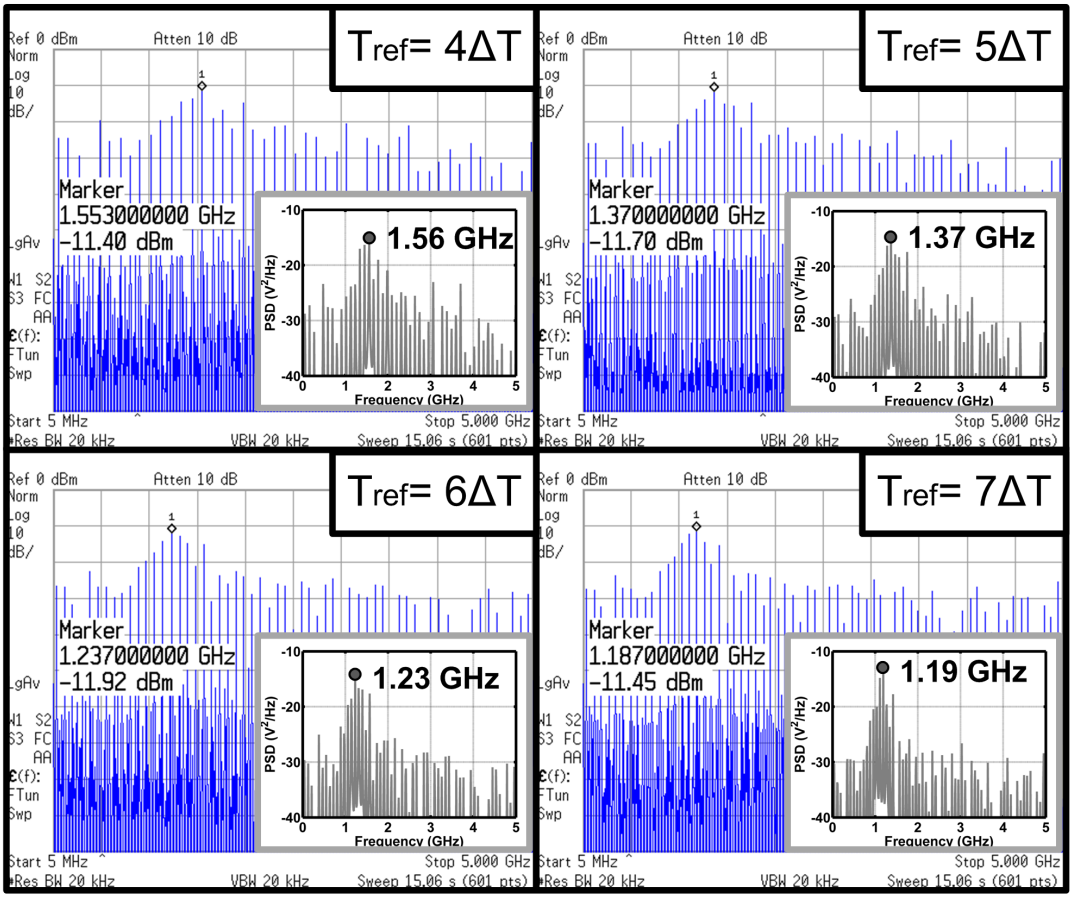


Fig. 3.13: Simulated PSD (gray) and measured PSD (blue) using T_{ref} = 4 to 7 $\triangle T$.

multiples of $\triangle T$. While DPWM eye diagram transitions are recorded over a unit interval of $\triangle T$ in the eye diagram, each transmitted pulsewidth lasts for at least T_{ref}. Because PWM/DPWM modulates the pulsewidth by $\triangle T$, it is straightforward to examine the signal integrity by looking into the timing resolution. In fact, when overlapping the PWM waveform by $\triangle T$, PWM eye diagram is similar to Fig. 3.14.

Under all conditions, the rms output timing jitter is less than 1.3 ps. The DTC is driven by the N4903 BERT 12.5 Gb/s clock outputs. For $T_{ref} = 4\triangle T$, the output TX RMS jitter ($J_{RMS,TX}$) and sampling clock RMS jitter ($J_{RMS,CK}$) measure 1.3 ps and 0.9 ps, respectively. The on-chip DTC circuitry jitter ($J_{RMS,DTC}$) induced by DCD, thermal noise, and power-supply noise can be calculated as:

$$J_{RMS,TX} = \sqrt{J_{RMS,CK}^2 + J_{RMS,DTC}^2}. \tag{3.3}$$

The integrated $J_{RMS,DTC}$ calculates within 0.94 ps for all T_{ref} cases. The measurement verifies the fine jitter control of new DTC design compared to previous DTC arts when extending the T_{ref} as described. Bathtub curves for $T_{ref} =$ 160 ps, which corresponds to 10 Gb/s, are shown in Fig. 3.15. The eye openings are 31 ps and 313 mV at a BER of 10^{-12} at the output of the transmitter. The EB operating frequency measures above 3.1 GHz ($2T_{ref}$) and can be incorporated in synchronous data links. According to the previous analysis, the actual transmitter measures a RJ tolerance of 2.2 ps (31 ps/14) at a BER of 10^{-12}.

3.8 Receiver Performance

The minimum timing resolution of time-to-digital converter provides an additional limit on the link performance. The overall timing SNR depends on a combination of random and deterministic jitter sources resulting from thermal noise, power-supply noise, channel response, mismatch of devices in the RX and TX, and the actual resolution of the TDC. For a BER of 10^{-12}, the total jitter must be less than the minimum timing resolution.

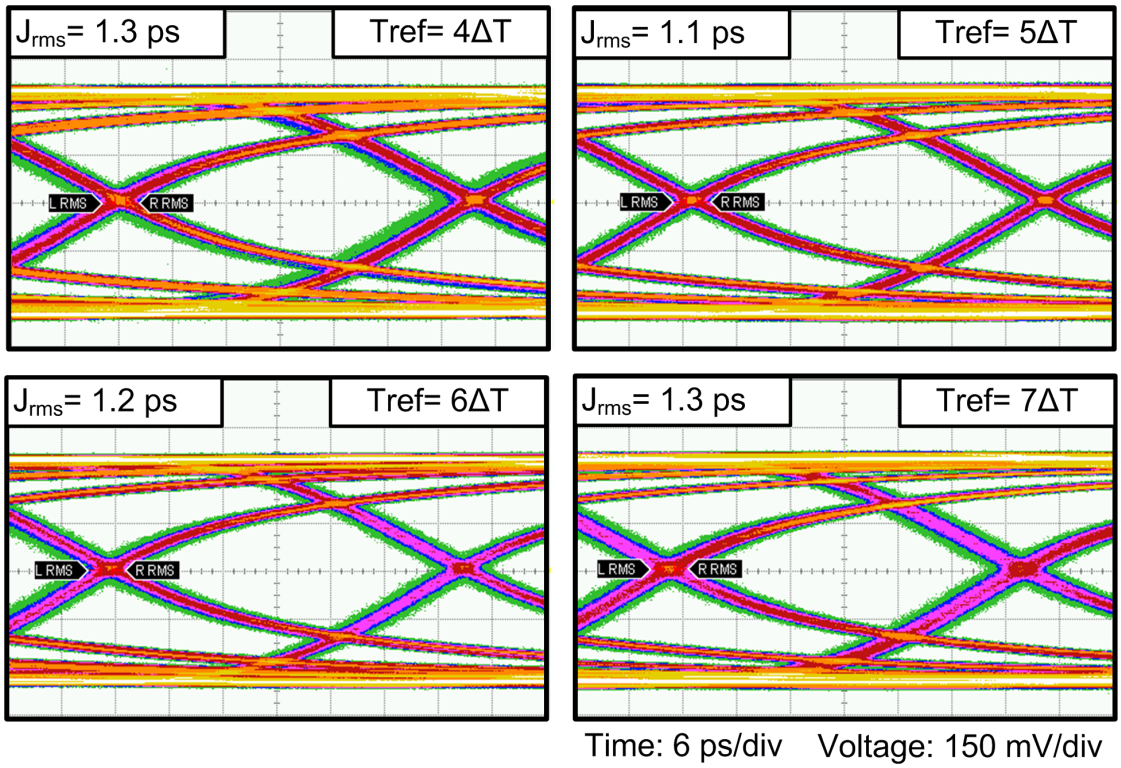


Fig. 3.14: Measured transmitter eyes of 8-DPWM of $T_{ref} = 4$ to 7 $\triangle T$.

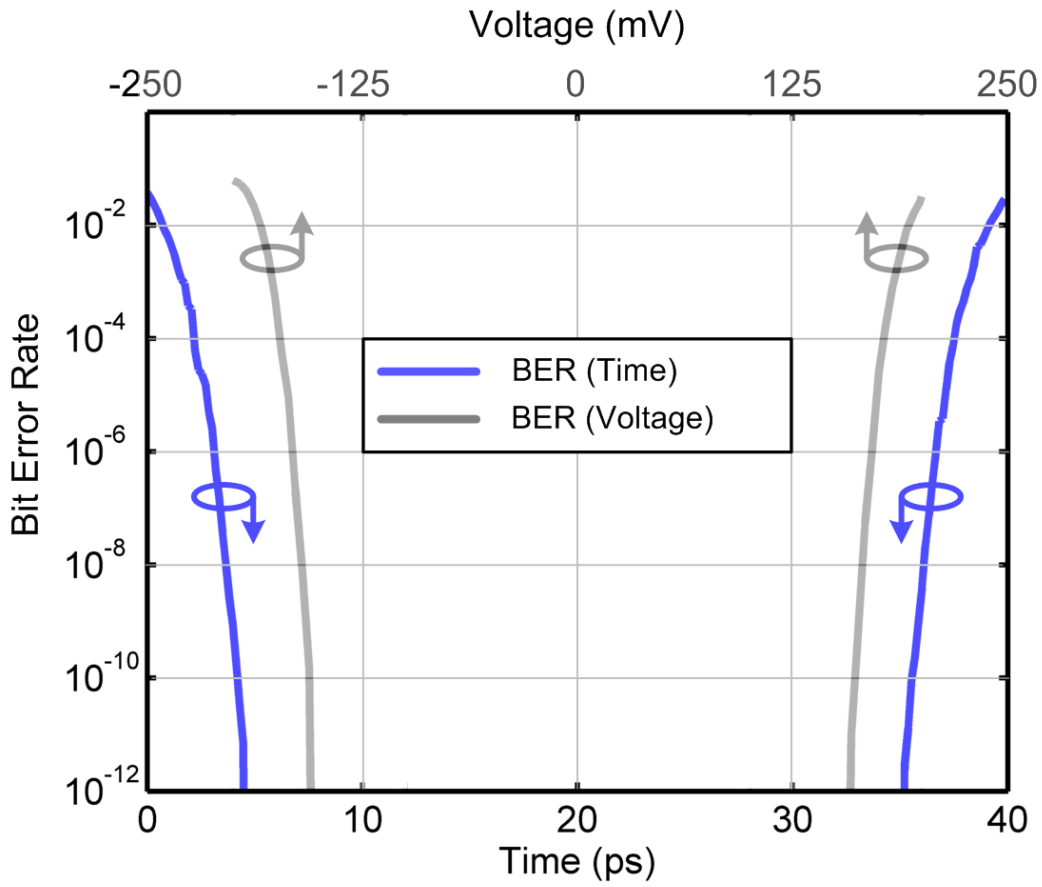


Fig. 3.15: Measured transmitter BER bathtub curves of sampling time and sampling voltage.

Fig. 3.16 depicts the simulated and measured timing margins versus different input swing conditions. The achievable performance of SOI circuitry implementation is simulated and presents eye opening degradation of ($DJ_{PP,TDC}$) from ideal opening. The simulated eye opening stays above 30 ps (0.75 UI) for the data swing larger than 50 mV. The actual RX sensitivity of 10^{-12} BER is measured versus data swing. The receiver measures the sampling phase range of 25 ps (0.625 UI) with 200 mV input swing. The data jitter and sampling clock jitter of N4903A BERT incur additional jitter ($J_{PP,BERT}$) deviates the performance from the simulated BER curve. $J_{PP,BERT}$ denotes the integrated peak-to-peak jitter of RJ and DJ from BERT. In the receiver test setup, $J_{PP,BERT}$ also represents $DJ_{PP,TX}$ in (3.2). The simulated eye opening imposed by $J_{PP,BERT}$ is compared. Phase mismatch from cables and connectors between differential data channels form the other jitter ($J_{PP,CH}$). Although $J_{PP,CH}$ is dominated by the DJ due to channel mismatch, an insignificant channel RJ in RF cable is also included into $J_{PP,CH}$. Note these jitter sources are uncorrelated and the integrated peak-to-peak jitter is derived as:

$$J_{pp} = DJ_{PP,TDC} + J_{PP,BERT} + J_{PP,CH}. \tag{3.4}$$

$J_{PP,JBERT}$ measures offsets within 0.2 UI when data swing is above 200 mV. Significant $J_{PP,BERT}$ is observed for data swing below 200 mV and unsuitable for BER measurements. The BER bathtub curves for T_{ref} = 160 ps (10 Gb/s) are shown in Fig. 3.17. The measured eye opening is 25 ps (0.625 UI) at a BER less than 10^{-12} given an input data swing of 200mV. The recovered bit streams for T_{ref} = 4 $\triangle T$ and T_{ref} = 7 $\triangle T$ are verified by BER tests.

Fig. 3.18 predicts the tolerable random jitter versus corresponding BER, assuming the RJ follows a Gaussian distribution. The theoretical and simulated RJ tolerances are compared to show the relative penalty of the implemented SOI circuitry. The estimated RJ tolerance presents the simulated tolerance curve affected by $J_{PP,BERT}$. The measured tolerance denotes the tolerable RJ calculated from the BER measurements in Fig. 3.17. The estimated RJ tolerance matches the measured tolerance. In Fig. 3.17, the timing margin of BER less than 10^{-12}

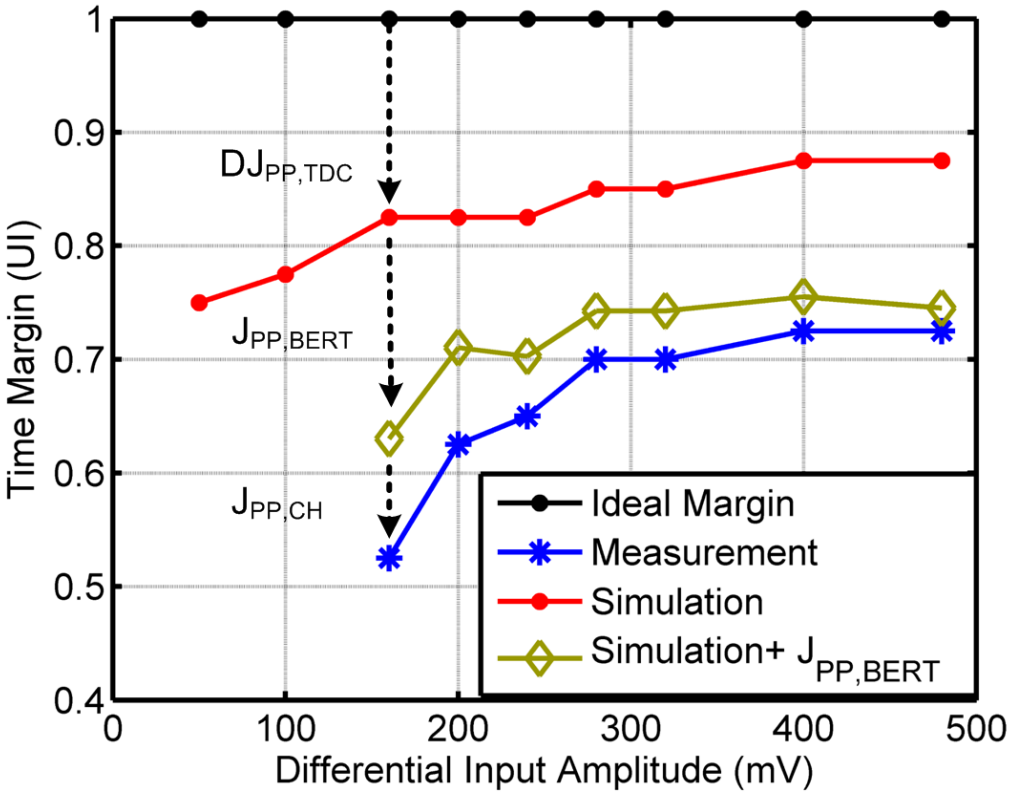


Fig. 3.16: RX time margin of BER 10^{-12} versus the signal swing.

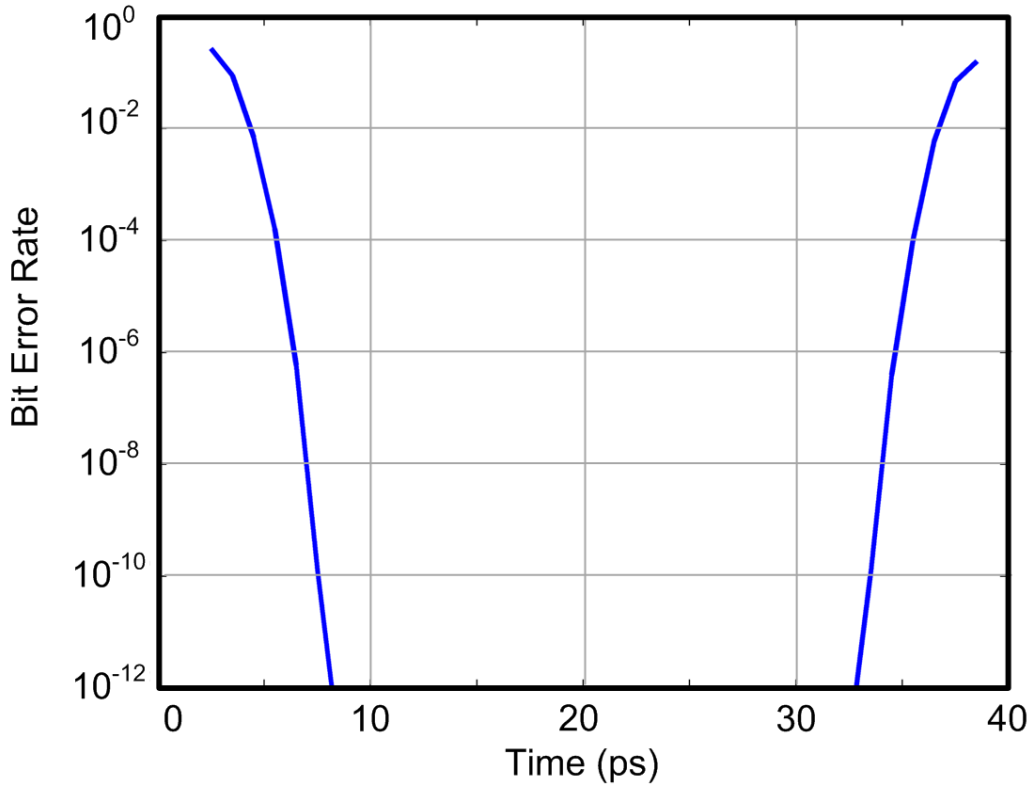


Fig. 3.17: Measured bathtub curve of sampling time of DPWM RX with the input swing of 200mV.

measures 25 ps and translates to a tolerable random jitter of 1.78 ps (25 ps/14). The predicted BER is under 10^{-12} at 1.78-ps rms jitter and degrades rapidly for larger rms jitter. Estimating the channel jitter is important to determining the minimum timing resolution for the DPWM system. More jitter implies a larger timing resolution and reduced bit rate as well as decides the choices of M.

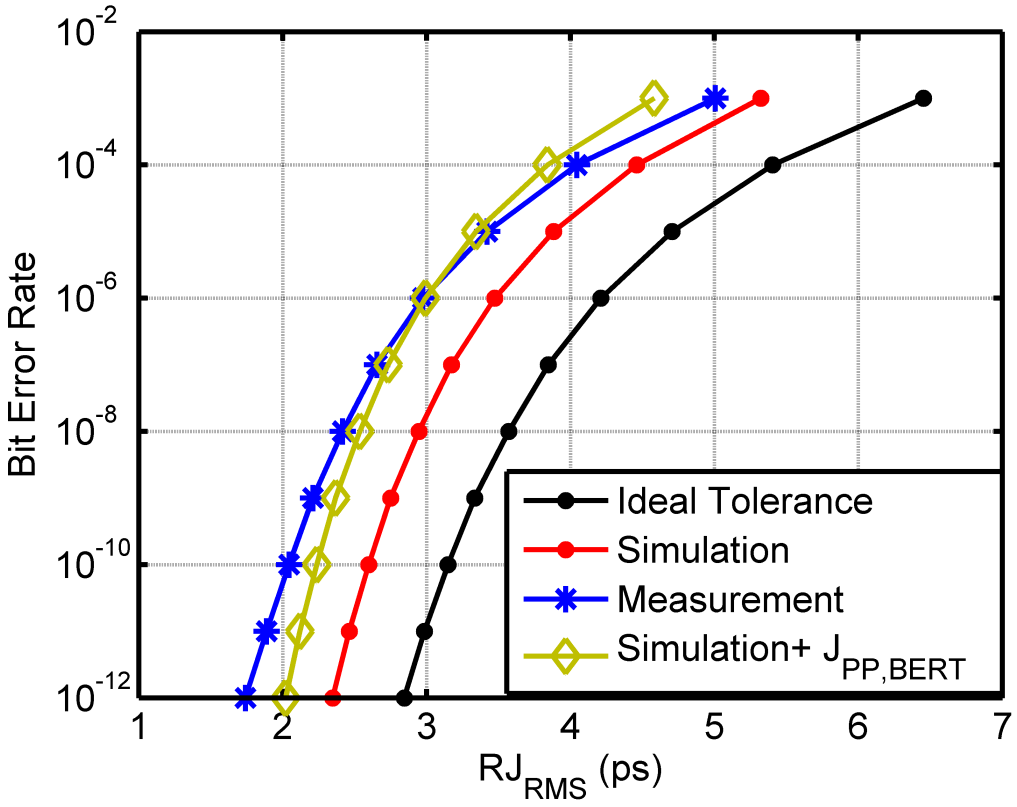


Fig. 3.18: BER versus the tolerable random jitter when data swing is 200 mV.

3.9 Band-Limited Channel

Fig. 3.19 demonstrates the frequency dependent loss of a PCB channel emulator for the DDR channels discussed in [2], [3], [7] using a standard lossy FR4 material. The main channel/stubs were 800 mil long and the gap was 200 mil long. The channel emulator includes two drops that can be populated or left unpopulated. When the second slave is unpopulated, the insertion loss from the

controller to the first module exhibits the sharp frequency rolloff around 5 GHz. Unlike typical lossy channels, the frequency response presents a notch characteristic due to signal reflection [2]. According to the previous analysis, DPWM should allow more eye opening under conditions with sharp channel rolloff at the Nyquist frequency of the NRZ signal. Fig. 3.20 verifies the signal integrity using NRZ and DPWM at different bit rates using $T_{ref} = 7$ to 4 $\triangle T$. Compared to DPWM, the NRZ presents superior eye quality at lower bit rates and indicates significant eye closure at higher bit rates. However, the DPWM data eye is open and demonstrates an eye height and width are 95 mV and 14 ps of 10^{-12} BER at 10 Gb/s, respectively. BER bathtub curves for 10^{-12} are measured using the BERT and recorded to specify the time/voltage margins. Fig. 3.21 depicts the eye diagrams of 7.1 Gb/s and 10 Gb/s using NRZ and DPWM. This emulation demonstrates that, with increasing rolloff in the frequency response, DPWM becomes a potential alternative to NRZ.

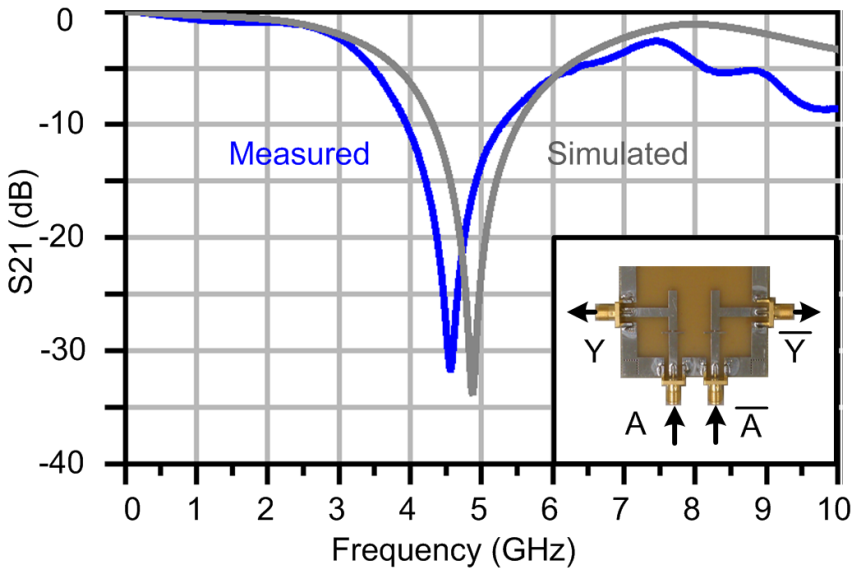


Fig. 3.19: Demonstrated channel with the sharp frequency rolloff.

Depending on design topology, channel difficulty and equalization complexity, the NRZ energy efficiency varies with a complicated number of parameters. At around 7 Gb/s, NRZ presents a energy efficiency of 2.2 pJ/bit using a receiver source-degenerated amplifier in [26]. When using feedfoward equalizer (FFE) /de-

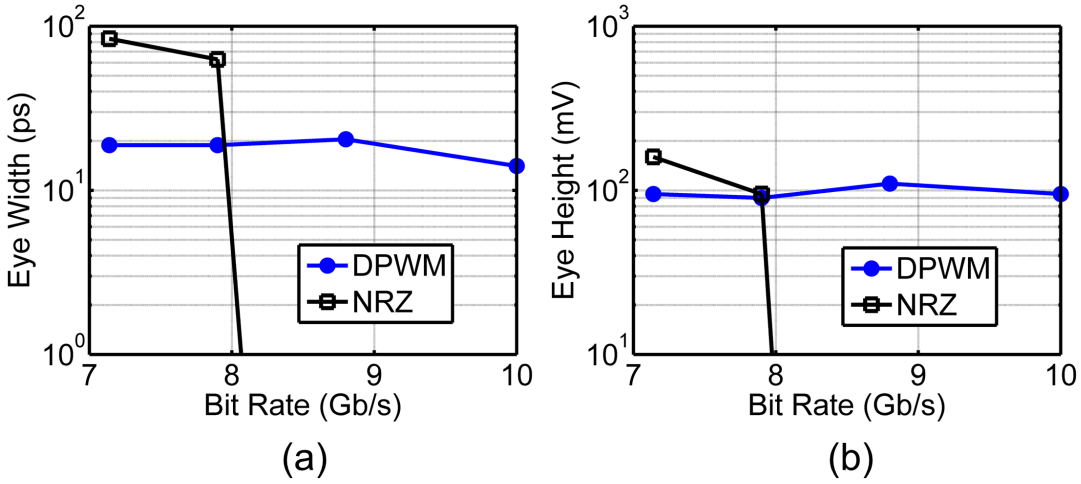


Fig. 3.20: Measured eye width and height of 10^{-12} BER for NRZ (black) and DPWM (blue) through the channel.

cision feedback equalizer (DFE) to combat more difficult channels, the energy efficiencies of 38 and 45 pJ/bit are reported in [27] and [28], respectively. At around 10 Gb/s, NRZ presents an energy efficiency of 13 pJ/bit at receiver by introducing an enhanced equalization concept of source degenerated amplifier [29]. When utilizing FFE/DFE, the transceiver energy efficiencies of 30 and 31 pJ/bit are reported in [30] and [31], respectively. Although both NRZ/DPWM can operate at low bit rates, NRZ should be the first consideration at low bit rates because of its hardware simplicity compared to multilevel signaling. At higher bit rates, DPWM outperforms NRZ in the channels with sharp frequency rolloffs.

The performance of the proposed transceiver is compared against prior PWM/DPWM circuit demonstrations in Table 3.2. While the CMOS SOI process clearly offers substantial (10X) data rate improvements, the proposed architecture is also substantially different from the prior work and has important advantages for limiting deterministic jitter generation in 10 Gb/s signals. The data rate of the proposed DPWM scheme was found to be limited by the critical path timing in the DPWM transmitter as well as the fundamental contributions to random jitter from the transmitter, channel, and the receiver. Additional reductions in power consumption could be realized through the extensive use of standard cell CMOS logic in timing blocks where CML was chosen to limit jitter generation.

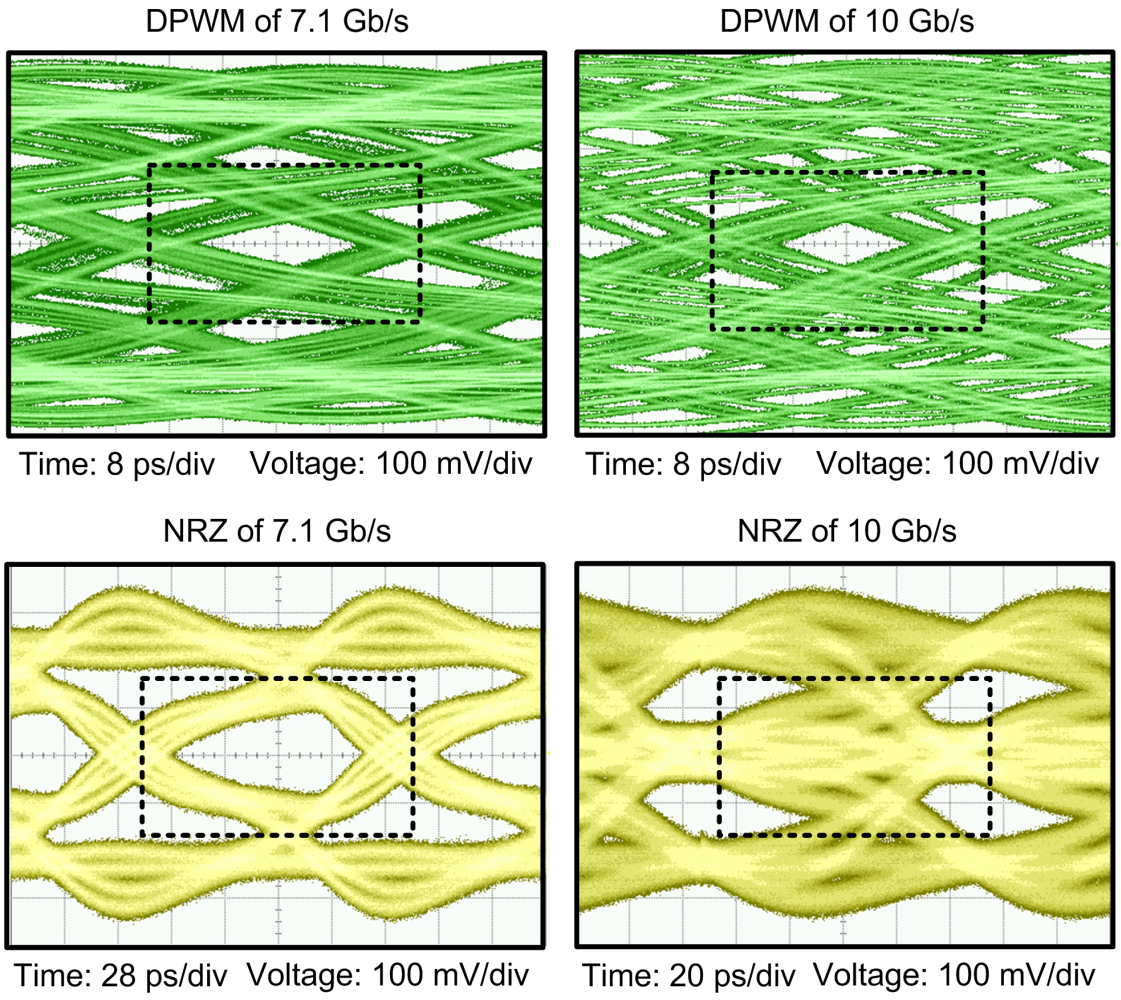


Fig. 3.21: Measured eye diagrams of DPWM (top) and NRZ (bottom) after the channel. The width of the measurement windows are two UI, and the dashed boxes indicate one UI and one-half signal swing.

The dissertation author would like to acknowledge Prof. Buckwalter for his revision of this chapter. This chapter, in full, is a reprint of the material as it appears in IEEE Transactions on Circuits and Systems: I - Regular Papers, 2013, Wei Wang; James F. Buckwalter. The dissertation author was the primary investigator and author of this paper.

Table 3.2: PWM/DPWM transceiver performance comparison

	This Work	JSSC96 [16]	JSSC01 [17]	TIM08 [32]
Modulation	DPWM	DPWM	PWM	PWM / PAM
Supply V.	1.2	3	2.5	1.8 / 3
Technology	45nm CMOS SOI	0.35um CMOS	0.25um CMOS	0.18um CMOS
Timing Resolution	40 ps	400 ps	1 ns	571 ps
Data Rate	10 Gb/s	1 Gb/s	400 Mb/s	1 Gb/s
Power Dissipation	107 mW	N/A	48 mW	112 mW
Energy per Bit	10.7 pJ/bit	N/A	121 pJ/bit	112 pJ/bit
BER	10^{-12}	N/A	N/A	10^{-12}
TX Area	93x94 um^2	N/A	823x481 um^2	1.65x1.4 mm^2 in total
RX Area	218x160 um^2	N/A	678x338 um^2	

Chapter 4

DPWM Signaling for Synchronous Data Links

4.1 Design Issues of frequency drift

A DPWM waveform is shown in Fig. 4.1. DPWM encodes $log_2 M$ information bits representing a symbol $a[k]$ into both positive and negative pulsewidth, where M denotes the total modulation levels. If $a[k]$ takes a value between 0 to $M-1$, the period of the DPWM pulsewidth is

$$T_{DPWM,p/n}[k] = T_{ref} + a[k]\triangle T, \tag{4.1}$$

where T_{ref} is the minimum pulsewidth and $\triangle T$ is the timing resolution for pulsewidth modulation. Longer T_{ref} condenses the signal power to lower frequencies which can be beneficial in bandwidth-limited channels. While T_{ref} should be chosen to satisfy the channel bandwidth, $\triangle T$ determines the achievable data rate and bit error rate subject to the accuracy of the time-to-digital conversion. Therefore, the DPWM data rate is calculated from the expected symbol value.

$$f_b = \frac{\log_2 M}{E\left[T_{ref} + a\left[k\right]\Delta T\right]} = \frac{\log_2 M}{T_{ref} + \frac{(M-1)}{2}\Delta T} \tag{4.2}$$

To adjust the bit rate of DPWM, we can choose the number of bits in a symbol, the minimum pulsewidth, and the timing resolution. For a fixed T_{ref}

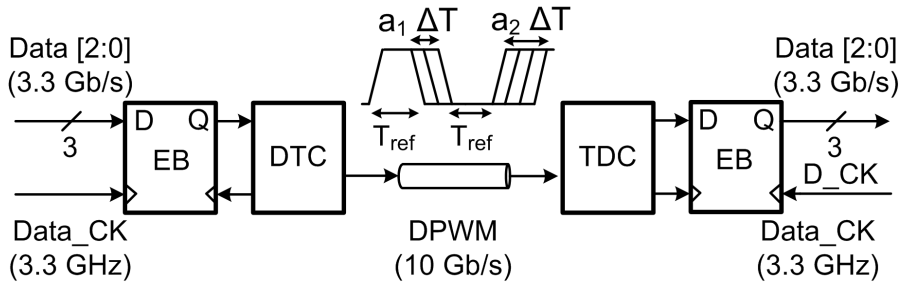


Fig. 4.1: DPWM Transceiver architecture.

and $\triangle T$, Fig. 4.2 illustrates the bit rates versus M in DPWM signaling. The numerator of (4.2) indicates an extension of total signal levels, M, enlarges the data capacity. The bit rate increases proportionally with M and peaks at a certain value depending on T_{ref} and $\triangle T$. A large M prolongs the average DPWM symbol period in the denominator of (4.2) and degrades the bit rate. Therefore, the optimal choice of M occurs when transmitting most information bits by using the least required symbol period. To achieve 10 Gb/s, for $\triangle T$= 40ps and T_{ref}= 160 ps, (4.2) indicates M= 8. Interestingly, DPWM also operates at 10 Gb/s for $\triangle T$= 80ps and T_{ref}= 80 ps when M is 4. A larger $\triangle T$ relaxes the timing resolution on transceiver, and fewer signal levels M may simplify the hardware implementation. However, the shorter T_{ref} distributes signal power into higher frequencies and incurs substantial ISI and DDJ in band-limited channels [16], [15], [18]. If $\triangle T$ is reduced through the use of fineline CMOS, a high bit rate is maintained even as T_{ref} is longer than 1/ f_b. Therefore, DPWM reduces the required channel bandwidth requirement by utilizing finer $\triangle T$ and relaxing T_{ref}.

Nonetheless, transmitting the DPWM poses an important problem; the instantaneous frequency of the DPWM signal is changing. If the values of $a[k]$ are equally probable, there is a chance that consecutive identical symbols (CIS) are transmitted. In the event of CIS of zero, $f_b = \frac{\log_2 M}{T_{ref}}$. In the event of CIS of one, $f_b = \frac{\log_2 M}{T_{ref}+(M-1)\Delta T}$. This means that the DPWM signal is plesiochronous because the rate of data transmission is changing based on the current symbol value. To mitigate this problem, we will subsequently introduce an EB for synchronous data

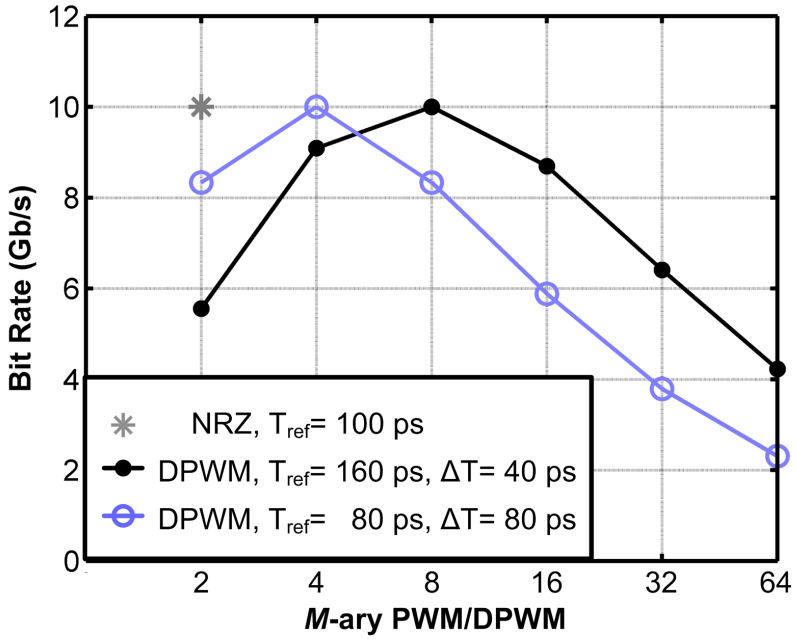


Fig. 4.2: Bit rate versus M-ary signaling.

links.

4.2 Plesiochronous-to-Synchronous Elastic Buffer

The signal transition time of the DPWM signal is a function of the symbol value as described in (4.1). Since data are available from a synchronous data bus, the EB is required to store data until the transmitter is prepared to transmit the data. Shown in Fig. 4.1, the system must accommodate the interface between the synchronous and plesiochronous timing domains. The EB is a circular shift register with $2N_{BUF}$ word registers that can accommodate for the timing skew between the synchronous data clock $Data\_CK$ and plesiochronous DTC_CK in Fig. 4.3. Head and tail pointers direct the read and write data access. The tail pointer holds the address of the next synchronous word to be written into the buffer while the head pointer holds the address of the next DPWM symbol to be encoded in the DTC. The $Data\_CK$ and DTC_CK respectively control the augmentation of the tail and head pointer. Since data are encoded on the rising and falling edges, the

DTC_CK triggers the head pointer of the EB on dual edges. While the tail pointer augments at a constant rate, the head pointer rate varies significantly based on the transmitted symbols. The EB must prevent access conflicts that occur when the head and tail pointer intersect by keeping the pointer difference under N_{BUF}.

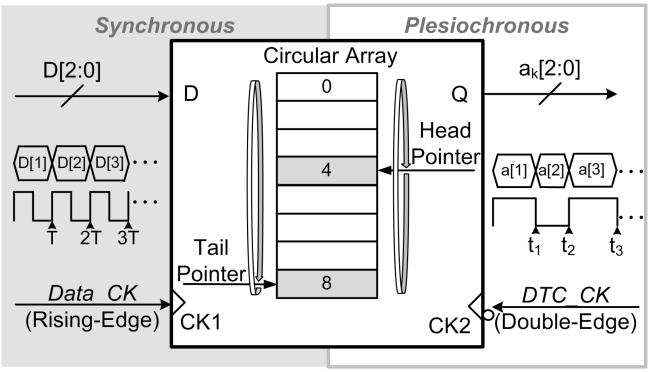


Fig. 4.3: Elastic buffer for synchronous and plesiochronous clock domain.

4.3 Elastic Buffer Timing Tolerance

While the EB can accommodate short-term variations in the frequency between $Data\_CK$ and DTC_CK, a long-term drift causes the buffer to overflow. The expected time to a pointer conflict is calculated from (4.1). The transition time of the kth transition of the DTC_CK is

$$t_k = kT_{ref} + \sum_{i=1}^{k} a[i] \triangle T, \tag{4.3}$$

where it is assumed that t_0 is aligned with the data clock at time zero. While $a[k]$ is a uniform variable over values from 0 to $M-1$, the summation of these symbols is a Gaussian distribution with variance proportional to k. The increasing variance implies an inevitable access conflict when the two pointers catch each other. The timing tolerance is only assured when the difference between the $Data\_CK$ and DTC_CK is less than the N_{BUF} depth, *i.e.*

$$t_{diff} = |t_k - kT| \leq N_{BUF} T, \tag{4.4}$$

where T is the synchronous data rate, *i.e.* $T_{ref} + 0.5 \cdot (M-1)\triangle T$. The running disparity (RD) is introduced here to evaluate the instantaneous frequency deviation between plesiochronous DPWM clock domain, T_{DPWM} and synchronous data clock, T. From (4.1), RD is expressed by $a[k] - 0.5 \cdot (M-1)$. For 8-DPWM, the RD is $a[k] - 3.5$. While RD captures the instantaneous frequency mismatch, digital sum variation (DSV) indicates the overall frequency drift between two clock domains in (4.4).

$$DSV[k] = \frac{t_{diff}}{\triangle T} = \sum_{i=1}^{k} RD[k] = \sum_{i=1}^{k} \{a[k] - (M-1)/2\} \tag{4.5}$$

When the DSV is zero, the two pointers rotate through the EB at the same speed in the long run. If DSV is positive, the DPWM pulsewidth is longer than the data clock on average and the head pointer moves more slowly than the tail pointer. To avoid access conflicts between the data clock domain and the DTC domain, the worst case deviation in DSV must be understood to determine the required size of the EB. Optimally, the two pointer addresses are always spaced by N_{BUF}. When transmitting a string of CIS, e.g. $a[k] = 7$, each symbol results in $RD = 3.5$ and incurs an infinite DSV augmentation shown in Fig. 4.4(b). While the EB is written at a constant clock rate of T, the EB is read at a slower clock rate due to the longest DPWM pulsewidth. The tail pointer runs faster and eventually catches the head pointer when data access conflicts occur. To increase the buffer size delays the data access conflict but fails to fundamentally eliminate the problem. A frequency adaptation loop is needed to assure the true plesioshronous feature in DPWM and limit the EB hardware cost that allows implementation of DPWM.

4.4 8b/9b Encoding Scheme

To ensure frequency tracking between the synchronous clock domain and the DTC domain, the synchronous clock period should equal the average DPWM pulsewidth. An adaptive 8b/9b encoding scheme is introduced for the DPWM transceiver. This 8b/9b scheme is distinct from traditional 8b/10b. Each encoded DPWM symbol pulsewidth is represented by either $T_{ref} + a_k \triangle T$ or $T_{ref} + (M -$

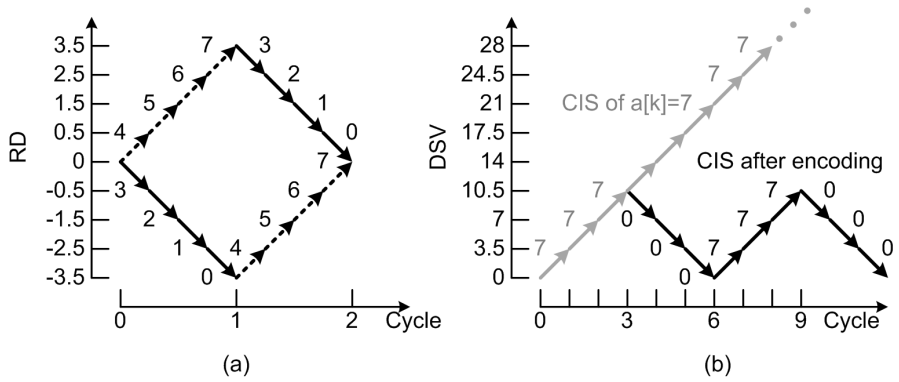


Fig. 4.4: (a) Running disparity. (b) Digital sum variation of transmitting $a_k = 7$ CIS with 8b/9b encoding (black) and without encoding (gray).

$a_k)\triangle T$ to contribute alternate RD polarities. To minimize the DSV, each encoded symbol provides the desired RD and control the overall frequency drift of the modulated signal. The encoding concept is illustrated in Fig. 4.4(b) to avoid a CIS and the implicit size constraints with the EB. The proposed scheme calculates the timing skew by dynamically examining the DSV. Depending on the current DSV polarity, the data is bit-wise inverted to equivalently map to a long or short pulsewidth and balance the speed of read pointer. If transmitting a CIS of $a_k = 7$, the feedback loop periodically inverts the information bits, alternatively generates long/short pulsewidths and equivalently adjusts the frequency of DTC_CK. By generating the desired RD, the loop seeks to balance DSV and lock DTC_CK pulsewidth to T. The long-term frequency wander between the clock domains is suppressed to avoid data access conflicts while the instantaneous frequency deviation is absorbed in EB. The feedback operation of the adaptive 8b/9b scheme is similar to a phase-locked loop. The DTC is essentially an oscillator with phase noise determined by the values of the transmitted symbols. The DSV behaves as a phase/frequency detector. The selected RD provides the frequency tuning of a oscillator.

Source encoding is implemented in the digital domain to minimize the hardware cost and complexity. In Fig. 4.5, an 8b/9b scheme is proposed to encode one 8b data byte into three 3-bit symbols with an additional inversion bit. Three

RDs are computed and accumulated by the integrator. The integrator records the deviation of the information bits with respect to the expected average value in (4.5). If the current DSV is positive and the next transmitted byte still results in a positive *RD*, the encoder inverts the every bit in the next byte. If the next transmitted byte demonstrates a negative or zero *RD*, the bits remain unchanged. The 8b/9b decoding is implemented by observing the inversion bit, INVERT. The decoder inverts the received byte when INVERT is one. If the DPWM receiver incorrectly demodulates a received symbol and results in the wrong INVERT bit, burst errors will occur but are limited to the current data byte. Because no feedback or accumulation computation is required, the 8b/9b decoding is robust to error propagation at RX.

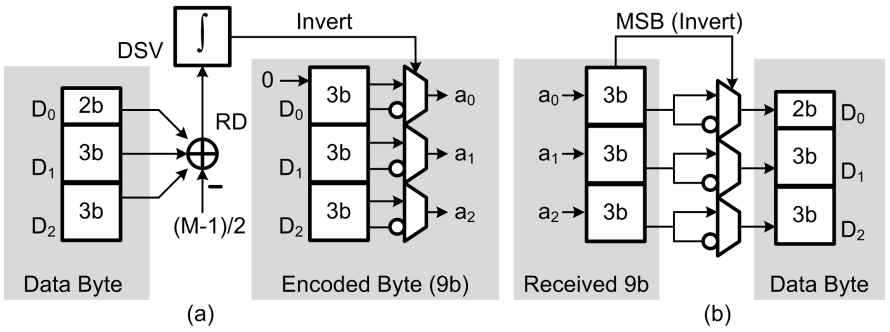


Fig. 4.5: 8b/9b encoding and decoding block diagram.

Fig. 4.6(a) simulates the *DSV* histograms of uncoded and encoded $2^{13}-1$ PRBS. When transmitting the uncoded PRBS, DPWM is incapable of tracking the frequency deviation. By repetitively transmitting the same pattern by ten times, the original PRBS demonstrates a peak *DSV* more than 125 and requires N_{BUF} of exceeding 16, i.e. 125/7.5. Most importantly, the *DSV* histogram broadens infinitely as the PRBS pattern length increases. The unbounded *DSV* makes an economical EB implementation impossible. On the contrary, the PRBS encoded by 8b/9b scheme results in a concentrated *DSV* histogram and bounds the *DSV* magnitude to 10.5. Fig. 4.6(b) simulates the temporal responses of original PRBS pattern for ten repetitions. The encoding presents several advantages. First, the

DSV is bounded because the peak DSV for three symbols is 10.5, i.e. $(7-3.5)\cdot 3$ as illustrated in Fig. 4.4(b). Second, the encoded pattern substantially shrinks the required EB size, i.e. N_{BUF}= 2, i.e. (10.5/7.5). Regardless of pattern format, the 8b/9b-encoded pattern presents a bounded disparity and only requires the total buffer size of four. Fig. 4.7 simulates the PSD of original PRBS pattern where the signal power is broadly distributed around 1.67 GHz (0.5/T). The PSD of encoded pattern presents strong spectral components at 1.67 GHz because the 8b/9b scheme suppresses the DSV and locks the average DTC frequency.

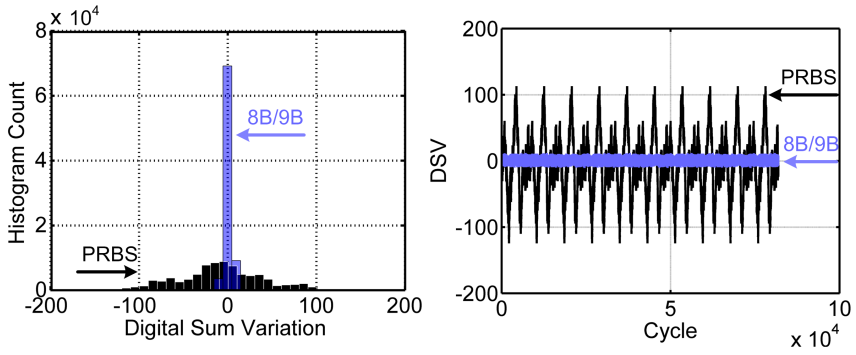


Fig. 4.6: (a) Histogram of DSV. (b) DSV versus transmitted symbol cycle.

The 8b/10b encoding for NRZ or 8b/5Q for PAM are utilized to assure the sufficient signal transition at the expense of 25% performance degradation [33] [34]. Similarly, the disadvantage of the proposed 8b/9b scheme is a reduced bit rate (12.5% penalty). However, the adaptive DTC transmitter is necessary for synchronous data links to prevent the access conflicts caused by timing skew between clock domains at the expense of performance.

The dissertation author would like to acknowledge Prof. Buckwalter for his revision of this chapter. This chapter, in full, has been submitted for publication of the material as it may appear in IEEE J. Solid-State Circuits, 2014, Wei Wang; James F. Buckwalter. The dissertation author was the primary investigator and author of this paper.

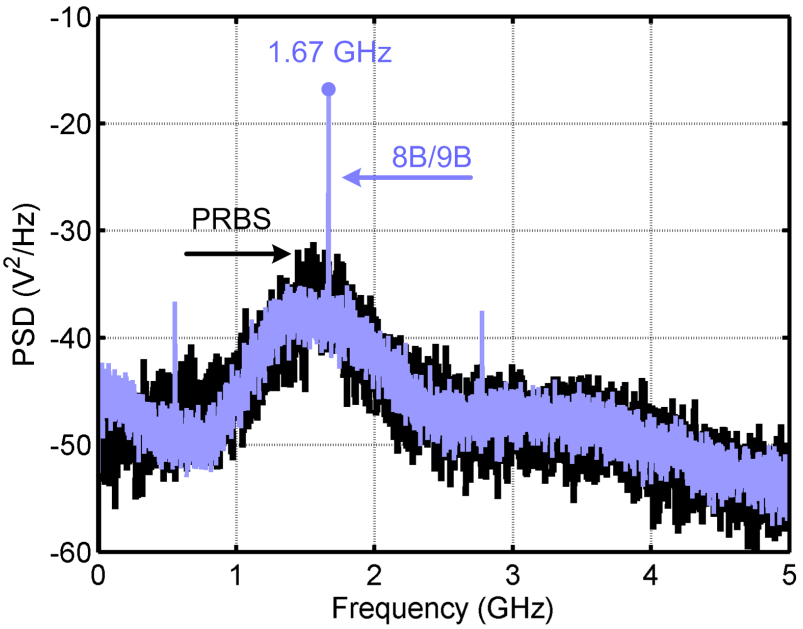


Fig. 4.7: Simulated PSD of original PRBS pattern and encoded pattern.

Chapter 5

DPWM Pre-emphasis

In band-limited electrical interconnects, the frequency-dependent loss due to skin effect and dielectric absorption is a dominant degradation in signal integrity. In addition to amplitude attenuation in channel, the phase dispersion introduces an additional significant source deteriorating the signal integrity. Group delay represents the derivative of phase response and group delay variation (GDV) evaluates the phase distortion in signal spectrum. Signal integrity degradation induced by GDV in circuit designs was investigated in recent literature [35], [36], [37]. Pre-emphasis is applied to the modulated signal to compensate high-frequency loss in conventional NRZ and PAM signaling [10], [6], [8], [38], [39]. DPWM signaling also improves signal integrity by using a feedforward equalizer. The transfer function of DPWM signal using an amplitude pre-emphasis tap weight G delayed by a duration T_d is

$$H(s) = 1 - Ge^{-sT_d}. \tag{5.1}$$

By using the first-order Pade approximation, the pre-emphasis can be modeled as a pole/zero combination where the zero frequency is $\left(\frac{1+G}{1-G}\right)\left(\frac{2}{T_d}\right)$ [40]. Fig. 5.1 illustrates the original DPWM signal transmitting a symbol stream of [0, 7, 4, 0]. While DPWM modulates signal pulsewidth according to the symbol values, the pre-emphasis boosts the signal amplitude and remains T_d in each pulsewidth. Since the pre-emphasis gain and duration both affect the peaking zero frequency,

the joint influence on magnitude and group delay variation should be addressed. Choosing the value of the pre-emphasis weight and the duration is investigated to improve the DPWM signal integrity.

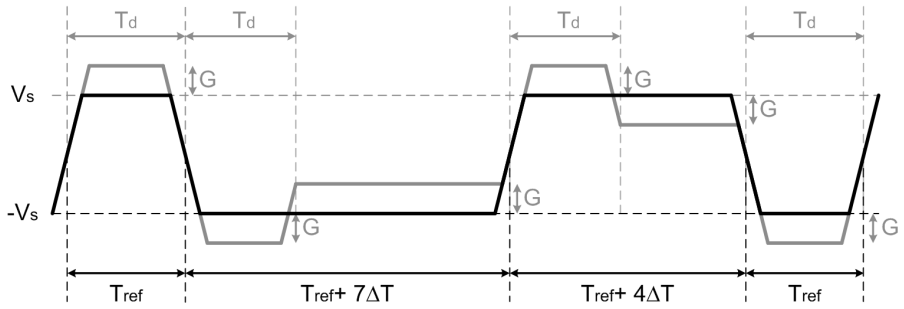


Fig. 5.1: Original DPWM signal (black) and pre-emphasized signal (gray).

Fig. 5.2(a) shows the peak in the frequency response shifts to lower frequency when G increases. While the gain peaking increases as G increases, the signal power closer to d.c. is reduced. As described previously, the signal attenuation around Nyquist frequency has a significant influence on signal integrity in band-limited channels. Fig. 5.2(a) also depicts the group delay response. As G increases, the group delay variation increases which causes phase distortion of DPWM. Fig. 5.2(b) simulates the gain peaking at 3.125 GHz versus pre-emphasis tap weight and summarizes the GDV. The GDV is captured among 1.14 to 3.125 GHz where the majority of DPWM signal power is located. A significant GDV contributed by the pre-emphasis potentially deteriorates the available timing resolution in pulsewidth modulation scheme. Here, the performance tradeoff between peaking magnitude and GDV is observed. When G=0, the transmitter presents a flat group delay response and therefore a zero GDV. While a larger tap weight increases the gain peaking at Nyquist frequency, the GDV worsens. The GDV introduced by the transmitter pre-emphasis contributes to the performance degradation in the overall DPWM group delay response where incorporates the GDV incurred in electrical channels.

In addition, T_d also affects the magnitude peaking frequency and phase response because increasing T_d lowers the peaking frequency. To evaluate the

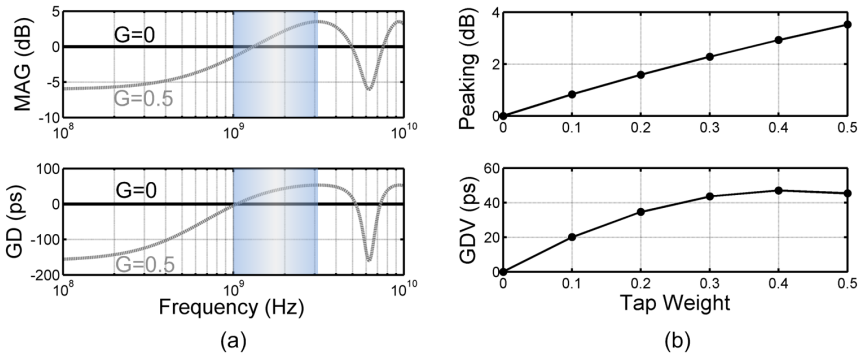


Fig. 5.2: (a) Magnitude and group delay responses versus pre-emphasis tap weight when $T_d = 4\triangle T$. (b) Magnitude peaking and group delay variation versus tap weight.

effects of T_d, Fig. 5.3(a) simulates the gain peaking and group delay versus T_d in terms of $\triangle T$. When delayed by $T_d = 4\triangle T = T_{ref}$, the pre-emphasis provides the strongest boost at 3.125 GHz. Fig. 5.3(b) depicts the peaking magnitude at 3.125 GHz and GDV with respect to T_d. The GDV increases rapidly when the pre-emphasis tap is prolonged above $T_d = 6\triangle T$.

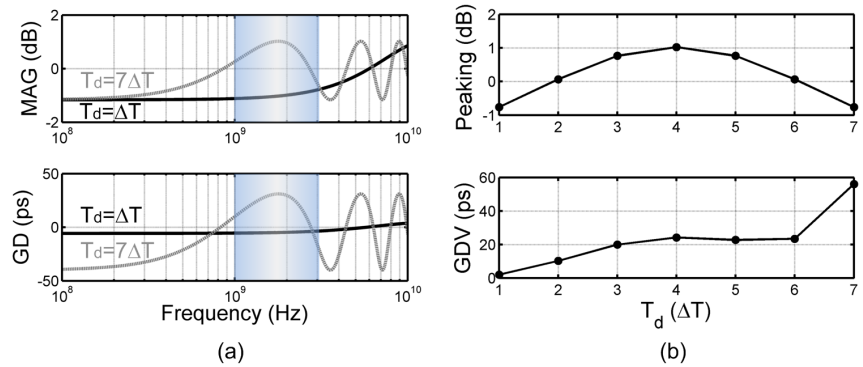


Fig. 5.3: (a) Magnitude and group delay responses versus pre-emphasis delay when $G = 0.125$. (b) Magnitude peaking and group delay variation versus T_d.

To quantify the signal integrity enhancement achieved by pre-emphasis, eye diagrams are simulated through the 24" standard FR4 PCB trace of an insertion

loss of 5 dB at 3.125 GHz. Fig. 5.4(a) shows the simulated the eyes of 8-DPWM. The time margin in terms of unit interval (UI) is normalized by $\triangle T$ (40 ps) and the differential input swing is $2V_s$. The original DPWM eye opening through the trace is 0.72 UI (28.6 ps) and 0.56 Vs at 10^{-12} BER. When pre-emphasized by G= 0.125 delayed by $4\triangle T$, the eye opening are 0.87 UI (34.6 ps) and 0.671 Vs. Fig. 5.4(b) depicts the eye width and eye height at 10^{-12} BER versus G and T_d. Generally, when G= 0.1 to 0.3, pre-emphasized DPWM presents eye quality improvement. However, a strong pre-emphasis, e.g. G= 0.4 or 0.5, incurs inferior eye opening due to reduced signal power reduction at low frequencies and worsens the group delay response. The tap weight within 0.1 to 0.2 is found to be sufficient and optimal for improving signal integrity in this channel. Fig. 5.4 also simulates the signal integrity for different tap delay. For DPWM using $T_{ref} = 4\triangle T$, the pre-emphasis delay around $4\triangle T$ presents the most improvement. To further evaluate the joint effects of G and T_d, Fig. 5.5(a) simulates the EH contour. Assume the target EH is 0.65 V_S, G of 0.1 to 0.2 is sufficient for $T_d = 4\triangle T$ and G above 0.2 is utilized for $T_d = 3\triangle T$. In fact, for a given eye opening, a lower G is desirable to reduce pre-emphasis power consumption and increase TX dynamic range. Fig. 5.5(b) simulates the EW contour. To achieve EW above 0.8 UI, DPWM requires the least pre-emphasis gain and provides the best energy efficiency when $T_d = 4\triangle T$.

The dissertation author would like to acknowledge Prof. Buckwalter for his revision of this chapter. This chapter, in full, has been submitted for publication of the material as it may appear in IEEE J. Solid-State Circuits, 2014, Wei Wang; James F. Buckwalter. The dissertation author was the primary investigator and author of this paper.

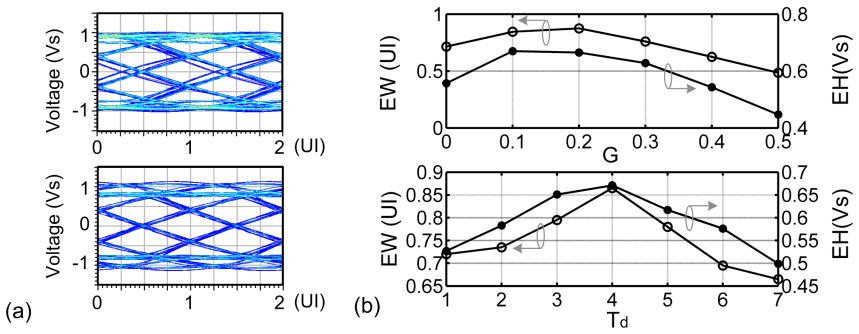


Fig. 5.4: (a) Simulated original DPWM signal when G and T_d= 0 (top) and pre-emphasized signal when G= 0.125 and T_d= 4$\triangle T$ (bottom). (b) Eye width/height at 10^{-12}BER versus tap weight (top) and versus tap delay (bottom) for 24" FR4 trace.

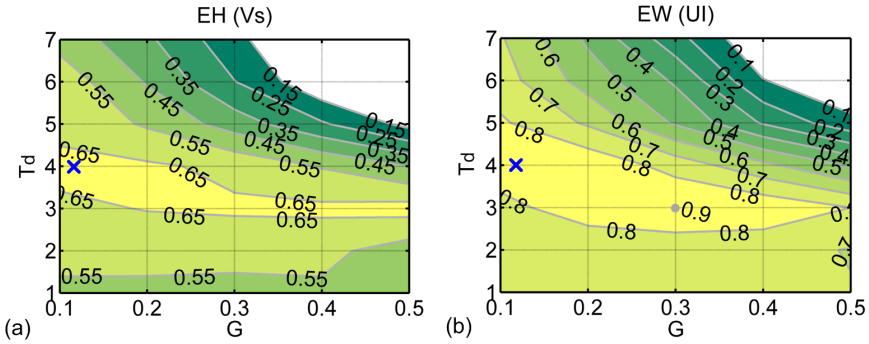


Fig. 5.5: (a) Simulated EH contour versus pre-emphasis gain and delay. (b) EW contour.

Chapter 6

DPWM Transceiver Circuit Implementation for Synchronous Data Links

6.1 Elastic Buffer

Fig. 6.1 illustrates the EB schematic consisting of two pointers and a register file of eight words (N_{BUF}= 4). For DPWM with T_{ref}= 160 ps, the EB must operate at 6.25 GHz. High-speed pointers are implemented by shift registers incorporating a one-hot coding to replace conventional binary counter. The tail and head pointers point two word addresses to be written and read. The tri-state buffers direct data flows to proper word registers. During the system initialization, EB presets H0 and T0, and equivalently activates the first (F0) and middle word (F4). During the normal operation phase, the enable bits (initially on H0 and T0) are circulated among each pointer chain to sequentially enable other word registers. If $Data\_CK$ and DTC_CK have the same frequency, the write and read addresses should be separated by four.

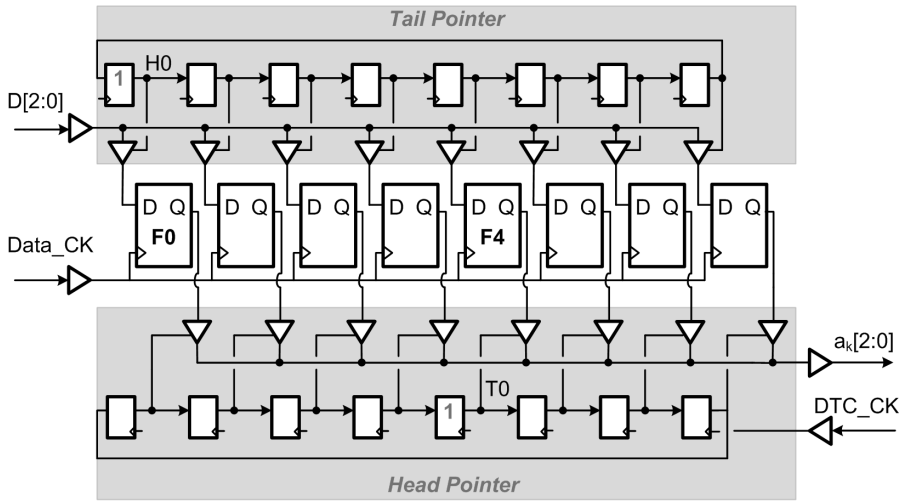


Fig. 6.1: Elastic buffer schematic (N_{BUF}= 4)

6.2 DPWM Transmitter

Fig. 6.2 shows the diagram of the low-jitter DTC circuitry for 8-level DPWM [41]. A phase-rotation circuit uses eight clock phases with state transition control to implement cycle-by-cycle pulsewidth control. For DPWM, the DTC modulates the dual-edge pulsewidth of $(a_k + P)\triangle T$, where $T_{ref} = P\triangle T$ and P is programmable for adaptation to different channel characteristics. When P programs from 4 to 7, the DPWM bit rate adjusts to 10, 8.8, 7.9 and 7.14 Gb/s.

The DTC integrates the current symbol $a[k]$ with the prior symbols and computes a modulo-8 divide to determine the current phase selection. The phase multiplexer (MUX) selects one of clock phases to generate the trigger signal (M_CK). When M_CK passes through the latch (L), the frequency divider alternatively generates positive and negative pulses without introducing duty-cycle distortion. Note M_CK is regulated by the FSM on the latch. When $a[k]$ is less/equal than TH , the double-edge pulses are generated by rotating the phases of MUX. When the excess phase change induced by large $a[k]$ (larger than TH), the FSM uses a state transition control to allow the phase to rollover and skip redundant clock cycles. When switching to the correct state, FSM enables the latch (L) and the

frequency divider to generate DPWM pulses. Eliminating the redundant delay cells adopted in conventional DTC, this feature substantially improves the signal integrity especially for larger T_{ref} or to increase the number of signal levels. The DTC timing diagram and pre-emphasis driver design are also illustrated in Fig. 6.2.

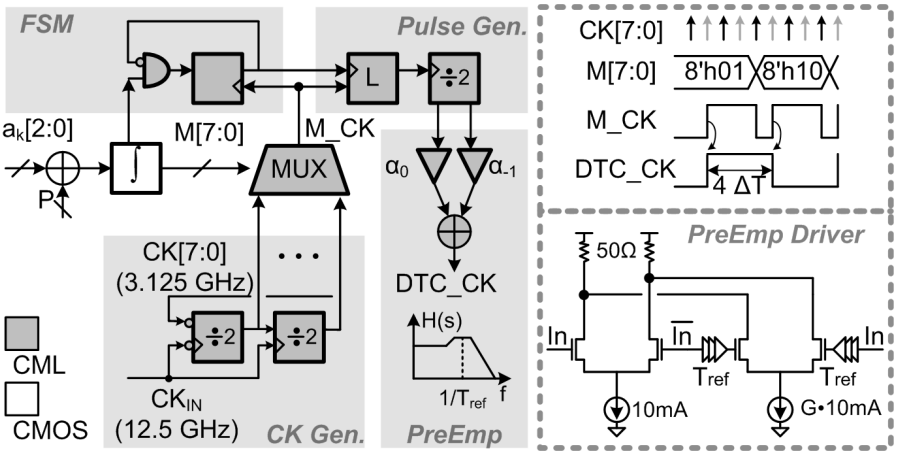


Fig. 6.2: Digital-to-time converter with pre-emphasis.

6.3 DPWM Receiver

Symbol recovery from the 10 Gb/s DPWM signal requires dual-edge pulse width conversions at 3.1 GHz ($1/(4\triangle T + 4\triangle T)$) with the timing resolution of 40 ps. The corresponding RX architecture is illustrated in Fig. 6.3. The proposed DPWM receiver uses time-interleaved (TDC) circuits to capture incoming positive and negative pulsewidths to recover the transmitted 3-bit symbol.. Fig. 6.3 depicts the proposed receiver block diagram. The receiver uses a common limiting pre-amplifier to regenerate the signal swing since DPWM has two signal levels. Sampled by the dual edges of $2\triangle T$-period clock CK_{IN}, the slicer quantitizes the pulsewidth in terms of $\triangle T$, and integrator records the conversion results for symbol demodulation. Dual TDCs perform time-interleaving pulsewidth conversions. L_CK represents the signal transitions of DPWM and triggers the write operations

of EB. The proposed TDC circuits operates above a conversion rate of 3.1 GHz and simulates the timing margin of 32 ps (0.8 UI) at an input swing of 50 mV. Sampling phases beyond 0.8 UI are constrained by the sense amplifier metastability. High-speed CML circuitry is used in slicers, and CMOS logic is utilized in computation blocks to save power consumption. The preliminary DPWM receiver design is demonstrated in [41], and the low-power version of receiver is presented here. By refining the pre-amp design and utilizing the sense-amp slicer, the new TDC reduces the 55% power consumption and improves 10% timing margin, compared to the previous design. At 10 Gb/s operation with 50 mV input swing, the simulated power consumption and timing margin of previous and new TDCs are 38 mW/0.7 UI and 17 mW/0.8 UI, respectively.

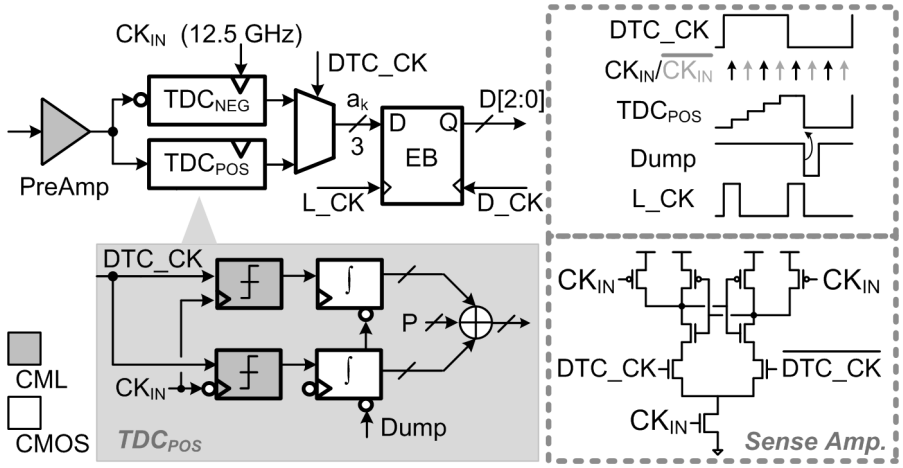


Fig. 6.3: Time-to-digital converter.

The lack of signal transition in NRZ and 4-PAM is not concerned in DPWM because DPWM alternatively transmits positive and negative pulses for every symbol transmission. Hence, DPWM naturally presents a run-length-limited characteristic and facilitates the CR. As shown in [41] [15], DPWM has energy nulls at low frequencies even without encoding. In addition, DPWM utilizes only two signal swings and presents one threshold crossing as in NRZ; therefore, the erroneous edge detection in 4-PAM is avoided. For the link applications with a forward clock channel, the clock recovery (CR) of DPWM is straightforward by using a PLL

or DLL. Without a forward clock channel, CR is required for sampling and synchronizing information bits. If T_{ref} can be implemented precisely as a multiple of $\triangle T$, the clock recovery concept is identical to the one in NRZ. However, because DPWM utilizes a finer timing resolution compared to NRZ, a multiphase CR can be considered to reduce receiver circuit bandwidth [24] [25] [42]. In this thesis, since the proposed DTC precisely generates T_{ref} in terms of $\triangle T$, the receiver CR is compatible with a typical design concept in NRZ.

Source encoding impacts CR for multilevel signaling. For the links without a forward clock channel, 8b/10b and 8b/5Q schemes are developed for NRZ and 4-PAM to assure signal transitions in a finite symbol length [34]. 4-PAM CR should carefully avoid edge detections on erroneous threshold crossings to reduce recovered clock jitter. A symmetric code for 4-PAM provides a good solution to eliminate erroneous threshold crossings [43]. Notably, 8b/10b, 8b/5Q and symmetric coding all demonstrate a bit rate penalty of 25%.

6.4 Transceiver Measurements

The chip was implemented in 45-nm CMOS SOI and the die photograph is shown in Fig. 6.6. Individual breakouts were used in the evaluation of the subcircuits.

6.5 8b/9b Encoder/Decoder

To demonstrate the hardware feasibility of 8b/9b scheme, the encoder and decoder designs are implemented on a 45 nm SOI CMOS at the target data rate of 10 Gb/s. Fig. 6.4 depicts the implementation including clock dividers, an on-chip PRBS, encoder/decoder designs, and data multiplexers. Subrate clocks ($CK3/CK9$) are used for the EB data clock and data bit multiplexing. The original 8b data byte is generated by PRBS and encoded by the proposed 8b/9b scheme. Assuming DPWM symbols are demodulated correctly, the encoded byte, $EN\_Byte[8:0]$ are forwarded to the input of decoder. According to the MSB

inversion polarity, the decoder inverts the received byte and recovers the original data byte. If the decoder functions correctly, the decoded byte, $DE\_Byte[8:0]$, represent the identical original data byte. To facilitate BERT testing, $EN\_Byte[8:0]$ byte and $DE\_Byte[8:0]$, are multiplexed to serial bit streams and compared to the expected bit patterns. The two circuitry consumes 1.5 mW in total when operating at 10 Gb/s. Fig. 6.5(a) measures the active area of encoder and decoder of 86 x 114 um^2 and 30 x 46 um^2. Fig. 6.5(b) measures the eye diagram of decoded data bit. The hardware implementation demonstrates the good area and power efficiency when utilizing 8b/9b scheme.

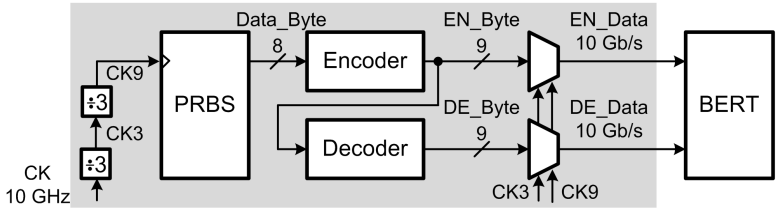


Fig. 6.4: The block diagram of 8b/9b encoder/decoder chip and testing interface.

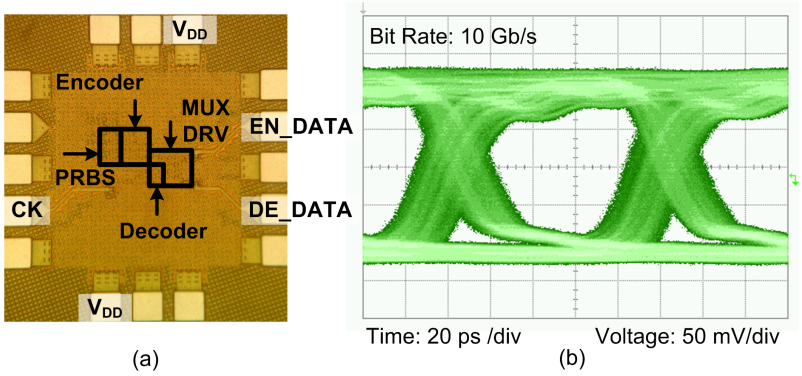


Fig. 6.5: (a) The 8b/9b encoder/decoder chip microphoto. (b) The decoded data bit.

6.6 Synchronous Data Links Incorporating Elastic Buffer and 8b/9b Encoding Scheme

The DTC/TDC chip microphotographs are shown in Fig. 6.6 with the active area measuring 93x94 um^2 and 218x160 um^2, respectively. The power consumption of DTC including output driver and TDC including the pre-amp are 65mW and 29mW, respectively. Any choice of T_{ref} from 4 to 7 $\triangle T$ exhibits comparable power consumption. DPWM achieves 10 Gb/s by using $\triangle T$ =40 ps and T_{ref}=160 ps. Transceiver performance is summarized in Table 6.1.

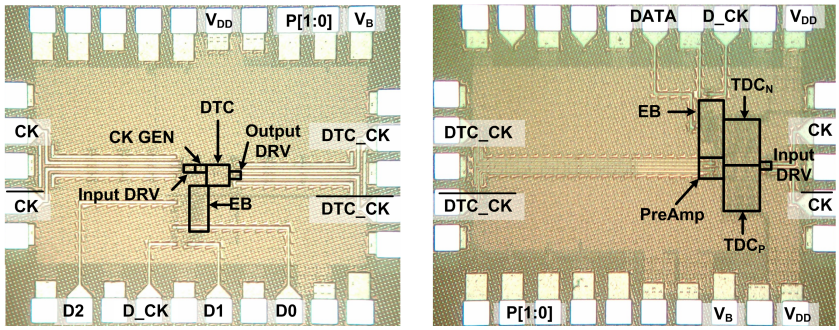


Fig. 6.6: Microphoto of the transmitter (left) and receiver (right).

Fig. 6.7 depicts the test setup for verifying DPWM synchronous data links using EB with 8b/9b scheme. Agilent 81142 pulse pattern generator is programmed to generate 10 Gb/s encoded bit stream (EN_Data) into TX. An on-chip demultiplexer provides a serial-to-parallel interface to convert the bit stream into DPWM symbols. DTC reads out the pattern from EB and generates DPWM signal. At RX, TDC demodulates DPWM symbols and stores conversion results into EB. The recovered bits are multiplexed to a serial bit stream (DE_Data). Fig. 6.8 measures the DPWM signal power and matches the simulated PSD. Note signal power concentrates on 1.67 GHz (4+3.5$\triangle T$) and integrates 77% within the Nyquist frequency of 3.125 GHz.

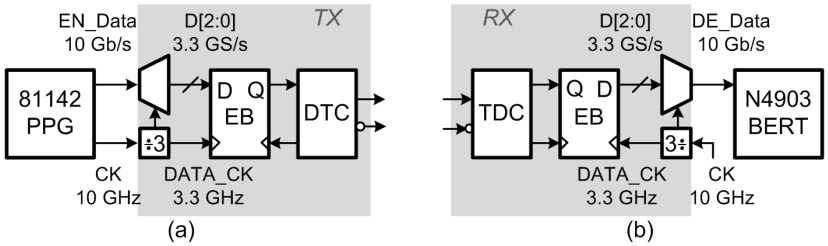


Fig. 6.7: (a) Test setup for the transmitter incorporating 8b/9b encoding. (b) Test setup for the receiver.

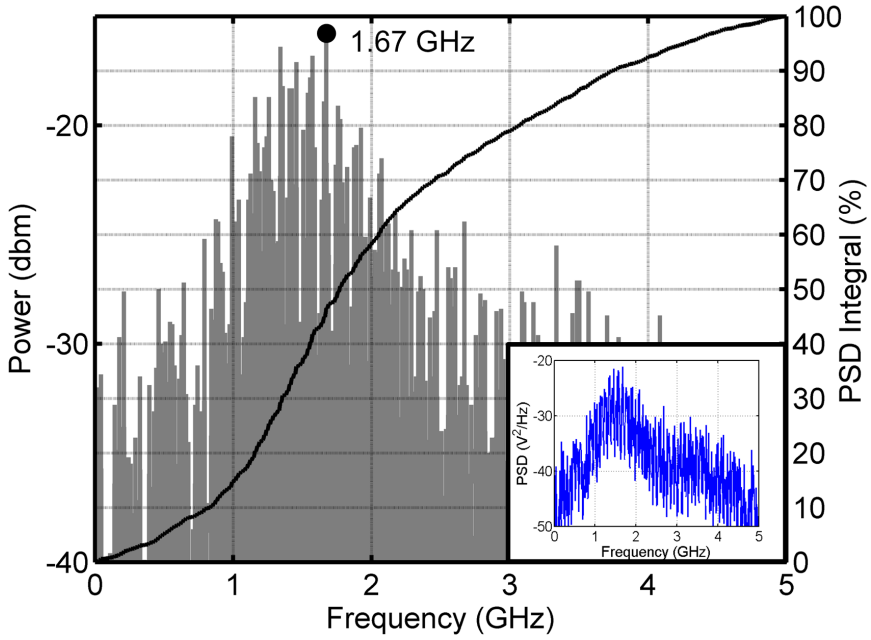


Fig. 6.8: Simulated PSD (blue), measured PSD (gray) and signal power integral (Y axis on right).

6.7 Transmitter Performance

Fig. 6.9 measures the frequency-dependent loss of 120" coaxial cable which has 4.5 dB loss at 3.125 GHz. DPWM pre-emphasis provides gain boosting around 1 dB at 3.125 GHz. The pre-emphasis gain is used to boost the high-frequency response specifically in the region around the peak of the DPWM in the PSD. Fig. 6.10 illustrates the BER bathtubs in the original and equalized channels. The transmitted eye width at 10^{-12} BER is 31 ps (0.78 UI). At the bit rate of 10 Gb/s, the received eye width at 10^{-12} BER is 20 ps (0.5 UI) without pre-emphasis and 26 ps (0.65 UI) with pre-emphasis to reduce data-dependent jitter. The pre-emphasized DPWM improves the eye opening by 0.15 UI. At the bit rate of 7.14 Gb/s, the received eye width at 10^{-12} BER is 25 ps (0.625 UI) without pre-emphasis and 28 ps (0.7 UI) with pre-emphasis. Fig. 6.11 measures the pre-emphasized eyes at the cable end.

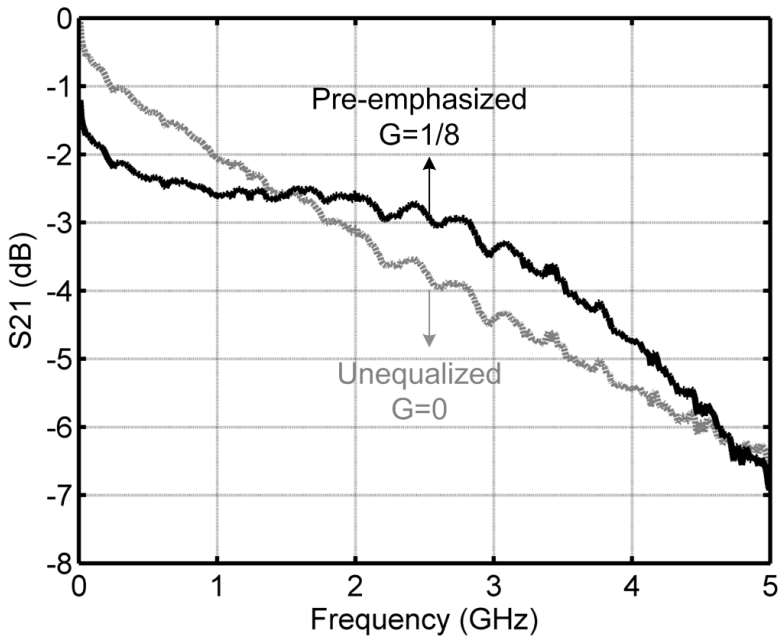


Fig. 6.9: S21 of 120" cable, and overall response using pre-emphasis.

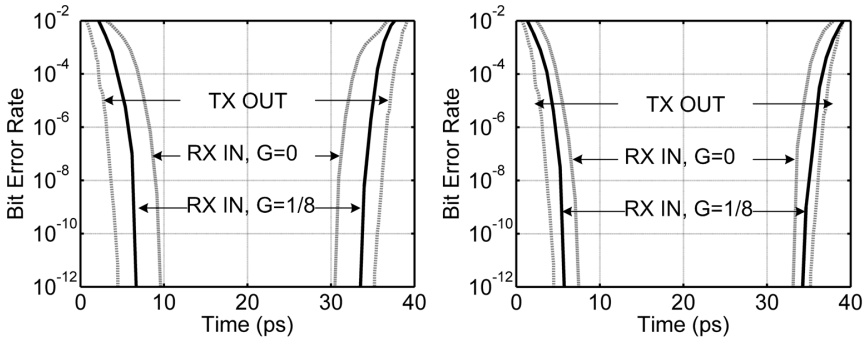


Fig. 6.10: Time BER bathtub of 10 Gb/s (left) and 7.14 Gb/s (right). Transmitted eye performance and received eye performance are compared in the same figure.

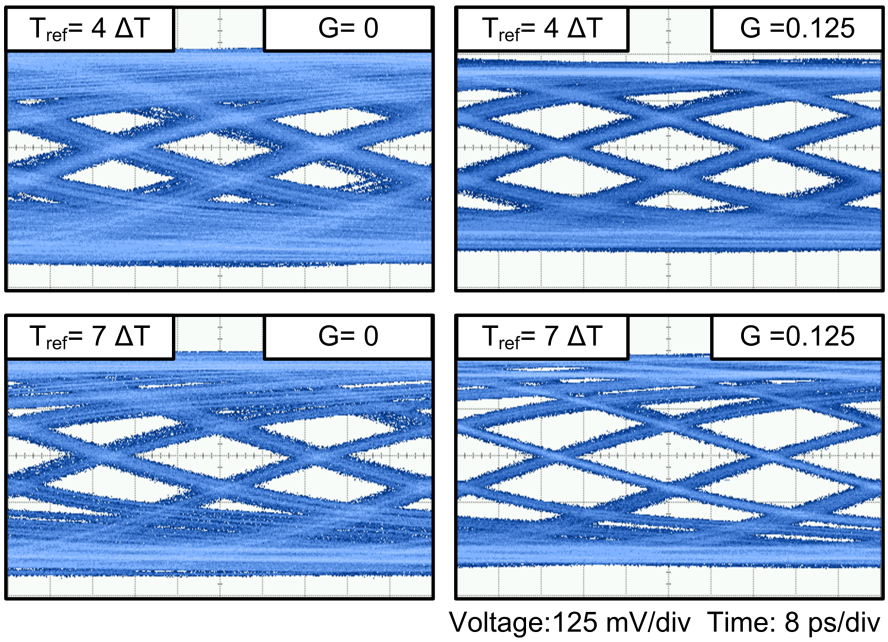


Fig. 6.11: Original and pre-emphasized DPWM through the cable at 10 Gb/s (top) and 7.14 Gb/s (bottom).

6.8 Receiver Performance

The timing resolution of TDC determines the tolerance for additional random jitter (RJ) and deterministic jitter (DJ) sources. The symbol recovery is corrupted if the peak jitter in the DPWM signal is larger than 40 ps. The receiver BER bathtub measurements and recovered data are shown in Fig. 6.12. Fig. 6.13 illustrates the receiver performance versus differential input swing. Generally, the measured performance presents a degraded time margin around 0.3 UI from the simulated performance. To explain the performance degradation, several major DJ sources should be considered. DJ_{TDC} denotes the simulated timing degradation caused by the actual SOI circuit implementation. DJ_{BERT} is the data jitter of pattern generator and increases as the data swing decreases. DJ_{CH} represents the cable/connector phase mismatches. Notably, BERT incurs significant jitter when generating data swing of around 200 mV. Therefore, the receiver performances are compared on a data swing of 240 mV. The simulated and measured time margin of BER less than 10^{-12} are 0.9 UI and 0.625 UI, respectively. Assuming the other DJ sources other than phase mismatches is negligible, the receiver tolerates additional RJ sources of 1.78 ps (0.625UI/14) at 10^{-12} BER.

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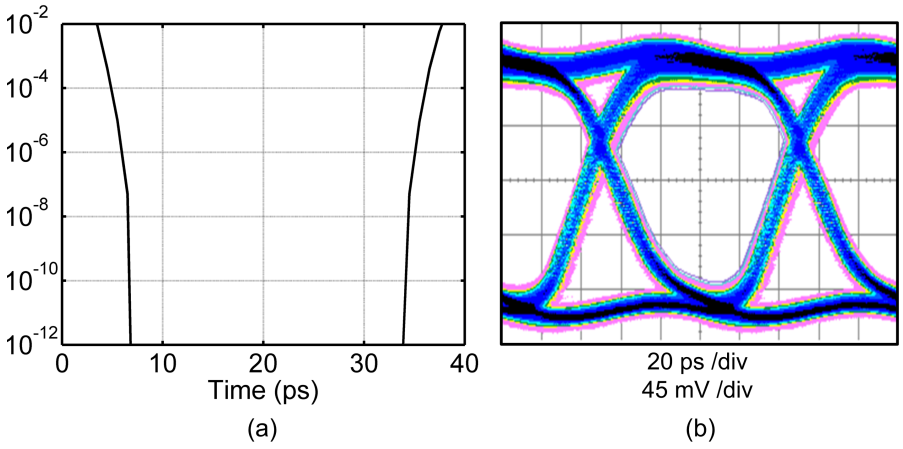

Fig. 6.12: (a) Time BER bathtub of RX sampling phase. (b) Recovered data.

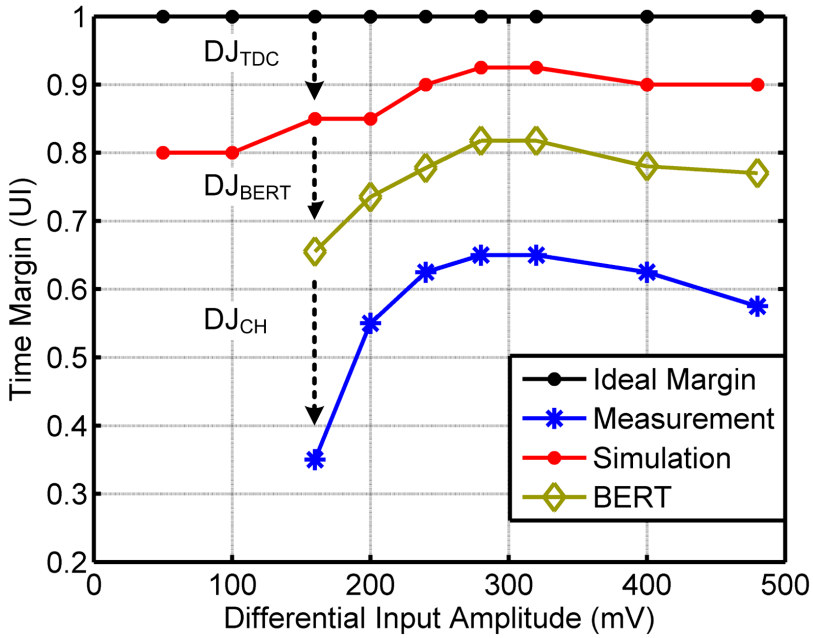

Fig. 6.13: RX time margin of 10^{-12} BER versus the signal swing.

Table 6.1: DPWM transmitter and receiver performance summary.

Technology	45nm SOI CMOS
Timing Resolution, $\triangle T$	40 ps
Minimum Pulsewidth, T_{ref}	4 to 7 $\triangle T$
Data Rate	10, 8.8, 7.9 and 7.1 Gb/s
Supply Voltage	1.2V (TX) / 1.1V (RX)
Power Dissipation	
TX EB	3 mW
TX Clock Generator/Buffer	18 mW
DTC	30 mW
Driver	14 mW
Transmitter Total	65 mW
PreAmp	3 mW
TDC	14 mW
RX EB	3 mW
RX Clock Buffer	9 mW
Receiver Total	29 mW
Transceiver Total	94 mW
Energy per Bit	9.4, 10.7, 11.9 and 13.2 pJ/bit
Tx Output Jitter	$\leq$1.3 ps
RX Input Sensitivity	50 mV/ 0.8 UI (Simulated)
	240 mV/ 0.625 UI (Measured)

Chapter 7

Conclusion

This thesis proposes the use of double-edged pulsewidth modulation for bandwidth-limited interconnects. DPWM signaling offers higher spectral efficiency than NRZ without using increasing voltage supplies. Timing parameters of a DPWM scheme are discussed in terms of required channel bandwidth. A digital-to-time converter architecture is introduced for generating a low-jitter DPWM signal generation and adapting the signal to the channel bandwidth. A multiphase time-interleaving time-to-digital converter architecture is introduced for the high conversion rate receiver. The transmitter and receiver is implemented in 45-nm CMOS SOI and experimentally verified to BER of 10^{-12}. At 10 Gb/s, the transmitter and receiver consume 107 mW. Finally, the advantage of DPWM to NRZ is demonstrated in a DDR channel emulation.

For synchrounous data links, this thesis presents a high-speed serial I/O scheme based on DPWM. DPWM signaling offers a doubled bit rate compared to PWM. The second-generation TX presents an eye opening of 0.78 UI at 10^{-12} BER. Pre-emphasis concept proves the common feedforward technique helpful for DPWM. The pre-emphasized DPWM improves signal integrity by 0.15 UI through a 120" cable. the second-generation RX time margin of 10^{-12} BER is experimentally verified versus input swing. Different to the conventional DPWM restricted in asynchronous applications, an adaptive 8b/9b scheme tracks the frequency deviation and enables DPWM for synchronous data links. To demonstrate the hardware feasibility of 8b/9b scheme of 10 Gb/s, the encoder and decoder implementations

achieve 10 Gb/s data rate and consume 1.5 mW.

The dissertation author would like to acknowledge Prof. Buckwalter for his revision of this chapter.

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