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Low-Power Clock Distribution Using a Current-Pulsed Clocked Flip-Flop

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Abstract—We propose a new paradigm for clock distribution that uses current, rather than voltage, to distribute a global clock signal with reduced power consumption. While current-mode (CM) signaling has been used in one-to-one signals, this is the first usage in a one-to-many clock distribution network. To accomplish this, we create a new high-performance current-mode pulsed flip-flop with enable (CMPFFE) using 45nm CMOS technology. When the CMPFFE is combined with a CM transmitter, the first CM clock distribution network exhibits 62% lower average power compared to traditional voltage mode clocks.

Index Terms—Current-mode, flip-flop, clock distribution network, crosstalk, low-power.

I. INTRODUCTION

PORTABLE electronic devices require long battery lifetimes which can only be obtained by utilizing low-power components. Recently, low-power design has become quite critical in synchronous Application Specific Integrated Circuits (ASICs) and System-on-Chips (SOCs) because interconnect in scaled technologies is consuming an increasingly significant amount of power. Researchers have demonstrated that the major consumers of this power are global buses, clock distribution networks (CDNs), and synchronous signals in general [1].The CDN in the POWER4 microprocessor, for example, dissipates 70% of total chip power [2].

In addition to power, interconnect delay poses a major obstacle to high-frequency operation. Technology scaling reduces transistor and local interconnect delay while increasing global interconnect delay [3], [4]. Moreover, conventional CDN structures are becoming increasingly difficult for multi-GHz ICs because skew, jitter, and variability are often proportional to large latencies [5].

Prior to and in early CMOS technologies, current-mode (CM) logic was an attractive high-speed signaling scheme [6]. CM logic, however, consumes significant static power to offer these high speeds. Because of this, standard CMOS voltage-mode (VM) signaling has been the *de facto* standard logic family for several decades.

Low-swing and current-mode signaling, however, are highly attractive solutions to help address the interconnect power and variability problems [1], [4], [7]–[9]. Traditionally, the static power dominates dynamic power consumption in a CM signaling scheme. However, the static power is often significantly less than VM dynamic power and latency is significantly improved over VM in global CM interconnect. CM signaling schemes also offer higher reliability since they are less susceptible to single-event transient upsets due to the absence of buffers with source/drain diffusion areas that can be hit by high-energy particles.

Previous CM schemes have been used for commonly, off-chip signals. Standard logic signals, however, have remained VM to benefit from the low static power of CMOS logic. In our proposed scheme, it is not practical to make each individual point-to-point segment of the CDN CM, but the clock signal should still benefit from the power and reliability of CM signaling. Instead, the power savings is maximized by creating a high-fanout physically or electrically symmetric distribution [5] that feeds many CM flip-flop (FF) receivers. Logic signals on the FF receivers retain VM compatibility with low-power CMOS logic in the remainder of the chip.

In this paper, we present the first true CM CDN and a new CM pulsed D-type FF where the clock (CLK) input is a CM receiver and the data input (D), an active low enable ($\overline{EN}$), and output (Q) are VM. In particular, the key contributions of this paper are:

- The first demonstration of a CM clocked FF.
- The effective integration of the CM FF with VM CMOS logic.
- Power consumption comparison of CM CDN and VM CDN at different frequencies.
- Noise and variability analysis of CM and VM CDN.

The rest of the paper is split into following sections: Section II gives a brief overview of some existing CM
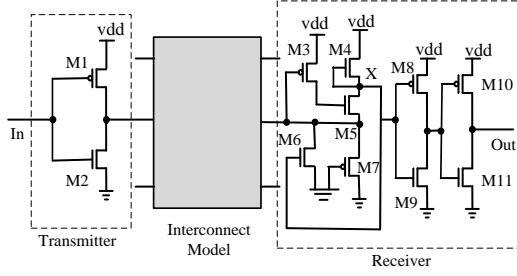
Fig. 1. Previous CM schemes used an expensive transimpedance amp Rx which could result in significant skew due to V_{CM} shift if applied to CDNs [10].
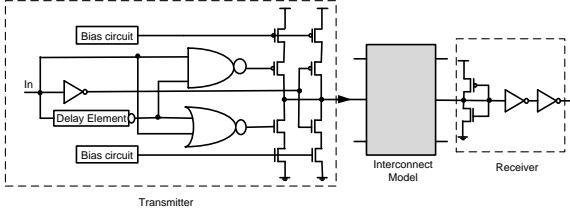

Fig. 2. Expensive variation tolerant CM signaling scheme [8] consumes large static and dynamic power when compared to the other CM techniques.

signaling schemes. Section III proposes our CM FF and CDN. Section IV compares our new FF and CDN with existing scheme considering power and noise immunity. Finally, Section V concludes the paper.

II. OVERVIEW OF EXISTING CM SIGNALING SCHEMES

In a CM signaling scheme, a transmitter (Tx) utilizes a VM input signal to transmit a current with minimal voltage swing into an interconnect (transmission line), while a receiver (Rx) converts current-to-voltage providing a full swing output voltage. The representative CM scheme in Figure 1 uses a CMOS inverter as the Tx while the Rx is based on a transimpedance amplifier [10]. This scheme provides delay improvement over VM schemes, but the Rx voltage swings around a common-mode voltage (V_{CM}) and any V_{CM} shift would cause a large CDN skew [11].

Other researchers have used a dynamic over-driving Tx with a strong and weak driver alongside a low-gain inverter amplifier Rx and a controlled current source that addresses the previous V_{CM} problem [4]. However, this scheme results in rise- and fall-time mismatch at the output [8] which can be problematic in CDNs.

Variation-tolerant CM signaling schemes have used a CM Tx with corner-aware bias circuitry [8]. Figure 2 shows the variation tolerant CM scheme including Rx and Tx circuits [8]. In this scheme, the inverter amplifier Rx circuit provides low-impedance to ground and holds

the terminal point at the switching threshold. However, this comes at the expense of large static and dynamic power when compared to the other CM techniques and makes it unattractive compared to existing VM signaling.

III. CURRENT-MODE CLOCKING

All of the previous CM signaling schemes perform current-to-voltage conversion and then use the buffered VM clock signal. However, driving the lowest level of a CDN with a full-swing voltage results in large dynamic power in addition to significant buffer area to drive the clock pin capacitances. Our CM scheme is highly integrated into the FFs that directly receive the CM signal to reduce overall power consumption and silicon area.

A. Current-Mode Pulsed Flip-Flop with Enable (CMPFFE)

Figure 3 and Figure 4 show the circuit and simulation data of the proposed current-mode pulsed DFF with enable (CMPFFE). The CMPFFE is similar to our previously published CMPFF [12], but uses an active-low enable ($\overline{EN}$) signal. The CMPFFE uses an input current-comparator (CC) stage, a register stage, and a static storage cell. The CC stage compares the input push-pull current with a reference current and conditionally amplifies the clock to a full-swing voltage pulse that triggers the data to latch at the register stage. The feedback pulsed FF is in stark contrast to the previous CM schemes which utilized expensive Rx circuits and buffers to drive the final FFs.

The choice of push-pull current enables a simple Tx circuit (discussed further in Section III-B) while maintaining a constant (or at least low-swing) bias voltage on the CDN interconnect. The CMPFFE in Figure 3 is only sensitive to unidirectional push current which provides the positive edge trigger operation of the FF. This design is easily modified using a complementary current comparator into negative clock edge FF using the pull current.

In order to efficiently receive an input pulse current, a CM Rx requires a low input impedance (Z_{in}). A small signal analysis at the input of the proposed CMPFFE ensures the low Z_{in} according to

$$Z_{in} = \frac{1}{g_{m1} + g_{m2}} \tag{1}$$

where g_{m1} and g_{m2} are the transconductance of transistor M1 and M2, respectively. The input impedance of the proposed CM FF is also identical to the previously reported variation-tolerant CM signaling Rx [8].

Traditionally, CM Rx/logic circuits consume a significant amount of static power even when the circuits are
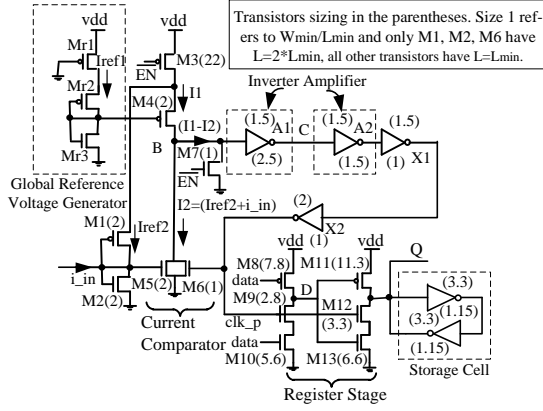
Fig. 3. The Proposed CMPFFE uses current-comparator and feedback connection to generate a voltage pulse that triggers a register stage to store data in the storage cell.
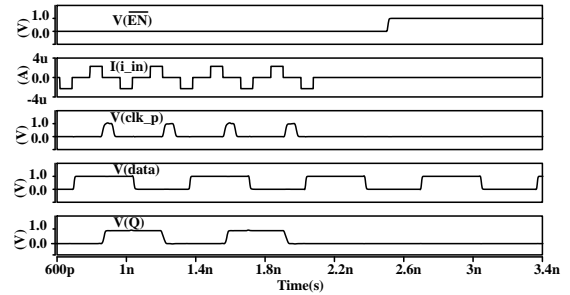

Fig. 4. Simulation waveforms confirm the internal current-to-voltage pulse generation (clk_p) that triggers input data capture.
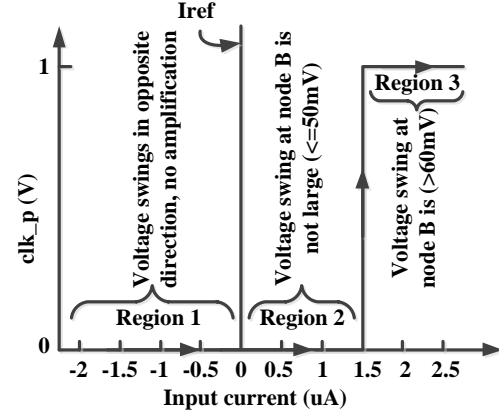

Fig. 5. The proposed CMPFFE generates an output voltage pulse depending on the input current and also complementing the edge triggered operation.

in sleep mode. Our CMPFFE incorporates an active-low enable ($\overline{EN}$) signal that, when low, connects PMOS (M4) to vdd for normal operation. On the other hand, it disables the static current I1 in stand-by mode when high. Since internal node B is decoupled in this stand-by mode, an additional transistor M7 is required to ground the internal clock node and prevent any unintentional latching of input data. Transistor M7 is disabled during normal operation. Adding an extra OFF transistor will introduce a stacking effect in the CC [13]; which in turn will reduce the leakage current in M4 significantly. The peak CMPFFE leakage current is $2.4\mu A$, significantly smaller than the peak switching current of $134\mu A$ in active mode. However, global $\overline{EN}$ routing requires extra metal resources. Since the proposed CM scheme does not require buffers in the CDN, it is not difficult to globally route $\overline{EN}$.

In the input stage, the reference voltage generator (Mr2-Mr3) creates a reference current (Iref1) that is mirrored by M4 and generates I1. Similarly, the M1-M2 pair creates the FF reference current (Iref2) which is combined with the input current (i_in); this current is then mirrored by M5 to I2. A PMOS (Mr1) is added to replicate the voltage drop of M3.

It is possible to use a local or global reference voltage generator for the input gate voltage of M4. Using a global reference can increase the robustness by reducing transistor mismatch between FFs. Hence, we used a global reference voltage generator that distributed across the whole chip, when we integrate the CMPFFE with the CM CDN. This also saves two transistors per FF and reduces static power with a negligible performance penalty. Unlike corner-aware reference voltage generators [8], we used a simple three transistor global reference voltage generator as shown in Figure 3. In addition, CM signaling eliminates the requirement of CDN buffers, which

reduces significant active area and makes easier global reference routing.

The mirrored currents I1 and I2 are compared using the inverting amplifier (A1) at node B and further extended to a CMOS logic level at node C by another inverting amplifier (A2). The inverter pair (X1-X2) generate the required voltage pulse duration before the feedback connection in M6.

The feedback connection from the generated voltage pulse with M6 quickly pulls down the current comparator node B which facilitates generating a small voltage pulse and results in fewer transistors in the register stage. In addition, we properly size the X2 inverter so that it can efficiently drive the clock capacitance of register stage without affecting circuit performance.

Figure 5 shows the transfer characteristics of the proposed CMPFFE based on input current and voltage pulse (clk_p) generation. Figure 5 identifies three regions of operation of the proposed FF. In region 1, the input current is ≤ 0, and node B starts discharging from steady state resulting in a high voltage (very low swing 980mV-850mV) at the A1 output. Hence, the clk_p signal stays at 0. In region 2, the input current is $(0 < i\_in < 1.5\mu A)$, and node B starts moving towards

steady state to high. However, the swing is not large enough resulting in a low clk_p signal. In region 3, the input current is $\geq 1.5\mu A$, and the voltage swing at node B is large enough so that the amplifiers and inverter chain can generate required voltage pulse (clk_p goes low to high Figure 4) for the register stage.

The register stage is similar to a single-phase register [14], but requires fewer transistors and has a reduced clock load compared to other pulsed FFs. The current-generated voltage pulse triggers storing data in the output storage cell.

The sizing of M6 is critical to the voltage pulse; we use a minimum sized NMOS transistor with unity aspect ratio. The width of the generated clk_p is also sensitive to the width and amplitude of input current (i_in). The amplitude of i_in strongly affects the FF performance by changing the operating point of M5 and adding extra delay to generated clk_p signal. In order to achieve minimum CLK-to-Q delay, the ideal input current has a $\pm 2.3\mu A$ amplitude and $70ps$ pulse width. This can be guardbanded to tolerate noise and variation.

### B. Current-Mode Transmitter and Distribution

In order to integrate the CMPFFE, a Tx provides a push-pull current into the clock network and distributes the required amount of current to each CMPFFE. Our proposed CM CDN with Tx, interconnect, and the CMPFFE is shown in Figure 6(a). The Tx receives a traditional voltage CLK from a PLL/clock divider at the root of the H-tree network and supplies a pulsed current to the interconnect which is held at a near constant voltage. The clock distribution is a symmetric H-tree with equal impedances in each branch so that current is distributed equally to each CMPFFE leaf node.

The pulsed current Tx in Figure 6(a) is similar to previous Tx circuits [4], [8], but uses a NAND-NOR design. The NAND gate uses the CLK signal and a delayed inverted CLK signal, clkb, as inputs to generate a small negative pulse to briefly turn on M1. Hence, the PMOS transistor briefly sources charge from the supply while the NMOS is off. Similarly, the NOR gate utilizes the negative edge of the CLK and clkb signals to briefly turn on M2. Hence, the NMOS transistor briefly sinks current while the M1 is off. The non-overlapping input signals from the NAND-NOR gates remove any short circuit current from Tx.

The Tx M1 and M2 device sizes are adjusted to supply/sink charge into/from the CDN. Depending on the size of load (number of sinks) and the size of chip, the device sizes need to be adjusted (discussed further in Section IV-C). The root wires of the CDN
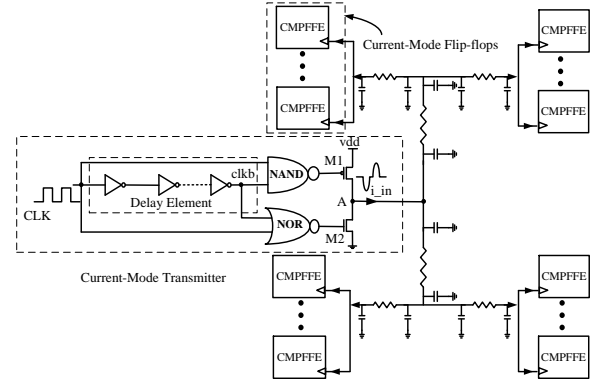
(a)
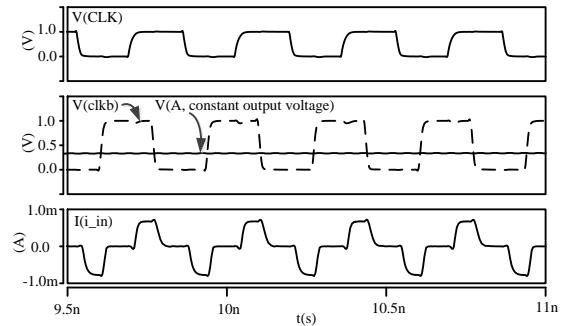
(b)

Fig. 6. (a) The proposed CM Tx and CDN converts an VM input signal to a push-pull current with minimal interconnect voltage swing and distributes current equally to the CMPFFEs and (b) simulation waveforms confirm a VM input is converted to a constant CDN voltage and a representative push-pull current at each CMPFFE.

carry current that is distributed to all branches so the sizing of CDN wires are critical for both performance and reliability. If the resistance of the wire is too high, the current waveform magnitude and period will be distorted and affect performance of the CMPFFEs. The wire width must also consider electromigration effects while carrying a total current to drive all the FFs with the required current amplitude and duration.

IV. EXPERIMENTS

A. Experimental Setup

We implemented our proposed CMPFFE, a traditional VM master-slave DFF (MS DFF), a traditional VM pulsed FF (Tra. PFF) [15], a high-performance conditional pulse-enhancement FF (CPEFF) [16], and a recently reported low-power dual dynamic node pulsed hybrid FF (DDPFF) [17] in FreePDK 45nm CMOS technology [18]. Each FF is compatible with a standard cell library height of 12 horizontal M2 tracks. The

Types of FF	Area (μm^2)	Delay (ps)			Total Power (static + dynamic) (μW)			
		CLK-Q	t_s	t_h	2 GHz	3 GHz	4 GHz	5 GHz
MS DFF	5.03	37.0	21.0	5.0	49	73	98	122
Tra. PFF [15]	7.48	75.5	-46.0	87.0	77	103	137	171
CPEFF [16]	7.75	25.0	-10.0	130	60	89	117	149
DDPFF [17]	9.86	33.0	-5.0	14	62	95	123	155
CMPFFE	7.34	40.3	-15.8	46.6	141	151	168	183

layout areas, maximum clock-to-Q (CLK-Q) delay, setup times (t_s), hold times (t_h), and total power are listed in Table I. The performance of the FFs was evaluated using post-layout SPICE simulation at clock frequencies from $2 - 5GHz$ with less than $10ps$ slew and a $1V$ supply voltage. The power considers input data at 100% activity and 4 minimum size inverter load.

In order to validate the functionality of the CM Tx and the proposed CMPFFE in a CDN, we implemented a symmetric H-tree network spanning $1.2mm \times 1.2mm$. Each branch of clock tree is modeled as a lumped 3-component Π-model and then connected together to make a distributed CDN model. The interconnect unit capacitance and resistance values are as suggested by 2009-2010 ISPD Clock Synthesis contest [19]. In addition, It is reasonable to model clock network as RC wires instead of RLC wires as suggest by 2010 ISPD Clock Synthesis contest [19]. The primary reason is the total clock network resistance is much higher than the total inductive reactance [20] for nominal global clock frequency range ($\leq 5GHz$). The functional simulation results with the resulting output current are shown in Figure 6(b).

B. CMPFFE Analysis

The CMPFFE consumes 5.3% and 26% less silicon area compared to the recently reported CPEFF and DDPFF, respectively. The proposed FF uses 25 transistors and the VM Tra. PFF and MS DFF use 26 and 20 transistors, respectively. While CPEFF and DDPFF use 23 and 22 transistors, respectively. In order to work in all process corners, we used 4 extra transistors in the pulse generation of the later 2 FFs. Figure 7 shows the layout of the proposed CMPFFE.

The CLK-Q delays of the FFs are measured under relaxed timing conditions – the data is stable sufficiently before the arrival of the clock edge. This applies both to the rising edge of the VM signal and the current pulse for the CM clock. In a VM FF, we considered 50%
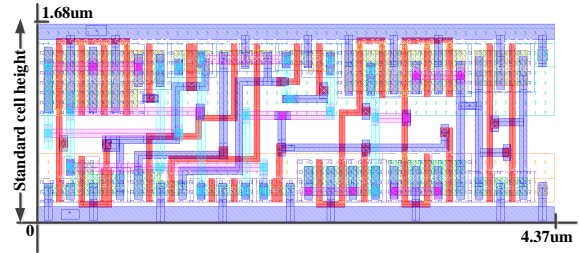

Fig. 7. Using standard cell height, the proposed CM FF consumes lower silicon area compared to the recently reported VM pulsed FFs [16], [17].

input clock transition to 50% FF output (Q) transition as the CLK-Q delay of a VM FF. Similar to a VM FF, in CM case we considered 50% ideal input current ($2.3\mu A$) transition to 50% Q transition as the CLK-Q delay of CM FF. Table I shows the maximum CLK-Q delay for both high-to-low and low-to-high Q transitions. Among all the FFs, the CPEFF has lowest CLK-Q delay. However, low CLK-Q delay and negative setup time also introduce large hold times for a FF. Clearly, the CMPFFE has lower CLK-Q delay than the Tra. PFF but is only slightly slower than the MS DFF. The DDPFF has 18% lower CLK-Q delay, but the proposed FF has 13% lower data-to-Q delay.

Figure 8 shows the Monte-Carlo simulations of CLK-Q delay of the proposed CMPFFE under varying process and mismatch conditions at $25°C$.

We also measured the t_s and t_h times for each FF. These use the common definition as the time margin that causes a CLK-Q delay increase of 10% beyond nominal. The t_s and t_h of the CMPFFE are $-15.8ps$ and $46.6ps$, respectively. The setup time of the CMPFFE is $1.75\times$ lower than the traditional MS DFF. In addition, recently reported CPEFF has $2.8\times$ more t_h compared to the proposed CMPFFE. The CMPFFE has $3.2\times$ better
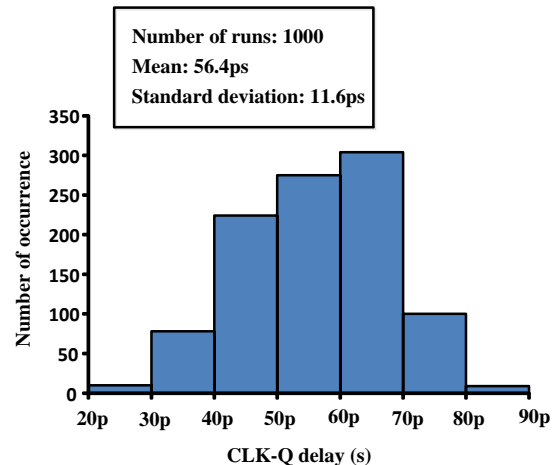

Fig. 8. The resiliency of the proposed CM scheme is demonstrated through non-uniform Monte-Carlo process variations and mismatch simulations.

TABLE II
THE RELATIVE SIZING OF CURRENT-MODE TRANSMITTER AT
FIGURE 6(A) INCREASES $6x$ IN EACH CASE.

No. of sinks	Chip-edge (mm)	Txs relative sizing
4	0.48	$W_{M1} = 1, W_{M2} = 1$
16	0.96	$W_{M1} \approx 6, W_{M2} \approx 6$
64	1.92	$W_{M1} \approx 36, W_{M2} \approx 36$
256	3.84	$W_{M1} \approx 216, W_{M2} \approx 216$
1024	7.69	$W_{M1} \approx 1296, W_{M2} \approx 1296$

t_s, but also has $3.3\times$ more t_h compared to the DDPFF.

Table I presents the total power including both static and dynamic. At low frequencies the CMPFFE consumes higher power than the Tra. PFF, CPEFF, DDPFF, and MS DFF due to a high static power overhead. However, the dynamic power of the CMPFFE increases proportional to the frequency at a slower rate than the other VM FFs. At high frequencies, the power consumption of the CMPFFE is comparable to the Tra. PFF and the CPEFF.

The FF power, however, does not represent the overall power consumption of a CDN because interconnect and buffers are major contributors. In Section IV-C, we show that the power savings in the CDN is worth the increase in CMPFFE total power despite the additional static power.

C. CM CDN Analysis

Total system power consumption of a CDN includes the CDN interconnect, buffer power and the FF power consumption. When measuring the total power consumption, we have considered different number of sinks distributed in different size chips followed by the references provided by 2009-2010 ISPD Clock Synthesis contest (i.e. sinks per unit area is the same in each case) [19]. In order to supply the required amount of current to each sink, we used different size Txs depending on the size of chip and number of sinks. Table II presents the Tx sizing for different number of load and chip size. Theoretically, the Tx size should increase $4\times$, since we are increasing number of sinks in the same manner. However, the chip size also doubled in each case, resulting approximately $6\times$ increase of Tx size. The control circuitry in the Tx may require size increases or buffers to drive a larger capacitive load when M1/M2 sizes in Figure 6(a) are increased.

In a VM CDN, the dynamic switching power of the interconnect and clock load capacitances along with clock buffers dominate the power consumption. In a CM CDN, the power due to small fluctuations in V_{CM} and the Tx power contribute, but the static power of the CMPFFE

dominates. In both cases, the number of sinks and chip dimensions increase the total power consumption.

We use the same H-tree model in both the CM and VM CDN, but buffers drive the VM CDN instead of the CM Tx circuit. The VM buffered network is optimized for an output clock signal with less than $20ps$ slew from $2 - 5GHz$. Since, the proposed CM FF is pulsed by nature, the VM CDN considers several pulsed FFs (Tra. PFF [15], CPEFF [16], DDPFF [17]) and also considers the MS DFF as reference. In order to facilitate normal CM FF operation, we used an active low ($\overline{EN}$) signal and also included the required routing power in the CM CDN power calculation.

Table III shows the power breakdown of the VM and CM CDN's simulation of clock frequencies ranging from $2 - 5GHz$. The total power consumption of CMPFFE system including $\overline{EN}$ signal routing, global reference routing, CM Tx, CMPFFEs power, and CM CDN power. On average, the CM CDN consumes less power than the VM CDN for all sizes of CDN at different frequencies. This is due to the large dynamic power consumption due to the voltage swing (0-to-V_{dd}) in the VM CDN, whereas the CM CDN has negligible voltage swing as shown in Figure 6(b).

Among different FF systems, the CM FFs consume higher power than the other VM FFs. However, VM interconnect power dominates the CM FF power even at small sizes. The real advantage is that the CM CDN power does not increase like the VM CDN power over frequency. Since the fluctuation of V_{CM} is relatively small, the dynamic power consumption of the CM CDN is negligible. At a low $2GHz$ clock frequency, the CM CDN system with number of CMPFFEs ranging from 4 to 1024 exhibits total power savings of 9% to 32% compared to a MS DFF system. At the same frequency, the proposed system with 1024 sinks shows a total power savings of 33% and 38% compared to the Tra. PFF system and CPEFF system, respectively. As expected and suggested by Table I, we observed a linear increase in total power savings with the increase of frequency using CM CDN compared to a VM CDN as in Figure 9. At $5GHz$ in particular, the CM CDN system exhibits 51% to 67% total power savings considering 4 to 1024 sinks. The primary reason behind that is at high frequencies the relative power consumption of the VM FFs and CMPFFE is nearly equal. At $2GHz$ the CM CDN system saves up to 33% average power compared to other VM CDN. While at $5GHz$ the CM CDN system saves 59% to 62% average power compared to other VM FFs (MS DFF, CPEFF, Tra. PFF, and DDPFF) system as shown in Figure 9.

In addition to dynamic power consumption of VM

TABLE III
POWER SAVING INCREASES WITH THE INCREASE OF FREQUENCY UTILIZING OUR CM CDN COMPARED TO OTHER VM CDNs.

Fre. (GHz)	# of sinks	CE[1] (mm)	Total CDN power (mW)		Total power consumption including FFs and CDNs (mW)					% Saving compared to			
			VM CDN	CM CDN	MS DFF sys.	Tra. PFF sys.	CPEFF sys.	DDPFF sys.	CMPFFE sys.[2]	MS DFF sys.	Tra. PFF sys.	CPEFF sys.	DDPFF sys.
2	4	0.48	0.72	0.26	0.92	1.03	0.96	0.97	0.83	9.82	19.63	13.95	14.66
	16	0.96	3.03	0.54	3.81	4.26	3.99	4.02	2.79	26.8	34.49	30.03	30.58
	64	1.92	10.62	1.13	13.75	15.54	14.46	14.58	10.16	26.14	34.66	29.74	30.36
	256	3.84	44.28	4.52	56.82	63.99	59.64	60.15	40.62	28.52	36.53	31.9	32.48
	1024	7.69	184.90	18.25	235.07	263.74	246.34	248.38	162.63	30.81	38.34	33.98	34.52
3	4	0.48	1.07	0.30	1.36	1.48	1.43	1.45	0.90	33.89	39.23	36.85	37.89
	16	0.96	4.23	0.58	5.40	5.88	5.66	5.76	3.00	44.42	48.96	46.94	47.82
	64	1.92	15.56	1.15	20.23	22.15	21.26	21.64	10.72	47.00	51.59	49.55	50.45
	256	3.84	66.51	4.91	85.19	92.88	89.29	90.83	43.64	48.77	53.01	51.12	51.95
	1024	7.69	270.02	19.78	344.77	375.49	361.16	367.30	174.71	49.33	53.47	51.62	52.43
4	4	0.48	1.13	0.33	1.52	1.68	1.60	1.62	1.00	34.26	40.37	37.38	38.3
	16	0.96	4.24	1.04	5.81	6.43	6.11	6.21	3.73	35.81	42.04	39.00	39.95
	64	1.92	21.88	1.20	28.15	30.65	29.37	29.75	11.94	57.58	61.03	59.34	59.86
	256	3.84	89.38	5.29	114.47	124.45	119.33	120.87	48.30	57.81	61.19	59.63	60.04
	1024	7.69	361.37	20.03	461.72	501.66	481.18	487.32	192.06	58.40	61.71	60.09	60.59
5	4	0.48	1.70	0.34	2.19	2.38	2.30	2.32	1.06	51.46	55.45	53.75	54.22
	16	0.96	7.18	1.38	9.13	9.92	9.56	9.66	4.31	52.83	56.56	54.96	55.40
	64	1.92	27.14	1.62	34.95	38.08	36.68	37.06	13.33	61.85	64.99	63.65	64.03
	256	3.84	112.05	5.78	143.28	155.83	150.19	151.73	52.65	63.26	66.21	64.95	65.30
	1024	7.69	453.62	20.37	578.55	628.72	606.20	612.34	207.76	64.09	66.95	65.73	66.07

CE[1]: Chip-edge, CMPFFE sys.[2]: Total power consumption of CMPFFE system including $\overline{EN}$ signal routing, global reference routing, CM Tx, CMPFFEs power, and CM CDN power.

and CM CDN, we also measured the static power consumption of the largest CDN network with 1024 sinks. The total static power consumption for CM CDN with no clock activity is $154\mu W$. In the same conditions, the total static power consumption of the VM CPEFF system is $186\mu W$. The results are nearly the same and the difference is negligible compared to the dynamic power consumption of each CDN.

D. Reliability Analysis

Unlike an exponentially tapered H-tree [21], we used homogeneous wire sizing from the root to each sink, and verified the maximum current density of CM CDN in the root wire to be $0.275 MA/cm^2$ which is less than VM CDN, $0.53 MA/cm^2$. This more than satisfies the ITRS suggestion that current density be limited to $1.5 MA/cm^2$ [22]. Therefore, electromigration is not a problem for the demonstrated sizes.
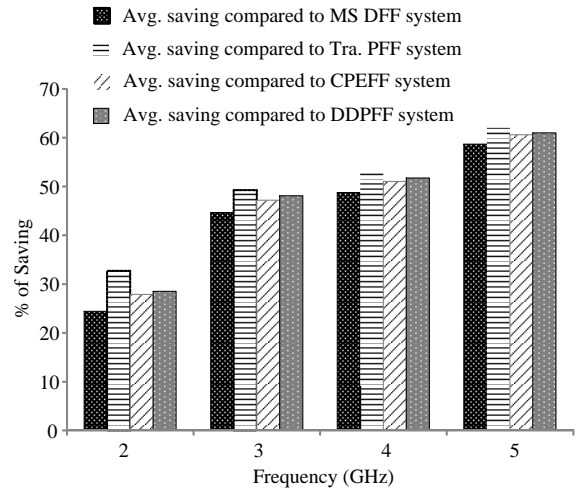

Fig. 9. The average power savings of the CM CDN system increases proportional to the frequency compared to the other VM FF based CDN scheme Table III.

E. Noise Analysis

In order to measure the noise immunity, we compare crosstalk noise simulations for both CM and VM.
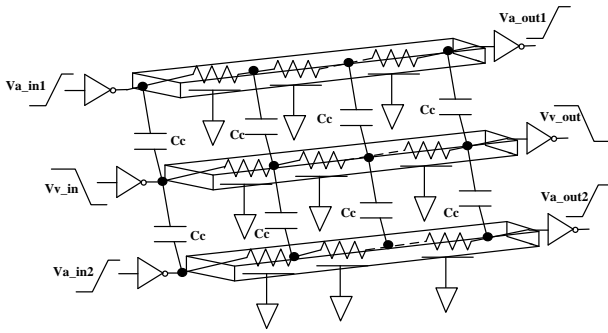
Fig. 10. Traditional VM schemes are most susceptible for crosstalk noise, when the aggressors are $180°$ out of phase compared to the victim line.

Figure 10 shows the testbench to analyze the effects of crosstalk noise on traditional VM buffer driven interconnects. This experiment is commonly used to quantify the effect of coupling capacitance on dynamic delay due to the switching activity of neighboring nets that have significant coupling to the original circuit. In scaled technologies, traditional VM schemes are most susceptible when the aggressors are $180°$ out of phase compared to the victim line. Figure 10 mimic the worst case crosstalk by considering 3 parallel inter-connections ($5mm$ long) driven by variable impedance drivers/buffers (VM). Hence, the victim line experience an effective capacitance which is double than the original coupling capacitance. Each $5mm$ interconnect line was buffered/segmented every $1mm$. In this case, simulation shows that victim line delay can increase up to 35%. In the CM design, two aggressors are driven by VM buffers, while the victim line is a CM Tx. Simulations suggest that the CM scheme exhibits negligible performance penalty and more robustness to noise because the CM victim line has a much larger capacitance without buffer-ing. This means that the relatively short neighbouring VM aggressor lines have less crosstalk coupling and therefore less influence on CM delay. Unlike VM CDN, the CM CDN requires a global reference voltage and active low enable ($\overline{EN}$) signal routing for the CMPFFEs. Since, the centralized reference voltage and EN signal both are constant voltage, these have minimum effect due to crosstalk noise. In addition, the wire cap is large so it is not affected much.

F. Variability Analysis

Transistor threshold voltage (V_{TH}) may be affected by variations in doping concentration, gate oxide thick-ness, gate length effective dimension, etc. [23]. Unlike crosstalk noise, V_{TH} mismatch can introduce large skew in clock network. Hence, quantifying V_{TH} induced clock skew is very critical for reliability of the clock network.

We considered the worst case corner for both the CM and VM CDN. For CM, this is with V_{TH} variation only
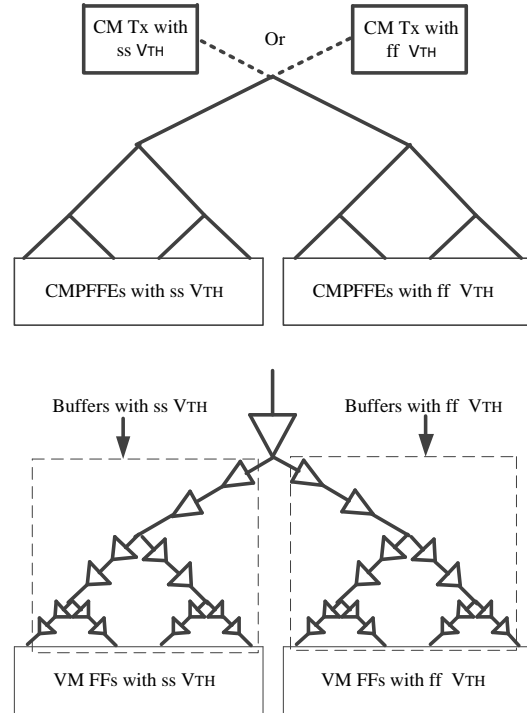

Fig. 11. In ss-ff corner, the proposed CM CDN has up to 60% less skew compared to other VM CDNs.

in the CM Tx and CM FFs because it does not use other buffers. However, the CM Tx is shared and adds zero skew. For VM, this includes variation in the VM FFs and the clock buffers. Traditionally, clock skew is measured at the clock pins of the FFs. However, we wanted to include the impact of variability on our new FF so skew is measured at the FF output. This effectively includes CLK-Q variation in addition to normal clock skew variation. Figure 11 shows an example to calculate skew due to V_{TH} variation at ss-ff corner. In CM CDN, we calculated the time delay considering input CLK signal transition of the CM Tx and the output of both CMPFFEs with ss V_{TH} and ff V_{TH}. The delay difference is the skew in CM case. Similarly, we calculated the skew in VM CDN considering CLK transition at the root buffer to the output of VM FFs with ss V_{TH} and ff V_{TH}.

Table IV shows the effect of worst corner V_{TH} vari-ation on different CDN skews. The traditional VM MS DFF, CPEFF, and DDPFF based CDN show comparable skew at all corner variations. In the ff-ss corner, the CM CDN clock has $17ps$ skew while classic MS DFF based VM CDN has $33ps$. In addition, the proposed CMPFFE-based CM CDN exhibits 51% and 60% less skew compared to the CPEFF and Tra. PFF based CDN, respectively. This is due to fact that the VM CDNs uses buffers to distribute the highly capacitive clock to the sinks.

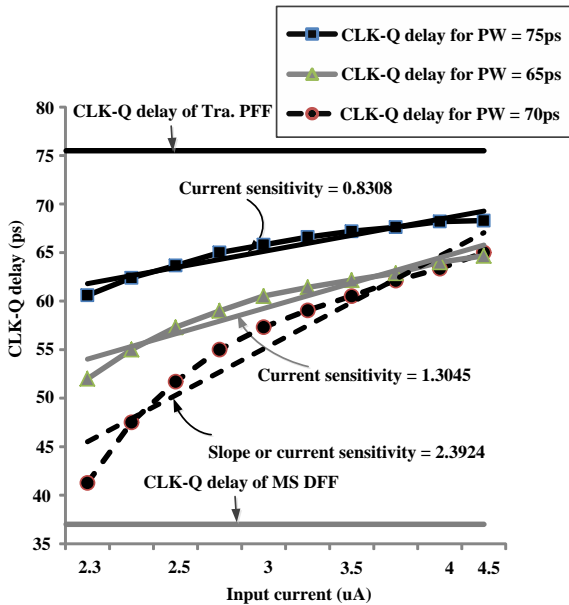As mentioned earlier, the performance of CMPFFE is

Fig. 12. The CMPFFE current sensitivity on CLK-Q delay is within the nominal CLK-Q delay of traditional VM MS DFF and Tra. PFF.

sensitive to the width and amplitude of its input current (i_in). We performed numerous simulations aimed at determining the sensitivity of the clock to output delay of the CMPFFE as function of the input current. Figure 12 shows the variation of this CLK-Q delay relative to input current amplitude and pulse width (PW) variations. We define the current sensitivity of the CLK-Q delay as the slope of the approximated linear trendline of the CLK-Q delay curves. We utilized the minimum input current (i.e. $\pm 2.3 \mu A$) and varied it up to $2\times$ considering different PW. At $PW = 70ps$, the current sensitivity on the CLK-Q delay is the highest and while providing the lowest CLK-Q delay compared to the other PWs. On the other hand, at $PW = 75ps$ the current sensitivity of CLK-Q delay is the lowest but provides the highest CLK-Q delay in comparison to other PWs. The delay variation, however, is within the nominal CLK-Q delay of traditional VM MS DFF and Tra. PFF. Hence, the proposed CMPFFE has a wide input current range while maintaining the optimal performance. This current sensitivity analysis is helpful towards understanding the performance tradeoffs in the proposed CMPFFE with respect to the input current, and guides the early stage design of the current Tx.

G. Supply Voltage Fluctuation

Due to the spatial variation it is possible that the power supply or V_{dd} could vary at different locations of the chip. Traditionally, designers utilize $\pm 10\%$ supply voltage fluctuation from the nominal value. Table IV shows effect of the supply voltage fluctuation ($\pm 10\%$ deviation

TABLE IV
THE PROPOSED CM CDN HAS LOWER SKEW DUE TO SUPPLY VOLTAGE AND THRESHOLD VARIATION COMPARED TO RECENTLY REPORTED PULSED FF BASED VM CDN SCHEMES.

CDN with	Skew (ps)		
	Supply voltage variation		Threshold voltage variation
	$V_{dd} = 0.9V$	$V_{dd} = 1.1V$	ff-ss
MS DFF	10	-18	33
Tra. PFF [15]	12	-21	43
CPEFF [16]	11	-17	35
DDPFF [17]	13	-17	34
CMPFFE	-4	15	17

from 1V supply) on the various CDNs' performance. Similar to the V_{TH} variation, we considered performance metric of CDNs considering the delay variation from root to FFs output. When the supply voltage is low ($0.9V$), the VM CDN and VM FFs have a positive skew from the nominal supply. The primary reason is the lower overdrive voltage ($V_{GS} - V_{TH}$). On the other hand, applying high supply voltage ($1.1V$) in VM CDNs exhibits a negative skew from the nominal case. However, at $0.9V$ supply the proposed CM CDN shown a negative skew compared to the nominal supply voltage. While at $1.1V$, the proposed scheme exhibits a positive skew. This is due to the operating point variation of the CMPFFE and also validates our current sensitivity analysis. Overall, the proposed CM CDN has a lower or comparable skew compared to the other VM CDNs.

V. CONCLUSION

In this paper, we presented the first true CM FF and its usage in a fully CM CDN. The proposed CMPFFE is 87% faster, requires similar silicon area and consumes only 7% more power compared to a traditional PFF at $5GHz$. Better yet, the CMPFFE enables a 24% to 62% power reduction on average when used in a CM CDN compared to conventional VM CDNs. The CMPFFE also eliminates the need for complex CM Rx circuitry and/or local VM buffers to drive highly capacitive clock sinks as in previously proposed CM signaling schemes.

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