UNIVERSITY OF CALIFORNIA SAN DIEGO

High Performance CMOS SOI Gbps Millimeter-Wave Transceivers, Phased-Arrays and Switching Networks

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Professor Patrick Mercier

2018

The dissertation of Yang Yang is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2018

DEDICATION

To my wife, Mengfei Li.

To my parents, Nanzi Xie and Xun Yang.

To my Father in heaven.

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PUBLICATIONS

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Y. Yang, O. Gurbuz and G. M. Rebeiz, "A 8-element 400 GHz phased-array in 45 nm CMOS SOI," in *Microwave Symposium (IMS), 2015 IEEE MTT-S International*, May 2015.

Y. Yang, S. Zihir, H. Lin, O. Inac, W. Shin, G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45nm CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC)*, June 2014.

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ABSTRACT OF THE DISSERTATION

High Performance CMOS SOI Gbps Millimeter-Wave Transceivers, Phased-Arrays and Switching Networks

by

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University of California San Diego, 2018

Professor Gabriel M. Rebeiz, Chair

With the CMOS process technology progress, transistor can achieve up to 260 GHz f_t and f_{max} referenced to the top metal, which makes it possible to develop lower cost circuits and blocks for THz high speed implementations such as active imagine system, short distance chip to chip communication systems, and large scale high speed ultra low power switch networks. The dissertation shows an 8x1 phased array transmitter working at 370-410 GHz with peak EIRP of 8.5 dBm, a QPSK modulated 20 Gbit/s transceiver front end (including modulator, voltage control oscillator, power splitter, doubler, mixer and wide-band baseband amplifier.) at 155 GHz and two cross connected high speed ultra low power switch matrices (an 8x8 matrix up to 25

Gbit/s matrix and a 16x16 matrix built using four 8x8 matrix). All circuits and blocks are built using the Global Foundries 45 nm CMOS SOI (silicon on insulator) process.

Chapter 1

Introduction

The potential of building large-scale imaging arrays and high data-rate communication links at relatively low cost makes designing transmitters and receivers using silicon SiGe and CMOS technologies in millimeter-wave (mm-wave) and terahertz (THz) an active area of research.

For imaging systems, silicon allows the construction of single chip focal-plane arrays with integrated antennas and detectors, together with all the multiplexing and readout electronics, thus reducing the system cost. Silicon also results in high yield and in uniformity from pixel-to-pixel, which is a prerequisite for fully integrated systems.

For communication systems, silicon offers acceptable performance up to 150-300 GHz for front end blocks such as mixers and modulators. The smaller device parasitics due to the technology progress also makes wideband IF circuits design possible. Those circuits and blocks are essential to be paired with the front end blocks for a whole system. Though SiGe and CMOS designs are still not as competitive as their GaAs counterparts, they are good enough for short distance communication systems and low power portable measurement equipments.

Meanwhile, in order to route the massive amounts of data for those new developed high speed circuits or to ease the increasing data traffic in current communication networks, switches are needed with the highest possible throughput. For the greatest versatility and performance

it is critical that the switches also added little jitter to the signal and meet the reconfigurability requirements. Cross-point switches with both passive and active circuits used in combination to improve both fan-out capability and lower power consumption,

Accurate modeling of the interconnections and extraction of the parasitics are essential for high frequency circuits design. Careful system level budget and integration is required for a working system or sub-system.

Chapter 2 presents an 8-element 400 GHz phased-array in 45 nm CMOS SOI. The phased-array transmitter delivers 8 dBm EIRP with a 3-dB bandwidth of 40 GHz and it is able to be scanned to +/- 35^o in one plane. This multiple multipliers coupled with no-chip antenna elements and quasi-optical combining technique provide the solutions that silicon technologies is weak in power generation in the THz domain (>300 GHz). The design is also capable to be scaled up to larger sized phased-array. To our knowledge, this is one the first demonstrations of a phased array operating at 400 GHz using CMOS technology and with wide operating bandwidth.

Chapter 3 presents an 155 GHz 20 Gbit/s QPSK transceiver front-end includes modulator, demodulator, LO chain with an option for external LO feed. It is intended for short distance high speed wireless communication link and is the first demonstration of a single-chip QPSK transceiver in CMOS at frequencies above 100 GHz. To achieve higher speed with lower power consumption is always the goal for wireless technology. There are mainly two ways to increase the data-rate of a system. One is to increase the signal-to noise ratio and hence high order modulations can be implemented. However, the signal to noise ratio requirement drastically increases as the modulation order increases. The more straightforward way is to increase the bandwidth which becomes the motivation for this D-band transceiver design. The transceiver consumes 345 mW with on-chip LO (290 mW without LO) and is 2.8x1.4 mm^2 in size with pads.

Chapter 4 presents a 0.24 pJ/bit, 30 Gbit/s 8x8 single-ended cross connection switch matrix and a 16x16 matrix built using four of the 8x8 cells which can achieve 20 Gbit/s per channel. The motivation for the research is towards ultra low power consumption and scalable

unit cell for large scale matrix. The core circuits of the 8x8 matrix is only 120x120 μm^2 in size and consumes 7.2 mW per channel. In order to lower the power consumption, passive cross point switch core with input and output buffer structure is investigated. Loaded transmission line routing mode as well as tradeoff among speed, power consumption and size limitation of passive switches array are analyzed. Measurement results for different channels at different rates are showed and the limitation of the measurement setup is discussed.

The thesis concludes with a summary and future work suggestions in Chapter 5.

Chapter 2

Millimeter-Wave Phased-Arrays

2.1 Introduction

The use of silicon SiGe and CMOS technologies in millimeter-wave and terahertz (THz) transmitters and receivers has been an active area of research due to the potential of building large-scale imaging arrays and high data-rate communication links at relatively low cost [1–18]. For imaging systems, silicon allows the construction of single-chip focal-plane arrays with integrated antennas and detectors, together with all the multiplexing and readout electronics, thus reducing the system cost. Silicon also results in high yield and in uniformity from pixel-to-pixel, which is a pre-requisite for fully integrated systems. For communication systems, silicon offers acceptable performance for mixers and modulators up to 150-300 GHz [19–21], and while these are not as competitive as their GaAs counterparts, they are good enough for short distance communication systems.

A weak point of silicon technologies is the difficulty of generating of adequate transmit power and EIRP in the THz domain ($>$ 300 GHz). SiGe and CMOS multipliers and oscillators have been successful at generating an output power of 20-21 dBm at 110-130 GHz and 2-8 dBm up to 250 GHz [22]- [23], but the transmit power quickly falls off above 250 GHz due to

the transistor f_t and f_{max} (which is typically in the 250-300 GHz range). Therefore, in order to increase the radiated power, multiple oscillators or multipliers, coupled with on-chip antenna elements, have been used. The quasi-optical combining technique eliminates the lossy on-chip transmission-lone combiner, results in 100% combining in free space and increased the EIRP by a factor of N^2 [14], [24], [25]. It is also well suited for on-chip THz systems since the antenna spacing is 0.3-0.5 mm. The array approach also leads to a straightforward phased-array transmitter if the phase at each element is controlled independently, resulting in a wafer-scale phased array [25], [26].

This paper presents the first 360-410 GHz 8-element linear phased array transmitter in 45nm silicon SOI, and is an expanded version of [27]. The design is based on W-band phase shifters and amplifiers coupled with x4 multipliers for frequency up conversion, and with on-chip high-efficiency microstrip antennas. The transmitter is capable of operating over a 30 GHz bandwidth with an EIRP $>$ 5 dBm a peak EIRP of 7-8 dBm at 380-400 GHz, and results in phased array patten scanning to +/- 35° in one plane.

2.2 Design and Single Block Measurements

2.2.1 System Architecture

Fig. 2.1 presents the block diagram of the 8-element phased-array transmitter. The 90-105 GHz input signal is divided into 8 different paths using Wilkinson splitters and amplifiers and fed to vector modulators. The phased-shifted output then pass again by high-efficiency W-band amplifiers and is fed into a x4 quadruplers with an output at 360-420 GHz. The distance between the quadrupler and the antenna is kept very short so as to minimize the transmission-line loss.

This architecture results in two design criteria which are important for large-scale phased arrays: a) The entire chip is at W-band frequencies with high-gain amplifiers and relatively low transmission-line loss, making it scalable to 16 or 64 elements, b) the W-band signal needs to be

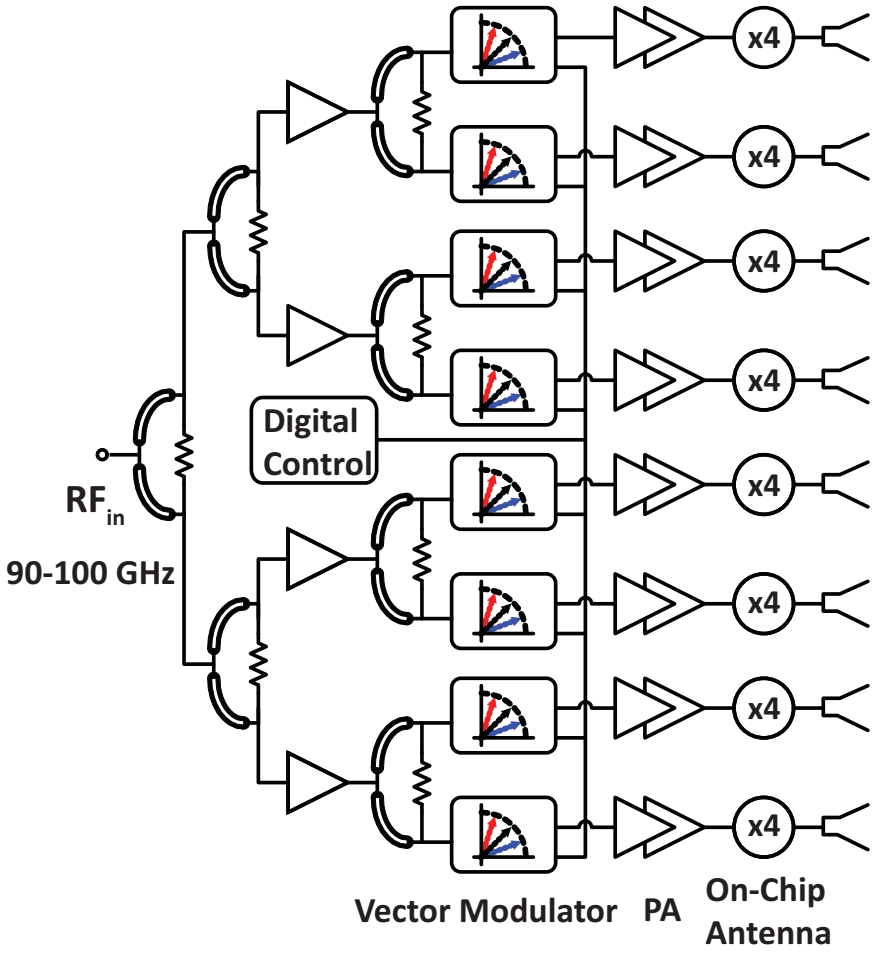


Figure 2.1: Block diagram of the 400 GHz phased-array transmitter.

controlled in a single quadrant only, that is 0-90°, since the x4 multiplication factor will expand the phase shift into 0-360°. Therefore, the phase shifter can be implemented as a single-ended vector modulator as opposed to the standard differential vector modulators used in mm-wave designs [28]. The entire chip is therefore designed in a single-ended configuration and this results in lower power consumption than differential designs. The use of a single-ended topology is also compatible with high-efficiency on-chip microstrip antennas.

For simplicity and ease of scalability, only four different components are used in the entire system: 1) Wilkinson combiner, 2) W-band amplifier, 3) W-band vector modulator and a 4) quadrupler. The components are all designed to be 50 Ω matched, and therefore are easily connected together without re-designing their input and output matching networks. This may not be as efficient as complex conjugate matching, but it results in wideband designs and is less sensitive to design error. Also, each component can be independently characterized using break-out circuits.

Note that the x4 architecture in the signal path does not allow for complex modulation signals such as 16QAM, and is more suited for continuous wave (CW), amplitude modulated (AM or OOK) or frequency shift systems (FSK, FMCW, etc.). However, if triplers are used instead of quadruplers, then a QPSK constellation can be supported as demonstrated in [19].

2.2.2 Technology

The Global Foundries (GF) 45nm CMOS SOI technology is used due to its high f_t, f_{max} transistors, 11 metal layers with copper metals and tungsten vias, and with thick dielectrics and thick metals for the top layers (Fig. 2.2). The technology results in an f_t and f_{max} of 240-260 GHz referenced to the top metal and a maximum available gain (MAG) of 6.1 dB at 94 GHz [29]. In this design, the microstrip transmission line is built usinfg the LB metal for the signal line and B2/B3 metals tied for the ground plane.

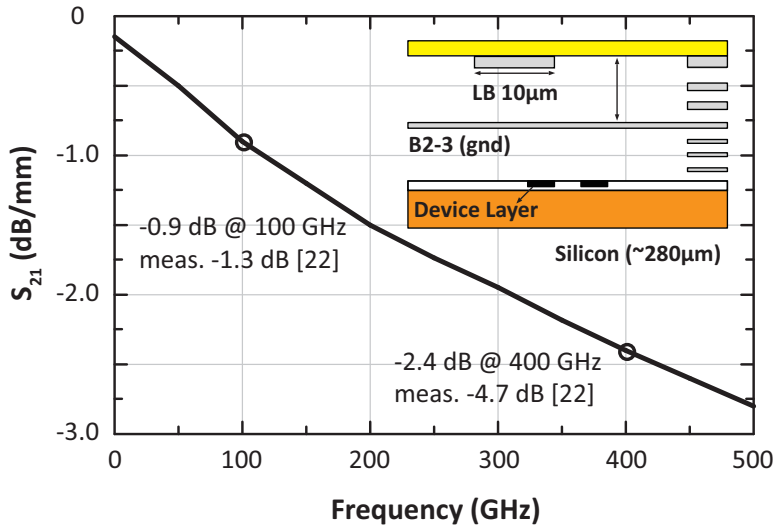


Figure 2.2: GF 45 nm SOI process. and simulated loss of a 1 mm long 50 Ω microstrip line.

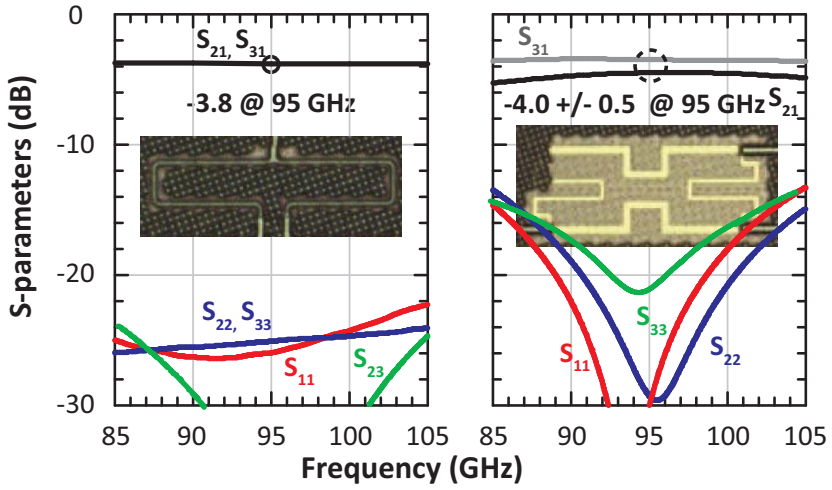


Figure 2.3: Simulated S-parameters of W-band Wilkinson and hybrid couplers. The wilkinson coupler is 348 x 63 μm^2 and hybrid coupler is 368 x 138 μm^2.

A 50 Ω line is 10 μm wide with a simulated loss of 0.9 dB/mm at 100 GHz (Q = 21) and 2.3 dB/mm at 400 GHz (Q = 7.5). Previous results found that the measured transmission line losses are 30-40% higher than simulations up to 110 GHz [29], [30]. However, measurements in [30] also show that the transmission line loss is 4.7 dB/mm at 400 GHz which is double the simulated values (investigations are currently under way to determine the mechanism for this additional loss, and it could be due to the thin high-resistivity adhesion layers used in advanced CMOS processes at every metal layer). This is the reason why the connection between the quadrupler and antenna is made as short as possible ($<$ 30 μm), and the high 400 GHz transmission-line loss has virtually no effect on the phased-array performance.

2.2.3 Wilkinson and Hybrid Couplers

Fig. 2.3 presents the Wilkinson power divider and the 90° hybrid coupler built using 35 Ω, 50 Ω and 70.7 Ω transmission lines, and simulated using Sonnet EM Suite (version 13.54). The hybrid coupler is required in the vector modulator for the 0-90° signal generation. The Wilkinson divider has excellent impedance match and isolation over a wide bandwidth and results in an insertion loss of 0.8 dB at 95 GHz (assuming 0.9 dB/mm loss at W-band). The hybrid coupler is also well matched with an insertion loss of 1.0 dB at 95 GHz and an amplitude and phase error of $<$ +/-0.5 dB and 2°, respectively at 90-100 GHz. There is $<$ 0.2 dB difference in the device insertion loss if a transmission line loss of 1.3 dB/mm is used due to the λ/4 line lengths at 100 GHz is 375 μm.

2.2.4 W-band Amplifier with High PAE

Fig. 2.4(a) presents the three-stage W-band amplifier used in the Wilkinson divider network and as a driver to the x4 quadrupler. The design is based on common source amplifiers with complex conjugate matching between the different stages. A single-contact finger length of 1

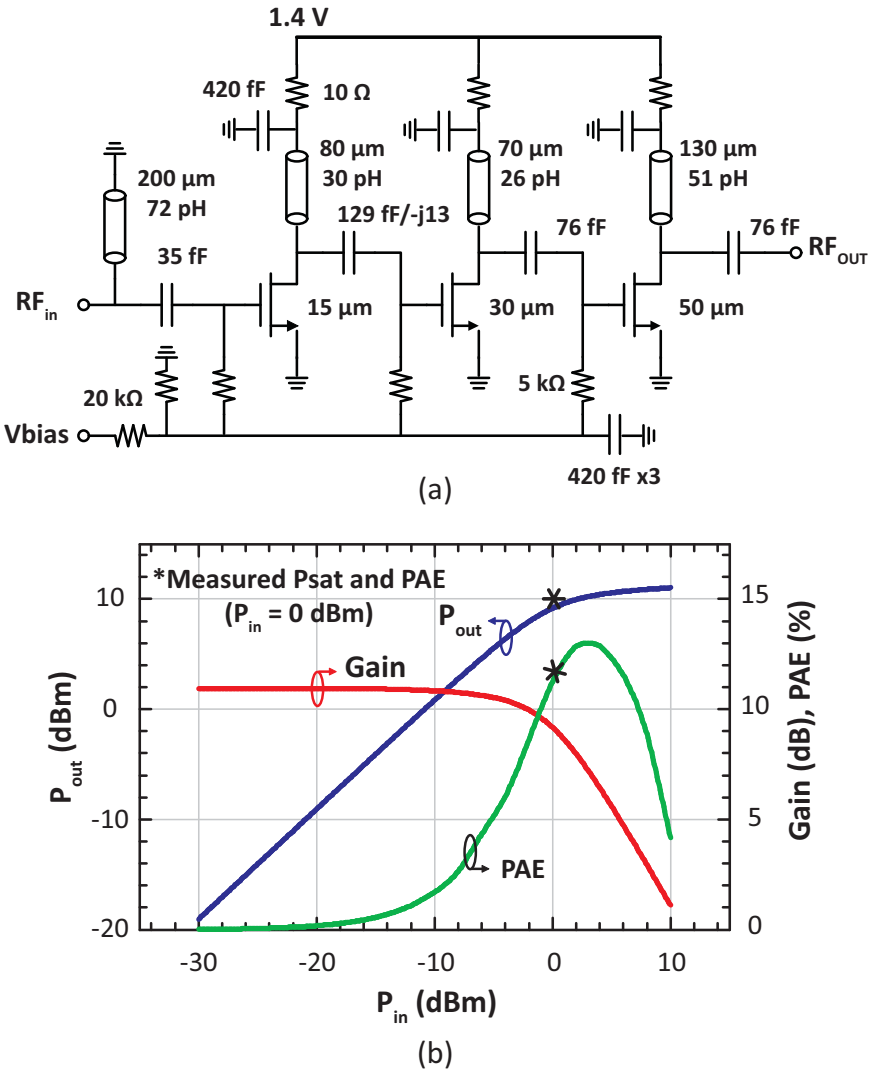


Figure 2.4: W-band amplifier: (a) schematic and (b) simulated gain output power and PAE at 95 GHz.

μm is used in all designs which results in an f_t/f_{max} of 240/250 GHz for the 30 μm transistor [29]. The stub loads are built using 50 Ω lines with a Q of ∼12 (degraded from 21 due to the via interconnection to ground) at 95 GHz, and the interstage matching capacitors are multi-finger metal-oxide-metal designs with a Q of 20 and 10 for a capacitance of 70 fF and 130 fF, respectively, at 95 GHz (Fig. 2.5). The GF 45nm SOI technology does not offer MIM high-Q capacitors and the matching capacitors introduce 1-1.5 dB of additional loss. The output stage is 50 μm wide for a saturated output power of 10 dBm and is biased at 19.6 mA. The simulated small-signal gain is 12 dB at 95 GHz with a 3-dB bandwidth of 85-107 GHz. The interstage conjugate match is staggered in frequency so as to result in a wideband design but at the expense of a slightly lower gain.

Note that 10 Ω resistors are present on the drain network and are mainly for stability since all the amplifiers employ the same V_{DD} and ground planes. Also, two W-band amplifiers are used after the vector modulator with a small-signal gain of 23 dB.

Fig. 2.6 presents a stand-alone W-band amplifier and its measured S-parameters. Calibration is done using SOLT (short-open-load-through) to the probe tips and the gain includes the GSG (ground-signal-ground) to CPW (coplanar waveguide) transition loss of 0.5 dB. The measured peak gain is 15 dB at 87 GHz with a 3-dB bandwidth of 85-95 GHz. This was obtained on several samples and indicates that the staggered wideband matching was not well optimized (most probably due to the interdigital capacitor models), and thus the higher gain and narrower bandwitdth. The measured P_{sat} is ∼10 dBm at 95 GHz and the associated PAE (power added efficiency) is ∼12%. This was done at P_{in} = 0 dBm using the vector network analyzer extender as a W-band source and is shown in Fig. 2.4(b). This PAE is competitive among medium power amplifier in CMOS at 10 dBm output power [31–33].

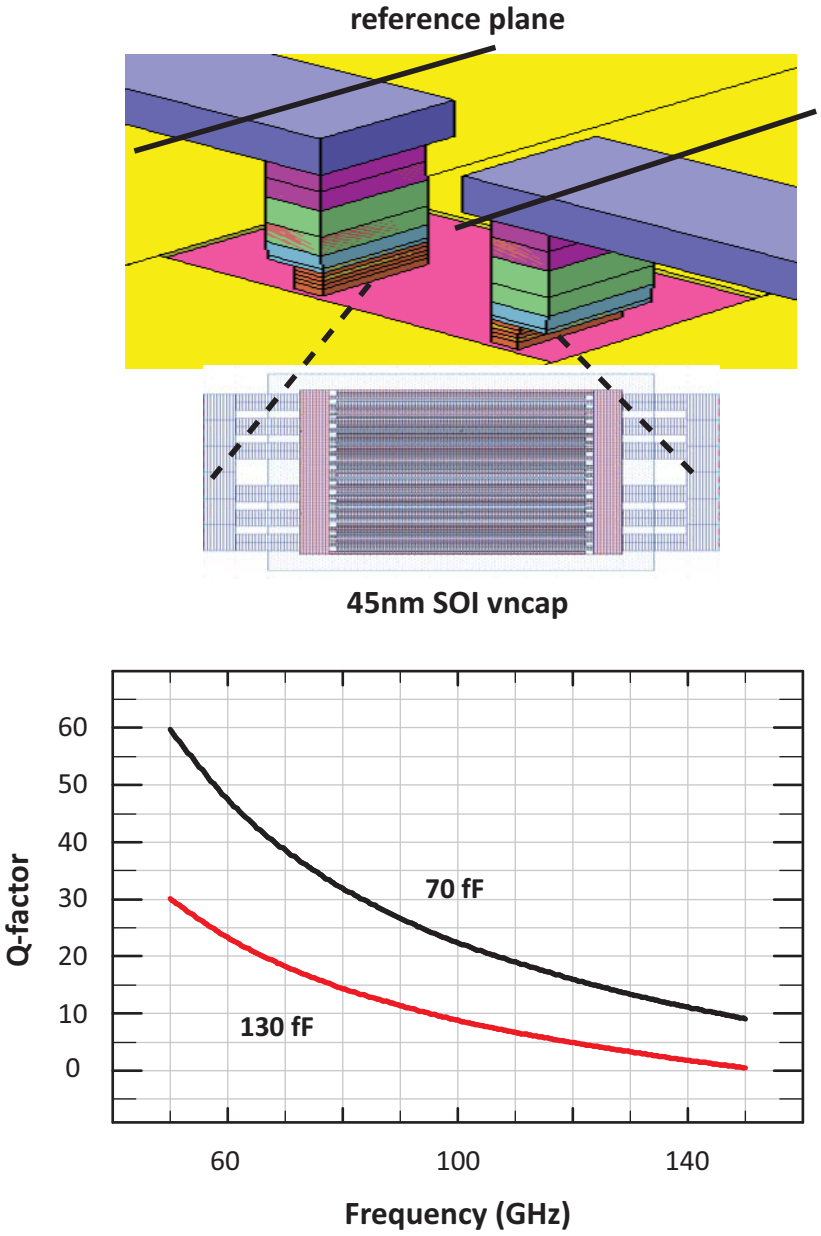


Figure 2.5: Simulated Q-factor of 45nm SOI capacitors (vncap) versus frequency.

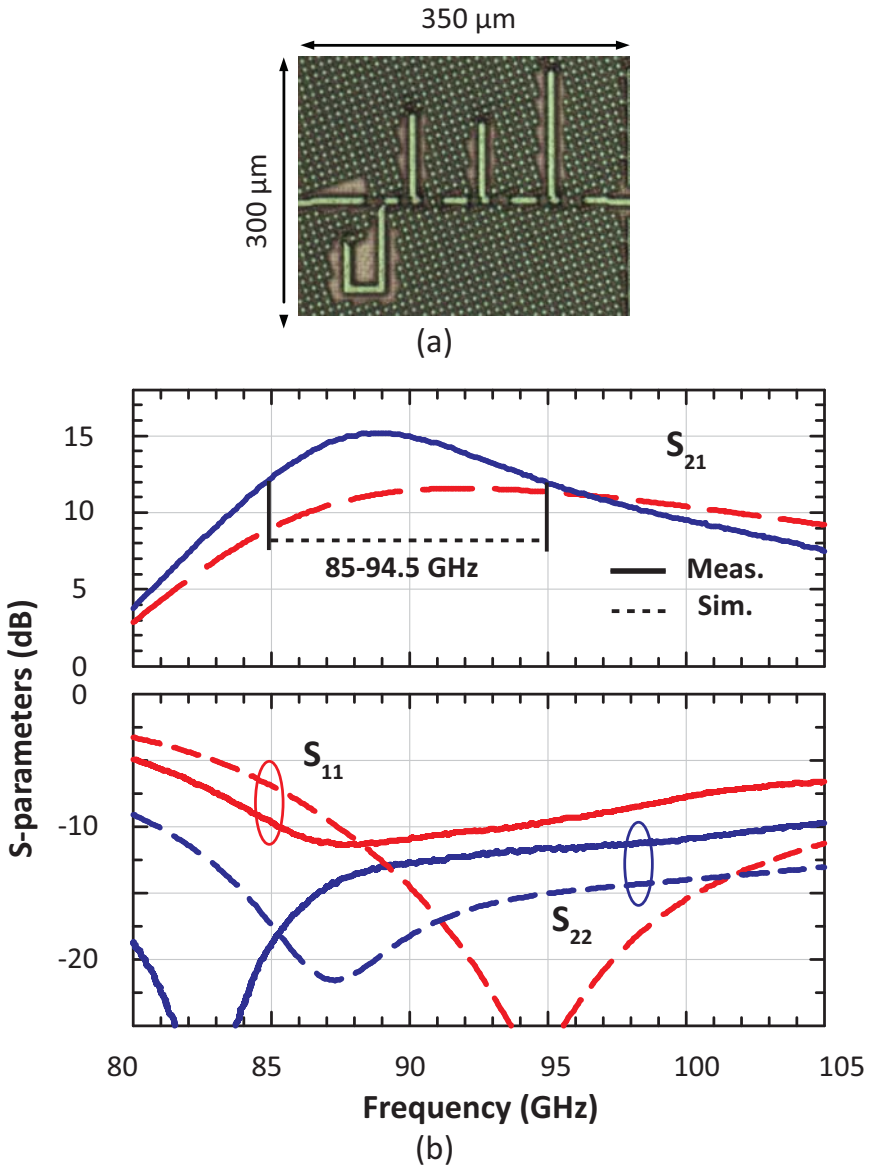


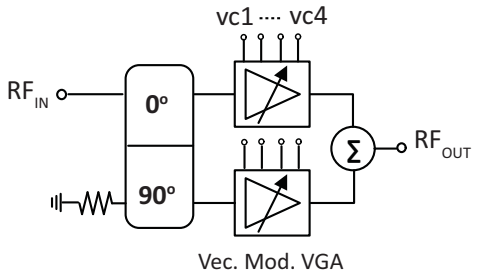
Figure 2.6: (a) W-band amplifier microphotograph, and (b) measured S-parameters. The 3-dB bandwidth is 85-94.5 GHz.

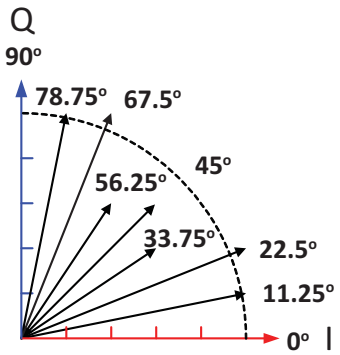
2.2.5 Vector Modulator

The W-band vector modulator is implemented by summing the in phase (I) and quadrature (Q) signals from the hybrid coupler (Fig. 2.7). The lower transistors M1, M2, M3, M4 in the cascode vector modulator generate the required currents in four different magnitudes, and the upper transistors steer the current between the supply and the output node [34]. Compared to a VGA (variable gain amplifier) with tail current control, this topology handles a higher input power and results in a constant input P_{1dB} of +3 dBm. The 3-bit phase shifter requires current levels of 0 (all off), 1, 2, 3 and 5 mA and these are synthesized using M1-M4 with different sizes. Note that this simple vector modulator topology results in $\sim$3 dB amplitude variation which can be compensated using a VGA stage. However, in this work, the driver amplifiers after the phase shifter operate in saturation mode and are not affected by this amplitude variation. The input and output of the vector modulator are matched to 50 Ω using a shunt stub and a series capacitor (LC network). The simulated S_{11} is independent of the phase state and is $<$ -10 dB at 75-110 GHz. The simulated gain is -6 +/- 3 dB for a power consumption of 31 mW and an output power of -3 +/- 3 dBm.

Fig. 2.8(b) presents the measured results of a stand-alone W-band vector modulator breakout. The conversion gain is -16 +/- 2 dB at 95 GHz which is 10 dB lower than simulated, and is due to a poorly defined ac ground at the upper transistor gates caused by a layout error. The measured 3-bit phase response is shown in Fig. 2.8. The phase shifter operates well with an RMS (root mean square) error of 5.4^o with 0^o being reference phase. The RMS phase error is calculated as:

$$\Phi_{rms} = \sqrt{\frac{\sum_{i=1}^{n} (\Phi_{measi} - \Phi_{ideali})^2}{n}} \tag{2.1}$$





Θ	0°	11.3°	22.5°	33.8°	45.0°	56.3°	67.5°	78.8°	90°
tanΘ	0	~0.20	~0.41	~0.67	1	~1.5	~2.4	~5.0	∞
I (mA)	5	5	5	3	3	2	2	1	0
Q (mA)	0	1	2	2	3	3	5	5	5

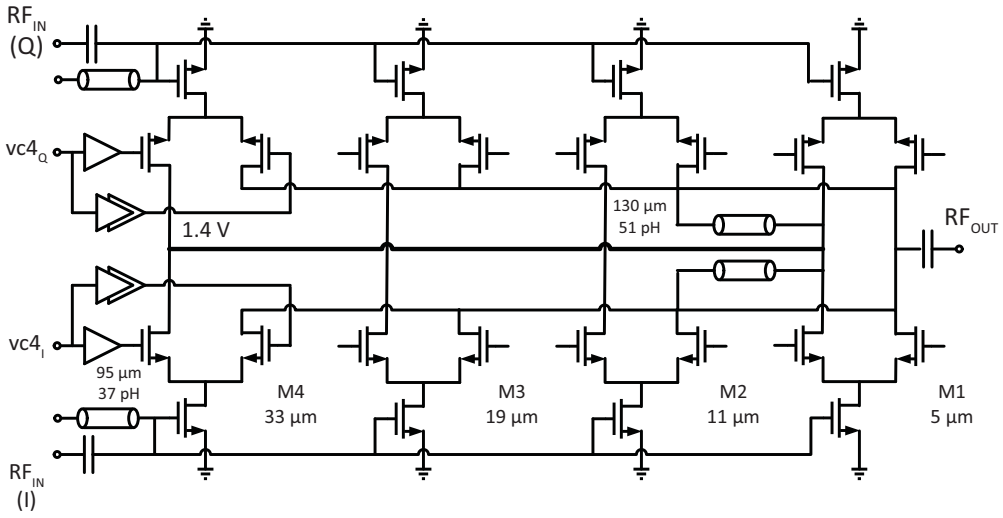


Figure 2.7: Vector modulator VGA with discrete transistors for 3-bit control in the 0-90^o quadrant.

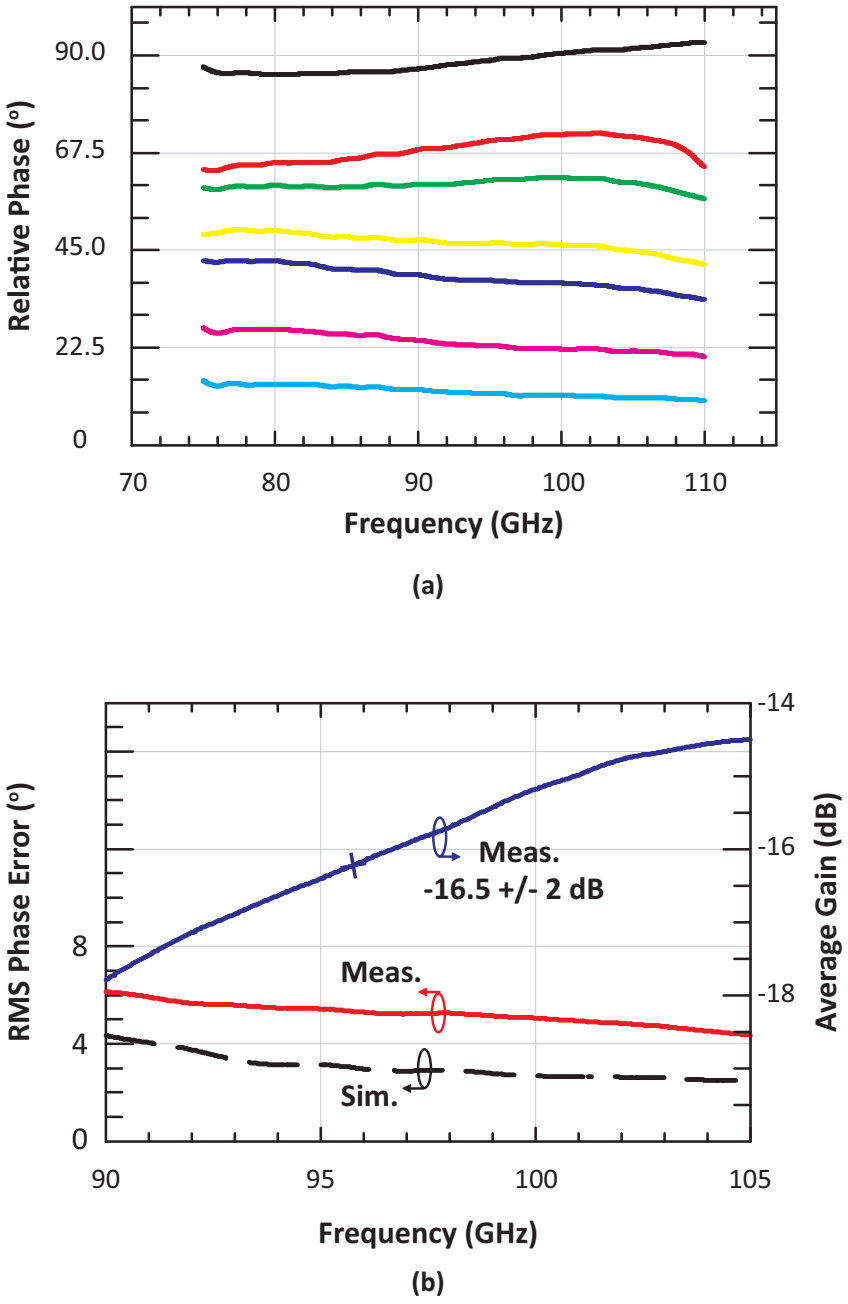


Figure 2.8: Vector modulator measurements: (a) Relative phase, and (b) gain and RMS phase error.

2.2.6 Quadrupler

The quadrupler is based on a balanced multiplier biased in a class C mode with a second harmonic choke, and results in a conversion gain of -20 dB at 390-410 GHz for an input power of 10 dBm (Fig. 2.9). Details of the design can be found in [14]. The quadrupler consumes 15.4 mW from a 1.4 V supply. The measured quadrupler output power is -10 dBm at 400 GHz when driven by a W-band amplifier with a P_{sat} of 10 dBm. Note that at 360 GHz, the conversion loss is 26 dB resulting in an output power of -16 dBm.

2.2.7 High-Efficiency On-Chip Antenna Array

For high transmit power and EIRP, it is essential that a on-chip high-efficiency antennas be used. A microstrip antenna directly integrated on the 45nm back-end with a 6.8 μm of SiO_2 dielectric results in a simulated peak radiation efficiency of 20% and an antenna gain of -2 dB to 0 dB at 360-400 GHz (Ansoft HFSS v14 is used for simulations). In order to improve the radiation efficiency, a $\lambda/4$-thick quartz superstrate is used on top of the microstrip antenna (Fig. 2.10). Note that there is no metal defined on the quartz superstrate, and the superstrate is just placed on the top metal layer. This technique has been proposed in the 1980's and enhances the radiation of planar antennas, especially when the antennas are placed on thin or on high dielectric-constant substrates [35]. The quartz superstrate has also been used with on-chip slot-ring antennas at 95 GHz, 170 GHz, 300 GHz and 400 GHz [2], [14], [35].

The simulated microstrip antenna with a 100 μm-thick quartz superstrate shows a peak efficiency of 45% and a gain of 2.8-3.5 dB at 360-400 GHz (Fig. 2.11). The antenna is centered at 380 GHz with a simulated directivity of $\sim$ 7.3 dB and a -10 dB impedance bandwidth of 26 GHz. Note that the gain drops rapidly above 410 GHz due to the trigerring of higher order modes in the dielectric superstrate (TE10) [35]. The quartz superstrate increases the antenna peak gain by 3.1 dB (from 0.4 to 3.5 dB) and the peak efficiency by 3.5 dB (from 22% to 45%) as compared to the

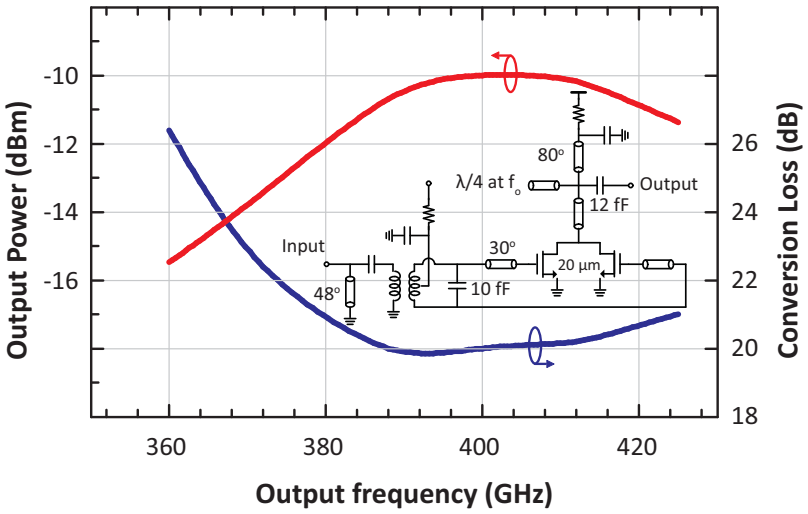


Figure 2.9: Qualdrupler schematic and measured output power and conversion loss [13] at an input power of +10 dBm (f_{in} = 90 - 105 GHz).

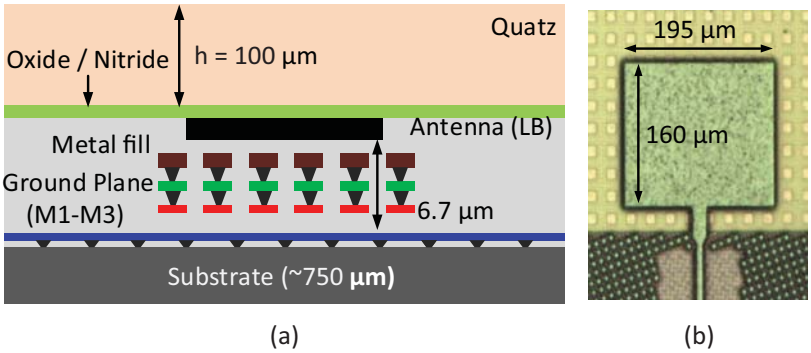


Figure 2.10: High-efficiency microstrip antenna on 45nm SOI with quartz superstrate: (a) cross-section view, (b) microphotograph of antenna showing metal fill.

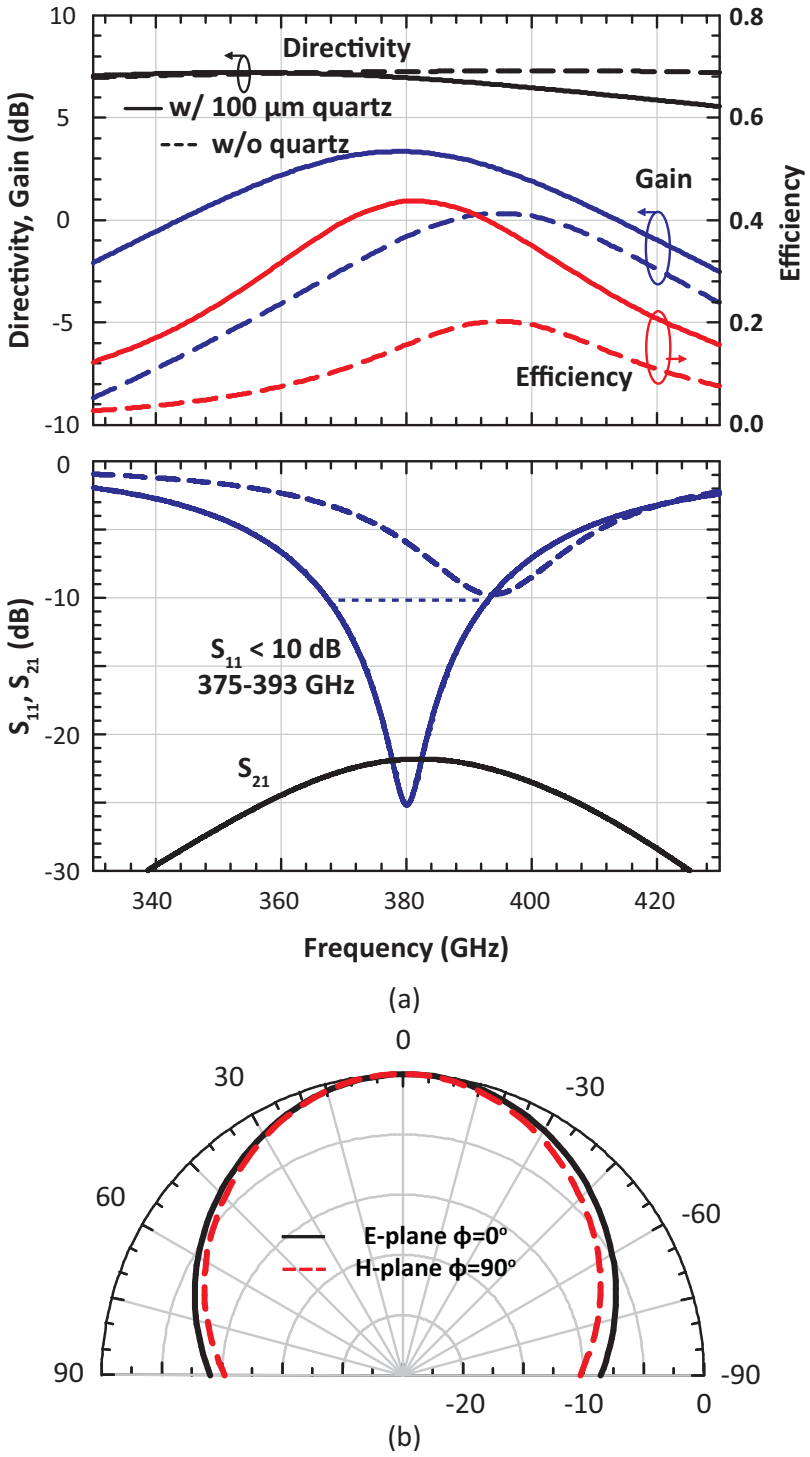


Figure 2.11: (a) Simulated microstrip antenna with and without quartz superstrate, and (b) simulated pattern for single element at 380 GHz.

design without a quartz superstrate. Note that both antennas satisfy the stringent metal-density rules in 45nm SOI and a 30% fill factor of isolated islands on all metal layers underneath the antenna. These isolated islands are not connected to the ground plane or to the silicon substrate and are floating. Still, they do reduce the antenna efficiency from 65% to 45%.

The 8-element linear microstrip array are placed at an element spacing of 0.5λ at 400 GHz (380 μm spacing) for an H-plane pattern scan, and this results in a simulated mutual coupling of $<$ -20 dB. The active antenna impedance is very similar to the single microstrip and is stable versus scan angle due to the H-plane scan. The simulated 3-dB beam-width of the 8-element array is 12° with a gain of 11-12 dB at 380-390 GHz (see Fig. 2.15 for comparison between measured and simulated beamwidth).

2.2.8 System-Level Simulations

The entire transmitter can be simulated using a block-diagram approach since all components are 50 Ω matched (Fig. 2.12). An input power of 6 dBm at W-band results in a power of +3 dBm and -3 dBm at the phase shifter input and output ports, repectively. This is then amplified by 23 dB to result in a P_{sat} of 10 dBm before the quadrupler, which in turn generates a power of -10 dBm at the antenna port. Note that two amplifiers with a linear gain of 23 dB are used after the phase shifter to ensure full output saturation after the vector modulator. This was the correct design approach since a saturated power of 10 dBm is still achievable at 95-100 GHz at the multiplier input even with the additional 8-10 dB loss present in the vector modulator.

The output power from each quadrupler is -10 dBm, which results in a total power of -1 dBm from the 8 elements at the antenna input ports. This, together with an antenna array gain of 11-12 dB, results in an EIRP of 10-11 dBm at 380-390 GHz. The simulated radiated power is -4.5 dBm when an antenna efficiency of 45% is taken into account.

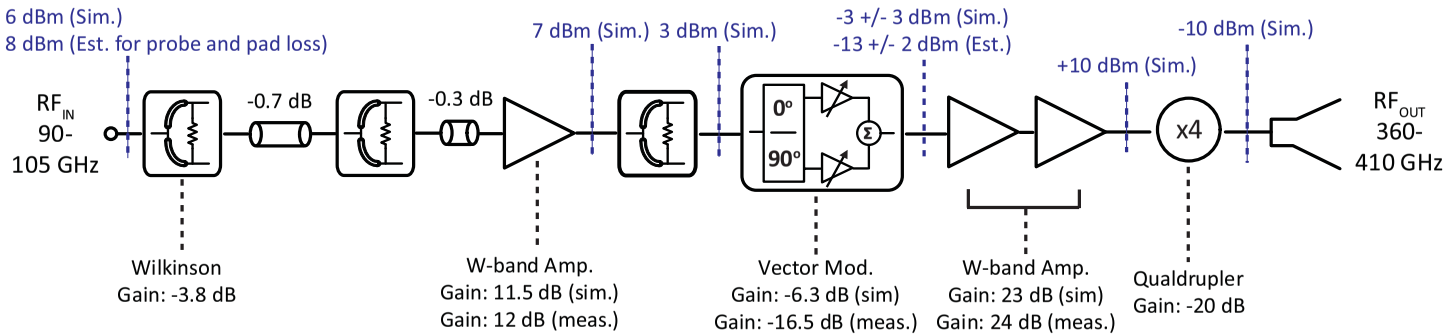


Figure 2.12: System-level simulations including estimated power levels at each block for a single channel.

2.3 Measurements

The 8-element phased array is fabricated on a 45 nm CMOS SOI chip with a size of 3 x 3.5 mm^2 (Fig. 2.13), and is biased at 1.4 V with a current of 1.1 A (1.5 W). The power consumption is divided into: a) W-band amplifiers: 1160 mW, b) W-band vector modulators: 246 mW and c) quadruplers: 123 mW. The CMOS chip is mounted on a Cascade Microtech measurement station and a 100 μm quartz superstrate is glued on top. A W-band GSG probe is used at the RF port and the input power is calibrated to the probe tip. The measured S_{11} is $<$ -10 dB at 90-110 GHz.

The radiated power is measured in the far-field using a WR-2.2 horn and a VDI Schottky diode detector (Fig. 2.14). The far field for the 8-element array is 4 cm at 400 GHz, and a range of 12 cm is used. Amplitude modulation at 30 kHz is applied to the W-band source, and the received voltage from the diode detector is sent to a lock-in amplifier. The measured output voltage is in the mV range, resulting in a dynamic range $>$ 25 dB.

The measured 8-element pattern in the H-plane at 390-400 GHz is shown in Fig. 2.15 when all the phase shifters are set to 0°. The pattern is the same at 390-400 GHz with a 3-dB beamwidth of 12° and agrees well with simulations. The cross-polarization component could not be measured and is $<$ -25 dB relative to the main signal.

The phased-array transmitter scans to +/- 35-40° at 380-400 GHz in the H-plane as shown in Fig. 2.15. The measured relative peak power drop by 5 dB at 40° scan angle can be attributed to 3 dB due to the element factor and 1 dB due to the phased array discretization of 3-bit. At 35-40^o scan angle, the sidelobe patterns are high, and this is not captured by simulations.

The measured EIRP ($P_t G_t$) is obtained using the Friis transmission formula:

$$P_r = P_t G_t G_r (\frac{\lambda}{4\pi R})^2 \tag{2.2}$$

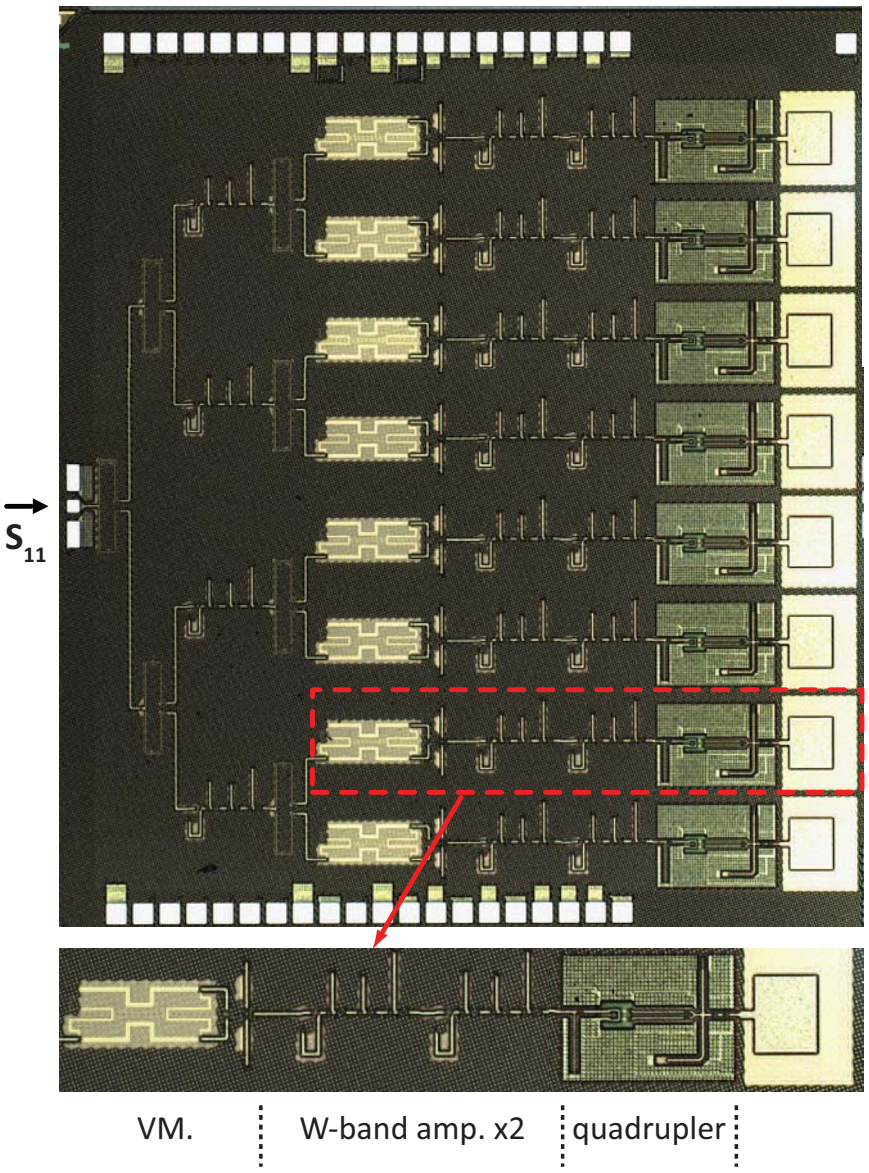
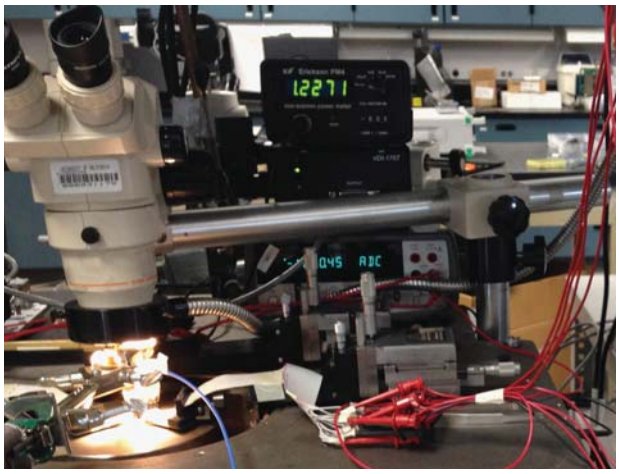


Figure 2.13: Phased-array transmitter microphotograph (3 x 3.5 mm^2) with a blow up of a single channel.



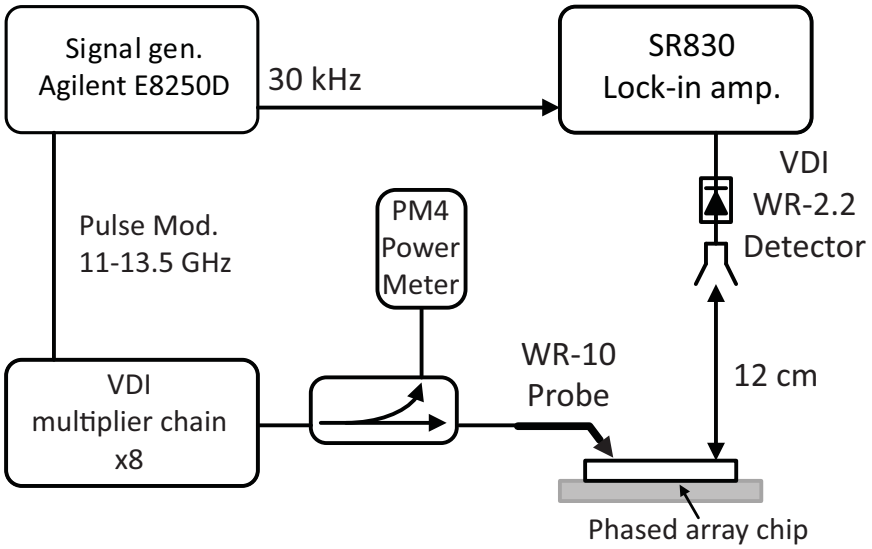


Figure 2.14: Measurement setup and associated block diagram. The phased array is on the Cascade Microtech chuck (under the microscope) and a W-band GSG probe is used for the 90-100 GHz input.

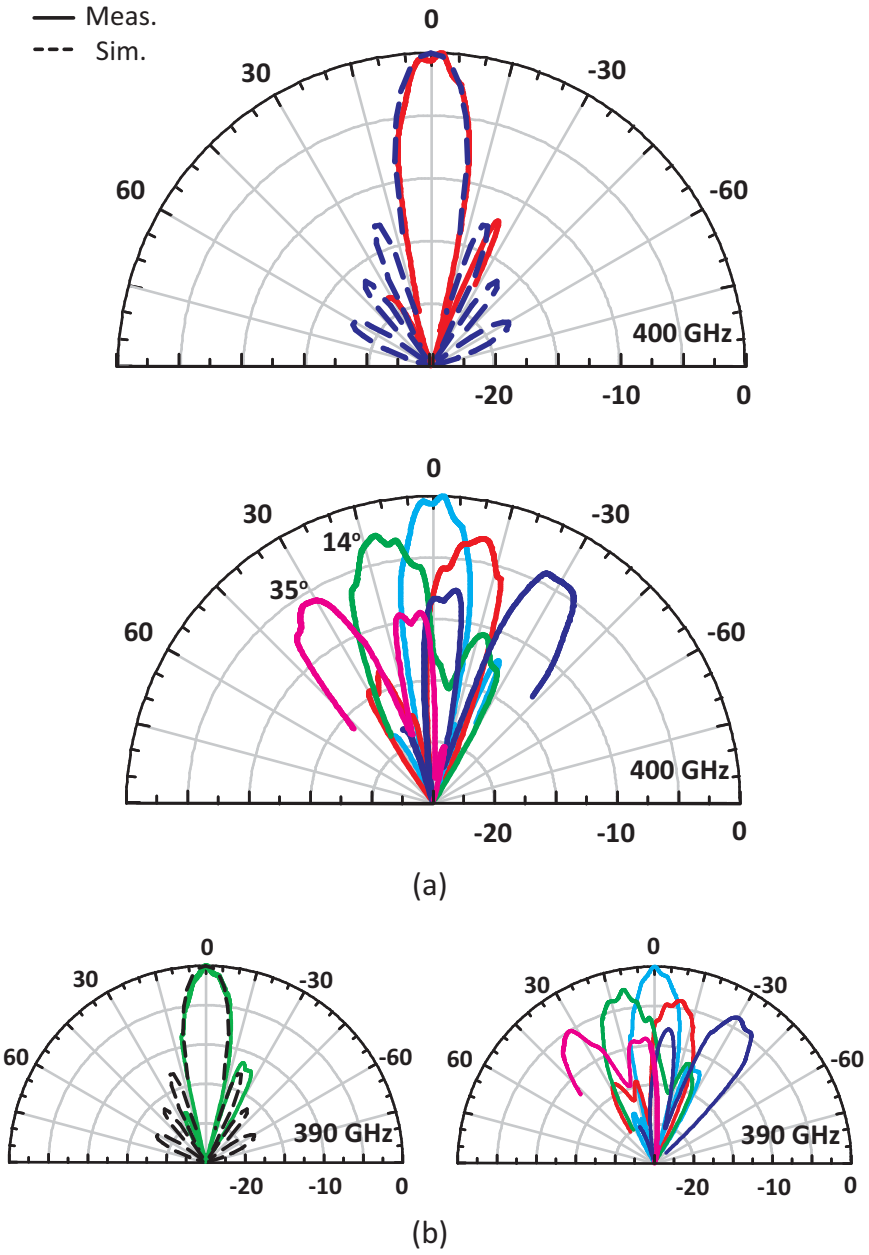
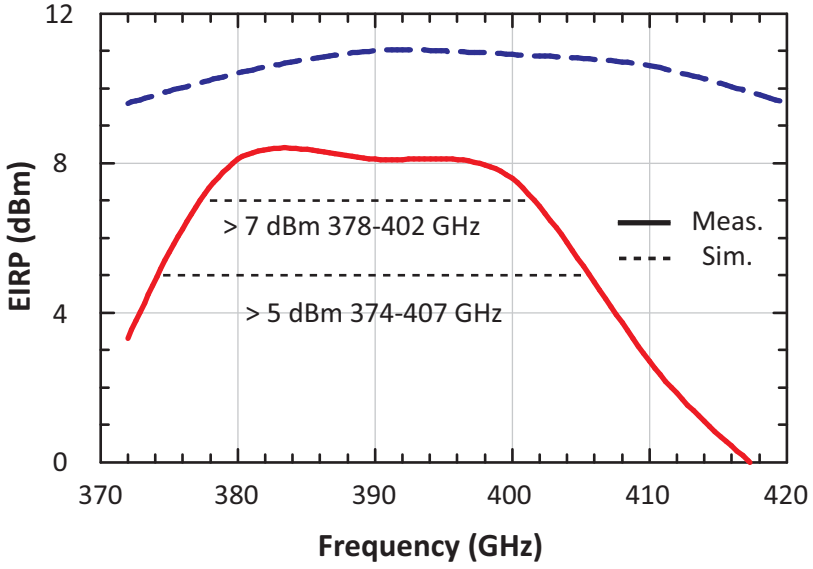


Figure 2.15: Measured and simulated patterns: (a) 390 GHz no scanning and with scanning, (b) 400 GHz no scanning and with scanning.

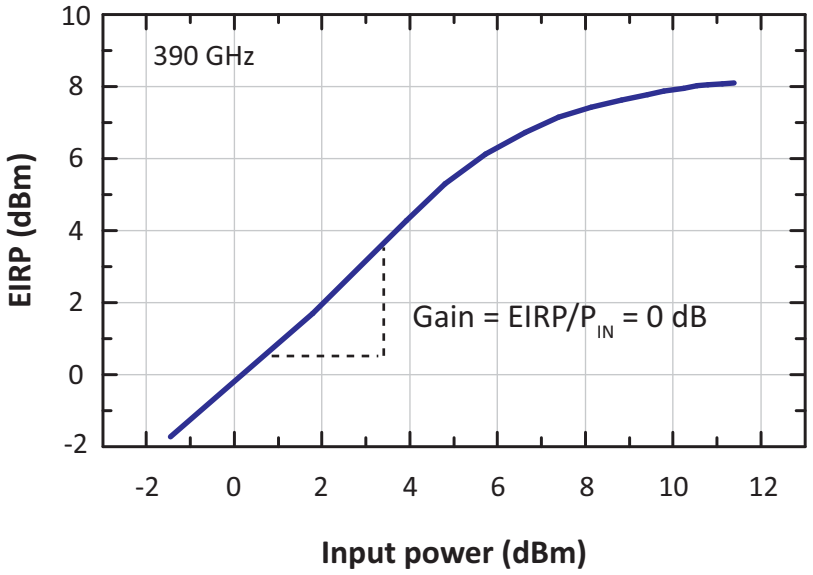
The receive antenna gain is calibrated using the two (identical) antenna method and is 22 +/- 0.5 dB at 390 GHz. The VDI diode detector is calibrated at the factory and also at UCSD, and its responsivity is $\sim$1250 V/W. The difference in responsivity between the VDI and the UCSD calibration is $<$ +/- 0.5 dB at 390 GHz as shown in [14]. The measured EIRP is then inferred from the received power and is plotted in Fig. 2.16(a). A peak EIRP of 8-8.5 dBm is obtained at 380-400 GHz, with a 3-dB bandwidth of 375-407 GHz. This is the highest EIRP obtained to-date at 400 GHz from a silicon-based phased-array, and without the use of a silicon lens. The total radiated power is 200 μW (-7 dBm) at 380-400 GHz. There is a 3-dB difference between the simulated EIRP of 11 dBm and the measured value at 8 dBm. The bandwidth is also narrower than simulations. The difference is possibly due to antenna efficiency reduction if the quartz substrate is not well mounted on the wafer (air gaps) and additional impedance mismatch between the quadrupler and the antenna.

The measured EIRP at 400 GHz versus input power at 100 GHz is shown in Fig. 2.16(b). The small-signal transfer function, defined as EIRP/P_{in} is 0 dB. The output power saturates at 8-10 dBm W-band input power (which is achievable using CMOS amplifiers). Table 2.1 summarises the array performance and presents a comparison with the state-of-the-art above 300 GHz using CMOS and SiGe technologies.

Note that the oscillator arrays summarized in [11,12,14] are narrowband, especially [12] with only 2 GHz of bandwidth. Also, silicon lenses are used in [11] and [12] which results in wider bandwidth and higher gain antennas. The work in this paper shows the widest 3-dB bandwidth (374-400 GHz) and also operation from 370-420 GHz with an EIRP $>$ 0 dBm. Without doubt, THz sources based on multipliers result in much wider band operation than these based on harmonic or push-push oscillators.



(a)



(b)

Figure 2.16: Measured EIRP: (a) versus frequency, and (b) versus input power at 97.5 GHz (fout=390 GHz).

Table 2.1: Summary and Comparison of Phased-Array above 300 GHz

Frequency (GHz)	**Technology**	**Design**	**Antenna/ Transition Type**	**Beam Steering**[1]	**Prad (μW)**	**EIRP (dBm)**	**Pdc (mW)**	**Ref.**
374-407[2]	45-nm SOI CMOS	8 x 1 active quadrupler array	Micro-strip with quartz superstrate	75^o	200	8	1500	This work
320	130 nm SiGe	4 x 1 acrive quadrupler array	SIW cavity backed patch	24^o	$\sim$1000	10.6	$\sim$1000	[11]
276-285	65 nm bulk CMOS	4 x 4 oscillator injection-locked	Diff. ring on a thinned substrate	80^o	190	9.4	817	[15]
337-339[2]	65 nm bulk CMOS	4 x 4 oscillator 4th harmonic coupled	Microstrip	95^o	813	17	1540	[13]
390-440	45-nm SOI CMOS	2 x 4 active quadrupler array	Slot ring with quartz superstrate	Fixed pattern	100	3	700	[14]
520-536[2]	130 nm SiGe	4 x 4 oscillator array triple-push	Wire-ring with silicon lens	Fixed pattern[3]	16 x 62	25	16 x 156	[12]

[1] Defined as entire steering cone.
[2] 3-dB power bandwidth.
[3] 16 incoherent patterns from 16 different transmitters.

2.4 Conclusion

This paper presented a 400 GHz phased-array transmitter with scalability being the prime design factor. This is achieved using W-band circuits for every component except the 100 to 400 GHz quadrupler placed before the antenna. This circumvents the high transmission-line loss at 400 GHz, and most of the phased-array is built at W-band which allows for scalability to large arrays. Also, 50 Ω blocks are used for all components, allowing straightforward connection of the transmitter array. The proposed topology also allows the W-band source to be phased-locked to a low frequency reference using standard frequency dividers, results in a wideband 400 GHz phased array, and can be used with any type of multipliers such as triplers, quadruplers and quintuplers.

2.5 Acknowledgment

The authors would like to thank Ozan Dogan Gurbuz and Michael Chang for technical discussions.

Chapter 2 is mostly a reprint of the materials from

• Y. Yang and O. D. Gurbuz and G. M. Rebeiz, ”An eight-element 370-410GHz phased-array transmitter in 45-nm CMOS SOI with peak EIRP of 8-8.5 dBm,” in *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4241-4249, Dec. 2016.

The dissertation author is the primary author of this material.

Chapter 3

Gbps Millimeter-Wave Transceivers

3.1 Introduction

THz systems at $>$ 100 GHz have been successfully demonstrated for active imaging systems, general-purpose transmitters, and Gbit/s communication systems using CMOS and SiGe. Application areas such as chip-to-chip or 1-100 m communications require high-order modulation such as QPSK for better spectral density [36–39], and while this was achieved using GaAs-based systems [40, 41], there has not been a QPSK transceiver demonstration using CMOS. This paper presents a 155 GHz transceiver with an I/Q modulator and demodulator capable of achieving $>$ 20 Gbit/s QPSK data-rates.

3.2 Design

3.2.1 Transceiver Topology

Fig. 3.1 presents the transceiver chip block diagram. A 74-77 GHz local oscillator is employed with an SPDT switch (2.2 dB loss) which allows an external LO feed. The LO signal passes by an active splitter and two balanced doublers with single-ended outputs. Two 150 GHz

$0/90^{o}$ quadrature hybrids are placed in the Tx and Rx paths (3 dB division loss + 0.8 dB ohmic loss) and 150 GHz passive baluns (1.5 dB loss) are used to drive the differential I/Q modulator and mixers. The system does not employ amplifiers at 150 GHz due to their power consumption and since the doublers can each generate 3 dBm which is enough to drive the 150 GHz circuitry. The I/Q mixers are directly attached to the input RF port using a Wilkinson splitter (3 dB division loss + 0.7 dB ohmic loss). The process is Global Foundries 45nm SOI CMOS, with ft/fmax of 250/240 GHz referenced to the top metal layer [42].

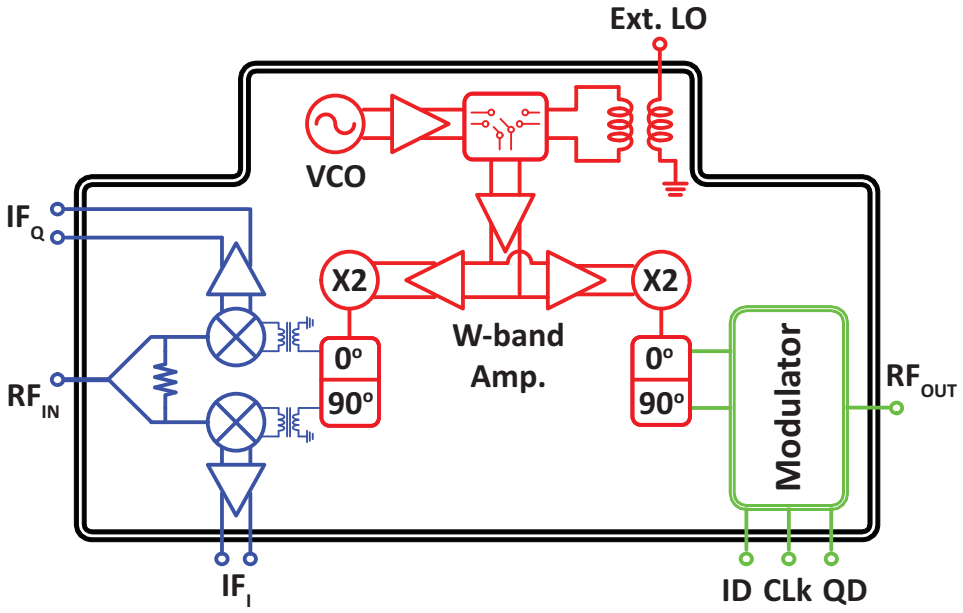


Figure 3.1: QPSK transceiver block diagram with option for an external LO feed.

3.2.2 Oscillator, Active Splitter and Doubler

The Clapp oscillator (Fig. 3.2) is believed to have lower phase noise compared to other architectures, at the expense of limited tuning range. Two capacitors combined with a varactor are used to achieve a frequency tuning range of $\sim$2 GHz. In order to save power consumption, the oscillator is working under 0.7 V supply domain. Common source amplifier based buffers which draw current from 1.0 V supply are used to deliver required power to saturate the followed by active power splitter.

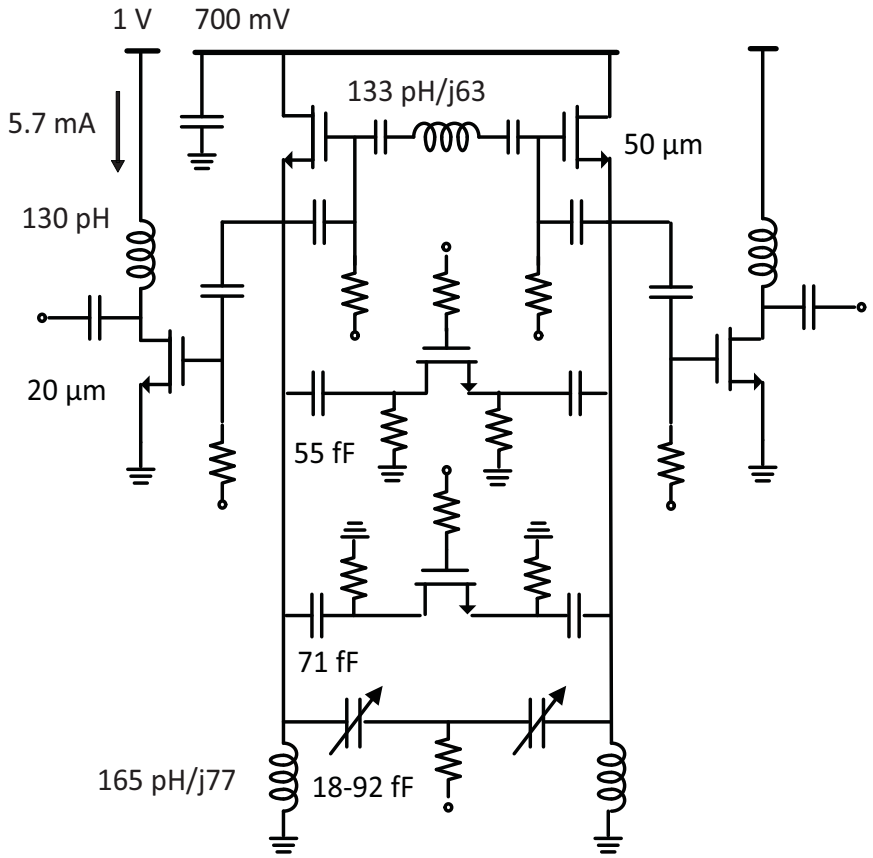


Figure 3.2: VCO schematic

The differential cascode-based active power splitter (Fig. 3.3) drives the classical balanced doubler on both transmitter side and receiver side with a output saturated power of 7.7 dBm.

Quarter wavelength short stubs are used at both double input and output to eliminate harmonics. (Fig. 3.4).

3.2.3 I/Q Mixer and IF Amplifier

The I/Q balanced mixers (Fig. 3.5) have a simulated gain of 0 dB at 150 GHz at an LO power of -3 dBm (2 V, 13.5 mA) [43]. IF amplifier (Fig. 3.6) is built of four cascaded fixed gain stages with a feedback loop for DC offset cancellation. Output buffer is designed to drive 100 Ω differential load. The simulated 3-dB receiver bandwidth (mixer + IF amplifier) is ∼140-152 GHz with an LO of 145 GHz, thus allowing for 20 Gbit/s data modulation. The simulated I/Q receiver gain and NF including the Wilkinson splitter loss for f_{RF} = 150 GHz is 23 dB and 20 dB, respectively.

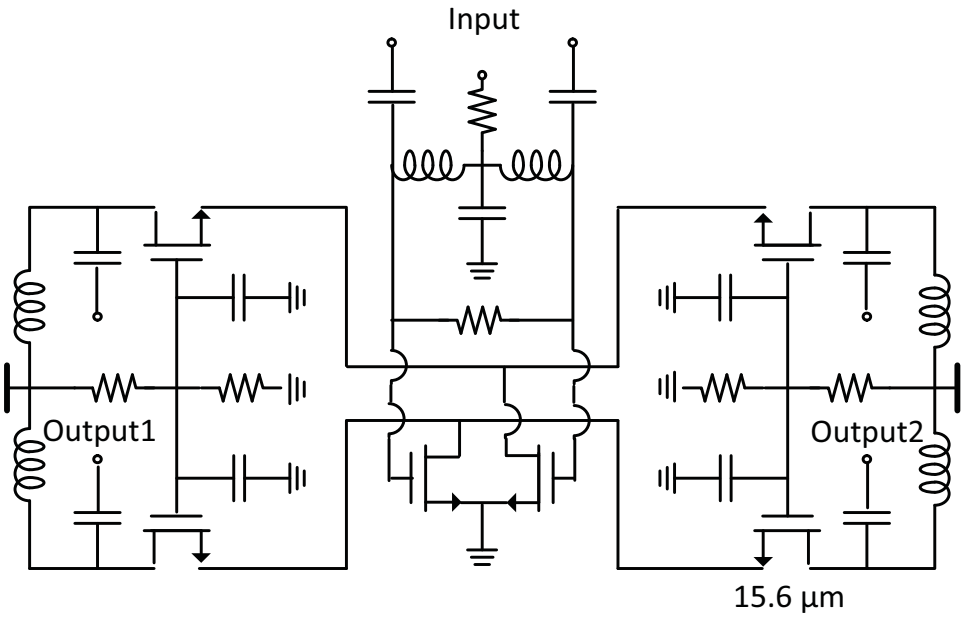


Figure 3.3: Active splitter schematic.

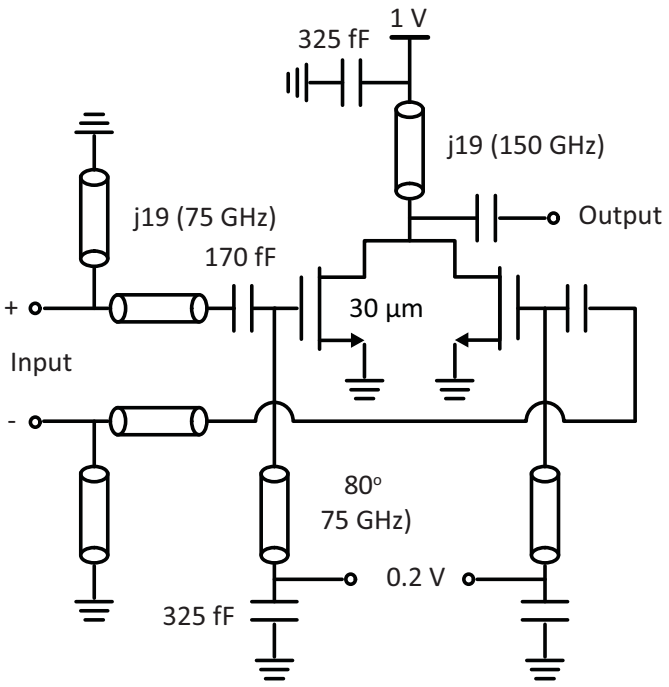


Figure 3.4: Doubler schematic.

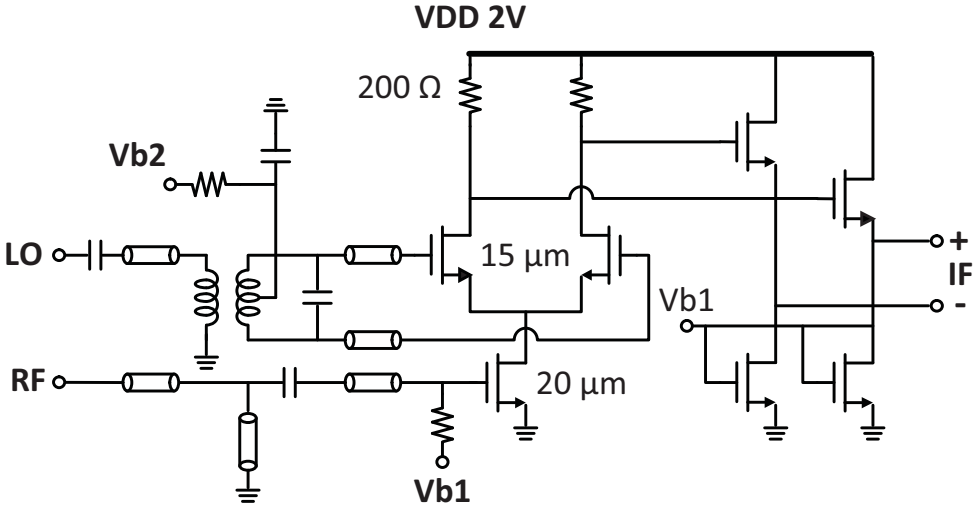


Figure 3.5: Balanced mixer schematic schematic.

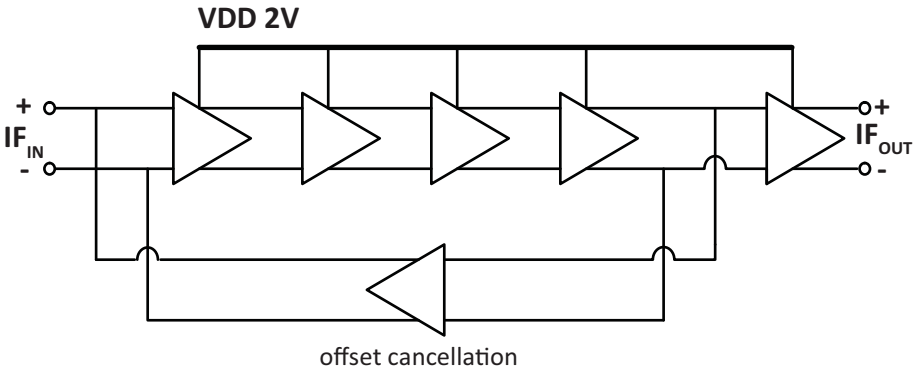


Figure 3.6: wideband IF amplifier schematic.

3.2.4 I/Q Modulator Design

The I/Q modulator uses an LO switching transistor quad on the top level and I/Q data transistors on the bottom level (Fig. 3.7). A balun is used at the output port and provides a wideband conjugate impedance match between the modulator and the output 50 Ω port. The I/Q input data is retimed with the clock (CK) signal and turned differential using D-flip-flops with a rise/fall times of 14 ps, thus allowing $>$ 20 Gbit/s per channel. The modulator interconnect parasitics are modeled from the top metal to C1 using Sonnet EM Suite and RC-extraction is done from M1 to C1.

3.2.5 Packaging

Fig. 3.8 presents the chip micrograph with a size of 2.8x1.4 mm^2. The chip consumes 345 mW with the on-chip LO (290 mW without the on-chip LO). The transceiver chip was placed on a Rogers-4003 board with ε_r = 3.5. The RF ports are probed using WR-6 GSG probes, and the off-chip LO is injected using a WR-10 GSG probe. (Fig. 3.9, Fig. 3.10)

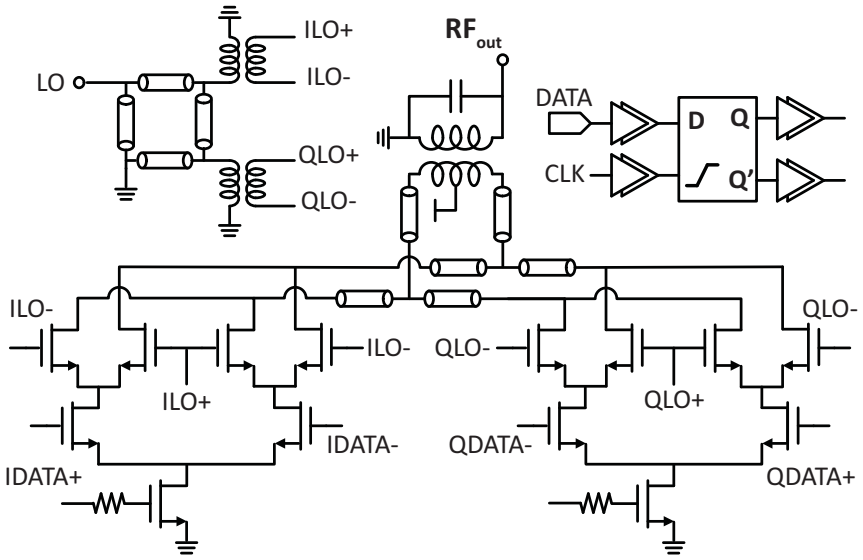


Figure 3.7: I/Q modulator schematic.

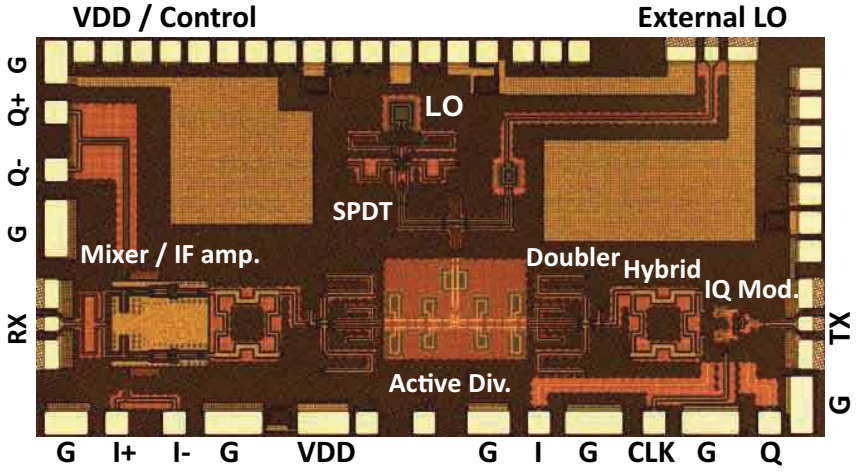


Figure 3.8: Die micrograph.

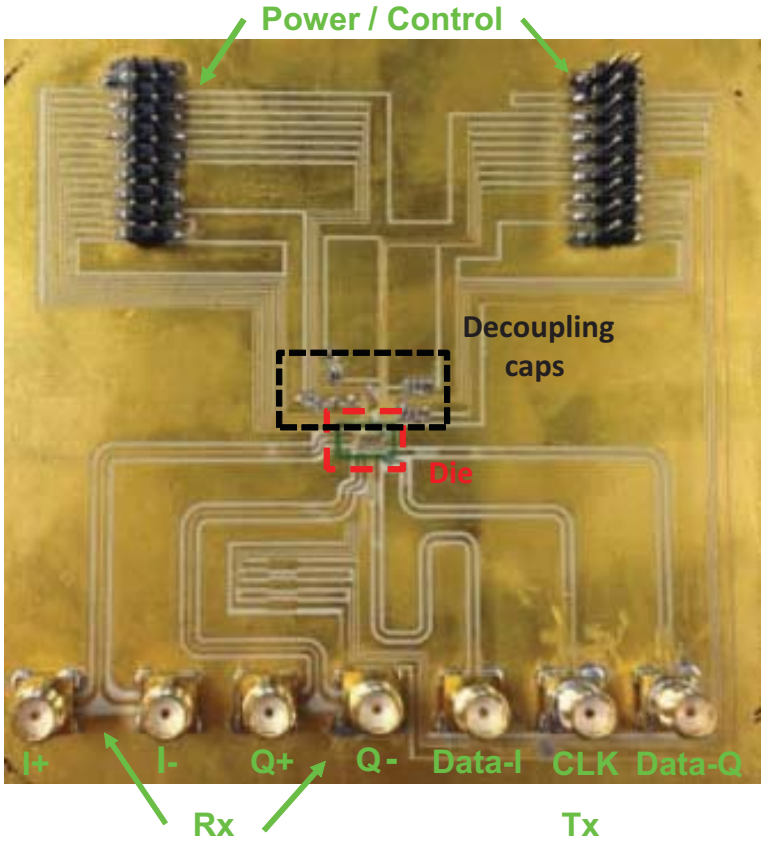


Figure 3.9: PCB board.

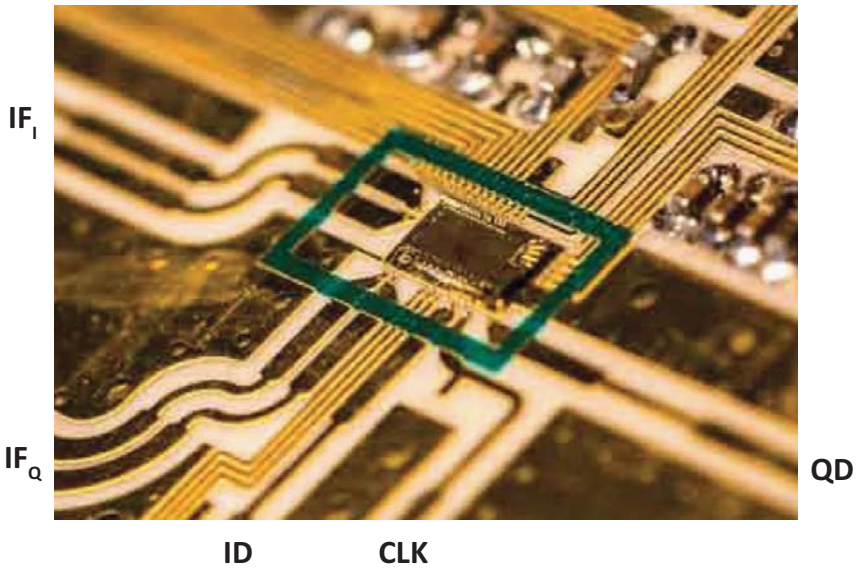


Figure 3.10: Die & bonding on PCB board.

3.3 Measurements

3.3.1 Oscillator, Active Splitter and Receiver

The Clapp oscillator operated at 78.5-80.5 GHz from a 1/0.7 V supply (56 mW) with an output power of 0-3 dBm and a measured phase noise of $<$ -92 dBc/Hz at 1 MHz. The oscillator shifted in frequency from a design of 74-76 GHz, but kept similar output power and phase noise values as simulated (Fig. 3.11, Fig. 3.12, Fig. 3.13)

The active splitter breakout has a measured gain of 6.8 dB at 75 GHz and an output P_{sat} of 8 dBm per channel (including GSG pads) from a 2 V supply (85 mW). The balanced doubler breakout results in a measured conversion loss of 3 dB and a peak output power of +3.5 dBm at 150 GHz, and with $>$ 1.3 dBm from 140-160 GHz (includes GSG pads) from a 1 V supply. (Fig. 3.14)

The measured conversion gain of the receiver is $\sim$23 dB with a 3-dB bandwidth of 146-155 GHz for an LO of 150 GHz (Fig. 3.15). The I/Q channels were amplitude matched to +/-0.9 dB over the 3-dB bandwidth (Fig. 3.16). In general, the S-parameter measurement results agree well with simulations. Fig. 3.17 illustrates the setup for receiver eye diagram measurement. Carrier frequency is generated by the VDI AMC 333 multiplier chain, then it is mixed with the data from Keysight JBERT N4903 using VDI WR-6.5 sub-harmonic mixer for BPSK pattern. Spectrum and eye -diagram measured with 5 and 10 Gbit/s BPSK modulation at 150 GHz carrier frequency are showed on Fig. 3.18 as an evidence that the receiver can handle such data transition speed. Due to the VDI sub-harmonic mixer limitation, only BPSK modulation can be implemented. QPSK modulation will be tested with the transceiver loop back setup and measurement results will be presented in 'Transceiver Measurements' subsection.

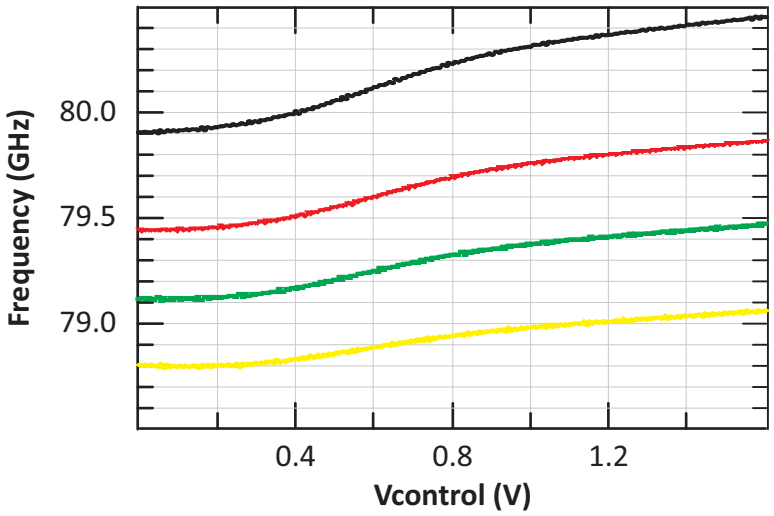


Figure 3.11: Measured VCO tuning range.

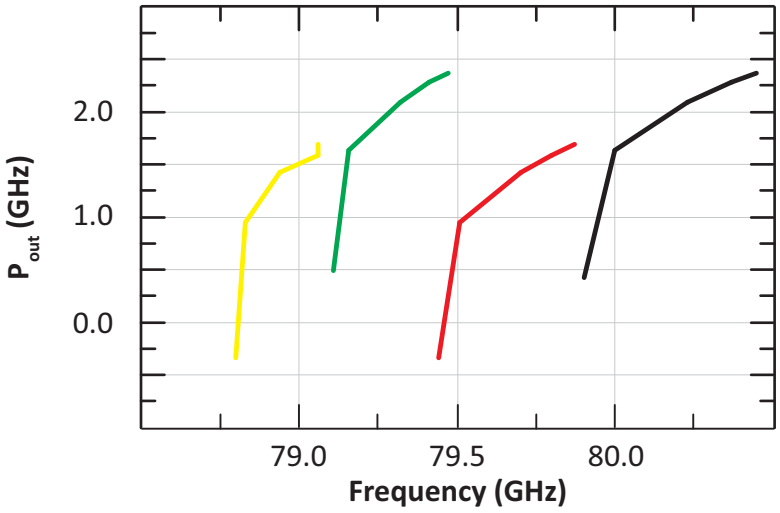


Figure 3.12: Measured VCO output power.

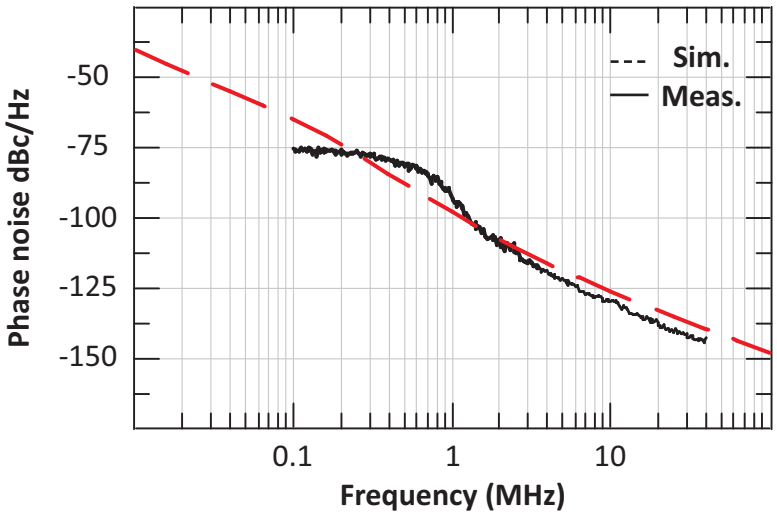


Figure 3.13: Measured VCO phase noise.

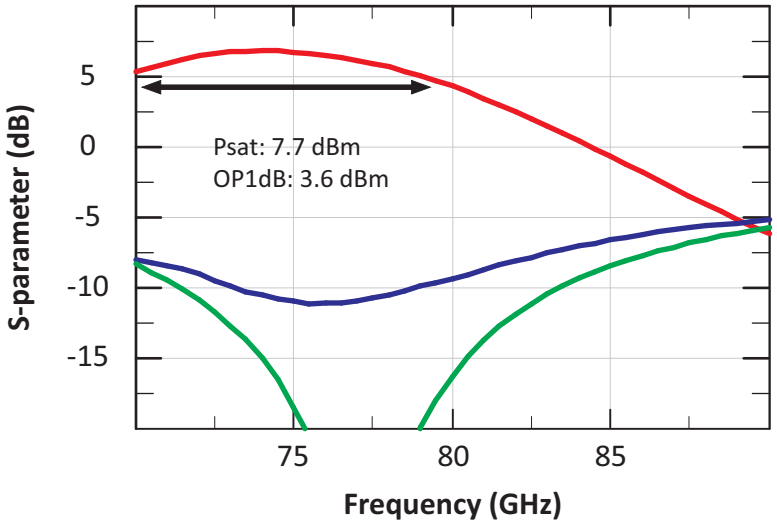


Figure 3.14: Active power splitter power measurement results.

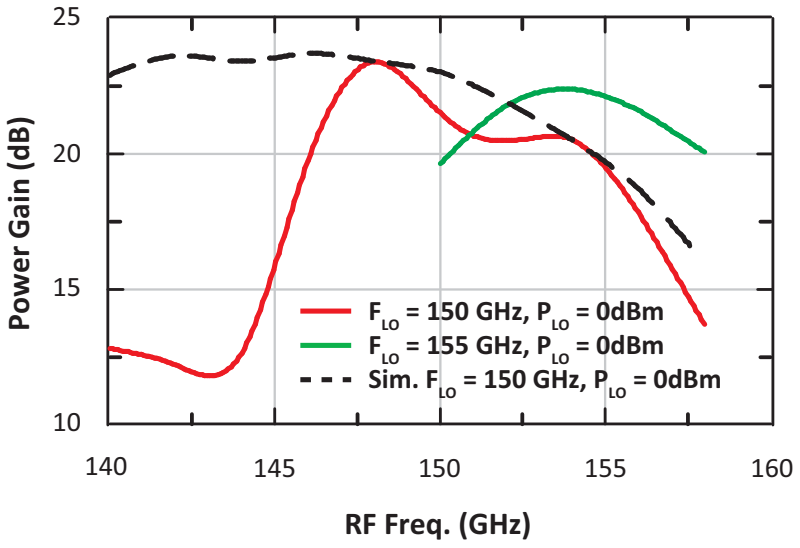


Figure 3.15: Receiver power gain.

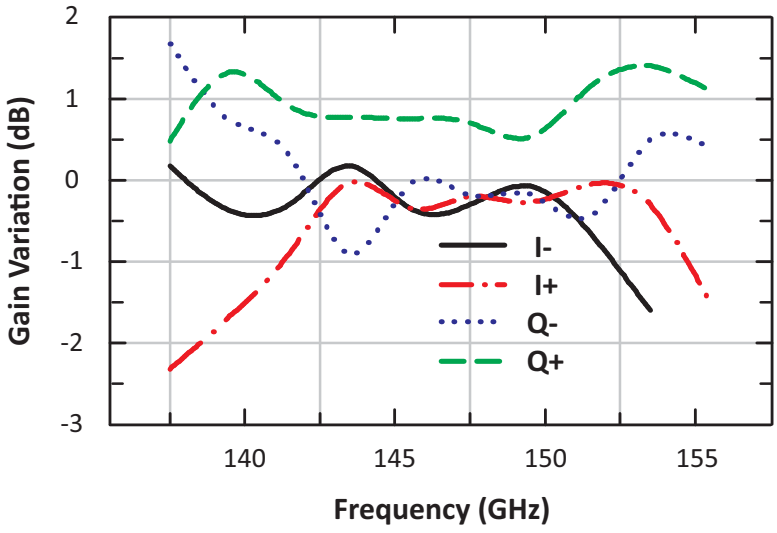


Figure 3.16: Receiver gain variation.

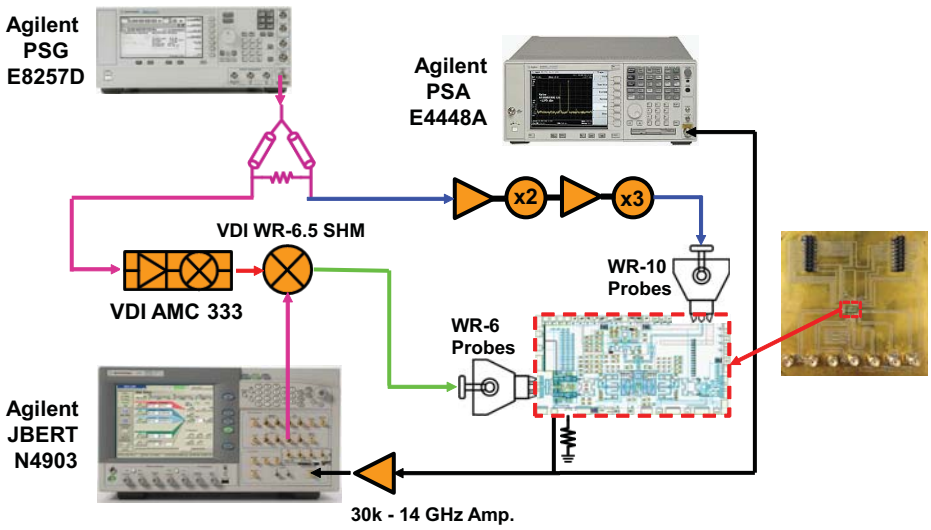
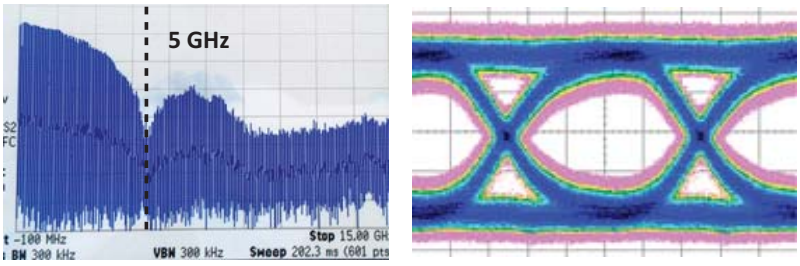
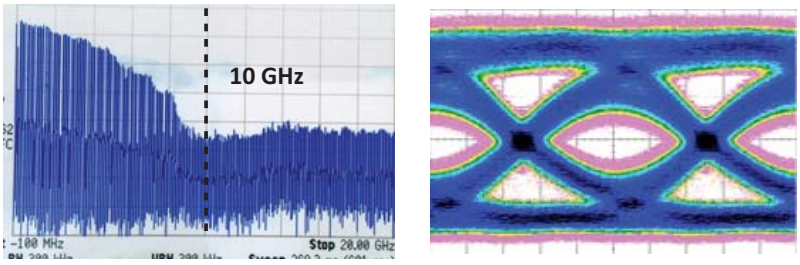


Figure 3.17: Receiver eye diagram measurement setup.



f_{LO}: 150 GHz, 5 Gb/s



f_{LO}: 150 GHz, 10 Gb/s BPSK

Figure 3.18: Receiver spectrum and eye diagram measurement results.

3.3.2 Modulator Measurements

Measurements on a modulator breakout with LO and RF input/output baluns and a 0/90^o hybrid show a peak gain of -4 dB at 140-145 GHz with a 3-dB bandwidth of 130-160 GHz, and a saturated output power of +1 dBm (Fig. 3.19, Fig. 3.20). The modulator results in $<$ +/-0.7 dB and +/-6^o error with I/Q inputs of 00, 01, 10, 11 at 135-170 GHz (Fig. 3.21, Fig. 3.22). The modulator was also tested at an LO of 150-155 GHz, an output power of -10 dBm at the GSG pads, and with 0.1-12.6 Gbps I/Q data streams (Fig. 3.23). In this case, the output spectrum was down-converted to a center frequency of 10 GHz using a wideband subharmonic mixer followed by a 0.5-18 GHz amplifier with 26 dB gain (total receiver NF = 24 dB), and the QPSK signal fed into a Tektronics DPO scope. Fig. 3.24, Fig. 3.25, and Fig. 3.26 are screenshots of software evaluated spectrums, eye diagrams and EVM from the scope. A QPSK constellation is seen at 20 Gbit/s without any equalization and with an rms EVM of 16.9%. The measured LO leakage is -18 to -20 dBc at 150-155 GHz. The S/N ratio at the GSG pads is 40 dB in a 10 GHz bandwidth, resulting in an expected EVM of 1% (the modulator I/Q errors above add another $\sim$1%). The increased EVM is due to impairments from the subharmonic mixer unequal upper side band/lower side band response, wideband external IF amplifier (+/-2dB ripple) and cable dispersion at DC-20 GHz. Measurements done at 2-20 Gbit/s show QPSK modulation EVM values of 6.6-16.9%.

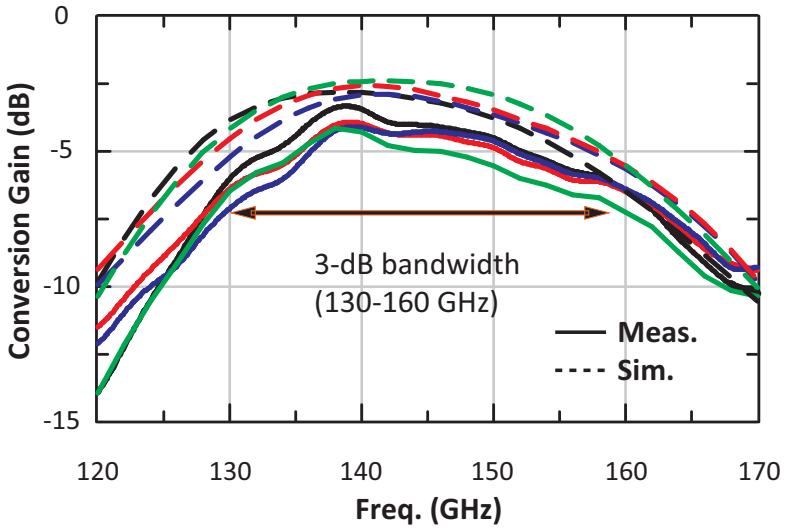


Figure 3.19: S_{21} measurement results for (00), (01), (10), and (11) I/Q inputs.

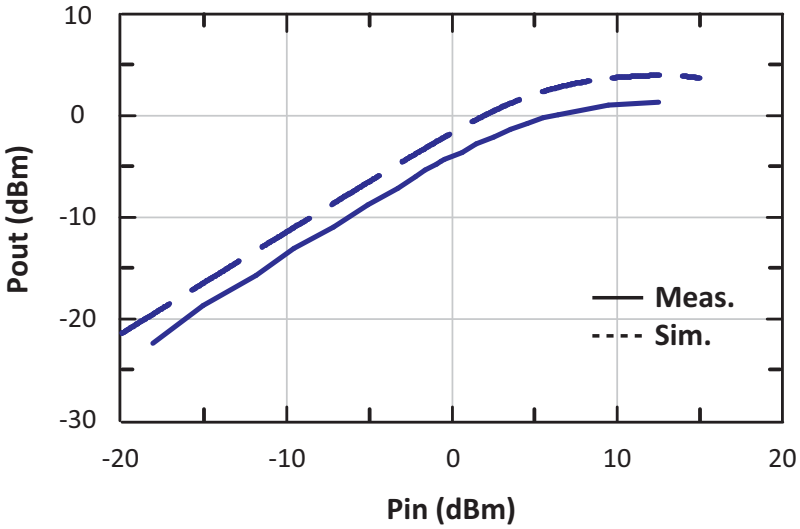


Figure 3.20: Modulator P_{in} (LO power) versus P_{out} measurement results.

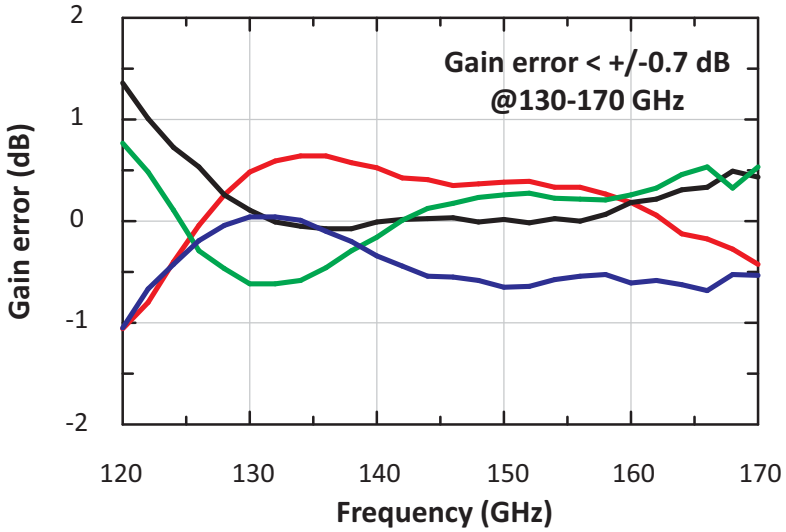


Figure 3.21: Modulator gain error for (00), (01), (10), and (11) I/Q inputs.

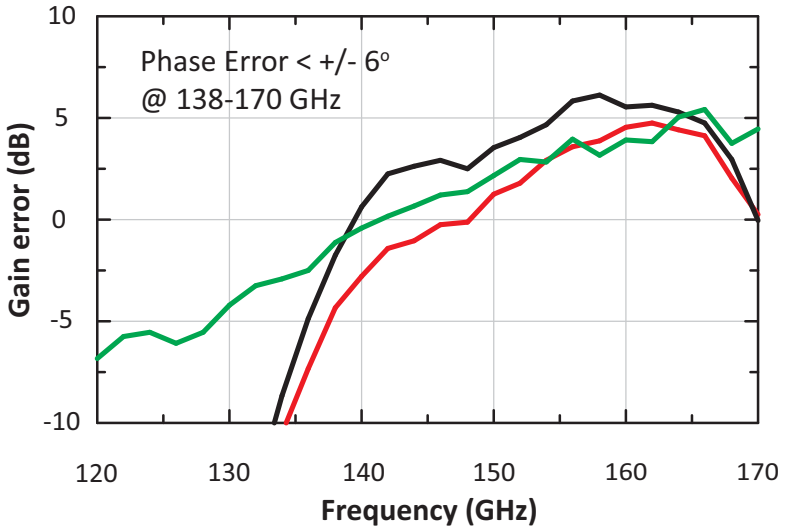


Figure 3.22: Modulator phase error for (00), (01), (10), and (11) I/Q inputs.

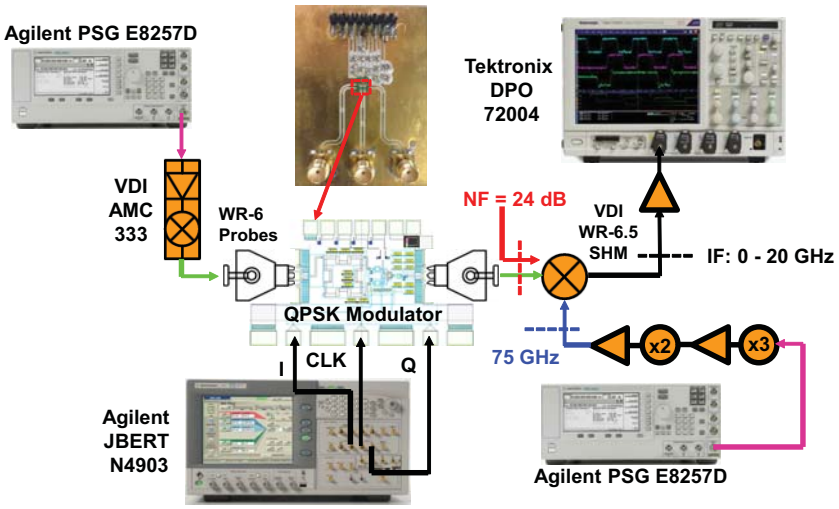


Figure 3.23: Modulator performance measurements setup.

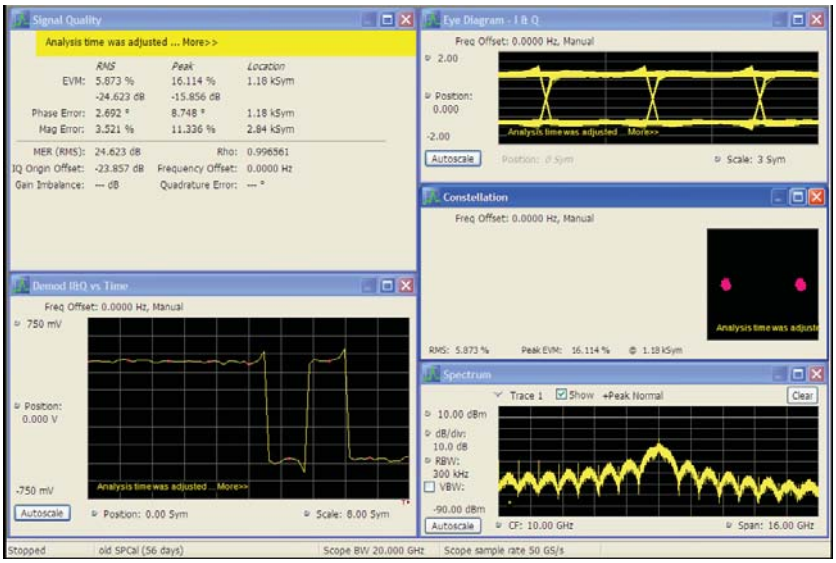


Figure 3.24: Measured modulator spectrum, eye diagram, and EVM at 150 GHz carrier frequency with 1 Gbit/s BPSK modulation

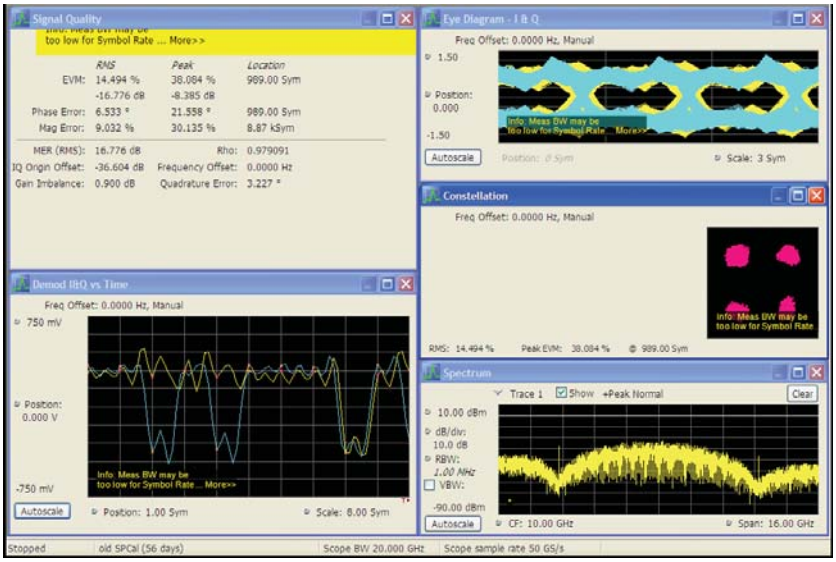


Figure 3.25: Measured modulator spectrum, eye diagram, and EVM at 150 GHz carrier frequency with 10 Gbit/s QPSK modulation

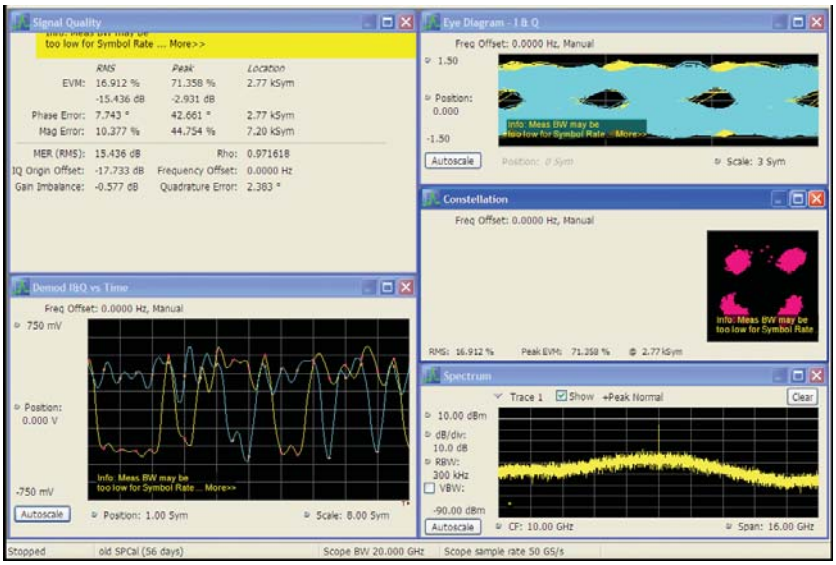


Figure 3.26: Measured modulator spectrum, eye diagram, and EVM at 150 GHz carrier frequency with 20 Gbit/s QPSK modulation

3.3.3 Transceiver Measurements

The transceiver was measured in a loop-back configuration at f_{LO} = 150-155 GHz with the Tx port connected to the Rx port using a WR-6 waveguide setup containing an attenuator and phase shifter (adjusted to result in equal signal values at the I and Q outputs). An external oscillator is used since the internal oscillator tuned a bit high. The loop-back loss is set at 20 dB, which results in an input power of -27 dBm for a measured QPSK modulator output power of -7 dBm at 150-155 GHz. The expected input S/N ratio is: -27 dBm / (-174 dBm/Hz + 20dB + 100 dB) = 27 dB in a 10 GHz channel. A 2-channel 12.6 Gbps J-BERT is used for I/Q data generation, and the Q channel is delayed by 14 ns from the I channel so as to randomize the I/Q data. The downconverted QPSK I/Q signals pass by DC-14 GHz amplifiers, and are fed to the BERT. A BER $< 10^{-12}$ is obtained for the I and Q channels up to 9.5 Gbit/s (19 Gbit/s total) and $< 10^{-6}$ up to 10 Gbit/s (20 Gbit/s total) (Fig. 3.28). A real time waveform at 14 Gbit/s QPSK modulation with eye diagram is illustrated in Fig. 3.30 to prove no missing of bits. Knowing that the chip consumes 290 mW (without the 74-76 GHz internal oscillator), this is 14.5 pJ/bit for a 20 dB loss channel. A BER vs. power for a 5 GS/s QPSK modulation (10 Gbit/s) shows 10^{-12}, 10^{-12}, 10^{-10}, and 10^{-6} for an input signal of -20 dBm, -27 dBm, -31 dBm, and -37 dBm, respectively (Fig. 3.29).

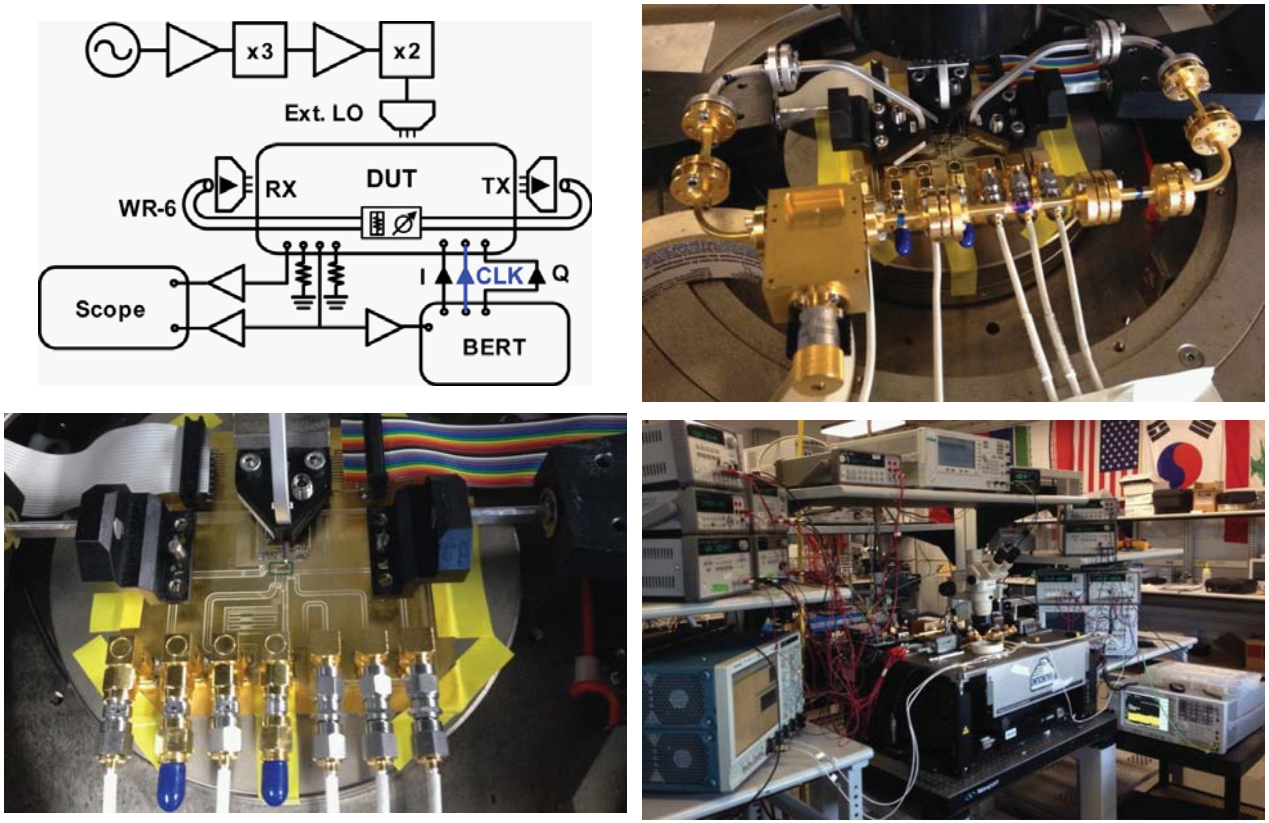


Figure 3.27: Loop-back transceiver measurement setup.

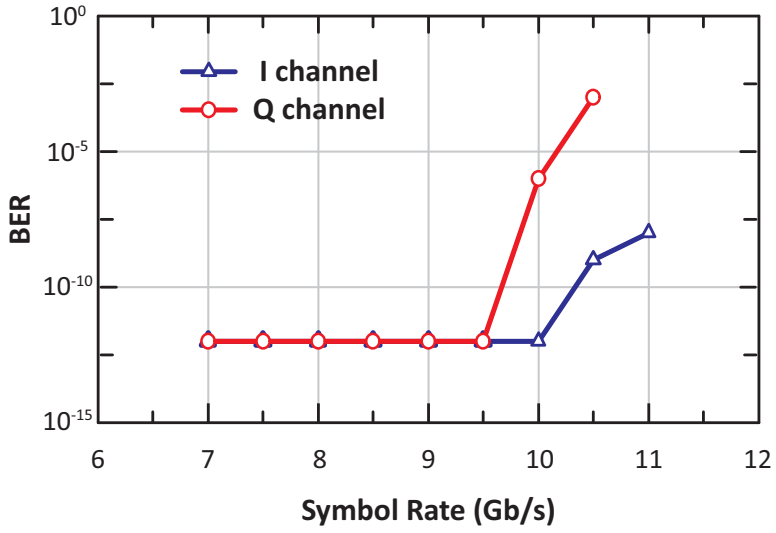


Figure 3.28: Measured Transceiver Bit-Error-Rate versus data rate with QPSK modulation at -20 dBm received power

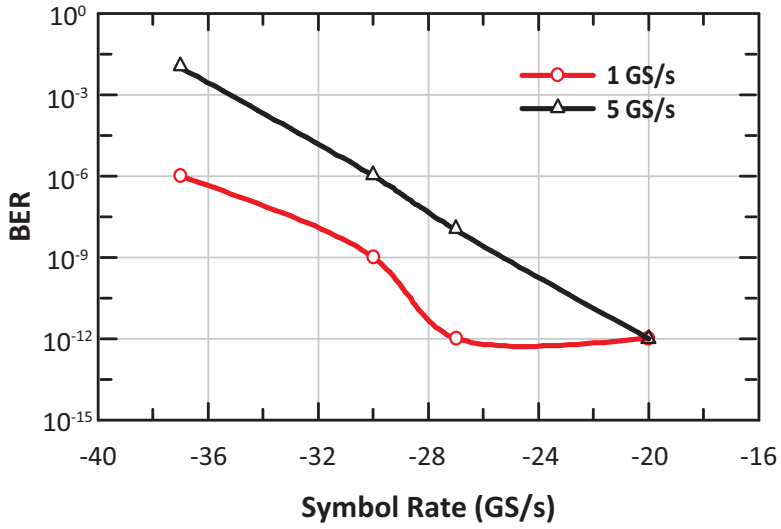


Figure 3.29: Measured Transceiver Bit-Error-Rate versus data rate with QPSK modulation at -20 dBm received power

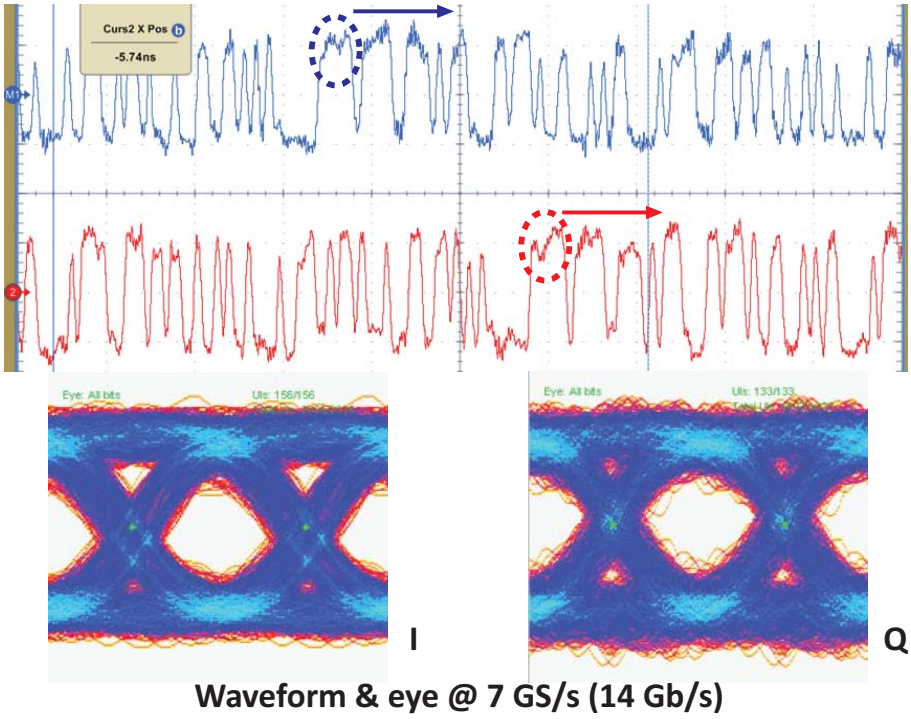


Figure 3.30: Measured waveform at 14 Gbit/s QPSK modulation with eye diagram for both I/Q channels.

Table 3.1: Performance Summary Table

VCO & Buf.		I/Q Modulator		Power Divider	
Output Power	0 – 3 dBm	S_{21}	-4 dB	S_{21}	6.8 dB
Tuning Range	79.7 – 80.5 GHz	3-dB BW.	30 GHz	P_{SAT}	8 dBm
Phase Noise	92 dBc / Hz	Output Power	1 dBm	OP1dB	3.7 dBm
Power Cons.	56 mW	Power Cons.	38 mW	Power Cons.	85 mW
Doubler		**I/Q Mixer w/ IF Amp.**		**TRX**	
P_{SAT}	3.5 dBm	Gain	23 dB	Data Rate	19/20 Gbit/s
Return Loss	< -10 dB	Return Loss	< -9 dB	BER	10^{-12} / 10^{-6}
3-dB BW.	> 20 GHz	3-dB BW.	10 GHz	RX SSB NF	20 dB*
Power Cons.	40 mW	Power Cons.	67 mW	Power Cons.	345 mW

***Simulation**

3.4 Conclusion

A state-of-the-art 155 GHz transceiver with QPSK modulation was presented. The modulator test cell had a EVM of 6.6-16.9% for 2-20 Gbit/s $2^{31}-1$ QPSK signal. The transceiver was measured on a Rogers-4003 board with probing for RF ports. Clear eye diagrams and spectrums were observed and BER was evaluated versus symbol rates and received power. Table 3.1 summarize the performance of the transceiver and that of its building blocks. A comparison with state-of-the-art is presented in Table 3.2.

Table 3.2: Comparison Table with Transceivers above 100 GHz

	This Work	[1]	[2]	[3]	[4]	[5]	[6]
Technology	45 nm SOI CMOS	0.18 µm SiGe BiCMOS	65 nm CMOS	65 nm CMOS	45 nm SOI CMOS	0.1 µm InP HEMTs	0.1 µm InP HEMTs
Frequency	155 GHz	70-110 GHz	120 GHz	135 GHz	110 GHz	120 GHz	140 GHz
Function	TX/RX	TX/RX	TX	TX/RX	TX	TX/RX	TX/RX
Modulation	BPSK/ QPSK	16 QAM	BPSK/ QPSK/ 8QAM	ASK	BPSK/ OOK	QPSK	16 QAM
Data Rate	20 Gb/s	10 Gb/s	10 Gb/s	10 Gb/s	2x44 Gb/s	10 Gb/s	10 Gb/s
Power Cons.	345 mW	500 mW	200 mW	98 mW	825 mW	1.5	-
Area	3.9 mm^2	3.4 mm^2	1.55 mm^2	2 mm^2	0.74 mm^2	4 mm^2 (x2)	-

3.5 Acknowledgment

This work is supported by Intel Corp. and UC Discovery Program.

Chapter 3 is mainly a reprint of the materials from

• Y. Yang, S. Zihir, H. Lin, O. Inac, W. Shin, G. M. Rebeiz, "A 155 GHz 20 Gbit/s QPSK transceiver in 45nm CMOS," in *Radio Frequency Integrated Circuits Symposium (RFIC)*, June

2014.

The dissertation author is the primary author of this material.

Chapter 4

Switch Networks

4.1 Introduction

Communication networks are continuing their growth trends, with current and projected rates in excess of 30% annualized increase in bandwidth. Such growth rates imply network bandwidth doubling every $\sim$2.5 years. At the same time, network hardware cost, space and power consumption allocations are staying roughly flat. Equipment manufacturers must therefore deliver substantial continuous reductions in per-bit metrics: cost, space, and power.

Many aspects that are important in high bit-rate circuit design are brought together in the design of a cross-connect switch IC for data routing. The switch matrix, which forms the core of the cross-connect switch IC, is an excellent example showing that optimum performance can only be obtained when circuits and interconnect are optimized together. It also requires Other high bit-rate circuits, such as input and output buffers and functions for built-in self-testing (e.g., a VCO and a PRBS generator) to support the matrix operation. Active III-V and SiGe technologies or p-i-n diodes are popular due to the accessible low-loss metal [44–48]. RF microelectromechanical systems(MEMS) switches is an alternative option due to longer life, smaller size and excellent isolation which are demonstrated in [49–52]. With the technology progresses in CMOS, high-

performance transistors can be used in low-loss/high-isolation switching matrices [53–56]. As for the structure, CML(Current Mode Logic) based multiplexer active switching consumes significant DC power [44,45,54]. While purely passive switch based matrices have limited scalability [53,55]. Designing switch matrices using both passive and active circuits is an alternative solution.

This section will present a 0.24 pJ/bit, 30 Gbit/s 8x8 single-ended cross connection switch matrix with input and output buffers and a 16x16 matrix built by 4 of the 8x8 matrix. Both matrix are capable of passing digital signals and the isolation between channels is greater than 40 dB.

4.2 Design

The block diagram of the 8x8 switch matrix is showed in Fig. 4.1 . A switch at each row and column cross point allows any input (In(i)) can be connected to any output (Out(i)) with conflicts prohibited by control logic. (e.g., multiple inputs connected to the same output are not possible). Input and output buffers compensate the path loss and reduce the rise and fall times. Suppose the routing line has a characteristic impedance (Z_o) of 50 Ω (the acuter loaded routing line mode shows only 24 Ω characteristic impedance which will be talked in next paragraph)and each row and column line are terminated with 50 Ω resistance, the input buffer is loaded by 25 Ω and in order to drive such low impedance at wanted speed, large current needs to be drawn from the supply. To save power, open termination is applied in this design since the row/column length is relative short ($<$ 1/50 wave length at 30 GHz). The delay between different inputs to outputs paths may vary in which In(1) to Out(1) will have the least delay and In(N) to Out(M) will results in the maximum one. The delay difference between the shortest and the longest paths defines the timing skew. And the timing skew can become a problem if there is no data recovery mechanism which need to be considered on system level.

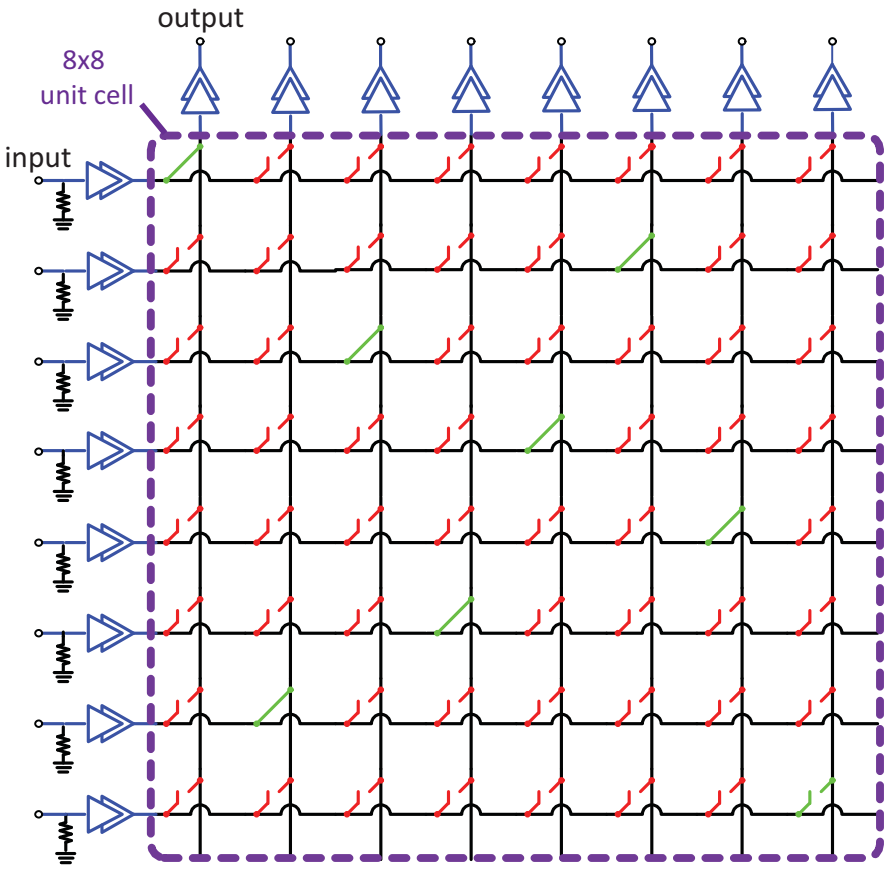


Figure 4.1: Block diagram of 8x8 single ended switch matrix.

According to metal stack-up in Fig. 4.2, UB metal layer (copper) is chosen to be the signal line instead of LB (Aluminum) because of the higher conductivity and less metal roughness variation. B3 metal layer is the ground plane which is 6.3 um to top metal layer to build transmission line and 2.8 um to bottom one. The lower metals are used for supply, biasing and logic routing. The row and column routing lines are 1 μm in width to have reasonable Z_o of the transmission line which will be discussed later. The simulated line loss is 1.2 dB at 20 GHz. Series-shunt-series switch is implemented at row and column cross point to achieve high isolation at off state. Fig. 4.3 illustrates the 'LEGO' single switch cell for the matrix. Transmission gate is used for the series switch instead of single transistor to get rid of the extra required 'stable time' causing by the DC initial voltage of the path when start up or change the switching configuration after a long idling time (Fig .4.4). The interconnection model of the series-shunt-series switch in Sonnet, on and off equivalent circuits model and simulated S-parameter are showed in Fig. 4.5. Trade off between R_{on} and C_{off} is made since R_{on} will causes the voltage droop while C_{off} will load the routing line. The R_{on} value of 40 Ω and C_{off} value of 20 fF is not optimized in this design but reasonable initiative ones which might be improved. For each row or column, there only will be one on switch while others off in mission mode. We can model the signal routing path as distributed capacitive loaded transmission lines which lower the Z_o of the unloaded one.

$$\begin{aligned} Z_0 &= \sqrt{L/C} \\ C &= C_{origin} + C_{load} \end{aligned} \tag{4.1}$$

The equivalent circuit with lumped elements and characteristic impedance calculation are showed in Fig. 4.6. We see that Z_o of 1 μm micro-strip line drop dramatically from 82 Ω to 24 Ω with the capacitive loading and this will transfer the open termination to a low impedance quicker and make buffer driving condition harder. Coupling between adjacent line is checked at 400 μm signal path with square wave input and simulation result shows less then 40 dB at 30 GHz (Fig .4.8).

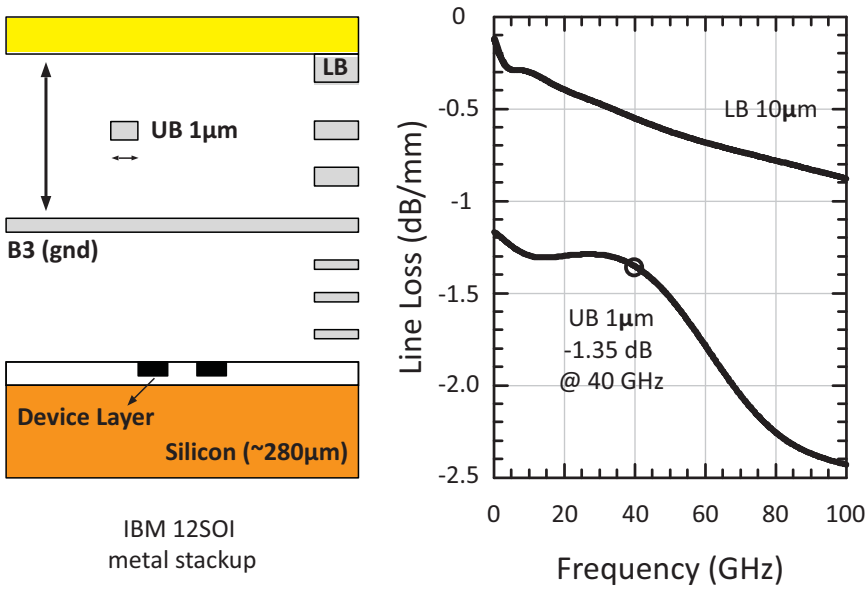


Figure 4.2: IBM 12SOImetal stack-up and simulated T-line loss versus frequency.

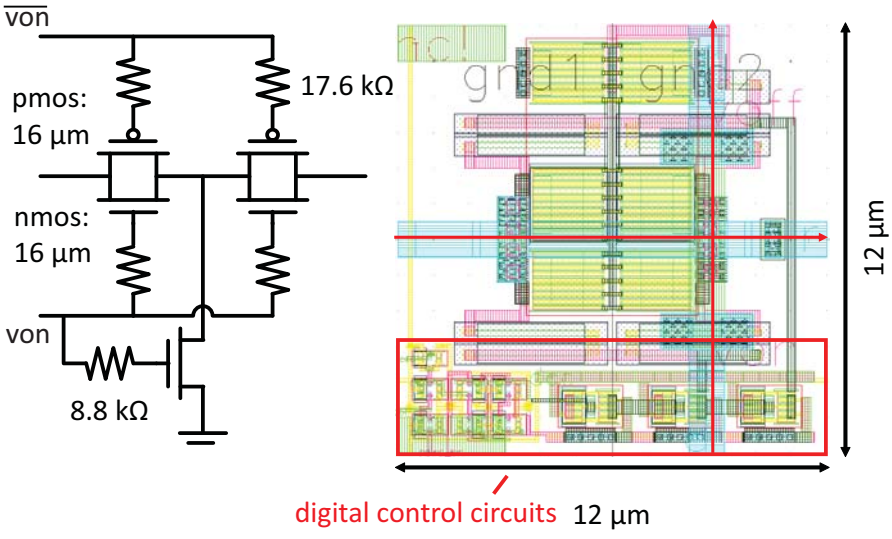


Figure 4.3: Single shunt-series-shunt CMOS switch schematic and illustrated layout.

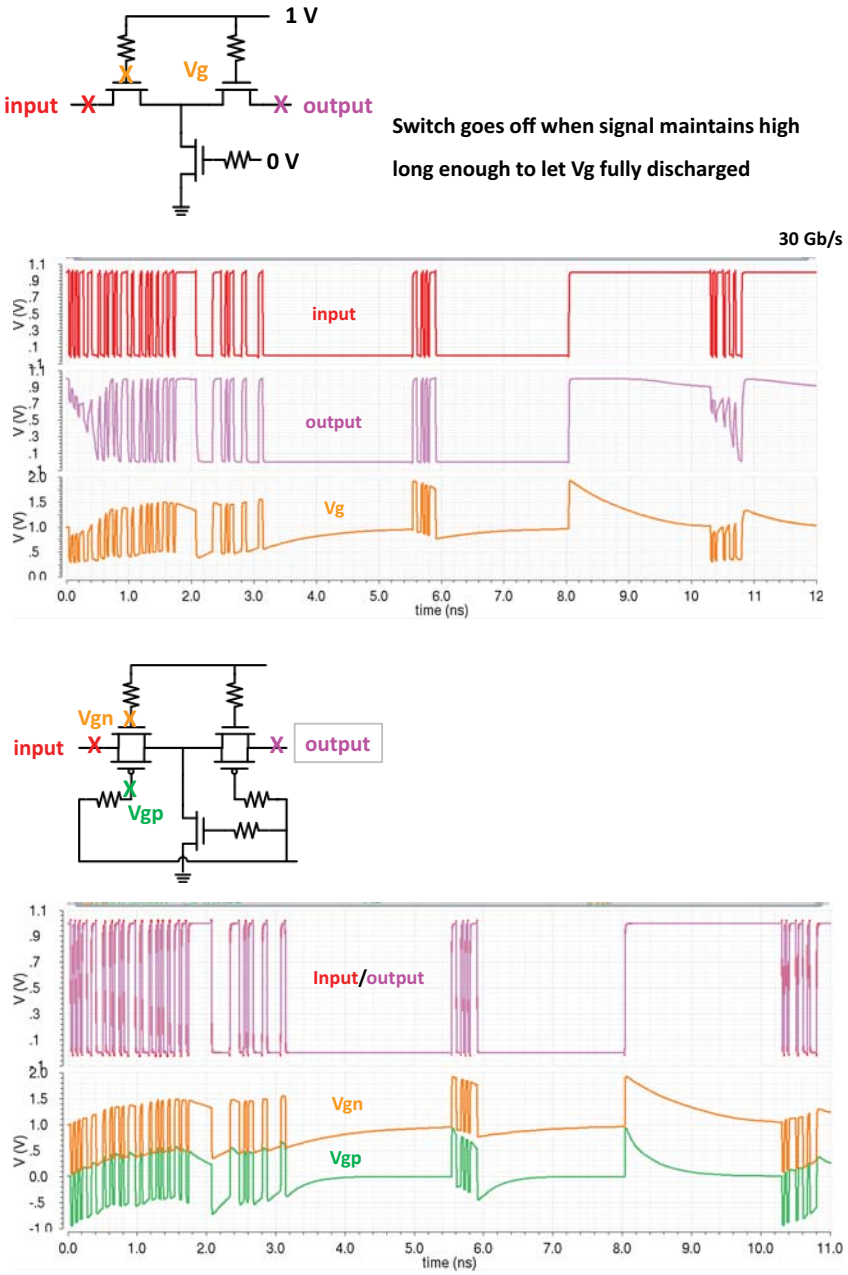
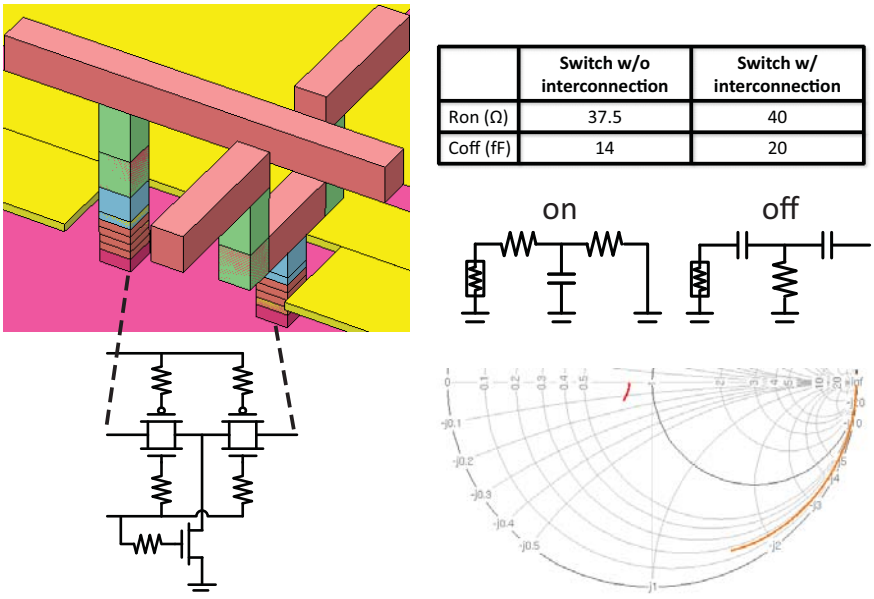
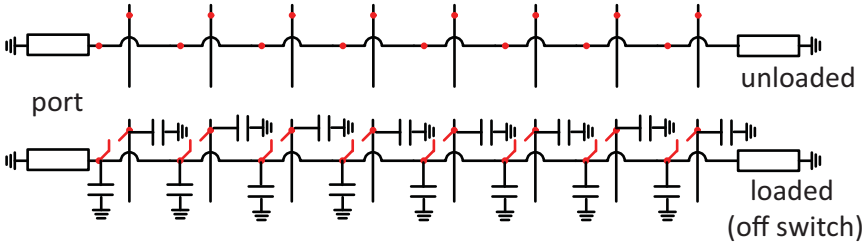


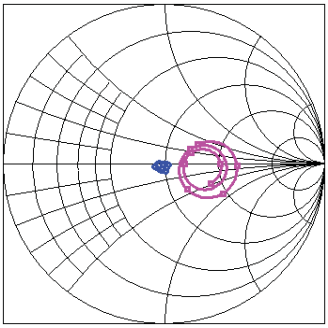
Figure 4.4: Comparison of single transistor switch and transmission gate based one on response of stimulation after long idle time pattern.



	Switch w/o interconnection	Switch w/ interconnection
Ron (Ω)	37.5	40
Coff (fF)	14	20

Figure 4.5: Series-shunt-series switch illustrated 3-D interconnection model in Sonnet, equivalent lumped circuits model and S-parameter simulation results.





	M-line (LB) W = 10 um	M-line (UB) W = 1 um	Unit cell w/ sw.
Zo	50	82	24
Er_eff	4.3	4.3	50
L	5.6e-7 H/m	5.6e-7 H/m	5.6e-7 H/m
C	2.2e-10	8.3e-11 F/m	9.7e-10 F/m
Added C			10.5 fF (12um)

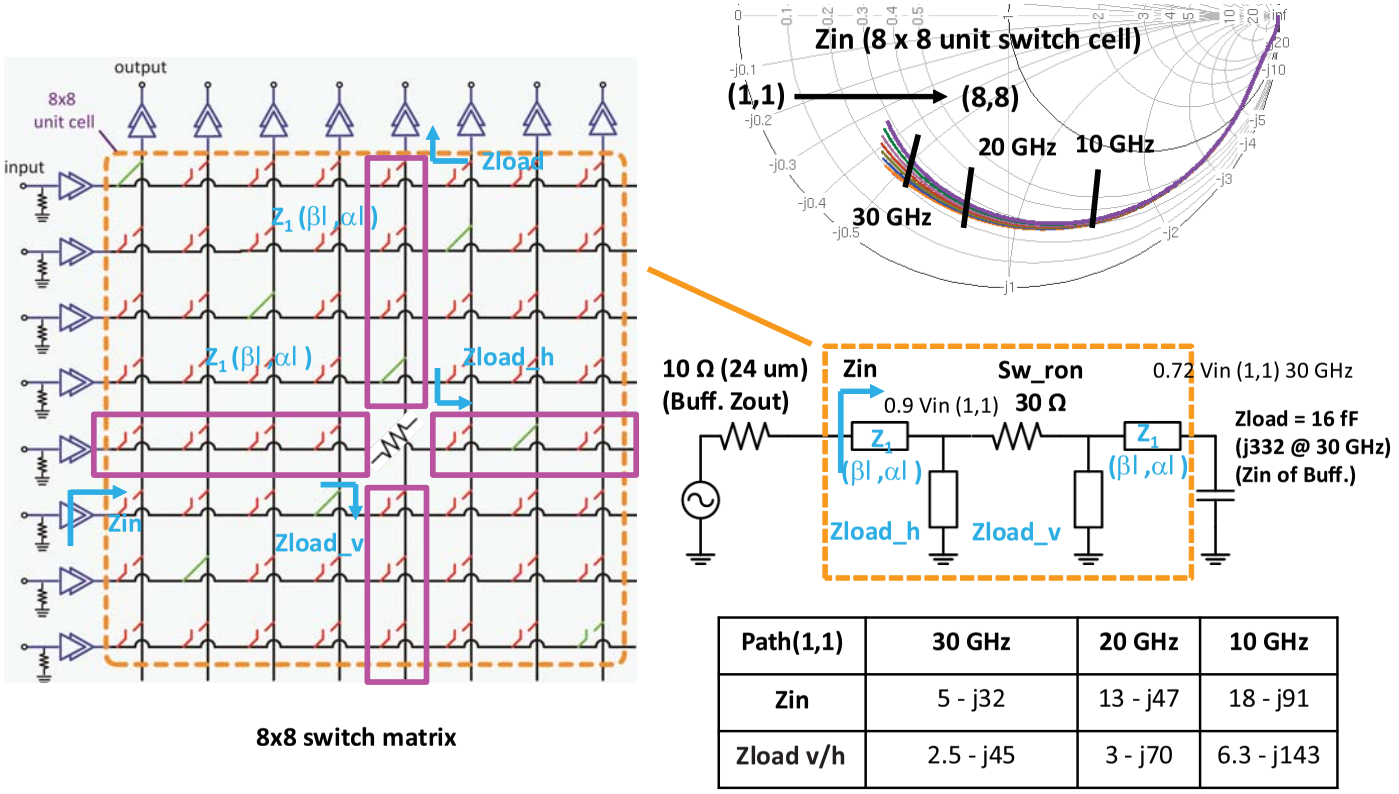
Figure 4.6: Stim of single transistor and.

The equivalent circuits model for the 8x8 matrix is illustrated in Fig. 4.7. The driving impedance see from the input buffer drops quickly versus frequency and the magnitude is only $\sim$32.4 at 30 GHz. Further increase the matrix size will make this impedance even smaller (magnitude of $\sim$17.7 16x16 passive matrix). Increasing the size of the buffer to have better driving ability will help to improve high frequency performance while power consumption will be increased proportionally.

Same input buffer and output are used in this design which cascades two inverters in a theocratical best fan out ratio of 1:3. Schematic and layout of the buffer are showed in Fig. 4.9. PMOS and NMOS size ratio is optimized to have the same strength so that the transition point is at half supply voltage. In order not to bend the output routing, the layout of the output buffer is modified to not the same as the input one. 50 Ω resistors at input of the matrix are tied to ground for matching while the output of the matrix are not matched to 50 Ω which will limit the maximum output magnitude.

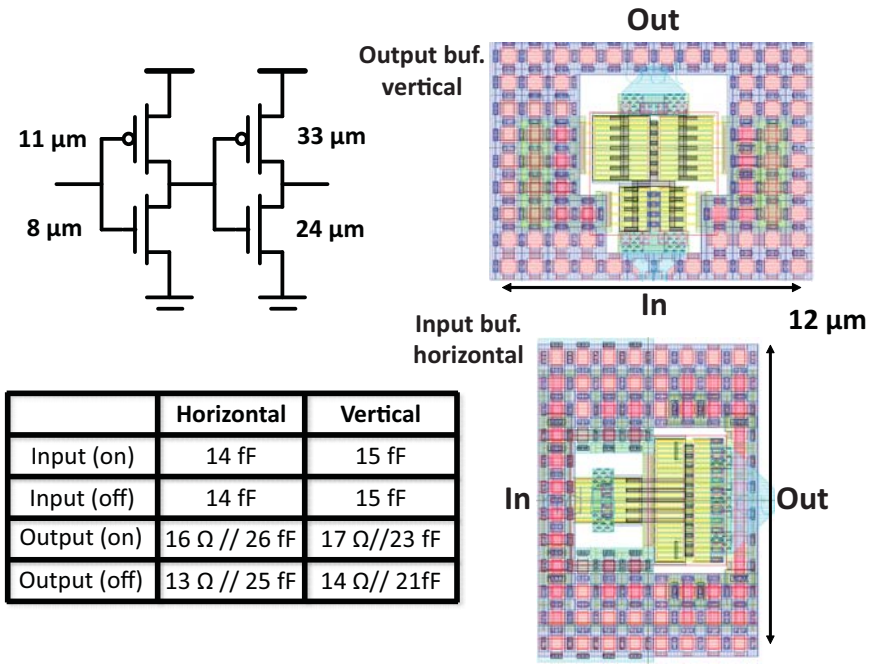
The 16x16 matrix block diagram is illustrated in Fig. 4.10. It is built using four of the 8x8 matrix to test the scalability. Some input buffers are tied together due to save pads and the required routing. Only part of the outputs are chosen to have the measurement access due to the same reason. According to the measurement results (next section), the 16x16 matrix shows a degraded performance and the author thinks the issue may due to the extra switch added in between the 8x8 matrices which divides the swing magnitude and thus narrows the bit width se from output buffers. One of the potential solution is to switch the buffer (for example to use head switch) instead of the signal path to improve the 16x16 matrix performance.

The matrices are fabricated using the Global Foundry 45 nm SOI process. The die (Fig. 4.11) occupies an area of 1.8mm x 2.0mm which is limited by the 100μm GSG pads. The core circuit is only 120μm x 120μm for the 8x8 matrix and 250μm x 250 μm for the 16x16 one. The routing from pad to buffer is modeled and simulated in Sonnet (Fig. 4.12). Matching is better than -15 dB and adjacent channel coupling is less than -30 dB up to 30 GHz.



Path(1,1)	30 GHz	20 GHz	10 GHz
Zin	5 - j32	13 - j47	18 - j91
Zload v/h	2.5 - j45	3 - j70	6.3 - j143

Figure 4.7: Equivalent circuits model for the 8x8 matrix.



	Horizontal	Vertical
Input (on)	14 fF	15 fF
Input (off)	14 fF	15 fF
Output (on)	16 Ω // 26 fF	17 Ω//23 fF
Output (off)	13 Ω // 25 fF	14 Ω// 21fF

Figure 4.8: Simulation of coupling between adjacent channels.

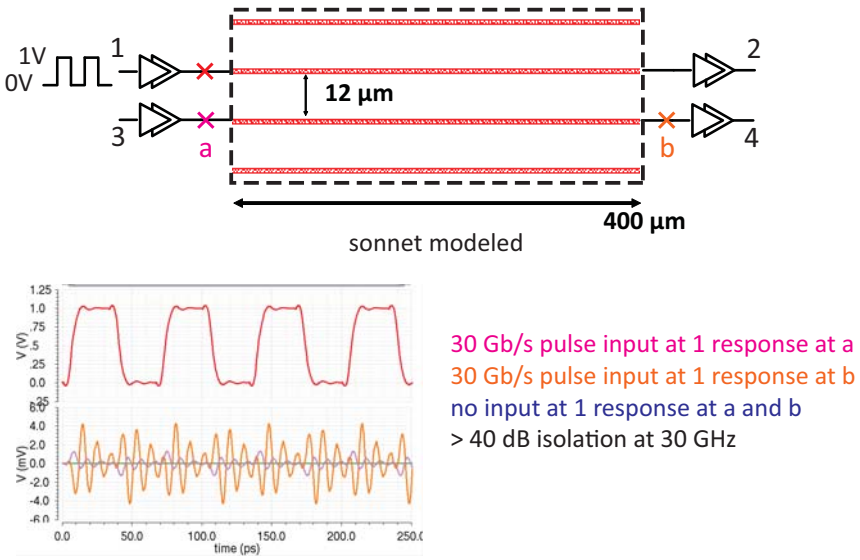


Figure 4.9: Schematic and layouts of input/output buffer.

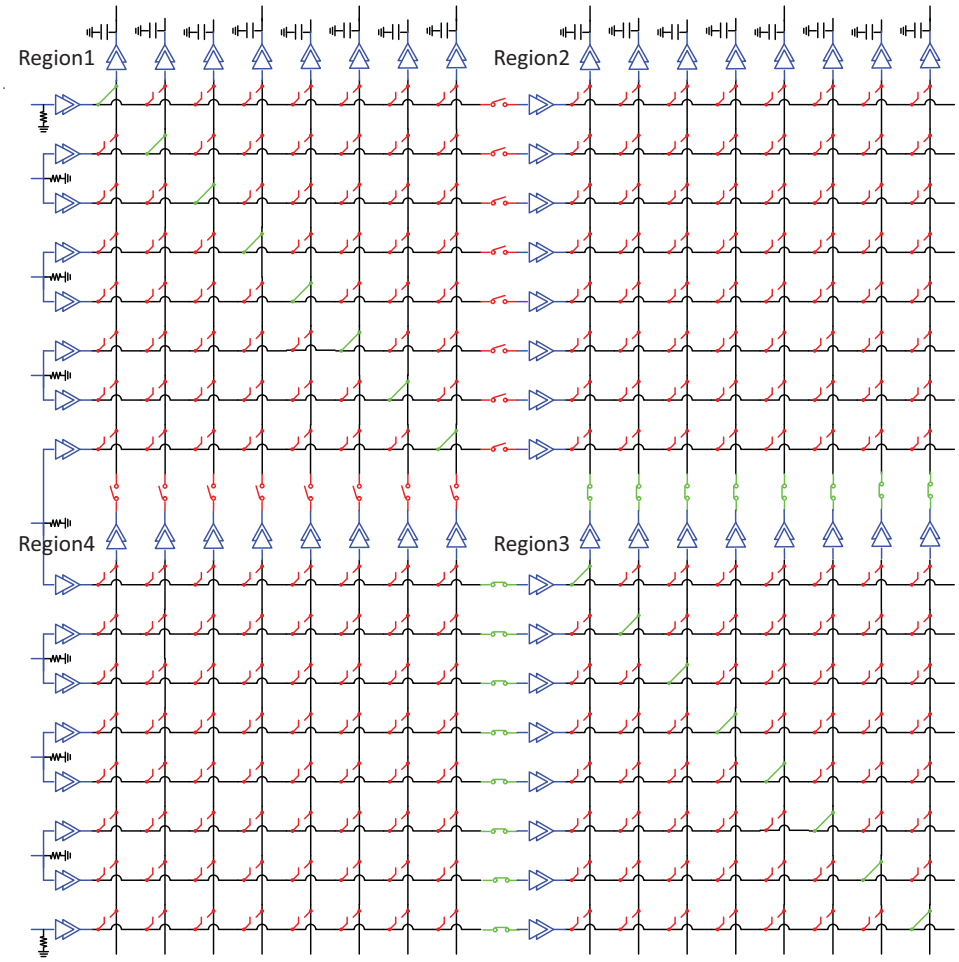


Figure 4.10: Block diagram of 16x16 single ended switch matrix.

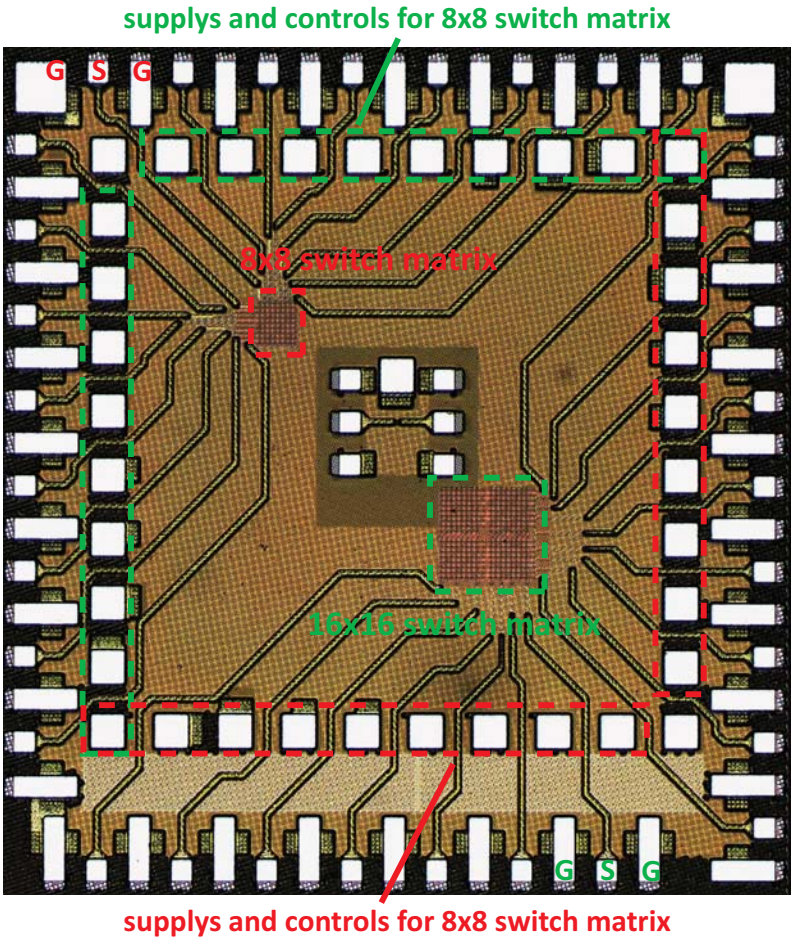
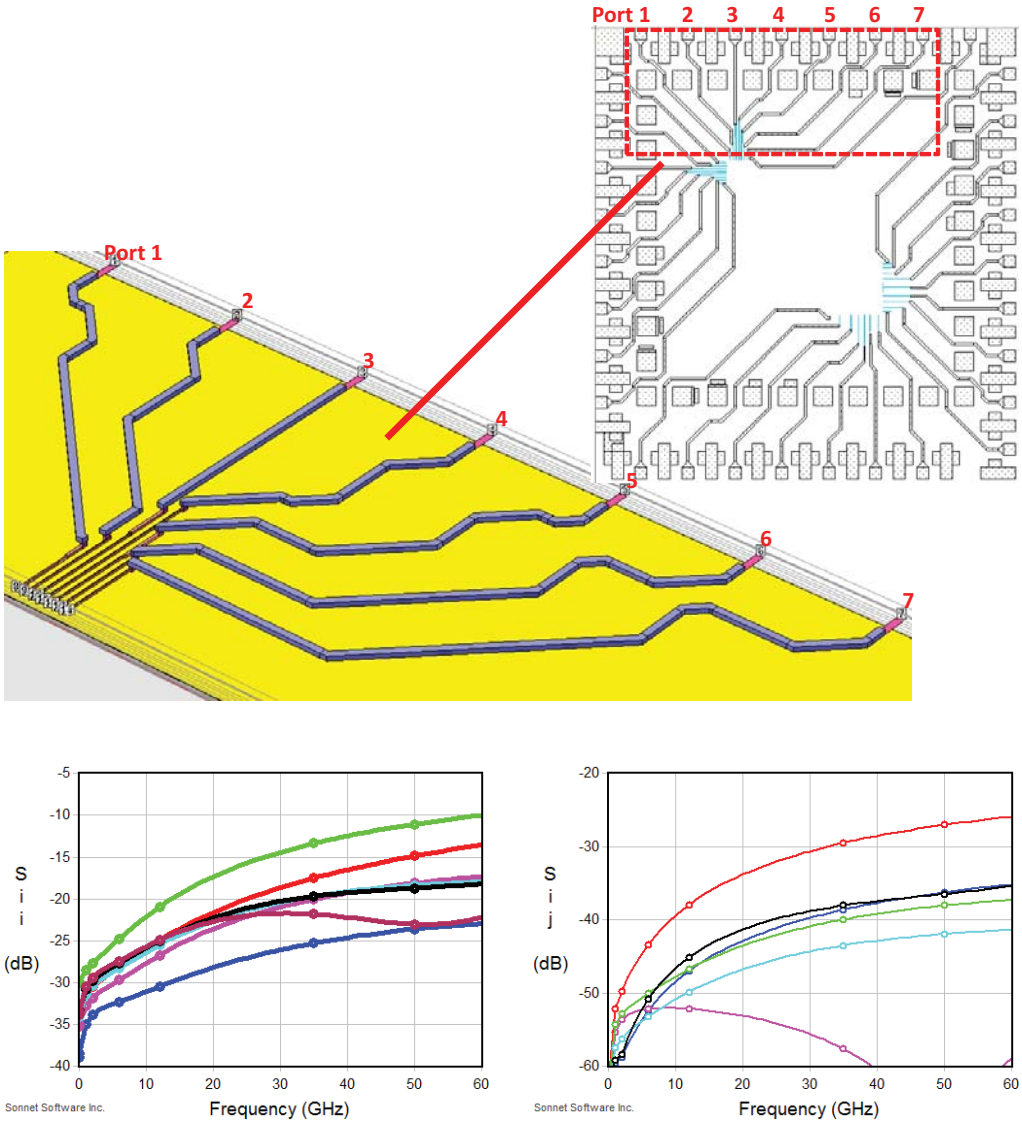


Figure 4.11: 8x8 matrix and 16x16 matrix die micrograph.



Input matching

$S_{j,j}$

neighbour couplig

$S_{j+1,j}$

Figure 4.12: Input/output routing from pad to buffer.

4.3 Measurements

Fig. 4.13 illustrates the lab measurement setup for both matrices. The chip are probed by two DC-50 GHz GSG probe. The input pattern is generated by Picosecond 12070 with a maximum speed of 30 Gbit/s. A 3-feet 2.4mm cable connected the input probe and the pattern generator due to physical limitation. The matrix output signal is then sampled right after the output probe by a Keysight N1045A sampling head which has a typical bandwidth of 65 GHz. The sampled signal is then evaluated by the Keysight 86100D oscilloscope ($>$ 100 GHz bandwidth). The negative port of the pattern generator is fed by another 3-ft cable and is also sampled as a reference. Pattern generator and oscilloscope are synchronized by the machine reference 10 MHz clk. The uneven response of the cable indicate more than 2 dB at 15 GHz and unfortunately this cannot be equalized or de-embedded. Worse jitter and smaller eye opening are observed as data rate increases. The eye diagram (Fig. 4.14, 4.15) indicates 16 ps peak to peak jitter at 30 Gb/s while more than half is contributed from the 3-ft feeding cable (Fig. 4.16). Jitter degradation due to the matrix it self is believed to be caused by narrower bit width of shrunken pattern at output buffer due to voltage division. Eye diagram for all row and column combination in Fig. 4.17 indicates that channel (1,1) is the worst case of all which agrees with the simulation observation for the lowest driving impedance of the input buffer. The real time waveform is also captured to prove no missing data since BER measurement is not available at this speed (Fig. 4.18). There will be no output when all switches are off so we believe the isolation is as good as expected. Blurred and smaller eye diagram will be observed if same input tied to two output at the same time which is as expected since the driving buffer sees a even lower impedance. Bit error rate (BER) estimation contour at 25 Gbit/s is showed in Fig. 4.19, 4.20 for both DUT output and reference feeding cable case. Greater than 10^{-9} BER can be achieved for random input pattern. Speed limitation of the matrix itself is not easy to estimate not only due to the feeding cable frequency degradation but also the input source speed limitation.

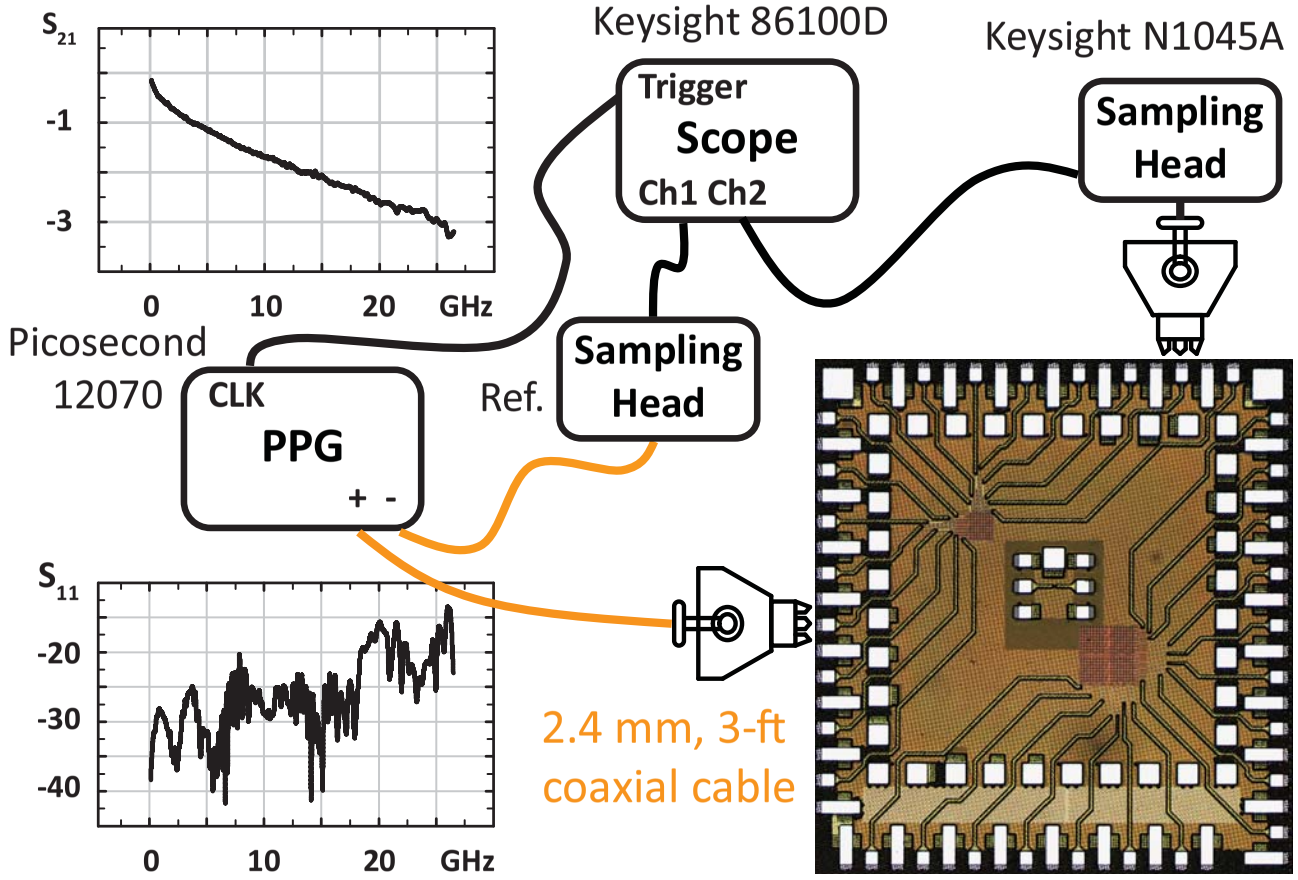


Figure 4.13: Equivalent circuits model for the 8x8 matrix.

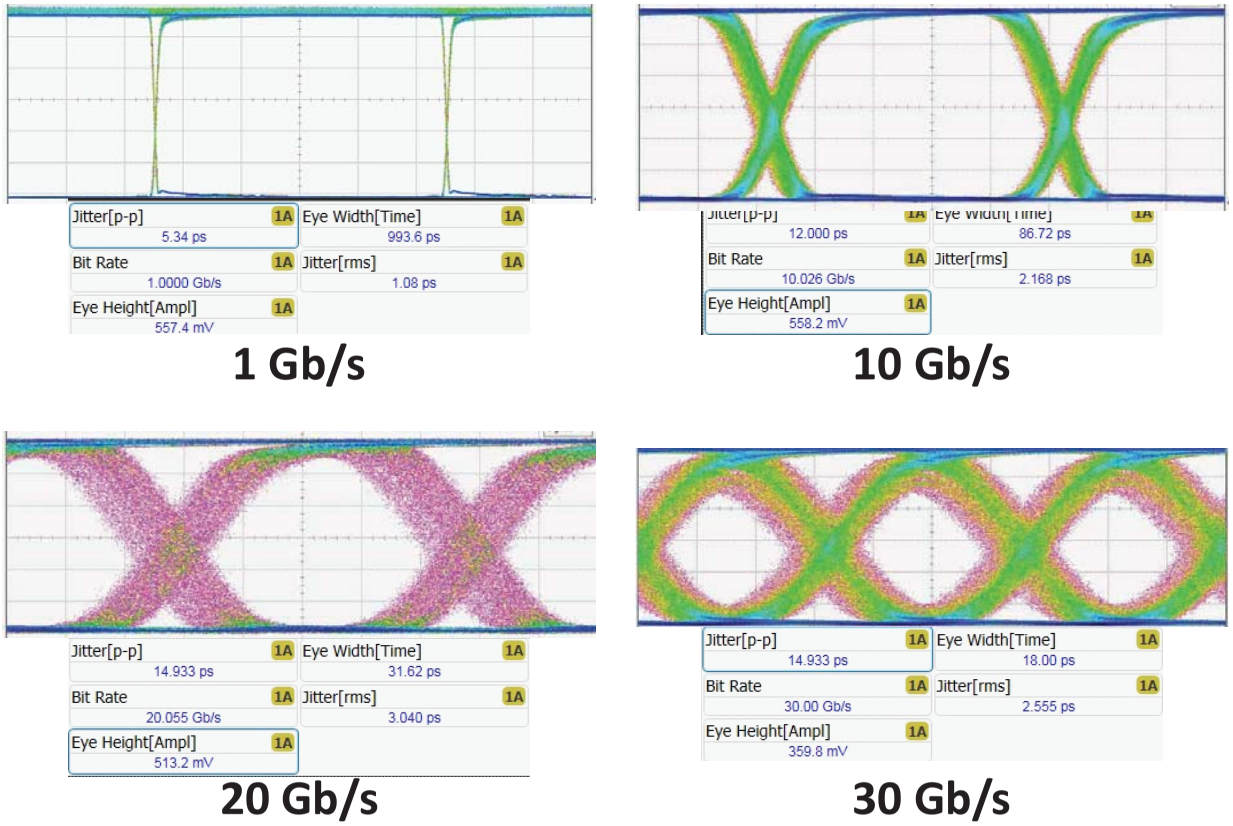


Figure 4.14: Eye diagram at 1, 10, 20, 30 Gb/s for channel(8,8).

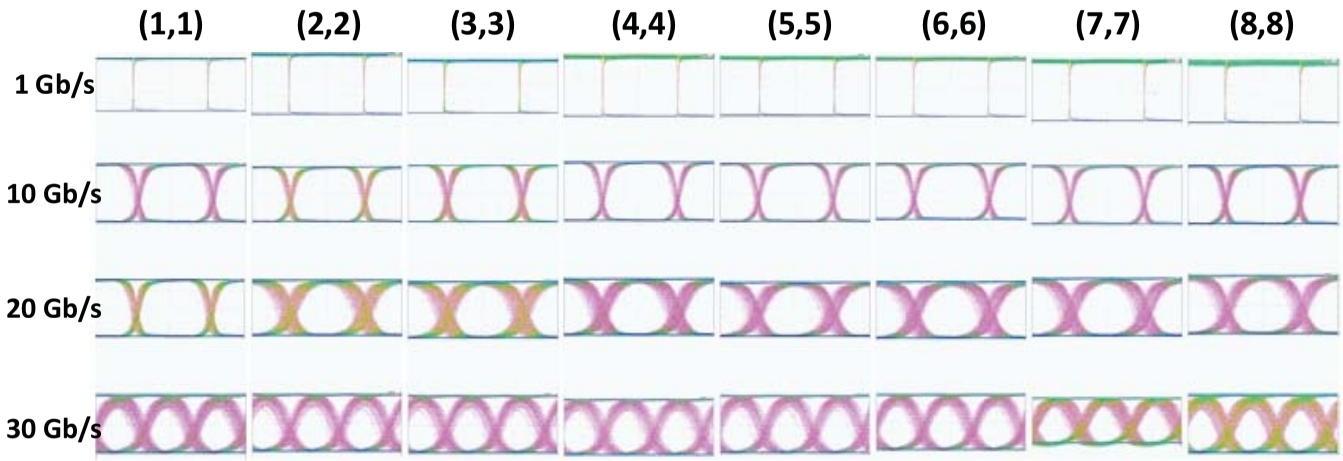


Figure 4.15: Eye diagram at 1, 10, 20, 30 Gb/s for diagonal channels.

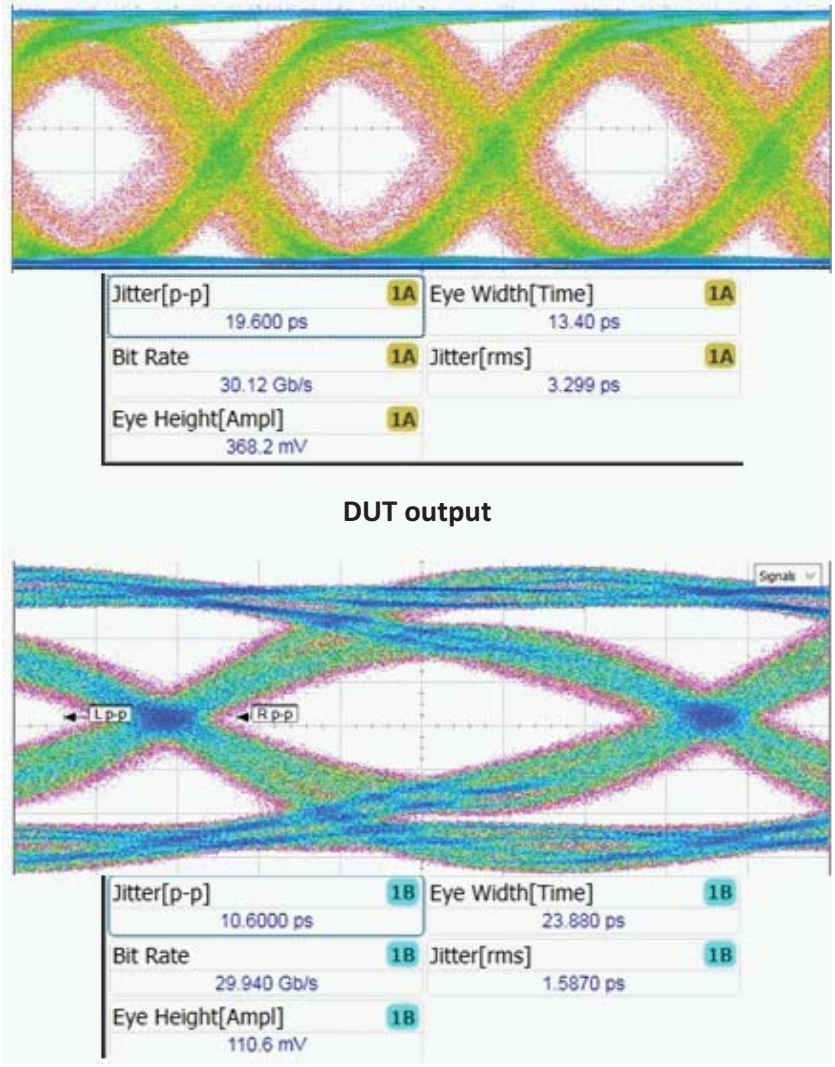


Figure 4.16: Eye diagrams at DUT(device under test) output(channel(1,1)) and 3-ft feeding cable output at 30 Gb/s.

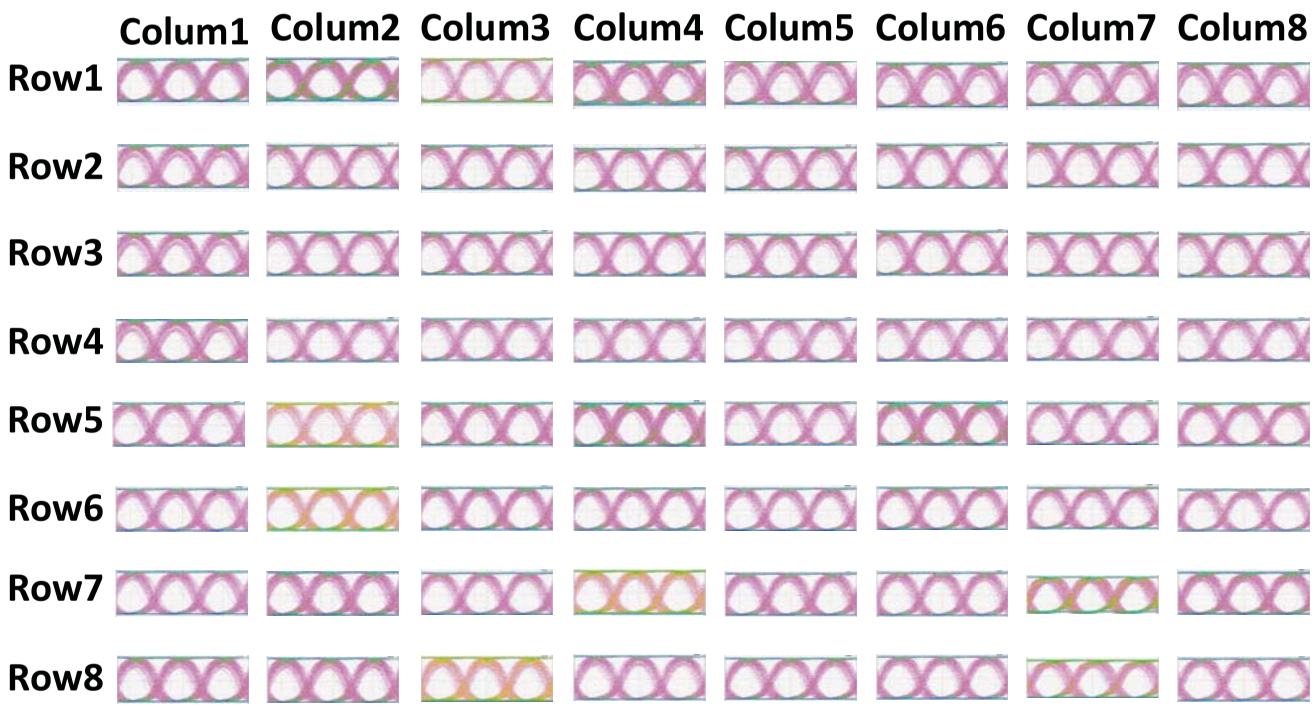


Figure 4.17: Eye diagram at 30 Gb/s for all channels.

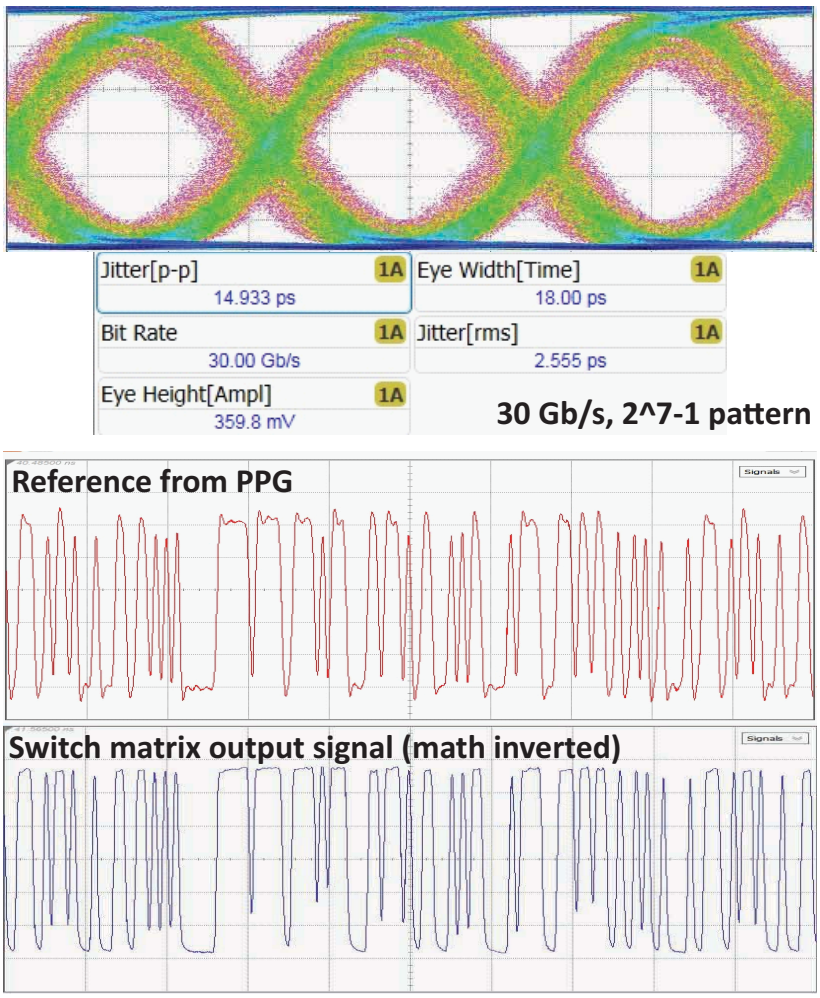


Figure 4.18: Eye diagrams and waveform for channel(5,4) at 30 Gb/s.

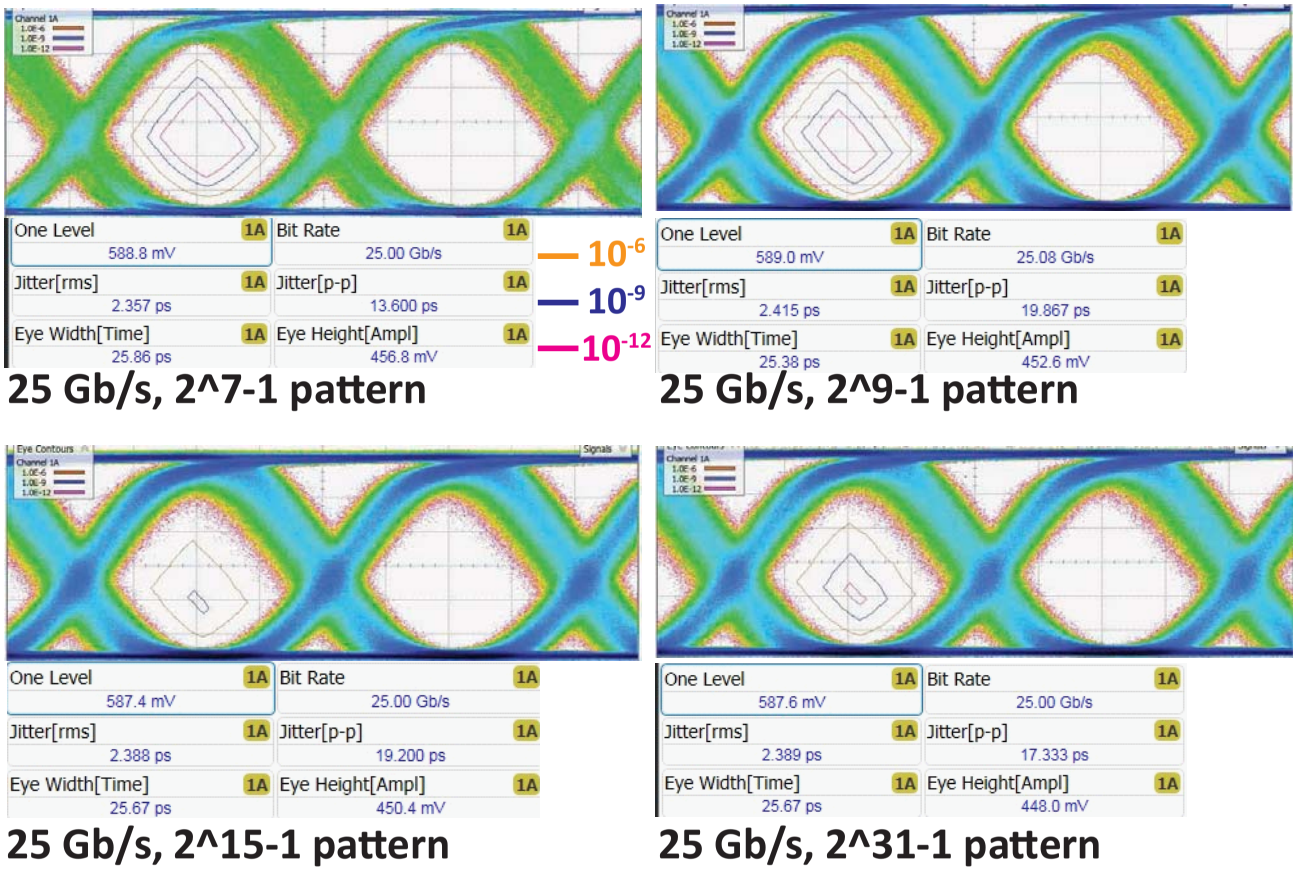


Figure 4.19: Channel(1,1) contour at 25 Gb/s for different patterns.

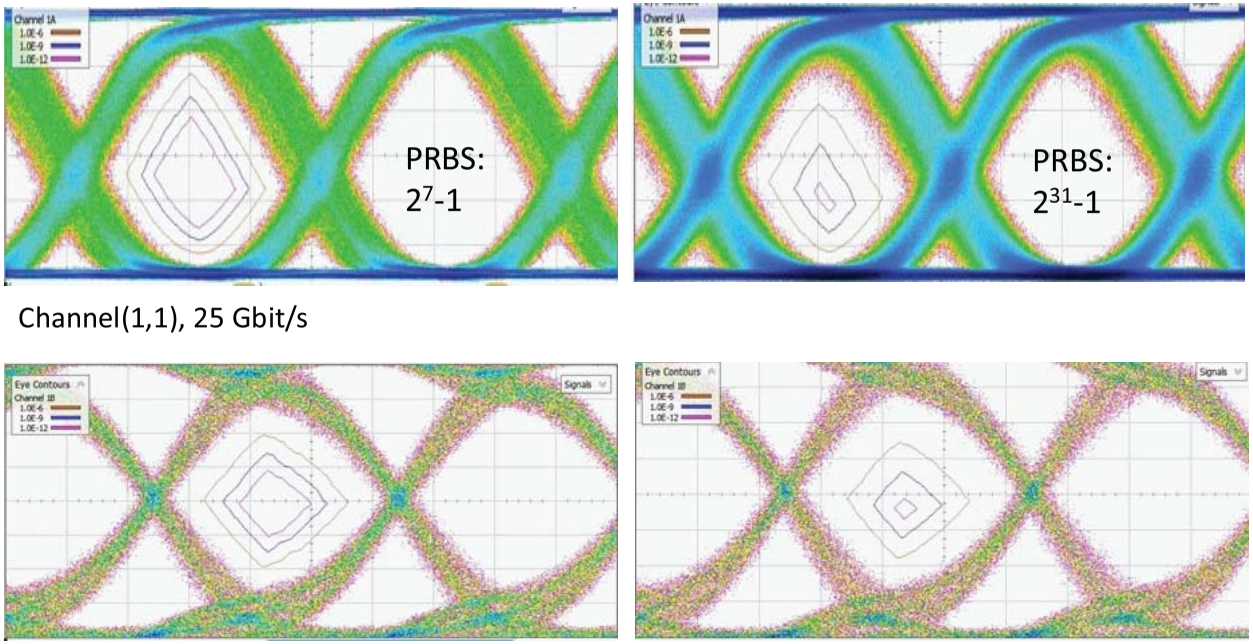


Figure 4.20: DUT output contour and reference output contour.

According to simulation, channel output eye still opens at 50 Gb/s. Current consumption versus data speed is plotted in Fig. 4.21 and the number is the average of the 8 diagonal channels. Power consumption for single channel is 0.24pJ/bit which is state-of-the-art. Measurement results of some representative channels of the 16x16 matrix are presented in Fig. 4.22, 4.23, 4.24, 4.25. In order to observe 10^{-12} contour with 2^{31}-1 pattern, channel(8,16) in region 2 can only achieve data rate of 19 Gb/s. The value drops to 17 Gb/s for channel(9,9) in region 3. The longer the signal path, the smaller of eye opening and worse jitter. The author thinks the issue is due to the additional signal division when passing the extra switch (there is one extra switch for channels in region 2/4 and 2 extra switches for channels in region 3) which narrows the bit width as discussed before. This performance degradation hypothesis need to be proved and fixed for larger scale cascaded matrix design implementation.

4.4 Conclusion

This paper presented two cross-point connection matrices. A 8x8 one and a 16x16 one built using the 8x8 matrix. Lumped circuits model for switch loaded transmission line is developed. Tradeoff between speed and power consumption is discussed. Measurement results are showed to demonstrate the matrix can achieve 30 Gb/s while only consumes a power of 0.24pJ/bit. The design is a great fit for ultra low power high speed digital signal data traffic and the scalability can be improved with not much efforts.

4.5 Acknowledgment

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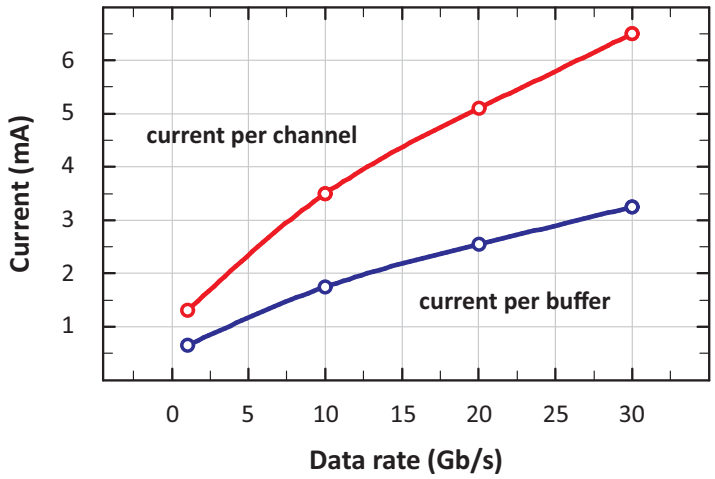
Chapter 4 is mostly reprint of the materials as will be submitted to *IEEE Transactions on*

Microwave Theory and Techniques, 2018. Y. Yang G. M. Rebeiz. The dissertation author is the primary author of the source material.



Current (mA)	(1,1)	(2,2)	(3,3)	(4,4)	(5,5)	(6,6)	(7,7)	(8,8)	Avg.
1 Gb/s	1.1	1.2	1.3	1.6	1.3	1.3	1.3	1.3	1.3
10 Gb/s	3.5	3.4	3.3	3.4	3.5	3.6	3.7	3.8	3.5
20 Gb/s	5.1	5.0	4.8	4.9	5.1	5.2	5.4	5.6	5.1
30 Gb/s	6.4	6.2	6.0	6.2	6.4	6.7	6.9	7.2	6.5

Figure 4.21: Measured current versus data rate.

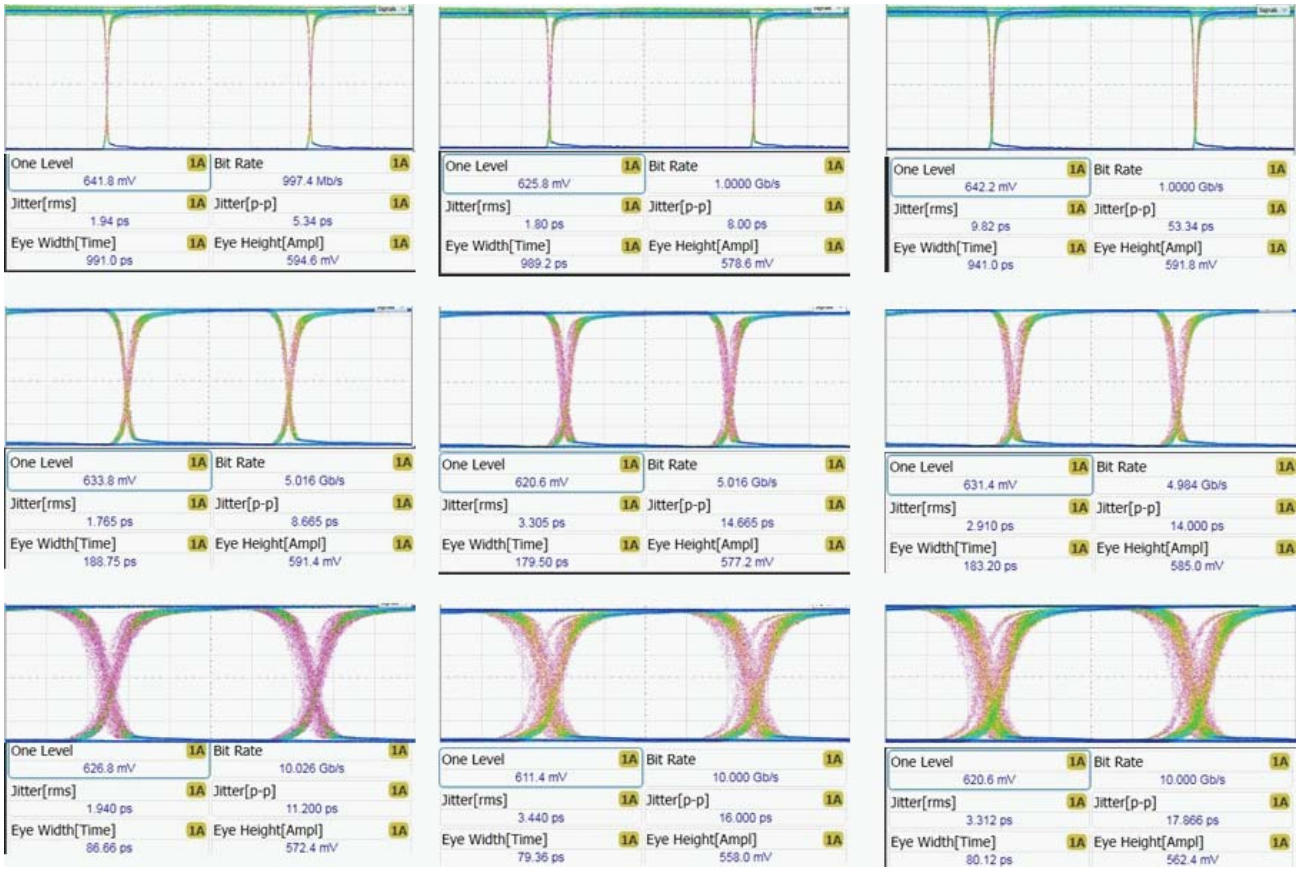


Figure 4.22: Channel (1,1)(9,9)(16,16) measured at 1, 5, 10 Gb/s.

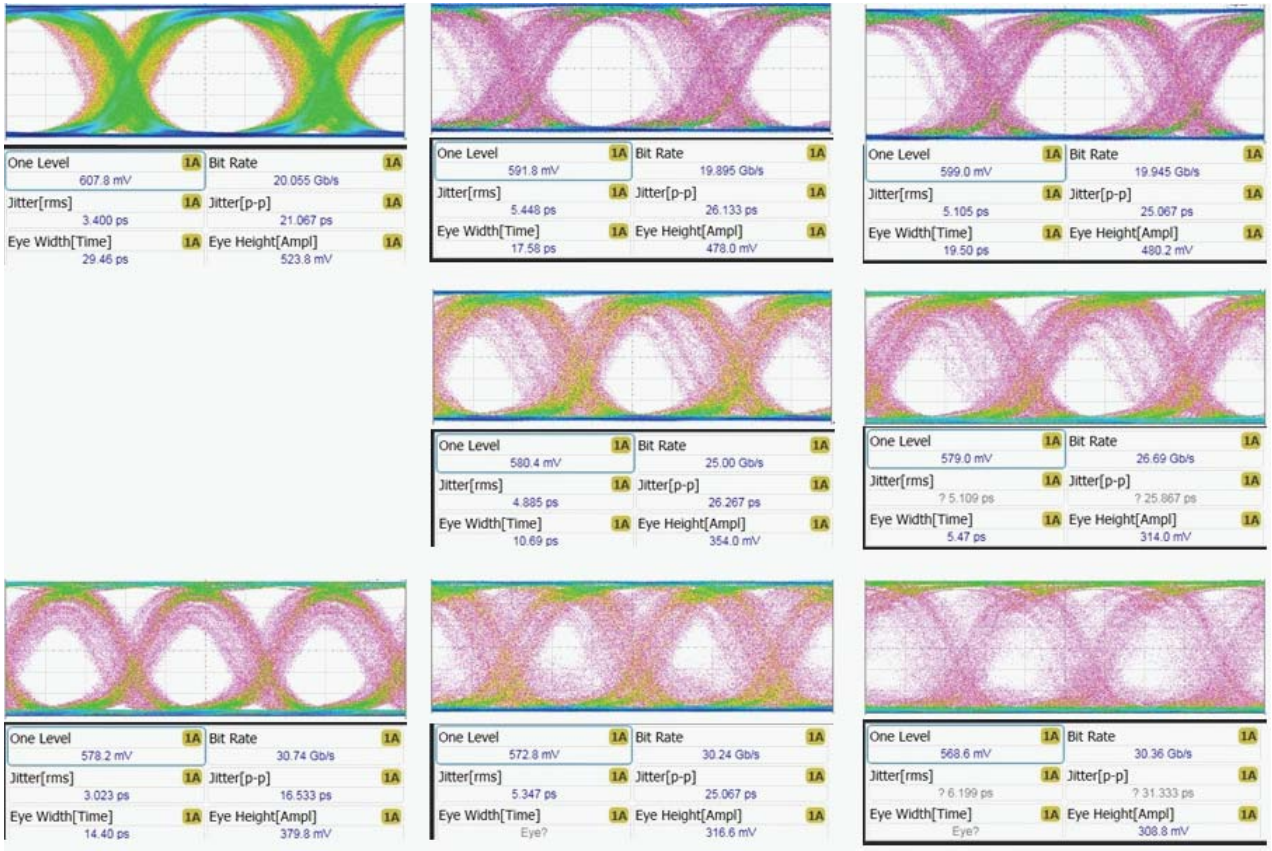


Figure 4.23: Channel (1,1)(9,9)(16,16) measured at 20, 25, 30 Gb/s.

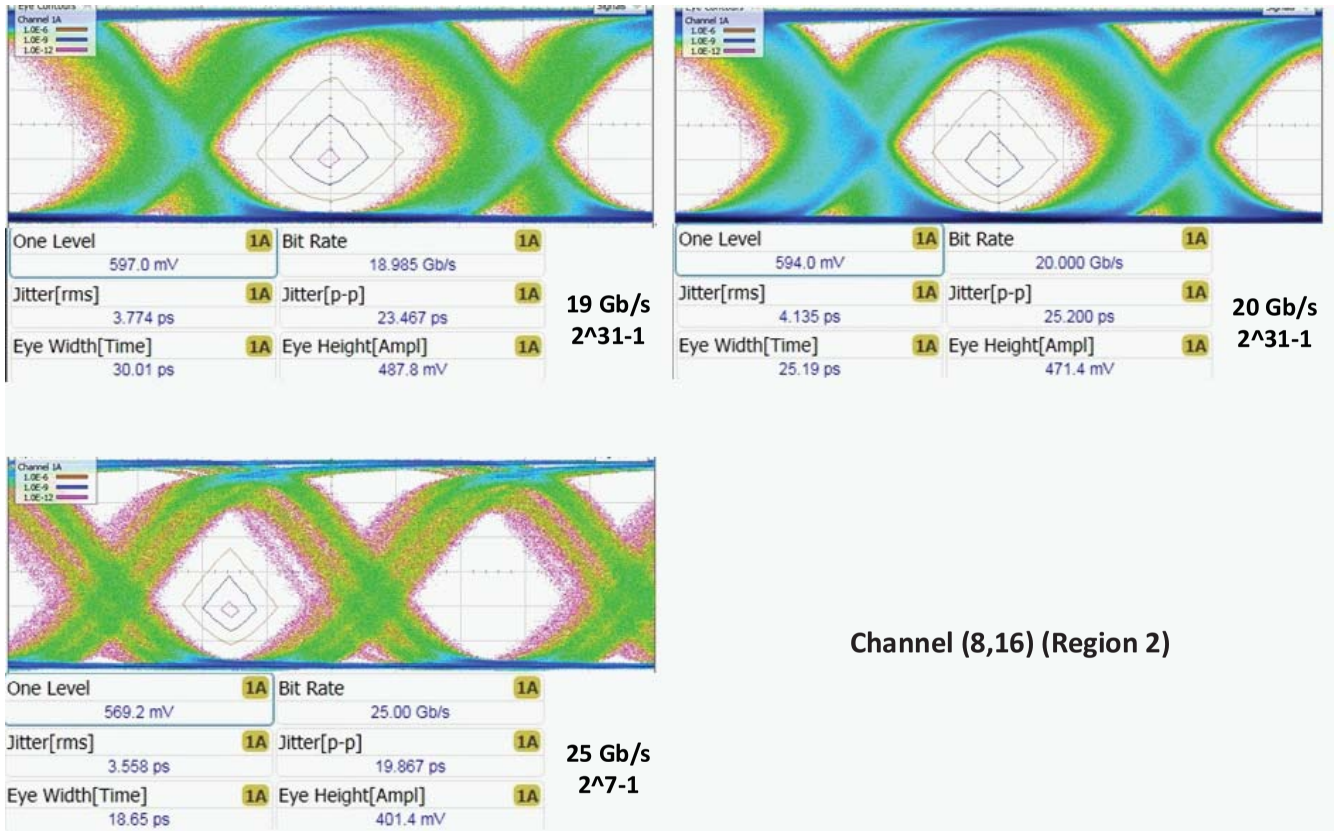


Figure 4.24: Channel (8,16) measured contour.

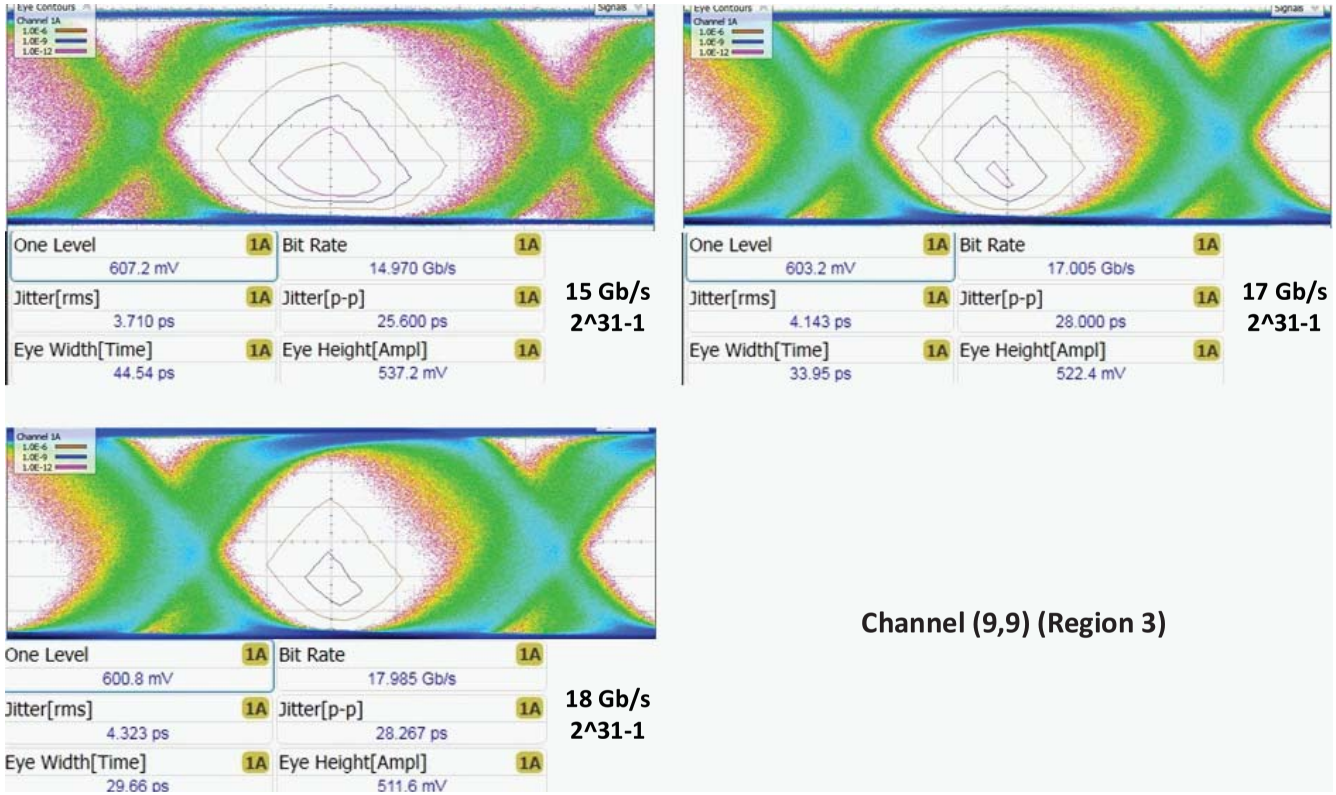


Figure 4.25: Channel (9,9) measured contour.

Chapter 5

Conclusion

The thesis presented two RF subsystems (transmitter/receiver) for high speed wireless links at mm-wave/THz band and two ultra low power switch matrices to handle rapidly increasing data traffic in communication networks. All of the design are implemented in 45 nm CMOS SOI process.

Chapter 2 presented a eight by one phased array transmitter working at 370-410 GHz with peak EIRP of 8.5 dBm. The 3-bit phase control for each element allows the transmitted pattern to be scanned up to +/- 35^o. Challenge to generate enough power and implementing phase shifting at such high frequency is discussed. Proposed design to implement phaser shifting at W-band then multiply the frequency to desire band is talked in detail.

In Chapter 3, a state-of-the-art 155 GHz 20 Gbit/s QPSK transceiver front end including VCO, power splitter, modulator, mixer and wide-band baseband amplifier is demonstrated. Detailed design and measurement results of each block are talked and showed. The transceiver consume a total power of 345 mW (17.2pJ per bit) and is 3.9 mm^2 in size. The modulator delivers an output power of 1 dBm output power which together with the high free space path loss limits the system to a short distance link application.

As a final work, Chapter 4 presents two switch matrices. Motivation and design challenges

towards high data rate are discussed. Circuits model of signal routing and termination choosing are investigated. The 8 by 8 switch matrix can run up to 25 Gbit/s while consumes only 7.2 mW per channel. The 16 by 16 switch matrix is built using four 8 by 8 matrices to test scalability. It can achieve a data rate of 20 Gbit/s per channel and consumes 139.2 mW if all 16 channels are at mission mode.

5.1 Future Works

For the phased array transmitter, extra loss and lower then expected radiated power was observe when steering the beam. According to post simulation, the reason might be the extra 7 dB loss of phaser shifter causing amplifier not saturated so for different phase setting gain varies. This extra loss is caused by a design mistake which can be fixed easily. The phase shifting technique using in this design is not suitable for QAM (quadrature amplitude modulation) which need to be modified for higher order modulation in order to get higher data rate with certain bandwidth.

For the D-band transceiver, to improve performance of the whole transceiver, low noise amplifier(LNA) and power amplifier(PA) at D-band need to be built. LNA will help with the signal to noise ratio(SNR) which allows implementation of higher order modulation for higher data rate with given bandwidth. PA will help with extending the link distance with higher output power. Besides the front-end circuits, data recovery circuits, phase-locked loops, analog to digital converter (ADC) can be added to fulfill a complete transceiver system.

For the matrices, the issue of degraded performance when scale the 8x8 matrix to a larger size is discussed and a potential solution is to remove the switches in between the 8x8 matrices and implements switching in buffers, for example to use head switch in the buffer. While the head switch may introduce extra resistance for mission mode and cause driving issue, so it might be a better option to put the switch between NMOS and ground instead. On chip sampling can be

implemented to get rid of the performance degradation caused by the 3-ft feeding cable and help to have a more accurate performance evaluation of the matrix itself.

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