Chip Scale Topography Evolution Model for CMP Process Optimization

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Abstract – A new chip scale model integrating pad height distribution and it's interaction with topography on a patterned wafer was tested. Pad asperity height distribution was used to calculate mean contact pressure at a single asperity contact region. Material removal by a single asperity was evaluated from Hertzian elastic contact model and abrasive indentation model. Simulation on a test pattern predicted relatively higher removal rate and lower planarization efficiency with higher nominal down pressure. Oxide thickness variation over a test chip for a time period measured from specially designed test structure matched well with the model prediction.

INTRODUCTION

Chemical Mechanical Polishing (CMP) has been used to achieve feature level planarization with global uniformity over a chip and a wafer. Use of polymer pad with conformality enables uniform contact between wafer and pad over a wafer scale. However, conformality of polymer pad also induces pattern dependency in a chip scale during polishing process. There are many factors affecting pattern dependency of a CMP process, which include polishing down pressure, speed, passivation mechanism of recessed area, initial topography, and pad surface condition. A robust physical model integrating these factors with pattern dependency in CMP process can be used to optimize a CMP process for better within die non-uniformity (WIDNU), to optimize deposition thickness in copper electroplating or oxide CVD step for better global planarity in a CMP process. Empirical pattern density dependent models for characterization and simulation of chip scale variation [1, 2] have been used successfully for CMP process characterization and optimization. Based on more physical reasoning, some models [3, 4] explained that the pattern dependency in a CMP process is induced by non-uniformity of local contact pressure over a chip based on flat pad surface model, where pad surface is assumed to be ideally flat. Then contact mechanics from elasticity theory was applied to calculate topography dependent local contact pressure. However, CMP pad surface is rough compared to the topography on a wafer surface, and the roughness of the pad surface plays an important role in maintaining material removal rate throughout a CMP process. Also it is believed to affect planrization efficiency. Pad glazing and wear of asperities make the pad surface smooth and the removal rate tends to drop. Pad conditioning to keep a pad surface rough is commonly used in-situ in CMP application. Hence the effect of pad surface roughness should be considered in a comprehensive chip scale modeling. Among many different parameters representing CMP pad surface, surface height distribution is known to be sensitively changing with pad conditioning process [5, 6]. Pad height distribution affects mean local asperity contact pressure, which affects overall pressure dependency of a CMP process. In this work we present a comprehensive chip scale topography evolution model based on the evaluation of the individual asperity contact pressure and overall asperity height distribution, which was integrated with conventional empirical chip scale modeling scheme.

PAD SURFACE MODEL

CMP pad surface plays two important roles for material removal; one is to deliver slurry to the material removal region and to remove byproduct. The other role is to exert pressure on individual material removal region. Pore structure play the former role and wall structure between pore plays the second role. Two-body abrasion at the contact regions between pad asperity and wafer is believed to be the main material removal mechanism in a CMP process using abrasive slurry [7]. Hence it is important to model the contact region between pad asperity and wafer for a physical model of material removal in CMP process. Because of the non-uniform pore size, shape, and rough cutting surface of the wall structure of a pad, contact areas for two body abrasion between pad and wafer have non-uniform shape and size. Also, it is randomly distributed over the surface. Statistical approach is required to calculate effective modeling parameters representing pad surface. For a local asperity contact, Hertzian elastic contact was assumed.

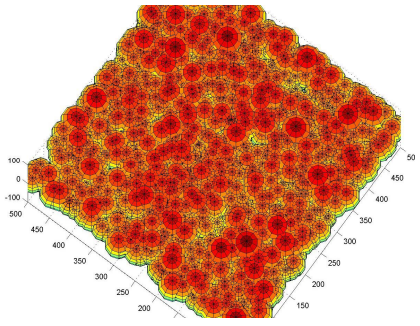

Figure 1. Pad surface model with Gaussian asperity height distribution and Herzian asperity contact

Asperity shape was assumed to be hemispherical and the deformation of asperities was assumed to be much smaller than the radius of the asperity. Pad surface with randomly generated asperities with same shape and Gaussian height and size distribution is shown in Figure 1.

MATERIAL REMOVAL AT A SINGLE ASPERITY CONTACT REGION

Pad asperity deforms as a wafer is pressed on to the pad. Real contact between pad and wafer happens at many different local contact points, where pad asperity and wafer topography directly interact. Local contact pressure at each contact area differs from each other with different asperity deformation. High asperity deforms more and exerts higher contact pressure than low asperity. Wafer surface also has topography because of the underlying pattern on the wafer. Asperities of different height and varying wafer surface topography lead to differing engagement length between asperities and topography, which is represented as ε in figure 2. A key modeling concept is to model the effect of ε on material removal per asperity and find the effective value over the pad for each location on the wafer. At the asperity-wafer contact region, contact force, contact area and mean contact pressure can be given as a function of ε by Hertzian contact assumption (equation 1-3 from [8]). a is the diameter of contact area and κ_s is the curvature of the asperity. The Effective young's modulus E^* in the equation is given by the Young's modulus and Poisson ratio of the pad and wafer material.

$$A = \pi a^2 = \frac{\pi\varepsilon}{\kappa_s} \tag{1}$$

$$F = \frac{4}{3} E^* \kappa_s^{-1/2} \varepsilon^{3/2} \tag{2}$$

$$P_m = \frac{4}{3\pi} E^* \kappa_s^{1/2} \varepsilon^{1/2} \tag{3}$$

$$\text{where, } \frac{1}{E^*} = \frac{1-\upsilon_{pad}}{E_{pad}} + \frac{1-\upsilon_{film}}{E_{film}}$$

Abrasive particles are captured at the asperity-wafer contact region. Then move over the wafer surface by pad motion and material removal occurs at the abrasive-wafer contact area. Material removal by a single asperity contact region increases with the number of abrasive particles captured in the contact area. The chance for an asperity to capture abrasive particles increases as ε increases, and as the asperity contact area increases. Effectively over a pad, the number of abrasive particles captured in an asperity contact region was assumed to be proportional to the contact area. Material removal by a single abrasive particle increases as the pressure exerted on the particle increases. With an assumption that the abrasive particle has spherical shape and the material removal by a single abrasive particle is proportional to its static indentation area, material removal by a single abrasive particle can be expressed as equation 4.

$$\frac{H_W^{-3/2}}{2R\sqrt{\pi}} F^{3/2} \tag{4}$$

Where, H_w is the hardness of the material being polished, R is the radius of the abrasive particle, and F is the force applied to a single particle, which changes as the contact pressure at the asperity contact region varies. From Hertzian contact model (equation 1-3) and equation 4, material removal by a single asperity can be expressed as equation 5.

$$\frac{\text{material removal}}{\text{asperity}} \propto H_W^{-3/2} R^{-1} E^{*3/2} \kappa^{-1/4} \varepsilon^{7/4} \tag{5}$$

CHIP SCALE TOPOGRAPHY EVOLUTION MODEL

Wafer surface can be expressed as a surface height distribution function z(x, y), which is eventually a function of chip layout. Pad asperities also have height distribution function. The population of pad asperities with height δ corresponds to PHD(δ) times total number of asperities moving over the position (x,y), where PHD is pad height distribution function. Figure 2 shows parameters used in the model. The center of pad asperity height distribution is located at $\alpha + z_{pad}$, where z_{pad} is the parameter determining mean distance between pad and wafer, and α is a parameter determining non-active asperities. It was assumed that the number of asperities with height greater than α can be ignored. Mean material removal by single asperity at location (x, y), where the surface height is z(x, y), can be expressed as equation 6. C is fitting constant that has to be determined experimental calibration. Mean contact force, C_F at location (x, y) on a chip was calculated from Hertzian contact model and pad height distribution (equation 7). In each time step, z_{pad} was determined from force balance by iteration until the sum of local mean contact force, C_F over a chip is balanced with the total force, which is nominal down pressure times the area of the chip (equation 8).

$$R_a(x,y) = C \cdot H_w^{-3/2} R^{-1} E^{*3/2} \kappa^{-1/4} \frac{\int_{z_{pad}}^{z(x,y)} \varepsilon(x,y,\delta)^{7/4} \times PHD(\delta) d\delta}{\int_{z_{pad}}^{z(x,y)} PHD(\delta) d\delta} \tag{6}$$

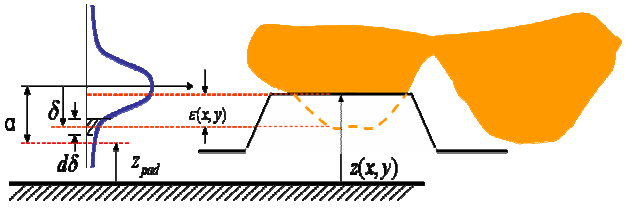

Figure 2. Parameters for the modeling of the interaction of pad asperity height distribution and wafer topography

$$C_F(x,y) = \frac{4}{3} E^* \kappa_s^{-1/2} \frac{\int_{z_{pad}}^{z(x,y)} \varepsilon(x,y,\delta)^{3/2} \times PHD(\delta) d\delta}{\int_{z_{pad}}^{z(x,y)} PHD(\delta) d\delta} \quad (7)$$

$$P_{\text{nominal}} \times A_{\text{chip}} = \sum_{chip} C_F(x,y) \quad (8)$$

Material removal rate at location (x,y) on a chip is obtained from mean material removal by a single asperity, R_a (equation 6) and total number of active asperities moving over that location, which can be expressed with the mean distance between asperities, D_p and relative speed between pad and wafer, V_p. (equation 9). Number of 'active' asperities, which is interacting with wafer topography, varies with nominal down pressure. It is also determined from force balance. Finally, to consider lateral pattern effect, conventional pattern density concept was integrated with the model. Effective pattern density, ρ(x, y), was evaluated using elliptic weighting function and initial topography. The evaluation window size was calibrated to fit with experimental data and fixed during time evolution. From the conventional pattern density model, the local material removal rate is inversely proportional to local effective pattern density ([1], [2]). Final form of new model integrating pad surface height distribution, effective asperity curvature, abrasive size, pattern density and material properties of the pad and wafer is given in equation 10. z(x, y) and z_{pad} was updated in each time step. The effect of nominal down pressure was implicitly integrated in the model because it affects z_{pad} in each time step.

$$n = \frac{V_p dt}{D_p} \quad (9)$$

$$MRR(x,y) = C \cdot \frac{V_p E^{*3/2} \int_{z_{pad}}^{z(x,y)} \varepsilon(x,y,\delta)^{7/4} \times PHD(\delta) d\delta}{\rho(x,y) D_p \kappa^{1/4} H_w^{3/2} R} \quad (10)$$

EXPERIMENTAL

On silicon wafer, thin (20nm) nitride was deposited and patterned to mark the oxide thickness measurement positions over a test die. There were 100 measurement sites, which were evenly distributed over a die forming 10×10 array with 800μm space between sites. Thick oxide (2.5μm) was deposited over patterned nitride and etched with 0.5μm depth with test pattern mask to create initial topography (figure 3). Figure 4 shows the test pattern, which have pattern density variation from 0% to 100% with varying space between lines and constant line width of 20μm for all line arrays in a die. Die size was 8mm × 8mm and 11 dies were formed across 100mm wafer diameter. Oxide thickness variation was measured only at the center die to avoid wafer scale variation. Initial oxide film thickness was measured at each measurement positions over the center die. Post CMP oxide thickness variations were measured after 2minutes, 4minutes and 8minutes of polishing to get the topography evolution. Table 1 summarizes the polishing condition.

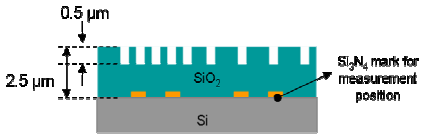

Figure 3. Cross section of the test structure

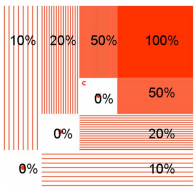

Figure 4. Test pattern

CMP machine	G&P Poly400
Pad	IC 1400 (k-groove)
Slurry	Cabot D7000
Down pressure	5 psi
Pad/wafer RPM	40/40
Slurry supply rate	100ml/min

Table 1. Experimental condition

RESULTS AND DISCUSSION

To investigate the effect of nominal down pressure on die scale topography evolution, simulation was done for varying nominal down pressures for the test pattern. Pad asperity height distribution was assumed to be normal distribution with standard deviation of 3μm and cut-off parameter, α = 6μm. Evolution of oxide thickness within the test die for 2minutes of polishing is shown in figure 5, where blue lines are oxide thickness at the lowest topography in the test die and the red lines are oxide thickness at the highest topography in the test die. Initial thickness variation in the test die was 0.5μm, same as the step height. As polishing continues, high area in the test die was polished faster than the low area, and within-die variation decreased. As down pressure increased, the initiation time for the low point polishing became faster because pad asperity deforms more and the chance for the asperities to touch the low areas in the die increases. In the simulation for 2minutes of polishing, low areas in the test die were not polished up to 3psi of down pressure. For the simulation, empirical parameters were calibrated with the experimental result of 5psi process. Figure 6 is a comparison of the within-die oxide thickness variation obtained from experiment and simulation for 8minutes of polishing. The solid lines in this plot show the model's prediction of evolution of the high and low areas of oxide

thickness for 8minutes of polishing. For comparison, experimental measurement data was plotted together as diamond dots and circles. Also shown in this plot is the model, which predicts the topographic evolution well in the time domain. 3D plots of the pattern evolution for 8minutes of CMP, comparing simulations and experimental measurements are shown in figure 7. The final oxide thickness variation over the test chip after 8minutes of polishing is shown in figure 8. The model slightly underestimated the polishing rate in the 100% pattern density area, and the RMS error calculated for 100 measurement sites over a chip was about 30nm.

CONCLUSION

A comprehensive chip scale CMP model, integrating pad asperity height distribution, pattern dependent topography, and physical parameters related to consumables and material being polished, has been developed. Model predicted lower planarization efficiency with higher down pressure because of faster low area polishing. Calibrated model well predicted the chip scale topography evolution in spatial domain and also in time domain.

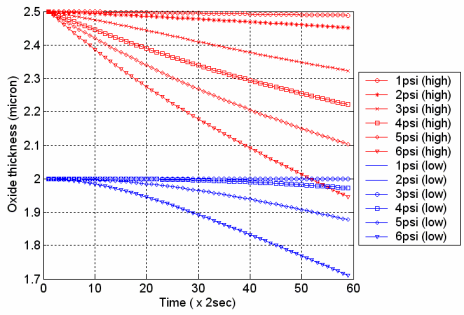

Figure 5. Pressure effect on topography evolution

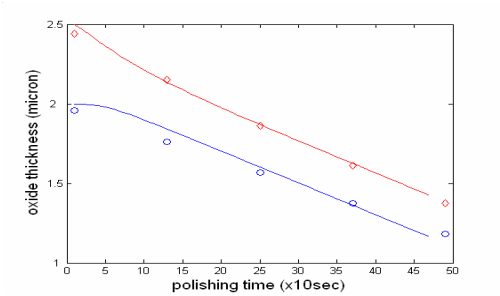

Figure 6. Model vs. experimental

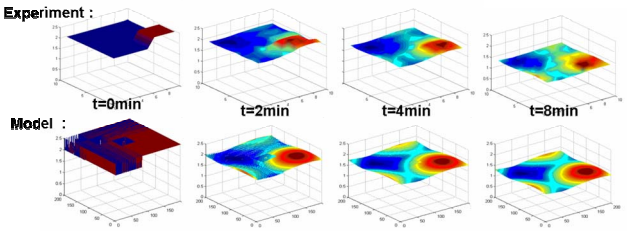

Figure 7. 3D plot of chip-scale topography evolution from experiment and simulation

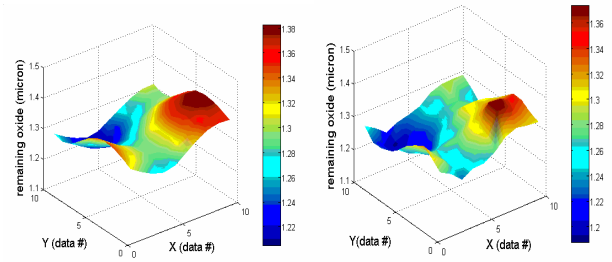

Figure 8. Oxide thickness variation after 8 minutes of polishing ((a) model prediction, (b) measured from experiment)

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