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Monolithic integration of quantum dot lasers on 300 mm silicon photonic wafers

A dissertation submitted in partial satisfaction
of the requirements for the degree

Doctor of Philosophy
in
Electrical and Computer Engineering

by

Kaiyin Feng

Committee in charge:

Professor John E. Bowers, Chair
Professor Jonathan Klamkin
Professor Nadir Dagli
Professor Chris Palmstrom

March 2024

The Dissertation of Kaiyin Feng is approved.

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March 2024

Monolithic integration of quantum dot lasers on
300 mm silicon photonic wafers

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by

Kaiyin Feng

This thesis is dedicated to my grandma Lin Zhixue.

Also to the ones who love and care.

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Curriculum Vitæ

Kaiyin Feng

Education

2024	Ph.D. in Electrical and Computer Engineering, University of California, Santa Barbara.
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Selected Journal Publications

1. **Feng, K.**, Shang, C., Hughes, E., Clark, A., Koscica, R., Ludewig, P., Harame, D. & Bowers, J. Quantum Dot Lasers Directly Grown on 300 mm Si Wafers: Planar and In-Pocket. *Photonics*. **10**, 534 (2023)
2. Shang, C., **Feng, K.**, Hughes, E., Clark, A., Debnath, M., Koscica, R., Leake, G., Herman, J., Harame, D., Ludewig, P. & Others Electrically pumped quantum-dot lasers grown on 300 mm patterned Si photonic wafers. *Light: Science & Applications*. **11**, 299 (2022)
3. **Feng, K.**, Nishimoto, M., Yu, C., Saylan, S., Taylor, R., Tanemura, T. & Nakano, Y. Waveguide-coupled metal-clad cavity with integrated feedback stub. *Japanese Journal of Applied Physics*. **56**, 082201 (2017)
4. Koscica, R., Shang, C.,**Feng, K.**, Hughes, E., Li, C., Skipper, A. & Bowers, J. Impact of Pocket Geometry on Quantum Dot Lasers Grown on Silicon Wafers. *Advanced Photonics Research*. pp. 2300317 (2023)
5. Shang, C., Hughes, E., Begley, M., Koscica, R., Fouchier, M., **Feng, K.**, He, W., Wan, Y., Leake, G., Ludewig, P. & Others Design Rules for Addressing Material Asymmetry Induced by Templated Epitaxy for Integrated Heteroepitaxial On-Chip Light Sources. *Advanced Functional Materials*. **33**, 2304645 (2023)
6. Zhang, Z., Shang, C., Norman, J., Koscica, R., **Feng, K.** & Bowers, J. Monolithic passive- Active integration of epitaxially grown quantum dot lasers on silicon. *Physica Status Solidi (a)*. **219**, 2100522 (2022)
7. Jung, D., Herrick, R., Norman, J., Turnlund, K., Jan, C., **Feng, K.**, Gossard, A. & Bowers, J. Impact of threading dislocation density on the lifetime of InAs quantum dot lasers on Si. *Applied Physics Letters*. **112** (2018)
8. Xiao, Y., Taylor, R., Yu, C., **Feng, K.**, Tanemura, T. & Nakano, Y. Room-temperature capsule-shaped wavelength-scale metal-clad laser with enhanced side mode suppression. *Applied Physics Letters*. **111** (2017)

Selected Conference Publications

1. **Feng, K.**, Koscica, R., Shang, C., Skipper, A., Netherton, A., Clark, A., Ludewig, P., Harame, D., & Bowers, J., On-chip monolithic integration of QD lasers coupled to foundry-processed SiN waveguides on 300 mm SOI wafer. Accepted by *IEEE Si Photonics Conference*. 2024.
2. **Feng, K.**, Shang, C., Hughes, E., Koscica, R., Clark, A., Debnath, M., Leake, G., Harame, D., Ludewig, P. & Bowers, J. Electrically Pumped Quantum-Dot Lasers Grown on CMOS-Compatible 300 mm Si Wafers. *2022 28th International Semiconductor Laser Conference (ISLC)*. pp. 1-2 (2022)
3. **Feng, K.**, Shang, C., Hughes, E., Koscica, R., Clark, A., Leake, G., Harame, D. & Bowers, J. Quantum-Dot Lasers Grown on CMOS-compatible 300 mm Si Photonic Wafers. *2022 Compound Semiconductor Week (CSW)*. pp. 1-2 (2022)
4. **Feng, K.**, Yu, C., Nishimoto, M., Taylor, R., Tanemura, T. & Nakano, Y. Subwavelength metallic laser coupled to silicon-on-insulator waveguide with integrated optical feedback stub for Q factor enhancement. *2016 International Semiconductor Laser Conference (ISLC)*. pp. 1-2 (2016)
5. Shang, C., **Feng, K.**, Hughes, E., Clark, A., Debnath, M., Koscica, R., Leake, G., Herman, J., Harame, D., Ludewig, P. & Others Scalable on-chip lasers grown on 300 mm Si wafers. *2023 Conference On Lasers And Electro-Optics (CLEO)*. pp. 1-2 (2023)
6. Shang, C., **Feng, K.**, Hughes, E., Clark, A., Debnath, M., Koscica, R., Leake, G., Herman, J., Harame, D., Ludewig, P. & Others Scalable and high performance monolithic on-chip light sources for integrated silicon photonics. *2023 IEEE Silicon Photonics Conference (SiPhotonics)*. pp. 1-2 (2023)

Abstract

Monolithic integration of quantum dot lasers on
300 mm silicon photonic wafers

by

Kaiyin Feng

Rapid development of the Si photonics industry and its applications in data communication calls for the making of on-chip light sources integrated on the Silicon-on-Insulator (SOI) platform for mass production. Monolithic integration of III-V lasers, especially quantum dot (QD) lasers has gained increasing attention as a key technology to realize efficient, cost-effective, industrial-scale integration of light sources for Si photonics.

In this thesis, we demonstrate for the first time, QD lasers grown and fabricated for electrically pumped lasing both on a planar template and in-pocket-template on 300 mm Si wafers. O-band edge-emitting in-pocket lasers are fabricated on Si with robust performance of continuous wave lasing up to 60 °C, a maximum double-sided output power of 124.8 mW at 20 °C and high fabrication yield. We also demonstrate for the first time, on-chip etched-facet lasers directly butt-coupled to SiN waveguides made on a 300-mm scale foundry-processed Si photonics wafer, characterized with fiber-coupling from on-chip edge couplers at waveguide output. Process developments addressing issues such as polycrystal deposition on surface, high aspect-ratio pocket geometry, and complications on growth interface affecting coupling are established.

Perspectives on scaling this QD laser process on a 300 mm scale in a Si photonics foundry is also discussed, including remaining challenges of improving laser performance and yield, and prospects on the implementation of fully monolithic integration with a III-V/Si co-processing foundry.

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Chapter 1

Introduction

1.1 Thesis objectives

The goal of this work is to establish an on-chip light source for 300-mm scale Si photonics with monolithic integration, especially for applications in data communications.

To accomplish this goal, we first established quantum-dot (QD) lasers heteroepitaxially integrated on Si at a 300 mm scale. Details for device fabrication have been revisited and meticulous process development has enabled a scalable yield and performance for technology transfer to large-scale processing facilities. This is also crucial in laying down the fundamentals in QD laser growth and fabrication from 300 mm Si wafers, and validating the QD laser epitaxial design for on-chip monolithic integration to Si photonic components on SOI wafers.

The rest of the efforts are dedicated to the establishment of the monolithic integration platform for Si photonics, through in-pocket QD heteroepitaxy growth and fabrication, for realizing in-plane butt-coupling of QD gain sections to SiN waveguides. Integrated PIC design, in-pocket laser design, in-pocket laser process development, coupling region process development, integrated device fabrication, and prototype testing were carried

out, along with efforts in sorting out unique challenges in logistics for the collaborative research project involving working closely with Si photonics foundry and PDK providers.

In this thesis, we present the first demonstration of QD lasers made from direct MBE growth on 300 mm Si wafer, the first demonstration of in-pocket QD lasers on 300 mm Si wafer, and the first demonstration of in-pocket QD lasers on 300 mm SOI wafer with direct on-chip in-plane butt-coupling to foundry-processed SiN waveguides. The lasers are designed with wavelength around 1300 nm targeting for integrated applications in data communications.

With the experiences in establishing these first demonstrations, we include our perspectives of the monolithic integration with QD heteroepitaxy and technology transfer for making III-V process at a 300 mm scale in photonic foundries, aiming to provide additional scientific resources and problem-solving guidelines for future advancement in the field.

1.2 Thesis outline

The outline of this thesis is as follows.

In Chapter 2, we provide the technology background of the development of photonic integrated circuit (PIC) technology and Si photonics, the quest for an efficient on-chip light source for Si photonics, and different integration schemes (hybrid, heterogeneous and monolithic integration). We include a brief review of the history and current state of quantum-dot (QD) lasers, and its application as a light source on Si. In the end, we provide an overview of the proposed monolithic integration scheme with in-pocket QD lasers on SOI wafers through heteroepitaxy.

Chapter 3 presents the epitaxial design, wafer preparation, fabrication development, measurement results and discussions for the first demonstration of QD lasers made from

direct MBE growth on 300 mm Si wafer.

Chapter 4 presents the first demonstration of in-pocket QD lasers on 300 mm Si wafer, including the integration design, wafer preparation, fabrication development including polycrystal removal and methods to address the high aspect-ratio narrow pocket geometry, followed by laser measurement results and discussions.

Chapter 5 presents the first demonstration of in-pocket QD lasers on 300 mm SOI wafer with direct on-chip in-plane butt-coupling to foundry-processed SiN waveguides. This includes (1) the demonstration of concept with a FIB-facet laser, (2) process development of an additional facet etch and the first demonstration of on-chip in-pocket etched-facet lasers, (3) investigations of the coupling region, additional process development to address the issues, improved integration design and fabrication and the first demonstration of on-chip etched-facet laser coupled to foundry-processed SiN waveguides from a 300 mm SOI wafer. Measurement results and discussions are included in each part, and process development details with discussions are included as some of the concepts can be extended to alternative platforms and for different processing facilities.

Chapter 6 takes on the perspectives on scaling QD laser process on a 300 mm scale with Si Photonics foundry process. We start with a review of the project this thesis based on, and the generations of integration design and wafer processing. Following that, we present discussions on our studies in improving the in-pocket QD quality from a growth aspect. We then discuss about the main challenge of improving coupling efficiency, including theoretical studies of the coupling configuration, proposed methods for improving coupling efficiency, and results of some development on the proposed methods, BCB gap-fill and MBE partial selective growth. Suggestions for future experiments are also included. In the end, we include our comments on the remaining challenges for yield and scaling, followed by a comprehensive review on the development in measurement technology on 300 mm scale for a shorter development cycle.

Finally, we will provide a brief summary and outlook of the thesis in Chapter 7.

The appendix section includes detailed step-by-step processing procedures for making electrically-injected in-pocket ridge-waveguide QD lasers monolithically integrated on SOI wafer with in-plane butt-coupling to SiN waveguides. This will be particularly useful for reproducing the results in Chapter 3-5 at UCSB Nanofab, and hopefully will also be informative as a remote reference for other semiconductor process developments. The procedures of the BCB gap-fill process and edge-coupling trench etching process and some additional resources are also provided.

Chapter 2

Monolithic integration for Si photonics through heteroepitaxy

2.1 Growth and scaling of Si photonics

Photonic integrated circuit (PIC) technology involves making integrated circuits with the use of photons to detect, process and transmit information more efficiently than electrical signals, as an optical analog to the concept of integrated circuit (IC) for electronic devices[1].

Complementary metal-oxide semiconductor (CMOS) technology is central for the evolution and scaling of IC electronic devices with high integration density and integrated manufacture capability enabled by the invention of metal-oxide semiconductor field-effect transistors (MOSFETs) as the functional building blocks of integrated circuits and the development of multi-layer semiconductor processing on silicon wafers including substrate preparation, oxide growth, photolithography, etching, doping, deposition, planarization, annealing, testing, packaging etc.

The field of Si photonics envisions using Si as the substrate and fundamental medium

for making PICs. This approach leverages existing CMOS technology to scale and streamline the production of functional optoelectronic devices with compact footprint and integration density akin to ICs [2], but providing the unique benefit of versatile functionality from directly manipulating light (photons). Si photonics has opened up a wide range of applications from communication transceivers for data centers, to sensors including light detection and ranging (LiDAR), gyroscopes, biosensors, and spectrometers [3].

Compared to alternative III-V PICs such as GaAs or InP based platforms, Si photonics has grown rapidly, taking advantages of the large-scale manufacturing capability of CMOS technology with the added edge of silicon wafer as a low-cost raw material. Since the revolutionary first-demonstration of low-loss, single-mode light guiding at 1.3 µm and 1.5 µm with Si waveguides on the silicon-on-insulator (SOI) platform[4], Si photonics has advanced quickly from the demonstration of individual functional components on Si [5, 6, 7] and small-scale integration (SSI) era of 1 - 10 components per chip in the early 2000s towards the start of large-scale integartion (LSI) era with 500 - 10,000 components per chip nowadays, within just the past two decades [2]. The CMOS platform has also advanced with the incorporation of versatile materials and processes in foundries, facilitating the making of a range of functional optoelectronic devices [2], such as Ge for high-speed photodetectors [8, 9], and SiN for ultra low-loss waveguides and compatibility with high optical power[10, 11].

In particular, Si photonics has emerged as the primary solution in the quest for low-cost, highly energy-efficient optical transceivers for data center interconnects. This pursuit is driven by the global surge in digital economy and the exponentially growing demand for data analysis, storage and communications [3]. With the growing demand, there are established Si photonics foundries now offering fabrication services such as multi-project wafer (MPW) service, customized process and volume production, some carrying large-scale manufacturing capability up to 300 mm wafer diameter scale with

the SOI platform [12]. This development has fostered an ecosystem of available processing technology, design tools, and testing and packaging solutions [13]. For an MPW service, for example, basic components of Si photonics PICs can be provided to external users/designers/fabless companies in the form of process-design-kits (PDKs), with device libraries including different waveguides and couplers, as well as functional high speed switches, microdisk modulators, and photodetectors etc. An overview of such state-of-art MPW technology can be found in [14].

2.2 Light source for Si photonics

With two decades of rapid development, the established Si photonics SOI platform is capable of producing large-scale functional PICs using Si and Si-based materials as efficient media for the transmission, modulation and detection of light[15]. However, the nature of Si being a Group IV semiconductor with indirect band gap makes it challenging to be utilized as a gain medium for efficient light emission. Since the first demonstrations of semiconductor diode lasers (GaAs-based) in 1962 [16, 17], the material systems for making compound semiconductor diode lasers have been dominantly GaAs-, InP- and GaN- based materials, all direct band gap III-V compound semiconductors[18].

Despite research efforts on engineering Si, Ge or GeSn alloys for enhanced light emissions, the mainstream solution of light source for Si photonics has been the integration of mature III-V light sources on Si in various schemes. Figure 2.1 illustrates three general categories of integration methods: hybrid integration through co-packaging, heterogeneous integration through wafer bonding or micro-transfer-printing, and monolithic integration through heteroepitaxy.

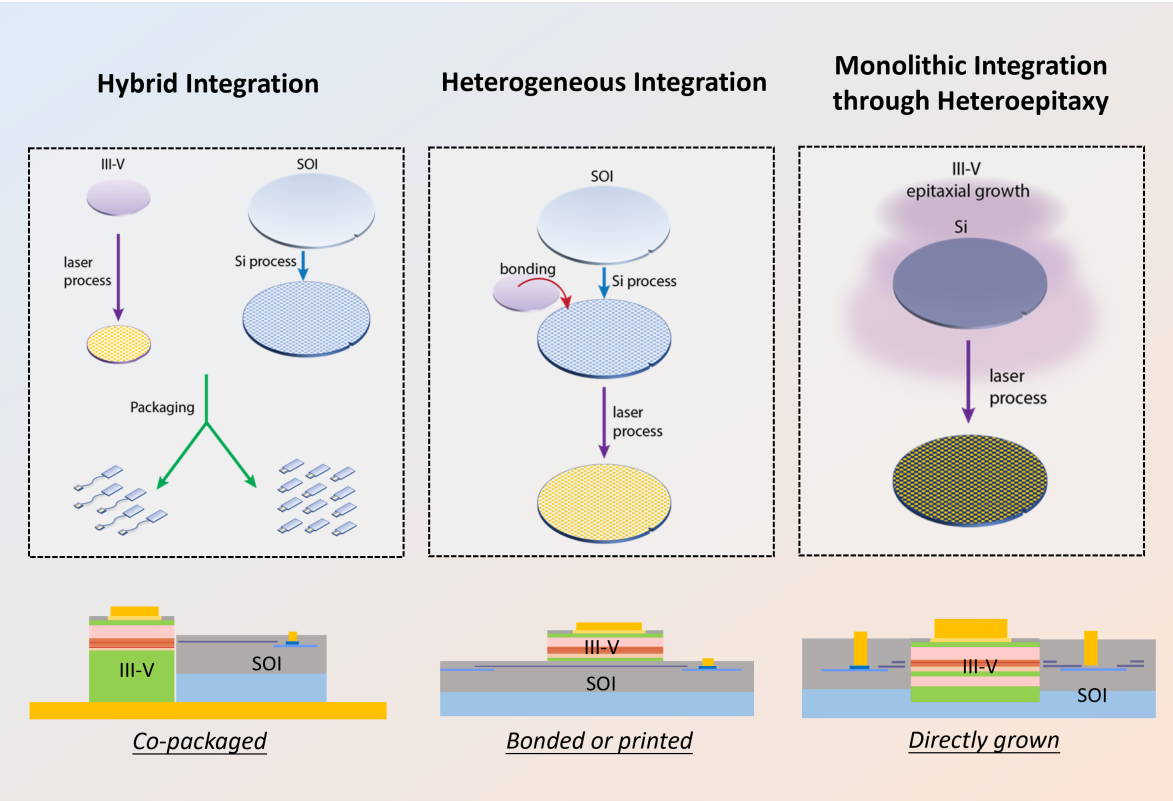

Figure 2.1: Integration schemes of III-V light sources for Si photonics. Illustrations adapted from [19, 20].

Recent reviews of the different laser integration techniques can be found in [2, 15].

"Hybrid integration" refers to copackaging the laser and other components after they are manufactured on native substrate (InP and Si, for example) and pre-screened for good performance. Common techniques include epoxy attachment, ball-lens, isolator, flip-chip bonding etc. This method is widely commercially available; though limited by factors such as large device footprint, high manufacturing cost and low scalability, it enables high quality components fabricated from native substrates and the complete PICs with high functionality. An example of recent demonstration of 1.6 Tbps Si photonics transmitter (Tx) IC can be found at [21].

"Heterogeneous integration" generally refers to the process of bonding III-V wafers

to silicon wafers, followed by substrate removal, and then co-processing the lasers on the silicon wafer with III-V thin film integrated on top. This enables full photonic functionality on a single chip on Si substrate. This technology, first demonstrated in UCSB in 2006 [22], has been successfully commercialized within the past two decades. III-V gain materials are usually evanescently coupled to Si-based waveguides, and the very low-loss transition from III-V to Si-based circuits has enabled the production of highly functional integrated lasers, such as tunable lasers, ultra-low-noise lasers, and comb sources. Recent comprehensive reviews and tutorials of this technology can be found in [23, 24, 25, 26, 27].

In addition, micro-transfer-printing technology is an emerging technology, where releasable coupons are prepared in a grid and then selectively transfered from the ative III-V substrate to target silicon wafers using a structured polydimethylsiloxane (PDMS) stamp, and the coupons can be either gain material itself or finished functional III-V devices [28]. It applies to versatile on-chip integration schemes, some in a butt-coupling configuration closer to the "hybrid" approach [29] and some using evanescent coupling and should be better categorized as "heterogeneous" integration, such as [30, 31]. An excellent recent review of this technology can be found in [32].

"Monolithic integration" needs a bit more clarification here. "Monolithic" originally means simply "a single stone" from the dictionary, from the French word "monolithe". [1] There are a few integration schemes that can be considered as "monolithic": (a) fully III-V based functional PICs including laser sources on one single chip on the same III-V substrate, such as InP PICs [34], (b) direct growth of III-V crystal on Si and making fully III-V based functional PICs on one single chip on Si substrate, (c) direct growth of

[1] The word "monolith" comes from French word "monolithe", originated from Latin monolithus, or Greek monolithos, constructed by "mon-" + "lithos" (stone), meaning consisting of a single stone. "Monolithic integration" generally refers to integration on a single cyrstal, or from a single piece of chip.[33]

III-V components on to patterned Si photonics wafers, such as SOI wafers, via selective or non-selective growth, and processed on Si wafer as III-V/Si integrated functional PICs, often with direct in-plane butt-coupling. Here in the context of Si photonics, we mainly use the term for scenarios (b) and (c), and to clarify the concept we name the approach "monolithic integration through heteroepitaxy", where "heteroepitaxy" refers to the direct growth of III-V on Si. This approach, generally enabled by the development of defect-tolerant quantum dots as active layer for lasers and amplifiers, is promising for the direct manufacturing of highly compact, scalable and efficient PICs with high reliability and low cost. Some recent reviews can be found in [35, 36, 37].

Integration	Conventional (Laser-isolator-fiber-PIC)	Hybrid 2.5D (FSO)	Hybrid 2.5D (PWB)	Hybrid 3D (flip chip/ transfer printing)	Heterogenous (Direct bonding/ transfer printing)	Monolithic (Hetero-epitaxy)
Coupling Loss	>2dB	>2dB	>2dB	1dB	1dB	few dB
Output Power	High	High	High	Medium	Medium	Low
Pol. Ctrl. or PMF	Needed	Needed	No Need	No Need	No Need	No Need
Thermal Management	Easy	Easy	Easy	Medium-Difficult	Difficult	Medium
Linewidth Reduction	N/A	Good	Good	Good	Best	Good
Assembly Size	Large	Medium	Medium	Small	Smallest	Smallest
Uses PIC Area	No	No	No	Yes	Yes	Yes
Cost	Laser assembly, packaging, coupling	Laser die, packaging, coupling	Laser die, packaging, coupling	Laser die, packaging, coupling	Low for high volume	Low for high volume, no III-V substrate
Test	Die	Die Wafer	Die Wafer	Die Wafer	Wafer	Wafer
Packaging Style	Known -good parts	Known -good parts	Known -good parts	Known -good parts	all-or-nothing if no redundancy	all-or-nothing if no redundancy
Suitability for applications	Bespoke (apps, λs), Low volume	Bespoke (apps, λs)	Bespoke (apps, λs)	Bespoke (apps, λs)	High volume (R&D)	High volume (significant R&D)

Figure 2.2: Comparing different techniques to attach a laser to a silicon PIC in power, performance (as of 2023) and area (PPA) metrics, cost, testing, packaging style, and suitability for applications Perspective. Reproduced from [2] ©Nature https://doi.org/10.1038/s41467-024-44750-0.

Figure 2.2 is a comparison of the three different techniques in terms of cost, testing, packaging style and suitability for applications, reproduced from a table in the review [2]. The monolithic integration approach, compared with other options, provides the potential for smaller per-chip cost if produced in large volume, and is compatible for wafer-scale integration design and testing.

In the next section, we will provide a deeper review of the background of quantum-dot (QD) lasers, and an overview of the monolithic integration through QD heteroepitaxy

that is the core pursuit of this thesis.

2.3 Monolithic integration through QD heteroepitaxy

2.3.1 Development of Quantum Dot Lasers

The Nobel Prize in Chemistry 2023 was awarded to Moungi G. Bawendi, Louis E. Brus and Aleksey Yekimov "for the discovery and development of quantum dots" [38]. Quantum dots are particle-like materials entering the regime of quantum phenomena with their nano-scale size where, as a result, their properties become directly linked to the particle sizes and shapes. In other words, for quantum dots synthesized with the same material compositions, their properties can be engineered by controlling the particle size in favor of specific applications.

Using semiconductor quantum dots as active gain media for lasers was first proposed by A. Arakawa and H. Sakaki in 1982, where the concept of "multidimensional quantum-well" with higher dimensional quantum confinement in the active region of a semiconductor laser than that of conventional lasers predicts lower temperature sensitivity of threshold current from the reduced dimensionality of electronic state [39]. Quantum dot laser was first demonstrated in 1994 by N. Kirstaedter *et al.* with nano-scale 3D clusters of $In_{0.5}Ga_{0.5}As$ formation on GaAs (100) surface from strain-induced transformation of the pseudomorphic layers with molecular beam epitaxy (MBE) [40]. In 1995, Mirin *et al.* demonstrated room-temperature photoluminescence at 1.32 µm from InGaAs quantum dots grown with Stranski-Krastanow growth mode in MBE, with atomic force microscopy (AFM) micrographs showing dot density of $2 - 3 \times 10^{10}$ dots/cm^2, which indicates the possibility of fabricating 1.3 µm lasers on GaAs substrates.

In the years thereafter, In(Ga)As grown lattice matched to (001) GaAs or InP has become the most well-developed quantum dot materials system for semiconductor lasers, especially with its flexibility to obtain luminescence at wavelengths between 1 µm to 1.8 µm for applications in the field of telecommunications and data communication [41]. Many advantages from using quantum dot as the gain media for semiconductor lasers have been demonstrated [41, 42], such as lower threshold currents [43, 44], better high-temperature performance [45, 46, 47], improved stability against optical feedback [48], ultrafast gain dynamics [36, 49, 50] and a few more. Commercialization of quantum-dot lasers in the telecommunication industry follows the rapid advancement of these studies, and the first mass-production line of QD lasers came out in 2009 from QD Laser, Inc., a company in Japan, being featured among their lines of different semiconductor laser products [37, 51]. Up to now, Quantum-dot Fabry-Perot lasers operating at 1300 nm up to 175 °C, quantum-dot distributed-feedback (DFB) lasers, gain chip and epitaxial wafers are commercially available from QD Laser, Inc [52]. More recently, Quintessent Inc., a start-up company in Santa Barbara, California, has also been developing quantum-dot based lasers and optical amplifiers for Silicon integrated photonics in partnership with Tower Semiconductor, a leading semiconductor foundry [53, 54]. Such development shows a state of maturity of the quantum dot technology as well as its ongoing potential for many applications, especially in integrated photonics and its innovative solution to optical connectivities in telecommunications, large-scale computations and artifical-intelligence applications.

Coming back to the scope of interest in this thesis, there is one specific advantage of quantum dots that is particularly important for the afore-described monolithic integration scheme for Si photonics. Quantum-dot (QD) as the laser active region, compared to quantum-wells (QW), provides much increased tolerance to crystalline defects due to the efficient capture and confinement of injected carriers by the individual dots that enables

reduced nonradiative recombination at defects or dislocations [35, 36, 37, 55, 56, 57]. In other words, given the same heteroepitaxially grown material on Si with a certain threading dislocation density, while it is challenging to make practical QW lasers [58], it can be much easier and more feasible to make high performance lasers just from switching to QD as the active region [59]. Direct comparison of InGaAs quantum well lasers on Silicon versus InAs quantum dot lasers on Silicon was conducted in 2015 by A. Liu *et al.*, showing that quantum dot active region gives better photoluminescence results and improved lasing characteristics with ridge waveguide lasers made with the identical fabrication procedure as the quantum-well counterparts when grown directly on Si through heteroepitaxy[35]. In 2019, Z. Liu *et al.* also demonstrates experimentally devices with QD active regions showing lasing up to higher dislocation densities than those with QW active regions, as well as provides a theoretical explanation of how it benefits from the ultrafast carrier capture from quantum dots and high thermal energy barriers preventing the carriers from migrating into defect states [59].

Such property makes quantum-dot the most suitable, if not almost the only practical, candidate of monolithic integration of lasers for silicon photonics through heteroepitaxy [35, 36]. Since the first demonstration of 1.3 µm quantum dot lasers epitaxially grown on Silicon in 2011 [60], there has been a series of efforts to improve device performance and reliability through a combination of different techniques [37, 61, 62, 63]. In 2021, C. Shang and E. Hughes *et al.* demonstrated 1.3 µm InAs quantum-dot lasers directly grown on CMOS-compatible on-axis Si (001) substrate with the hero device showing minimum degradation after more than 1200 hours of constant current stress at 80 °C [64], following several generations of development [63, 65] including (1) using GaP/Si templates to remove antiphase domains (APDs) at the interface of III-V to Si [66, 67, 68, 69]; (2) using thermal cyclic annealing (TCA) to glide-annihilate dislocations during buffer growth [70] and (3) using strained layer superlattice (SLS) as the dislocation

filter layers (DFLs) to reduce the threading dislocation density (TDD)[69, 71, 72]; (4) using p-type modulation doping to supply extra holes in the active region to improve high temperature performance and lifetime [73, 74]; (5) using strained quantum-wells as trapping layers (TLs) to displace misfit dislocations (MDs) away from the active region during the dislocation migration happening from the post-growth cooldown due to mismatch of coefficient of thermal expansion (CTE) in the III-V and Si materials [75, 76]; and more recently (6) using asymmetric graded filter (ASG) structures instead of the traditional SLS for better relaxation of the DFL to further lower the surface TDD [77].

Given the marvelous research work that pushed forward the field of heteroepitaxial integration of quantum dot lasers directly grown on Si in the past decades, it is challenging to include all relevant references and list out alternatives approaches and their achievements in material quality and device performance here. The previous paragraph points out a few selected works, and hopefully have made the point of the promises of quantum dot lasers on Si. To readers that are interested, the review papers cited [35, 36, 37, 41, 62, 63, 65] and a few more general discussions on the broader topic of on-chip light sources on Si [15, 78, 79] can be of some assistance to dig deeper.

2.3.2 Monolithic integration of QD lasers on 300 mm silicon photonic wafers

Brief review of the remaining challenges and previous works

With the unprecedented rapid development of QD lasers for heteroepitaxy on silicon wafers, the efforts are pushed forward in two main directions:

- scaling up the production of QD lasers on Si wafers;

- coupling of directly-grown QD lasers with Si photonics components on the same chip for fully integrated functional PICs.

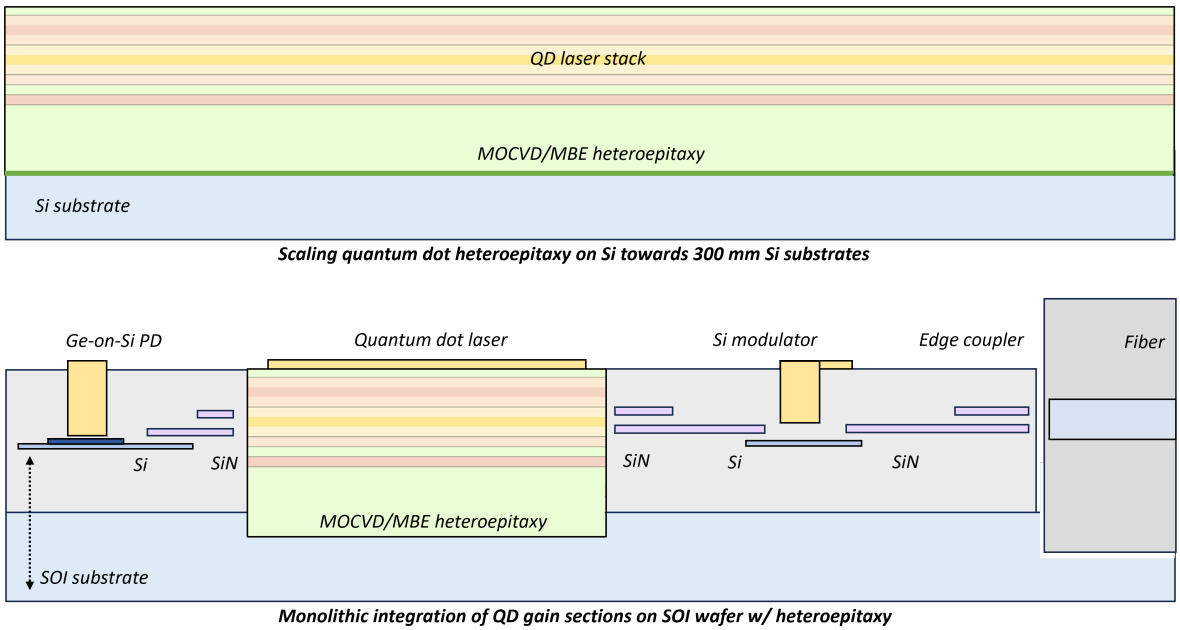

Figure 2.3: Vision of the monolithic integration platform: schematic of wafer cross–sections and top-views of (1) scaling QD heteroepitaxy and laser production towards 300 mm scale Si substrates, and (2) coupling of QD gain section with Si-based components on SOI wafer, potentially also at 300 mm scale.

In terms of scaling, the lower cost of Si substrate and larger available diameter than III-V substrates makes growing QD lasers and other III-V based materials on Si a more economical choice. Table 2.1 compares the typical diameter and estimated cost of common semiconductor substrates[2]. In the example of producing InGaAs/InAs QD lasers at 1.3 µm wavelength for datacom applications, the cost per unit area of the substrate will be eight times cheaper with a Si substrate compared to GaAs substrate, while in comparison, traditional hybrid integration with native substrates or heterogeneous integration both still require the use of smaller, expensive III-V wafers[3]. With APD-free GaP on Si substrate commercially available at 300 mm [81], it is valuable to experiment with 300 mm scale MBE growth to produce QD lasers and evaluate the device performance, yet no such demonstration had been done yet prior to this thesis.

Substrate sizes and costs				
Substrate	GaAs	InP	SOI	Si
Typical diameter (mm)	150	150	300	450
Estimated cost ($/cm^2)	1.65	4.55	1.3	0.2

Table 2.1: Common semiconductor wafer sizes and costs. Adapted from [82]

In terms of the pursuit of coupling between III-V and Si with heteroepitaxy platforms, there has also been considerable active research with both metalorganic chemical vapor deposition (MOCVD) and molecular-beam epitaxy (MBE) approaches. For example, optically pumped nano-ridge lasers on 300 mm Si wafer [83], selective-growth of InGaAsP quantum well (QW) structures on v-groove SOI wafer [84], selective-area-heteroepitaxy of APB-free GaAs microridges in-pocket on Si were demonstrated [85]. There have also been demonstrations of selective growth of GaAs/AlGaAs waveguides with MOCVD in-pocket

[2]Original source dated in 2018. Si substrate size updated from "300 mm" to "450 mm".

[3]As an example of the exceptions, recent technology has showcased the possibility of reusing the InP substrate after bonding. Utilizing smart-cut technology, InP-on-Si (InPOSi) templates can be produced at up to 200 mm size, see [80].

with efficient optical couplings (-2.5 dB loss/transition) [86]. However, heteroepitaxy of practical lasers on SOI wafer with on-chip coupling with Si photonic components remains a challenge.

Brief review of concurrent research during the formation of this thesis

Some works were conducted concurrently with the research presented in this thesis spanning 2020 - 2024, and were published around the same time or shortly after our results.

Our collaborators at UCSB have demonstrated MOCVD growth of optically-pumped microdisk QW lasers in-pocket in 2022 [87] and QD lasers at 1.3 µm on blanket v-groove Si in 2023 [88], yet no in-pocket QD growth, in-pocket electrically pumped laser, or coupling to Si waveguides have been demonstrated with this approach yet. An alternative MOCVD approach using selective growth in a lateral configuration by Y. Xue *et al.* has shown III-V photodetectors selectively grown with in-plane butt-coupling to Si waveguide on SOI wafer in 2022 [89]. Optically pumped DFB lasers demostrated with lateral selective growth in a similar approach on SOI wafer very recently in 2024 [90], but coupling is yet to be shown.

In 2022 - 2023, W. Wei *et al.* has demonstrated MBE-grown QD lasers directly grown on trenched SOI substrate with butt-coupled silicon waveguides [91], with an in-plane monolithic integration platform similar to ours. The work was first published on arXiv in July 2022, quickly following ours (mostly covering results from Chapter 4, online on arXiv in June 2022) [92], and later on the same journal *Light: Science & Applications*. Their successful demonstration of on-chip laser-to-waveguide coupling through monolithic integration, albeit on a smaller scale and not from foundry-processed wafers, preceded our results in Chapter 5. Another MBE demonstration with mid-IR GaSb-based diode laser directly grown with MBE on a pre-patterned Si photonics wafer with in-plane butt-

coupling to SiN waveguides on 4-inch Si wafer were published on the same journal in June 2023 [93].

The concurrent advancements in research underscore the dynamic pursuit in the field of monolithic integration for Si photonics through heteroepitaxy. Through a diverse collections of growth methodologies, wafer scales, coupling configurations, and demonstrated outcomes, the reviewed works have been inspiring and stimulating to our own endeavors, and we invite readers to explore the works further if interested.

Proposed works on monolithic integration platform with QD heteroepitaxy on 300 mm scale

This thesis aims to advance QD lasers for Si photonics in the two aforementioned key directions of "scaling" and "coupling". The first part of the work demonstrates the production of QD laser on Si wafers on 300 mm scale. The remaining parts delve into the design, growth, implementation, fabrication and testing processes of the proposed monolithic integration platform with QD laser heteroepitaxy for Si photonics, and present the first demonstration of directly grown QD lasers coupled to Si photonics components on the same chip from a foundry-processed 300 mm SOI wafer.

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Chapter 3

QD lasers directly grown and fabricated on 300 mm Si wafers

3.1 Introduction

In this chapter, we present our work to scale quantum dot (QD) laser heteroepitaxy on Si towards 300 mm Si substrates. Wafer preparation, QD growth with molecular-beam epitaxy (MBE) at 300 mm scale and subsequent wafer characterizations will be included. Then, we will present critical improvements in the ridge-waveguide laser fabrication process for improving device performance and yield, and eliminating some previously known issues. Comprehensive design guidelines for best practice of layer dimension and clearance for making these devices will be provided, in an effort to lay down the groundwork for technology transfer to enable QD laser fabrication on a 300 mm scale. We will include device fabrication and measurement results, evaluations of the performance, distribution and yield on the results, and provide a comprehensive summary.

The work in this chapter also introduces a "thin" QD stack design with mesa etch depth of 1885 nm, in contrast to the original 3551 nm in our "standard" design as de-

scribed in previous publications on QD lasers grown and fabricated on Si. This serves as a validation run for QD material stack design and devices performance, as the introduction of "thin" stack is intended to facilitate its transfer to the monolithic integration platform in a "in-pocket" configuration for on-chip in-plane butt-coupling with SiN waveguides on SOI wafers, a topic that will be covered in the remaining chapters.

3.2 300 mm QD laser on Si wafer preparation

3.2.1 QD laser epitaxial stack optimization for direct monolithic integration

The QD laser epitaxial stack is designed as graded index separate confinement heterostructure (GRINSCH) composed of AlGaAs layers as top and bottom cladding, and an active region formed by multiple layers of InAs quantum dots embedded in $In_{0.15}Ga_{0.85}As$ quantum well with p-modulation doped GaAs barriers. Most of the previous demonstrations of QD lasers grown on Si in the past decade [1, 2, 3, 4, 5] have adopted structures with $Al_{0.4}Ga_{0.6}As$ top and bottom claddings of about 1.4 µm each, similar to that shown on the left of Table 3.1. The design includes an active region containing 5 layers of InAs QDs in about 9 nm $In_{0.15}Ga_{0.85}As$ quantum well and 37.5 nm GaAs barriers. With top and bottom UID 50 nm GaAs surrounding the multi-layer dots-in-a-well (DWELL) structure, the core waveguide thickness is about 295 nm, and total stack thickness over 4 µm.

The QD epitaxial stack proposed for 300 mm growth in this project, is adjusted to a thinner overall stack thickness, as shown on the right of Table 3.1, sometimes mentioned as the "70%", "asymmetric" or "thin" stack. The cladding composition is adjusted to be $Al_{0.7}Ga_{0.3}As$, with the higher aluminum content lowering the refractive index of the layer

to approximately 3.0887 compared to that of $Al_{0.4}Ga_{0.6}As$ being 3.2483. Correspondingly, the top cladding thickness is adjusted to be 400 nm with 50 nm of grading layers above and below. The lower cladding is adjusted to be 400 nm of $Al_{0.2}Ga_{0.8}As$ above the 300-nm thin n-contact layer, with an additional 700 nm of $Al_{0.7}Ga_{0.3}As$ bottom cladding located beneath n-contact layer for mode confinement. The top and bottom GaAs around the 5 layers of DWELL structure is also thickened to 250 nm for an increased overall core waveguide thickness of 685 nm.

"standard" stack	"70% asymmetric thin" stack
p+ GaAs 300 nm	p+ GaAs 300 nm
p-AlGaAs grading layers 50 nm	p-AlGaAs grading layers 50 nm
p-$Al_{0.4}Ga_{0.6}As$ 1405 nm	p-$Al_{0.7}Ga_{0.3}As$ 400 nm
p-AlGaAs grading layers 50 nm	p-AlGaAs grading layers 50 nm
UID GaAs 12.5 nm	UID GaAs 212.5 nm
QD in QW (37.5 + 9)×5 nm	QD in QW (37.5 + 7)×5 nm
UID GaAs 50 nm	UID GaAs 250 nm
n-AlGaAs grading layers 50 nm	n-$Al_{0.2}Ga_{0.8}As$ 400 nm
n-$Al_{0.4}Ga_{0.6}As$ 1400 nm	n-GaAs 300 nm
n-AlGaAs grading layers 50 nm	$Al_{0.7}Ga_{0.3}As$ 700 nm
n-GaAs buffer 500 nm n-GaAs ∼ 2000 nm	dislocation filters GaAs buffer
dislocation filters GaAs buffer	Si substrate
Si substrate	

Table 3.1: Schematics of QD laser epitaxial stacks.

The demonstration of 300 mm QD growth is independent of choosing either the "standard" stack or the "70% asymmetric thin" stack, and both should be able to yield high performance QD lasers with narrow ridge waveguide, two-step etch waveguide or

broad area laser design. The reason for choosing the thin stack in this project is partially to use the wafer as a tool for validating growth conditions and QD laser performance towards the monolithic integration platform with in-plane SiN waveguide coupling, where the QD laser mode is intended to align with the waveguide mode vertically for on-chip butt-coupling, and the overall stack thickness needs to be compatible of the limit for the oxide pocket and silicon recess depth in the Si photonic foundry fabrication. More details of this configuration will be introduced in the subsequent discussions of Chapter 4 and Chapter 5. It is also considered as an effort to explore thinner stack's potentially reduced tendency of cracking when growing on Si [6].

Theoretical analysis is conducted using Lumerical MODE to compare the mode profile of the two QD epitaxial layer designs. The results of power intensity distribution are shown in the Figure 3.1 below with a deeply etched configuration (one-step etch stopping at top of n-GaAs contact). The simulated structure contains the etched mesa with a surrounding oxide passivation layer, and the metal contacts and probes shown in the illustration are not included. The mesa width is set to be 3 µm, and both designs operate as multi-mode ridge waveguide lasers. The numbers in the figure indicate simulated results from the fundamental transverse electric (TE) mode of both cases. Confinement factor is computed as the fraction of optical power within the 5 dots-in-a-well (DWELL) layers compared to the total power. Power intensities across height along center line of mesa ($x = 0\mu m$) are extracted and normalized in the plots below, where red dashed lines indicates boundaries of the active region.

The simulation results show good mode confinement in both designs, with a lower confinement factor in the "thin" stack (0.0577) compared to that of the"standard" stack (0.0786) . This can also be inferred from the mode image, as the "thin" stack exhibits a more rounded mode shape from the asymmetric layer design and higher index contrast from the top cladding than the lower cladding. Quantitative comparison is shown in the

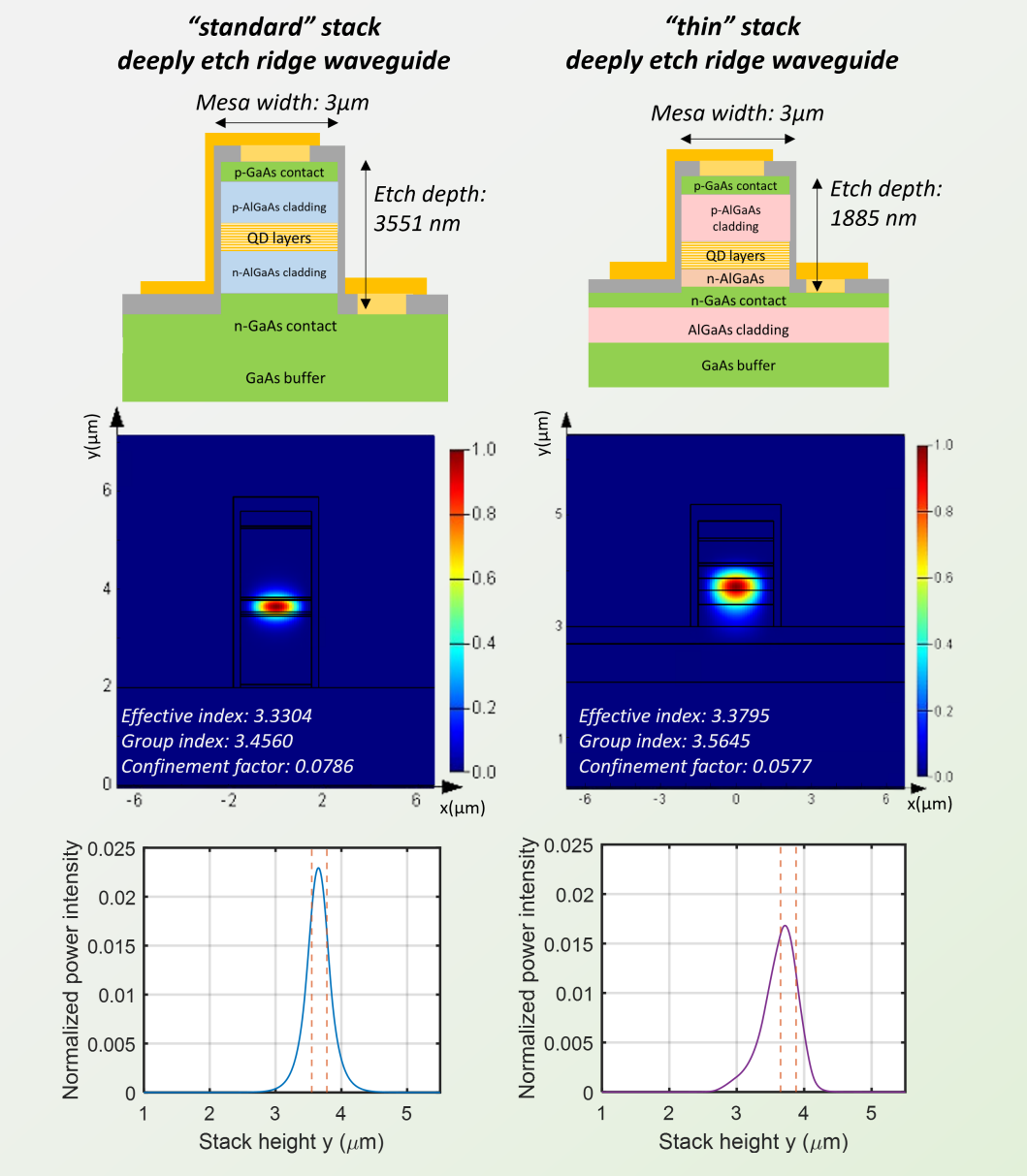


Figure 3.1: Comparison of the "standard" and "thin" stack cross-sections.

normalized line plots of power intensity versus height (bottom to top) at $x = 0\mu m$. In the case of deeply etched ridge waveguide cavity, leakage into the bottom GaAs buffer is not a concern. Further discussions of the on-chip butt-coupling configuration with SiN waveguide couplers and simulations of the coupling region will be included in Chapter 5

and Chapter 6.

3.2.2 300 mm Si template preparation and MBE direct growth

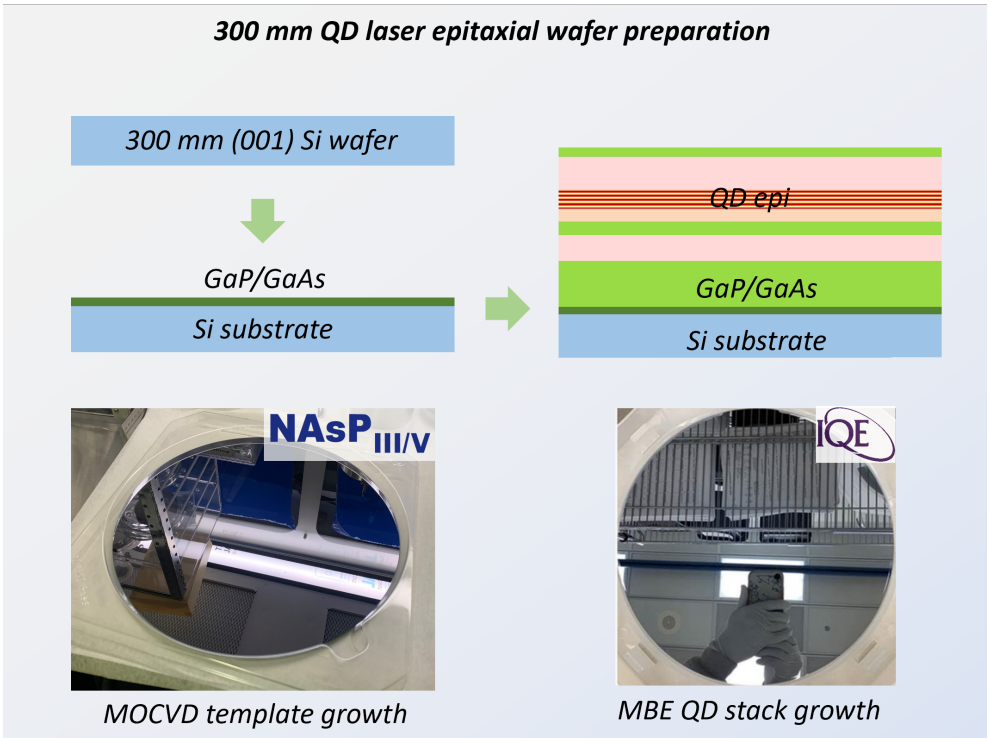


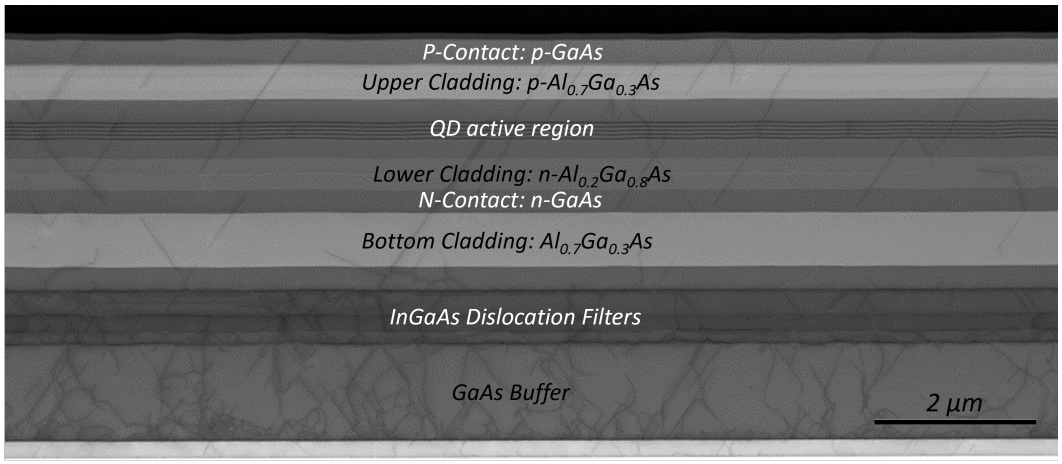
Figure 3.2: Preparation of 300 mm QD laser epitaxial wafer.

Figure 3.2 shows the preparation of QD epitaxial layers on Si. The wafer preparation started with a 300 mm CMOS-compatible (001) Si wafer. The template was prepared by $NAsP_{III-V}$ GmbH growing GaP and GaAs initial layers on on-axis Si using MOCVD [7, 8], with a thickness of 200 nm GaP and 500 nm GaAs. Such template is commercially available and is considered to be free of dislocations, stacking faults and twins and presents an anti-phase domain (APD) free surface [9]. With the MOCVD template, the GaAs buffer layers followed by complete QD laser stack was grown at IQE, Inc. in a 300 mm MBE reactor. The initial 100 nm GaAs nucleation layer was grown at 500 °C, then

1.5 µm of GaAs grown at 580 °C. Asymmetric graded filter layers were then applied for defect reduction to complete the buffer structure [10]. The QD laser stack with trapping layers [5] were subsequently grown on top of the buffer, with the "70% asymmetric thin" stack shown previously in the table. Examples of the top view of the 300 mm wafers after MOCVD template and after MBE growth are also shown in the figure.

3.2.3 Wafer characterizations

The wafer is then cleaved into smaller pieces at UCSB for characterization and for QD laser device processing. Figure 3.3 shows cross-section scanning transmission electron microscopy (STEM) prepared from a cleaved-out piece of the 300 mm QD epitaxial wafer. Critical layer compositions are marked on the image. We estimate the threading-dislocation density (TDD) in the active region to be around 1.5×10^8 cm^{-2} measured by TEM.



Credit: Eamonn Hughes

Figure 3.3: Cross-section STEM of the QD laser stack with critical layer compositions marked on the image. Credit: Eamonn Hughes, from [11]. ©MDPI 2023.

We measured photo luminescence (PL) of the wafer with a pump laser wavelength of

785 nm to compare variations of QD growth quality across the wafer. Data was taken from different cleaved pieces from the wafer, with different distance to wafer center or edge, and from different sides of the wafer. Figure 3.4 shows four PL characterization results from the same pumping level and from four different pieces that are representative for the observed quality of the MBE QD growth and its variation across the 300 mm wafer.

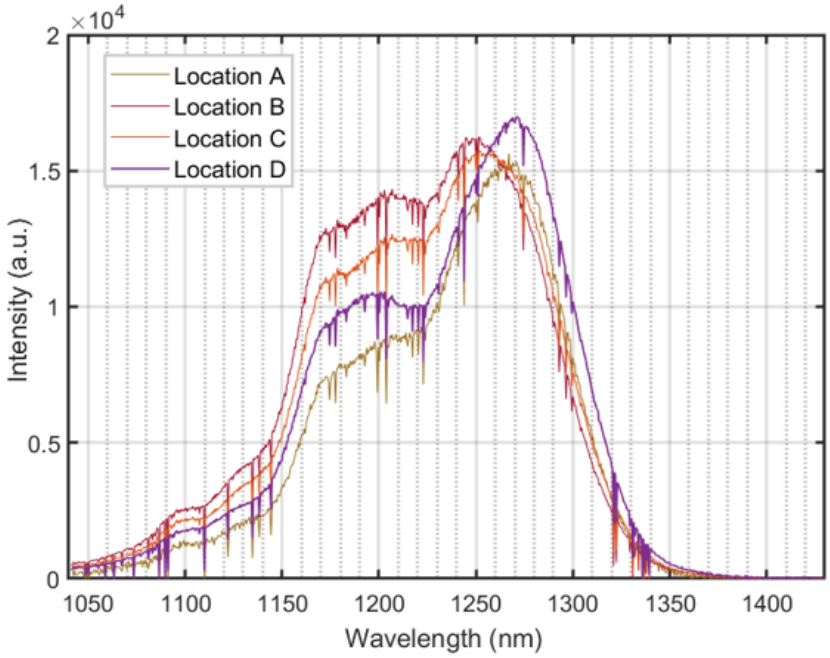


Figure 3.4: PL characterizations of four locations across the 300 mm wafer. From [11]. ©MDPI 2023.

The QD ground state PL peak wavelength is around 1260 - 1280 nm, with a variation up to 25 - 30 nm and slight discrepancy in the intensity and its separation from the excited states as well. Despite that, there is consistency in the wavelengths and the general composition of PL profile across the wafer. There are multiple excited states that are hard to distinguish, populating the wavelength range around 1160 - 1230 nm, with less than ideal energy separation of the excited states from the ground state.

The local variation of PL can be likely attributed to local temperature differences

across the wafer, though a clear trend or dependence is yet to be found. It is conceivable that the heater set-up of the MBE chamber may not be able to guarantee uniform temperature distribution within the range required for the best QD quality at a 300 mm scale, but this is not an issue that is insurmountable. Analysis tools such as 300 mm scale PL map will be beneficial to provide a deeper insight of the origin of the variations, and improvements can be made accordingly with that information. Nevertheless, the wafer with 300-mm scale QD growth exhibits satisfying QD growth quality targeting on O-band applications and is ready to be used for functional device processing.

3.3 Fabrication developments for QD lasers

3.3.1 Fabrication process overview

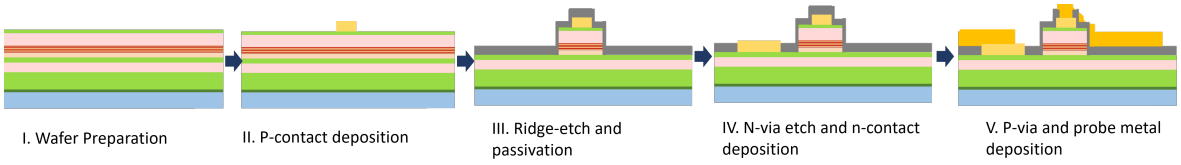


Figure 3.5: Fabrication process of cleaved-facet ridge-waveguide lasers on Si. From [11]. ©MDPI 2023.

The fabrication process of cleaved-facet ridge-waveguide lasers on Si is shown in Figure 3.5.

The process starts with wafer preparation, where pieces are diced out from the 300 mm wafer for fabricating at the Nanofab at UCSB. Then p-contact deposition on top of the epitaxial layer is conducted with a bi-layer lift-off process using e-beam evaporation, and the deposited p-contact stack is Pd/Ti/Pd/Au with thickness 100/400/400/5000 Å. After that, the ridge waveguide is defined with a hard-mask patterned mesa etch followed

by a passivation to protect the sidewall of the exposed III-V ridge. The n-contact layer at the bottom of the mesa etch is then exposed with an n-via oxide etch, followed by another bi-layer lift-off process using electron-beam evaporation to put down the n-contact stack Pd/Ge/Au with thickness 400/1600/5000 Å. Rapid thermal annealing (RTA) at 350 °C for 60 seconds is applied to anneal the n-contact. The p-contact is annealed during the hardmask deposition and passivation steps in the 300 °C PECVD chamber). After that, p-via is opened with oxide etch and probe metal for both p- and n- contacts is deposited using a final bi-layer lift-off process of e-beam deposition, where a planetary rotation is applied to ensure coverage on sidewalls and a stack of Ti/Au with 220/15000 Å, where the additional gold thickness is also aimed at improving sidewall coverage and ensuring effective probing of the p-contact.

For additional information that will be helpful to understand the fabrication process, please refer to the process follower in the Appendix.

After the major fabrication process steps, the finished sample is diced or cleaved into individual dies of about 1 cm × 1 cm dimension, and substrate thinning is performed with a mechanical polisher (Allied) using SiC film (Ted Pella) for the initial thin-down towards around 300 µm followed by diamond lapping films (3M) of finer grids (30 µm, 6 µm etc., up to 1 µm if needed) to aim at a target substrate thickness between 150 µm and 180 µm with a smooth shiny finish to facilitate the later cleaving process. Thinner substrate (such as 120 µor even thinner) would likely provide a better cleaving result, but it makes the piece very fragile and increases the difficulty in handling. Thicker substrates (such as 200 µm or even thicker) are easier to handle, but may risk cracking, turning or non-vertical sidewalls during the cleaving due to the nature of the Silicon substrate. Cleaving is performed with an automated wafer cleaver (Loomis LSD-155LT) to yield laser bars of various lengths such as 1 mm, 1.5 mm and 2 mm for cleaved-facet Fabry-Perot laser measurements.

The process is very similar to that reported in previous publications of QD lasers directly grown and fabricated on Si. Nevertheless, several developments have been made to simplify the process and reduce unnecessary steps, improve laser performance and reliability, and improve overall yield. A selection of the fabrication development will be discussed below.

3.3.2 Development for mesa etch

The mesa etch forms the ridge waveguide structure of the laser Fabry-Perot cavity, and it is desirable to have (1) desired mesa width as designed; (2) high sidewall verticality; (3) high sidewall smoothness; and (4) precise etch-stop to expose the n-contact layer; (5) minimum etch residue to avoid further contamination and complication in process affecting laser quality.

In order to achieve these desired qualities, the step is developed carefully with (a) etching chemistry and bias parameters, etching chamber cleanness and maintenance, (b) mask design for clearance dimensions between layers, and (c) precise etch-stop control.

(a) Etching chemistry and bias parameters

The etching step is performed using an inductively-coupled plasma etcher (ICP #2, Panasonic E640) with Cl_2/N_2 based dry etching with a SiO_2 hardmask deposited by PECVD and patterned with lithography and dry-etch. The etching parameters are listed in Table 3.2 below:

AlGaAs/GaAs Etching Recipe using ICP #2 (Panasonic E640)				
Flow-rate (sccm) for Cl_2	Flow-rate (sccm) for N_2	Pressure (Pa)	Bias (W)	ICP (W)
20	10	0.2	100	900

Table 3.2: AlGaAs/GaAs Etching Recipe using ICP #2 (Panasonic E640).

The bias set as 100 W is relatively high to provide a more vertical sidewall angle. Similar recipes can be created for different ICP etchers, such as ICP-Etch (Unaxis VLR) and Oxford ICP Etcher (PlasmaPro 100 Cobra).

ICP-Etch (Unaxis VLR) has been the choice of many previous fabrication runs performed in the research group for similar InAs/InGaAs QD laser device fabrications, and it was favored due to its adjustable temperature setting and relatively stable etch rate when doing timed etch without any monitor, whereas ICP #2 (Panasonic E640) is known for a fixed chuck temperature of 15 °C and its etch rate drifts from time to time, but is usually more available and has less maintenance down time. Oxford ICP Etcher (PlasmaPro 100 Cobra) is a newly installed ICP etcher in the Nanofab, and a series recipe development was performed to reproduce the AlGaAs/GaAs etch with it, potentially with better etching results. Details of the experiments will be presented in Chapter 5. Table 3.3 and Table 3.4 are the recommended AlGaAs/GaAs recipes for ICP-Etch (Unaxis VLR) and Oxford ICP Etcher (PlasmaPro 100 Cobra).

AlGaAs/GaAs Etching Recipe using ICP-Etch (Unaxis VLR)					
Flow-rate (sccm) for Cl_2	Flow-rate (sccm) for N_2	Pressure (mTorr)	Bias (W)	ICP (W)	Temp (°C)
20	10	2.0	75	800	30

Table 3.3: AlGaAs/GaAs Etching Recipe using ICP-Etch (Unaxis VLR).

AlGaAs/GaAs Etching Recipe using Oxford ICP Etcher (PlasmaPro 100 Cobra)					
Flow-rate (sccm) for Cl_2	Flow-rate (sccm) for N_2	Pressure (mTorr)	Bias (W)	ICP (W)	Temp (°C)
20	10	2	75	800	30

Table 3.4: AlGaAs/GaAs Etching Recipe using Oxford ICP Etcher (PlasmaPro 100 Cobra).

In general, the writer was able to produce satisfying mesa etch results with all three

ICP etchers mentioned above, while the discussions and results presented in later section of this chapter were produced with ICP #2 (Panasonic E640). From a personal point of view, taking on extra process development time with comprehensive and experimental scientific approaches is more beneficial than holding on to inherited fab myth or dealing with stress in fabrication due to uncertainties from lack of experience.

(b) Clearance dimensions between layers

In the current process, the p-contact is deposited before the mesa etch and it would also act as a hardmask if it is exposed. In order to protect the mesa sidewall quality, it is important to have the oxide pattern slightly wider than the p-contact pattern so as to avoid a direct masking from p-contact which will produce additional roughness and possibly also undesired angle at the mesa sidewall translated from the roughness and angle of the p-contact edge through metal lift-off. At the same time, the oxide pattern should also not be too much wider as it will affect the current injection and spreading path from p-contact and inefficient pumping will lower the laser gain and increase the threshold.

The actual clearance is affected by not only the dimension in the mask layout design, but also the choice of photoresist and settings of focus, dose and exposure for lithography for the p-contact and mesa hardmask layers, as they may either make the actual dimension wider or narrower than what is designed on the mask GDS. Detailed studies of layer dimensions from mask layout and fabricated device will be covered in the upcoming section 3.4.4.

(c) Precise etch-stop control for n-contact

For lasers grown directly on Si, back-side n-contact is not a readily available option, and the n-contact is made with exposed n-doped layer on one or both sides of the mesa.

For the one-step deep-etch design, the mesa etch will also serve as a step that exposes the n-contact.

In particular, for the newly introduced "70% AlGaAs asymmetric thin" epitaxial layer design, the n-contact layer is only 300 nm, and the total etch depth is 1885 nm from top of p-contact to top of n-contact. To avoid overetching the n-contact, it means there has to be etch uniformity and etch-depth control within roughly 15 % of the total etch.

In-situ laser monitor is used to ensure precise control of etch depth and immediate termination of the reaction when the target layer is reached.

The laser monitor installed on ICP #2 (Intellemetrics Laser Etch Monitor) has a wavelength of 670 nm, and traces of the reflectivity are plotted as the etch goes through. For films that are transparent at the laser monitor wavelength, usually an sinusoidal signal will be shown as the films are etched thinner due to optical wave interface [12]. Change of the sinusoidal signal period usually indicates that the etch is entering a different material composition.

For example, when using the recipe in Table 3.2 to etch through a dummy piece of our "70% AlGaAs asymmetric" thin epitaxial layer design, the following laser monitor trace can be obtained, as shown in Figure 3.6.

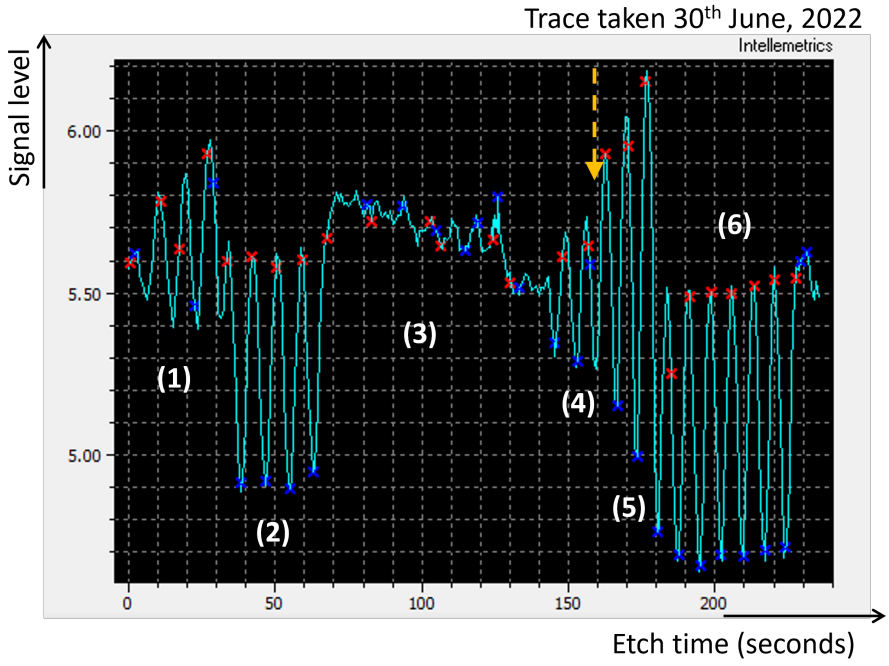


Figure 3.6: An example of the *in-situ* laser monitor etch trace with ICP #2.

In the etch trace in Figure 3.6, the different groups of reflection signals sequentially represent the ongoing etch from top to bottom in order, for the following layers and their thickness estimation: (1) p-doped GaAs p-contact layer of 300 nm thickness; (2) after 50 nm of graded transition, 400 nm of p-doped $Al_{0.7}Ga_{0.3}As$ upper cladding layer with another 20 nm graded transition and 30 nm p-doped $Al_{0.2}Ga_{0.8}As$ layer; (3) GaAs waveguide and 5 periods of quantum-dot-in-well structure with total thickness of 685 nm; (4) n-doped $Al_{0.2}Ga_{0.8}As$ lower cladding layer of 400 nm thickness; (5) n-doped GaAs n-contact layer of 300 nm thickness; (6) $Al_{0.7}Ga_{0.3}As$ lower cladding layer of 700 nm thickness. The layer below is the GaAs buffer and is where the interference trace ends.

The yellow arrow in the figure indicates the intended etch stop at the top of n-contact layer for the mesa etch. Using this method, the total etch depth and target layer can be

inferred and it is more reliable than any timed etch, even if the desired stack has higher tolerance for the etch stop.

It is important to stop the etch closer to the end of the n-cladding layer, right before reaching the n-contact layer. In this way, the highest possible n-contact thickness can be left for a lower n-contact resistance. This will be paired with a slightly over-etched n-via etch to ensure the n-contact layer to be exposed, even if there is a thin n-cladding layer left from mesa etch. A very minor extra benefit is that since the chemistry for n-via oxide etch does not react with GaAs, it will be more a physical attack for a rough (or "matte") finishing of the n-contact surface, potentially giving the benefit of larger contact area thus also lower n-contact resistance.

As mentioned before, there is condition drifting in the ICP #2 (Panasonic E640) etcher and the etch rate has been suspected to fluctuate if experiment is conducted in a few weeks or months of separation. Figure 3.7 shows the trace taken from the same etching recipe towards pieces from the same epitaxial wafer at two other times, one in May 2022 and one in August 2023.

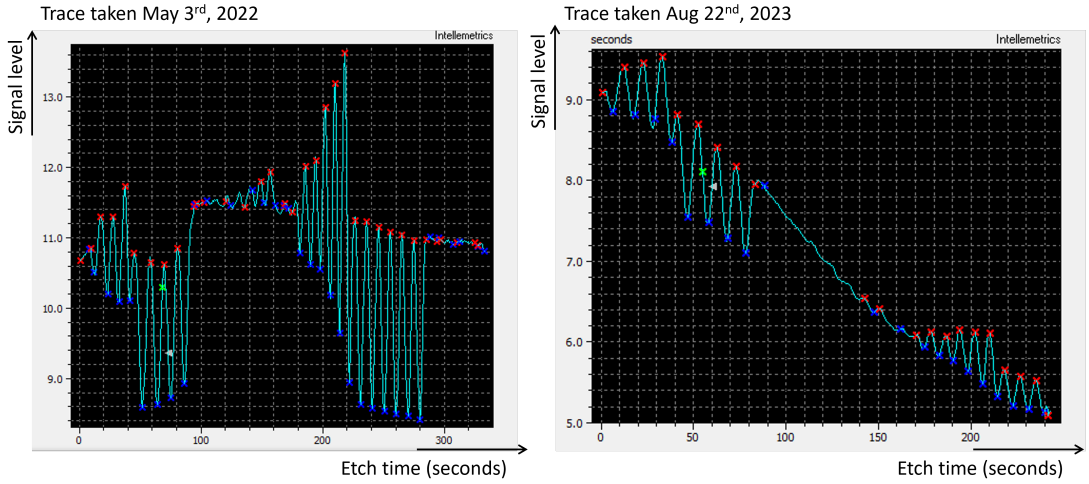


Figure 3.7: Alternative *in-situ* laser monitor etch traces with ICP #2.

In these two additional examples, the time to etch towards top of n-contact are about 195 s and 190 s, respectively, compared to the previously shown trace of about 160 s. This indicates a 19 % increase in etch rate. Additionally, the trace on the right shows a decay in signal level as the etch goes in, which was seen repeatedly during different etches around that time and has occurred in different time of the year as well, and was suspected to be a result of a change in laser monitor alignment or chamber being coated with residues. Nevertheless, the period transition and overall etching speed remains comparable for this same epi and same recipes, and successful etch monitoring and etch-stop control can still be conducted given careful observation of the trace and unhesitating reaction (to manually terminate the etch) when the etch-stop point is reached.

Sample-loading effect of having different etch rate (as well as etching angle and side-wall profile) for different location of the sample or for different sample sizes was raised as a concern from experiences of previous fabrications involving AlGaAs/GaAs etches. In the current experiment, the sample size is kept around 3 cm $\times$ 3 cm with a consistent Si substrate, and the etching results are consistent for different inspected locations across the same sample. In the future, should there be variations in etch rates occur across different locations of a larger wafer, techniques such as dummy fills can be implemented to improve the uniformity of pattern density across the wafer and mitigate any potential effects. This practice is commonly employed in Si photonics foundries for established processes such as waveguide etch.

3.3.3 Development for eliminating void formation

"The void problem" has been occurring in the QD laser fabrication and testing across different batches of devices with variations of different epitaxial stacks such as 70% versus 40% AlGaAs cladding, different mesa designs, such as two-step etch and one-step

etch, and different fabrication process details such as exposure and dose setting, cleaning procedures etc.

"The void problem" is a visible hole typically appearing at the top-cladding layer of the finished device visible from cross-section SEMs after cleaving, both before and after LIV testing. Figure 3.8 below shows some example of such images from previous fabrication runs in the group.

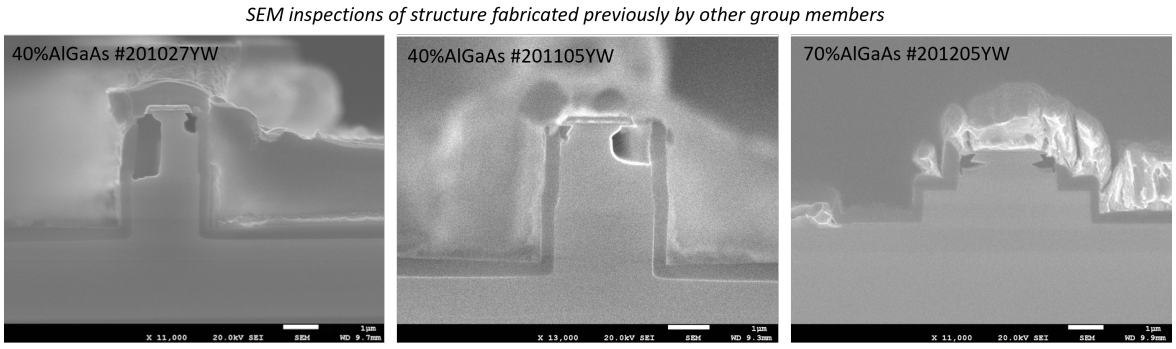


Figure 3.8: SEM inspections of structure fabricated previously by other group members showing "the void problem".

Previous investigations conducted by J. Selvidge has confirmed that the voids are corrosion happening along the entire ridge instead of any defect from cleaving or cross-section imaging, shown in the top-view SEM of the fabricated lasers with top cladding removed in Figure 3.9.

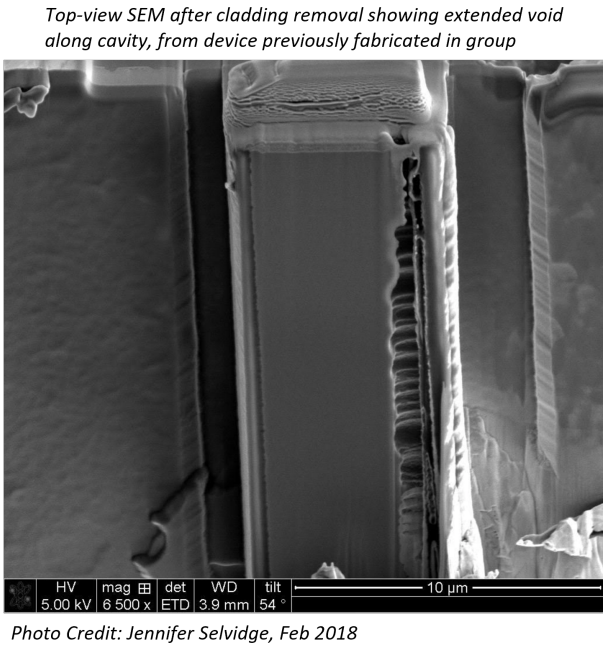


Figure 3.9: Top-view SEM after cladding removal showing extended void along cavity. Credit: Jennifer Selvidge.

Such voids are undesirable as they degrade the device performance and accelerate structural damage and device aging, not to mention that the added uncertainties would make it hard to draw a conclusion of the QD growth quality from analyzing device performance when comparing the different sample groups. It is critical to figure out the science behind the formation of voids, or at least make improvements of the fabrication process to avoid their formation.

Here are some findings from discussions and tests to narrow down particular steps or factors that aggravate the situation:

(1) Voids appear on both the process with order of p-metal before mesa etch and process with order of p-metal after mesa-etch.

(2) Voids appear on both the device with 70% cladding and 40% AlGaAs cladding.

(3) Voids appear on either one side of the device or both sides of the device, and there

seem to not be a consistently preferred side.

(4) Some voids are paired with cracked oxide passivation layer with poor adhesion to the mesa sidewall.

(5) Voids are not visible from the samples we inspected after mesa etch and passivation, so they may appear after n-via, p-via etch, their related cleaning steps or probe metal deposition and lift-off.

A conference proceeding in 2003 studied the occurrence of corrosion formation near ohmic and gate metal layer during GaAs wafer processing[13]. The study showed corrosion to AlGaAs next to the metal line with Ti/Pt/Au as the alloy shows up after treatment with photoresist stripper, compared the experimental results with SEMs for visible corrosion and tested contact degradation for different combination of solvents commonly included in different photoresist stripper products, and provided some theoretical support for galvanic corrosion. Though there has been limited supportive literature resources such as journal publications, and more experiments need to be done to confirm whether the visible voids in our case is the same reaction as presented in this work, the study provides a perspective of the importance of choosing photoresist stripper, reducing exposure time to solvents and rinsing solutions, and considering alternative techniques for effective photoresist stripping and residue cleaning than extensive soaking.

Also, a few device fabrication runs that I conducted with different sets of mask parameters and inconsistency of certain details from the group heritage recipes show significantly less voids, as shown in Figure 3.10. These fabrication was done with epitaxial layers of similar composition to the ones with voids, including both deep-etch design and two-step-etch design. One difference that can be seen from the cross-section SEMs is their smaller p-via opening dimension, which may be related to the prevention of extensive corrosion.

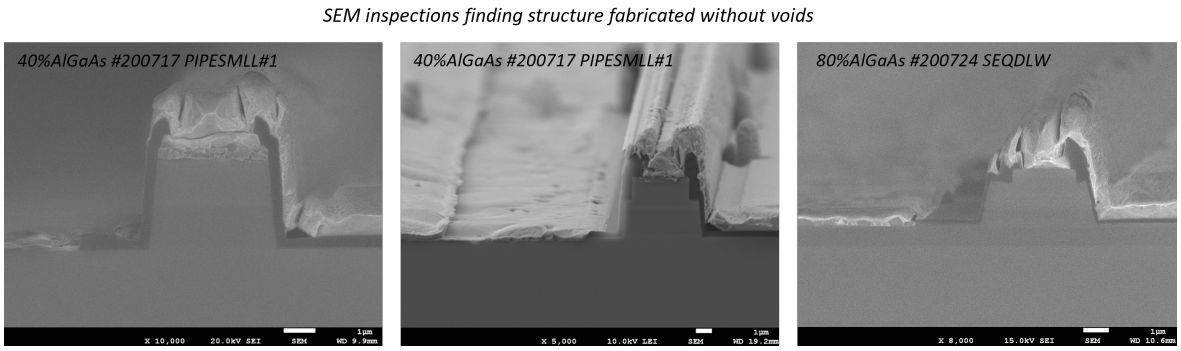


Figure 3.10: SEM inspections finding structure fabricated without voids.

Closer inspections of cross-sections of different devices with or without voids, or with void only on one side, from one same sample, show more correlation between p-via opening and void formation. Figure 3.11 shows these structures fabricated in the early generations for the topic in Chapter 4 in parallel of the fabrication development here, where the misalignment in p-via layer opens the passivation wider on one side and less on the other, which leads to void formation on the side with wider opening. On the same sample, from the bars in locations with less misalignment of the p-via opening, the passivation layer is sealed on both sides and there is no void found at p-cladding.

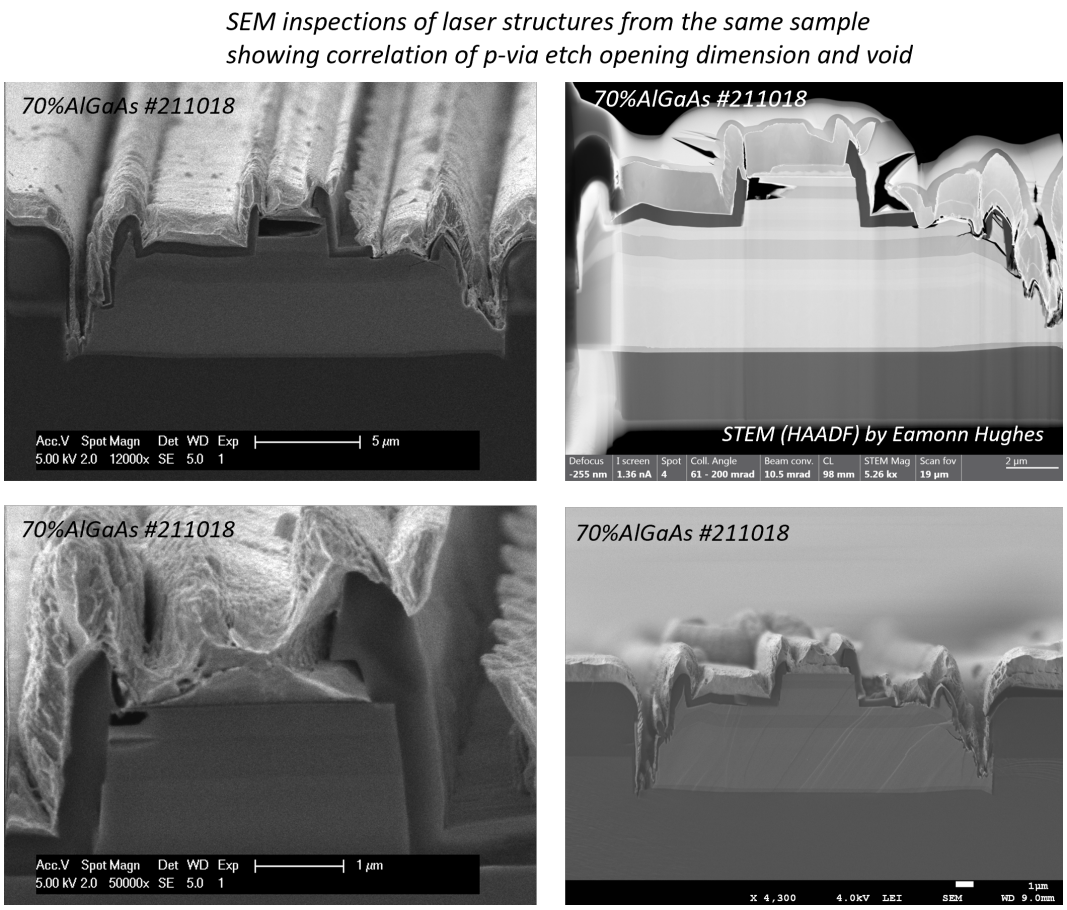


Figure 3.11: SEM inspections of laser structures from the same sample showing correlation of p-via etch opening dimension and void.

From these clues, I suspect the voids are formed with certain reactive liquid penetration through gaps created from edges of p-via etch or imperfect oxide passivation. I have never been able to verify this hypothesis, but rather the focus was shifted to improve the fabrication process to avoid void formation for practical purposes.

There are two major improvements taken into consideration. One is to eliminate unnecessary cleaning and ashing steps as well as extra handling in the process and limit total liquid exposure time, and the other is to redesign structure dimensions to ensure better sealing and prevent liquid penetration.

(a) Simplified and shortened cleaning steps

During the fabrication, it is typical to see tenacious photoresist residue after the hardmask dry etch using ICP, which occurs in the steps of mesa hardmask etch, n-via etch and p-via etch. As the oxide thickness increases, the total dry-etch time is also longer, which causes longer photoresist exposure in the etching plasma and potentially harder to be removed. The common process is to adopt a 20 mins O_2 ashing using the ICP #1 (Panasonic E626I) ashing chamber, followed by rinsing in acetone, isopropanol, and soaking in NMP solution in a heated bath of 80 °C for at least 20 minutes to an hour, and sometimes overnight or even longer. In some heritage process followers, NMP soak is also used for metal lift-off process, including the p-metal, n-metal and probe metal steps, which adds more overall heated soaking time to the sample.

NMP (N-methyl-2-pyrrolidone) is a solvent commonly used to dissolve a wide range of polymers. As a powerful photoresist stripper it has been used in many Si photonics fabrication processes. It is possible that the "heritage step" of long soak in NMP is causing the formation of voids.

Experiments were conducted to look for the "simplest possible" procedures to clean the PR. The simplified cleaning procedures are below.

For post hardmask dry-etch or via-etch: the sample first goes through a quick but thorough acetone and isopropanol rinse, with about 2 - 5 mins soak time in acetone. After that, use Plasma Clean (YES EcoClean, nicknamed "YES Plasma") for a 2 min 100 °C recipe with O_2 and N_2 gas.

The YES Plasma tool [14] is an ICP downstream asher, and the excitation of the oxygen is done remotely without the charged ions reaching sample surface, so that the gas mixture only contains neutral oxygen radicals for sample cleaning. It is a purely chemical process with no ion bombardment compared to plasma ashing directly with an

Improvement of cleaning procedures		
Process	Previous practice	New process
Post dry-etch cleaning	Acetone rinse, O_2 ashing with ICP #1, NMP soak in 80 °C heated bath for 20 mins - 1 hour, up to overnight, PEII ashing (sometimes with high power), inspect and cycle (wet cleaning and ashing) until clean.	Acetone rinse, 2 mins YES Plasma ashing with 3kW at 100 °C with O_2 and N_2 , inspect and add one or two cycles of 2mins ashing if needed.
Post lift-off cleaning	Acetone/NMP rinse or soak overnight, followed with PEII ashing	Acetone rinse and soak until lift-off (20 mins), DUV flood exposure 5 mins, and AZ726 develop for 2 mins.

Table 3.5: Comparison of new cleaning procedures with previous practices for post dry-etch cleaning and post lift-off cleaning.

ICP tool, and the heated temperature helps accelerate reaction time [15].

Using this simple and efficient method, it is usually enough to clean-off PR residues for mesa hardmask etch. For p-via etch and sometimes n-via etch, it may need one or two more cycles of the 2 min YES Plasma clean for additional clean-up, and usually that would be sufficient. The limitation of the small cleaning time interval is said to avoid overheating of the sample from the 200 °C hot plate in the chamber, though the sample is lifted, but may not be critical depends on the actual material and process steps. It is also recommended to use a recipe with O_2 only (without N_2) when there is exposed gold metal on surface to avoid oxidation, but it comes with the price of less efficient stripping and added cycles needed for complete cleaning.

This new cleaning process reduced more than an hour of soaking in NMP helps

eliminating one factor that may contribute to the void formation. It saves processing time and avoids the complication of linked tool booking (booking ICP # 2 and ICP #1 in connected slots for etch and clean) or turning into a typical late night cleanroom Hamlet pondering "is this clean enough or should I put it back in NMP", "should I go home and leave it soaking overnight or should I wait longer and check", "will it clean the PR more or will it harm the wafer more". In this case, less is more.

Though PPE and hood is always required, unsafe handling could still be seen in the cleanroom, likely as a result of carelessness and fatigue, especially from frustration of dealing with tough residues. NMP is a class 2 hazard [16] and can cause eye and skin irritation and have a chronic effect on fertility, "particularly pregnant women and women of childbearing age" [17, 18], the new process is bearing far less risk of toxic exposure than the previous practice that involves hours of struggle with NMP.

For post metal deposition lift-off: the sample first gets soaked in acetone solution for dissolving the top-layer SPR photoresist, which usually takes 10 - 20 mins depends on pattern sizes and aspect ratios. Covering large chunks of non-depositing area with aluminum foil during deposition helps reducing the acetone lift-off time. Using pipette to blow air in the beaker also helps mechanically accelerate the complete lift-off. Rinse in isopropanol. Then expose the sample in DUV Flood exposure for 5 mins for complete exposure of the underlying PMGI layer (SF15, in this case), followed by 2 mins soaking in AZ 726 for complete removal. Rinse in DI water carefully and thoroughly, since left-over PR stripper trapped on sample could cause potential penetration and corrosion. Dry thoroughly with N_2 gun. Usually the sample is cleaned enough after this step and no scums should be left.

This whole lift-off process takes only less than half an hour in total, and also avoids long soaking in either acetone or NMP which is completely unnecessary.

With these improvements, the total liquid exposure time of the process is reduced by

at least an hour, if not tens of hours (if previously soaked overnight). Exposure to NMP solvent is completely eliminated in the new process, which is also a safer process.

(b) P-via etch improvements

P-via etch is a critical step that is suspected to be causing a pathway of liquid leakage into the p-cladding layer for corrosion, especially as it is a longer dry etch due to the accumulated oxide thickness usually exceeding 1 µm on mesa-top with two accumulated oxide depositions (mesa hardmask and passivation), and a longer etch time causes harder PR residues from the extended exposure to the etching plasma hence harsher PR cleaning procedures with longer liquid exposure and surface attack. Also, unnecessary overetch time could potentially open the sidewall coverage and create cracks at mesa edge leading to liquid leakage and corrosive trapping.

The heritage method was to use a total 20% additional etch time, calculated with the total deposition time without taking into account the oxide thinning from physical bombardment during mesa etch (usually around 100 - 150 nm with ICP #2). The excessive 100 - 150 nm oxide thickness in calculation will add about 30 sec unnecessary etch time, independent from the 20% addition. Two changes are made in the new process: (1) to use a separate Si dummy with the two passivations as well as being loaded during the mesa etch to monitor the oxide thinning for more accurate estimation of p-via oxide thickness; (2) to use the laser monitor for a quicker etch stop (about 10 seconds overetch after the trace flats) instead of always conducting a 20% overetch time. The two improvements reduces potential of passivation cracks from overetch and reduces the amount of PR residue scums hence a lighter cleaning procedure is needed, going in line with the improvements in (a) to reduce the chance of liquid corrosion.

(c) Clearance dimensions between layers

To further reduce the chance of liquid penetration, it is important to limit the dimensions of the via etches. In the heritage process, there is usually only about 250 nm clearance between p-contact and mesa on each side, and sometimes the p-via dimension is left as the same as p-contact. The resulting device structure shows significant overlapping of p-via opening, p-contact and mesa, resulting from both misalignment (up to 150 nm or more if using GCA Stepper #2 (AutoStep 200)) and pattern distortion from focus offset due to the height difference of different layers.

To improve the situation, some focal offset numbers were adjusted during alignment, a new set of clearance dimension between layers were made in the layout design, and inspections with cross-section SEM were conducted to compare with the designed value for a clear guidance of the clearance dimension, eliminating any guessing element and uncertainties in the previous practices. Details of the layer dimension clearances in mask design will be shown in the next section, and the resulting fabricated dimension clearances will be discussed in the fabrication results.

3.3.4 Design guidelines for layer dimensions

Table 3.6 shows a summary of the recommended parameters on mask for making deeply-etched ridge waveguide Fabry-Perot lasers with top-side contacts for both p- and n-contact. An illustration of the dimensions is shown in Figure 3.12.

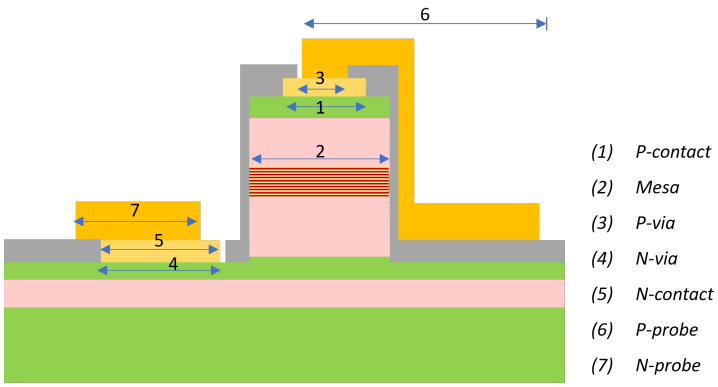


Figure 3.12: Schematic illustrating critical dimensions in ridge waveguide laser fabrication.

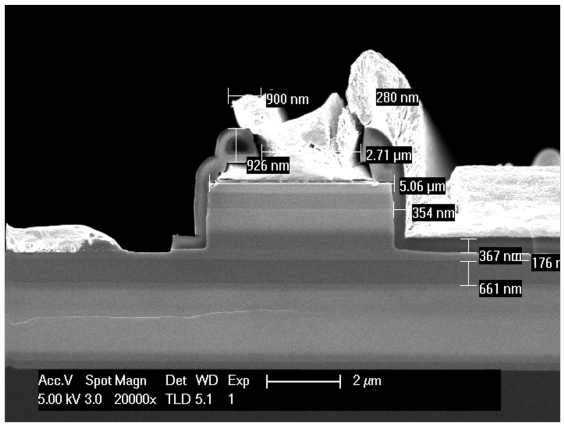
Design guideline for layer dimensions			
Suggested layer clearances on mask		Example of layer dimensions on mask	
-	-	Pcontact	4 µm
Mesa outside Pcontact	0.5 µm each side (critical)	Mesa	5 µm
P-via inside Pcontact	0.75 µm each side (critical)	P-via	2.5 µm
N-via from mesa	1.5 µm (suggested)	N-via	100 µm
N-contact from mesa	3 µm (buffered)	N-contact	100 µm
P-probe metal inside mesa edge	0.8 µm (critical)	P-probe metal	125 µm
N-probe metal away inside n-contact edge	10 µm (buffered)	N-probe metal	100 µm

Table 3.6: Recommended deisgn guideline for layer dimensions for deeply etched ridge waveguide laser.

The most critical clearance is between p-via, p-contact and mesa. It is important for the mesa to be wider than p-contact with potential misalignment taken into account, to ensure the mesa hardmask edge defined with dry etch will be the one that masks the etch of ridge waveguide sidewall, since higher sidewall roughness would occur and cause higher loss if the etch is shadowed from the edge of metal deposited by lift-off instead. The p-via needs to be much narrower than the p-contact to prevent potential liquid leakage pathway at the edges of p-via and prevent serious corrosion, as mentioned previously.

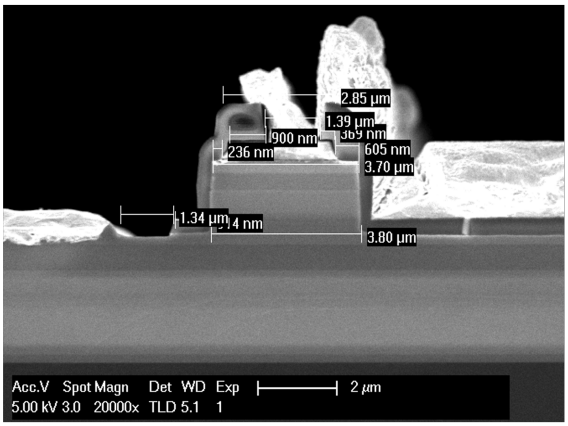
Apart from that, abundant separation of the n- and p- contact metals and probe metals will help prevent metal absorption loss (if the contact is placed too close to the mode) and potential shortage (if the n- and p- probe metal touches each other). The extra buffer for separating n- and p- probe takes into account the larger undercut usually used in bi-layer lift-off for probe metal and the heavier angled deposition when using e-beam evaporation with the planetary rotation fixture.

SEM of device with 5 μm on-mask mesa width



	On mask	By SEM
P-via	*2.5 μm*	*2.71 μm*
P-cont	*4 μm*	*3.71 μm*
Mesa	*5 μm*	*5.06 μm*

SEM of device with 3.7 μm on-mask mesa width



	On mask	By SEM
P-via	*1.2 μm*	*1.39 μm*
P-cont	*2.7 μm*	*2.85 μm*
Mesa	*3.7 μm*	*3.80 μm*

Figure 3.13: Comparisons of dimensions designed on mask layout versus measured from fabricated devices.

Figure 3.13 shows a comparison of the dimensions measured from a cross-section SEM of the fabricated devices with the dimensions designed on mask layout. Note that this is also specific to the lithography tool used in this fabrication process, and the focus offset and exposure time settings [1].

[1]For the process run discussed in this chapter, GCA Stepper #2 (AutoStep 200) is used for lithography; SPR 1.8 is used for p-contact, and SPR 3.0 for the rest; focus offset is applied at the n-contact layer for lower focal plane. In the later fabrications discussed in Chapter 4 and 5, Maskless Aligner (Heidelberg MLA150) is used primarily and the parameters are listed in the process follower at the Appendix.

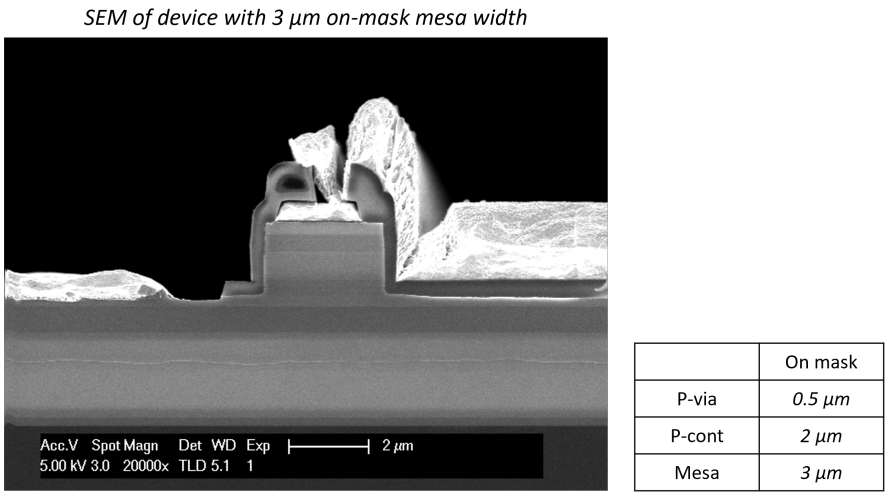


Figure 3.14: Cross-section SEM of ridge waveguide laser with 3 µm on-mask mesa width.

These numbers should serve as a rough guide for reproducing the results here, and can be further adjusted if different designs are adopted. For example, we were able to make lasers with 3 µm mesa width, as shown in Figure 3.14, but the high aspect-ratio of the narrow p-via with thick passivation is hinting a challenge for further shrinkage. Changes such as lower the passivation thickness or squeezing the clearance dimension (e.g. widen the p-via marginally) are probably needed.

3.4 Measurement results and discussions

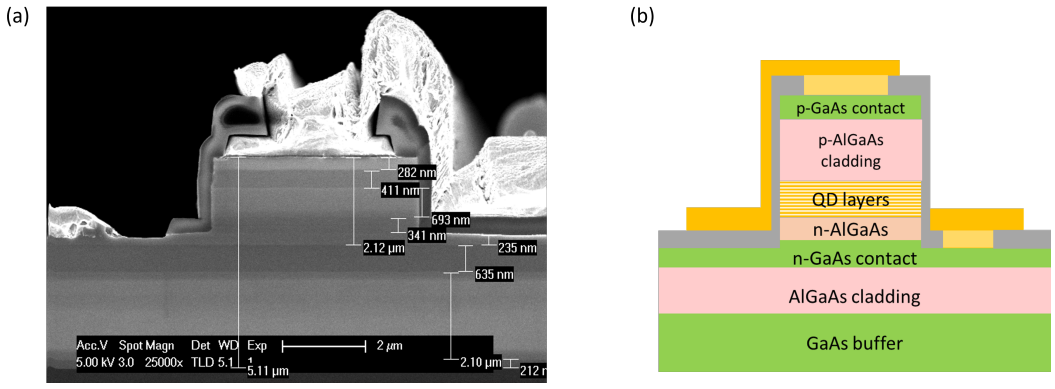


Figure 3.15: Fabrication results. (a) Cross-section SEM of a laser with ridge width of 5 µm. (b) Schematic of the deeply etched ridge waveguide laser design.

Figure 3.15 (a) shows the cross-section SEM of a laser fabricated from planar growth with a ridge width of 5 µm. Following extensive process development, the fabricated ridge waveguide laser structure shows good side wall verticality, precise etch-stop at top of thin n-contact layer, conformal passivation and sufficient clearance for via-opening and contact metals, matching well with the designed structure in the illustration in (b).

After fabrication, back-side thinning and cleaving was performed to make cleaved-facet laser bars with lengths of 1.5 mm and 2 mm. No additional facet coating is applied at this stage.

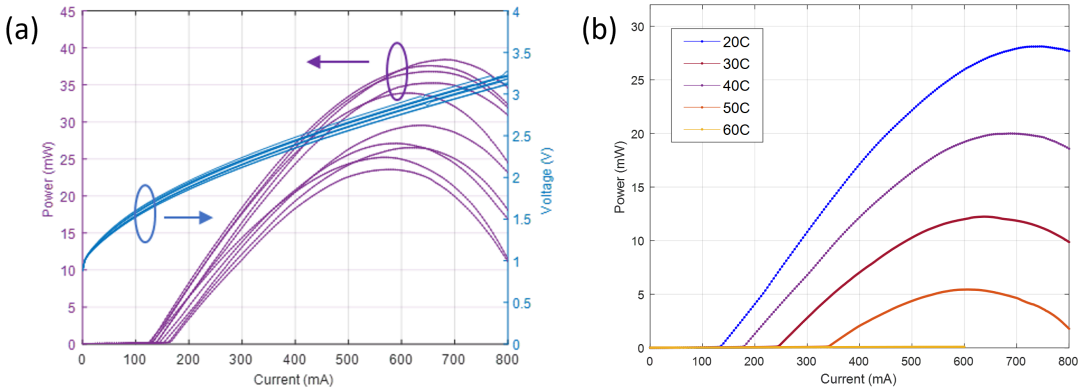


Figure 3.16: (a) LIV characteristics of 10 devices on one bar. (b) Temperature-dependent LI characteristics of a laser. From [11]. ©MDPI 2023.

We screen the devices with light-current-voltage (LIV) measurement with a temperature-controlled stage where device is probed with one set of probe needles, and an integration sphere is placed adjacent to the stage to collect the emission from the bar edge. Figure 3.16 (a) shows the LIV characteristics of ten devices from the same bar under continuous wave (CW) current injection at 20 °C. The bar length is 2 mm, and the device mesa widths cover splits between 3 - 5 µm. The maximum output power of each device from a single side varies between 20 - 40 mW. We achieved 100 % yield on some bars, though device performance varies with each design. Most devices have a series resistance around 2 Ω. Figure 3.16 (b) shows the LI characteristics of one device at different stage temperatures, and we achieved CW lasing up to over 50 °C.

We estimate the overall characteristic temperature T_0 and the characteristic temperature for above-threshold current increment T_η of this device with the following equations[19]:

$$\frac{I_{th1}}{I_{th2}} = e^{(T_1-T_2)/T_0} \tag{3.1}$$

$$\frac{\eta_{d1}}{\eta_{d2}} = e^{-(T_1-T_2)/T_\eta} \tag{3.2}$$

where T_1 and T_2 are two different temperatures, and the relative changes in threshold current I_{th} and differential efficiency (slope efficiency) η_d of the laser with regard to the change in temperature are expressed with the characteristic temperatures T_0 and T_η, respectively. The results are summarized in Table 3.7.

Temperature dependency of laser performance				
Stage temperature	I_{th}	η_d	T_0	T_η
20 °C	134.9 mA	6.094 %	34.8 K	123.6 K
30 °C	179.8 mA	5.621 %	32.1 K	64.5 K
40 °C	245.5 mA	4.814 %	30.2 K	27.6 K
50 °C	341.7 mA	3.351 %	-	-

Table 3.7: Temperature dependency of laser performance.

We estimate the T_0 to be in the range of 30 - 35 K, while the above-threshold estimation of T_η varies in the range from about 120 K to 30 K. The results shows plenty room for improvement compared to the demonstrated record results to date of QD lasers grown on Si with CW lasing up to 150 °C [20] and extrapolated lifetime over 22 years at 80 °C [21], especially for data center applications where operation temperature up to 60 °C - 80 °C is typically required [22]. Given a measured series resistance around 1.8 Ω for a laser cavity length of 2 mm, the contact resistance should not be the limiting factor of the thermal performance here. Further investigations should be needed to provide more insights on enhancement of the thermal performance, especially on the QD growth perspective.

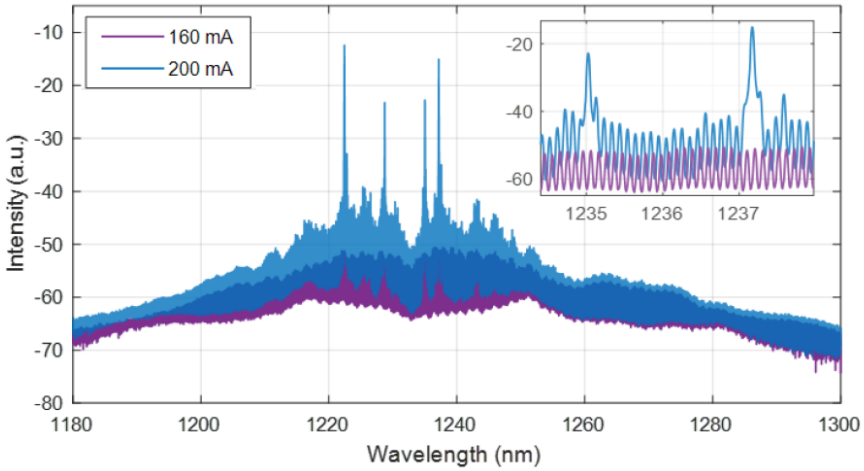


Figure 3.17: Spectrum of a laser at injection currents below (purple) and above (blue) the lasing threshold. Inset shows zoom-in details near 1236 nm. From [11]. ©MDPI 2023.

Figure 3.17 shows the spectra collected from a lensed fiber at the cleaved facet of a laser under constant current injection of 160 mA and 200 mA, which are below and above the lasing threshold of this device, respectively. This laser has a ridge width of 4 µm and a cavity length of 2 mm, and the testing stage is uncooled in a room-temperature environment. At 200 mA, multi-mode lasing near 1230 nm can be observed, corresponding to the shorter-wavelength peaks in the PL measurement results shown in Figure 3.4. The predominance of excited-state lasing is expected given the competitive PL intensity of excited states compared to the ground state [2], as well as the higher threshold current density of these lasers. From the zoom-in figure in the inset, mode spacing corresponding to a Fabry–Perot laser with cavity length of 2 mm is observed.

[2]The PL in Figure 3.4 was taken at a high pumping level to maximize ground state output intensity, which may not affect the best excited-state ground-state separation, but the excited states still appear more distinguishable than known-good in-house planar samples at the same pumping level.

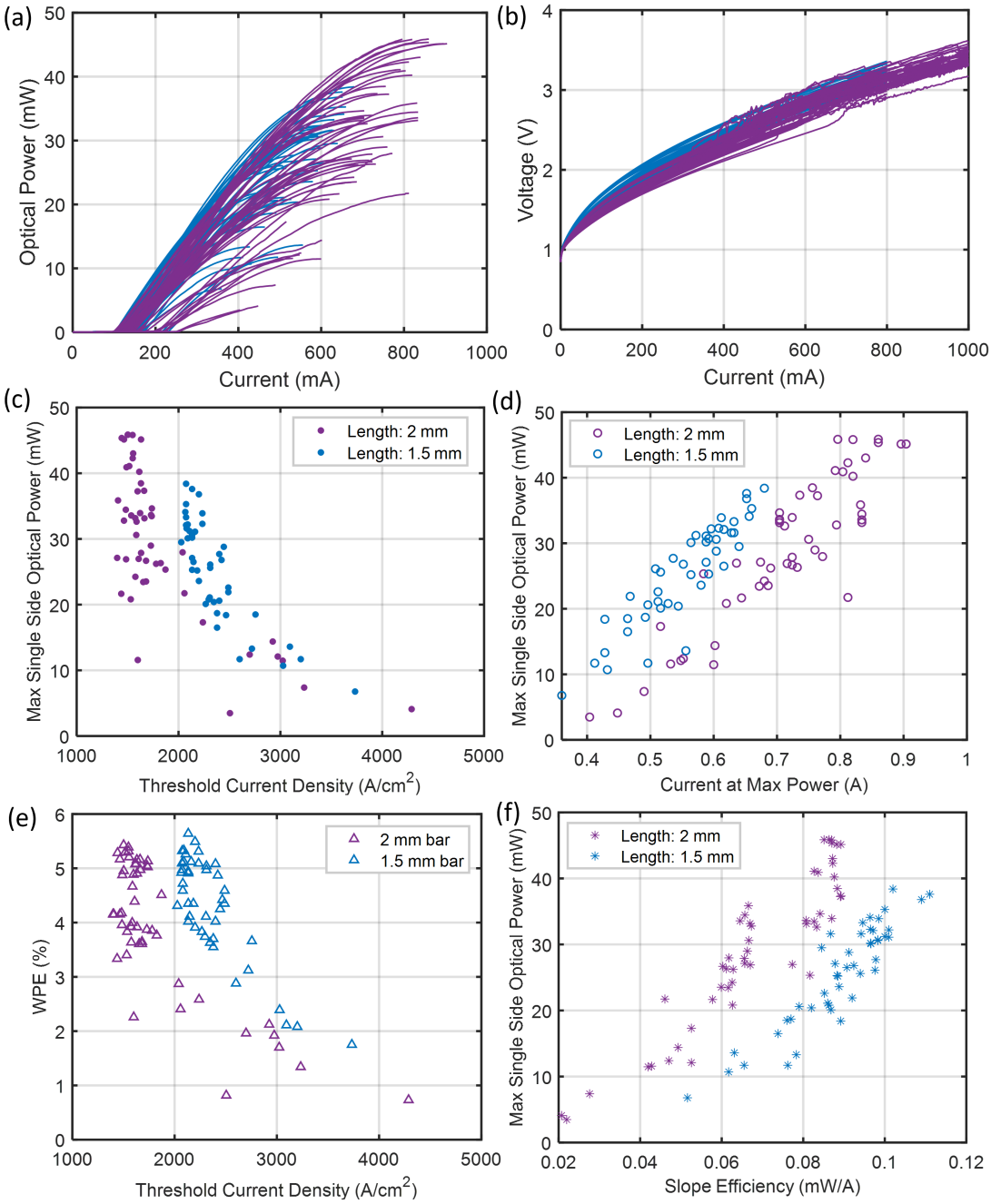


Figure 3.18: (a) LI and (b) IV characteristics from four cleaved bars, followed by comparison of performance of 2 mm bars and 1.5 mm bars in (c) highest output power and threshold current density, (d) highest output power and current required to achieve maximum power, (e) wall-plug-efficiency (WPE) and threshold current density, (f) highest output power and slope efficiency.

We analyze about 100 LIV data from four different cleaved bars from two dies on the same sample, two with cavity length about 1.5 mm, the other two about 2 mm [3]. The devices have various designs of mesa widths including 5 µm, 4 µm, 3.7 µm, and 3 µm.

Figure 3.18 (a) and (b) shows simple overlapping LIV plots of the four bars, where blue lines indicate data from the 1.5 mm bars, purple lines from the 2 mm bars. The overall LI and IV performance is comparable, showing a high yield and material consistency across sample.

We compute threshold current density with device footprint, and extract key performance parameters including maximum single side optical power, double-side wall-plug-efficiency (WPE), and slope efficiency from the LIV characteristics. The results are shown

[3]Yield of the four bars: 24/26 (1.5 mm), 22/26 (1.5 mm), 26/26 (2 mm), 25/26 (2 mm)

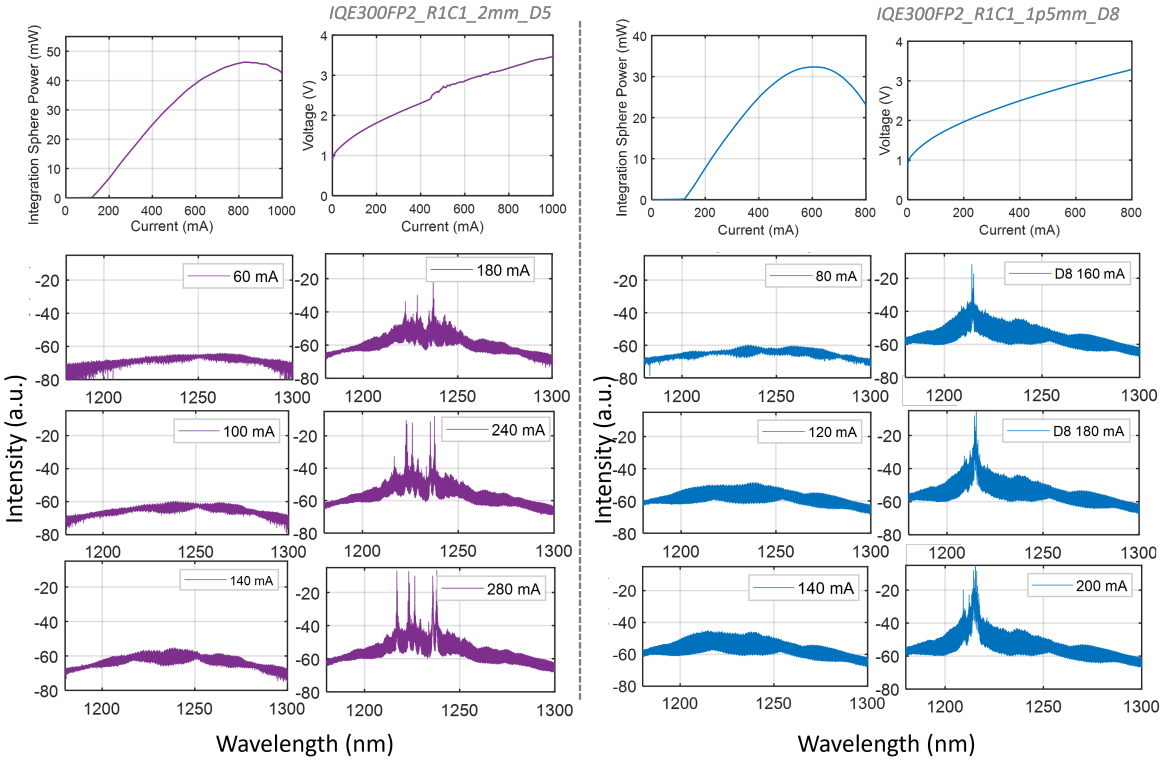


Figure 3.19: Spectra at different injection currents for (a) a device with 2 mm × 5 µm, and (b) a device with 1.5 mm × 3.7 µm.

in (c) (d) (e) (f).

The device threshold current density (J_{th}) is relatively higher compared to published results from QD growth at UCSB [2, 5, 22], which is expected from the wider FWHM from PL results showing QD growth quality differences. The devices with 2 mm length show an overall higher maximum optical power output than the 1.5 mm bars as expected, and also have lightly lower threshold current density, as shown in (a). However, despite the higher threshold current density, the 1.5 mm cavities show a higher (double-side) WPE (c) and slope efficiency (d), also displays lower current at the same maximum optical power.

In terms of spectra, here we compare a device from a 2 mm bar (left) with a device from a 1.5 mm bar (right) with different injection currents below and above threshold, respectively, as shown in Figure 3.19. Both devices exhibit excited state lasing with multiple peaks around 1220 nm. This phenomenon is expected from the inhomogeneous broadening and the low separation between ground state and excited states observed in the PL characteristics. These observations validate the previously shown results published in [11] as typical representations of our observations across all finished devices.

3.5 Summary and outlook

We demonstrate for the first time quantum dot lasers grown on a planar 300 mm Si template, with the material quality ready for large-scale laser fabrication and applications. We have shown the merits of quantum dots' tolerance to crystalline defects as an efficient gain material, and demonstrated the repeatability of MBE growth conditions irrespective of wafer sizes. Planar growth shows high quantum dot uniformity across the wafer and high yield in edge-facet laser fabrication, which is a critical step in the cost reduction and scaling of monolithically integrated III–V on Si light sources.

Comments on 300 mm QD growth improvement

The QD growth material quality at 300 mm scale is expected to be further improved if advanced techniques such as thermal-cyclic annealing (TCA) can be incorporated to further reduce the TDD in the heteroepitaxial wafer. For techniques such as TCA for a planar wafer, the concern is mainly regarding the extended growth time in a large-scale production setting. In this case, the decision would depends on achieving a well-rounded balance in cost and production quality (application values).

In terms of PL variation across the wafer, temperature non-uniformity or variations in source flux is likely the primary contributor, and this can be experimentally investigated with more sensitive *in-situ* local temperature monitoring in the large-scale MBE chambers. 300 mm wafer-scale PL mapping tools can also be beneficial in material analysis to enhance the understanding of the local dependency of PL wavelength and intensity. This can also potentially facilitate post-growth screening and inter-wafer quality grading to enhance overall yield in device processing. If the lower production cost from Si substrate and large-scale heteroepitaxy can offset a limited sacrifice in overall yield, and if the post-growth screening can be done automatically and routinely prior to device fabrication, the monolithic planar heteroepitaxy approach to III-V laser production would remain an economically favorable solution.

Comments on fabrication improvement

We have undertaken critical process developments in the ridge-waveguide laser fabrication process for improving device performance and yield, and for reducing the effect from fabrication variation when making connections between device performance and material growth quality. The design and fabrication guidelines also serve as a reference for future technology transfer to 300 mm-scale III-V/Si integrated foundry processing

[23], a promising approach for cost-efficient, large-throughput photonics integration.

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Chapter 4

QD lasers directly grown and fabricated in-pocket on 300 mm Si photonics wafers

4.1 Introduction

In this chapter, we set out to establish the monolithic integration platform with QD lasers directly grown and fabricated in-pocket on 300 mm Si photonics wafer. Following an overview of wafer preparation and MBE growth development, we present an extensive report on the fabrication process development that enabled the making of the first in-pocket QD lasers on 300 mm Si photonics wafer, addressing the challenges of MBE polycrystal deposition on sidewall and sample surface and high aspect-ratio geometry associated with the thick-oxide in-pocket configuration. Measurement results obtained from cleaved-facet lasers as well as anti-reflection(AR)-coated semiconductor optical amplifiers (SOAs) on this integrated platform are also presented, with discussions and insights that are purposed to facilitate the future improvement of in-pocket laser performance and

production yield.

4.2 300 mm Si photonics wafer preparation and MBE direct growth

4.2.1 Wafer preparation

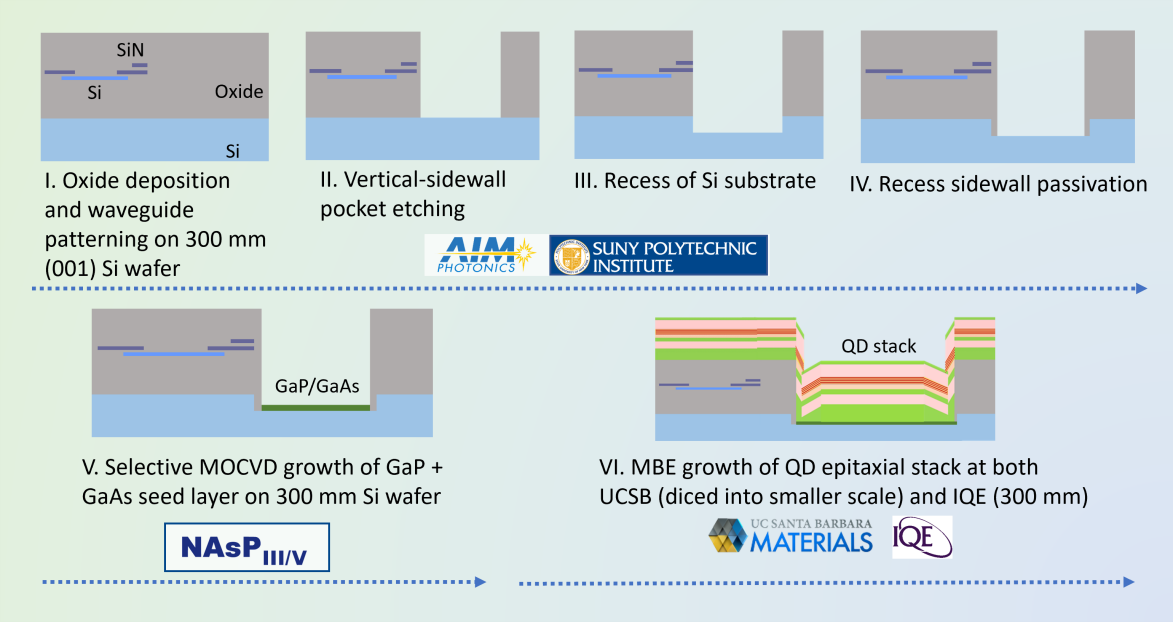


Figure 4.1: 300 mm Si photonics wafer preparation and MBE growth.

The preparation of 300 mm Si photonics wafer and the in-pocket MBE growth is illustrated in Figure 4.1. The template was prepared using a 300 mm CMOS-compatible (001) SOI wafer with SiN/Si waveguides and other Si photonics elements [1]. On the SOI wafer, 4.5 µm tetraethoxysilane (TEOS) SiO_2 was deposited to embed the waveguides. Dry-etch patterning of SiO_2 was then performed to create long, narrow pockets with vertical sidewalls in a compact configuration for on-chip heteoepitaxial growth. The

etching was followed by additional Si recess of about 2 µm for vertical alignment of the III-V growth that enables in-plane on-chip butt-coupling of QD laser/amplifiers to SiN waveguides. After that, another thin SiO_2 layer was deposited to protect the vertical Si sidewall within the recess, preparing the wafer for the initial MOCVD heteroepitaxy.

At $NAsP_{III-V}$, the in-pocket Si surface was etched back with HCl and selectively refilled to the previous level after a high-temperature heat treatment, and the template containing 200 nm of GaP followed by 500 nm of GaAs was grown in a similar manner to the planar wafer in Chapter 3 with selective MOCVD. With the finished template, MBE growth of subsequent layers was carried out either directly in a 300 mm reactor at IQE, Inc. or on smaller pieces (26 mm × 32 mm) after dicing for MBE growth experiments at UCSB. In particular, the small piece MBE growth experiments were crucial as a low-cost fast turn-around method for initial development, and the successful growth recipes were transferred to IQE, Inc. for a large-scale implementation. The in-pocket laser stack is the same as the "thin" stack introduced in Table 3.1 in Chapter 3.

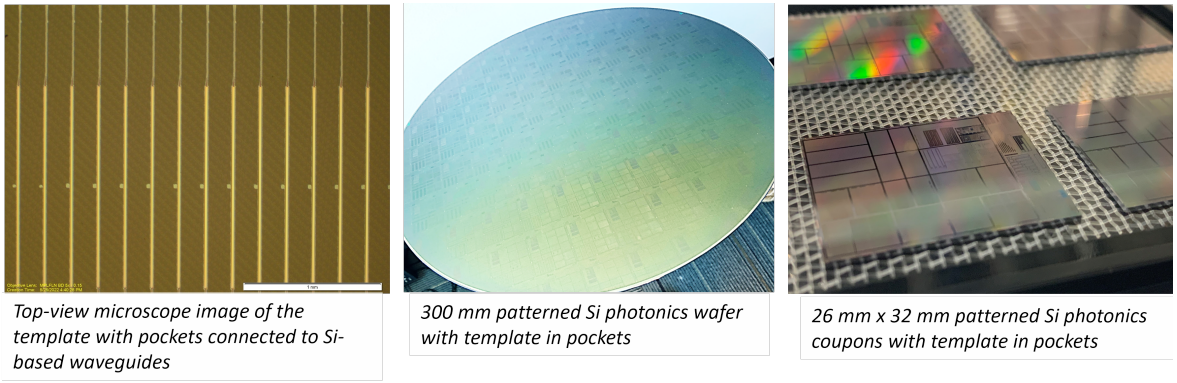


Figure 4.2: 300 mm Si photonics wafer preparation. (a) Top-view microscope image of the template with pockets connected to Si-based waveguides, (b) a 300 mm template, (c) 26 mm x 32 mm small-coupon templates.

4.2.2 MBE direct growth results

First demonstration of in-pocket QD growth on Si

The challenge of growing QD laser stack in-pocket with MBE arises from the shifting thermal profile from the template with thick oxide and its effect on the conventional techniques for chamber growth temperature control such as pyrometer readings and heater power settings. *In-situ* monitoring is not feasible to access the narrow pocket region on sample, and pyrometer readings calibrated from either Si blanket template, oxide-only surface or polycrystalline covered surface will no longer serve as an accurate representation of the actual in-pocket growth condition. However, precise temperature control is essential, as the optimal temperature window for QD nucleation as small as about 5 °C.

Experiments were conducted to gauge the overheating of the growth temperature by analyzing the indium composition analysis in the InGaAs filter layer. The desired indium composition observed indicated that the overheating was no more than 45 °C. A growth campaign with adjustments to the heater power to reach intervals of 5 °C decrements in pyrometer reading was carried out and finally high-quality QD nucleation was achieved with a minus 30 °C offset [2].

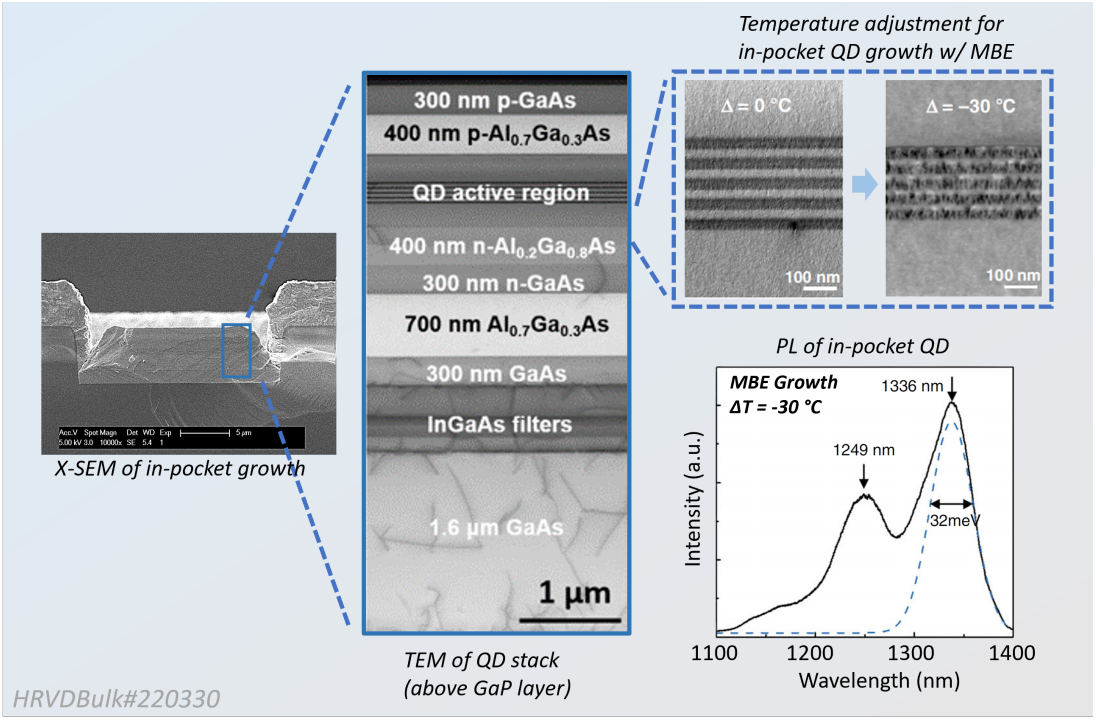


Figure 4.3: MBE development for in-pocket QD growth. Adapted from [2].

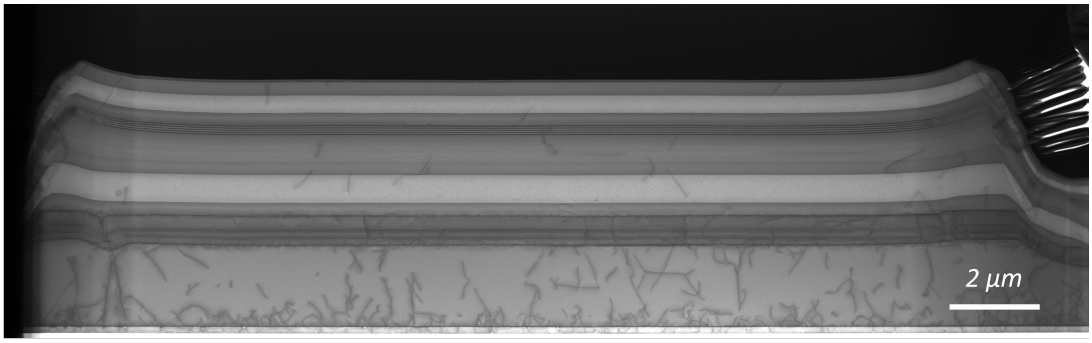
Figure 4.3 depicts the outcome of the successful QD in-pocket growth. Cross-sectional TEM shows the in-pocket QD stack as designed (note that the thickness here is just an estimate; for detailed layer structure, refer to Table 3.1), and the zoomed-in TEM pictures highlight the clear difference between the results without QD with no temperature adjustment and with 5 layers of QD with minus 30 °C temperature adjustment. The room-temperature PL spectrum shows a ground state peak near 1300 nm, with a full-width at half-maximum (FWHM) approximated to be 32 meV and a ground-to-excited-state peak separation of 70 meV [2].

The growth results were later repeated on various generations of integration layouts with different pocket size, orientation and fill-factors on sample. Encouragingly, the conditions remained generally stable and resistant to the changes in integration patterns.

These initial growth experiments have laid the groundwork for extending MBE heteroepitaxial growth of QDs on Si for larger-scale in-plane monolithic integration schemes.

First demonstration of in-pocket QD growth on Si at 300-mm scale

The developed recipe was transferred to IQE, Inc. to perform direct MBE growth of the QD laser stack, with identical layer compositions including the Trapping Layer (TL) design, on patterned Si wafer with the in-pocket selectively-grown MOCVD template. The grown wafer is then diced into smaller pieces for characterization and device processing at UCSB.



Credit: Eamonn Hughes

Figure 4.4: Cross-section STEM of the in-pocket crystal growth across the pocket width. Pocket width is 20 µm. Credit to: Eamonn Hughes. Reproduced from [1]. ©MDPI 2023.

Figure 4.4 is a cross-section scanning transmission electron microscopy (STEM) of the in-pocket cyrstal growth across the pocket with a pocket width of 20 µm. The central region shows a flat-top epitaxial stack that is comparable to planar growth and ready for ridge waveguide fabrication with electrical contact. We have observed general consistency in the MBE stack thickness across the same 300 mm wafer regardless of the various splits of pocket widths, lengths and local pattern densities, which demonstrates the low geometry dependency of growth rate with MBE. The successful knowledge transfer from MBE

laboratory of a university research facility to a 300-mm MBE system in a commercial facility shows the robustness of growth conditions and feasibility of scaling heteroepitaxial technology for photonic integration with MBE [1]. The threading-dislocation density (TDD) in the active region of this sample was estimated to be roughly 4.8 $\times 10^7$ cm^{-2}.

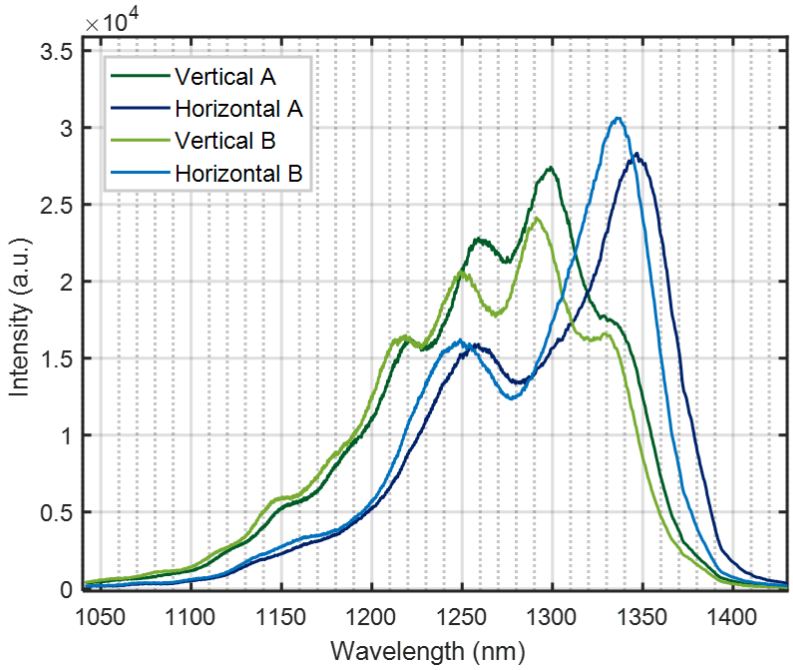


Figure 4.5: PL characteristics of in-pocket QD growth from different pockets of the same 300 mm wafer. Reproduced from [1]. ©MDPI 2023.

We perform photoluminescence (PL) measurement for the in-pocket material, using the same setup as the one in Chapter 3. Figure 4.5 shows the PL characteristics across different pockets of the same wafer. Strong PL around 1200 nm to 1350 nm can be observed at all pockets, covering the target wavelength around 1300 nm for O-band

[1]In subsequent growths of different wafers with several generations of design in this project, we do observe layer thickness variation and QD quality variation, and the difference will be briefly discussed in Chapter 4 during in "Development of mesa etch" and also in Chapter 6 in "Other factors that affect QD PL". Nevertheless, following the first demonstration of 300-mm in-pocket QD growth with O-band PL, all the wafers from this project that were received and characterized at UCSB facility have demonstrated satisfying QD PL despite the slight variations.

applications. PL variations across different pockets are also observed, with ground state peak variation about 20 nm and the close proximity of multiple excited states. This variation is also attributed to a difference of local temperature on wafer, similar to that of the 300 mm MBE growth on a blanket GaAs/GaP/Si template in Chapter 3. Here, the material configuration of the patterned Si wafer with pockets is believed to increase the variation due to the complication of thermal conductivity from the thick oxide on surface as well as the gradually deposited polycrystal during growth, and slight local variations on the die from the wafer may also occur from the varying in-pocket temperature due to different local pattern fill-factors and pocket widths.

In the plot, "vertical" and "horizontal" indicate two orientations of the pockets on the wafer orthogonal to each other. With the project moving forward, we observed a recurring trend of PL difference from the pockets in these two different orientations, which was later found out to be a QD growth dependency related to the anisotropic diffusion of the adatoms [3]. The detailed explanations of the pocket designs with relation to the wafer orientations and the observed PL dependency will be discussed in Chapter 6, together with other factors that affect the QD growth uniformity and the implications on large-scale monolithic integration through heteroepitaxy.

Nevertheless, QD PL of comparable intensity is observed across the 300 mm wafer, with pocket "A" and "B" in the plot located roughly 150 mm apart on the wafer, demonstrating monolithic integration of QD on Si using MBE as a scalable approach. The variations can be tailored with a more profound comprehension of QD growth condition dependency on pocket geometry, and further applications such as on-chip tunable lasers or laser arrays with groups of wavelengths of a wide tuning range may become achievable through careful engineering.

4.3 Process development for post-MBE growth polycrystal removal

4.3.1 Challenges with polycrystal in device fabrication

A main difference of the in-pocket sample growth, compared with QD growth on blanket template, is the polycrystalline deposition on the side walls of the oxide pockets as well as on the top surface, as shown in Figure 4.6.

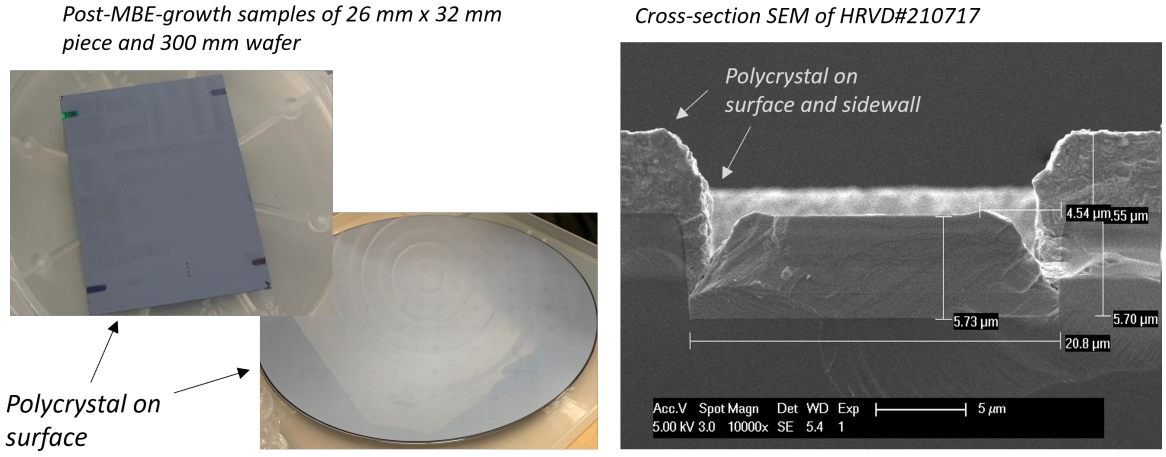


Figure 4.6: Post-MBE-growth samples with polycrystal on sample surface and pocket side walls.

This has caused a few major challenges for direct fabrication: (1) alignment: The polycrystalline surface becomes non-transparent, yet covers the alignment markers of underneath layers (in SiN layer or Si layer) for alignment to the pre-defined passive components and the pockets; (2) focus and exposure: the height difference between the top of polycrystalline surface and the bottom of the pocket is as much as about 8 µm, which creates major difficulty in managing focus and exposure in lithography.

Figure 4.7 shows cross-section after development of a bi-layer patterning for metal

deposition and lift-off using PMGI SF15 as the underlayer and SPR 1.8 as the upper layer photoresist. The SEM on the left shows how the opening and undercut looks like with a normal planar wafer. On the right, it shows the results from the same bi-layer coating inside a narrow and deep pocket. The PR fills in the pocket during spin-coating and creates non-uniform thickness inside and near the pocket, and the thickness also varies for both the PMGI and the SPR layers in different ways due to their different viscosity. The same exposure and development was not able to fully open the thicker photoresist inside pocket, and the underlayer is completely not opened regardless of additional DUV flood exposure and development time, due to the incomplete opening of the top photoresist layer.

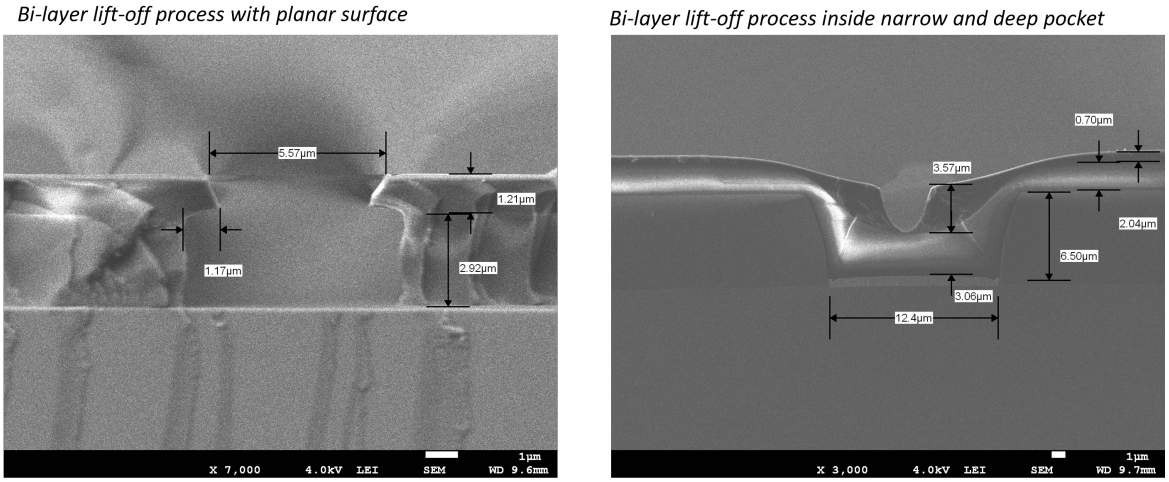


Figure 4.7: Cross-section SEMs showing effect of the high aspect-ratio pocket geometry on bi-layer photoresist thickness.

One way to address this problem is to proceed with an etched window using some corners of pockets for alignment to reveal the markers, and then use experiments to

re-calibrate the actual in-pocket focus and exposure with the extra polycrystal layer.

Some experiments were conducted to recalibrate the focus and exposure using samples with empty pockets to simulate the thickness variation and aspect ratio of the post-grown sample with polycrystal. In the Figure 4.8 below, the left two SEMs show the difference in pattern opening for different pocket width for the same recipe, as a wider pocket faciliate a thinner in-pocket photoresist thickness, and will open the underlayer more. This means the calibration would need to take into consideration the width distribution of different pockets on the same sample, and perform local adjustment of the exposure pattern, or pick a preferred number to sacrifice total yield. However, the opening is still much smaller than the dimension designed on-mask, and the curved shape is undesired for making structures with deposition and lift-off. In order to fix the pattern size, a longer exposure time needs to be applied to fully expose the thicker photoresist, and the SEM on the right shows the resulting bi-layer opening with undercut using double the original exposure time, which is one way to "fix" the pattern with series of recalibration.

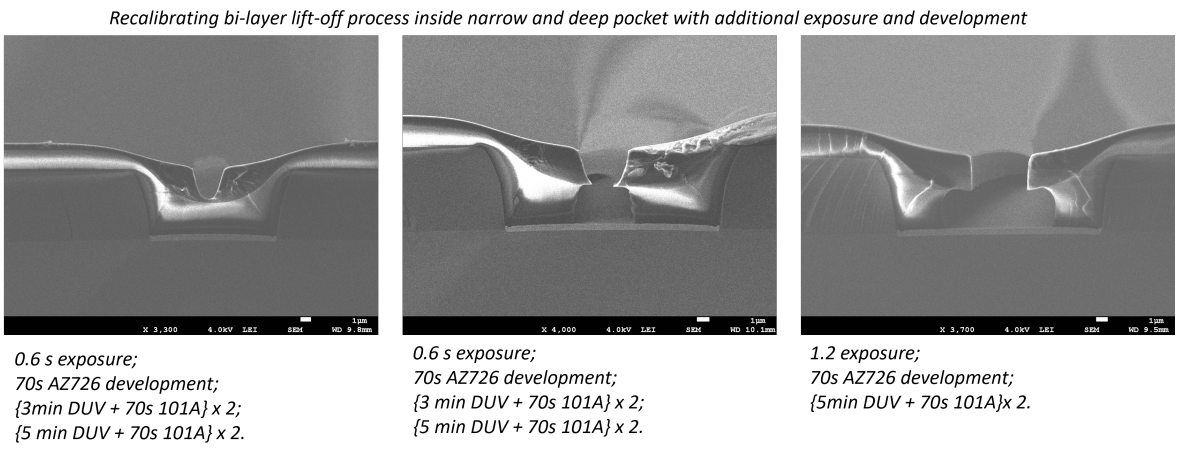


Figure 4.8: Cross-section SEMs showing bi-layer PR exposure and development result with different parameters, in an attempt to recalibrate for high aspect-ratio pocket geometry.

However, as one could tell, it is a non-trivial task to list out the relationship of the

photoresist thickness inside and outside pockets for each pocket design, and the spin-on thickness also changes as the in-pocket geomtery changes throughout the fabrication process - such as a difference of p-contact with pattern focal plane on top of mesa, n-via with pattern focal plane on bottom of mesa, or even layers like probe metal which links from inside to outside pockets covering territories with changing photoresist thickness.

In order to minimize the complication involved, it appears apparent that a process to entirely remove the polyscrystalline materials on top of sample surface would be the best choice to move forward. The illustration shown in Figure 4.9 visualizes the additional polycrystal removal and planarization step to prepare the wafer before proceeding to actual in-pocket device fabrication.

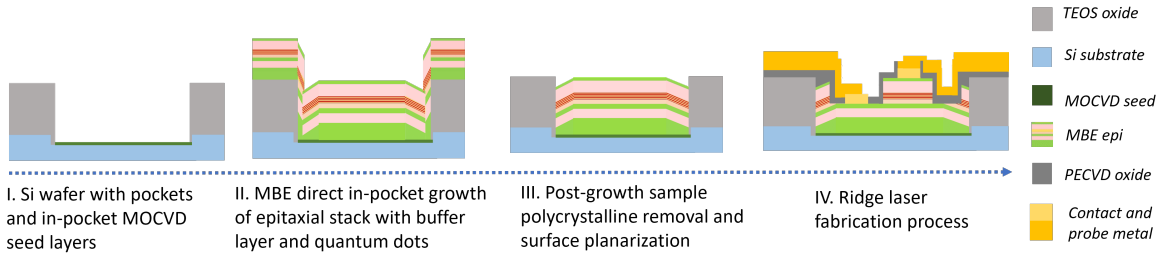


Figure 4.9: Schematics of processing flow including post-growth polycrystal removal and surface planarization prior to in-pocket device fabrication.

4.3.2 Wet etch polycrystal removal

The polycrystalline material is composed of a similar composition of the III-V crystalline stack grown inside the pockets, which contains alloys of AlGaAs, GaAs as well as some InAs/InGaAs components.

The most direct way to remove III-V anisotropically with a known pattern is to use dry etch with a known chemistry like a Cl_2/N_2 etch similar to how the ridge waveguide mesa is defined. However, the polycrystalline thickness of over 4 µm makes it risky to

go through a full dry etch, since the long etching time required may cause a build-up of unwanted residues, especially as it is likely to pile up at the line of pocket sidewalls. Also, such a long etch may require thick oxide hardmask, thick photoresist softmask, or a specific metal hardmask with very high selectivity for protection, which all adds to the complication.

An alternative is to use wet etch with a controlled etch stop mechanism to selectively remove the polycrystalline material yet leave the crystalline inside pocket intact with no additional damage or surface roughening.

A self-aligned PMGI mask protection method is designed here to protect the in-pocket material for a controlled wet etch, as shown in Figure 4.10. The process is described as follows:

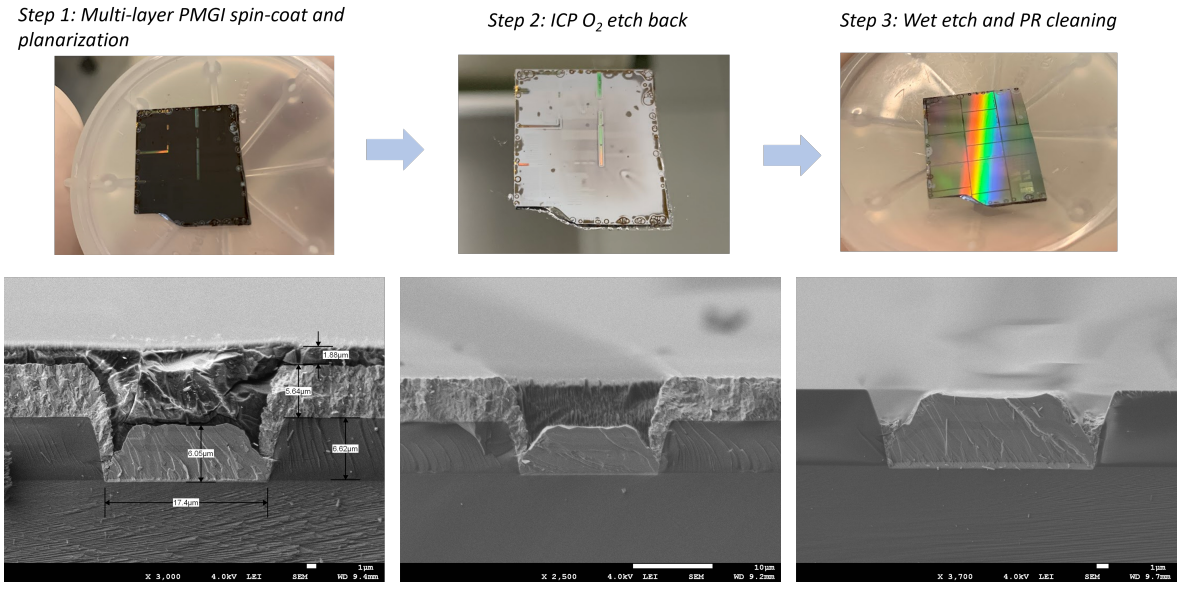


Figure 4.10: Wet etch polycrystal removal with self-aligned PMGI mask.

Step 1: Multi-layer PMGI spin-coat and planarization

A total of four layers, including one layer of PMGI SF3 followed by three layers of PMGI SF15 are applied. Each layer is applied to the sample surface with spin coating with 3000 rpm for 30 s, and a soft bake of approximately 200 °C for about 2 minutes is applied after each layer. The thinner SF3 provides better planarization as the initial layer, and the multiple layers of SF15 will further build up the fill above the sample surface.

After all layers of soft bake, the hot plate is gradually raised to 275 °C and kept for about 30 minutes or more for a hard bake of the sample. After the hard-bake, the sample surface should look planarized, with bubbles only at the edge of the sample piece. The "Step 1" in Figure 4.10 shows the top view of the sample after the hard bake as well as a cross-section SEM showing the planarized multi-layer PMGI covering over the top surface of the polycrystal.

Step 2: ICP O_2 etch-back

An oxygen-based dry etch was used to etch back the planarized PMGI top surface to reveal the polycrystalline top surface, and leave the PR inside pocket only as the protective pattern. The etch stop is controlled by *in-situ* laser monitor pointing towards the larger area sample top-surface as the reflected wave interference trace flattens when the PMGI at monitored area becomes fully removed. Figure 4.11 is a screenshot from the laser monitor software showing the etch trace flattens from about 290 s, and the reaction is stopped right after. "Step 2" in Figure 4.10 shows the top view of the sample after the monitored etch, revealing the polycrystalline surface across wafer. Note that due to the rippling of photoresist from spin-coating, there's thicker coatings near the edge of sample yet leaves some areas still covered in photoresist after the dry etch. This

usually wouldn't affect the following lithography or processing. The cross-section SEM shows the preserved PMGI inside pocket for protecting the crystalline epitaxial material during the following wet etch.

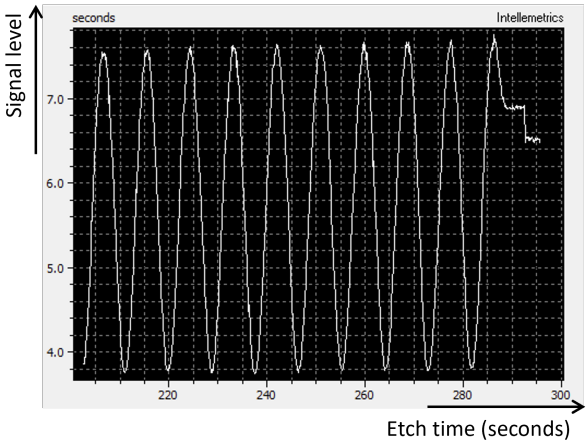


Figure 4.11: *In-situ* laser monitor trace for PMGI etch-back with ICP #2.

O_2 Etch Recipe using ICP (Panasonic E640)			
Flow-rate (sccm) for O_2	Pressure (Pa)	Bias (W)	ICP (W)
20	0.5	100	900

Table 4.1: O_2 etch recipe using ICP (Panasonic E640).

After establishing the self-aligned PMGI mask protection, now it is safe to perform a wet etch to react with the revealed polycrsytalline material.

Step 3: Wet etch and PR cleaning

The wet etch solution used here is a mixture of diluted phosphoric acid (H_3PO_4) and hydrogen peroxide (H_2O_2), which is known to react with alloys of AlGaAs and GaAs with different Al contents [4, 5, 6, 7]. The ratio is chosen as H_3PO_4:H_2O_2:H_2O = 1:4:45 (by volume) for a suitable etch rate and for timely etch stop control.

The reaction is performed with the solution mixure in a clear beaker with the sample being held by a teflon holder. It could be done in a timed manner, yet it is better to constantly observe the sample surface and watch a surface clear-up that marks the finish of polycrystal removal, then rinse in water promptly and thoroughly to terminate the reaction. The cleared-up sample surface is shown in "Step 3" in Figure 4.10.

The total reaction time is around 12 minutes until the surface clears up. Sometimes, an additional 15 or 30 seconds would be needed until some local grains of polycrystal finally clears up. This is done with cycles between microscope inspection and short intervals of reaction. The total reaction time may fluctuate due to to different sample growth conditions or sample sizes.

After completion of the polyremoval wet etch, the remaining PMGI mask is cleaned off with 5 mins of DUV flood exposure followed by 2 mins of AZ726 developer soak and consequent water rinsing. A cross-section SEM of the finished sample with mostly only in-pocket polycrystal remaining is shown in the bottom of "Step 3" in Figure 4.10. Since the top surface of the epitaxial layers is designed to roughly line up with the top of oxide surface, the sample now has minimal depth variation across the surface, and is ready for in-pocket device fabrication.

Comments on the wet etch polycrystal removal process

Alternatively, one can use photoresist with a lithography step to define an inverse pattern of the pockets on sample, and expose only the areas outside the pocket, leaving photoresist protection inside pocket. The alignment can be done using locations of corners of pockets, considering that the original markers in SiN or Si waveguide layers are still covered and the alignment tolerance in this step is slightly better than the later laser fabrication steps.

We switched to this lithography patterning method for a later generation (testsite

"Lincoln", or shorten as "LICN" [2]) of small-sized sample (26 mm x 32 mm) fabrication, since there was severe PMGI bubbling showing up after Step 2 of hard bake through-out sample. The actual cause of bubbling was unsure, since all preparation steps were kept identical and it had always worked for previous generations. It is suspected that it may be because that the "Lincoln" pattern has a different/higher III-V fill factor across sample, or that because it has different template and total stack thickness due to growth-rate non-uniformity for the MOCVD initial template (an issue that will be discussed later in Chapter 6) that causes near-pocket end material to curve up and create a difficult surface topography for planarization. Slower temperature ramping and many other methods were tried to mitigate the problem, yet little progress was made to prevent the bubbling after the temperature comes as high as 275 °C. Figure 4.12 shows an example of the bubbled surface, and the rework with slower temperature ramping. Nevertheless, the lithography method worked just as great as a patterned photoresist mask and either way the sample is readily protected and prepared for the polycrystal removal wet etch.

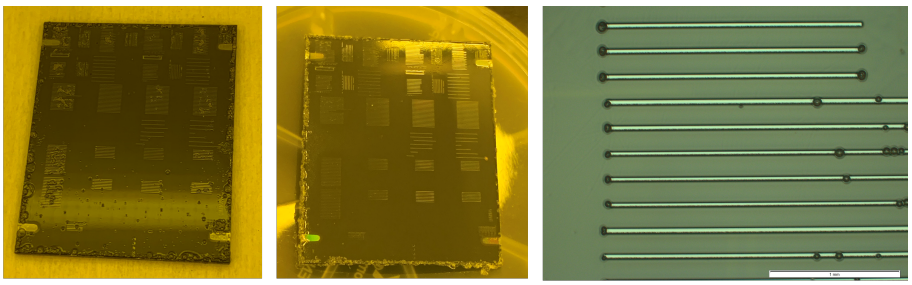


Figure 4.12: Examples of PMGI bubbling from hard-bake.

It is worth notice that this method provides a reasonable management for both underetching or overetching. For underetching, cycles of inspection and additional etch can

[2]A brief review of the project testsites and design generations will be included in the beginning of Chapter 6.

be easily performed as described earlier. For overetching, since the liquid would start reacting with the sidewall materials through the edges of the self-aligned PMGI mask if left for long enough time, it raises the concern of potential damage of the cyrstalline laser stack inside the pocket. However, assuming fully isotropic wet etch and a steady penetration, it would take at least a few minutes to leak through the sidewall polycrystal, which is beyond the etch-stop range that can be controlled with human reaction time - which will be in terms of seconds, at most.

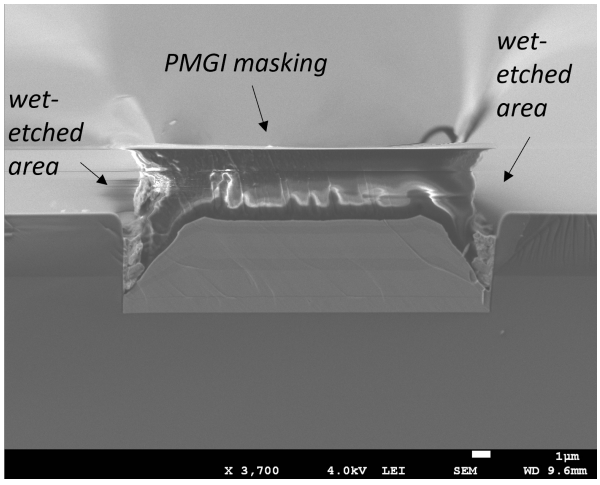


Figure 4.13: Cross-section SEM of the wet-etch result with self-aligned PMGI masking.

Throughout different generations of sample fabrication, there has been cases where the sidewall polycrystal was partially removed during the wet etch with minimal over-etching, as shown in Figure 4.13. Such over-etch could actually be preferable, as it helps clear the pathway for efficient on-chip butt-coupling from laser to SiN waveguides at pocket ends. However, as it was tricky to precisely control the sidewall etch and protect the in-pocket material, this idea was put aside. More rigorous approaches to re-engineer the coupling region will be detailed in Chapter 5.

The wet etch approach to polycrystal removal is efficient as it selectively removes

only the polycrystal outside the pockets with a reasonable tolerance and controllable reaction termination. It is a process that has been repeated with almost no failure throughout different generations of device fabrications. The etching chemistry itself is non-selective for stack compositions of different Aluminum content in AlGaAs/GaAs cladding layers, which makes this process straight forward, since no layer-by-layer etching and inspection is needed. Additionally, the wet etch approach is in general more tolerant to polycrystalline thickness variation across surface compared to dry etches, which can be a problem, for example, for MOCVD growth where the growth rate can be more sensitive to fill factors.

This process has been tested with sample sizes of 26 × 32 mm (single die size) up to 52 × 64 mm (two-by-two making four dies). There were some minor issues for clearing up to corners with samples that are more rectangular than square-like, mostly from PMGI rippling and thickness variation at the sample corners due to uneven spinning.

The wet etch process itself is technically achievable at a 300 mm scale, however, there can be many potential handling issues for the wet etch control. To develop a more scalable process for processing 300 mm wafers directly, another method of polycrystalline removal will be discussed at the next section.

4.3.3 Chemical-mechanical polishing

Chemical-mechanical polishing (CMP) is a method widely adopted in semiconductor fabrication for surface planarization and topography removal. The process, once developed, is naturally suitable for processing wafer at a larger scale. However, unlike a more common scenario such as oxide thinning and planarization on a 4-inch Si wafer, minimum research work or readily developed process can be found for etching uneven polycrystal of AlGaAs/GaAs mixture with a high thickness of around 4 µm and different patterns

throughout the wafer surface, and requiring a precise etch-stop within approximately the scale of 100 nm. Here are examples of some main challenges to develop this process from scratch:

(1) Finding the best chemistry (slurry) for AlGaAs/GaAs removal;

(2) Process development for the chemical reaction speed (slurry flow rate settings) and mechanical polishing force (pressure settings) to maintain the best processing result with a smooth surface;

(3) Etch-stop control to ensure no over-etching of the oxide fence as well as the in-pocket polycrystalline material;

(4) Residue control to ensure (a) no scratch marks from particles trapped on sample surface during polishing and (b) no dried-out particles from slurry or reaction products fall into the in-pocket crystalline top surface.

Some initial efforts have been paid to develop the CMP process at UCSB Nanofab facility with the Logitech Chemical-Mechanical Polisher. Small pieces of GaAs dummy wafers of size around quarter of a 2-inch wafer were mounted on 4-inch Si carrier wafers (one piece on one wafer at a time) using wax-mounting and the Logitech WBS7 wafer bonder. Chemlox polishing fluid (product code "0CON-141") was used, which is a sodium hypochlorite (NaClO) based polishing fluid with a high pH, as described from the product vendor, "suitable for polishing GaAs, InP and similar semiconductors" [8]. Since the polisher at Nanofab was a shared facility for different materials, special care was taken with extra fluid flushing time for polishing fluid change as well as designated polishing pad and polishing plate to avoid cross-contamination.

Unfortunately, initial tests gave very slow etch rate of the GaAs dummy samples and severe scratches on corners of the mounted small piece. It is suspected that the nature of mounted small pieces made it harder to have efficient planarization compared to full 4-size wafers. There may be ways to get around it, but the efforts to develop this process

on small samples at a shared facility were paused.

On the other hand, the CMP process was fully developed at the processing facilities of our collaborator, SUNY RF, at a 300 mm scale.

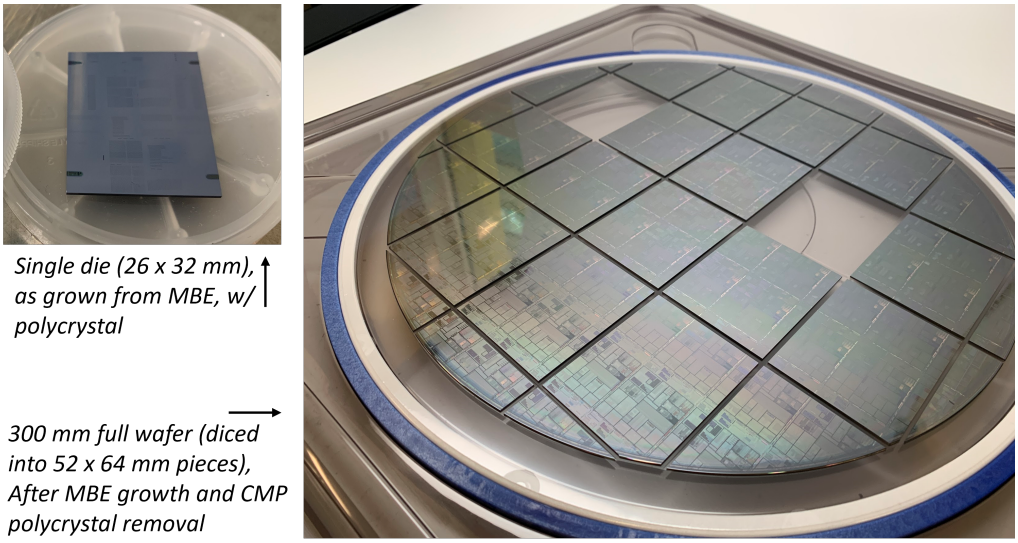


Figure 4.14: 300 mm wafer with full-scale MBE growth and CMP polycrystal removal, compared to the small-coupon growth before wet-etch polycrystal removal.

Figure 4.14 shows a 300 mm wafer with full-scale MBE growth at IQE Inc. and CMP polycrystal removal, compared to the small-coupon growth at UCSB that requires the wet-etch polycrystal removal as an CMP alternative. Full-wafer CMP process enables easy planarization and saves processing complications involved for the additional PMGI-masked wet etch steps.

However, there are still a few remaining challenges that were not unveiled until closer inspections were conducted later:

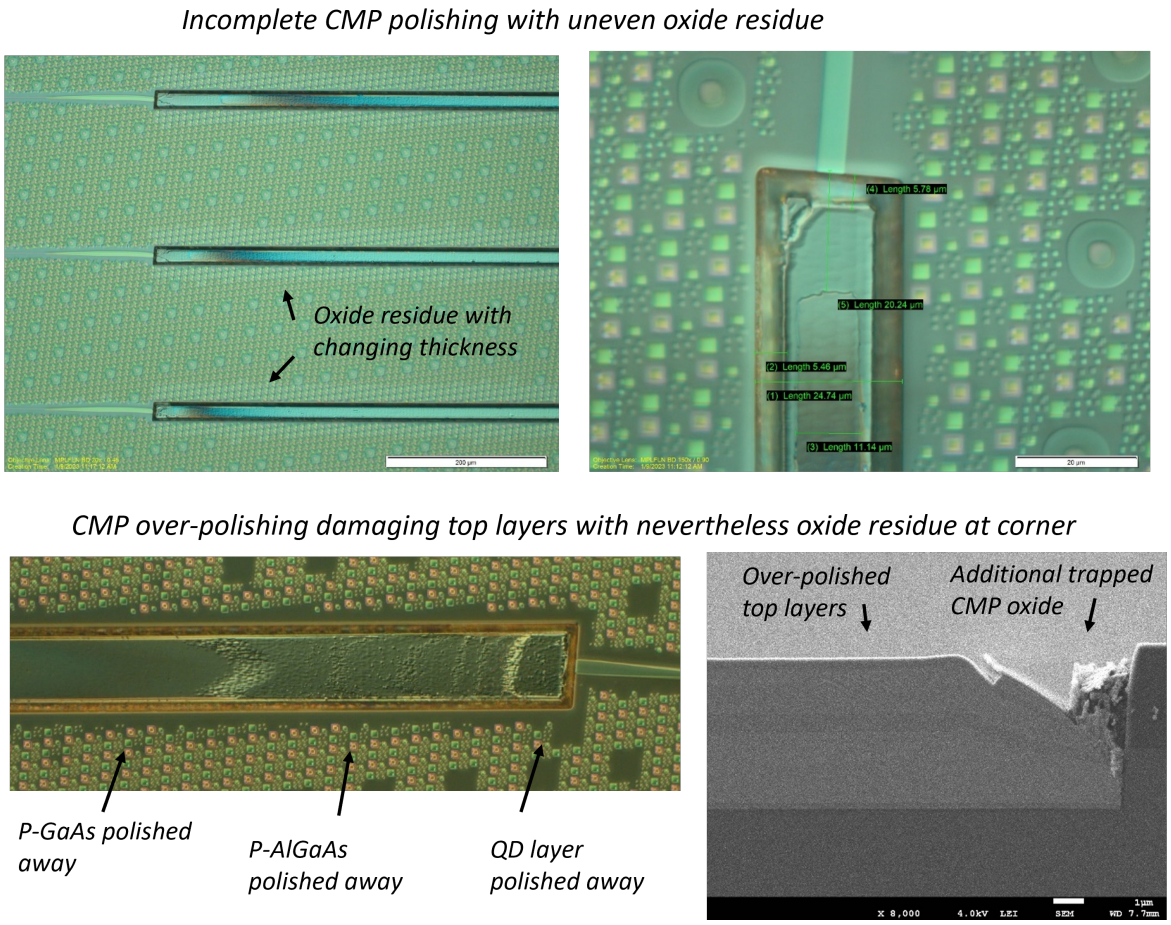


Figure 4.15: Remaining challenges with 300 mm CMP polycrystal removal.

(1) Thickness non-uniformity of the MOCVD template growth, translated into total stack thickness non-uniformity after MBE growth, has caused parts of the in-pocket stacks to pile higher than the oxide surface. In such cases, if terminate the reaction early to prevent overetch, there will be uneven CMP oxide left in center of pocket, as shown in the top two Nomarski microscope imgaes in Figure 4.15. If further polishing to clear the CMP oxide in center of the pocket, the CMP would clip off the popped-out area and damage the top GaAs contact layer or even deeper layers at parts where the stack is taller, as shown in the bottom row Nomarski microscope image. In addition, the

chemistry could leak into the high Al content AlGaAs cladding layer underneath GaAs layer and selectively overetch the AlGaAs p-cladding layer as well even if the layer height is below surface level, like shown in the cross-section SEM in the bottom row of Figure 4.15. Extra efforts to deal with this issue will be discussed in Chapter 6.

(2) There is trapped oxide at the corner in between the faceting III-V crystalline material and the polycrystalline deposition on sidewalls, like shown in the cross-section SEM just mentioned. This is the remaining part of filled oxide for CMP protection, and even with extra reaction time intended to clear off the oxide, the nature of CMP as a planarazation step still prevents the possibility of selectively remove the trapped oxide underneath the top surface line of the crystalline stack that is intended to be kept. The trapped oxide acts as potential "shadow masks" that would add additional difficulties when removing the faceting and side-wall polycrystal materials for engineering the coupling region. Detailed development regarding this will be discussed in Chapter 5.

4.4 Fabrication developments for in-pocket QD lasers

4.4.1 Overview of the fabrication process

The fabrication process after polycrystal removal is similar to that of the device on blanket wafer described in Chapter 3, yet requires additional development to deal with the high aspect ratio and narrow dimensions of the pockets. Figure 4.16 shows a general overview.

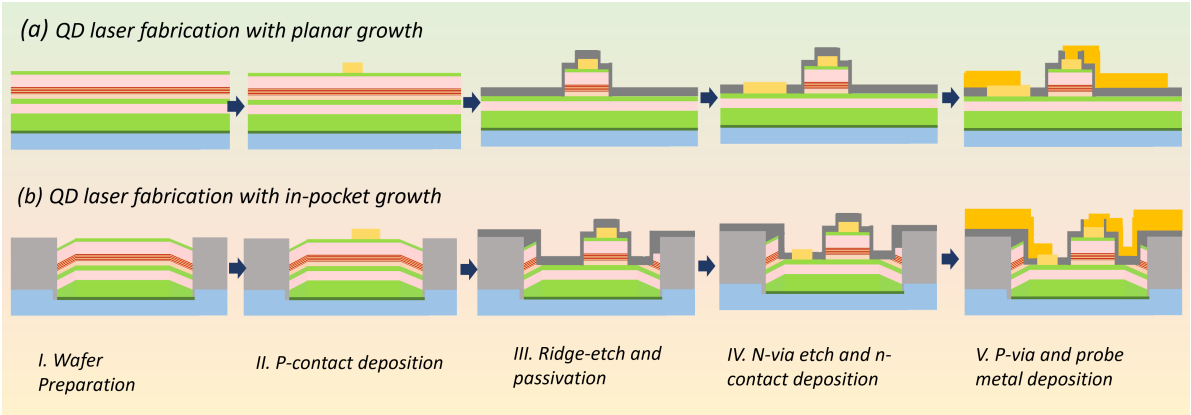


Figure 4.16: Fabrication process of electrically pumped ridge waveguide lasers on the in-pocket growth wafer (b) compared to that from the planar growth (a). Reproduced from [1]. ©MDPI 2023.

Several process development series were performed using dummy samples to dial in a new recipe, since it is usually required to cleave out and check the cross-section SEM to confirm satisfactory resulting structures. Complete iterations of device fabrication runs were also performed, and it was conducted in a parallel timeline with the growth development mentioned in section 4.2.2. Early fabrications were made with samples with no QD layers and were only to debug the process in development.

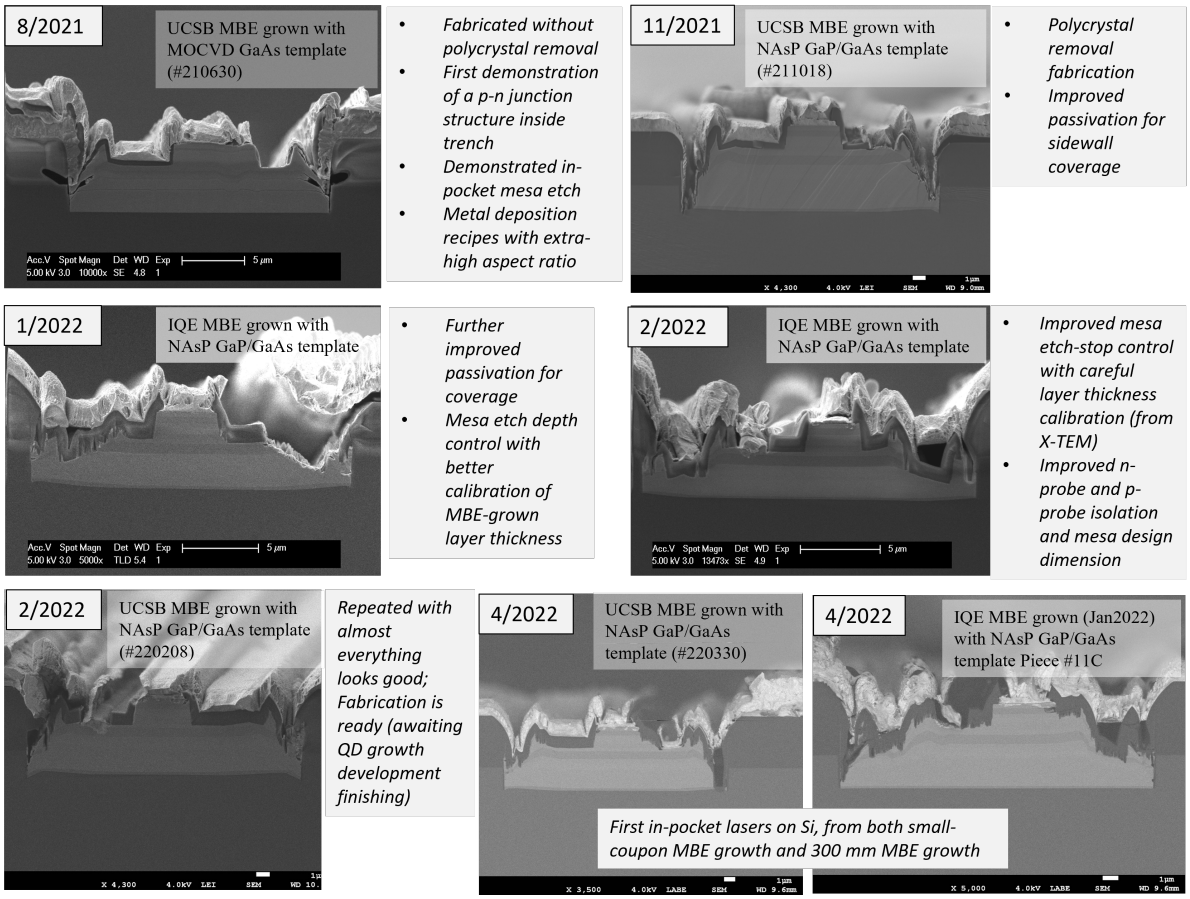


Figure 4.17: Cross-section SEMs of finished devices from seven fabrication runs from August 2021 to April 2022.

Figure 4.17 listed out the 7 fabrication samples that has gone through complete iterations from a long haul of development from August 2021 to April 2022. Early iterations revealed problems such as side wall passivation coverage, and mesa etch depth uncertainty from the MBE growth rate fluctuation. The sixth iteration of full fabrication (*#220208*) shows the repeated results from critical developments (especially mesa etch and passivation) and worked as excellent LEDs which marks the readiness for the fabrication, awaiting good in-pocket QD growth to make lasers, though in hindsight it still needs better management for the p-via dimension. Following that, the last two samples

(*#220330 and IQEJan22P11C*) successfully produced cleaved-facet in-pocket QD lasers for the first time. Table 4.2 lists out the fabrication issues encountered in each step and the corresponding developments.

This section will cover details of some major developments for the in-pocket laser fabrication process.

4.4.2 Developments for mesa etch

The mesa etch step that defines the ridge waveguide and exposes the n-type doped GaAs layer for making n-type contact alloy, poses one of the main challenges during the fabrication development.

The dry etch recipe is kept the same with the ones developed for making the QD lasers on blanket wafers as described in 3.4.2. When performing the mesa etch on blanket wafers, *in-situ* laser monitor was used for etch-stop control with the laser spot focused on the large opening area to be etched on sample surface.

On the ICP #2 tool, the laser monitor spot size is roughly 25 µm at the tool, and it is wider than the majority of the pocket width (20 µm) at our first generation of devices and impossible to be used for monitoring mesa etch inside the pocket. As a simple estimation, it would require a pocket width of at least more than 60 µm to have clear windows of width more than 25 µm, not to mention extra clearance that may be needed to provide sharp and clear traces from the reflected waves.

In this case, an alternative approach becomes needed for monitoring the etching process and confirming an etch stop at the n-contact GaAs layer. To the best of our knowledge, there is not efficient selective dry or wet etch for etch-stop of $Al_{0.2}Ga_{0.8}As$ versus GaAs that has been developed. Strictly timing the etch for an etch stop could be another option, yet the etch time variations from the same tool over different times as

Steps	Fabrication issues	Fabrication development
Polycrystal removal	Needs development for this additional step	Refer to previous section
P-contact deposition	Need to align to markers on passive layers (Si or SiN) from foundry fabrication with best possible rotational control	Consider marker placement for MPW combined mask at integration design phase
Mesa etch	Hard to monitor the epi inside narrow pocket with laser monitor to stop at 300 nm n-contact layer	Developed method of co-loading dummy blanket sample for precise etch-stop control
Passivation	Hard to passivate across rugged geometry across pocket edges	Developed protocol for adding extra fill passivation layer using PECVD with high power
N-via and n-contact	Dimension constrains from the narrow in-pocket flat region width risks potential shortage	Careful layer design and clearance parameters for enough distance to avoid shorting, with focus offset taken into consideration
P-via	General concerns about void formation and PR cleaning with extra thick passivation	Careful layer design clearance parameter along with proper focus offset to avoid extra widening, accurate passivation thickness monitoring to avoid excessive overetch
Probe metal	Hard to cover and route probe metal across height difference at pocket edges	Probe metal thickness and dimension for sufficient sidewall coverage as well as avoiding shorting, with additional probe metal "patching" or two separate probe metal depositions
Thinning and cleaving	Large die size and non-square dimension causes uneven substrate thinning, non-uniform pocket line-up adds complication for cleaving plan	Additional care for handling thick Si substrate, careful planning for predicing and order of cleaving lines

Table 4.2: Fabrication issues in each step of the in-pocket laser fabrication and corresponding process developments.

well as the strict requirement posed from the thin contact layer have made this option also less reassuring.

One way is to co-load a small dummy piece of the same epitaxial stack from on-blanket growth to use as a "monitor piece" for the etch trace during the actual sample mesa etch. Co-loaded experiments were performed with actual in-pocket growth samples, and several SEM cross-sections were examined at different locations of the same sample to ensure uniform etch depth even with different local epitaxial layer density (in-pocket with different pocket length and pitch variations on the same sample), and ensure uniform etch depth between the co-loaded blanket sample and the in-pocket growth sample.

Figure 4.18 shows the loading configuration. The dummy sample can be as small as about 5 mm $\times$ 5 mm for efficient use of material and reducing complications. In this fabrication run, another small piece of in-pocket growth was loaded as a sacrificial witness piece, and cross-section SEM was taken after etch to ensure complete mesa etch and accurate termination at the n-contact layer. The oxide etch depth monitor is loaded as well, for the purpose of careful calibration of resulting p-via oxide thickness described in 3.4.3 (b) p-via etch improvements. Each piece is loaded onto the carrier wafer with oil on the backside for fixation and efficient heat transfer, and it is advised to take special care especially for the small pieces to avoid oil overflow outside the sample edges which may cause contamination.

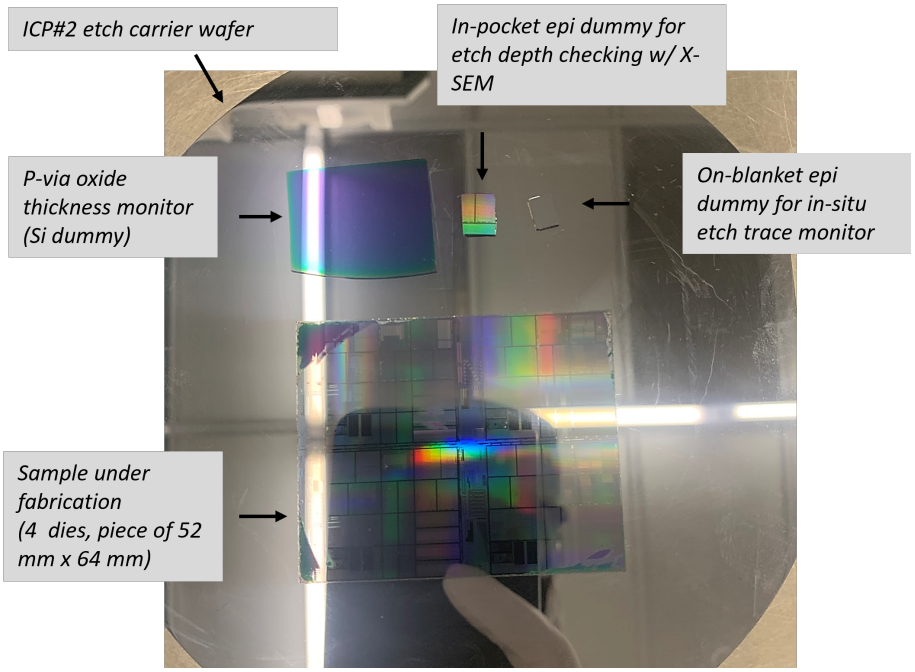


Figure 4.18: Loading configuration for the mesa etch using ICP #2.

Another concern is growth rate variation across different growth. Though MBE growth ensures uniform epitaxial stack thickness across different regions of the sample regardless of local pattern density, which is a dominating advantage for this monolithic integration platform, there are still thickness variations observed up to 200 nm - 300 nm of accumulated mesa etch depth difference across samples grown at different time even with the growth rate calibration performed periodically. Figure 4.19 shows the comparison of the layer thickness of the blanket dummy piece (from IQE 300 mm blanket growth) measured through STEM and the layer thickness from a given IQE 300 mm in-pocket growth measured in FIB SEM, and the table 4.3 shows the accumulated mesa etch depth difference from the measured numbers and that compared to the designed layer thickness. The relevant scale of thickness variation can be informed even taking into consideration the minor inaccuracy for thickness measurement through SEMs. Since

the n-contact layer is as thin as 300 nm, such variation of thickness (and the resulting thickness difference between the in-pocket sample under fabrication and the co-loaded on-blanket dummy sample) may cause an overetch. It has become a practice to perform a FIB cross section SEM on the in-pocket sample for calibration of layer thickness, and use that as a guidance for earlier etch stop or later etch stop when monitoring with the co-loaded on-blanket dummy epitaxial sample.

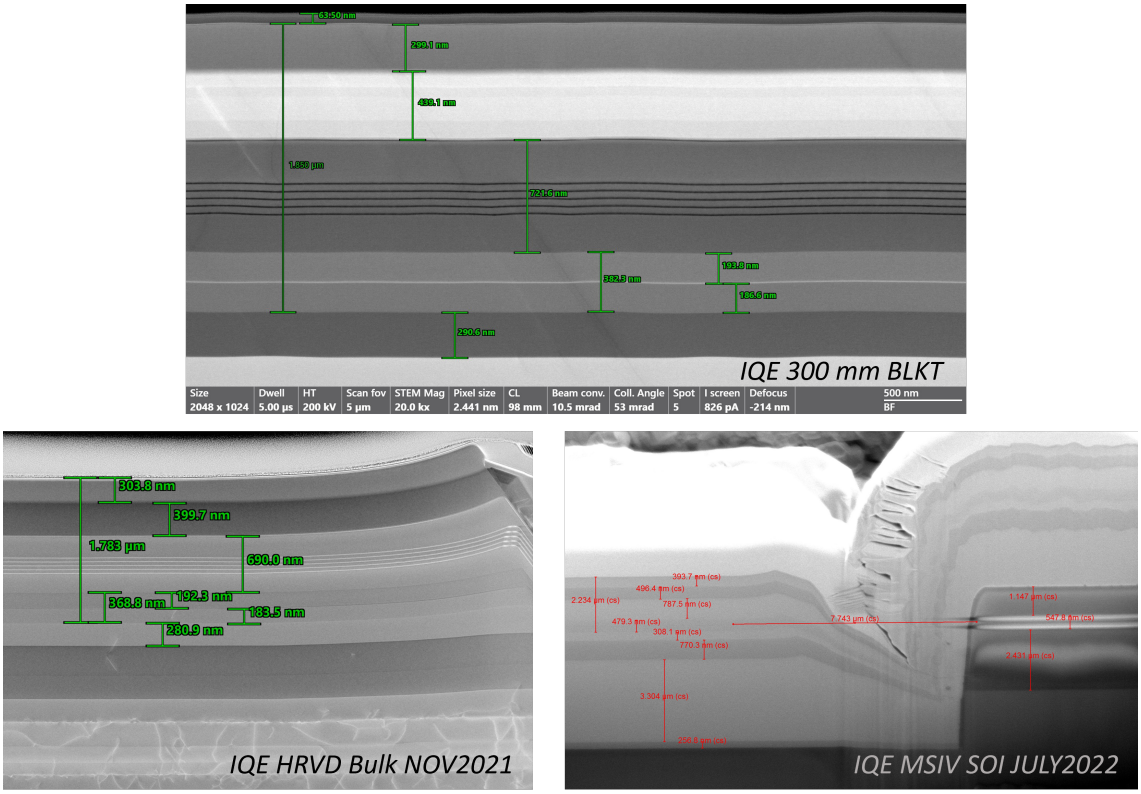


Figure 4.19: STEMs and FIB SEM images showing in-pocket stack with different layer thickness inconsistent with the design, for both 300 mm growth and small-coupon growth.

Additionally, it becomes clear that although it would be fine to stop the etch at anywhere in the 300 nm n-contact layer, it's always advised to stop right at the beginning to avoid consequences of over-etching due to etch-rate non-uniformity. Underetching is less of a concern than overetching, and the risk can be counteracted with effectively

Epitaxial layer (roughly)	Design	Blanket monitor piece*	In-pocket growth example(1)*	In-pocket growth example (2)*
p-GaAs contact	300 nm	299 nm	304 nm	394 nm
70 % p-AlGaAs and gradings	500 nm	439 nm	400 nm	496 nm
GaAs waveguides and QDs	685 nm	722 nm	690 nm	788 nm
20 % n-AlGaAs	400 nm	382 nm	369 nm	479 nm
n-GaAs contact	300 nm	290 nm	280 nm	308 nm
70 % AlGaAs	700 nm	-	-	770nm
Mesa etch depth (Top to n-GaAs)	**1885 nm**	**1842 nm**	**1763 nm**	**2157 nm**
Etch depth compared to design	**-**	**-43 nm**	**-122 nm**	**+272 nm**

Table 4.3: Designed layer thickness compared to measured layer thickness from three grown samples. *Blanket monitor piece corresponds to "IQE 300mm BLKT", in-pocket growth example (1) "IQE HRVDBulk NOV21", and (2) "IQEMSIVSOI JULY22".

the 15 seconds or 20% ever-etch of the following n-via etch step, as the remaining thin GaAs layer could be punched through with physical attack despite a selective dry-etch chemistry used in the n-via SiO_2 etch.

As a result, a small dummy piece with on-blanket wafer epi has been co-loaded for etching in-pocket materials, and with accurate epi layer thickness calibration and some extra care of the *in-situ* laser trace monitoring, it becomes a standard process to ensure a reproducible mesa etch for fabricating in-pocket ridge waveguide lasers.

4.4.3 Developments for passivation

The passivation step also needs special care due to the nature of high aspect-ratio process in the pockets, especially given the pocket width of the first few generations are mostly 20 µm, as shown earlier in the cross-section SEMs in Figure 4.17.

The passivation procedure for the on-blanket lasers in Chapter 3 was simply about 500 nm of PECVD SiO_2 deposition. For the in-pocket laser, an additional PECVD "fill" recipe is adopted to add an extra passivation layer. The recipe uses the ICP-PECVD (Unaxis VLR) tool [9] at UCSB Nanofab, and the fill recipe deposits at 250 °C with higher bias (450 W) compared to the normal recipes (15 W for Low-Deposition-Rate SiO_2 and 100 W for High-Deposition-Rate SiO_2 on Unaxis PECVD).

The conditions are listed in the Table 4.4 below:

SiO_2 Fill Recipe using Unaxis PECVD			
Temperature (°C)	Pressure (mTorr)	Bias (W)	ICP (W)
250	5.0	450	600

Table 4.4: SiO_2 Fill Recipe using Unaxis PECVD.

A few process development experiments were conducted to compare the oxide sidewall coverage from depositions through PECVD #2 standard SiO_2 recipe versus the Unaxis PECVD SiO_2 Fill recipe. Figure 4.20 shows comparison of the cross-section SEMs for in-pocket growth samples after polycrystal removal that have gone through either 35 mins (deposits about 1 µm on blanket surface) of PECVD #2 or 540 s (also deposits about 1 µm on blanket surface) of Unaxis PECVD SiO_2 Fill. The PECVD #2 oxide deposition shows a slightly higher likelihood to have void formation from piled up angled deposition, while the Unaxis PECVD fill recipe produces a more smooth and conformal coverage over the rugged sample surface.

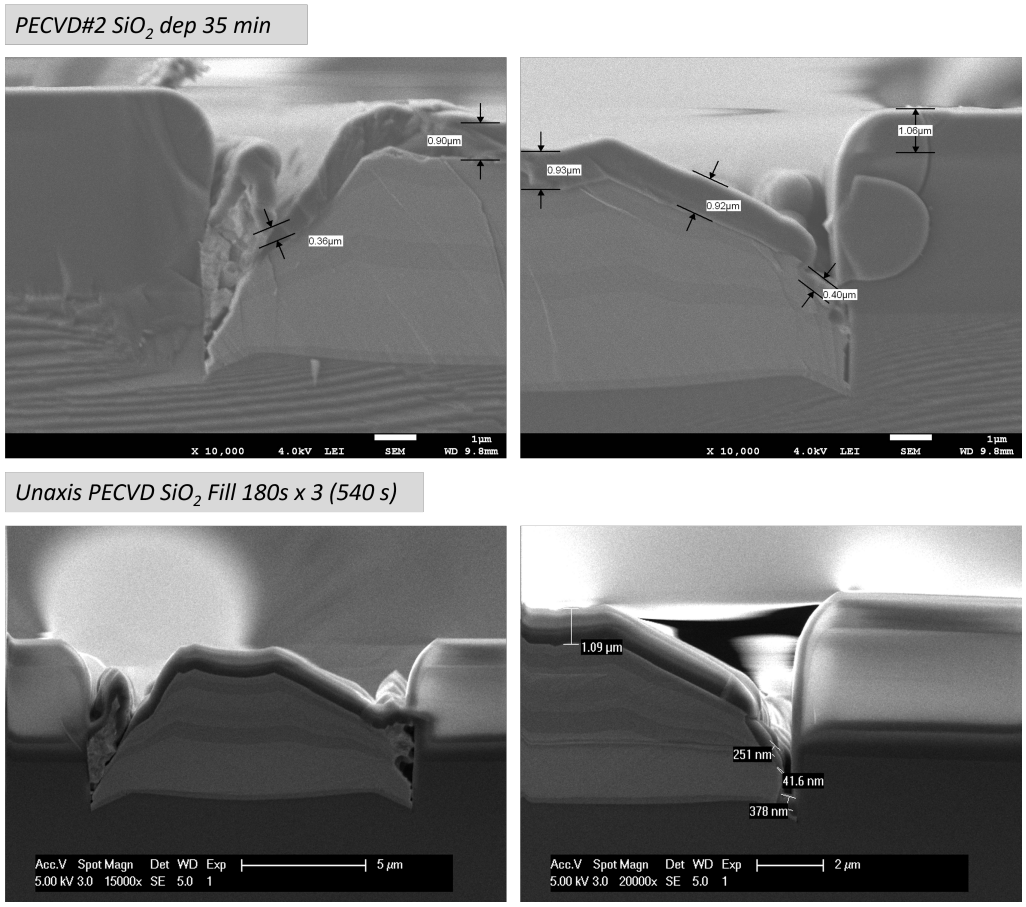


Figure 4.20: Comparison of cross-section SEMs for samples with either PECVD #2 oxide or Unaxis PECVD SiO_2 Fill depositions.

As a result, an additional 540 s of Unaxis PECVD SiO_2 Fill is adopted as a second passivation layer to smooth out the corners after the first 10 - 15 mins of PECVD #2 SiO_2 passivation. The finishing device sidewall coverage and smoothness has been improved, as can be seen in the later iterations (1/2022 and later) in Figure 4.17, and no related device shortage has been observed. For more details of the related fabrication procedures, please refer to the Appendix.

However, as more fabrication runs were conducted later on this project (including the ones for the topic of Chapter 5), it becomes more evident that the PECVD Fill

may not be the best choice also due to more cases of clear observation of its loading effect, as different deposition thickness was seen from different Si dummy samples (with different initial oxide thickness) that are loaded during the same deposition. There is also the changing thickness across different geometries of the in-pocket sample, which is a natural result of the "smoothing" effect with the high RF bias in the recipe, as the old saying goes "every medicine has its side effect". This step has been kept in the process as it has never truly caused any performance degradation or device failure, and it remains a "known working process" for dealing with the passivation across high aspect ratio surface and frequent small gaps when fabricating in-pocket lasers. After all, there is always limited time for limitless improvement that could be done.

An alternative to using the high-bias PECVD Fill recipe is to use Atomic Layer Deposition (ALD) instead, which is a well-known option to deposit uniform and conformal films layer-by-layer [10]. Considerations such as avoiding etch-rate uncertainty added to the n-via and p-via etches, limiting changes to the recipe in each iteration to avoid additional variables for process debugging, as well as some more untenable practical concerns such as the ALD tool availability at a certain late night window before reaching the scheduled series of tool slots for the next steps in fabrication have unfortunately so-far hindered me from exploring the option and developing an alternative step to use ALD as either the first or second passivation. Hopefully this extra piece of puzzle can be put in place soon.

In the future, for transferring the process to a 300 mm CMOS-compatible III-V fabrication facility, the oxide fill and planarization process should be readily available and there should not be much complication involved for post-etch passivation, fill and planarization.

4.4.4 Developments for probe metal deposition

Another obvious challenge that comes with high aspect-ratio pockets in small dimensions is the routing of probe metal. The probe metal layer used in the fabrication process in Chapter 3 is one thin layer of titanium (Ti) of 22 nm followed by a thick layer of 1.5 µm of gold (Au), deposited using E-beam Evaporation (E-Beam 4 (CHA) [11] at UCSB Nanofab) with bi-layer lift-off. The extra thickness of the gold layer and the planetary rotation fixture for a conformal deposition is used to ensure metal continuity when routing through the sidewall of the ridge waveguide. For the FP lasers on blanket wafer, the n-contact is extra wide in the order of 100 µm pad width, and the n-probe metal is pushed further for about 10 µm away from the n-contact edge to ensure a large gap between the p-probe and n-probe metal pads and avoid shortage due to the large bi-layer photoresist undercut and the deep deposition angle with planetary rotation.

For the in-pocket lasers with pocket widths on the order of 15 µm, 20 µm, or 35 µm, with about 6 - 7 µm of polycrystal and faceting area on each side, the flat area for the device mesa and n-contact region is much more limited. The n-contact width is shrunk to 3 µm or smaller, in some cases, and the n-probe metal needs to be pushed closer to p-contact. The clearance in design for reaching enough clearance yet making the best use of available geometry becomes an additional necessity, and the recommended dimensions will be listed out in the next section. For the record, it is possible to fabricate ridge-waveguide lasers within a pocket width as small as 15 µm, as the finished device SEM shown in Figure 4.21. The total flat area for fabrication is only 8 µm and the n-contact width is only about 1.5 µm, with a distance about 1 - 1.5 µm to the edge of the 4 µm mesa [3].

[3]This device has 45.6 mW of single-side CW power uncooled in RT, 3.98 % single-side wall-plug efficiency, and less than 2 ohm series resistance (device length is about 3.8 mm).

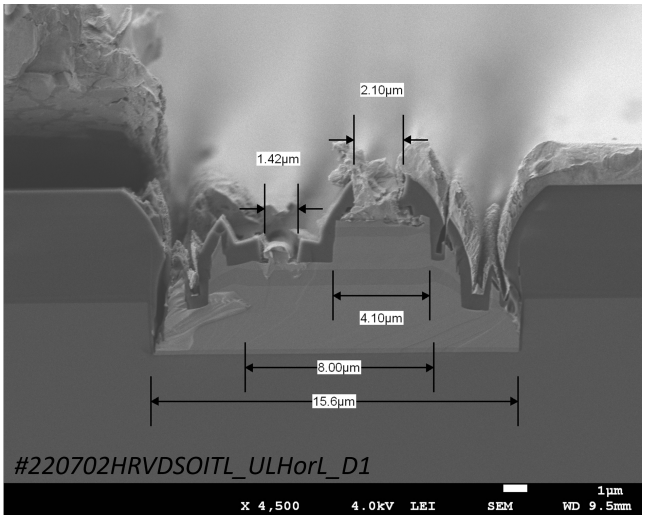


Figure 4.21: Cross-section SEM of a working laser in a pocket with 15 µm width.

In some cases, even with the conformal deposition with planetary rotation and 1.5 µm of gold, open circuit still occurs during on-chip preliminary device LIV screening, sometimes burnt open as the sweeping current increases. An additional "probe metal patch" deposition is performed with a patching mask opening where the open circuit happens, usually at transitions of pocket edge, or at n-contact edge in some runs when the total oxide thickness is very high. The patching metal is also 22 nm of titanium followed by 1.5 µm of gold. After patching, the device shows healthy LIV results and does not have any open or shortage with repeated testing. For example, Figure 4.22 shows the FIB cross-section SEMs of a device before and after patching.

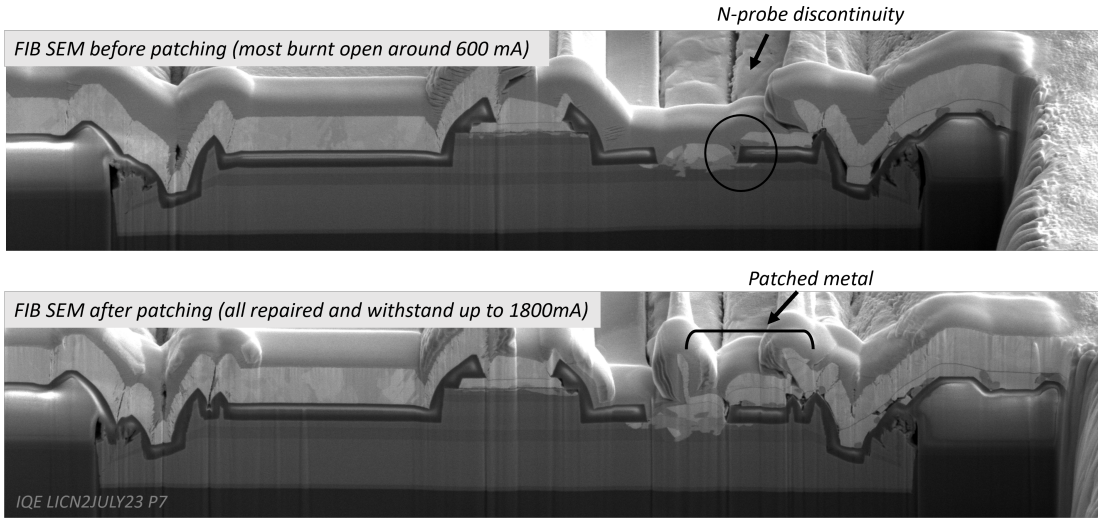


Figure 4.22: FIB cross-section SEMs of a device before and after additional probe metal patching.

As a conclusion from several iterations of different probe metal design and "patching" designs, it seems easier to separate p-probe metal and n-probe metal in two separate depositions so as to maximum the overlap of probe metal and contact metal without worrying about potential shortage or difficulty with lift-off when the gap between metal is too narrow. This has been adopted as part of the process follower in the Appendix.

4.4.5 Design guidelines for layer dimensions

Similar to that in Chapter 3, this section is aimed for providing a guidance of design parameters and layer dimension clearance for making ridge waveguide lasers in narrow pockets for monolithic integration.

We separate the case for narrow pockets (15 - 25 µm) and wider pockets (30 - 50 µm) here to take into account the priority of squeezing in limited footprint or having abundant clearance. As can be shown in Figure 4.23, the flat widths available for fabrication is about 10 µm or more further smaller than the pocket widths, especially if there is also

defect present on one side of the pocket, an issue we will cover in Chapter 6.

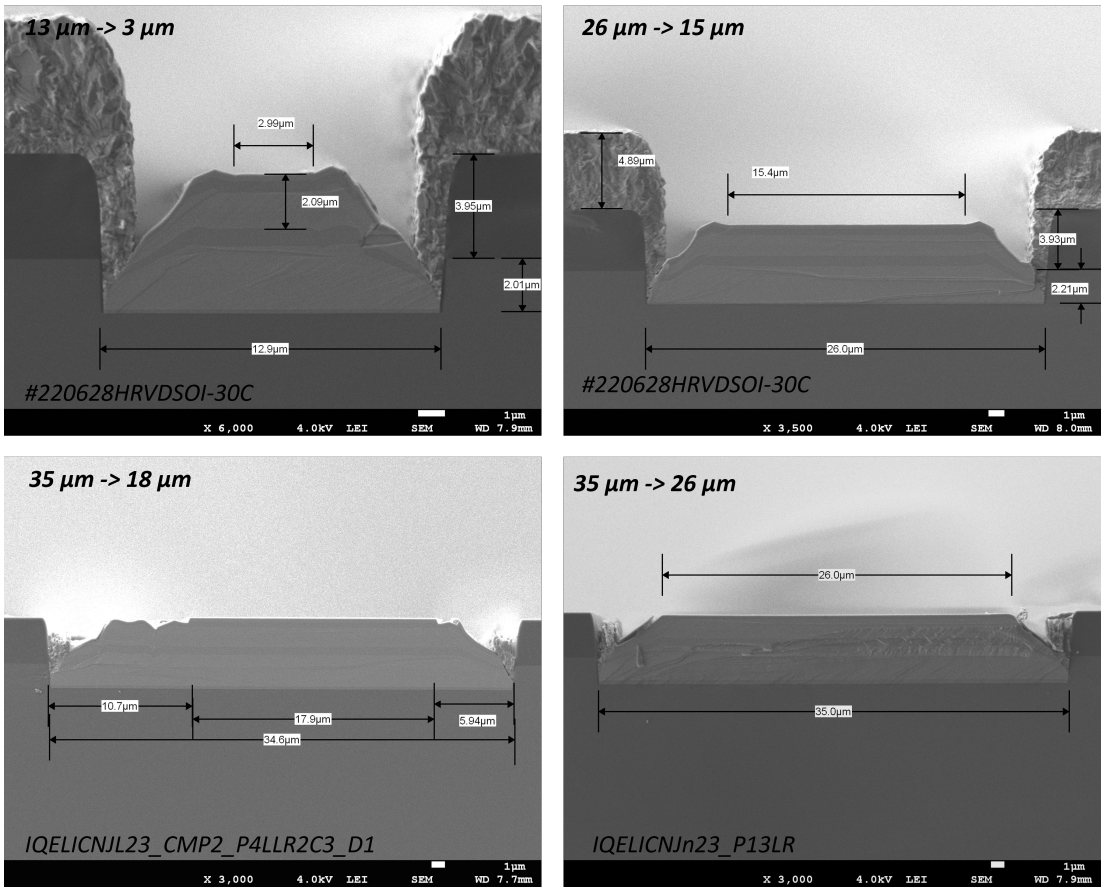


Figure 4.23: Cross-section SEMs showing flat-are widths available for fabrication with different pocket widths and conditions.

Despite the challenges, there have been satisfactory laser fabrication results from 15 µm, 20 µm, 23 µm, 30 µm and 35 µm pocket widths that have been incorporated in the few generations of integrated masks in this project. Figure 4.24 shows the cross-section SEM of fabricated facet of ridge waveguide lasers for a range of different designs, either off-center or at-center of the pocket.

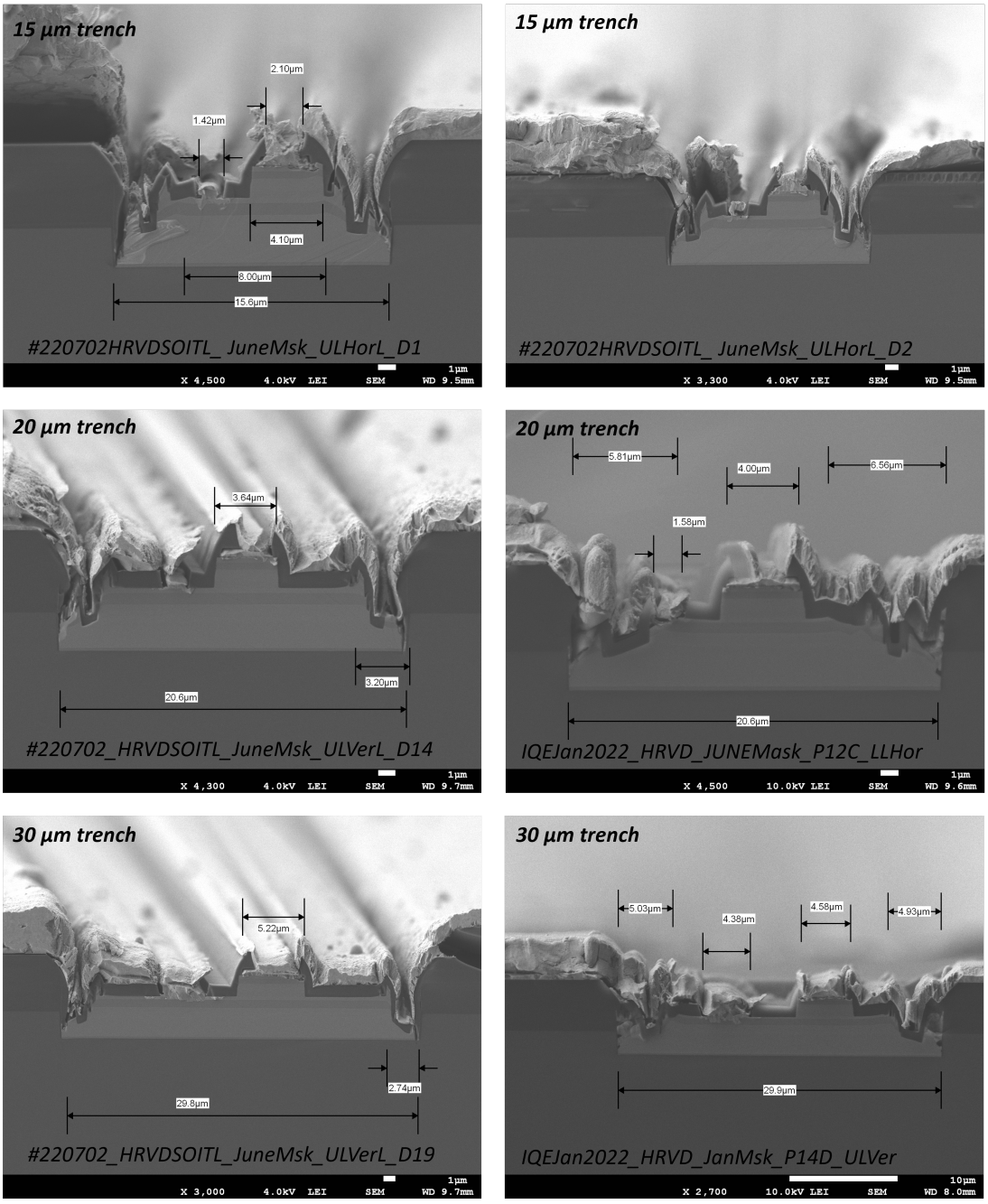


Figure 4.24: Cross-section SEMs of cleaved facets of ridge waveguide lasers for a range of different designs with pocket widths of 15 µm, 20 µm, and 30 µm.

Though many of the concerns of limited footprint for flat area for mesa and contact placement get lessened as the pocket dimension gets wider, the design considerations

and empirical practices can be advisory for general cases when developing multi-layer semiconductor processes for a given territory. Table 4.5 [4]and Table 4.6 [5]list out the recommended clearance numbers and reference design parameters from previous fabrications runs that have successfully yielded in-pocket lasers.

Layer dimensions for narrow pockets (15 - 25 µm)			
Suggested layer clearances on mask		Example of layer dimensions on mask	
-	-	P-contact	3 µm
Mesa outside Pcontact	0.5 µm each side (critical)	Mesa	4 µm
P-via inside P-contact	0.8 µm (critical)	P-via	1.4 µm
N-contact from mesa	2 µm (may further shift)	N-contact	80µm
N-via inside n-contact	0.2 µm (squeezed)	N-via	1.3 µm
Probe metal inside p-contact edge	? µm (critical)	P-probe metal	70 µm
N-probe metal away inside n-contact edge	0.5 µm (critical)	N-probe metal	70 µm

Table 4.5: Recommended clearance numbers and reference design parameters for narrow pockets (15 - 25 µm).

For the narrower pockets, the constrains imposed by the pocket width are very tight in relation to the footprint required for the ridge wavegude mesa, n-contact exposure

[4]Note on probe metal dimensions: during development for narrow pockets, we used the original probe metal mask with 10 µm distance to n-contact first, and added an n-patch probe metal using the same mask plate with n-contact and applied this manual shift. It was produced with Autostepper #2. The p-probe metal to p-contact edge distance number was lost in the processing notes at the time of writing (and remains specific to the alignment tool used here), and we encourage the readers to find out the answer themselves.

[5]Note on probe metal dimensions: during later fabrications, we realized the need for additional coverage on the n-contact side, as described in the development section earlier. The dimension of n-probe metal away inside n-contact edge here applies for the adjusted fabrication procedure with separate p-probe and n-probe metal depositions. For the detailed procedure, see Appendix.

and sufficient clearance for avoiding absorption loss or electrical shorting, which is also further complicated by finite lithography resolution and alignment tolerance.

For some narrow pockets, we had to shift the mesa away from pocket center for effective use of the flat region. If taken into production, the passive components aligned with the mesa for efficient in-plane coupling should be updated to accommodate this change. Double-side n-contact was no longer an option for further reducing of series resistance and increasing injection efficiency.

Layer dimensions for wider pockets (30 - 50 µm)			
Suggested layer clearances on mask		Example of layer dimensions on mask	
-	-	P-contact	4 µm
Mesa outside Pcontact	1 µm each side (critical)	Mesa	6 µm
P-via inside P-contact	0.8 µm (critical)	P-via	2.4 µm
N-contact from mesa	3 µm (may further shift)	N-contact	80µm
N-via inside n-contact	0.2 µm (squeezed)	N-via	3.8 µm
Probe metal inside p-contact edge	1.2 µm (critical)	P-probe metal	70 µm
N-probe metal away inside n-contact edge	1 µm (recommended)	N-probe metal	70 µm

Table 4.6: Recommended clearance numbers and reference design parameters for wider pockets (30 - 50 µm).

With the wider pockets beyond 30 µm, many of the previous constraints are alleviated. However, the requirement of p-via, p-contact and mesa dimension control with sufficient clearance remains significant for avoiding the void formation as discussed earlier in Chapter 3.

Another change here is the wider designed mesa width, set as 6 µm here. This was

partially a result of shifted focal conditions of p-contact as we switched to a new lithography tool, the Maskless Aligner (Heidelberg MLA150) which is harder to calibrate for a fixed focal offset for in-pocket fabrication during exposure given its continuous, automatic autofocus exposure scheme. The p-contact expanded wider than expected, measuring 5 µm when designed as 4 µm on the mask. We carefully inspected the dimension difference and expanded the mesa dimension wider as 6 µm to avoid overshadowing, especially since the mesa mask has a flipped polarity, and its dimension would shrink instead of expand if out of focus.

This is mainly a result from the switch of lithography tool, as the Heidelberg MLA provides more flexibility for mask design adjustment on the go. We anticipate that reproducing the narrow pocket results with designs aforementioned in Table 4.5 using MLA instead of Autostepper #2 will be challenging, and requires additional calibration and process development.

4.4.6 Comments on fabrication developments

We have conducted a series of process development addressing difficulties in mesa etch, passivation, probe metal and many other steps for making in-pocket ridge waveguide edge-emitting lasers with the "thin" epitaxial stack which leads to the first-demonstration of in-pocket QD lasers on Si with electrical injection. We expanded the working pocket range to 15 µm at the narrowest, and provided a variety of working devices for different pocket geometries for performance comparison. The fabrication iterations also provide insights into improvements of high-level integrated designs and pocket geometries for better yield and easier production. The learning process goes parallel with our efforts in improving fabrication quality of ridge waveguide lasers on planar substrates and can be extended to applications in other fabrication schemes.

Furthermore, a stable and reliable process reduces the uncertainty in device performance resulting from fabrication variations. This benefits statistical analysis on device performance as a direct reflection of epitaxial quality, facilitating effective learning and improvement in the growth aspect, which will be covered in the next section.

4.5 Measurement and results

4.5.1 Post processing for making cleaved facet lasers

To make the first demonstration of lasers grown in-pocket on Si, we proceed to post-processing in order to make cleaved facet lasers with the fabricated in-pocket ridge waveguides.

Although the III-V gain section is grown with the GaAs/AlGaAs material system, it is challenging to directly cleave the sample to create cleaved-facet mirror due to the thick Si substrate (approximately 780 µm), where Si has a diamond cubic crystal structure with strong covalent bonds between each silicon atom and its four neighboring atoms. This is different from devices made from common native III-V substrates (InP or GaAs, for example), which have zinc blende crystal structures with preferred cleavage planes where the bonds are weaker.

We use a mechanical polisher (Allied) [12] to perform back-side thinning of the finished sample. The polishing process was developed from previous research of QD lasers grown on Si substrate.

For the case of samples in this project, the first difference is the sample size. As shown in Figure 4.25, the die size is 26 mm × 32 mm and the patterned area is rectangular instead of square like, which poses difficulty of uniform polishing results and a smooth finish. The initial samples were finished precautiously at 200 - 300 µm thickness, and

roughness up to 30 µm - 6 µm. There were definitely concerns on the roughness and visible scratches on the backside placed unevenly, but we were able to make clear cleaves despite the imperfections. In the later batches, we were able to improve the polishing quality by pre-cleaving or pre-dicing the sample to smaller, more square-like pieces, and pushing the finishing thickness towards 120 - 150 µm and roughness within 1 - 3 µm.

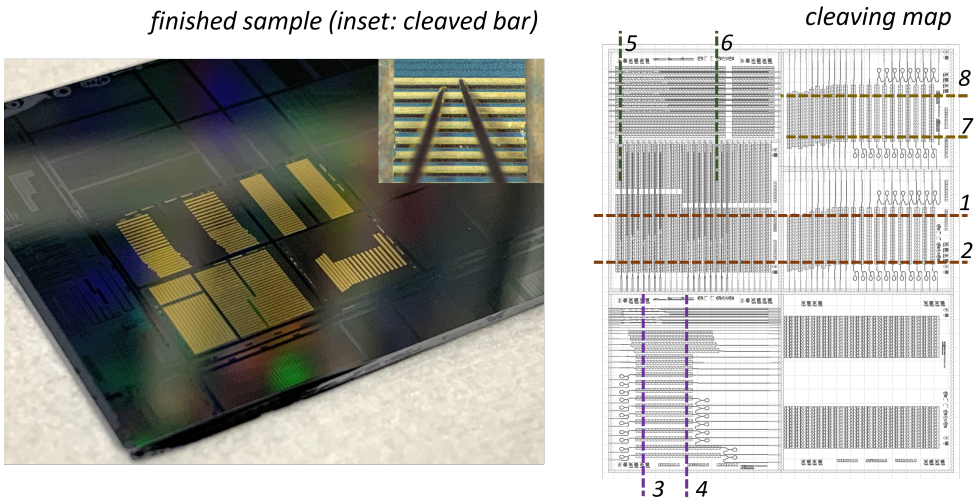


Figure 4.25: (a) A finished sample with die size 26 mm × 32 mm, inset showing a cleaved bar. (b) Cleaving map for a given waveguide arrangement with integrated design (in this case, for the test site "Harvard").

The second challenge is from the ridge waveguide arrangement on the sample. The patterning of the sample was originally designed to make gain sections coupled to external reflectors in the SiN or Si layers, and splits in designs of the passive components have caused variation of the gain section locations across the sample, making it hard to effectively plan out and cleave laser bars at any desired cavity length. Following the orders of cleaving lines shown in Figure 4.25, we were able to produce the following groups of bars, listed in Table 4.7.

List of cleaved laser bars from "Harvard" layout				
Bar	Cleave lines	Orientation	Device length	Pocket width
ULVerL	1, 2	Vertical	1.5 - 1.8 mm	15, 20 and 30 µm
URVerD	1, 2	Vertical	1.5 - 1.8 mm	20 µm
LLHor	3, 4	Horizontal	1.8 mm	20 µm
ULHorL	5, 6	Horizontal	3.8 mm	15 and 20 µm
URVerU	7, 8	Vertical	1.8 mm	15 µm

Table 4.7: List of cleaved laser bars from "Harvard" layout.

4.5.2 Cleaved-facet laser LIV results

The cleaved laser bars were screened with continuous wave (CW) current injection through a pair of probing needle on p- and n-probe of finished bar, on a temperature control stage with stage temperature of 20 °C. The device bar was held down to the stage surface with a vacuum pump. Edge-emitting light from single side of the bar was collected with an integration sphere adjacent to the stage. Light-current-voltage (LIV) characteristics were collected for all screened devices. No additional facet coating was applied at this stage.

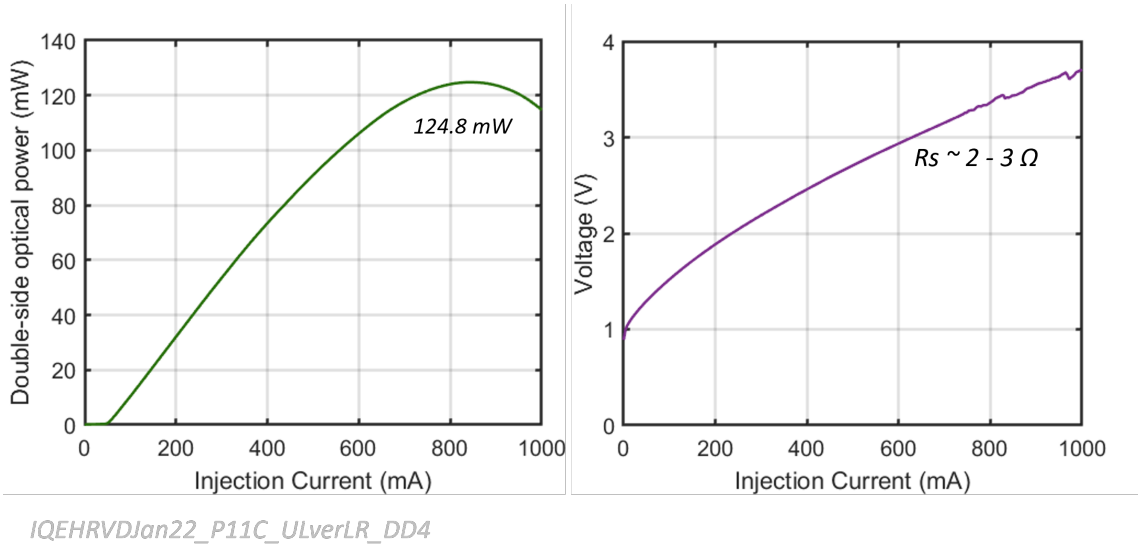


Figure 4.26: LIV characteristics of the peak performing in-pocket cleaved-facet laser. Device footprint is 4.5 µm × 1800 µm.

Figure 4.26 presents the peak performing device from the screened cleaved facet lasers, with the total output power computed from two measurement from both left and right emitting facet of the laser. The results exhibit a maximum double-side output power of 124.8 mW [6], a threshold current of 47.5 mA and a series resistance of about 2 - 3 ohms at higher current. This device has a cleaved length of about 1.8 mm and a designed mesa width of about 4.5 µm, and the computed threshold current density is about 500 A/cm^2. The performance is comparable to devices grown on blanket Si substrate with similar TDD [13]. The highest double-side wall-plug efficiency of 8.6% is achieved at an injection current of 216 mA.

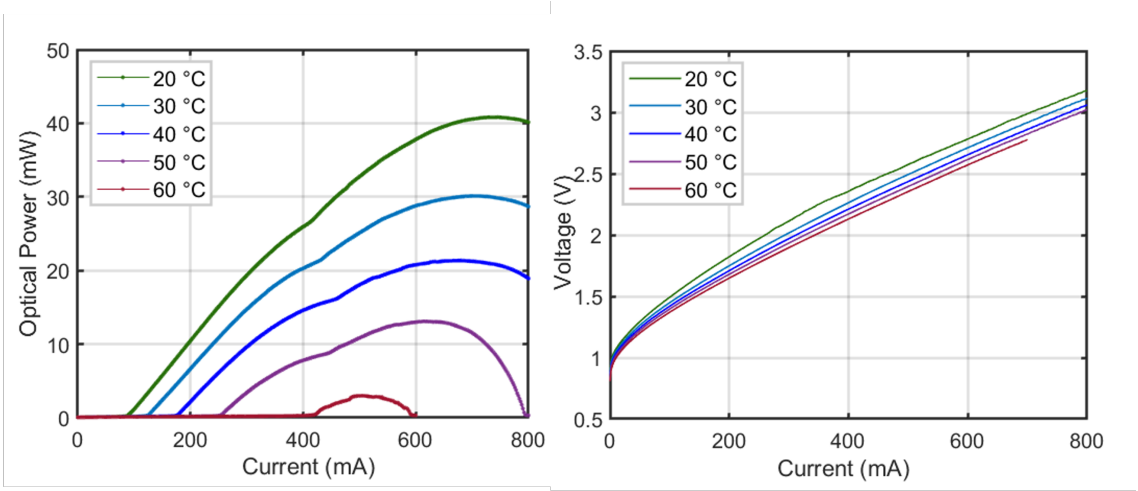


Figure 4.27: Temperature-dependent LIV characteristics of an in-pocket cleaved-facet laser. Reproduced from [2].

Figure 4.27 shows the high temperature LIV characteristics of another peak performing laser cleaved from the same die as the above result. Single-side optical power reaches

[6]Note that this result was reported in our publication [2] with a maximum double-side output power of 126.6 mW, which was incorrectly added from the maximum power of left and right side measurement respectively. However, the two max-power data occurred at different current injection level, likely attributed to the asymmetric heating and/or current spreading non-uniformity in the cavity, so should not be added to represent the practical highest output power from this device.

over 40 mW at 20 °, and lasing was observed up to 60 °C.

To provide a more comprehensive summary of the device performance, we analyzed a total of about 85 lasers out of 13 bars on 7 samples, fabricated through April 2022 to August 2022 with a few generations of laser masks. The devices are from the same "Harvard" layout[7]. Figure 4.28 shows an overview of the LIV results.

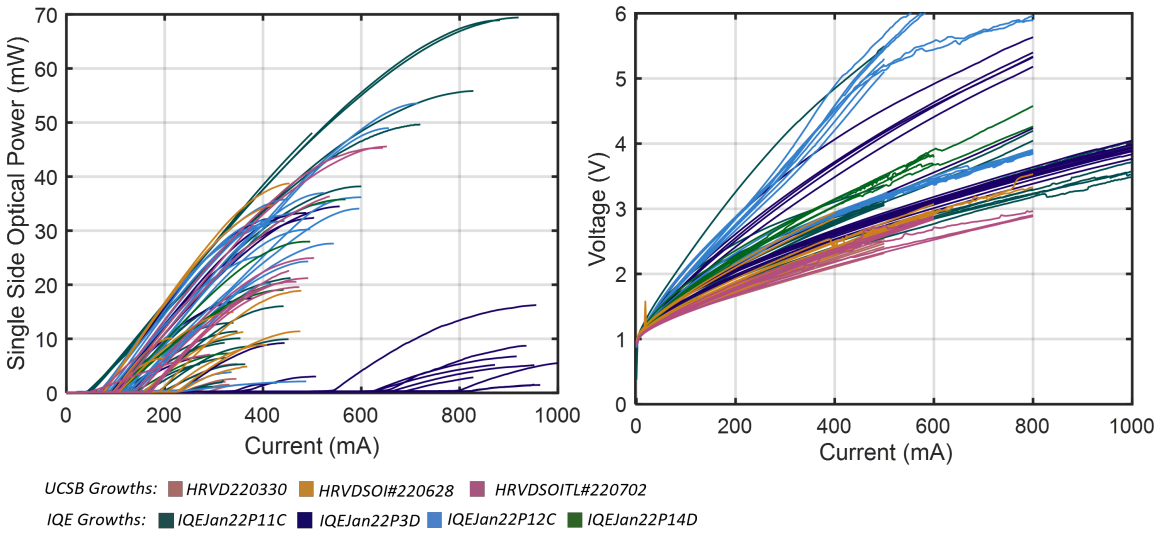


Figure 4.28: LI and IV characteristics of 85 in-pocket lasers yielded from 13 bars on 7 separately fabricated samples.

At a glance, the threshold current spans from sub 50 mA to as high as 800 mA, with variations in maximum output power and series resistance as well. Taking into account differences in cleaving lengths, mesa widths, pocket widths, and orientations among devices, we perform data analysis regarding these various factors and seek correlations accordingly. Table 4.8 provides a brief overview of the distributions. [8].

Figure 4.29 comparing pockets from different orientations, a "vertical" pocket versus

[7]For a complete list and timeline of device fabrication runs, integration layout generations and wafers, see the Chapter 6.

[8]The statistic analysis included one extra device (so 86 in total) which was shorted during testing and not plotted in the overview.

Test Date	Sample	Total bars	Total lasers	Orientation	Pocket width
20220408	HRVD220330	1	6	V×6, H×0	30 µm×1, 20 µm×5
20220429	IQEJan22P11C	3	19	V×15, H×4	30 µm×5, 20 µm×14
20220512	IQEJan22P3D	1	18	V×18, H × 0	30 µm×6, 20 µm×12
20220714	IQEJan22P12C	2	18	V × 6, H × 12	30 µm×6, 20 µm×12
20220715	IQEJan22P14D	1	5	V×5, H×0	30 µm×5, 20 µm×0
20220805	HRVD220628	3	10	V×5, H×5	30 µm×5, 20 µm×5
20220813	HRVD220702	2	10	V×5, H×5	30 µm×5, 20 µm×2, 15 µm×3
Total	7 samples	13 bars	86 lasers	V×60, H×26	30 µm×33, 20 µm×50, 15 µm×3

Table 4.8: Overview of tested samples.

"horizontal" pocket. "Vertical" here straightforwardly means the pocket design is vertical on the integration mask layout, and "horizontal" means it is horizontal on the integration mask layout. In production, there is a "notch" direction on the patterned Silicon wafer that is parallel to the Si surface step edges. Since the mask layout is always initially aligned the same way on the 300 mm Si wafer, the "vertical" pockets are always parallel to the "notch" direction and "horizontal" pocket orthogonal to the "notch" direction. The in-pocket III-V crystal orientation, so far as we observed, has been examined to hold the same relationship to the wafer orientation of the 300 mm Si wafer, either from a patterned bulk Si template or patterned SOI template. As a result, the [1 1 0] crystal orientation always shows in "vertical" pockets that are parallel to the "notch" direction and the [1 $\overline{1}$ 0] crystal orientation always appears in the "horizontal" pockets that are orthogonal to the "notch" direction. Note that this relationship could be different regarding growth conditions [14]. We will revisit this disccusion on QD growth dependency on pocket geometry in Chapter 6, in "Improvements on in-pocket QD quality".

While the highest power and lowest threshold devices were produced from the vertical orientation, the distribution of medium performance devices are mostly comparable for

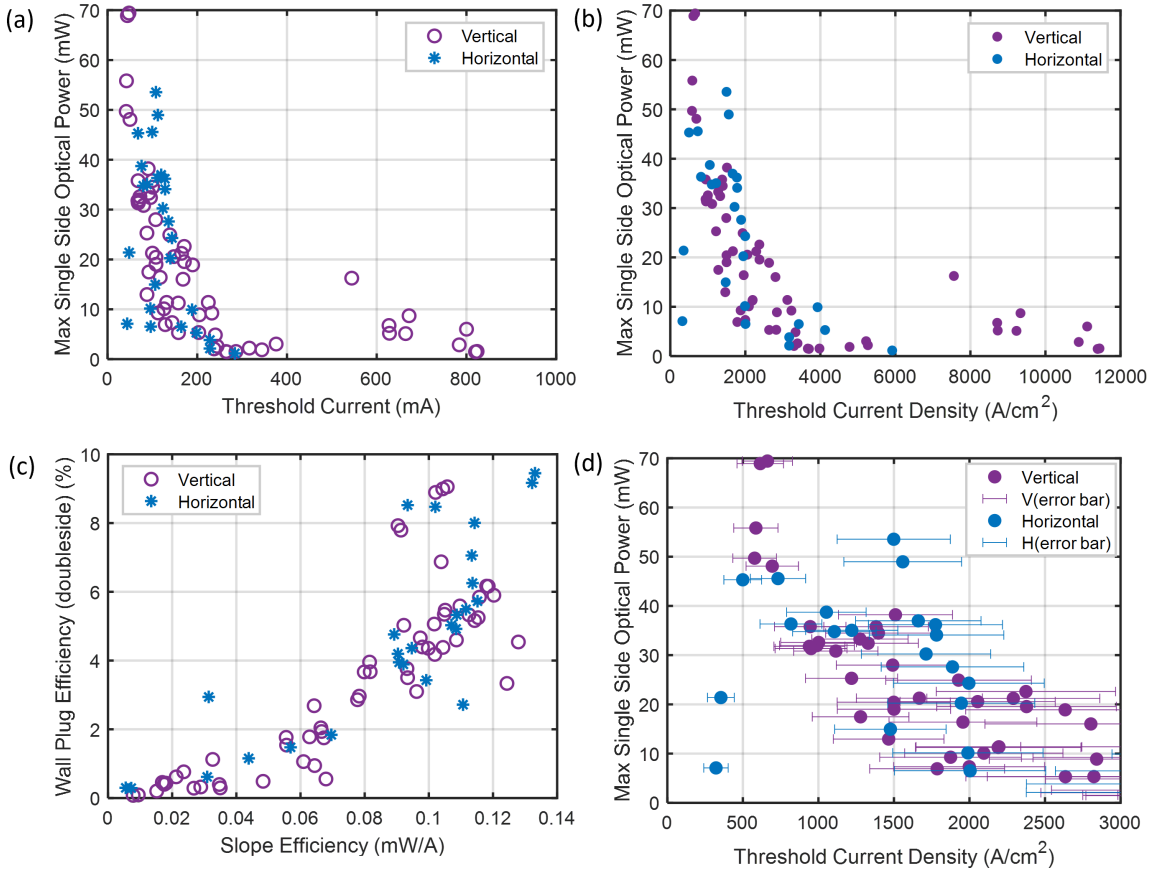


Figure 4.29: Statistical analysis of the laser performance with regard to different pocket orientations, "vertical" and "horizontal". (a) Maximum output power and threshold current, (b) maximum output power and threshold current density, (c) wall-plug efficiency and slope efficiency, (d) zoom-in of maximum output power and threshold current density with error bars.

the two orientations, in the range of 50 - 200 mA threshold current and 10 - 40 mW maximum output power as shown in (a). The bars have various cleaved lengths as shown in the cleaving map depicted in Figure 4.25 and listed in Table 4.7. We compute an estimation of threshold current density taken into account the different device footprint with an estimated average mesa width of 4 µm, as shown in (b). A closer look at the 0 - 3000 A/cm^2 range in shown in (d), with added error bars of ±25% variation in fabricated mesa width taken into account. The lowest threshold current density falls into

horizontal orientations, with limited difference compared to the group of high-performing vertical devices. We also compared slope efficiency and wall-plug efficiency (WPE), and the results are combined in (c). While the horizontal devices show the highest slope efficiency and WPE, the majority of the performance with two orientations overlaps following the same trend.

Overall, the statistical analysis the dependency of laser basic performance parameters on horizontal and vertical orientation appears inconclusive. On the other hand, a detailed theoretical and experimental study of the QD growth dependency on pocket orientation was conducted by our colleagues and published in [3]. A brief review and discussion is included in Chapter 6 in "Improvement of in-pocket QD quality".

Noting that the experiments were not conducted with controlled variables. There are a total of 6 wider pockets at 30 µm pocket width, only present in the vertical orientation, and they make up for the majority of the vertical devices here, while the horizontal orientation results are almost all with 20 µm pocket width, with the exception of three distinguishingly well-performing devices with 15 µm pocket width. The comparison of laser performance difference with regard to different pocket widths are summarized in Figure 4.30.

From the figure, it appears that lasers with 30 µm pocket width typically outperform the ones with a narrower 20 µm pocket width. Figure 4.30 (a) shows that the 30 µm pocket shows in general higher maximum output power, and lower threshold current. Threshold current density and error bars are produced in the same way as in the previous statistical analysis results in Figure 4.29. We can see that though 30 µm pocket width gives generally lower threshold current density and higher output power as shown in (b), the distribution remains a fairly overlapping population if ruling out the data with threshold current density higher than 3000 A/cm^2 as shown in the zoomed-in plot with error bars in (d). In terms of slope efficiency and WPE, 30 µm also takes on the better

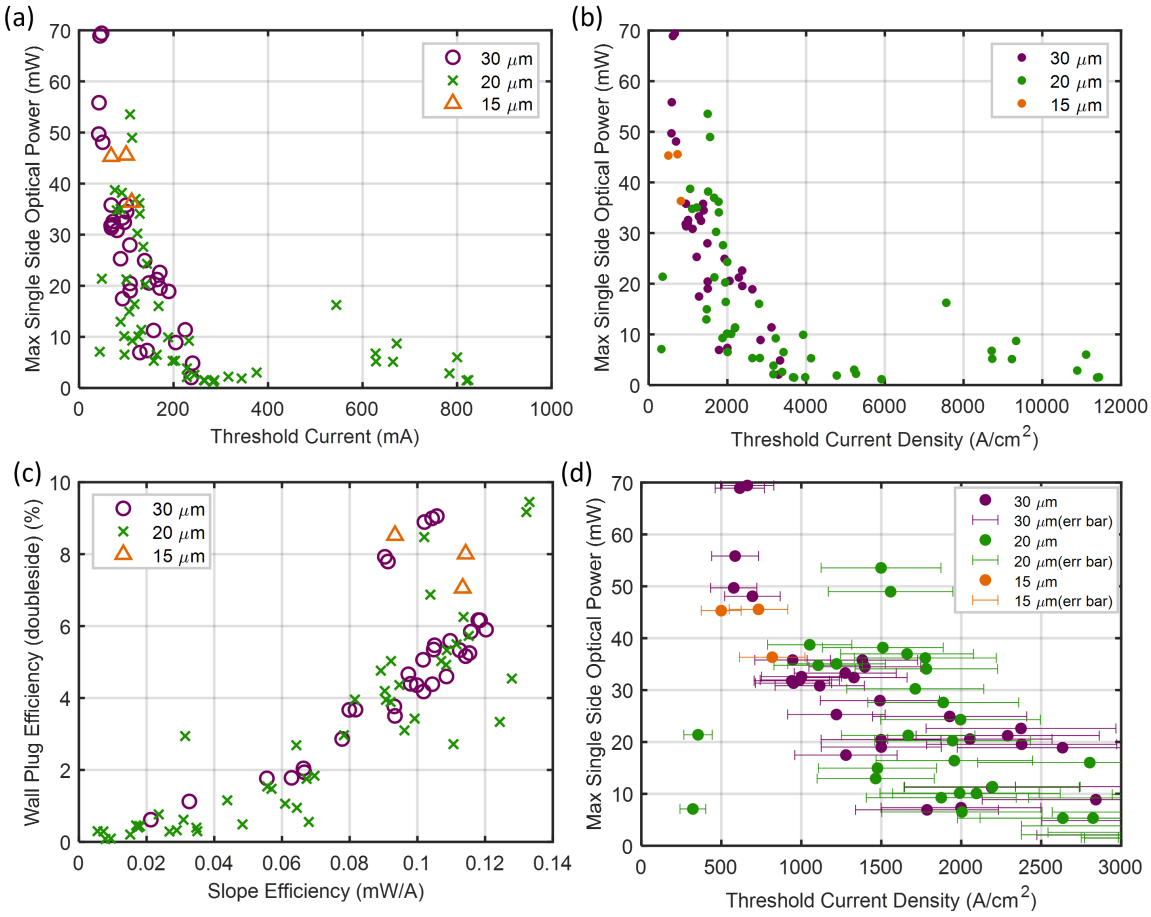


Figure 4.30: Statistical analysis of the laser performance with regard to different pocket widths, 30 µm, 20 µm and 15 µm. (a) Maximum output power and threshold current, (b) maximum output power and threshold current density, (c) wall-plug efficiency and slope efficiency, (d) zoom-in of maximum output power and threshold current density with error bars.

side of the plot more predominantly than the 20 µm results. However, the three devices we yielded from 15 µm pocket width [9] with remarkably low threshold current density, high maximum output power, high slope efficiency and WPE, outperforming the majority of the 20 µm results. Since these 15 µm pocket-width devices were also the only ones with longer cleaving length (around 3.5 mm - 3.8 mm, compared to 1.5 - 1.8 mm, as listed in

[9]One may recall seeing a beautiful cross-section SEM of a device with 4 µm mesa width in a 15 µm pocket in Figure 4.21.

Table 4.7), we suspect mirror loss may be another varying factor due to the uncertainty in device cleaving, which is hard to quantify here to provide a rigorous discussion.

To address these uncertain factors, additional studies of QD growth quality with different pocket widths were conducted with our colleagues. Semi-pocket templates made at UCSB were used in these experiments, allowing for more controlled variables and a systematic approach. The results were published in [15]. The work is also briefly reviewed in Chapter 6 in "Improvement of in-pocket QD quality".

4.5.3 Spectral analysis

Characterization of lasing wavelength was performed by aligning a lensed fiber at the cleaved facet to collect the spectra with an optical spectrum analyzer (Yokogawa, AQ6370C). Figure 4.31 shows an example of data collected from one sample at injection currents ranging from 20 mA to 800 mA with a constant a stage temperature of 20 °C. The below-threshold amplified spontaneous emission spectra have peaks at around 1300 nm, where lasing was achieved around the same wavelength just above threshold (60 mA, 80mA). This is consistent with the ground-state PL wavelength of the in-pocket QDs. As the injection current increases, a slight red shift in the lasing peak wavelength, likely attributed to junction heating, can be observed, as well as appearance of shorter wavelength peaks from the excited states expanding towards 1260 - 1280 nm. This laser has a ridge width of 4.5 µm and cleaved length of about 1.8 mm, fabricated from the same area on the same sample as the peak-performance LIVs in the previous section.

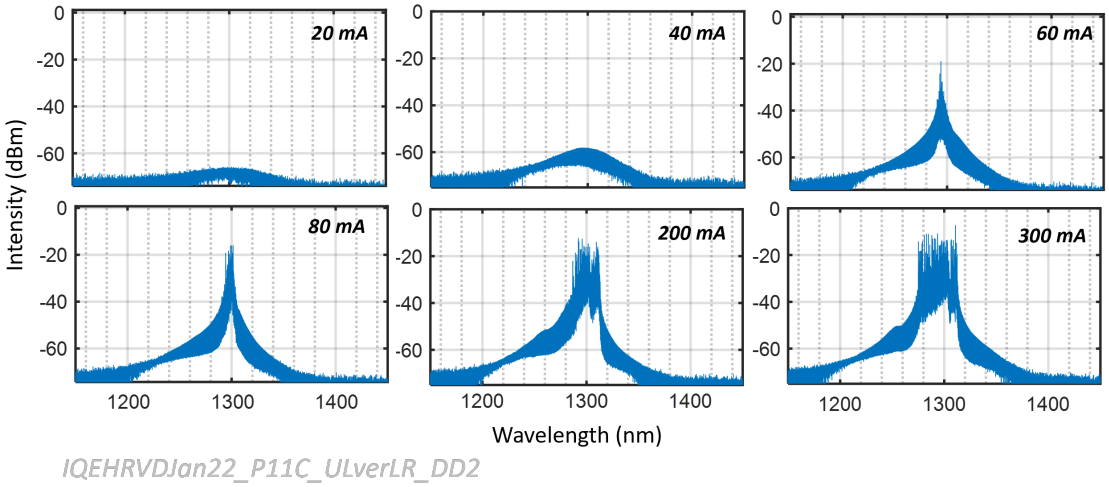


Figure 4.31: Spectra of an in-pocket cleaved-facet laser with different injection currents.

The temperature dependency of the lasing spectra is investigated by adjusting the stage temperature and collect data from 15 °C to 35 °C. The results from the same device are plotted in Figure 4.32, with injection currents just above threshold (100 mA) and well above threshold (300 mA), respectively. It can be observed that the similar trend of excited states appearance with higher current remains consistent across different stage temperatures. Additionally, for the same injection current, a gradual red-shifting of the same peak (or group of peaks) can be observed with increasing stage temperature, in line with our expectations.

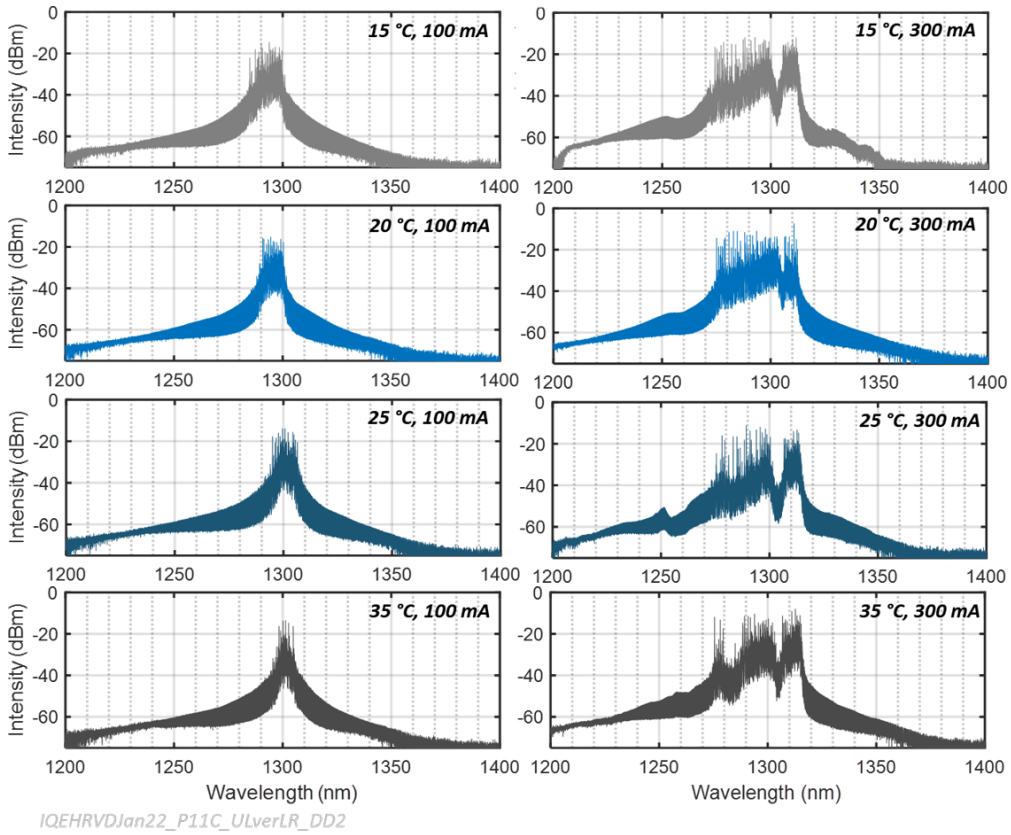


Figure 4.32: Spectra of the same in-pocket cleaved-facet laser with different injection currents and different testing stage temperatures.

We have collected spectrum from different devices at various regions of the same sample (with different pocket orientations and cleaving lengths), and from different batches of in-pocket growth. There are variations in the peak lasing wavelength, akin to the variations observed in the PL from in-pocket QD growths. In particular, some of the PL spectrum shows low ground-state and excited state separation, and/or multiple excited state only (such as the "vertical" in Figure 4.5). Similarly, we also observed devices with only excited state lasing, as examples shown below at Figure 4.33.

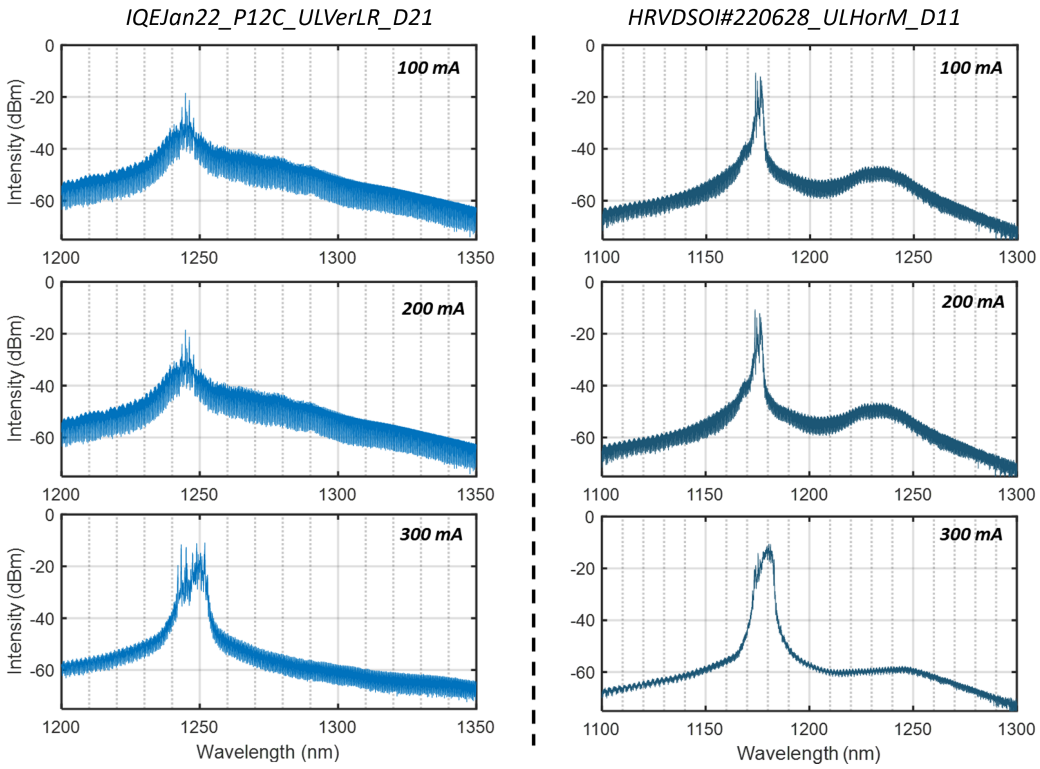


Figure 4.33: Spectra of two different devices from different batches of in-pocket growths and fabrications.

On the left side, "IQEJan22 P12C ULVerLR D21" is from the same area on mask layout (vertical 30 µm pocket) , same designed mesa width (4.5 µm) and device cleaving length (about 1.8 mm) compared to the peak performance devices above, and it is also from the same 300 mm in-pocket growth wafer, but from a different die and fabricated separately. This device shows peak lasing wavelengths around 1240 - 1250 nm with injection currents from 100 mA to 300 mA.

On the right side, "HRVDSOI#220628 ULHorM D11" is from the same mask layout but a different area (horizontal 20 µm pocket), with similar designed mesa width and cleaving length (4.5 µm and 1.8mm). It is from a UCSB in-house MBE growth with the same "-30 °C" temperature offset as growth condition. Though there is spontaneous

emission near 1230 - 1250 nm with increasing current, the lasing wavelength falls even shorter at about 1180 nm, much bluer than the designed ground-state lasing wavelength.

4.5.4 Aging analysis

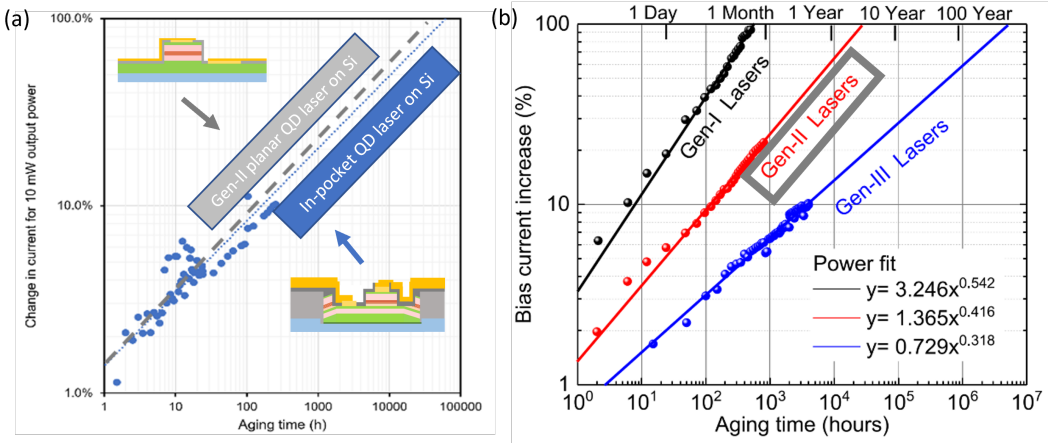


Figure 4.34: (a) Preliminary aging experimental results of an in-pocket cleaved facet laser, reproduced from [2]. (b) aging results of Gen-I, Gen-II, Gen-III lasers. From [13], ©2018 AIP Publishing.

Device reliability characterization was performed by preliminary aging a representative device with continuous current injection with two times the initial threshold at a stage temperature of 35 °C. Data was taken at a test interval during aging to record the change in LIV characteristics. The change in the current required for 10 mW output power for the first 350 hours of aging is plotted in Figure 4.34 (a). An increase of 10 % of current for 10 mW output power was observed at the end of the aging session, at about 350 h.

The aging performance is compared with previous reliability test results published on "Gen-I", "Gen-II" and "Gen-III" QD lasers grown on blanket Si substrate at UCSB, shown in Figure 4.34 (b) [13]. The fitted slope is similar to that obtained in "Gen-II Lasers", which carry a similar TDD level to the in-pocket growth ($1.5 \times 10^7\ cm^{-2}$).

Note that this TDD level is still an order of magnitude higher than the longest lifetime lasers demonstrated ("Gen VI" Lasers with $1 \times 10^6\ cm^{-2}$ TDD and extrapolated lifetime over 200, 000 hours at 80 °C [16, 17]) is likely related to the lack of Thermal Cyclic Annealing (TCA) during the in-pocket growth. Research by Koscica *et al.* on MBE QD growth in a "semi-pocket" configuration with TCA on planar GaAs on the GaP/Si template has demonstrated a lower TDD level at $7 \times 10^6\ cm^{-2}$ [15].

Nevertheless, the initial aging results suggest that the MBE-grown in-pocket crystalline quality is comparable to that of the "Gen II" lasers obtained on a blanket Si template with a similar TDD. This suggests that there are no obvious additional factors (independent from the TDD level) compromising device reliability from the in-pocket geometry. The specific adjustments developed for the device processing to fabricate electrically pumped ridge waveguide lasers in a narrow, long pocket configuration also have not revealed any newly introduced factors that would hasten device degradation.

4.5.5 Semiconductor optical amplifiers

In order to explore the purpose of using the in-pocket material as active gain sections for the monolithic integrated platform, we also demonstrate semiconductor optical amplifiers (SOAs) made with the in-pocket QD gain materials.

The SOAs were fabricated by applying extra anti-reflection (AR) coatings to both sides of the cleaved laser bars. The AR coatings were applied using ion beam deposition (Veeco NEXUS) at UCSB Nanofab. The coating is composed of a duo layer of tantalum pentoxide (Ta_2O_5) and silicon dioxide SiO_2. After calibration of the deposition rate of each layer, we simulated the desired thickness for the lowest reflectance at target wavelength (1230 nm to 1250 nm, in this case, according to measured lasing spectrum of the given device). In the fabricated bar, we applied approximately 104 nm of Ta_2O_5

followed by 118 nm of SiO_2 on the left side, and 104 nm of Ta_2O_5 followed by 123 nm of SiO_2 on the right side. The approximated thickness were measured with a Si witness piece co-loaded in the deposition chamber with the bar during the actual depositions.

Figure 4.35 shows (a) the lasing spectrum of a given device on this bar before AR coating, and (b) the reflectance at peak wavelength for coated Si witness pieces during left-side and right-side coating depositions.

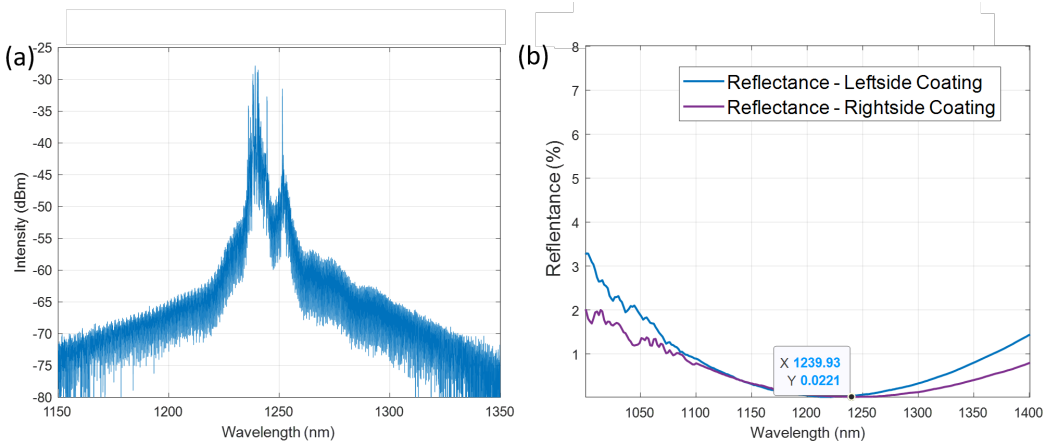


Figure 4.35: (a) Spectrum of a cleaved laser before AR coating; (b) measured reflectance of the Si witness pieces for left and right side AR coating.

Figure 4.36 shows the measured light-current relationship with increasing current using an integration sphere placed on one side of the device, before and after the AR coatings. Before coating, the device functions as an edge-emitting laser with peak power of over 30 mW on both sides, and after the AR coating, the increased mirror loss effectively suppressed lasing. An earlier roll-over was also observed. It is worth noticing that there is slight asymmetry for the emission on left and right side, which may be due to uneven pumping and/or fabrication imperfections of the cavity and coating.

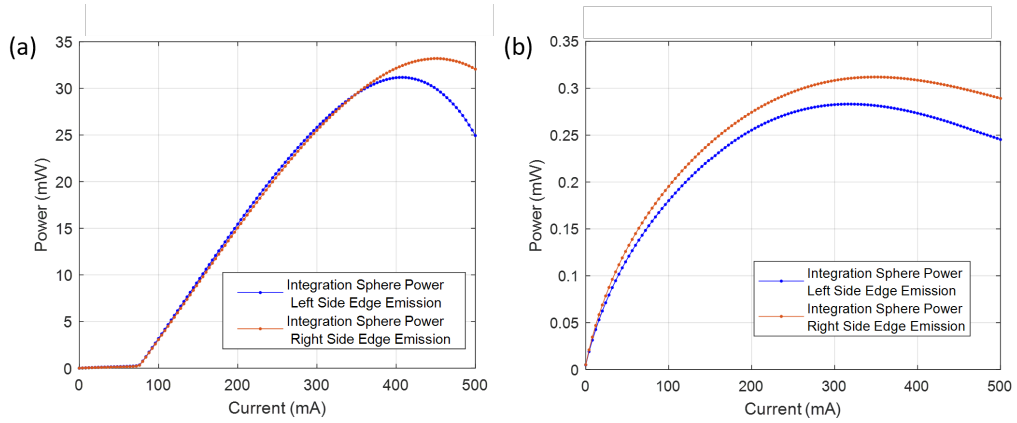


Figure 4.36: (a) edge-emitted LI for the cleaved laser before AR coating; (b) edge-emitted LI for the same device as an SOA after AR coating.

The SOA emission spectra of the same device as Figure 4.35 (a) is shown in Figure 4.38 (a). The peak wavelengths are centered around 1230 nm - 1250 nm, consistent with the previous lasing peaks as well as the desired low-reflection zone of the applied coatings, showing successful post-processing for making the SOA. With an increase in pumping current, the intensity increases with a shift of peak wavelength towards the shorter region, showing a transition to more excited states emission.

The SOA performance of the coated bar was measured with lensed fibers coupled to both facets. Figure 4.37 shows the experimental setup. The stage TEC temperature was kept at 20 °C.

The experimental setup is shown in Figure 4.37. Since there is no waveguide coupling and/or spot-size converted at the edge of chip for efficient coupling to a fiber mode, the edge-to-fiber coupling loss is quite significant, in the range of 20 dB. With a 99:1 power splitter feeding to the piezoelectric controller (K-Cube Piezo Controller, Thorlabs), the feeding output power was so low that it was hard to automatically track the stage and maintaining consistent coupling unless extra care was taken.

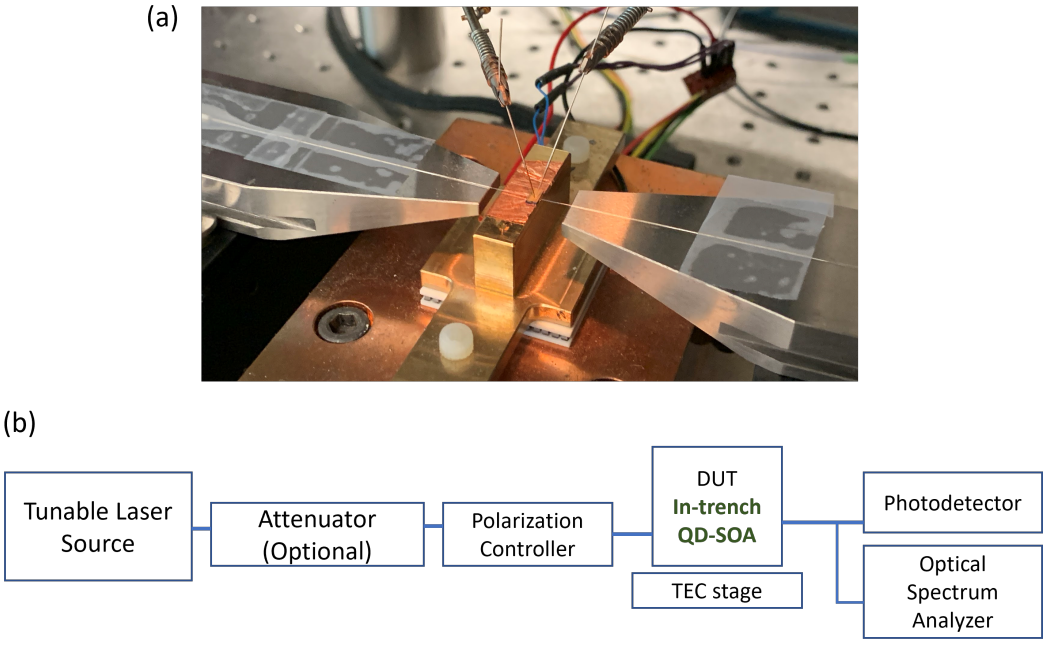


Figure 4.37: (a) AR-coated in-pocket QD SOA bar at experimental setup with fiber-coupled to both facets; (b) Schematic diagram showing experimental setup for measuring the in-pocket QD SOAs.

Nevertheless, input-output power was collected for injection current of 50 mA, 100 mA and 150 mA and pumping wavelengths of 1240 nm, 1250 nm, and 1260 nm. On-chip input and output power numbers were estimated with pre-calibrated fiber-to-chip coupling loss, as plotted in Figure 4.38 (b). Figure 4.38 (c) shows the relationship of on-chip amplifier gain with increasing on-chip input power. The wall-plug efficiency is also computed using the collected data, as plotted in Figure 4.38 (d). Due to the high coupling loss from fiber to chip as explained earlier, it was difficult to collect data with higher on-chip input power to inspect a clearer saturation, limiting the interpretation of our experimental results.

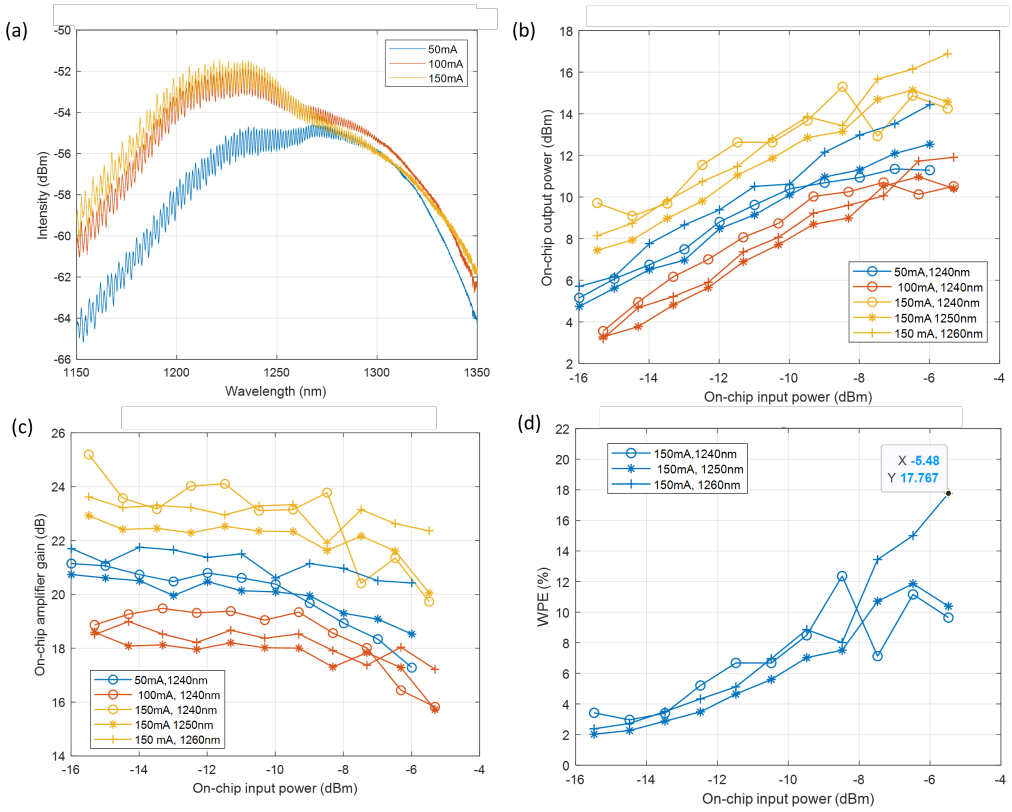


Figure 4.38: SOA measurement results. (a) Emission spectra of the same device from Figure 4.35 (a), taken after the AR coatings at different current; (b) On-chip output power with increasing input power at different pumping wavelengths with different injection currents; (c) on-chip amplifier gain with different input power; (d) calculated wall-plug efficiency (WPE) with 150 mA injection current.

4.6 Summary and outlook

We have demonstrated the first in-pocket QD lasers on 300 mm Si wafer, with cleaved-facet lasers exhibiting highest CW output power of 124.8 mW and lasing up to 60 °C. Wafer preparation procedures and MBE growth development was presented, followed by extensive reports of the fabrication process development, including post-MBE growth polycrystal removal, and details on addressing fabrication challenges regarding the high aspect-ratio pocket geometry. In particular, the notes on fabrication process development

can be applied beyond this integration scheme and benefit innovative solutions regarding the increasingly complicated integration schemes.

In addition to laser measurements, we also conducted characterization of the gain section as SOAs with AR coating on both cleaved facets. Performance characterization has provided insights of the in-pocket QD material.

Despite the limitation of per-chip yield from the initial parameter splits in the integration design, we collected sufficient measurement results from various generations of sample fabrication and performed statistical analysis on the collected data of laser performance. Correlations of laser characteristics with pocket geometry were studied, and the initial findings have led to further investigations that significantly improved the yield of the platform in subsequent generations of integration designs. Comprehensive reflections on the findings across different generations of designs and combined insights from both growth and fabrication aspects for the integration platform will be covered in Chapter 6.

For practical implementation of our proposed monolithic integration platform, the imminent challenge is to demonstrate on-chip in-plane coupling of the in-pocket lasers to Si photonics components readily produced on the 300 mm SOI wafer. The challenge turns out to be utterly nontrivial, and our journey starts in the next chapter.

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Chapter 5

On-chip QD lasers coupled to SiN waveguides on foundry-processed 300 mm SiPh wafers

5.1 Introduction

Following the making of the first in-pocket lasers on 300 mm Si photonics wafers, the main focus now is to realize on-chip coupling from the lasers to the foundry-processed Si-based components on SOI wafers. This chapter presents a exploratory passage towards the first demonstration of in-pocket QD lasers on 300 mm SOI wafer with direct on-chip in-plane butt-coupling to foundry-processed SiN waveguides.

We will start with the demonstration of concept with a FIB-facet laser, and qualitative experiments showing light coupling in the SiN waveguide. Then, we include detailed process development of an additional facet etch and the first demonstration of on-chip in-pocket etched-facet lasers.

The additional complication of the MBE polycrystal deposition on side-wall and the

faceting added more challenging hurdles for clearing the on-chip butt-coupling pathway, which goes beyond the scope of main-stream flat-layer epitaxial layer processing in semiconductor device manufacture. Investigations of the coupling region, additional process development to address the issues, improved integration design and fabrication will be presented in detail, leading to the first demonstration of on-chip etched-facet laser coupled to foundry-processed SiN waveguides from a 300 mm SOI wafer.

Measurement results and discussions are included in each part, providing resources for evaluating the monolithic integration platform and identifying remaining challenges. The experiments regarding vertical facet etch conditions, process designs for multiple III-V etch with different depths, and strategies for handling non-uniform material and polycrystalline materials also serve as valuable references for intricate semiconductor process development that increasingly drives advancements in photonic integration today.

5.1.1 Photonic integration with in-pocket QD lasers through heteroepitaxy

5.1.2 On-chip butt-coupling configuration

QD laser mode and SiN waveguide mode

The in-pocket QD laser stack was designed with the intention for in-plane butt-coupling with SiN waveguides on the patterned SOI wafer through on-chip monolithic integration. In this project, the SiN waveguide layer thickness and configuration is fixed with the available process with the foundry-processed Si photonics platform provided by our collaborator. With this in mind, the QD laser stack design was carried out earlier in the project to ensure a vertical alignment of the QD mode with the SiN mode. The layer thickness of the two material systems are listed in Table 5.1.

The oxide thickness is designed to be approximately 4 µm, with the two 220-nm SiN waveguide layers separated by 100 nm. Slight variations in the thickness of oxide template may be present [1], and characterization was performed before MBE growth to allow for adjustments of the bottom GaAs buffer layer thickness to ensure the vertical alignment.

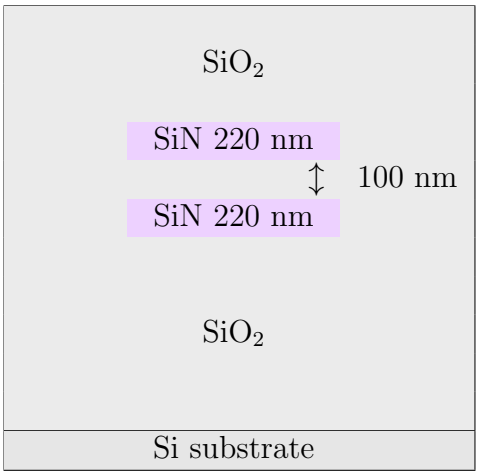
In-pocket QD laser stack	Duo-layer SiN coupler
p+ GaAs 300 nm	
p-AlGaAs grading layers 50 nm	
p-$Al_{0.7}Ga_{0.3}As$ 400 nm	
p-AlGaAs grading layers 50 nm	
UID GaAs 212.5 nm	
QD in QW (37.5 + 7)×5 nm	
UID GaAS 250 nm	
n-$Al_{0.2}Ga_{0.8}As$ 400 nm	
n-GaAs 300 nm	
$Al_{0.7}Ga_{0.3}As$ 700 nm	
dislocation filters GaAs buffer	
Si substrate	

Table 5.1: Schematics of the in-pocket QD laser stack and duo-layer SiN coupler.

Coupling configuration

Figure 5.1 illustrates the concept of in-plane butt-coupling. The vertical alignment of the laser mode and SiN coupler mode, and the duo-layer SiN end coupler shape is tapered to that of a single-layer SiN waveguide for downstream function, and can be

[1] Later in this project, we found significant variations of the MOCVD initial template thickness, which later becomes a main factor affecting MBE bottom GaAs thickness adjustments. Details will be discussed in Chapter 6.

further tapered and coupled to Si waveguide for different functions and for coupling to other PDK components from the Si photonics foundry such as Si ring modulator and Ge photodetectors. The green dashed line in the figure indicates area fabricated from in-pocket heteroepitaxy.

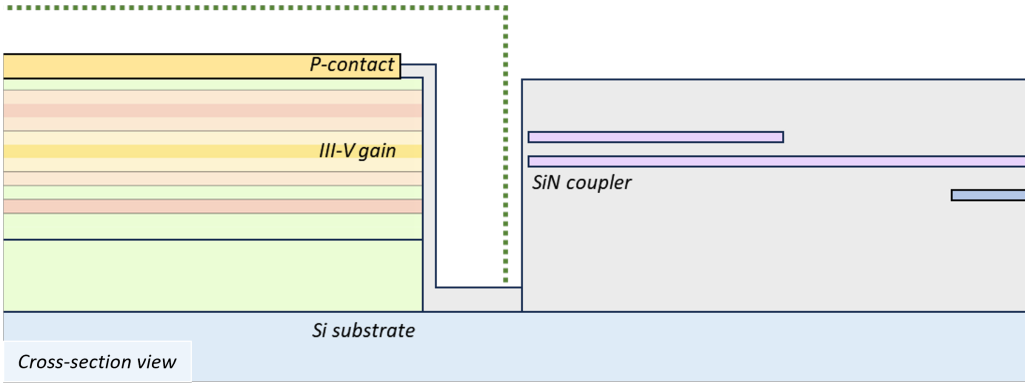


Figure 5.1: Schematic of on-chip in-plane butt-coupling between III-V gain and SiN waveguides at pocket end.

The reflection between the III-V cavity and the SiN coupler can be reduced by designing the pocket to an angled configuration, as shown in the top-view illustrations in Figure 5.2. In the initial layout, we designed the pockets with splits from 4°to 8°("angled pocket, laser").

Due to concerns of material growth at pocket edges complicating the case, we added splits with simple rectangular pockets. Keeping the vertical III-V etch area rectangular will inevitably introduce multiple reflection at the III-V/oxide/air interface and air/oxide/SiN interface, and this is considered a trade-off for design simplicity in early-stage system demonstrations. We also considered designs of gain section with tilted facet matching with tilted couplers that work as on-chip semiconductor-optical amplifiers (SOAs), as shown in the bottom two illustrations. Some splits adopted tapers on the SOA cavity to enable better coupling efficiency with the SiN end coupler. Splits of laser

mesa widths in early iterations includes 3 - 6 µm, and tapered SOA end 4 - 8 µm. Splits of the SiN coupler widths were also included, such as 4.8 µm and 5.8 µm, for example.

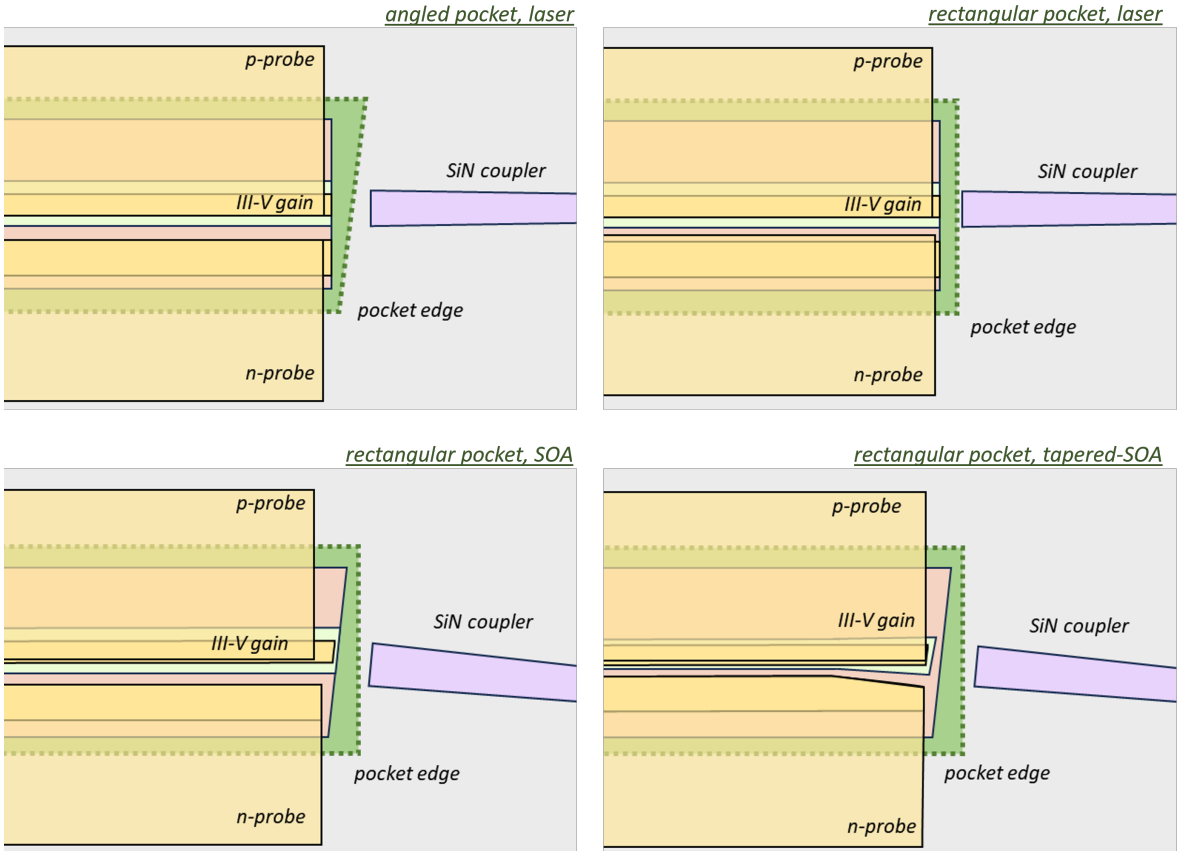


Figure 5.2: Top-view schematics depicting various schemes of in-pocket QD gain sections coupled to SiN couplers.

Detailed simulations of the coupling region using Lumerical MODE and Lumerical FDTD were conducted, and early integration design assumed the III-V facet to SiN gap within 2 µm from the initial expectation, which turned out to be a major underestimate of the realistic case including side-wall polycrystal and faceting for the in-pocket growth. Coupling region re-engineering was performed later in the project to address this issue, and detailed simulation and future proposals for improving coupling efficiency is included in Chapter 6 under section “challenges for coupling efficiency”.

In this chapter, we will focus on endeavors towards the first on-chip QD lasers coupled to foundry-processed SiN waveguides with this monolithic integration platform, both as a demonstration of principle through FIB and with a scalable approach through etched-facet lasers. Detailed fabrication development, experiment procedures and measurement results will be included, and fiber-coupled characterization of the in-pocket QD lasers through SiN edge couplers will be presented.

5.2 Demonstration of concept with a FIB-facet laser

Experimental concept

In Chapter 4, in-pocket lasers have been fabricated on patterned SOI wafer, and lasing demonstration was completed with extra post-processing including backside thinning and cleaving. The results were measured as cleaved-facet lasers, similar to those presented on blanket wafer in Chapter 3.

Figure 5.3 shows a top-view microscope image of the finished sample following fabrication procedures developed in Chapter 4 before cleaving. The designed SiN waveguide couplers as well as other passive elements are adjacent to the III-V gain section in a butt-coupling configuration. The right side shows an example of FIB cross-section SEM of the butt-coupling connection region at the pocket end [2] after device processing described in Chapter 4.

[2]Note that the indication marks are aimed to show where the cross-section SEM is taken conceptually, it is not from the exact indicated in the yellow rectangle on the left, but from the same sample.

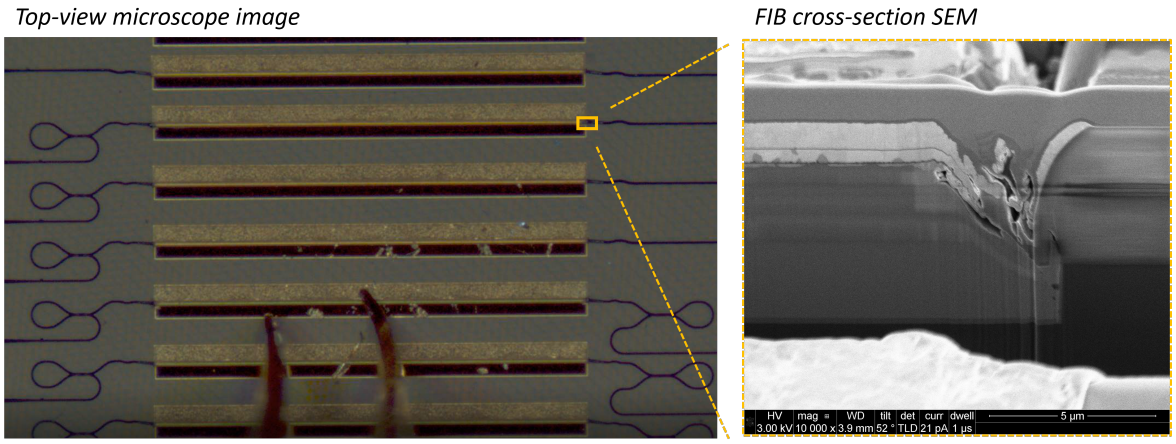


Figure 5.3: (a) Top-view microscope image of finished sample with in-pocket lasers without cleaving. (b) FIB cross-section SEM of the butt-coupling region at the pocket end.

Without additional consideration for the materials at pocket-end, the region naturally becomes complicated accumulations of initial growth faceting and side-wall polycrystal, partial side-wall polycrystal removal through the wet etch, p-metal deposition and multiple hardmasks. Electrical injection of the gain section can be performed and LIV characteristics shows clear LED results with output power at, for example, the range of 50 - 60 µW with an injection current around 200 mA, aligning with our expectation given the lack of effective mirrors and the presence of heavy scattering loss at both ends of the gain section.

The low LED power and heavy scattering loss is clearly suboptimal for realistic coupling experiments. A "short-cut" to increase the output power from the III-V gain section and re-engineer the coupling section for possible on-chip butt-coupling is to use a focused ion beam (FIB) milling process to fabricate rectangular vertical trenches on both ends of the pocket, forming highly reflective mirrors to establish a Fabry-Perot cavity inside the pocket. This process also clears up the complications at the interface of III-V gain section and SiN waveguide couplers, possibly creating a pathway for on-chip butt-coupling

to existing SiN waveguides on the sample, as depicted in Figure 5.4 below.

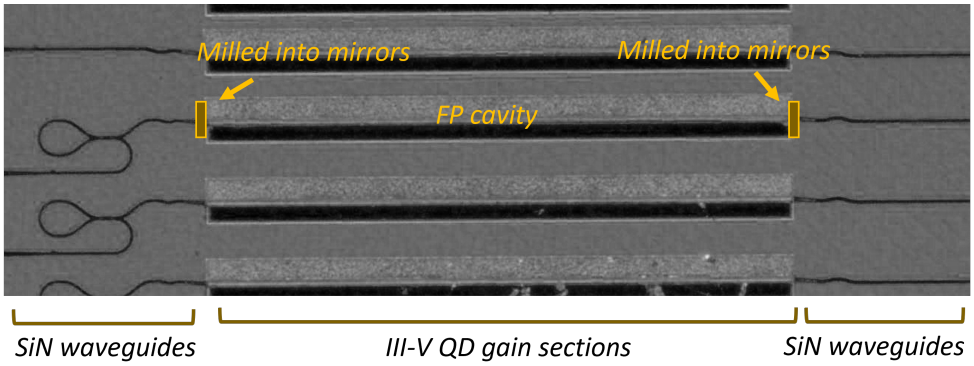


Figure 5.4: Concept of a FIB-facet laser coupled to SiN waveguides.

Fabrication of FIB-milled mirrors

The milling of mirrors at pocket ends using focused ion beam is non-trivial due to the re-deposition of milled materials towards the opposite side, and the tight spacial constraint at the pocket end - it is preferred to keep the III-V mirror facet as close as possible to the SiN couplers, as the free-space propagation between will enlarge the mode mismatch and dramatically reduce coupling efficiency. The target distance between the III-V facet and SiN waveguide coupler end is about 5 µm.

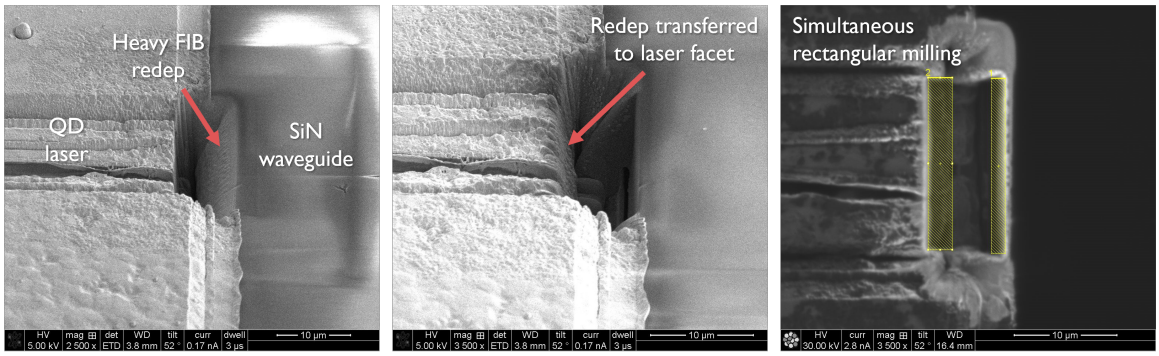


Figure 5.5: FIB milling process to create narrow trenches as pocket ends as reflectors with coupling channel.

Figure 5.5 shows the heavy FIB re-deposition on the SiN waveguide end when cleaning the QD laser facet, and the re-deposition transferred to the QD laser facet when cleaning the SiN waveguide side. The initial attempts were made on a device with as-fabricated LED output power with about 5 µW at 200 mA, and the FIB-milled facets improved the output power to 10 µW at 200 mA, yet was not able to reach lasing. A second attempt was made with a carefully screened out device with higher as-fabricated LED output power of 56 µW at 200 mA [3], and improved FIB milling procedures and extra careful FIB-mill cleaning were carried out with the assistance of my colleague Eamonn Hughes. The right top-view ion-beam microscope image in Figure 5.5 shows the construction of simultaneous rectangular milling that helps dealing with the delicacy of constructing two smooth and vertical sidewalls in a tight spatial constraint at the pocket end. The same procedures were repeated at the other facet of the gain section, making two mirrors at both ends of the pocket.

[3]The first one is HRVD#220628ULVerD2, the second one is HRVD#220628LLHorD11. Later we find out the performance difference can be attributed to the QD growth dependency on pocket orientation (vertical or horizontal), the details will be explained in Chapter 6.

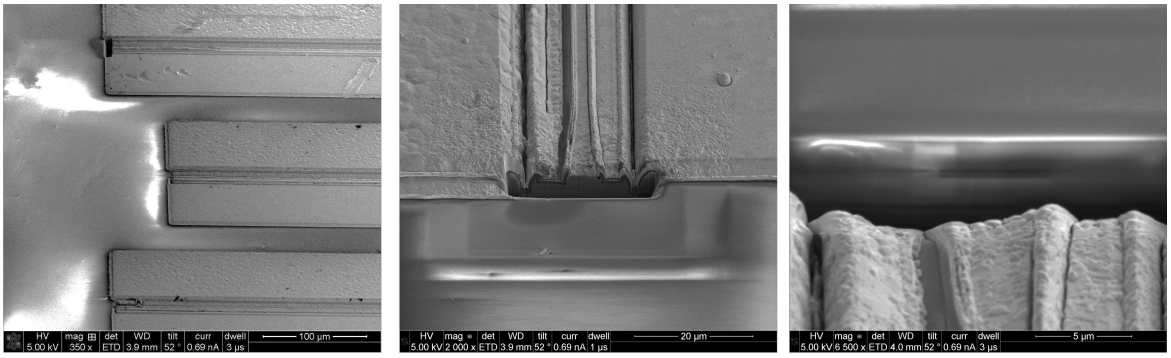


Figure 5.6: SEM images of FIB-milled mirrors at the pocket end.

Figure 5.6 shows more SEM images presenting the FIB-milled mirrors at the pocket end[4]. Clear III-V ridge waveguide cross-section designed with an end-taper is exposed with no additional passivation steps. SiN waveguide coupler made of two layers of SiN waveguide with thickness of 220 nm each and an 100-nm spacing in between is also visible in the tilted SEM [5].

Measurement results and discussion

The LIV characteristics were performed on a testing stage kept at 20 °C with an adjacent integration sphere with continuous wave (CW) current injection. Figure 5.7 shows LED-like characteristics of the device after in-pocket ridge waveguide gain section fabrication described in Chapter 4, with the collected output power of 56 µW at 200 mA. After fabrication of the FIB-milled mirrors on both sides of this cavity, the LIV characteristics shows clear lasing results with the threshold current around 150 mA and output power of 5 mW at 500 mA, orders of magnitude higher than the collected power from the previous LED results. We have collected optical power both from the left side

[4]The left image is from the device with first FIB attempt, the right two are from the device with the second FIB attempt.

[5]Charging effect is fairly noticeable in these SEMs due to the thick oxide on the sample.

and the right side (by turning the chip 180 °, instead of rearranging the experimental set up), as shown in Figure 5.7. The slight difference in collected power could be due to the difference in mirror reflectivity of the two FIB-milled mirrors, and the slight difference in threshold current and IV characteristics may be due to uneven current spreading with a change of probing position on the cavity. We were able to repeat the LIV sweeping result a few times and no noticeable degradation of the characteristics was observed.

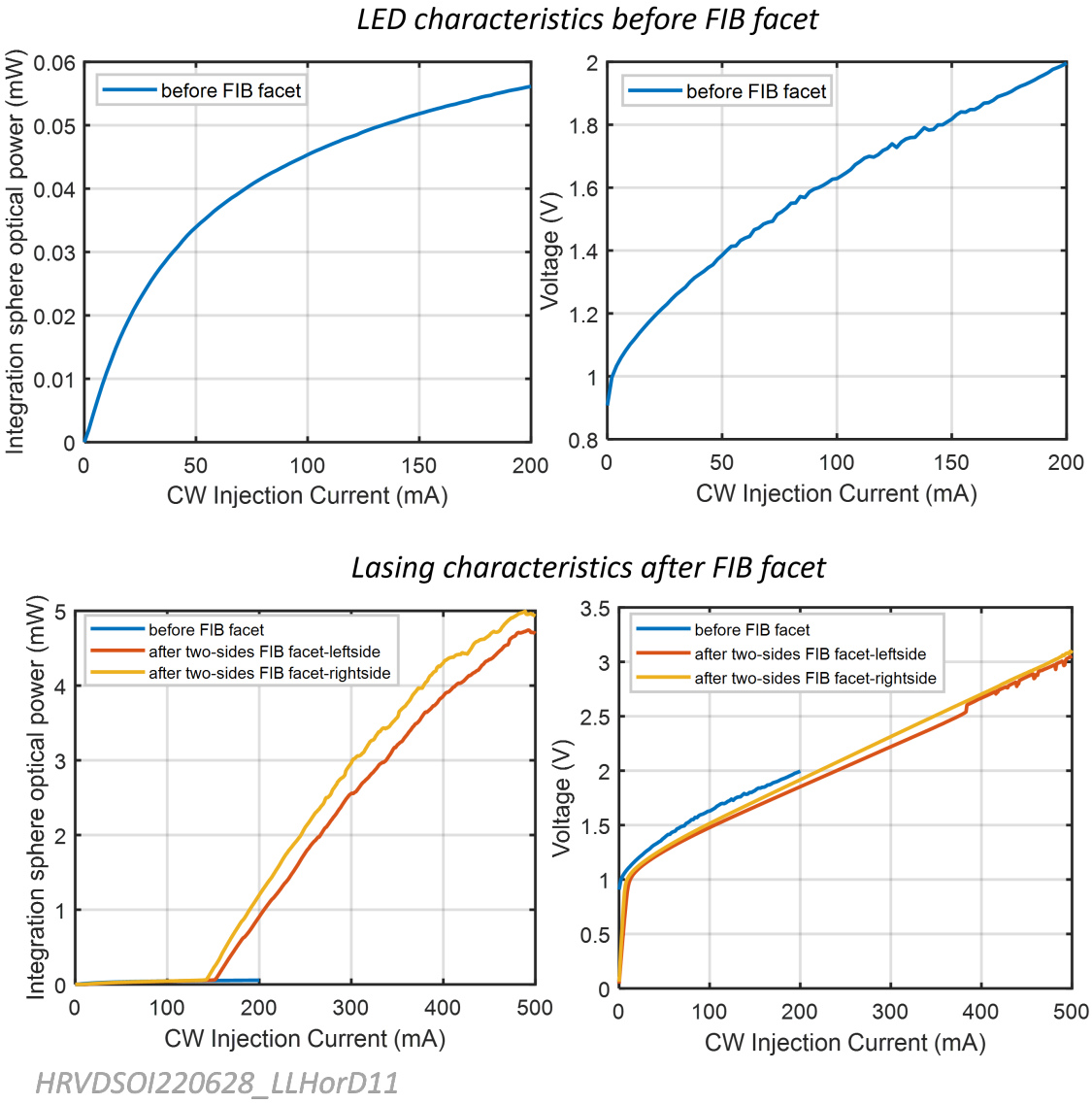


Figure 5.7: LIV characteristics of the device before and after FIB facet. Adapted from [1]. ©MDPI 2023.

Inspections of waveguide coupling from this FIB-facet laser cavity was conducted using an IR camera with a 20× objective towards the sample edge. The laser is probed with a constant sub-threshold current of 18.5 mA with a low output power in the range of 10 µW. Through careful adjustment of the focal plane, a clear indication of the waveguide-

coupled output of light can be observed, indicated by the orange arrow on the right, distinct from the scattered light along the III-V ridge waveguide (green arrow) (Figure 5.8). The top-view microscope image indicates the offset of the SiN waveguide output and the III-V gain section ridge waveguide, also indicated by green and orange arrows respectively.

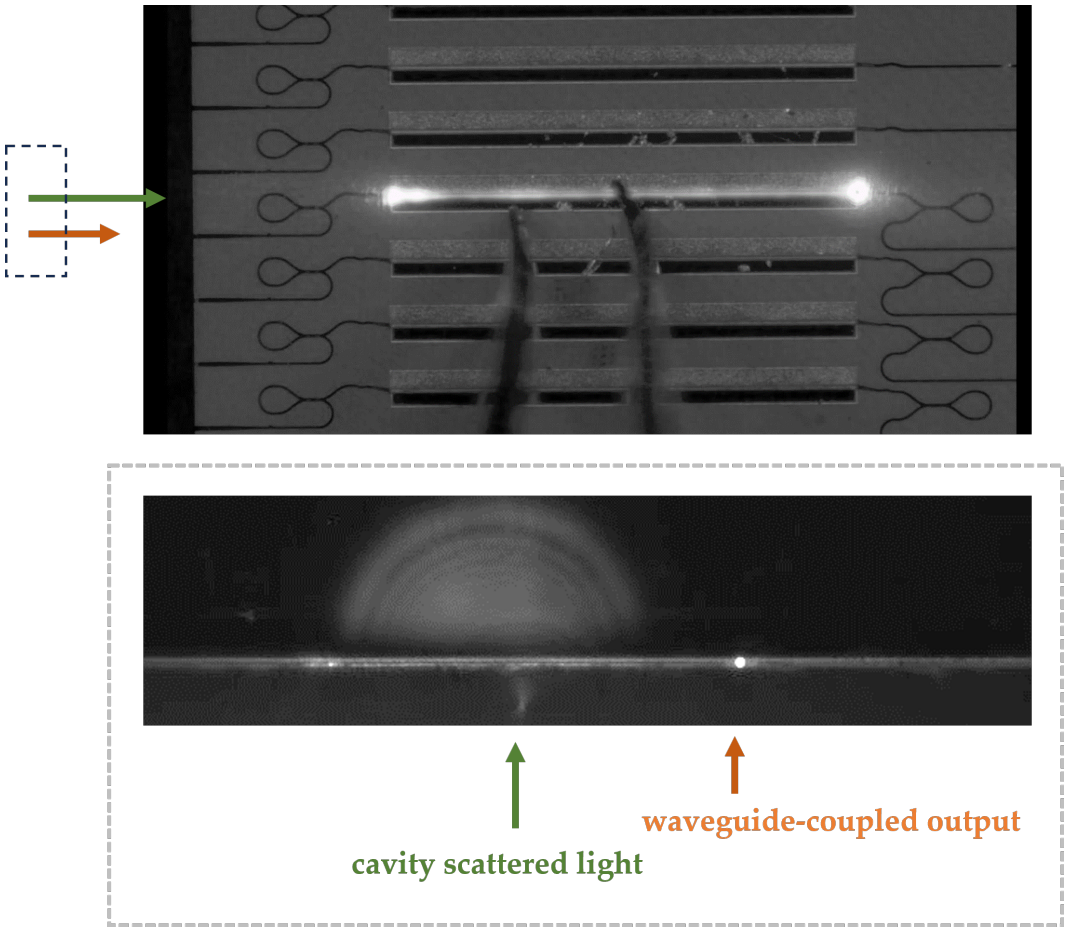


Figure 5.8: (a) Top-view optical microscope photo of the on-chip in-pocket FIB-facet laser on the testing stage. (b) IR camera image showing waveguide-coupled output from the laser.

This experiment acts as a successful demonstration of concept with quantitative laser LIV results and qualitative proof of light butt-coupling between the III-V gain section and SiN waveguide on the same chip despite undesirable air gap at pocket ends. It is a

very first step that shows the potential of monolithic integration with vertical in-plane mode alignment for on-chip butt-coupling and compact arrangement of the III-V active region and Si-based passive components on SOI wafer realized by heteroepitaxy.

5.3 On-chip etched-facet lasers on Si

5.3.1 Introduction

Starting from the demonstration of concept, the next step is naturally to figure out a scalable approach to produce on-chip facet replacing one-by-one FIB miling. Etched facet lasers become the top choice with simplicity, where passivated etched mirrors at both ends of the in-pocket ridge waveguide form a Fabry-Perot cavity.

Alternatives would be to make in-pocket distributed-feedback lasers (DFBs) or distributed Bragg reflector lasers (DBRs), where single frequency laser cavities can be formed by periodic gratings etched inside the in-pocket material. Considering high coupling loss to be one of the main concern, it is better to start with a simple etched-facet laser to reduce the amount of process development and fabrication complication, as well as to produce the largest output power for measurement through coupled waveguides.

In this section, we will cover the fabrication development for exploring the dry etch conditions for making etched facets, and present the first demonstration of in-pocket etched facet lasers.

5.3.2 Fabrication developments for etched facet

Recipe development for the facet etch

To make etched facet lasers, an additional "facet etch" step is added, and it is considered best to be a hardmasked dry etch of the AlGaAs/GaAs epitaxial stack which will

possibly provide the highest verticality, an important factor to make effective mirrors.

The mesa etch recipe presented in Chapter 3 is adopted as a starting point, where initial changing variables are limited to gas ratio and temperature settings to better isolate the factors and understand the results. Pieces of about 1 cm × 1 cm size are prepared with QD laser epitaxial pieces grown on blanket Si template (from pieces of IQE 300 mm growth used in Chapter 3), where identical dies of ridge waveguide with different ridge widths were patterned with PECVD oxide hardmask using older generations of "mesa" layer mask, ready for comparing different III-V dry etch recipes. Table 5.2 lists out the recipes tested.

This experiment is conducted to also serve as a purpose to explore the etching conditions and results with the newly acquired tool Oxford ICP Etcher (PlasmaPro 100 Cobra) [2], short as "Cobra" in the table, which provides versatile settings of temperatures compared to the previously used heavily used III-V dry etching tool ICP Etch 2 (Panasonic E640) [3] (short as "ICP #2" in the table) with only fixed temperature of 15 °C and is required to load samples with backside oil. The previously used GaAs/AlGaAs etching recipe on the tool ICP-Etch (Unaxis VLR) [4] (short as "Unaxis") is also transferred to Cobra to check the etching results, as Unaxis is ready to be retired.

The starting point #1-1 uses the previously developed Cl_2/N_2 based III-V etch on Unaxis, and recreated the recipe in Cobra. #1-2 is a the previously developed Cl_2/N_2 based III-V etch recipe # 113 on ICP #2 that is used for the mesa etch in Chapter 3. #1-3 takes another Cl_2/N_2 based III-V etch recipe # 191 on ICP #2 as reference, the original #191 was created by Bill Mitchell and contains higher Cl_2 and N_2 flow rates and lower bias compared to the other two recipes.

The three samples in group #2 were used to explore recipes on ICP #2. #2-1 is the original version of #1-2, ICP #2 #113 in Chapter 3. #2-2 is a variation of #2-1 with lower bias, which is a split presented on the recipe control data from the UCSB

No. #	Tool	Temperature and loading	Flow-rate (sccm) for Cl_2	Flow-rate (sccm) for N_2	Pressure	Bias (W)	ICP (W)
#1-1	Cobra	30 °C w/o oil	20	10	2 mTorr	75	800
#1-2	Cobra	15 °C w/o Oil	20	10	2 mTorr	100	900
#1-3	Cobra	15 °C w/o Oil	30	30	2 mTorr	50	800
#2-1	ICP#2	15 °C w/ Oil (fixed)	20	10	0.2 Pa	100	900
#2-2	ICP#2	15 °C w/ Oil (fixed)	20	10	0.2 Pa	75	900
#2-3	ICP#2	15 °C w/ Oil (fixed)	30	30	0.2 Pa	50	800
#3-1	Cobra	30 °C w oil	20	10	2 mTorr	75	800
#3-2	Cobra	15 °C w Oil	20	10	2 mTorr	100	900
#4-1	Cobra	60 °C w/o oil	20	10	2 mTorr	75	800
#4-2	Cobra	60 °C w oil	20	10	2 mTorr	75	800

Table 5.2: List of tested recipes for the facet etch experiments.

Nanofab wiki page [5] that produced similar vertical etches shown in the presented test results. #2-3 is the recipe #191 created by Bill Mitchell. The temperature settings of these samples are fixed at 15 °C as a limit of the tool and the samples are all loaded with backside oil according to the tool operation recommendations.

The initial results suggest all samples in group #1 have provided better sidewall verticality. To see if this is relevant to not having backside oil as a main difference between the two groups, we added a few more tests to load with backside oil with Cobra. Group #3 is the repeat of #1-1 and #1-2 with backside oil. After that, group #4 is also added to see what will be the difference with a higher temperature setting at 60

°C, with or without backside oil, which is also the recommended highest possible setting temperature for etching with oil to try as advised by the tool supervisor at the time of the experiments.

Figure 5.9 summarizes the results from the first two groups. Note that the etched samples were hand-cleaved for cross-section SEM, which caused minor cracking due to the thick Si substrate, and some parts of the top oxide hardmask were chipped off at the facet too - these are not related to the etching results.

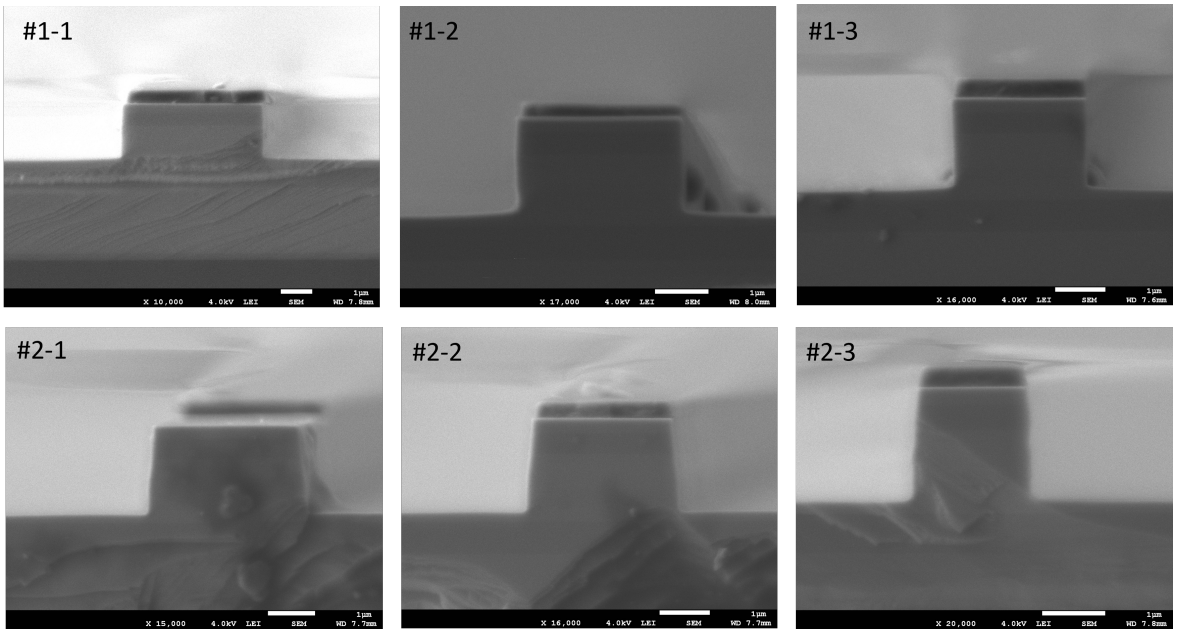


Figure 5.9: Cross-sectional SEMs of etched samples from the first two experimental groups.

The three samples etched in Cobra all showed quite vertical sidewalls. #1-2 shows a bit undercut at the mesa foot, which may be a result of the high bias. #1-3 shows a very minor tilt for in the horizontal etched surface as it extends closer to the mesa feet. The three samples for ICP #2 etch has lower verticality from the etch, possibly as a result of the lower sample temperature. #2-3 also shows more sidewall roughness, which could be a rather undesirable result of the higher flow rate.

The additional two test groups are shown in Figure 5.10, with a comparison to the winning recipe #1-1 from the previous groups. #3-1 and #3-2 is the exact same with #1-1 and #1-2, except that these samples were loaded with backside oil. The sidewall angle clearly have worsened to about 81°- 83°. Note that #3-2 is exactly the same with #2-1, except for the different chamber Cobra vs. ICP #2, yet they have produced similar results. We suspect the change of sidewall angle due to backside oil is due to the heat conductivity of the oil changes the sample temperature, makes it closer to the setting temperature ("Table Heater" temperature) than the ones loaded without oil. In other words, the actual sample temperature in cases of group #1 may be higher than the setting temperature, as a combination of the setting temperature ("Table Heater") and chamber temperature ("Heater", which is fixed at 55 °in Cobra). These assumptions are not validated yet.

To further study the temperature effect, we decide to put a higher Table Heater temperature in Cobra to see if we can force both temperature settings to be higher and create a consistent environment of the sample, which will reduce loading effect (e.g. temperature difference with different sample sizes due to change of conditions in heat transfer). Group #4 are tested with the setting temperature ("Table Heater") at 60 °C, higher than the fixed chamber "Heater" of 55 °C. However, the one loaded without oil, i.e. insufficient heat transfer, showed better sidewall angle and smoothness than the one with oil. The supposedly well-transferred 60 °C table heater setting lowered the etching sidewall angle. These two samples also showed asymmetry in the two sides of ridge sidewalls, which raises higher concern of uneven condition across sample and loading effect.

In the end, we choose #1-1 as a tentative conclusion. The verticality was reproduced with further test samples using in-pocket materials, yet the sidewalls were not always as smooth as shown here. There are still questions about the repeatability and loading

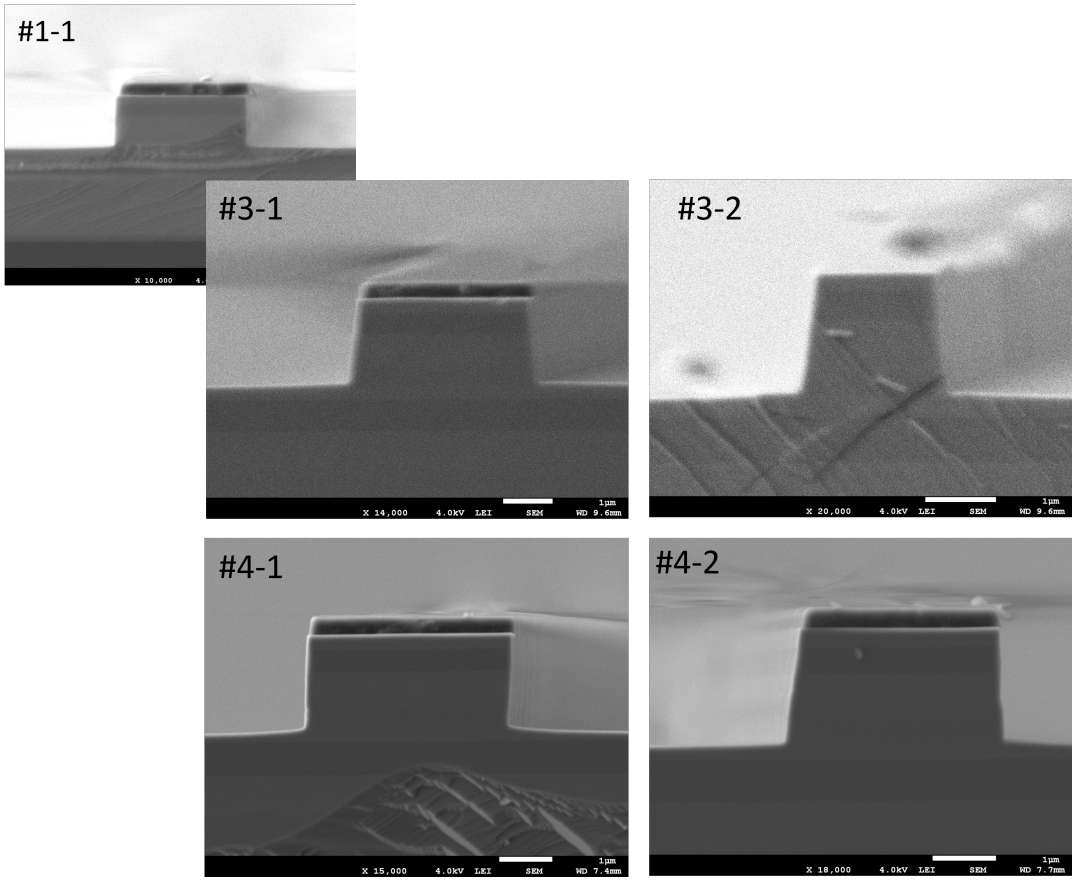


Figure 5.10: Cross-sectional SEMs of etched samples from the two additional experimental groups.

effect. There is also question about whether different cleaning procedures between etches will affect the etch results - for the record the tests here were conducted back-to-back with one initial seasoning run with recipe #1-1 before any sample was loaded. In the facet etch in later device runs, one seasoning etch with a dummy piece is conducted before the actual run (while the etch trace is also checked to record the etch rate and compare to previous numbers and understand chamber condition drift). It also remains unclear why #2-1, the recipe repeatedly produced vertical mesas in Chapter 3, has shown a worsened sidewall angle in this test [6]. Additionally, we encountered more severe sample sliding

[6]It may be a result of different conditions of the hardmask etch - the test samples here should be etched with #104 Nanoetch with ICP#2, yet there are another groups of test samples etched with the

when etching in Cobra without backside oil in future fabrication runs producing device fabrication results in later sections of this Chapter, yet decided to add small drops of backside oil at corners of sample to fix their locations.

Some later fabrications runs also span a time difference (in late 2023, and early 2024) compared to the test samples here (in July - August 2022), and we suspect that chamber conditions may also have changed as the tool gets more used and the post-etch cleaning procedures also have changed a bit. In general, for critical samples, it is always advised to test the etching recipes with dummy epi samples as close as possible to the real etch, and check the etch rate, etch trace, and SEM cross-sections [7]. It is also recommended to separate the dummy test and the real test with their own sets of seasoning etch and post-etch cleaning, so that their conditions are as close as possible. It is time consuming, but an additional half day of effort may be well worth it for a critical step that can determine the device quality of a three or four week fabrication effort.

Process considerations for adding the facet etch

The additional facet etch should be deep enough to prevent mode leakage into the GaAs substrate at the facets, allowing the etched facets to function effectively as reflective mirrors. The mesa etch, on the other hand, defines the ridge waveguide and exposes the n-contact layer and has a fixed etch depth stops at top of n-contact layer. There are a few options of adding the facet etch to the in-pocket laser process concerning (1) whether the mesa etch should be shorter than the facet etch or longer; (2) the orders of the mesa

oxide etch recipe in Fluorine ICP. This assumption is not validated yet. Also, some of the test samples were shared with another colleague for her experiments, and I may have mixed up which ones were from which etch, though the chance is low. Both hardmask etches are laser-monitored with a dummy Si piece to avoid excessive overetch.

[7]The difference in sample sizes may affect the etch sidewall profile, but should not have a large effect on etch speed, which is the basis for using a dummy etch-trace monitor piece for in-pocket laser mesa etches explained in Chapter 4. The same dummy etch monitor method has been used for both facet etch and mesa etch for in-pocket lasers in this chapter.

etch and facet etch; (3) whether the facet etch hardmask should be wider than pocket or narrower than the pocket dimension. We will cover the thought process and decisions in this subsection.

Figure 5.11 shows the options of either having the mesa etch shorter or longer than the facet etch. For ease of interpretation, the shaded areas show the protective hardmask regions of the two etches defined by dry etch using positive photoresist with a boolean of the patterns. I decide to proceed with option 2 as it will be much easier to ensure one smooth, deep, vertical III-V etched facet than the complication of the close adjacency of two facets one shorter and one longer, as it is very hard to achieve them having the same length.

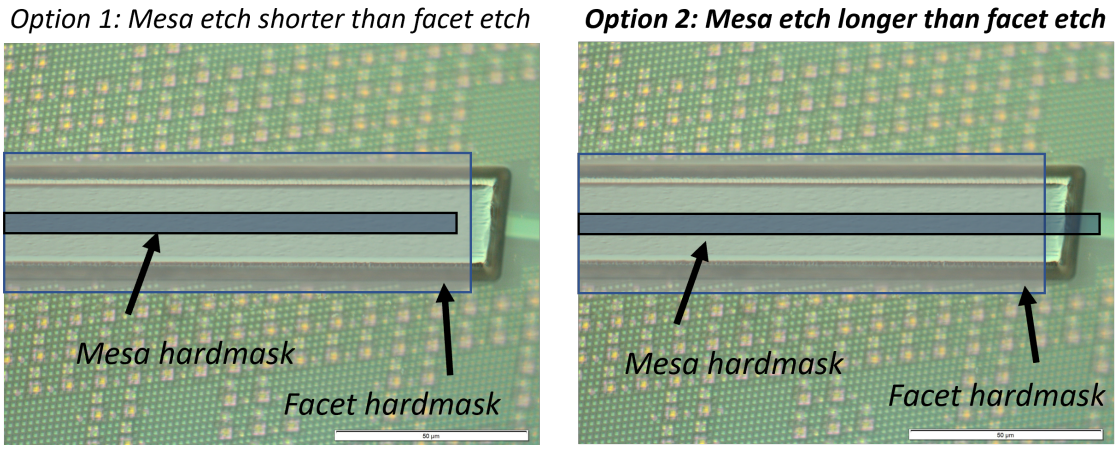


Figure 5.11: Design considerations for the lengths of the mesa etch and the facet etch.

With the mesa etch longer than facet etch, it becomes clear that the facet etch needs to be conducted before the mesa etch, otherwise the area under mesa ridge hardmask protection will have a different oxide hardmask thickness compared to the rest of area during the facet etch, and the facet etch will have to act on materials with different thickness or risk mask edge overlaps from misalignment even with booleaned shapes. It

is easier to imagine the process this way: the facet etch protects all in-pocket material except for the end of pocket, where those parts are attached and etched as the facet. The mesa etch then protects the mesa from being etched, which defines the ridge waveguide. The protection extends longer than the facet so there is no additional etch at the direction across pocket, thus no additional risk of vertical reflections created.

Another consideration at this stage is whether to shrink the facet etch mask to narrower than pocket, so that the materials near the sidewalls along the pocket can also be lowered. The scenario is illustrated in Figure 5.12. Would it be beneficial for metal routing?

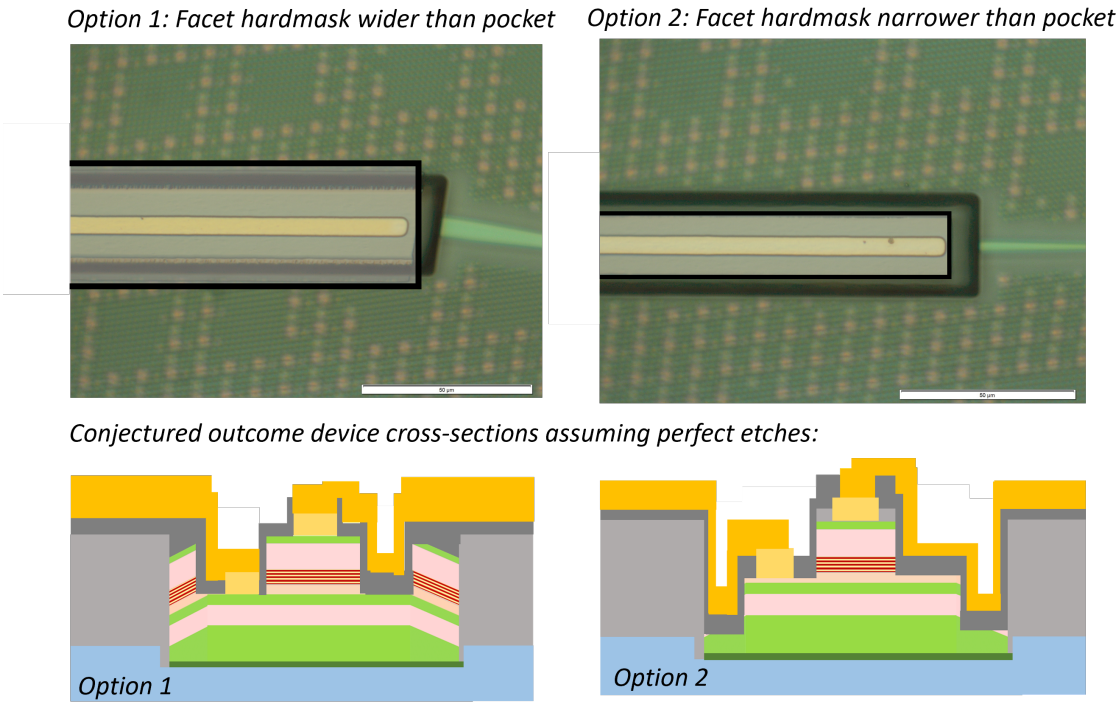


Figure 5.12: Design considerations for the facet etch hardmask width.

We kept splits of both options in the device run. As a result, it is actually better to keep the facet mask wider than pocket, as the etch acting on the polycrystal and faceting

regions along the pocket sidewalls are non-trivial and will only further complicate the surface topography of pocket, as shown in Figure 5.13. In the subsequent section, we will delve deeply into discussions regarding this effect, given its pivotal role in reshaping materials at the end of pocket and affecting the coupling quality from the laser to passive waveguides.

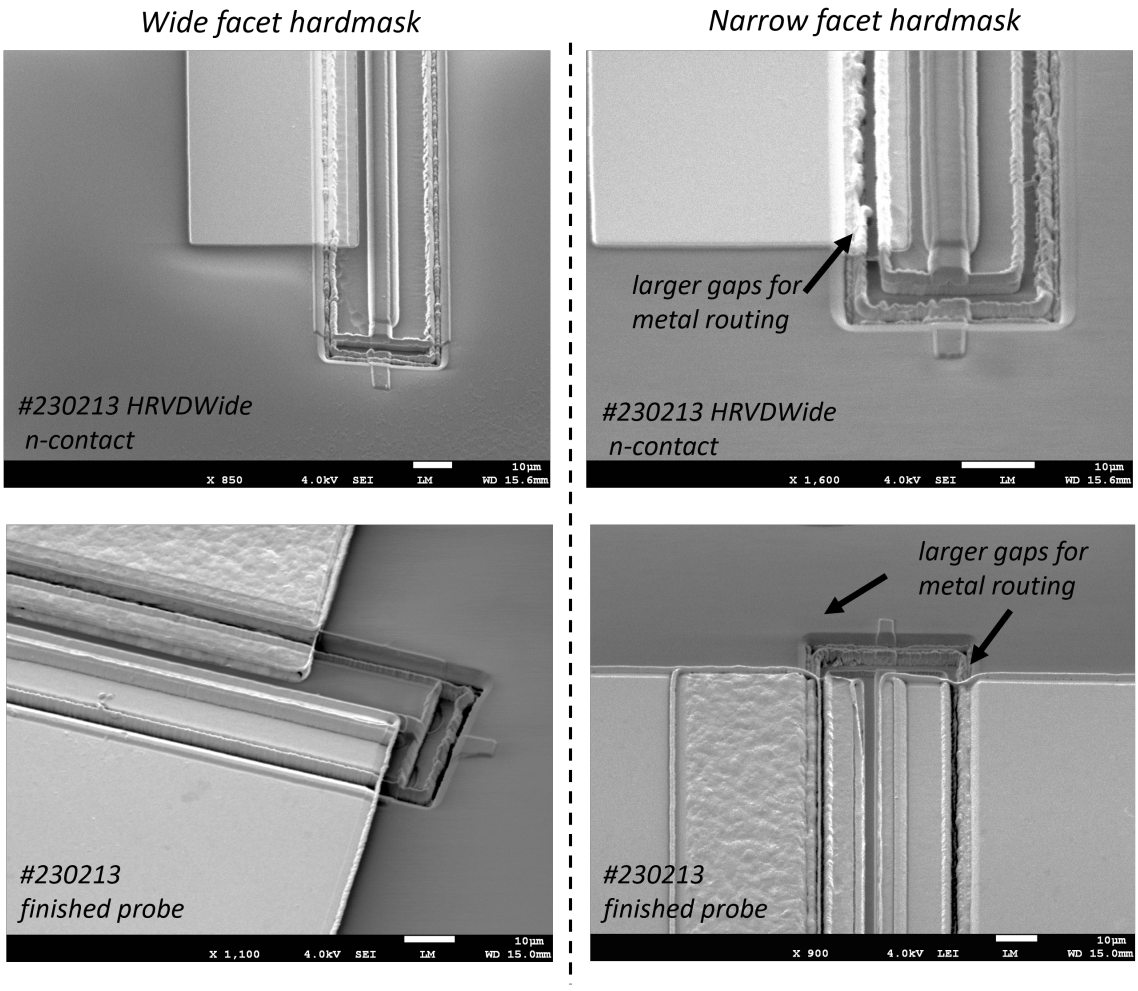


Figure 5.13: SEMs of devices fabricated with wide facet hardmask versus narrow facet hardmask.

As a conclusion, we decided that the facet etch should (1) be shorter than the extended mesa ridge hardmask to define the facet; (2) be conducted before the mesa etch; (3) have

the protective hardmask pattern wider than the pocket width.

The facet etch step is now ready to be incorporated into the in-pocket laser fabrication process developed in Chapter 5 and explore the possibility of making on-chip etched facet lasers. Note that now the process includes two oxide hardmask-defined III-V dry etches, and it should require passivations after each step. It is important to understand the coverage of each passivation and also the etched-back thickness of the existing oxide hardmask during each III-V dry etch, so that there can be a clear record of the remaining oxide thickness on top of mesa and on top of n-contact after the two etches, in order for proper calibration of the p-via etch and n-via etch, respectively. Especially as the facet etch depth is required to be deeper than the mesa etch, potentially into the substrate i.e. over 3 µm, it is important to have enough initial oxide thickness to avoid hardmask getting cleaned off during the etch and risk damaging of the top p-contact layer. The detailed procedures for oxide thickness monitoring and recommended passivation thickness for each step can be found in the Appendix.

5.3.3 Etched facet laser results

A fabrication run incorporated with the additional facet etch was conducted with two samples, one with UCSB in-house MBE growth on new generations of widened version of Harvard testsite template with wider pockets with width of 30 µm where the original width was 20 µm. The SOI wafer preparation, MOCVD initial layers, dicing and MBE growth is similar to that described in Chapter 4.

Figure 5.14 shows some SEMs of fabricated devices with preferred splits of the wider facet hardmask. The vertical etched facets are clearly visible from the tilted side views.

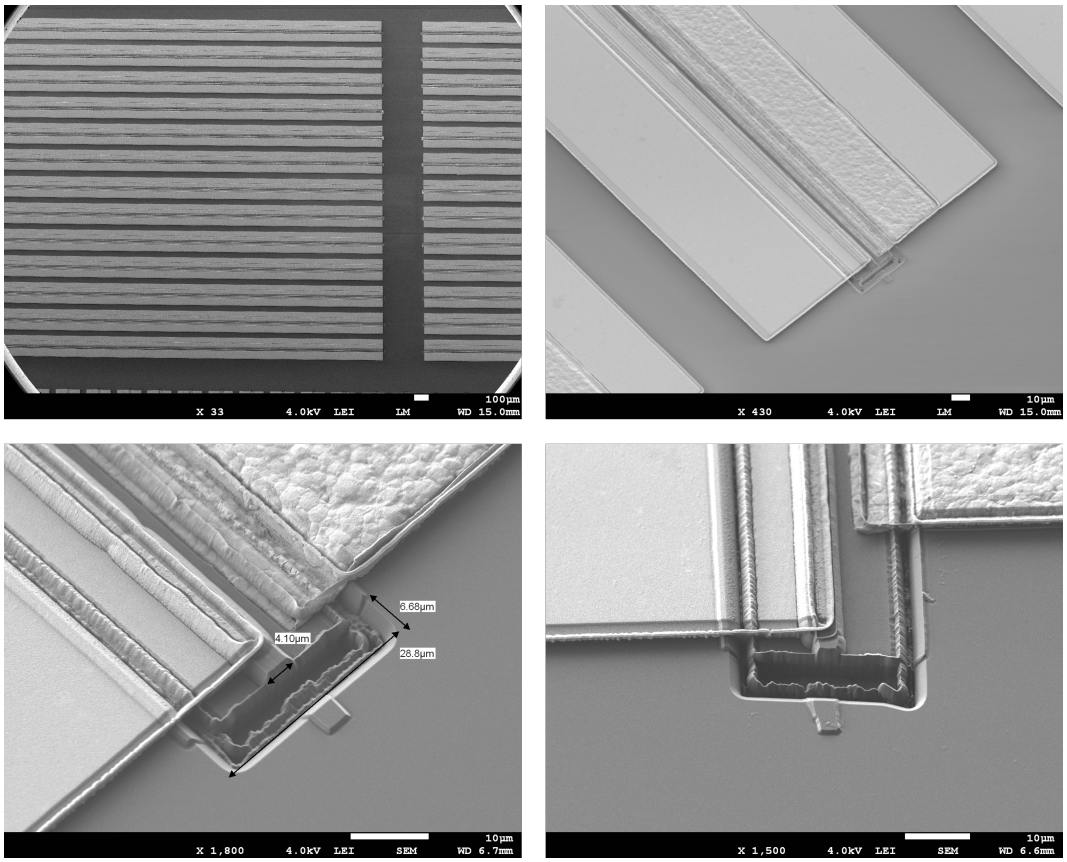


Figure 5.14: SEM images of fabricated on-chip etched facet lasers.

The device LIVs were screened with the integration sphere placed adjacent to the testing stage with temperature control. The collected power indicates the scattered optical power from the device, and a clear turn-on current should be visible if the device is a laser. Figure 5.15 shows the top view from a microscope on testing stage showing the probed device (ULHorLD7) with length about 4 mm, the purple indicating scattered light from top of the ridge collected by the microscope camera (considering color distortion). The right side is a tilted view SEM of the facet of this exact device. Note that for the groups of devices shown in this window, there is no waveguide coupling in the design.

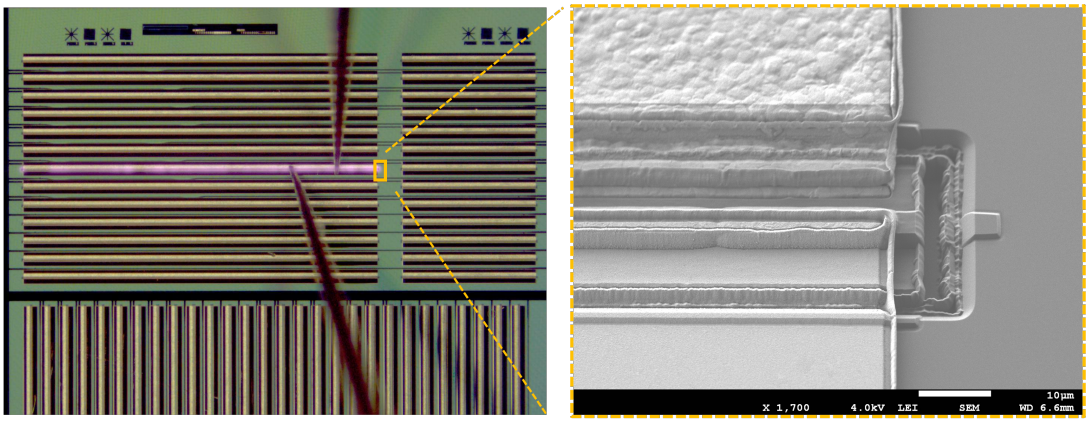


Figure 5.15: (a) Top-view microscope image of the on-chip etched facet laser on testing stage, being probed for electrically-pumped lasing. (B) Tilted-view SEM image of the etched facet of this laser.

The LI and IV plots of the above device was plotted together with the other lasers in the graph below in Figure 5.16. The data was taken in continuous wave (CW) mode at 20 °C stage temperature, and the output power is collected from the left side of the chip only. We were able to produce four lasers from the fabricated sample. Their threshold currents are around 300 - 500 mA, and output power in the range of several milliwatts. Device "ULHorD7", "ULHorD8" and "ULHorD9" are from the same area shown in Figure 5.15, with 4 mm length and horizontal configuration.

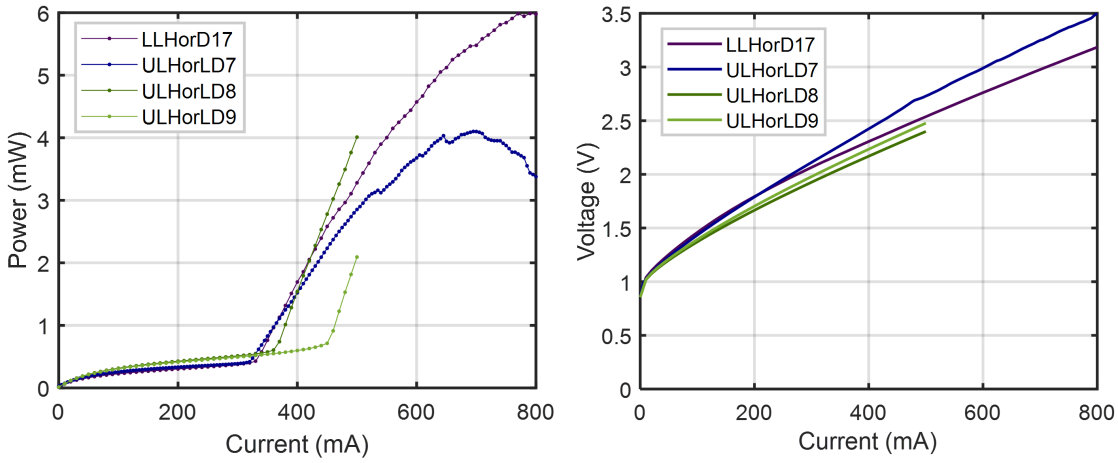


Figure 5.16: LIV characteristics of the on-chip in-pocket etched facet lasers on Si.

We attribute the low yield to the limitation of the splits of pocket widths, orientations affecting QD growth quality on the layout originally intended for integration demonstration, an effect that will be discussed in detail in Chapter 6 on yield and scaling. With the integrated layout design adjusted to the preferred parameters, we anticipate achieving a satisfying yield and overall performance, as will be demonstrated in the subsequent sections of this chapter.

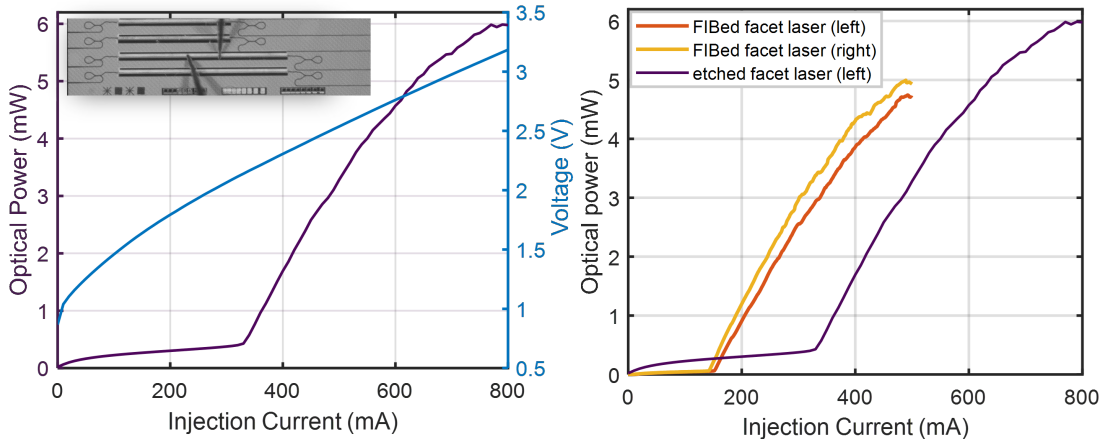


Figure 5.17: (a) Peak performance of the on-chip etched facet lasers. (b) LI characteristics of the etched-facet laser compared to that of the FIB-facet laser.

Figure 5.17 shows the hero device ("LLHorD17") of the four lasers, with maximum output power of 6 mW measured from the left side. The device is located in a different area of the sample from the other three etched-facet lasers, with inset showing the top-view microscope image. The threshold current is about 300 mA, and the calculated threshold current density with its footprint of 4 µm × 3 mm is approximately 2500 A/cm^2. Its higher threshold current density is likely attributed to the increased mirror loss of using etched facet compared to cleaved facet or FIBed facet. Despite the high threshold current density, the slope efficiency and maximum output power is comparable to that of the FIBed-facet laser (which has a device length about 2 mm) we presented earlier in this chapter (Figure 5.7). The right side of Figure 5.17 presents a direct comparison, demonstrating the feasibility of using dry-etched facets for on-chip laser integration.

5.4 On-chip etched-facet lasers coupled to foundry-processed SiN waveguides

5.4.1 Introduction

The on-chip integration between III-V gain section and Si-based waveguides is configured in a butt-coupling regime. With the etched facet, it was expected that the III-V material at the pocket end should have been cleared, since the vertical dry etch is conducted with an extended etch time to etch through the total thickness of the QD laser epitaxial stack as well as the bottom buffer layers.

As one might have noticed, the SEM in the previous section shows a "skirt" like pile of materials at both the ends of the pocket and the left and right sides. A closer inspection was conducted through FIB cross-section SEM along the ridge waveguide direction through mesa center, covering the end of etched facet laser and the start of SiN waveguide couplers, as indicated in the left of Figure 5.18. The FIB cross-section SEM is displayed on the right. There appear to be remnants of III-V with irregular shapes sitting between the III-V etched facet and the oxide pocket. They appears to be either remaining parts of the III-V materials near the pocket edge that were not fully reacted during the facet etch, or residues from the etch that have piled up and re-deposit from the facet etch. They form the "skirt" like structures visible from the etched facet lasers.

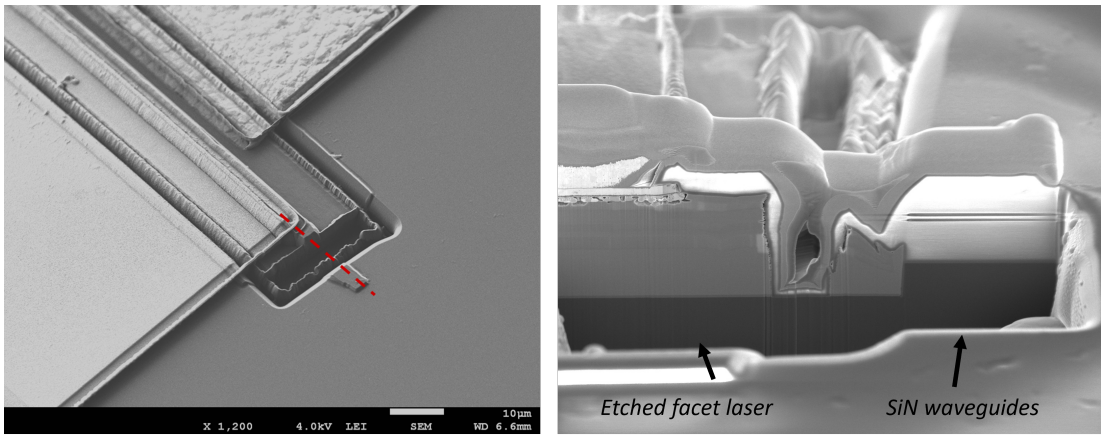


Figure 5.18: Left: SEM image showing the the in-pocket etched facet laser with residue "skirt". Right: FIB cross-section SEM at the pocket end area (red dashed line in the left SEM) of the etched facet laser.

Figure 5.19 shows a few other instances of FIB cross-section SEMs inspected after either the etched facet device fabrication or facet etch only[8]. All three images exhibit the III-V residues at the end of pocket to a certain extent, with distinct shapes, widths and heights. The top of Figure 5.19 shows the FIB cross-section SEM after MBE growth, prior to polycrystal removal and device fabrication. It shows the presence of polycrystal deposition on the sidewall of the oxide and faceting of the epitaxial layer near the polycrystal. The affected region length is roughly 5 µm from end of flat region to start of SiN waveguide couplers, in some cases around 7 µm or longer, subject to MBE chamber and growth conditions [9].

[8]The center one SEM of the three shows a two-step etch at the end of pocket, which is one of the splits on mask discussed in Figure 5.11. The bottom one is a process development sample with facet etch, the dark background between III-V and oxide fence is BCB fill fabricated after the facet etch, a technique employed to reduce coupling loss, which will be covered in later part of the thesis.

[9]We will also discuss ongoing research about different methods to shrink the faceting and polycrystal affected area in later parts of the thesis.

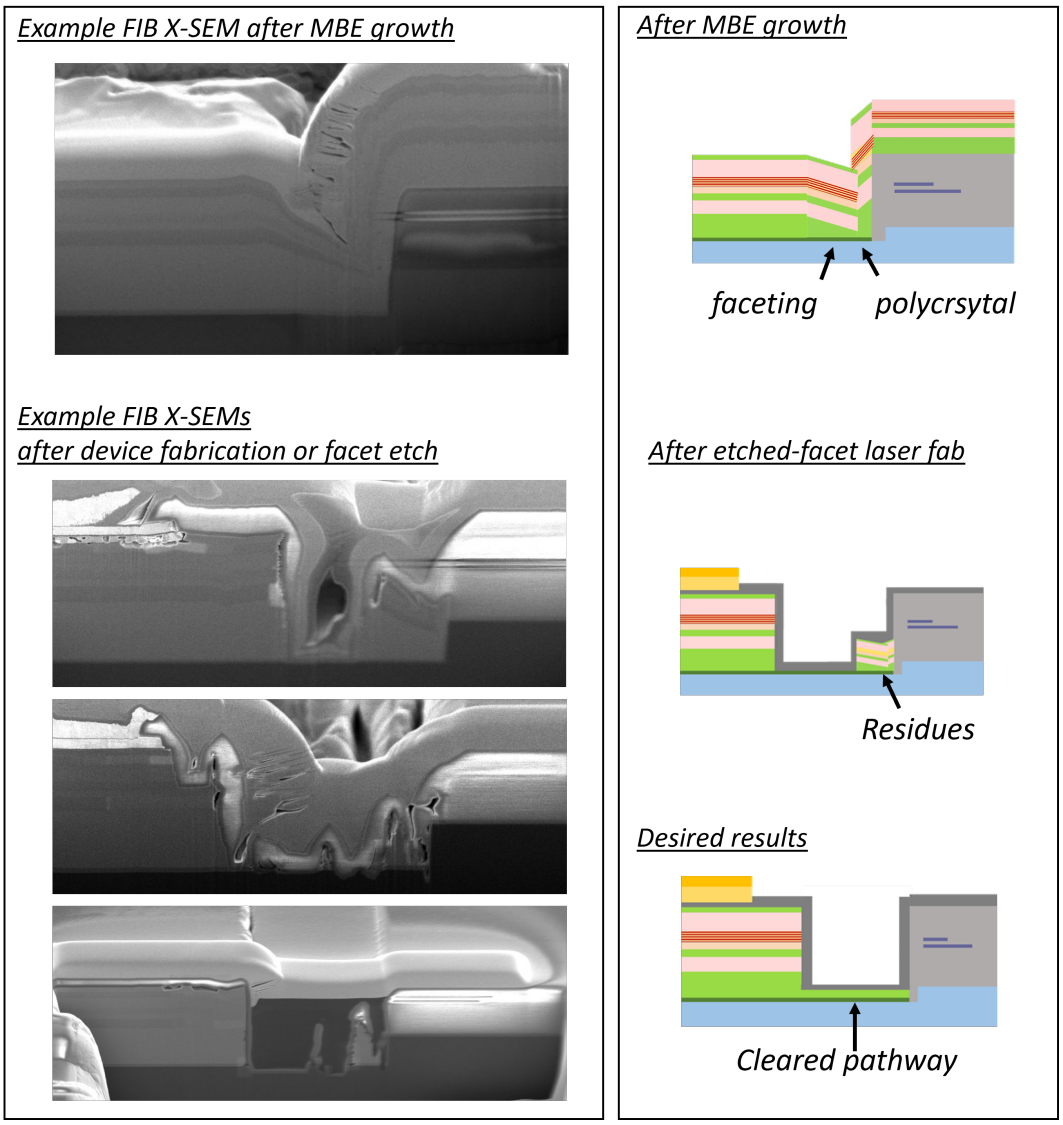


Figure 5.19: Complication of on-chip butt-coupling regarding processed polycrystal and faceting at the pocket end.

The un-reacted III-V remnants or redeposited facet-etch residues at the pocket edge will lead to undesired reflections and scattering for this butt-coupling configuration, and it is essential to develop an effective method for either complete removal or thorough prevention of their formation, creating a cleared pathway like illustrated in the "desired results" in Figure 5.19. However, with the peculiarity of this innovative heteroepitaxial

integration platform, no previous knowledge was available on how they were formed and how to remove them.

5.4.2 Fabrication developments for coupling

Attempts to enhance the facet etch

A series of study was conducted in an effort to improve the facet etch and explore the possibility of thoroughly etching away any remnants. However, the remaining "skirt" was still present with increasing dry-etch bias (hence improved etch rate and maybe lower selectivity (?)) or increasing etch time. In the extreme case, as shown in the bottom SEM on the left of Figure 5.19, the Chlorine-based dry-etch punched through the bottom Si layer and overetched for at least tens of nanometers, with the bottom vertical offset visible at the foot of the etched facet. The remaining III-V pile was not cleared. On the contrary, the height is as tall as roughly 4 - 5 µm.

This shortly shows that during the facet etch, the material at the flat epitaxial layer area and the material in the faceting and polycrystal area are not being etched away in the same rate, even given a similar III-V composition of AlGaAs/GaAs that should be non-selectively reacted.

Attempts to develop a residue removal procedure

With the initial experiments, it appears the problem cannot be resolved by simply extending the facet etch. Shortly after, efforts were redirected towards figuring out a possible way to remove the remaining materials after the facet etch.

Wet etch experiments were conducted using post-facet etch samples to try to remove the remaining materials. Since they are suspected to be composed of AlGaAs/GaAs, with or without oxide hardmask, the samples were put in short-dip of wet-etch chem-

istry such as mixture of hydrophosphoric acid with hydrogen peroxide solution in water (H_3PO_4:H_2O_2:H_2O = 1:4:45, which was previously used for the polycrystal removal in Chapter 4), with variations of either with or without a preceding dip of HF or buffered HF (BHF) solution or an oxide dry etch. Many combinations of etching time were tried, and in most cases the liquid would have travelled faster through the crystalline III-V materials and created visible underetch pattern before the unwanted piles could be cleared.

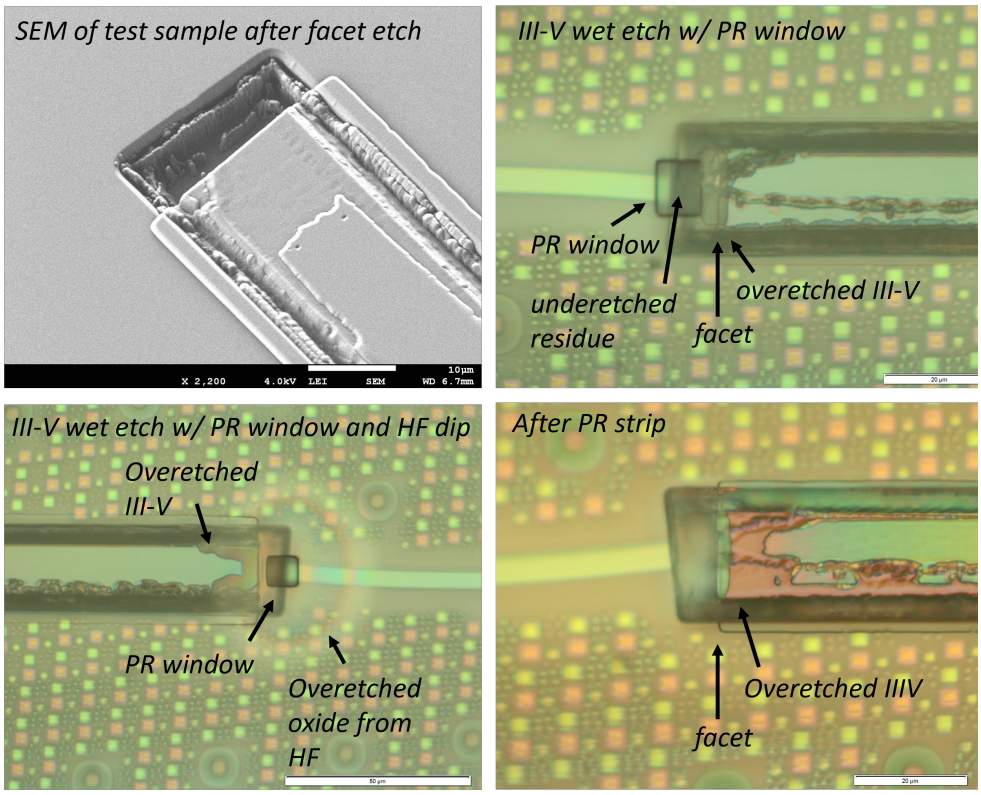


Figure 5.20: Attempts to clean up residues after the facet etch.

Figure 5.20 presents an amusing collection of the many failed attempts for the experiments, with a patterned PR protection window, with H_3PO_4:H_2O_2:H_2O wet etch, and with a short HF dip[10]. The underetch of the III-V crystal behind the facet etch boundary

[10]The surface roughness and defects appeared on the material grown in-pocket will be discussed in Chapter 6, it is not from fabrication.

repeatedly appeared prior to the complete clearance of the residues in the window.

As a result, it appears impractical to employ a wet etch for selectively removing the residues due to the isotropic nature of wet etching and the close spacial proximity between the residues and the ridge waveguide facet.

On a positive note, we observed that with a desperately long-enough soak in a mixture of hydrophosphoric acid and hydrogen peroxide in water, all the remaining III-V in the pocket was effectively removed (as well as the crystalline material in the center, obviously). This means the materials are probably just the un-reacted III-V as we suspected, and there's no additional inert residues introduced such as hardened polymer etc. directly sticking to the bottom surface or sidewall. Interestingly, there remains some minor particle-like patterns of from the lining of uneven surface in the as-grown materials in the pocket was left after the desperate long soak.

With more careful thoughts and some discussions, it starts to make sense that there seems to be remaining thin oxides at the end of pocket and they would mask the III-V underneath and "protect" the piles from being cleared away.

Experiments to study the effect of undesired oxide on facet etch

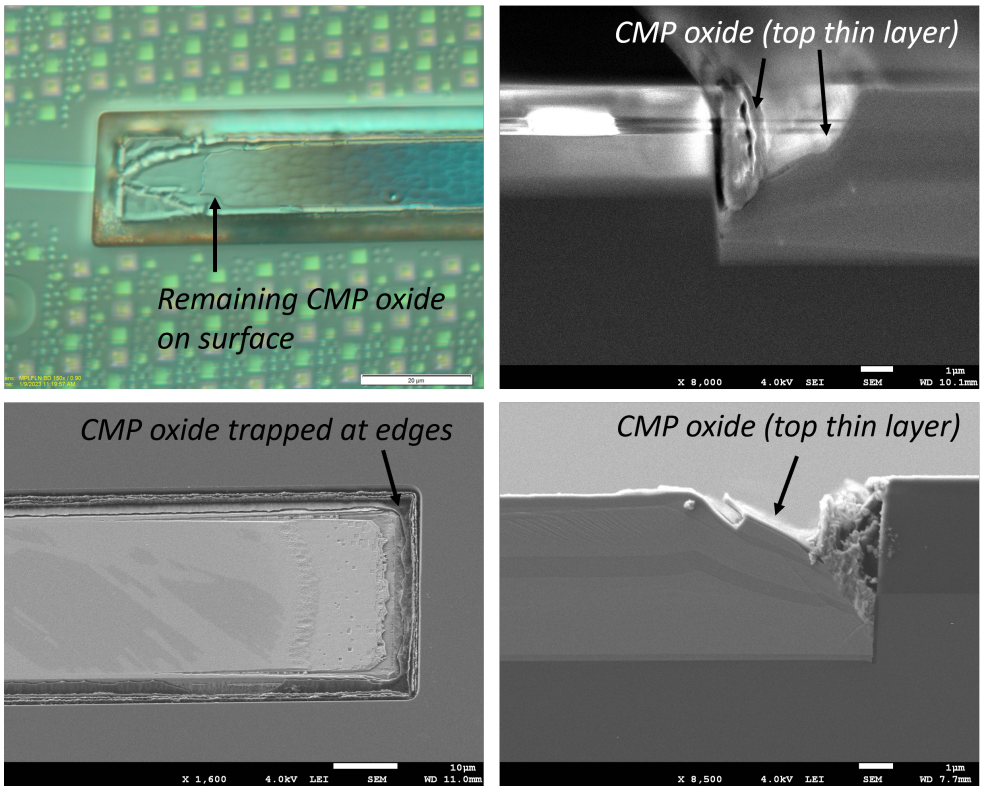


Figure 5.21: Inspections of the in-pocket material after CMP with remaining CMP oxide on surface and at pocket edges.

For the wafers with IQE 300 mm MBE growth since Dec 2022, they have undergone the CMP process for 300 mm-scale polycrystal removal and planarization. The CMP is controlled with an oxide layer deposited on top of wafer surface as a protection layer to create some buffer of reaction termination to avoid overpolishing (and overetching). However, the nature of planarization prevents the oxide on the faceting and sidewall polycrystal part to be completely removed, as they are below the horizontal plane of top epitaxial stack surface. Figure 5.21 shows some images of the in-pocket material after CMP. In the particular wafer shown in the cross-section SEM, the CMP has overetched the top surface of flat epitaxial stack and removed the p-GaAs contact, and created a bit

of undercut into the faceting part as well [11]. Even with that, the oxide protection layer is visible in the below-surface pocket corner, hardly noticeable with only a top microscope view or even top SEM view.

Experiments have been conducted to see the effect on III-V etching with or without additional wet (or dry) etch removal of the remaining CMP oxide. Figure 5.22 shows the comparison between four samples A, B, C, and D from two IQE growth with full-wafer CMP process, respectively. Sample A and D are from a wafer where the CMP has overetched the flat epitaxial surface and no remaining oxide is present in the in-pocket flat crystalline area ("IQE LICNSOI June2023"), and sample B and C are from a wafer where the CMP has been stopped at the oxide surface and a thin oxide with changing thickness [12] ("IQE MSIVSOI Dec2022").

Sample A has no treatment and directly is conducted with 8 min of the III-V dry etch using the facet etch recipe [13] with no patterning or masking. Clear residues can be seen around the edge of pocket, while in-pocket flat area is completely removed. Sample B has gone through a 5 min SiO_2 dry etch with ICP#2 recipe #101 (which has an estimated etch rate of 250 nm/min, so 5 min is enough to etch 1.25 µm of oxide), and then the 8 min III-V etch. However, even with the far extended oxide dry etch, there is no change in the sidewall residues after facet etch. Sample C and D have undergone a 5 min wet etch with BHF (the CMP oxide is Plasma TEOS Oxide, which has a HF etch rate about 4 to 5 times that of thermal oxide, as informed by our collaborator [14]), then the 8 min

[11] This is a result of height variation of in-pocket material due to MOCVD template growth rate nonuniformity, another problem we will cover in Chapter 6.

[12] This is also the result of height variation of in-pocket material due to MOCVD template growth rate nonuniformity, which will be covered in Chapter 6.

[13] All III-V dry etch in this paragraph were conducted using the developed facet etch recipe in the Oxford Cobra ICP at UCSB Nanofab.

[14] Thermal oxide etch rate in BHF 5:1 etch rate is reported to be 100 nm/min[6], so we are estimating the CMP oxide etch rate to be roughly 400 - 500 nm/min. 5 min should be more than enough to clear the CMP oxide (informed to be 200 nm original thickness). Also, just as a note, PECVD Oxide from PECVD #2 at UCSB Nanofab has a BHF etch rate around 400 nm/min, with variations due to change of film quality across time.

III-V etch. These two samples exhibit smaller grains of residues, more like short grass or dots compared to the taller wall-like structure from Sample A and Sample B. [15]

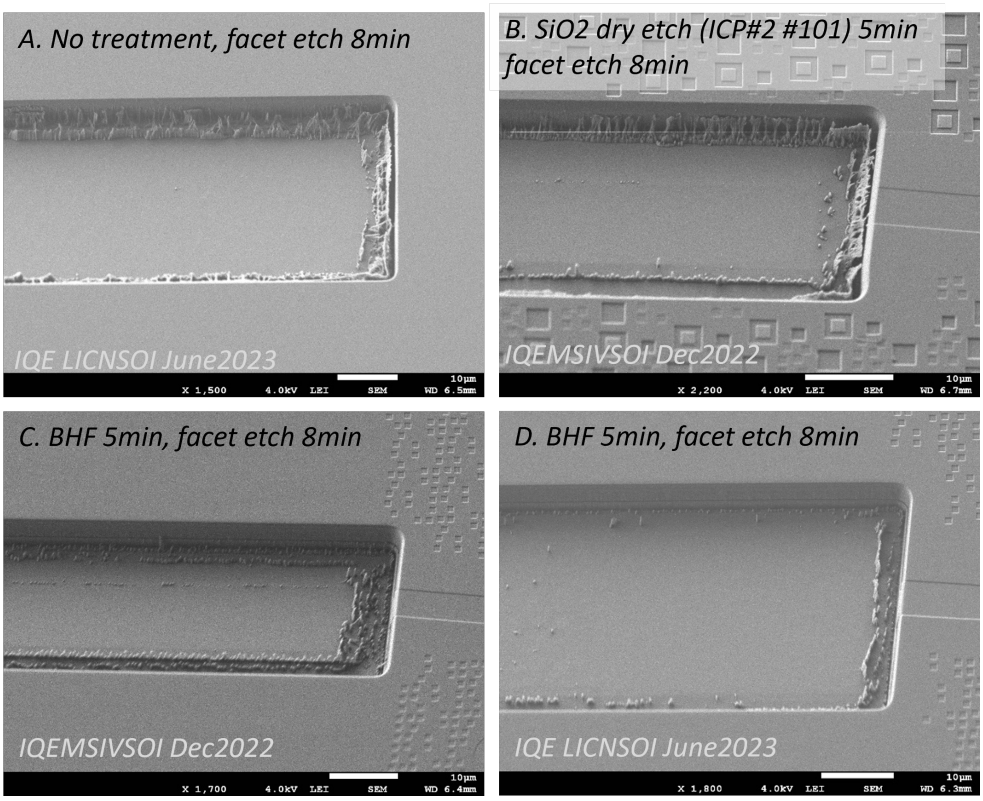


Figure 5.22: Experiments to compare III-V etching results with or without additional precedent wet or dry etch removal of the remaining CMP oxide.

With these experiments, we can see the effect of oxide shadowing in the faceting and polycrystal area at the edges of the pockets, and an oxide dry etch is not feasible to remove the excessive oxide on tilted surface. Wet etch is possible to be employed for pre-etch cleaning, with much less remnants after the III-V dry etch. Though traces of minor residues following the angled lines of the III-V surface may still remain, their height is

[15]The more apparent horizontal residue lines along the pockets from the "IQEMSIV" wafer compared to ones from the "IQELICN" wafer are a result of in-pocket defects on the templates before MBE growth, an issue we will cover later in Chapter 6, and should not be seen as a result of the variations of the etching conditions here.

much lower and will lead to a mitigated impact on the on-chip butt-coupling from etched facet laser to SiN waveguides.

However, the remaining CMP oxide on wafer is not the sole source of undesired hardmask during the facet etch. The facet etch itself employs a SiO_2 hardmask deposited using PECVD, which also acts similarly and remained in the faceting and polycrystal area after the hardmask dry etch, which also applies to the samples grown at UCSB that have gone through wet etch polycrystal removal instead of CMP. Consequently, treatment of the CMP oxide itself is not enough to clear away the "trapped oxide" problem. To fully resolve this problem, comprehensive consideration regarding materials from preceding steps before the facet etch and their respective effect needs to undertaken.

Process development of a wet-and-dry combined hardmask facet etch

An illustration is made using cross-section SEMs to elucidate the scenario described herein (Figure 5.23).

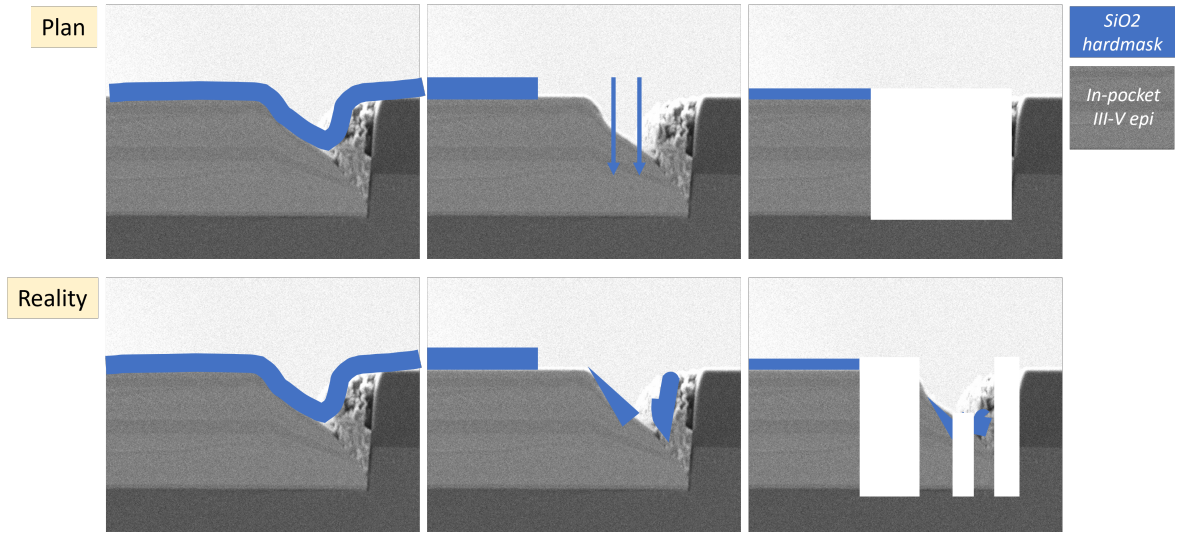


Figure 5.23: Depictions of planned versus actual scenarios regarding in-pocket facet etch with a patterned hardmask.

In the original etched-facet laser fabrication plan, the facet etch opens the oxide hardmask at the facet area with a first dry etch, and expose the III-V for the chlorine-based dry etch for removing the polycrystal and faceting material, leaving a vertical facet. However, in reality, the oxide deposition was conducted almost conformally with PECVD, with the sidewall thickness about half of that on the planar surface. Then, the chlorine-based III-V dry etch would attack the oxide surface mostly anisotropically. There is a sloped part on the wafer surface, the oxide will not be completely cleared off in the same way, which can be seen as a result of effectively very high thickness (over 2 µm when it is vertical), as shown in the illustration. As a result, the remaining or "trapped" oxide in the sloped part of the epitaxial layer will act as a "micromask" for the following deep facet etch, and leave behind tall towers of III-V remnants. This looks similar as what is usually referred to as "grassing" in dry etch, where spotty residues left on surface will give grass-like results after the etch, since the parts underneath the residue spots will not be removed. It is also generally more severe when the etch is highly selective and fast with a high bias. In this case, it's still "grassy", with the grass bigger and taller like towers, as the "micromask" is from the oxide on the sidewall instead of extra dirt or residues.

In this case, a wet etch would be effective to remove the trapped oxide near the sides of the trenches, but it wouldn't be able to create a sharp edge on the hardmask to fabricate the desired a deep and vertical mirror facet in the III-V materials. To solve this problem, a "combined etch" approach is proposed to use a wet etch and a dry etch to create the desired hardmask patterning in two steps, as shown in Figure 5.24.

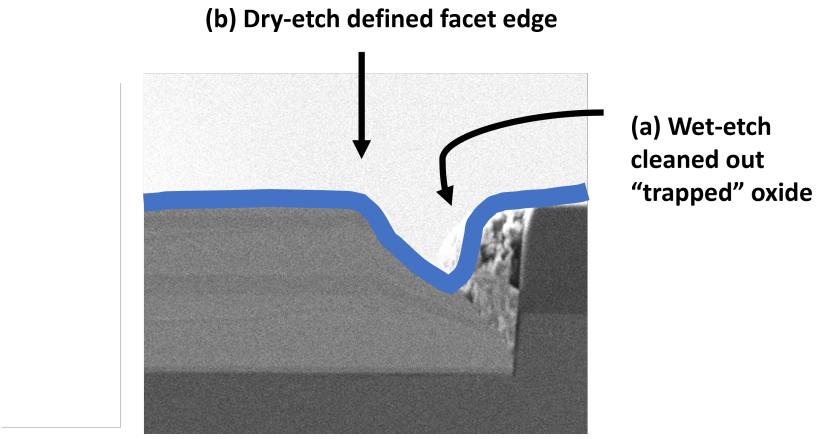


Figure 5.24: Wet-and-dry combined facet etch hardmask.

Figure 5.25 briefly depict the fabrication steps for the wet-and-dry combined facet etch hardmask and the following III-V dry etch (facet etch). Explanation of each step is listed below:

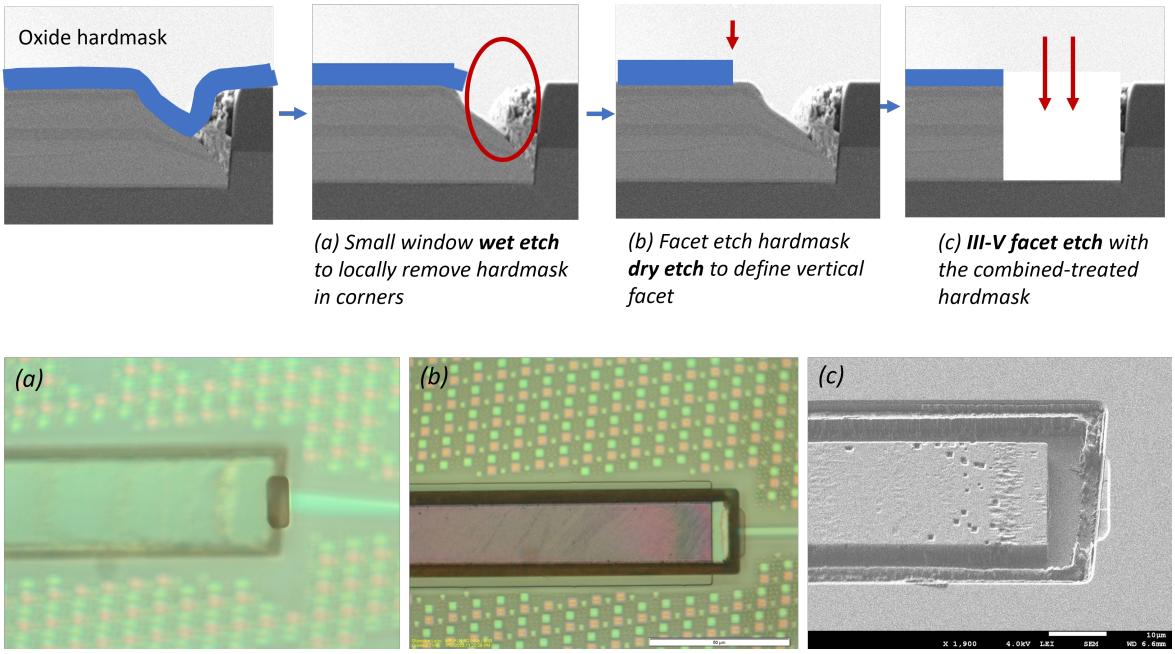


Figure 5.25: Step-by-step illustrations and top-view microscope or SEM images of the processing of III-V facet etch with wet-and-dry combined hardmask.

(a) Wet etch cleaning of the hardmask at edges: After oxide hardmask deposition, a photoresist is spun on for patterning. Firstly, a small window was opened to locally remove the hardmask with wet etch at the end of pocket where a clear coupling path is desired for on-chip butt-coupling to SiN waveguides. Figure 5.25 (a) shows a top-view SEM for the wet etch window. Note that very careful timing of the wet etch was conducted to avoid any undesired undercut. A dummy piece with oxide deposition on Si was used to calibrate the BHF etch rate for the exact same deposition tool, since different oxide film density would affect the etch rate. With the calibrated etch rate, the wet etch was timed tightly, and then carried out in short intervals with microscope inspection until a very limited undercut can be seen to confirm the complete removal of the trapped oxide. Slight color change or lightening of the shades near pocket (dark boundaries in picture) could be observed, but it was not convincingly clear, so a certain amount of undercut is still advised in this step.

(b) Dry etch defining the hardmask for the facet: Then, the photoresist is cleaned off and a new photoresist patterning is done to open a slightly larger window for dry etch to define the facet etch boundry. Figure 5.25 (b) shows a top-view of the sample after this patterning. The clear rectangle on the left is the dry etched hardmask pattern, where the slightly ragged small window on the right at end of the pocket was from the wet etch in (a). After cleaning of the second photoresist, we can confirm that there is the desired hardmask patterning without any trapped oxide on the sidewall or around the polycrystal, and with the desired sharp edge for etching the vertical facet.

(c) III-V facet etch: The sample was then ready for the III-V facet etch. The same recipe as what was developed previously in section 5.3 was used, and Figure 5.25 (c) shows an SEM image of the pocket after III-V facet etch. On the left, there was the rectangular III-V material that is preserved for the device, and a clear sharp edge is made on its right facet as the reflection mirror. On the right, the continuous "skirt"

of remaining polycrystal/faceting III-V and/or etch build-ups is no longer present where the wet-etch window was opened. Note that (b) and (c) are not from the exact same pocket and they did have different splits of the dry-etch rectangle pattern, as (b) had it wider than the pocket width and (c) had it more narrow, yet it does not affect the desired results at the coupling region near the pocket end.

More details of the parameters and step-by-step handling instructions are included in the process follower in the Appendix.

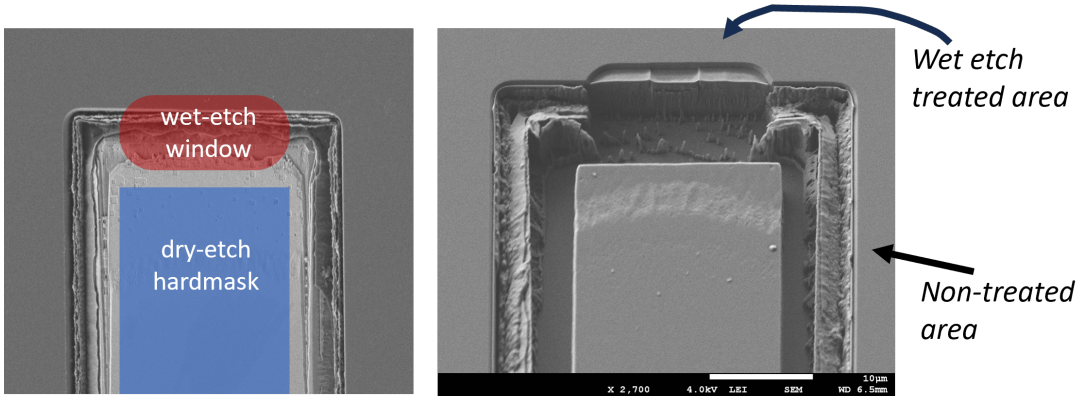


Figure 5.26: Tilted SEM of the pocket showing facet etch test results with wet-etch treated area and dry-etch hardmask edge.

Figure 5.26 shows the tilted SEM of the pocket with a clear view showing the difference between pocket edges inside and outside the wet-etch window. The sidewall build-up is clearly visible for the area outside the wet-etch window, with its profile similar to what was seen before. Inside the wet-etch window, there is distinctively no build-up of anything, leaving an air gap at pocket end and exposing the oxide sidewall containing SiN waveguide couplers.

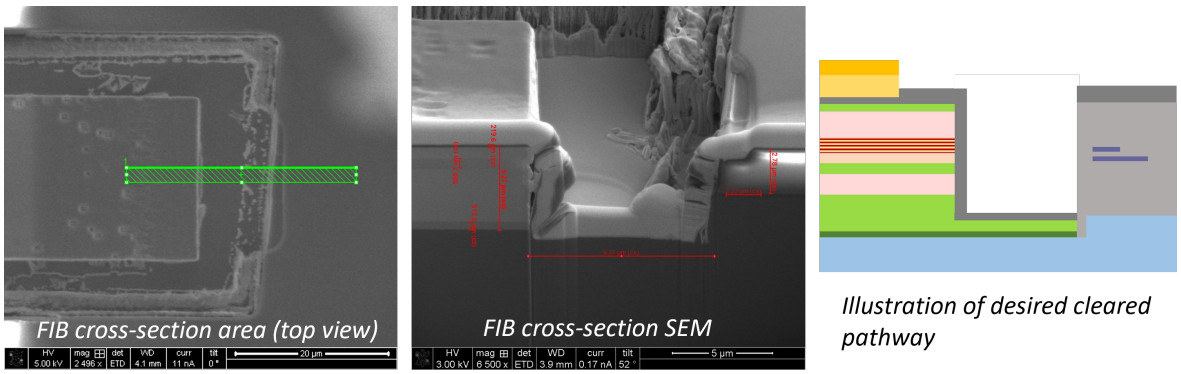


Figure 5.27: FIB cross-section SEM at pocket end after the developed facet etch, compared with a schematic of the desired cleared pathway.

To further inspect the coupling region, we obtained FIB cross-section SEMs of the test sample. Figure 5.27 shows the FIB cross-section alongside with an indication of the spot where the FIB was taken. The coupling region is cleared with no remnants of III-V materials present (as a comparison, in the distance one could see that they still build up outside the wet-etch window). Additionally, the vertical sidewall is ensured by the dry-etch defined hardmask edge. The cross-section closely resembles the illustration of the desired cleared pathway with vertical facet presented at the beginning of this section in Figure 5.19.

Some overetch of the oxide outside the pocket above the SiN waveguide is observed in the test samples, attributed to an overlap of wet etch window pattern outside the pocket edge, as depicted in the window in Figure 5.26. The overlap was intentionally included in the layout pattern of the test samples to see how much of oxide will be etched as a reference. In the actual fabrication process, the overetch can be mitigated by aligning the wet-etch window edge with the pocket edge. Subsequent refinements to the process, such as more careful wet etch time control and tighter clearance between the wet-etch window and dry-etch boundary to reduce the coupling gap, were implemented through the two complete device fabrication runs. The fabrication results will be discussed in

the later sections. Detailed enhancements are also included in the process follower in the Appendix.

Concluding remarks on the fabrication developments

The combined hardmask patterning for the facet etch introduces one additional wet etch pattern that calls for careful decisions in mask layout dimensions, delicate wet etch timing control, which adds the complication and risk to the fabrication process. However, it is one solution that can be adopted in this heteoepitaxial integration scheme and solved the unprecedented problem with on-chip butt coupling. Further discussions on this method and its implications will be included in the later Section 5.5. For now, we will conclude with this developed step and move on to the first demonstration of etched-facet lasers coupled to foundry-processed SiN waveguides using this facet etch.

5.4.3 Etched-facet lasers coupled to foundry-processed SiN waveguides

Device fabrication and preliminary testing

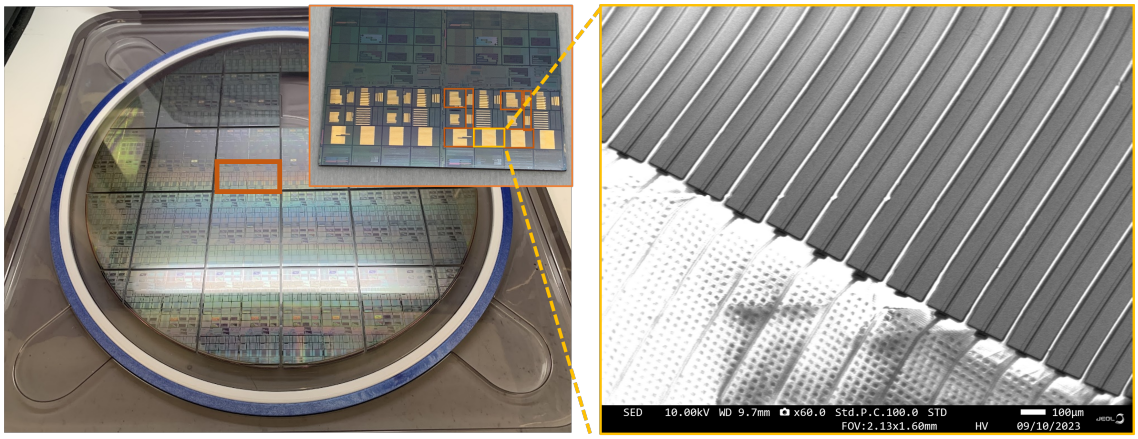


Figure 5.28: Fabricated sample from 300 mm growth on SOI wafer, and bird's eye view SEM of in-pocket etched facet cavities coupled to SiN waveguides.

Device fabrication was carried out with the newly developed combined hardmask patterning for facet etch incorporated into the existing process. Rest of the process is kept similar as previous runs, with only minor adjustment of mask dimensions to further improve the yield and performance. Figure 5.28 shows a bird's-eye-view of the finished devices. Etched facet with clear pathway next to on-chip SiN waveguides can be seen. The inset shows an overview picture of the chip, where the chip dimension is 52 mm × 32 mm with two identical dies (each 26 mm × 32 mm). On-chip etched facet lasers were yielded in areas marked out in red rectangles. 76 lasers were made.

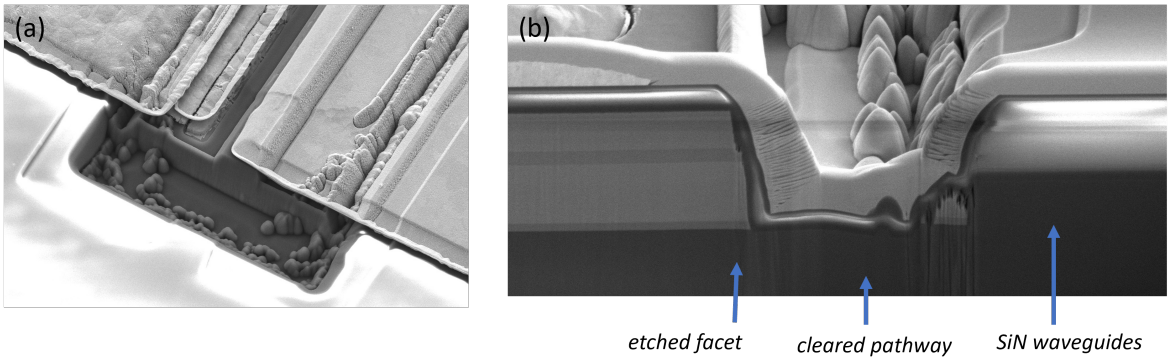


Figure 5.29: (a) SEM of the etched facet and cleared pathway at pocket end. (b) FIB cross-section SEM showing the etched III-V facet, cleared pathway from combined wet-and-dry hardmask method, and the SiN waveguides in oxide.

Figure 5.29 shows the (a) angled-view SEM and (b) FIB cross-section of the coupling region fabricated on these devices. Sharp facet with cleared pathway is confirmed, showing the successful incorporation of the combined hardmask facet etch step into the total device fabrication.

From Figure 5.29 (b), we can see that the etched facet angle is still not ideal in some areas, and this may be attributed to loading effects or change of etching condition in the chamber, and further improvements can be made to increase the facet mirror quality. The rounding of the oxide cladding on the waveguide side (right side in this image) is also concerning as one of the factors that will affect coupling efficiency.

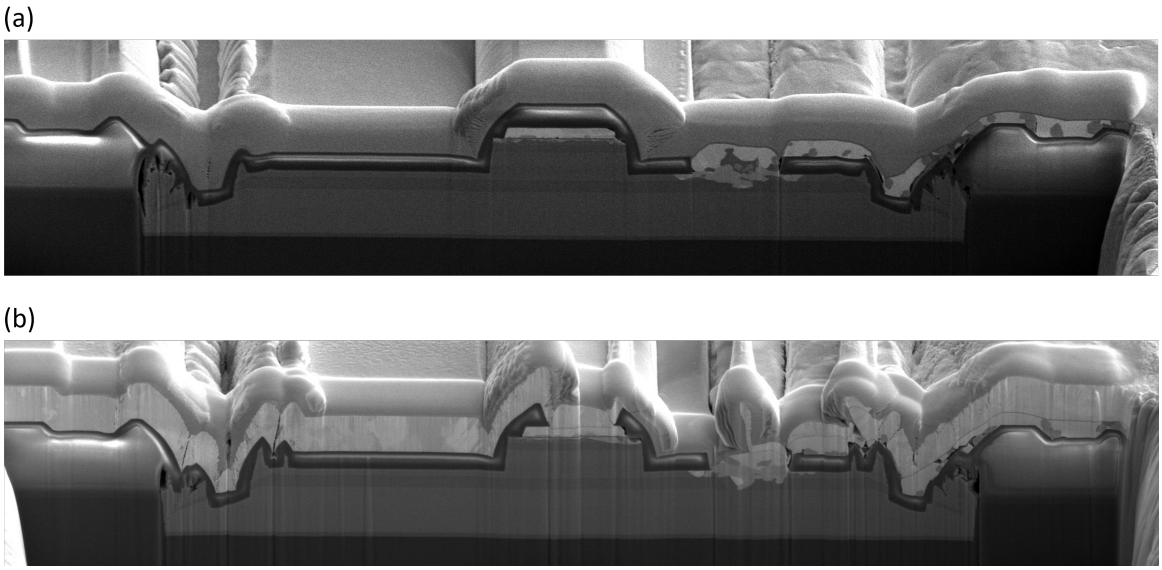


Figure 5.30: FIB cross-section SEMs of the device. (a) In the middle of fabrication process before p-via etching and probe metal depositions, and (b) after probe metal and additional probe metal patching.

Figure 5.30 shows the FIB cross-section SEMs of the device, both (a) in the middle of fabrication before p-via and probe metal, and (b) after probe metal. Good dimension control of the p-contact metal, mesa width, n-contact and n-via can be clearly observed, and the mesa sidewall appears vertical as desired. The mesa etch was terminated at the n-contact layer (about 300 nm above the lower cladding) as designed. The passivation covers the remaining polycrystal and faceting slops and the probe metal wiring was connected after the additional probe metal patching. The devices showed good I-V performance withstanding injection current as high as 1.5 A or above [16].

[16]Note that the first probe metal deposition has left many devices burnt open after the initial screening with higher current, and we found out it was due to the discontinuity at the step from inside to outside n-via edges. An additional strip of probe metal ("patching") was then added to the samples, where the lift-off edge can be observed in Figure 5.30 (b) with two ears near the right edge of n-via. Details of this process and better control for probe metal was covered in Chapter 4. Section 4.

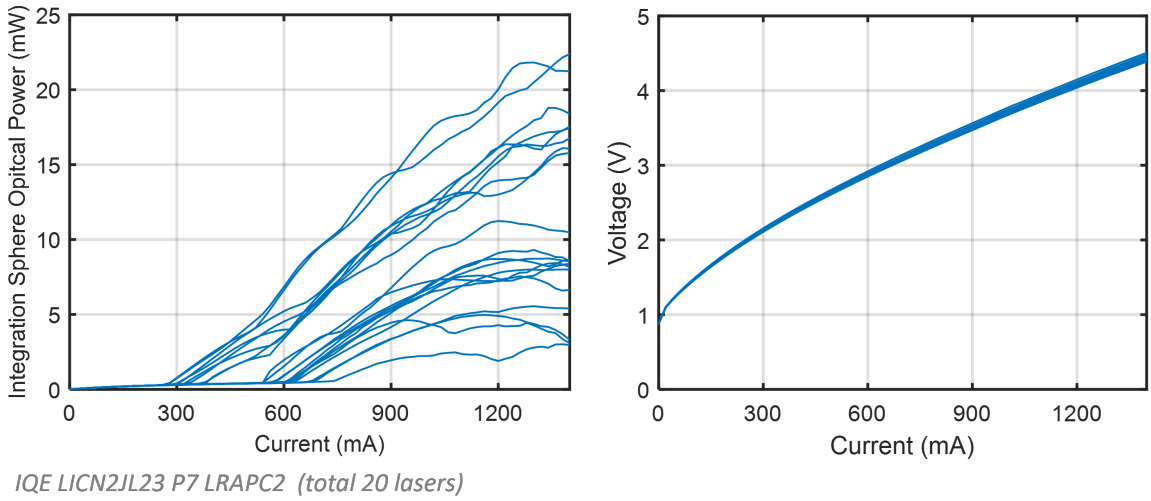


Figure 5.31: LIV measurement of 20 etched facet lasers of the same length 3 mm and width 6 µm yielded from the same region on sample.

The LIV measurement of one region of 20 lasers (yield 20/22) of the same length 3 mm and width 6 µm is shown in Figure 5.31. The data was taken before any dicing or cleaving. The power shown here was taken by integration sphere on one side of the chip, which can be considered mostly scattered light from top of the bar as well as the etched facet region. The highest single-side collected power is over 20 mW, and the medium result is about 10 mW - 15 mW. These numbers do not stand for the actual total output power of the lasers, but should be taken as only indications of their relative performance.

Metal reflector coating for lower mirror loss on etched-facet lasers

In the fabrication run above, we noticed clear difference of two groups of threshold current from the same device footprint from the same bar, with threshold current one around 300 - 400 mA, the other around 500 - 700 mA.

This is discovered to be a result of accidental metal cladding on the left-side etched facet of some devices, due to a mismatch in a left-side aligned in-pocket laser processing

layers layout and the ragged pocket alignment from our collaborator's design from the splits in SiN coupler tilted angle. As a result, the probe metal covers the etched facet (which was produced aligned to the raggedly arranged pockets) on some devices. Assuming the feedback from left-side SiN waveguide was weak and the difference in SiN coupler tilted angle will not affect the threshold current of the devices, the lower threshold current should be a direct result of the lower mirror loss with the highly-reflective metal cladding. This is backed with careful sorting of the device performance and their designs.

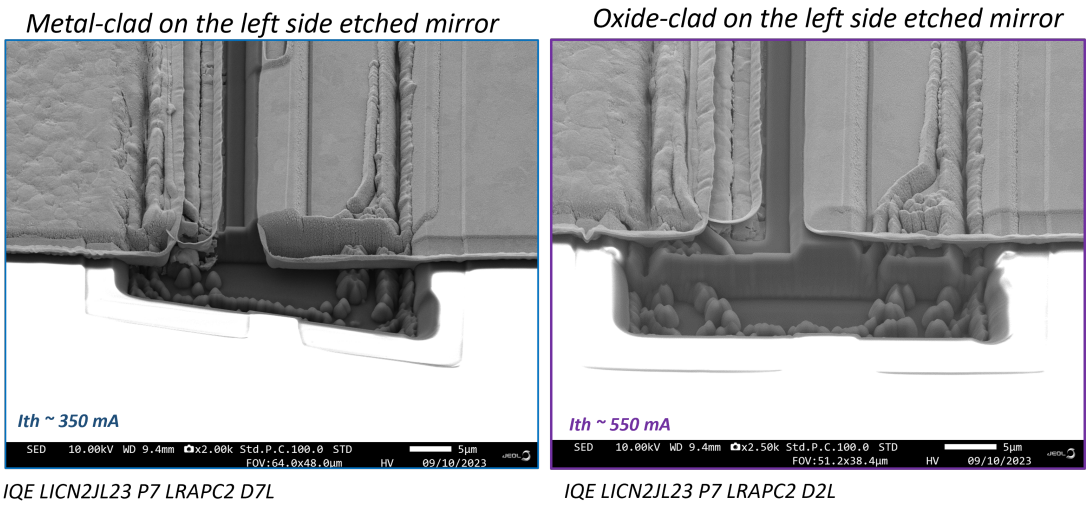


Figure 5.32: Tilted-angle SEMs of the devices with and without metal cladding at the left-side etched facet.

Figure 5.32 shows the tilted-angle SEMs of the left facet of two devices, one with metal cladding (D7) and one with only passivation on etched facet (D2). They are from the same bar and have the same footprint of about 6.5 µm × 3 mm. The passivation between the etched III-V facet and the metal comes from the post-facet etch oxide deposition and the post mesa-etch oxide depositions[17], and the metal cladding is composed

[17]For oxide thickness and details of the deposition steps, please refer to the process follower in the Appendix.

of Ti/Au 22 nm / 1.5 µm from the probe metal deposition.

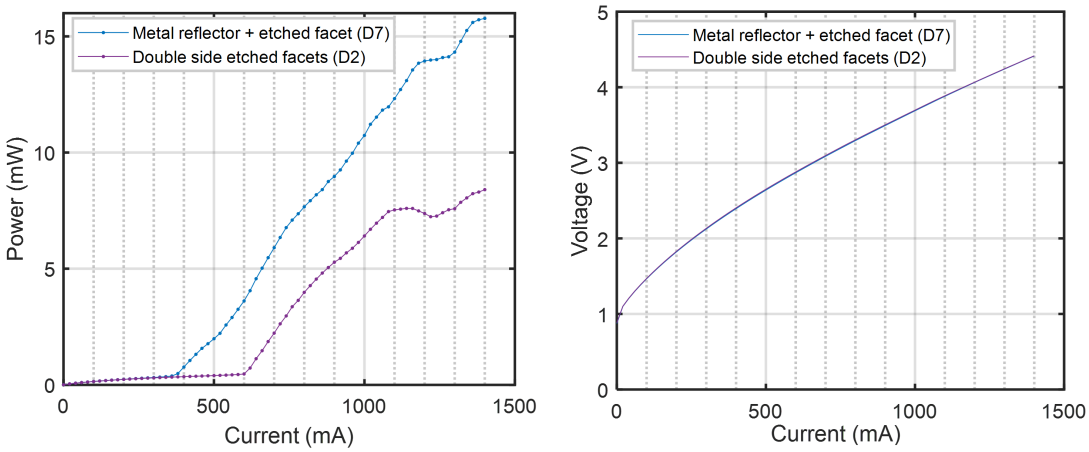


Figure 5.33: LIV characteristics of the devices with (D7) and without (D2) metal cladding at the left-side etched facet.

The LI and IV characteristics of the two devices are compared in Figure 5.33. The threshold current of D7 (metal cladded) is about 350 mA, and D2 (etched facet only) about 550 mA, corresponding to a threshold current density of 1800 A/cm^2 and 2800 A/cm^2, respectively. With comparable slope efficiency, D7 with metal reflector reached a maximum output power over 15 mW at current of 1.4 A, which is almost double the output power of D2 at the same injection level (8.4 mW at 1.4 A). The IV comparison shows almost identical electrical performance of the two devices, with a series resistance lower than 2 Ω at higher injection current.

In the second process run for making lasers coupled to SiN waveguides, we specifically redesigned the mask to make metal-cladded facet on the laser. Though the overall device performance and yield was worse than the first-batch results, we confirmed clear advantages of metal-reflector for reducing mirror loss, as the majority of lasers yielded only from the metal-cladded design. Further testing is still ongoing for the chip (as of Feb 2024).

Fiber-coupled measurement results

After characterization of the etched-facet lasing, fiber-coupled testing is needed to characterize the coupling between laser and the SiN passive waveguides. We first tested a bar with the etched-facet laser section designed to connect to SiN couplers and waveguides on both ends, with edge couplers at both terminations for fiber coupling.

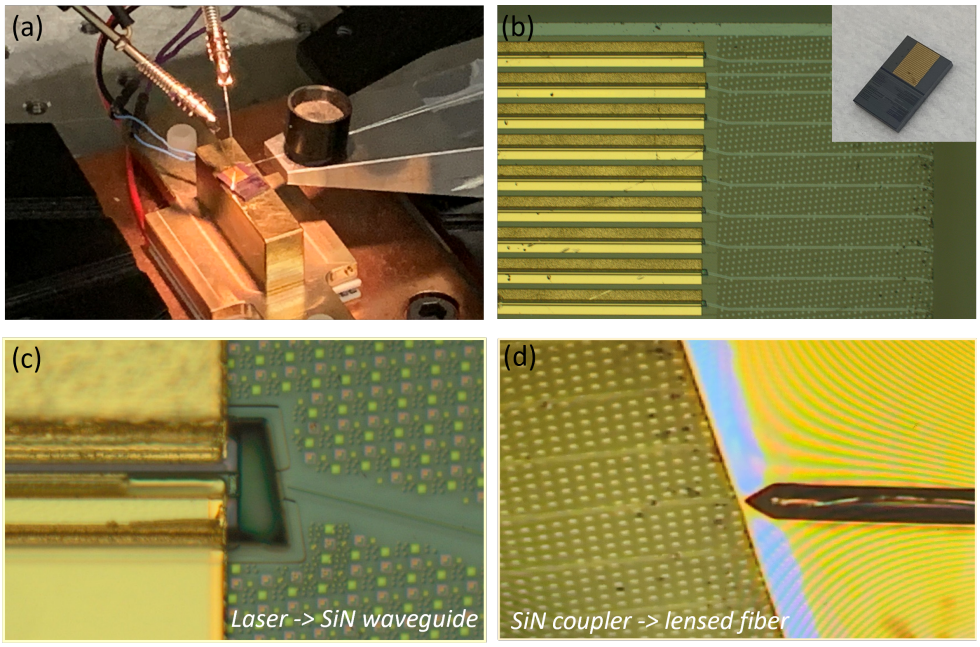


Figure 5.34: Experimental setup of the fiber-coupling experiment. (a) Diced sample on testing stage with electrical probes for current injection and single-side fiber coupling. (b) Top-view microscope image of the diced-out chip, inset showing the chip with size around 5 mm × 10 mm. (c) Top-view microscope of the on-chip III-V to SiN coupling region. (d) Microscope camera display of the coupling region between SiN edge coupler and the lensed fiber.

Dicing was performed at the dicing streets with facet polishing for a smooth finish at the end of edge coupler tips. Figure 5.34 (a) shows the experimental setup, where the diced-out chip is placed on top a stage with TEC temperature control at 20 °C, and a lensed fiber is brought in from the right side, (b) shows a top-view microscope image of the diced-out chip, with the inset showing the chip sizing around 5 mm × 10 mm.

The cavity lengths are about 3 mm. (C) shows the coupling region between the etched laser facet, pocket end as well as the SiN coupler tip, and (d) shows the coupling region between the SiN edge coupler and the lensed fiber at one side of the chip.

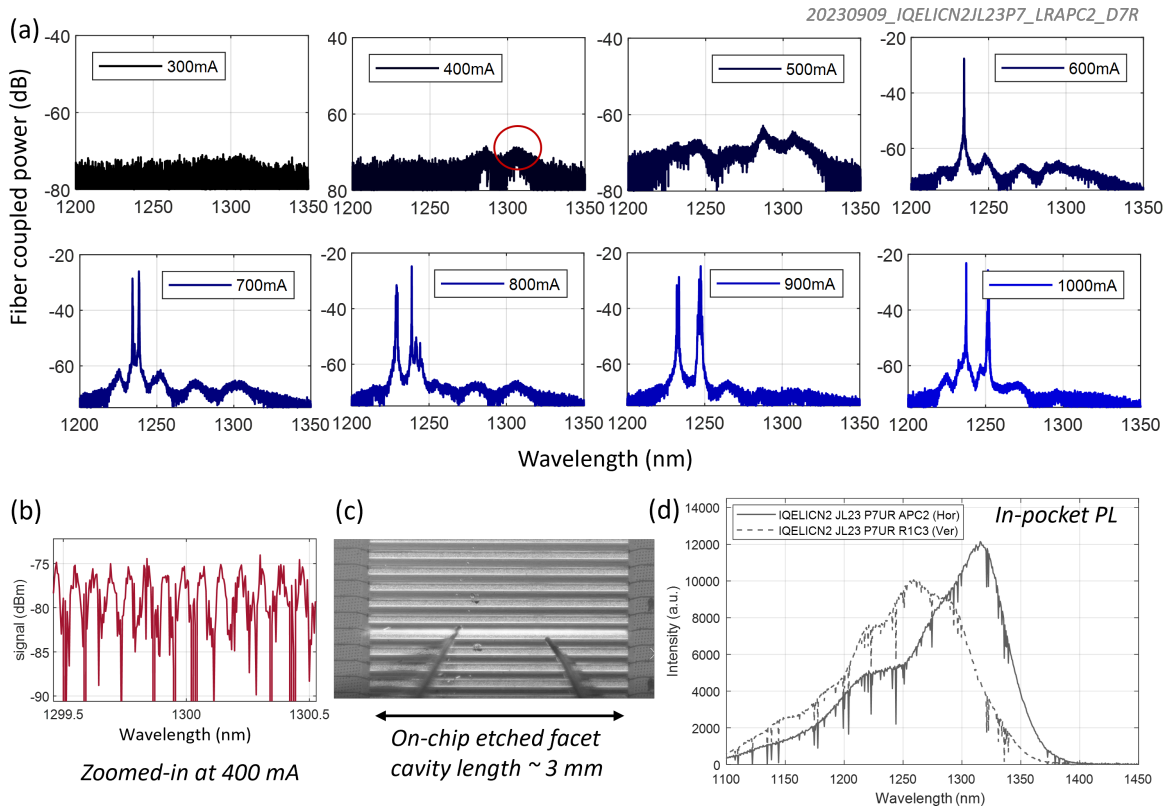


Figure 5.35: (a) Spectra of device D7 under different injection currents. (b) Zoomed-in of spectra showing FSR around wavelength of 1300 nm at 400 mA. (c) Top-view microscope showing on-chip cavity coupled to SiN waveguides, while being probed at testing stage. (d) In-pocket PL measured from the same area on an adjacent die from the same wafer.

The spectra of device D7 (threshold current is around 350 mA) under different injection currents below and above threshold is shown in Figure 5.35 (a). Ground state lasing around 1300 nm can be observed at lower injection current, and additional peaks representing excited states show up as the current increases. There appears to be multiple excited peaks coexisting, with wavelengths ranging from as short as 1220 nm to

closer proximity of 1300 nm. The lasing spectra is consistent with the in-pocket PL (d) of the horizontal pockets measured from the same wafer (from one die above the fabricated sample), in same area[18]. Zoomed-in plot of the spectra near 1300 nm at 400 mA injection current is shown in (b), and the free spectral range (FSR) spacing is measured about 0.0769 (1/13) nm. With the FSR estimation equation and the group index of 3.56 from the MODE simulation of the laser (presented earlier in Chapter 3), one can get:

$$\begin{aligned} \text{FSR}\,\Delta\lambda &\approx 7.69 \times 10^{-5}\,\mu\text{m} \\ \text{Cavity}\,L \approx \frac{\lambda^2}{2 \cdot n_g \cdot \Delta\lambda} &\approx \frac{1.3 \times 1.3\mu\text{m}^2}{2 \times 3.56 \times 7.69 \times 10^{-5}\mu\text{m}} \\ &\approx 3087\,\mu\text{m} \approx 3\,\text{mm} \end{aligned}$$

The estimated cavity length of the resonance is about 3 mm, which corresponds to the cavity/pocket length of the etched facet laser, as shown in the microscope image in (c). Determining additional reflection from either the pocket facet or the SiN coupler interface is challenging due to the small air-gap distance of about 11 µm at the pocket end, and the noise in the FSR spectrum needs further investigation. For this specific device, we anticipate minimum reflection from the pocket facet due to its angled pocket design of the 10 °tilted edges on both ends [19]. In summary, we demonstrated lasing from etched-facet lasers with a single-side metal reflector and showcased fiber-coupled laser characterization through the SiN waveguide integrated with the laser through on-chip in-plane coupling.

[18]The solid line and dashed line in this PL measurement shows the measurement taken from "horizontal" and "vertical" pockets that align to the [1 $\bar{1}$ 0] and [1 1 0] III-V crystal orientation respectively. The measured lasers were made from "horizontal" pockets, which explains the 1320 nm peak at ground state, consistent with its PL. Further discussions on the difference in quantum dot PL wavelength with different pocket orientations will be covered in Chapter 6.

[19]Discussion on splits of angled pockets and different coupling configurations were included earlier in this chapter. See around Figure 5.2

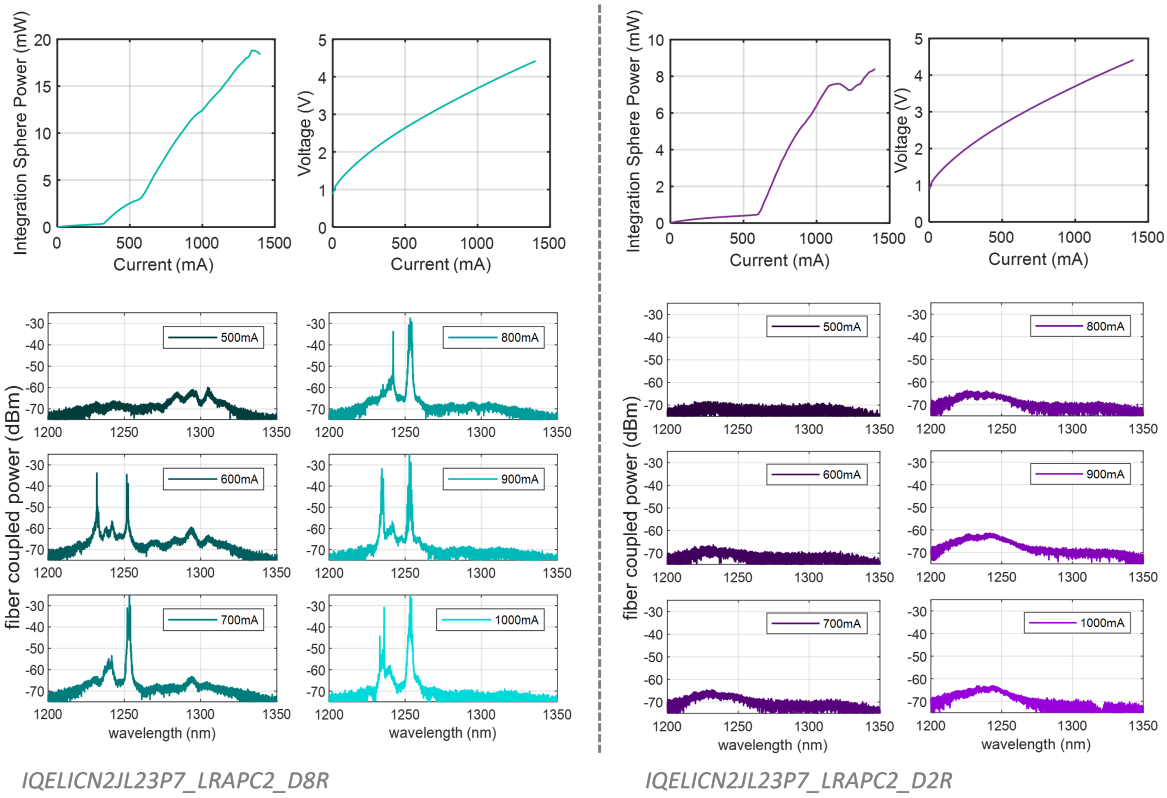


Figure 5.36: Additional integration sphere LIV characteristics and fiber-coupled spectra measurement results from (a) etched facets with single metal reflector D8 and (b) double-side etched-facet-only D2.

Additional spectra measurement results are shown in Figure 5.36, together with the LIV characteristics taken from the integration sphere during initial screening. The left (D8) is a device with metal reflector, and its threshold current is around 300 mA, the right (D2) is a device with two etched facet shown earlier in the comparison, with a threshold current of about 550 mA. Spectra of D8 is similar to D7, with initial ground-state peaks followed by multiple higher intensity excited peaks tightly above threshold. For device D2 with higher threshold current density, only excited state peaks were observed and the overall intensity is weaker.

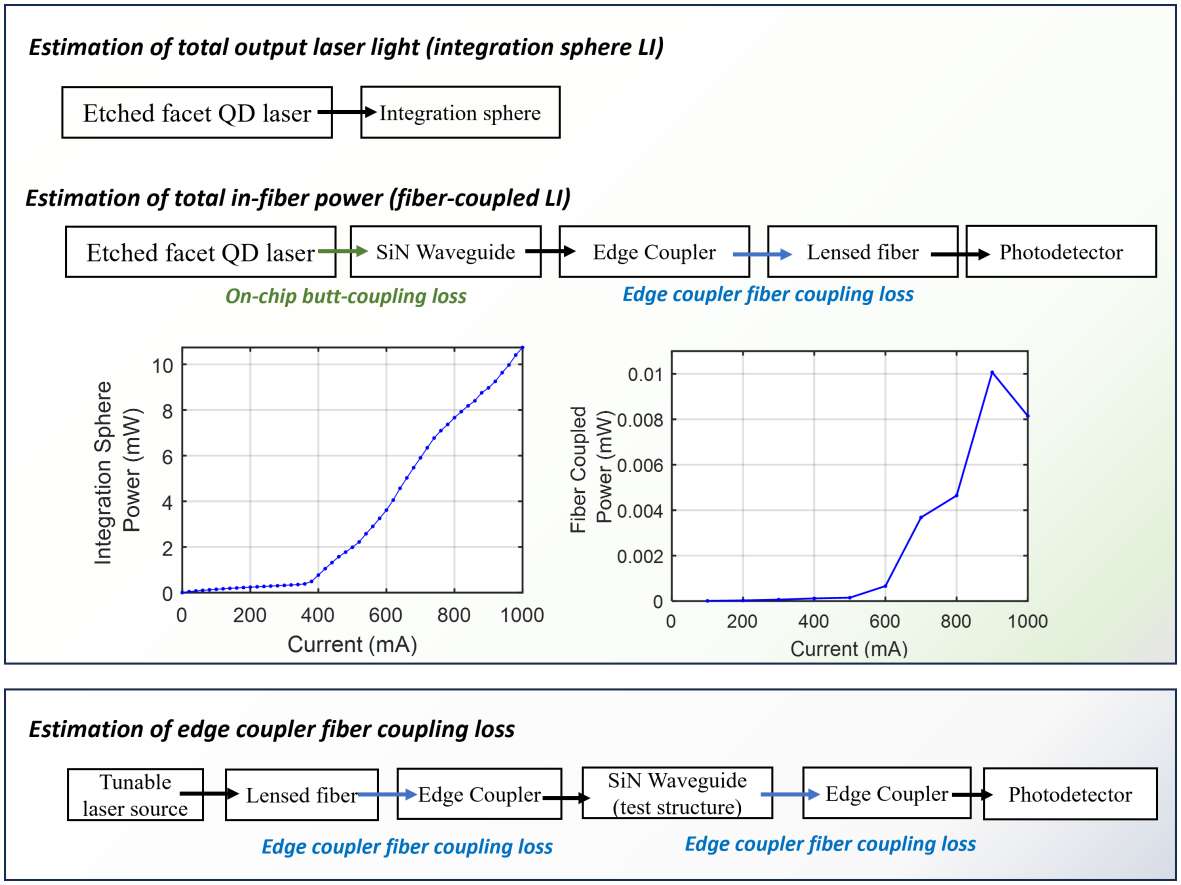


Figure 5.37: Fiber-coupled LI versus integration sphere LI results of D7, and experimental concept for estimation of coupling loss.

To estimate the fiber-coupled power, we measure the device LIV in a turn-key manner with a photodetector from the fiber output, and the result is plotted in comparison to the integration sphere (collecting all emitted and scattered light) LIV in Figure 5.37. The detected value is approximately 30 dB lower than the integration sphere power, which raises concerns about the overall coupling loss in this measurement. The coupling loss is a result of both on-chip butt-coupling from the laser to the SiN coupler, as well as the fiber coupling between the diced and polished SiN edge coupler output and the horizontally placed and aligned lensed fiber at the chip edge.

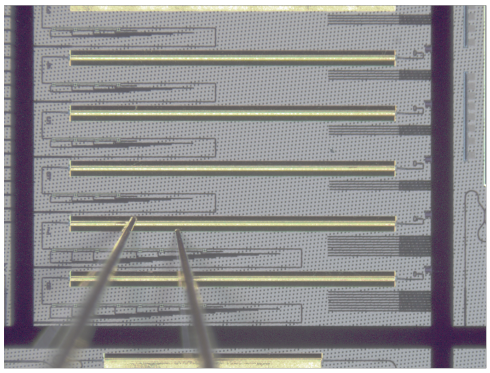
We were able to utilize the test structure on-chip with simple back-to-back edge

coupler with SiN waveguides on the same diced bar to estimate the coupling loss from the edge coupler to fiber, as depicted in the bottom of Figure 5.37. The estimated loss is very high as 20 dB/facet, far beyond our expectation [20]. With this number, we estimate the on-chip laser to SiN coupling loss of about 10 dB. However, it is premature to claim this number without further experiments to validate the edge coupling loss. We attribute the high edge coupling loss to damages and/or variations in facet polishing, and uncertainties of edge-coupling loss difference among different devices across the same bar can be introduced subject to imperfect angular alignment in mounting for facet polishing. Given the current edge coupler design from our collaborator's PDK library on this platform, it is better to substitute the dicing and facet polishing step with a deeply-etched trench at the edge coupler output as intended for vertical fiber array coupling (with wafer-level testing compatibility). This technology is available at foundry level, and an equivalent process for samples fabricated in small pieces is currently under development at the UCSB nanofab.

On the other hand, even the estimated number of 10 dB on-chip coupling loss from laser to SiN waveguide is higher than desired for efficient integration. Simulation of the coupling loss with the current configuration, discussions on improving the coupling efficiency in the current scheme or with different strategies, and a summary of current ongoing efforts will be covered in detail in Chapter 6.

[20]The PDK expectation value is less than 2.5dB/facet at 1260 - 1360 nm (mode field diameter of 5.0 µm) for coupling to an UHNA 1 fiber. Potentially, higher loss can also be attributed to the shorter lasing wavelength falling out of the "spec" range, but it shouldn't be as high as 20 dB.

QD lasers with on-chip coupling to external Si/SiN cavities



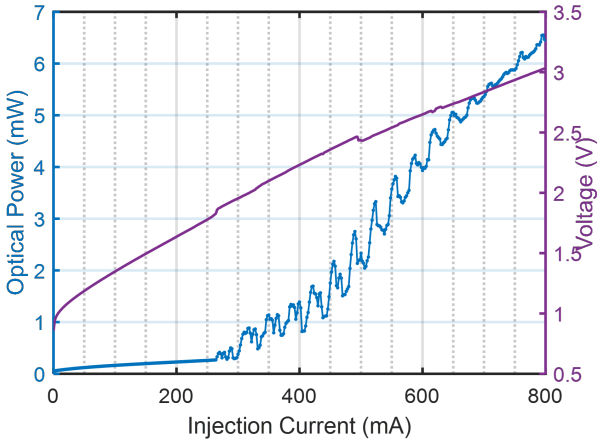


Figure 5.38: Top-view microscope image of the designed integrated laser with external cavities. LIV of the device showing mode-hopping with increasing current injection.

In the second attempt of fabrication run with adjusted designs adding metal-coating on one etched facet as an HR mirror, and with improved growth conditions from UCSB growth with no CMP damage regarding the MOCVD non-uniformity, and shorter facet-to-pocket distance with partial selective MBE growth [21], we have yielded a few on-chip metal/etched facet lasers with 3 mm length and designed with integrated external cavities for wavelength tuning. Figure 5.38 shows a top-view microscope image of the finished device being probed on test stage, and the right shows the LIV characteristics collected with an integration sphere adjacent to the fabricated sample.

The ripples appearing in the LI trace are typically not observed in those designed to couple only to straight waveguides or Sagnac ring reflectors. It suggests a high degree of coupling to the designed external cavity mirror containing silicon micro-ring resonators.

[21] Discussions on the effect of CMP damage and MOCVD non-uniformity on yield is included in Chapter 6 "Challenges with yield and scaling", discussions on the partial selective MBE growth on improving coupling efficiency is included in Chapter 6 "Challenges with coupling efficiency".

The ripples could possibly be perturbation of the laser output power attributed to non-linear phase shifts introduced by the significant energy in the rings from self-heating [7]. The integration design of the external cavities was performed by our colleague Andrew Netherton and further research and testing is currently ongoing.

This result highlights the potential for efficient coupling and production of highly-functional integrated lasers, such as tunable lasers, single-wavelength lasers from the platform.

Additional testing on the emission spectra is needed and we are planning further characterizations with the etched trenches for sample-scale vertical fiber edge-coupling to ensure reliable and stable fiber-coupling control, as mentioned in the previous section[22].

5.5 Summary and outlook

The experimental results confirm the world's first demonstration of on-chip butt-coupling of QD lasers to foundry-processed SiN waveguides on 300 mm SOI wafer, to the best of our knowledge. The process development of the design and fabrication recipe of the vertical facet etch in ridge waveguide lasers has laid down the foundation of gain material definition with in-pocket growth on Si wafers. The combined hardmasks patterning method for on-chip butt-coupling region definition proposed and demonstrated to cope with non-selective in-pocket heteroepitaxy has been proven a critical step in pushing through higher coupling efficiency and reduced scattering loss.

Comments on improving coupling efficiency

Further analysis on coupling loss as well as proposed methods to improve coupling efficiency either with the current MBE growth and etched-facet fabrication scenario or

[22]Details on the vertical fiber edge coupling for wafer-scale testing is also included in Chapter 6, in "Improvements of measurement technology".

with novel hybrid MOCVD/MBE growth solutions will be included in Chapter 6 Section 6.4.

Comments on etched facets and metal reflectors

The idea of using etched facet as mirror for the on-chip cavity started as a makeshift to provide sufficient gain section output for the demonstration of successful on-chip coupling, given the complication of pocket-end growth that went beyond the initial expectation and the coupling loss would be too high to characterize the cavity as an SOA [23], and turned out to yield our first-demonstration results. In addition, the "happy accident" of mis-aligned probe metal with the integrated pocket layouts has led to better device performance with lower threshold and higher maximum output power, likely attributed to the lower effective mirror loss with metal coating.

We followed up with careful evaluation of using intended probe-metal coating on one etched facet as an effective "high reflection" (HR) coating (while the other left as passivation only etched facet), and an additional fabrication run was conducted. The fabricated devices with coated metal reflector have shown consistently better performance than the ones without metal coating. Notably, the fabrication method for the metal reflector remains wholly straight-forward, requiring only a modification of the probe metal deposition boundary, as illustrated in Figure 5.39.

Further experiments to quantify the reflection of on-chip metal reflectors and verify the reliability is recommended. We have not observed catastrophic damage at the passivated etched facet or metal-coated facet yet, and if proved highly reliable, this design can be extended towards other integration schemes with in-plane or evanescent coupling, such as micro-transfer printing, bond and regrowth, or heterogeneous integration. This

[23] One might have noticed from the top-view images - we designed many sagnac ring reflectors connected to both ends of the cavity in the first generation of integrated design, hoping to make external cavity lasers with the platform.

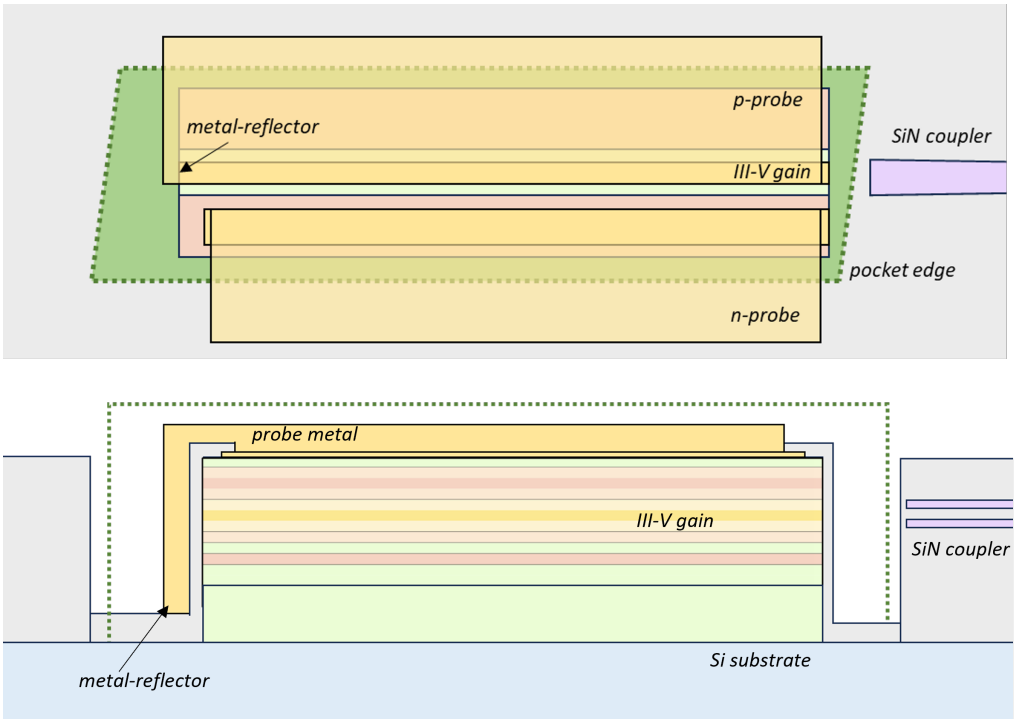


Figure 5.39: Schematic illustration of the probe-metal coated metal reflector for on-chip etched facet laser.

naturally provides a working alternative that bypasses the difficulties of making traditional interference-based dielectric layers HR coating on an integration platform without cleaved facets.

Comments on process development for on-chip in-plane butt-coupling of III-V to SiN

In order to address the polycrystal and faceting materials near pocket edges at the growth interface and create a clear pathway between the growth interface and the passive area, we developed the wet-and-dry combined hardmask for removing uneven material in a tightly constrained footprint. For this specific problem, there are alternative engineering solutions such as using angled etch or fabricating additional grating structures to re-direct the light upward and then back into the horizontal plane as a bypass to the pocket-

end region. However, these methods either require more complex consideration, process development and fabrication precision or appear to be not suitable in a scalable approach for a foundry process. Therefore, they were not at the forefront of our considerations.

Extending further, the issue of removing material with an uneven surface was not entirely an isolated case that applies only to this specific integration scheme. The complication appears unprecedented as most cases of III-V fabricated started with flat layers of epitaxial material, and pocket geometry edges are inherently different in this manner. With the recent development of compact integration scheme of III-V and Si photonics, there has been more cases dealing with increasing intricacy in handling integrated materials.

For example, when conducting die-to-wafer bonding of cleaved-out III-V pieces to Si wafer, the cleaving edge of the III-V pieces may contain a line-up of residues from the cleavage, acting like a low "fence" at end of the epi. In the subsequent III-V component fabrication steps, such "fence" would pile up higher through steps such as hard mask deposition and dry etches, and will remain almost impossible to remove unless using a combined method of strong acid wet etch with photoresist protection in center of the epi, or even using a razor blade to scratch off as an alternative. Another example is cases such as micro-transfer-printing for butt-coupling regime [8], where the fabricated laser cavity will be transfered into a slot on patterned SOI wafer with a thin layer coating of BCB, and the BCB will curl up and become effectively thicker near the end of the slot, creating an uneven surface that prevents the laser cavity to be transferred as-flat at very close proximity to the waveguides on SOI. These on-chip butt-coupling schemes are still in the initial demonstration phase. Moving forward, closer investigations into material thermal properties and integration reliability through extended aging will be necessary. This is akin to the preceding example of heterogeneous integration, where the bonding by-products absorbed in the buried oxide layer at bonding interface causing local-

debonding and interface void formation was discovered and addressed with additional vertical outgassing channels [9].

With the growing demand of compact integrated co-processing of III-V and Si photonic components, the development of new techniques and processes regarding engineering the integration interface will continue to be challenging and continue to require innovative solutions. As the standard fabrication process becomes more established, we expect addressing challenges at the integration interface will shift to become a focal center for translating academic results into practical applications in the industry.

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Chapter 6

Perspectives on scaling QD laser process on a 300 mm scale with SiPh foundry process

6.1 Introduction

This chapter shows some perspectives on the scaling of on-chip monolithic integration of QD lasers towards a 300 mm scale Si photonics foundry process.

We start with a review of the project upon which this thesis is based, and an overview of the generations of integration design, wafer processing and device fabrication involved in the research conducted from 2020 - 2024, which produced the results in Chapter 3 - 5.

We dedicate the following sections to provide some detailed discussions. Research on improvement of in-pocket QD quality for the monolithic integration platform will be included, summarizing learning through characterizations of 300 mm growth attempts and fabrication results involved in this project. We will also review some spin-off experiments elucidating the mechanism behind in-pocket QD growth by MBE. Then, we will

discuss the challenges with on-chip butt-coupling efficiency in the current scenario, supported by optical simulation results and their implications. We discuss a list of proposed methods for improving the coupling efficiency, from either a fabrication approach or innovative MBE/MOCVD/hybrid growth approaches. Preliminary development results for a gap-fill process to reduce coupling loss at pocket end and fabrication with MBE partial selective growth in-pocket will also be presented.

We will also comment on remaining challenges with yield and scaling, some of which were unforeseen at the outset. In the end, in an effort to bridge the gap between academic research and industrial applications, we include a comprehensive review on the development in device screening and measurement technology on 300 mm scale for a shorter development cycle for large-scale integrated photonics.

With this, we hope our experiences can advance the field towards realizing a truly monolithic integration platform with QD heteroepitaxy for Si photonics, aligning with the promised benchmarks of device performance and reliability, production scale and economic value.

6.2 Overview of integration process development and scaling

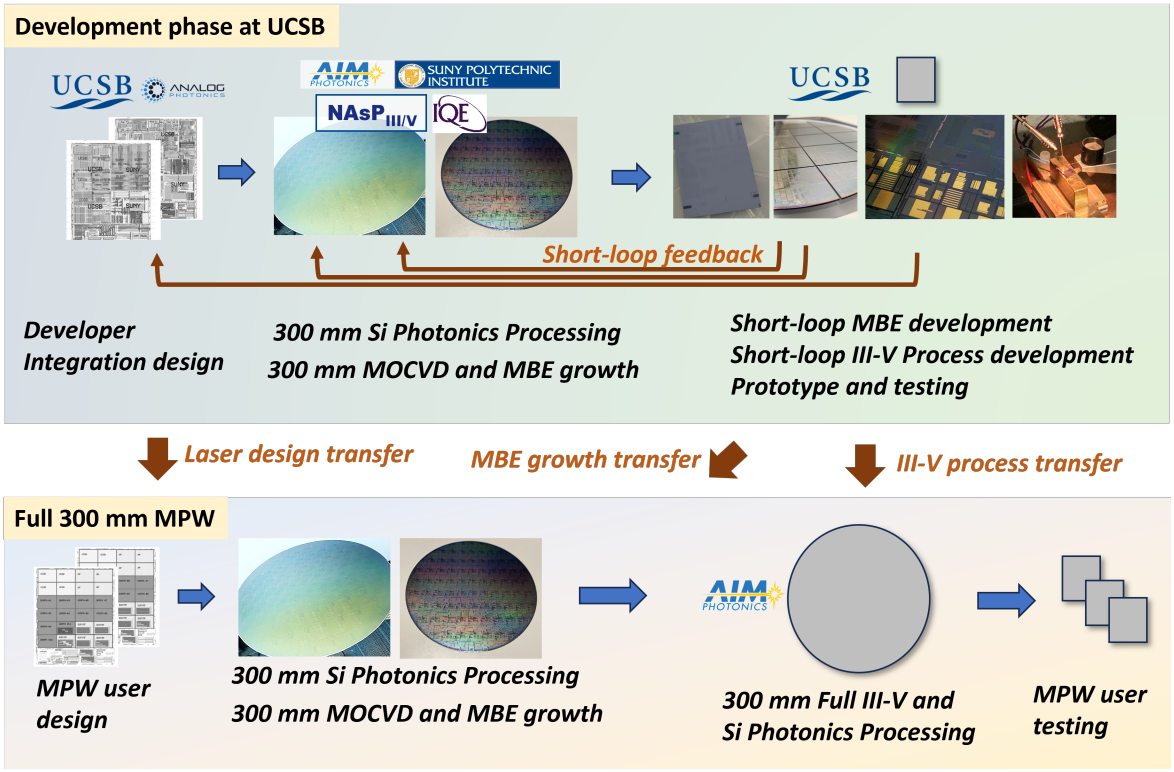

Figure 6.1: Overview of the development flow of QD laser process on a 300 mm scale with Si photonics foundry process.

The studies presented in Chapter 4 and Chapter 5 were carried out with the aim of technology transfer of full-scale monolithic integration of quantum-dot lasers on Silicon photonic wafers through short-loop development at a university facility, collaborated with Provider Development Kit (PDK) providers, 300 mm growth facilities ($NAsP_{III/V}$, IQE) and Si photonic foundry (AIM Photonics and SUNY RF).

Figure 6.1 shows an overview of the development flow. The 300 mm wafer was prepared and patterened in a Silicon photonics foundry, and then brought to a 300 mm

MOCVD facility for the initial template preparation. After that, the wafer is either diced into smaller pieces for in-house MBE epitaxy of the QD laser stack at UCSB, or prepared at a 300 mm MBE facility for full-scale epitaxy of the QD laser stack, and then diced into smaller pieces. In either cases, the small pieces after growth were prepared at UCSB Nanofab for process development and device fabrication to demonstrate in-pocket QD lasers as well as initial on-chip coupling and photonic integration.

The developer integration layout design ("test site" designs), MBE growth development, QD laser process development and device testing conducted at UCSB play an important role in innovative research and validation of development phase technology breakthroughs. These findings are incorporated into the next generation of iterations, which will enable quick learning of critical design, growth and fabrication parameters and enhance overall platform performance and yield.

The knowledge is also currently being transferred to a III-V product line of photonics foundry to enable large-scale manufacture of monolithically integrated photonic circuits. This step is crucial in realizing the objective of achieving low-cost, high-volume integration of III-V components on Si photonics wafers through monolithic growth and fully integrated device processing. The developed platform is envisioned to carry capability of Multi-Wafer Project (MPW) service for individual users to carry out design with PDK support, and receive finished Photonic Integrated Circuit (PIC) chips featuring integrated quantum-dot gain sections with Si photonics for individual testing of functional units.

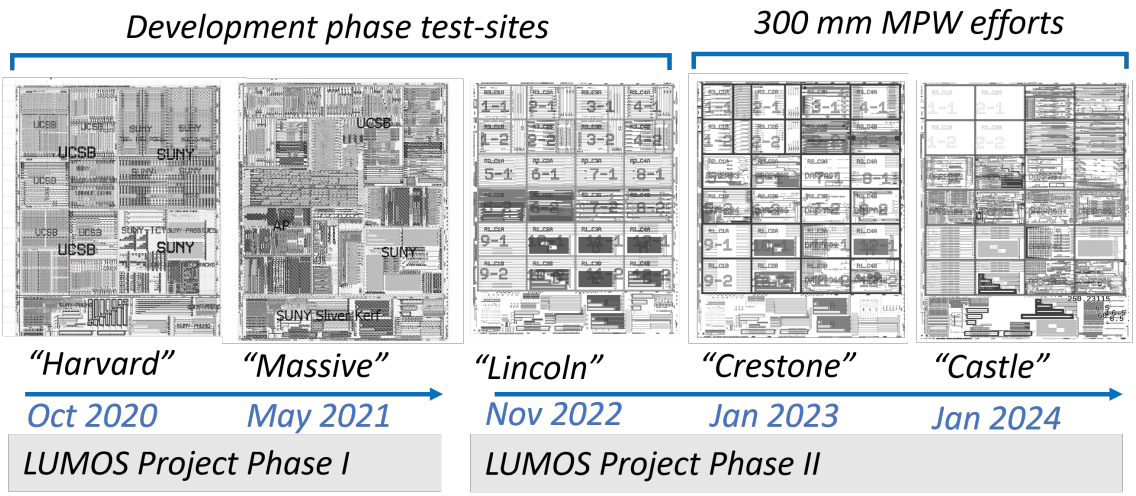

Figure 6.2: Generations of developer integration design layouts.

The generations of developer integration design mask layouts are listed in Figure 6.2. The dimension of each die is 26 mm × 32 mm, where UCSB team is in charge of a portion of the design space for the purpose of exploring laser design and coupling, as well as functional devices and PICs. The learnings from the previous test site results are usually taken into considerations for down-selecting splits and improving parameters for the next generation of the design, though some overlap of the development phases makes it hard to entirely finish one design-process-test cycle before going into the next. Table 6.1 lists out the key roles of each test site, the design submission time and the time of critical demonstration finished from that design. In particular, the first laser demonstration took an entire year and half, which marks the initial efforts for in-pocket growth condition study and in-pocket laser process development detailed in Chapter 4. The last two test sites are currently under development at the foundry.

IQE Inc. is in charge of the 300 mm scale in-pocket MBE growth in this project. Some of the grown wafers from different test sites are shipped to UCSB for both in-pocket PL analysis and device fabrication, both with or without post-MBE growth CMP. Extensive

Test site or MPW Name/Abbr.	Design submission date	Role	Demonstrations	Demo time
"Harvard"/HRVD	2020/10/15	First short-loop laser test site	First in-pocket QD laser on Si at UCSB	2022/4
"Massive"/MSIV	2021/5/18	First full-build SiPh test site	First 300 mm post-MBE growth CMP at AIM/SUNY	2022/12
"Lincoln"/LICN	2022/11/15	Second short-loop laser test site ("Harvard 2.0")	First on-chip QD lasers coupled to foundry-processed SiN waveguide at UCSB	2023/9
"Crestone"/MPW1	2023/1/15	First SiPh full build MPW	300 mm III-V run path under development	-
"Castle"/MPW2	2024/1/15	Second SiPh full build MPW	300 mm III-V run path under development	-

Table 6.1: List of test site objectives and demonstration results.

analysis of the in-pocket PL has provided sufficient feedback for 300 mm MBE growth condition maintenance, and for learnings of the science behind growth quality variations that will be covered in the next section in this Chapter. There are also new findings regarding other aspects affecting wafer-scale material quality that will be covered in the section "Challenges on yield and scaling towrads 300 mm scale". A summary of the total 8 full-scale wafers from IQE is listed in Figure 6.3 and the following Table 6.2.

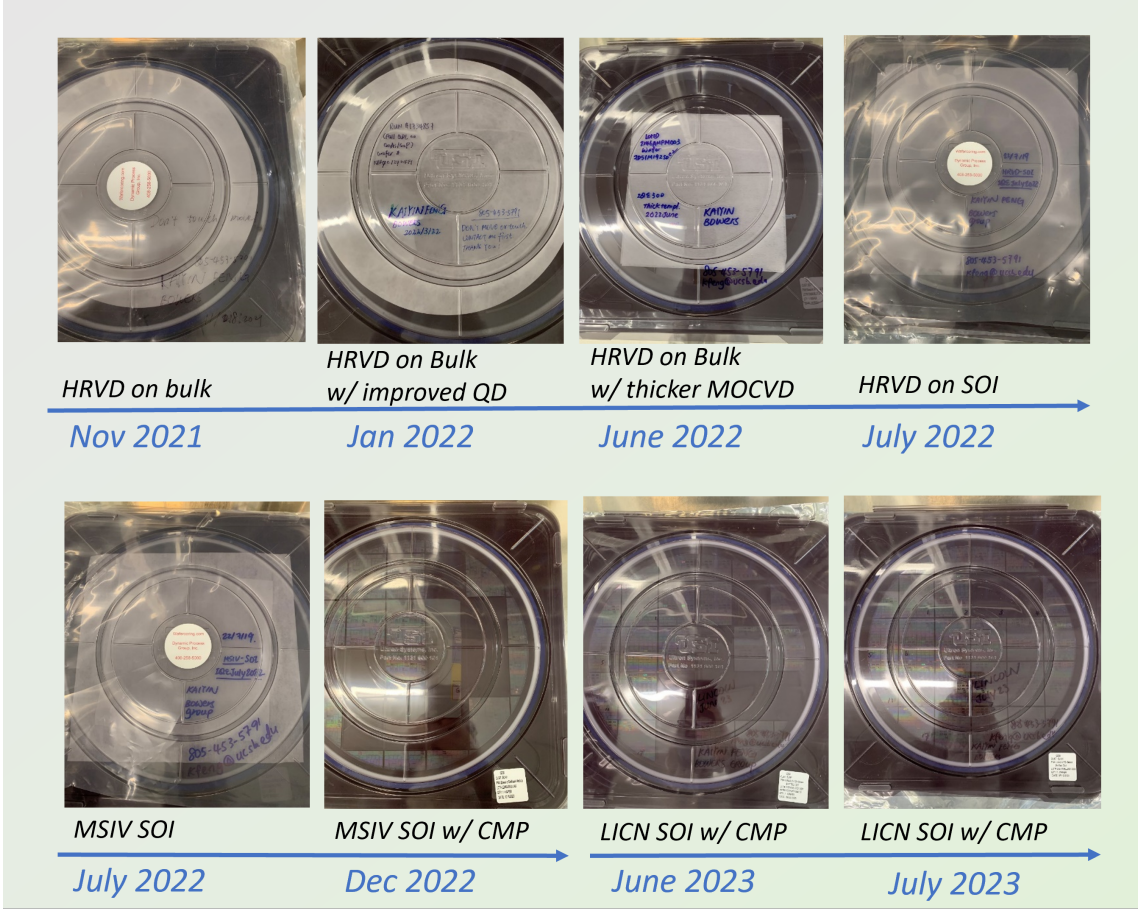

Figure 6.3: Generations of full-scale 300 mm Si photonics wafers with QD laser growth from IQE for wafer characterization, process development, device demonstrations and testing at UCSB.

In terms of device fabrication development, roughly 14 complete samples were fabricated at UCSB Nanofab, from either UCSB in-house MBE growth on diced coupons of size 26 mm x 32 mm, or using diced pieces from the IQE full-scale growth wafer, following the additional process development runs mentioned in the beginning of fabrication section in Chapter 4. Note that for most of the later wafers, the dicing dimensions were expanded to 4 dies per sample (52 mm x 64 mm) for easy handling and efficient processing with multiple dies per fabrication run. Figure 6.4 shows a summary of the finished samples and the corresponding timeline.

Wafer	Receive date	Role	Comments
HRVD on Bulk	Nov 2021	First IQE 300 mm in-pocket growth wafer	Poor QD PL quality
HRVD on Bulk	Jan 2022	Second IQE 300 mm in-pocket growth wafer with optimized growth conditions	Improved QD PL quality
HRVD on Bulk w/ thicker MOCVD	June 2022	Grow GaAs buffer with MOCVD for shorter MBE growth time	Stack height variation duo to MOCVD growth rate sensitivity
HRVD on SOI	July 2022	First IQE 300 mm in-pocket growth on SOI wafer	-
MSIV on SOI	July 2022	MSIV test site, IQE 300 mm in-pocket growth on SOI wafer	Severe in-pocket defect, pocket widths too narrow
MSIV on SOI w/ CMP	Dec 2022	First IQE 300 mm in-pocket growth with AIM/SUNY CMP for post-MBE planarization	CMP non-uniformity and in-pocket defects
LICN on SOI w/ CMP	June 2023	IQE 300 mm in-pocket growth with AIM/SUNY CMP with optimized template	CMP non-uniformity and in-pocket defects
LICN on SOI w/ CMP	July 2023	IQE 300 mm in-pocket growth with AIM/SUNY CMP with optimized template	CMP non-uniformity and in-pocket defects

Table 6.2: List of 300 mm development wafer ID, dates, objectives and comments.

The first in-pocket lasers were demonstrated in April 2022, with one sample from UCSB growth (#220330) and one from IQE (HRVD Jan22 P11C). Immediately after, a few more device fabrication runs were done to check repeatability of experimental results with newly available SOI templates (#220702 and #220628), explore possibilities for improved stack design (#220915 with 7 QD layers), produce more devices for testing (IQE

HRVDJan22 P3CD, IQE HRVDJan22 P14CD), and further improve the fabrication process with a new generation of laser mask design (IQE HRVDJan22P12CD). The next few runs are focused efforts to produce etched facet lasers (#230213, #230719[1]) for the first demonstration of in-pocket lasers coupled to SiN waveguides (IQE LICNJuly23 P7). Additional two samples MBE partial selective growth were fabricated (#231012, #231102) for the demonstration of improved coupling efficiency with in-pocket etched facet lasers with shorter gap distance at pocket ends, and the research is still ongoing awaiting the development of deep Si etch for vertical edge coupling with duo-facet polished fibers, a topic that will also be covered in later sections.

[1]This one sample with partial selective growth on Lincoln Bulk template, turned out to be LEDs with suspected chamber condition drifting affecting QD growth quality. #230719 is co-fabricated with IQE LICNJuly23P7.

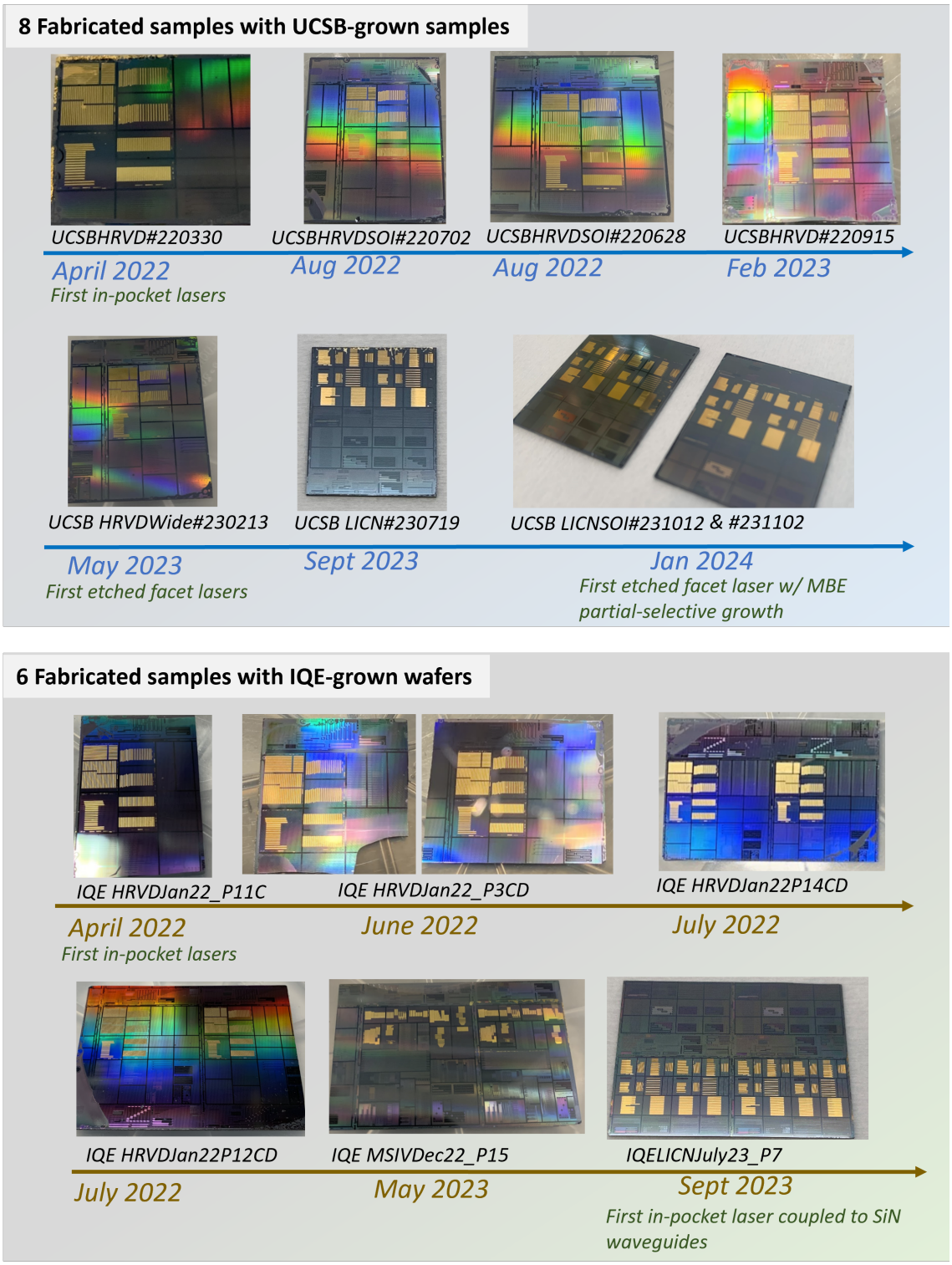

Figure 6.4: Generations of fabricated samples at UCSB, from both UCSB MBE growth and IQE 300mm growth.

This chapter will cover the research efforts for improving overall performance and yield of the monolithic integration platform from iterations of the short-loop development cycles of this project, and comment on major challenges of technology transfer towards 300 mm scale, remaining problems and future directions.

6.3 Improvement of in-pocket QD quality

Photoluminescence (PL) characteristics of the in-pocket QDs with a pump laser wavelength of 785 nm were performed to compare the dot quality variation across different wafers, as well as across different dies on the same wafer, and different pocket design (size and orientation) on the same die. Throughout the project, we collected PL data from different growth campaigns, and from both UCSB MBE chambers and IQE 300 mm growth chambers, and with different test site pocket layouts.

In this section, we will discuss the PL variations which indicates the variations of in-pocket QD growth conditions, and the efforts to improve the overall in-pocket QD growth quality for the highest yield and repeatability.

6.3.1 QD growth dependency on pocket orientation

Variation in PL characteristics for pockets with different orientations

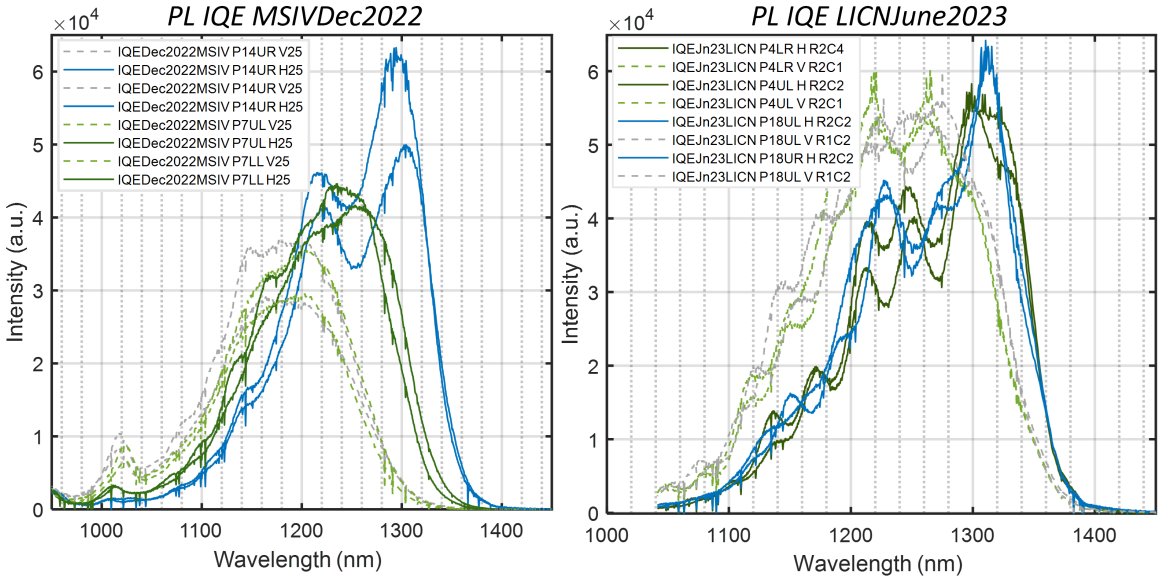

Figure 6.5: Variations in PL for pockets with different orientations from IQE 300 mm growth. The left plot is from wafer "IQE MSIV Dec2022" with all data taken in pocket width of 25 µm, and the right plot is from "IQE LICN June202" with all data taken in pocket width of 35 µm. In the label, the "P" number indicates the location of the diced piece (each piece is 52 mm x 64 mm and contains four dies of 26 mm x 32 mm), "UL", "LR" ("Upper Left", "Lower Right") etc. indicate the location of the die within the piece, and for "IQE LICN June2023", "R2C1" ("Row 2 Column 1") etc. indicates the location of the pocket within each die. "V" means the direction of the pocket is vertical on mask (dashed lines) and "H" means the direction of the pocket is horizontal on mask (solid lines).

Figure 6.5 shows the in-pocket PL taken from the diced 300 mm wafer "IQE MSIV Dec2022" and "IQE LICN June2023". Within each plot, the pockets have the same width, 25 µm width for"IQE MSIV Dec2022" and 35 µm width for "IQE LICN June2023". In the label, the "P" number indicates the location of the diced piece (each piece is 52 mm x 64 mm and contains four dies of 26 mm x 32 mm), "UL", "LR" ("Upper Left", "Lower Right") etc. indicate the location of the die within the piece, and for "IQE LICN

June2023", "R2C1" ("Row 2 Column 1") etc. indicates the location of the pocket within each die."V" means the direction of the pocket is vertical on mask and"H" means the direction of the pocket is horizontal on mask.

The first obvious trend observed was the difference for in-pocket PL of QDs in different pocket orientations. The solid lines from the "horizontal" pockets have PL with higher ground state peak intensity under the same pump level suggesting potentially higher QD density [2], and a more clear separation of ground state and excited states indicating better carrier confinement, as well as a lower full width at half maximum (FWHM) indicating higher uniformity of QD size distribution.

For some of the PL from the"vertical" pockets, there is wide emission around shorter wavelength around 1150 nm to 1250 nm, and some of the measurement does not show any clear separation of states, which indicates a fluctuation of QD size distribution within the pocket. This trend is apparent across different locations on the same die, among different dies and among different wafers receivd from IQE grown at different time and with different integration designs (i.e. different local and global pocket density and lengths).

[2]PL intensity can also be impacted by many other factors, such as modulation doping efficiency, dopants-per-QD, etc., and the suggestions from the observation here should be only seen as a "first guess" and not a correlation. Other techniques such as surface QD AFM scans should be employed to further study the QD densities.

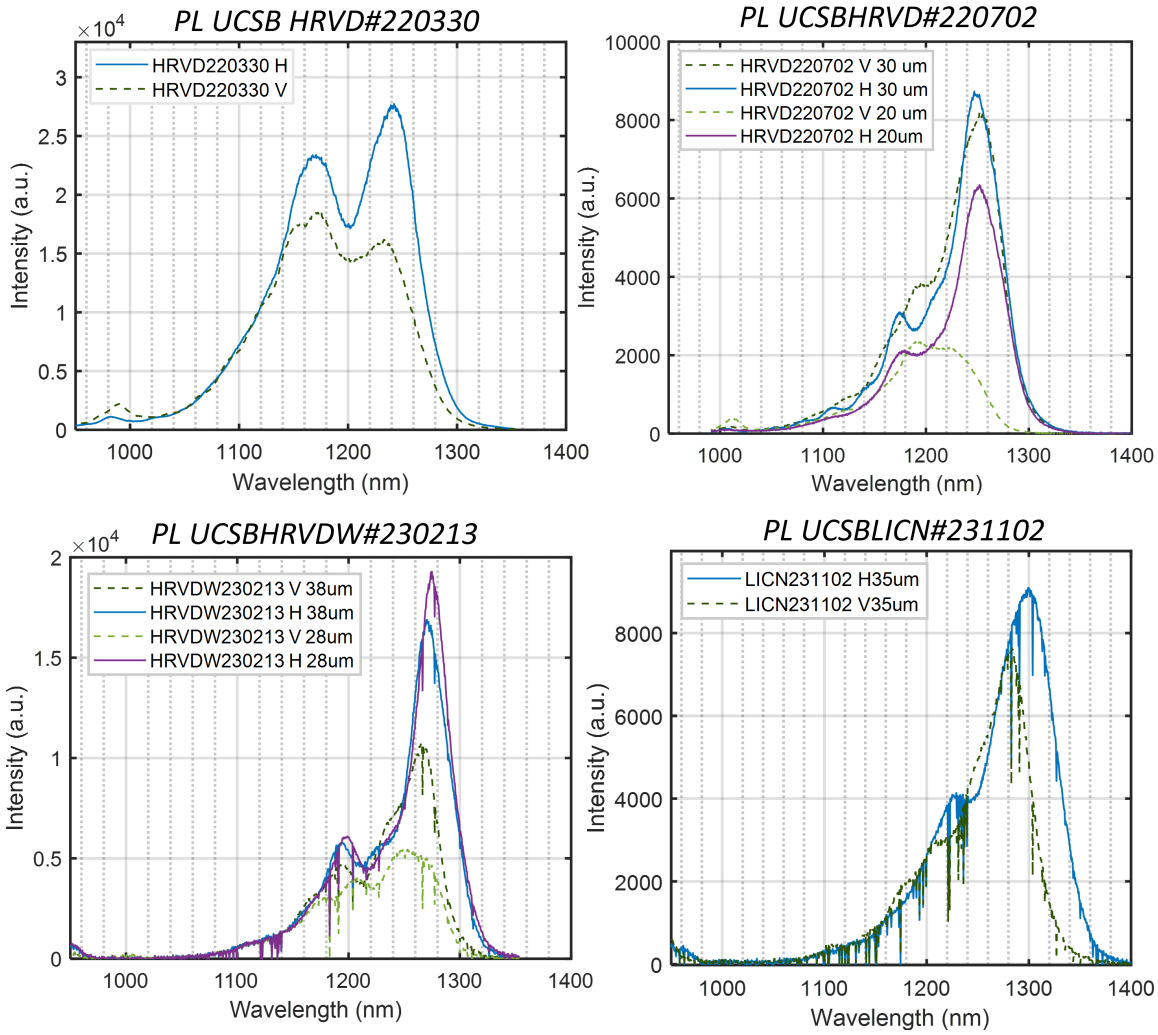

Figure 6.6: Variation in PL characteristics for pockets with different orientations from UCSB MBE growth. Each plot is from one sample, and the label "V" means the direction of the pocket is vertical on mask (dashed lines) and "H" means the direction of the pocket is horizontal on mask (solid lines). The growth results in "vertical" pockets shown in dashed lines are generally dimmer and in shorter wavelengths compared to those in "horizontal" pocket shown in solid lines.

It is also observed from the PL measurement results obtained from the in-pocket MBE growth performed at UCSB MBE lab on diced out small coupons (26 mm × 32 mm each). Figure 6.6 shows the PL data across four different growths. The growth results in "vertical" pockets shown in dashed lines are generally dimmer and in shorter

wavelengths compared to those in "horizontal" pocket shown in solid lines.

Research of QD growth dependency on pocket orientation

"Vertical" in the above analysis straightforwardly means the pocket design is vertical on the integration mask layout, and "horizontal" means it is horizontal on the integration mask layout. Further research into the above findings needs to connect these orientations to the crystal formations on the wafer. In production, there is a "notch" direction on the patterned Silicon wafer that is parallel to the Si surface step edges. Since the mask layout is always initially aligned the same way on the 300 mm Si wafer, the "vertical" pockets are always parallel to the "notch" direction and "horizontal" pocket orthogonal to the "notch" direction.

The in-pocket III-V crystal orientation, so far as we observed, has been examined to hold the same relationship to the wafer orientation of the 300 mm Si wafer, either from a patterned bulk Si template or patterned SOI template. As a result, the [1 1 0] crystal orientation always shows in "vertical" pockets that are parallel to the "notch" direction and the [1 $\overline{1}$ 0] crystal orientation always appears in the "horizontal" pockets that are orthogonal to the "notch" direction. Note that this relationship could be different regarding growth conditions [1].

Detailed analysis of the pocket orientation influence on QD morphology and in-pocket stress profile was carried out by our colleague and the results are published in *Advanced Functional Materials* in 2023, see [2].

Design guidelines and application remarks

Through these findings, we have updated the design guidelines to set "horizontal" orientation as the centered design for these pockets. The pocket width on "Harvard" holds splits of about the equal number of horizontal and vertical pockets, with uneven

distribution of pocket lengths and integrated devices due to the limit in design space. "Massive" unfortunately was designed before any production from "Harvard" and was set with similar splits. In the later test sites "Lincoln" and the first MPW "Crestone", three fourths of the pockets at our internal UCSB team design space were set as "horizontal", with the other quarter being "vertical" for a consistency check and comparison, as we did not have enough understanding to guarantee the initial III-V crystal orientation will always hold the same relationship with the Si surface step edges, hence the "notch" orientation of the 300 mm Si wafer which directly links to the mask layout patterning orientations. This knowledge was also transferred to the PDK provider (Analog Photonics) for the writers on the first and second MPWs to hold "horizontal" orientation for their designed gain sections for the best expected yield.

However, with close inspection of more PL data, we can see that this is a general trend, but does not necessarily hold true for every single pocket. In Figure 6.6, the PL for "UCSBHRVD#220702", the "vertical" for a pocket width of 30 µm has similar performance compared to "horizontal" 30 µm pockets. We notice that it seems the wider the pockets are, the less difference there is for the horizontal and vertical pockets. The details of the dependency on pocket size will soon be discussed in the next subsection.

These orientation dependency results should not be interpreted as a blunt guiding conclusion of "horizontal" is always "better" than "vertical". Like mentioned above, as the pocket width gets wider, the effect is less apparent. We also noticed that the variation of PL within the same pocket orientation within one wafer or across different wafers can sometimes be as large as the variations based on orientation dependency, which will be shown in the later subsections.

Furthermore, even with a "better" PL performance, it does not always link to better laser performance made with the material, as several other factors will play a role, such as defect density, thermal dynamics. For example, the "hero" device presented in Chapter 4

with the record high double-side maximum output power of approximately 125 mW with a footprint about 5 µm × 2000 µm was from a vertical 30 µm pocket from "IQE HRVD-Jan2022". No horizontal or vertical device in the future runs has shown a higher total output power so far. We have also observed samples with better PL and/or with horizontal pocket at 35 µm width that "should" be better, but have worse device performance in terms of wavelength centering, output power, threshold current, etc. compared to a vertical pocket at narrower width at a different growth, or compared to a vertical pocket at the same width on the same sample (through results from "IQE LICNJuly23P7").

As an innovative integration platform developing fast with changing factors and generations of improvements towards both heteroepitaxy growth and device fabrications, these early findings are critical for making prompt adjustments to shrink the split space and enhance the overall device performance and yield. It is also important to keep in mind to reevaluate initial findings with the changing factors and update the "guideline" based on practicality and target applications.

6.3.2 QD growth dependency on pocket size

Variation in PL characteristics for pocket with different widths

With a closer look at the PL plots in Figure 6.6, it can be seen that for "UCSBHRVD#220702" and "UCSBHRVD#230213", where there are also variations of PL for the same pocket orientation on the same sample. Figure 6.7 includes two more PL results from UCSB small-sample MBE growth in addition to those taken from the last subsection. In general, the PL taken from a wider pocket (e.g. 30 µm) shows a higher intensity than that from a narrower pocket (e.g. 20 µm), and this stays true for both horizontal and vertical pockets.

However, in "UCSBHRVDW#230213", the relatively narrower pocket with width of

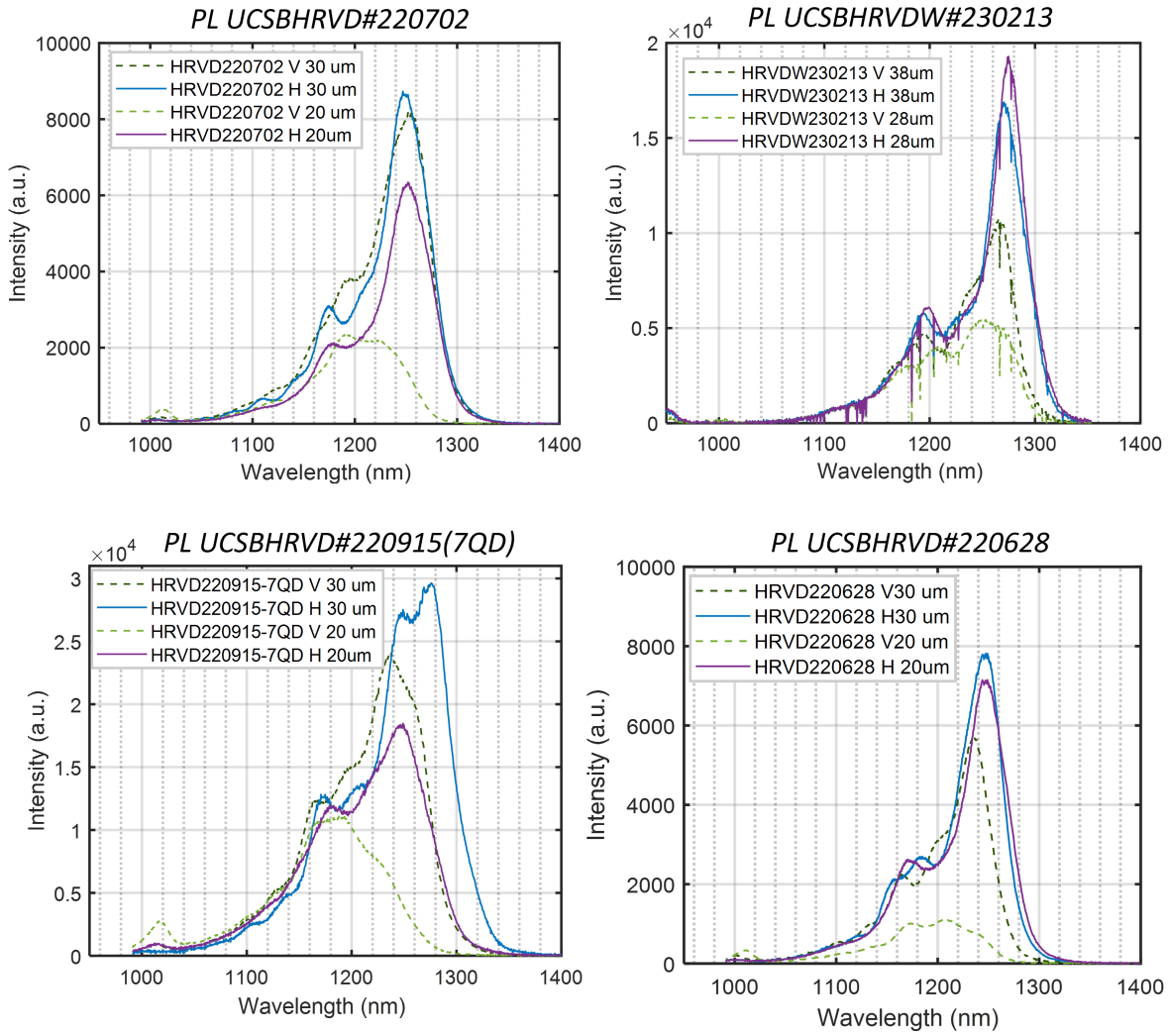

Figure 6.7: Variations in PL for pocket with different widths. Each plot contains PL data taken from the same one sample grown with UCSB MBE. "V" means the direction of the pocket is vertical on mask (dashed lines) and "H" means the direction of the pocket is horizontal on mask (solid lines). Here, PL difference between different pocket widths is compared across the same orientations for both vertical and horizontal cases in search for a valid conclusion. In each sample, the number of µm in the label represents width of the pocket where the PL is taken from, and the blue line is from a wider pocket width and purple line is from a narrower pocket width in the horizontal direction, while the dark green line is from a wider pocket width and light green line is from a narrower pocket width in the vertical direction.

28 µm has a higher PL intensity compared to the relatively wider pocket with the width of 38 µm. Again, I suspect this is due to the weakening of the effect from geometry

constraints as the pocket dimension gets wider.

The PL intensity study alone was not enough to conclude the direct relationship to what extent the QD growth quality degrades with narrower pocket. From a device result point of view, it is also hard to draw a conclusion that narrower pocket has worse PL thus produce lasers with worse performance. First, there has been device with better performance in certain aspects (e.g. higher maximum output power) from narrower pocket compared to that from wider pocket on the same sample (as seen from the result of HRVD#220702 in Chapter 4). Secondly, complications of fabrication when the pocket gets narrower also add factors when linking device performance results to QD growth quality only, even if the device result comparison is suggesting worse device performance from narrower pocket.

Research of QD growth dependency on pocket width

In order to separate the factors of fabrication quality from material quality when comparing different pocket sizes, the research was carried out by our colleagues using house-made "semi-pocket" structure at UCSB, where oxide deposition and pocket etch were done at UCSB Nanofab, and QD stack was grown inside pockets of the same length 3900 µm and various width from 10 µm to 50 µ. The results were published in [3].

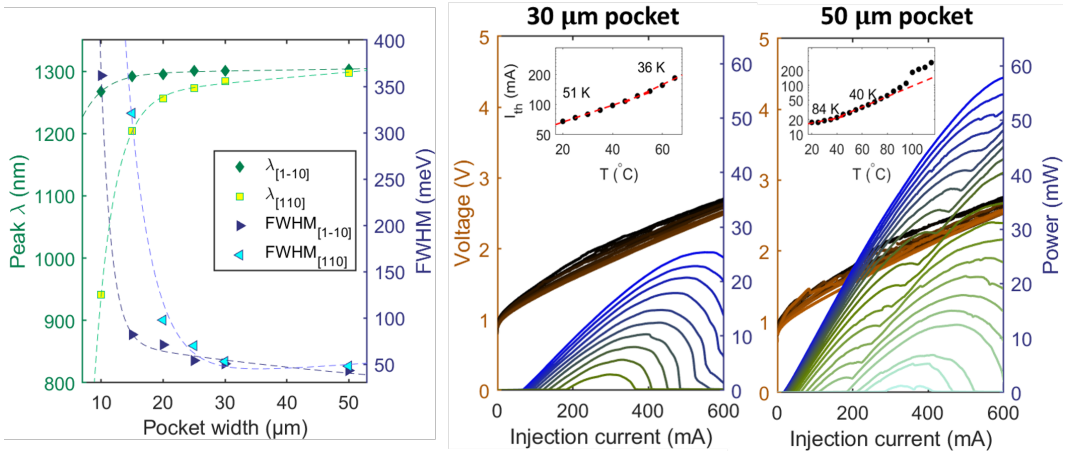

Figure 6.8: (a) PL peak wavelength and full width at half maximum (FWHM) as a function of pocket width. (b) Left: T-dependent LIV measurements, with inset threshold current I_{th} and thermal tolerance parameter T_0 fits for device of 2300 µm by 4 µm mesa grown inside a 30 µm pocket; right: T-dependent LIV with inset T_0 fits for an adjacent 50 µm device of the same dimensions and laser bar on the left. Reproduced from [3], ©Advanced Photonics Research published by Wiley-VCH GmbH. https://doi.org/10.1002/adpr.202300317

As shown in Figure 6.8 (a), the center wavelength of ground state emission redshifts as the pocket widens, and the full width at half maximum (FWHM) gets narrower with wider pocket, showing more desirable QD emission wavelength for O-band applications and better uniformity. Edge emitting ridge waveguide lasers of the exact same geometry (4 µm × 2300 µm) were fabricated from these pockets and the performance from a 50 µm pocket is distinctively better than that of the 30 µm pocket, as shown in Figure 6.8 (b). The laser in 50 µm pocket demonstrated ground state lasing up to 95 °C and excited state lasing up to 115 °C, which is far better than the one in 30 µm pocket [3].

Detailed study with systematic comparison of different pocket geometry shows that the MBE growth of QD growth quality itself is dependent on pocket width and a wider pocket yielded laser with lower threshold and better thermal performance even with the same design of laser mesa width and length. It demonstrated the variations of in-pocket QD PL intensity, peak wavelength and FWHM with pocket width, and shows the

correlation with QD device performance and reliability.

Design guidelines and application remarks

From the conclusions above, it is apparent that a wide pocket (e.g. 50 µm or wider) should be preferred to provide the best performance and yield for the monolithic integration platform. These results were communicated clearly with the developer team and in the most recent layout "Castle(MPW2)", it is finally adopted as a global rule that all the pockets across the MPW die are set with a width of 50 µm.

From a device fabrication point of view, it is also obvious that the wider pocket will provide easier handling in fabrication as the effect from the high aspect-ratio pocket geometry gets less dramatic. Figure 6.9 shows the cross-section SEMs of pockets with different widths as a visualization. The discussion of fabrication development was covered in Chapter 4. This reinforces the preference for a wider pocket, aligning with its positive effects on QD growth quality, thus presenting a beneficial choice that should be unequivocally adopted.

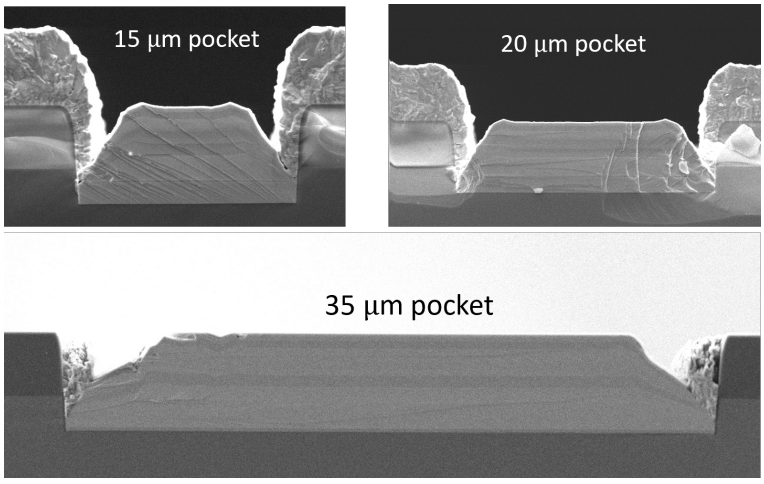

Figure 6.9: Cross-section SEMs of pockets with different widths. Larger pocket width provides wider flat-area in the center of the pocket cross-section, posing less constrain on the fabrication of mesa and electrical contacts, in addition to the benefits in better QD growths.

As a review of this project, the initial "Harvard" was designed with pocket width splits of 15 µm, 20 µm, and a few 30 µm. The second "Massive" was designed centered with 15 µm. This was based on a premature assumption that it may favor the material quality of selective MOCVD growth in pocket and also a false argument of pocket with more narrow width would give a higher overall integration density for the monolithic integration platform. In reality, the actual integration density is limited by many other factors, such as the maximum III-V fill factor that can be approved in a Si photonics foundry for processing, as well as the minimum pocket spacing ("pitch") that can be allowed for material quality, especially for MOCVD uniformity. The smallest pitch allowed in this platform due to limitation of III-V fill factor was decided to be around 125 - 150 µm, which is much wider than the pocket width. Later in the project, the pitch width was pushed to a minimum of 700 µm for MOCVD template uniformity, which would be the biggest limiting factor for active gain density. Details of the relationship of the gain spacing and MOCVD growth uniformity will be discussed later in the following sections.

Later production of "Massive" was expanded to 23 µm from the foundry side with feedback from the initial "Harvard" laser testing results. Then "Lincoln" and "Crestone" were expanded to 35 µm [3]. In the end, "Castle" was finally pushed to 50 µm width with the published results indicating clear evidence of the correlation [4].

Viewed as an achievement from the fabrication point of view, the process development

[3]This was a compromise between the existing results asking for wider pocket design (50 µm or wider) and the conservative concerns about "too many changes too soon". The writer believes that any wider pocket will only make the fabrication better, yet there has been much difficulty in decision making and much of lagging in the time of different phases of development cycles of each generation of designs, which is a pitiful sacrifice of device performance improvement in exchange for the repeatability and overestimation of the risk of making a rational change for better even in the bold development phase of this project. (Almost felt bad about working too hard to make it possible to make lasers in narrower pockets from a fabrication point of view, as otherwise it may be easier to advocate for a wider pocket width.)

[4]This decision was finalized with the developer team at the very final stage of the layout campaign, only a few days ahead of submission deadline, which left me dumbfounding as the bitterness of how long a time it has taken almost took away the joy of seeing this change finally happen and it only seems unreal at the moment. Well, things do get better.

detailed in Chapter 4 has led to successfully demonstrate in-pocket lasers with a range of pocket widths of 15 µm, 20 µm, 30 µm and 35 µm despite the difficulties from lower gain and tighter device fabrication constrains with the smaller width. However, this is one challenge in the monolithic platform that could be dodged, but was not able to be due to the constraints in decision-making. For the research of on-chip integrated QD lasers itself, one could imagine when the pocket width is as wide as the orders of 100 µm, or expanding the pocket into a big box of e.g. 16 mm × 16 mm like demonstrated by Wei *et al.* also in 2022 - 2023 [4], it would be about the same growth quality and process in terms of making ridge waveguides compared to fabricating lasers on blanket wafer, and we could have saved many rounds of frustrations towards demonstrating the first working lasers. On a positive note, the learning through desperately pushing the fabrication limits in high aspect-ratio geometries has been beneficial for cultivating the know-hows towards coping with the complications of the polycrystal and faceting material at pocket ends and would be necessary anyways even if the pocket width was not a constratint, and will remain useful in a general sense for dealing with challenges in semiconductor processing, especially for innovative solutions of on-chip integrations.

6.3.3 Other factors affecting in-pocket PL

Variation in PL characteristics regardless of orientation and size

The conclusion regarding PL dependency on pocket orientation and size is not deterministic, as there are also other factors affecting in-pocket QD growth results, and this point is proved true by the outlier data shown above.

Analysis on PL fluctuations with the factors of changing pocket geometry completely ruled out, on the other hand, would be able to provide a general range of the variations. How much of PL variation is presence with the same pocket orientation and size across

a 300 mm wafer? And how much of that can be observed locally for the same pocket orientation and size from the same die or on the same small-sample MBE growth?

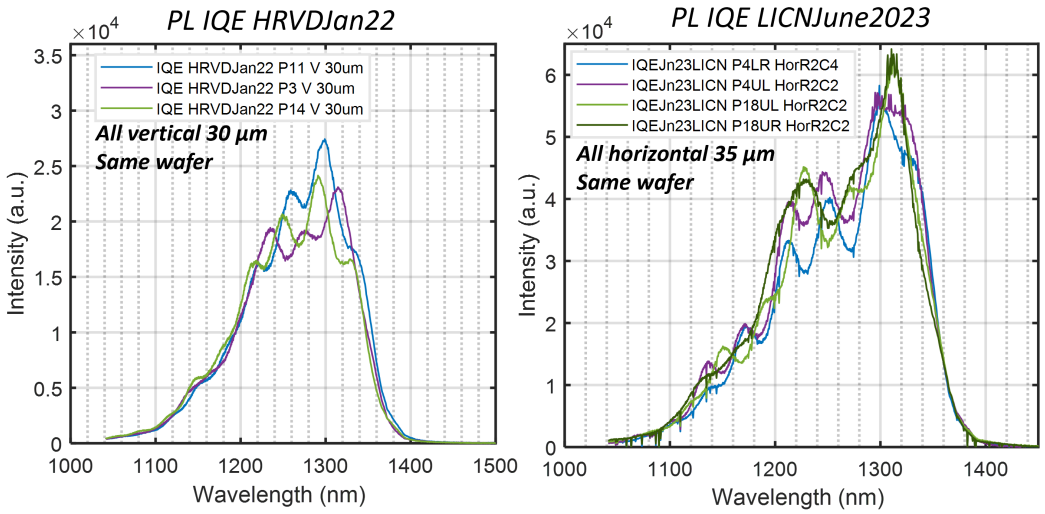

Figure 6.10: Variations in PL of pockets with same orientation and same width, but across different dies, on the same 300 mm wafer grown by IQE. Left: IQEHRVDJan22, right: IQELICNJune2023. In the label, the "P" number indicates the location of the diced piece (each piece is 52 mm x 64 mm and contains four dies of 26 mm x 32 mm), "UL", "LR" ("Upper Left", "Lower Right") etc. indicate the location of the die within the piece, and for "IQE LICN June2023", "R2C4" ("Row 2 Column 4") etc. indicates the location of the pocket within each die. "V" means the direction of the pocket is vertical on mask and "Hor" means the direction of the pocket is horizontal on mask.

Figure 6.10 shows the PL variations through different dies on the same 300 mm wafer grown by IQE, on either the "Harvard" template with all data taken in the vertical 30 µm pockets, or on "Lincoln" template with all data taken in the horizontal 30 µm pockets. Both plots exhibit fluctuations of peak ground state intensity of at least 10 nm, with more variations of span and intensity in the multiple excited states, especially for the data taken in the vertical pockets.

Comparing these findings to the PL variation on 300 mm blanket wafer shown in Chapter 3, this range of fluctuation is understandable given the wafer size. The variations overall QD dot density, size and uniformity (indicated by PL intensity, peak wavelength

and FWHM) are likely attributed to temperature variations across wafer during growth, as there is not a significant correlation observed between the trend of changes and the radial or linear location where the data was collected on the wafer.

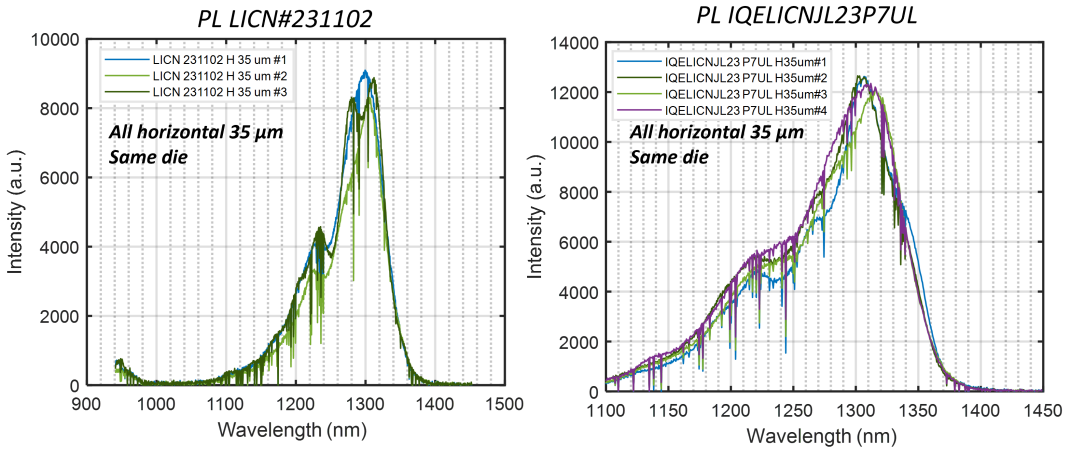

Figure 6.11: In-pocket PL characteristics of the same orientation, same pocket width on the same die, from UCSB growth (left) and IQE 300 mm growth (right). For the IQE 300 mm growth, the PL is taken from the same die in the same diced piece, "P7UL". All data here is collected from horizontal pockets with a width of 35 µm.

As shown in Figure 6.11, if looking at PL of the same orientation, same pocket width on the same die, either on small-sample growth at UCSB or on one same die from a 300 mm in-pocket growth, there is greater consistency in the PL results. The ground state peak wavelength still varies up to 20 nm, excited states as well. In some instances, there is a "duo peak" around the ground state wavelength even for the horizontal pocket, as shown in "LICN 231102 H 35 µm #3", the two peaks are separated by 20 nm with comparable intensity. We suspect this could be related to localized in-pocket temperature fluctuation as a sensitive response to the accumulating polycrystal thickness on sidewall and oxide surface, and it is possible that the multiple QD layers within the epitaxial stack were grown at different temperatures, leading to a discrepancy in their peak wavelengths.

Concluding remarks

Further MBE studies aimed at comprehending the underlying the physics of in-pocket QD growth conditions and enhancing the overall repeatability of high-quality in-pocket QD growth will be beneficial to augment the overall device yield on this monolithic integration platform. Concurrently, it is important to set up global ground rules that favors greater consistency across samples, such as uniform pocket pitch and length (which affects local polycrystal density, and consequently likely also in-pocket growth temperature), in addition to the uniform pocket orientation and size with the preferred parameters. It becomes also critical to be aware of this variation during integration layout design phase when establishing the target range for wavelength-sensitive applications, such as single-mode lasers with DFB or DBR gratings.

6.4 Challenges with coupling efficiency

6.4.1 Coupling region overview

Coupling efficiency is another major concern for the monolithic integration platform with heteroepitaxy. As a comparison, in heterogeneous integration through bonding and substrate removal, the core of III-V waveguide and Si/SiN waveguides can be designed very close and optical coupling with extremely low loss can be realized with careful taper design. In the heteroepitaxial integration platform with MBE in-pocket growth, the III-V and Si waveguide cores are in the same plane, yet the interface of the two inevitably is covered with polycrystal and faceting material that will create excess scattering loss unless specifically engineered.

The QD laser to SiN coupling efficiency in the first-demonstration in Chapter 5 is predominantly limited by the distance from the etched-facet on III-V and SiN waveguide

edges. The air-gap (created by the developed wet-and-dry combined hardmask etch) at pocket-end has cleared up the polycrystal and faceting area, but also introduces mode expansion of the traveling wave from the laser facet and reduces the modal overlap from the designed laser facet mode and the SiN coupler mode, as well as creating reflection if no tilting between the interfaces is introduced. Theoretically, an inverse-taper design from the SiN coupler side may assist the coupling, yet the current air-gap of 6 - 8 µm is still large to cope for, and the nature of the project (where integration mask is laid out first and the passive structures are manufactured in foundry and fixed in each generation of integration design, and only the III-V cavity can be re-engineered with quick turn-around) also pose challenges to have sufficient splits and iterations for developing the inverse-tapers.

Assuming in-pocket MBE growth of QD stack, vertical etched facet laser cavities and a complete etching of the polycrystal and faceting area at pocket-end, we can simulate the coupling efficiency with relation to the gap distance from laser facet to SiN waveguide for a given SiN coupler in the integration layout. Naturally, the use of a higher-index material to fill in the air-gap will provide modal guiding and improve the optical field overlap from the laser emission to the SiN coupler ends, and its effect on the coupling efficiency is also numerically investigated.

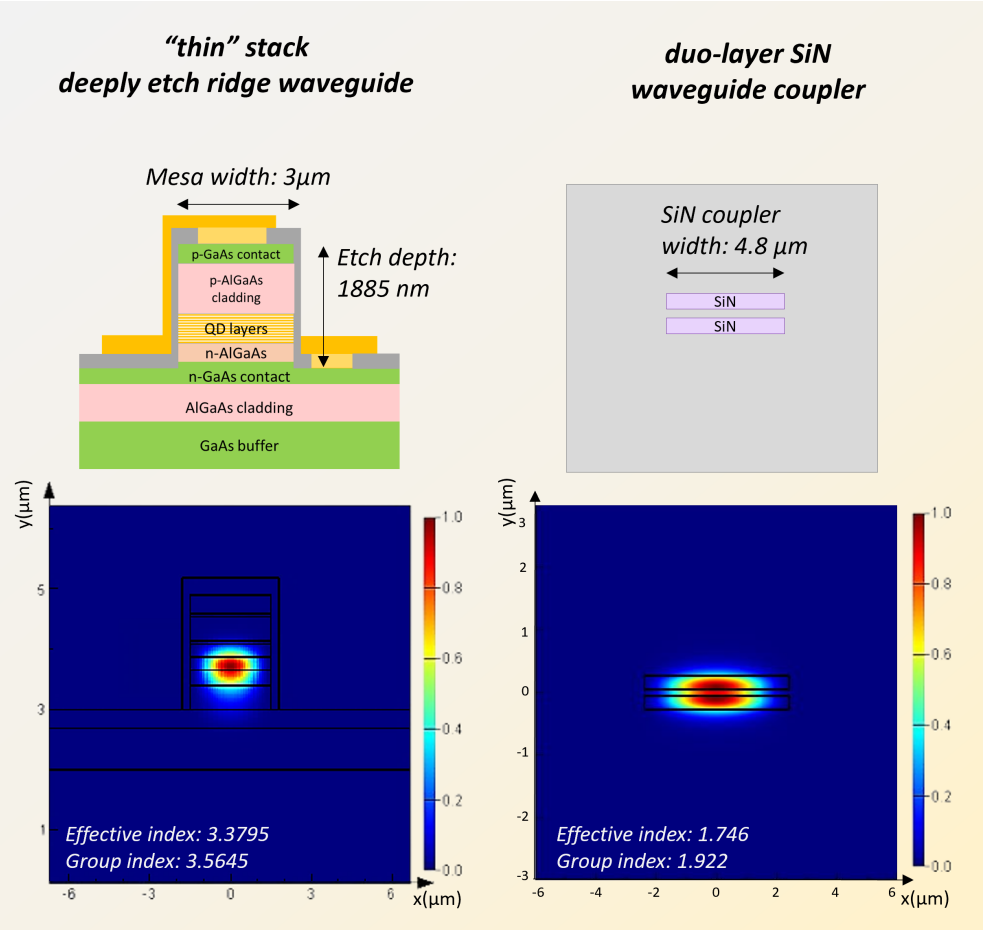

Figure 6.12: Cross-section schematics and optical mode simulation results of the QD ridge waveguide laser and SiN waveguide coupler.

Optical mode analysis of the QD ridge waveguide laser and SiN waveguide coupler cross-sections were conducted with Lumerical MODE, as shown above in Figure 6.12. The initial concept behind the coupler design is to match with the QD ridge waveguide FP laser transverse mode profile, assuming very small gap around 1 μm (which turned out to be a drastic underestimate of the real case).

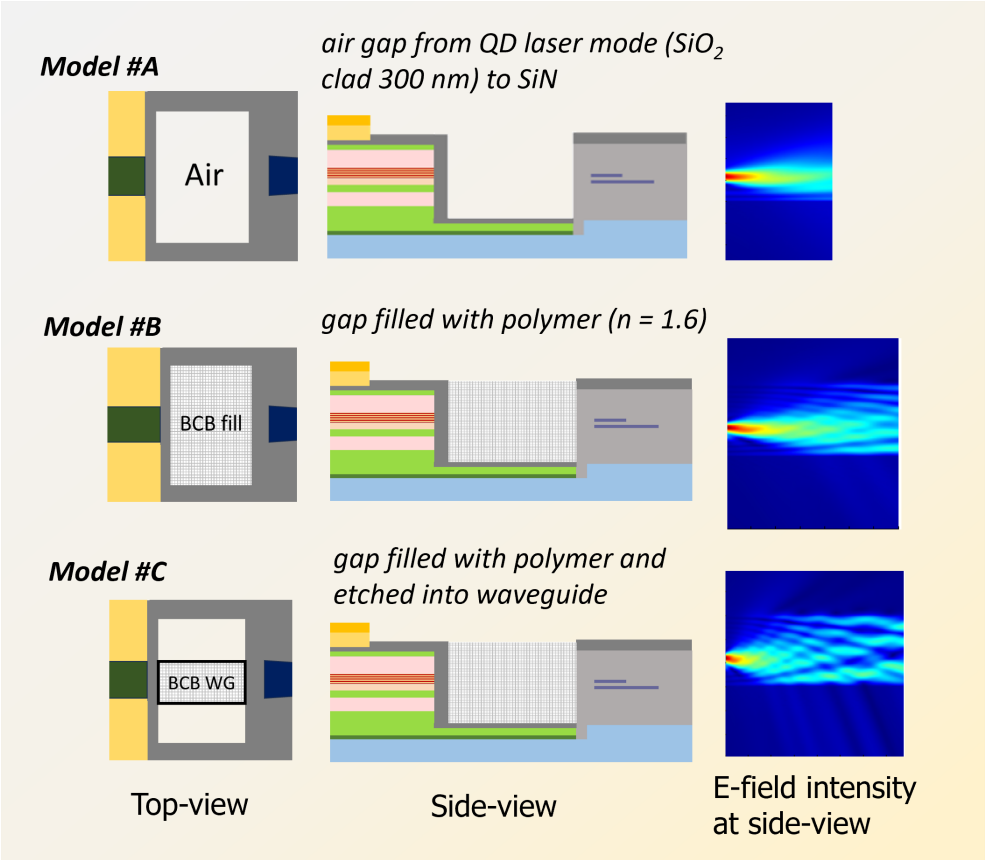

Figure 6.13: Top-view and side-view schematics of the three models of coupling region and the simulated E-field intensity at side-view through Lumerical FDTD. Model (A): air-gap with 300 nm of sidewall SiO_2 passivation only; Model (B): gap filled with polymer with refractive index of 1.6, Model (C): gap filled with polymer etched into waveguide with a width of 4 µm.

Finite-Difference Time-Domain (FDTD) simulation was conducted to estimate mode expansion in the "gap" region between the laser and waveguide. The following three models were considered: (A) air-gap with 300 nm of sidewall SiO_2 passivation only, (B) gap filled with polymer with refractive index of 1.6, and (C) gap filled with polymer etched into waveguide with a width of 4 µm. The top-view and side-view illustration of the models are shown in Figure 6.13, with the simulated E-field intensity at the side-view included on the right. This simulation does not take into consideration and reflection or interaction with the SiN waveguide end. Model (B) shows better vertical

confinement from the interface between the BCB fill top-surface and air, and Model (C) has an additional effect from the confinement in the transverse plane.

With the optical profile from the in-gap expansion, coupling efficiency with the SiN coupler end is estimated using the "power coupling" function in Lumerical, which takes into account both the mode overlap and the mismatch in effective indices between modes (Fresnel transmission) [5]. For the SiN coupler design, we included two initial splits of the end dual-layer waveguide width, 4.8 µm ("SiN Taper Design 1"), and 5.8 µm ("SiN Taper Design 2"). The integration mask layout and some of the demonstrated coupled laser results in Chapter 5 also adopt alternative designs such as inverse tapers (designed by our collaborator), and/or tapers with tilted angle, which is not included in the numerical studies here. The resulting coupling efficiencies are plotted in Figure 6.14.

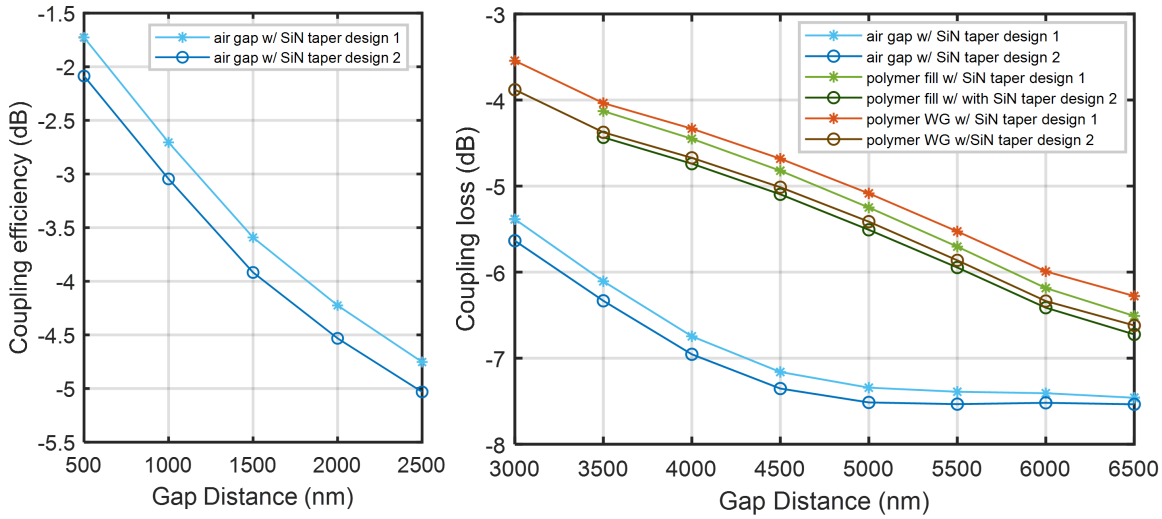

Figure 6.14: Simulations of coupling efficiencies with different gap distance for the various models. "SiN Taper Design 1" has a taper end width of 4.8 µm and "SiN Taper Design 2" has a taper end width of 5.8 µm.

Coupling loss lower than 3 dB can be achieved with an etched air gap only if the distance is shorter than 1 µm. For a longer distance, the coupling loss with air-gap drops substantially to 7 dB. This can be improved if the air gap is filled with a higher

index material. With advanced coupling region engineering as well as improvements in growth to shrink the sidewall polycrystal and faceting dimensions, the coupling loss can be reduced to about 5 dB at a gap of 4.5 µm, comparable to that of the air gap at a gap of 2.5 µm.

Note that the same SiN coupler cross-section and a straight angle is assumed here, as introduced in the beginning of Chapter 5. Clearly, optimized SiN coupler cross-section with mode matching according to the expanded optical profile with different coupling distance, and implementation of angled coupler and non-rectangular pocket geometry that reduce multiple facet reflection will benefit a better coupling efficiency, yet the experimental validation of these designs are challenging with the current integration process scheme due to the long development cycle with Si photonics passive components coming directly from a foundry production. Theoretical and experimental investigations at a smaller production scale, incorporating collective engineering of the pocket-end heteroepitaxy material, pocket geometry, and SiN coupler design would offer a more comprehensive demonstration of optimized coupling, and such research is currently ongoing with templates with waveguides and pockets fabricated at UCSB cleanroom, outside the scope of this thesis.

6.4.2 Methods for improving coupling efficiency

Several methods have been proposed to improve the coupling efficiency. In addition to directly working on gap-fill and gap distance reduction as suggested by the simulation above, alternative scenarios of re-engineering of the coupling region, such as using selective MOCVD growth for a GaAs fill, and then etch and regrowth the QD stack in a "mini-pocket" inside the pocket, are also proposed. Table 6.3 lists out six options that are currently being developed in this project.

Methods for improving coupling efficiency			
No.	Method	Description	Merits
1	Polymer (BCB)/Oxide fill	BCB/oxide fill and etch back at air gap Improved refractive index matching	Lower reflection and diffraction, compatible with all other methods
2	MBE partial selective growth	Selective buffer growth with MBE enabling delayed polycrystalline formation for a smaller gap distance	Reduces coupling gap distance by over 2 µm
3	MOCVD fill, etch and MBE regrowth	MOCVD GaAs fill, etch and MBE QD stack regrowth	Potential zero gap coupling and no polycrystal on sidewall
4	MOCVD selective and MBE QD hybrid growth	MOCVD half-stack with GaAs buffer with AlGaAs or InGaP n-cladding; MBE QD growth on MOCVD half-stack	Potential gap reduction with partial MOCVD selective stack
5	MOCVD selective wet-etch and regrowth	MOCVD n-AlGaAs template selective wet-etch for polycrystal removal; MOCVD QD regrowth on etched templates	Gap reduction with selective wet etch half-growth
6	MOCVD full selective growth	MOCVD selective growth with InGaP claddings and QD active regions	Potential one-step growth with minimum gap

Table 6.3: List of proposed methods for improving on-chip coupling efficiency.

In the table, method #1 and #2 are direct improvement that could potentially reach the 5 dB loss point in the numerical study with a reduced coupling gap and higher index material fill, keeping the heteroepitaxy integration scheme MBE growth on MOCVD template (500 nm GaAs/ 200 nm GaP) on Si. Method #3 and Method #4 explore the possibility of a hybrid approach of MOCVD and MBE growth, taking advantage of the possibility of selective growth with MOCVD and the robust QD growth quality with MBE. Method #5 and Method #6 are pure MOCVD growth solutions [6, 7, 8], and challenges of selective growth of InGaP cladding for QD active regions may be mitigated by growing the bottom cladding non-selectively using AlGaAs as a compromise, and

regrowing the remaining stack after a short processing of polycrystal removal after the bottom growth section, resulting in a final epitaxial stack as close to the pocket sidewall as possible.

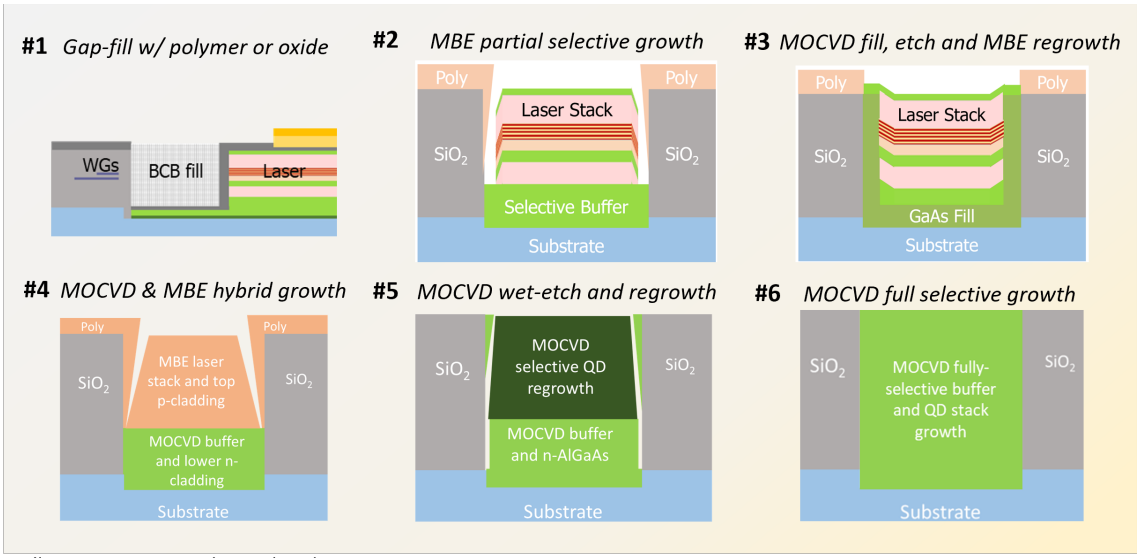

Illustration #2-5 credit to Alec Skipper

Figure 6.15: Schematic illustrations of the proposed methods for improving coupling efficiency. Method #1: gap-fill with polymer or oxide; method #2: MBE partial selective growth; method #3: MOCVD fill, etch and MBE regrowth; method #4: MOCVD & MBE hybrid growth; method #5: MOCVD wet-etch and regrowth; method #6: MOCVD full selective growth.

Figure 6.15 collects illustrates of the methods. Method #2 and #4 are possible to push the distance of gap at pocket-end shorter, possibly into the range of 2 - 3 µm, which will provide a short-term improvement of the coupling efficiency for early demonstrations of the project.

If one wants to further lower the coupling loss and enter the regime of making functional devices with passive components, such as single-wavelength laser or tunable laser using external coupled cavity or external reflectors, a shorter gap may not be enough. To push the III-V mode closer to the SiN area, it may be essential to force a larger portion of selective growth to fill the pocket, such as method #3, #5 and #6. The

challenge of these methods raises from the difficulty of growing QD active region reliably with MOCVD, and engineering the regrowth interface if using a hybrid or MOCVD-only hybrid approach.

In the next subsection, we will talk about details in the current process and growth development on method #1 and #2.

6.4.3 Development for improving coupling efficiency

BCB gap-fill process development

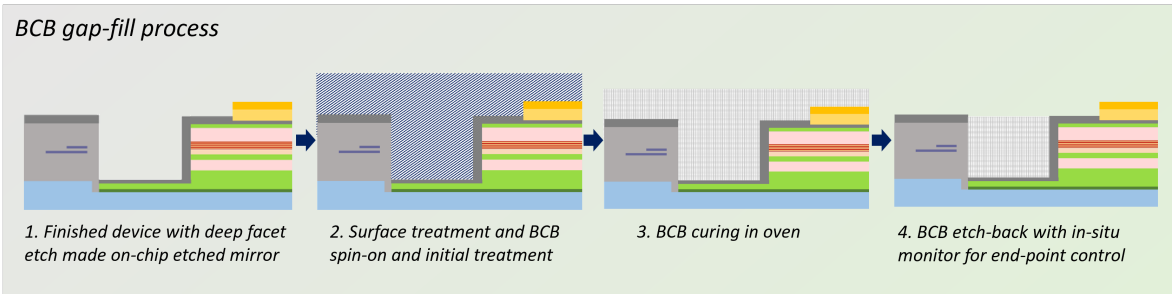

Figure 6.16: Illustrations of the BCB gap-fill processing steps.

The gap-fill process with BCB is developed at UCSB Nanofab. Figure 6.16 shows the process flow. The concept is to utilize BCB as a spin-on material that fills-in the pocket-end etched slots, overflows with thorough coating on the sample top surface, and planarizes after thermal curing. The etch-back step is performed with *in-situ* monitor in an ICP dry-etch chamber, in a similar manner to the making of self-aligned PMGI proctection mask for polycrystal removal in Chapter 4.

Note that this method is compatible with any growth method and can be added in the end of the device fabrication. The curing step is conducted in a thermal oven at 250 °C with 1 hour of soak time and a few hours of ramping and cooling down before and after, which is considered safe for the QD material quality and the electrical contacts.

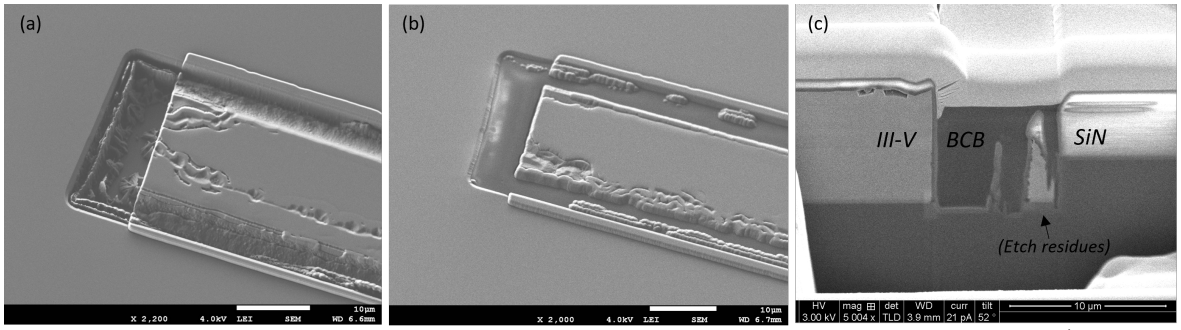

Figure 6.17: SEMs of the BCB gap-fill process development results. (a) Test structure with a simple hardmask facet etch; (b) test structure after BCB spin-on, curing and etch back; (c) FIB cross-section SEM of the BCB gap-fill region on the test sample.

Figure 6.17 shows SEMs of our process development result, where a test structure was created with a simple facet etch (without using the wet-and-dry combined hard mask, thus having large residues near pocket as expected), and then the BCB process is conducted. After etch-back, the surface of the sample is revealed and only the gaps were filled up to a similar height. The FIB cross-section SEM shows the level of fill up to within 500 nm under the top surface on the pocket side. The small distance is attributed to slight over-etch during the etch-back step when using laser monitor, and may be improved with a careful etch-rate calibration for better thickness control[5].

[5]Note the defect in III-V from CMP damage shown on this sample will be discussed in the later section of this Chapter. The tall etch residues in the gap also can be addressed with the developed wet-and-dry combined hardmask facet etch presented in Chapter 5.

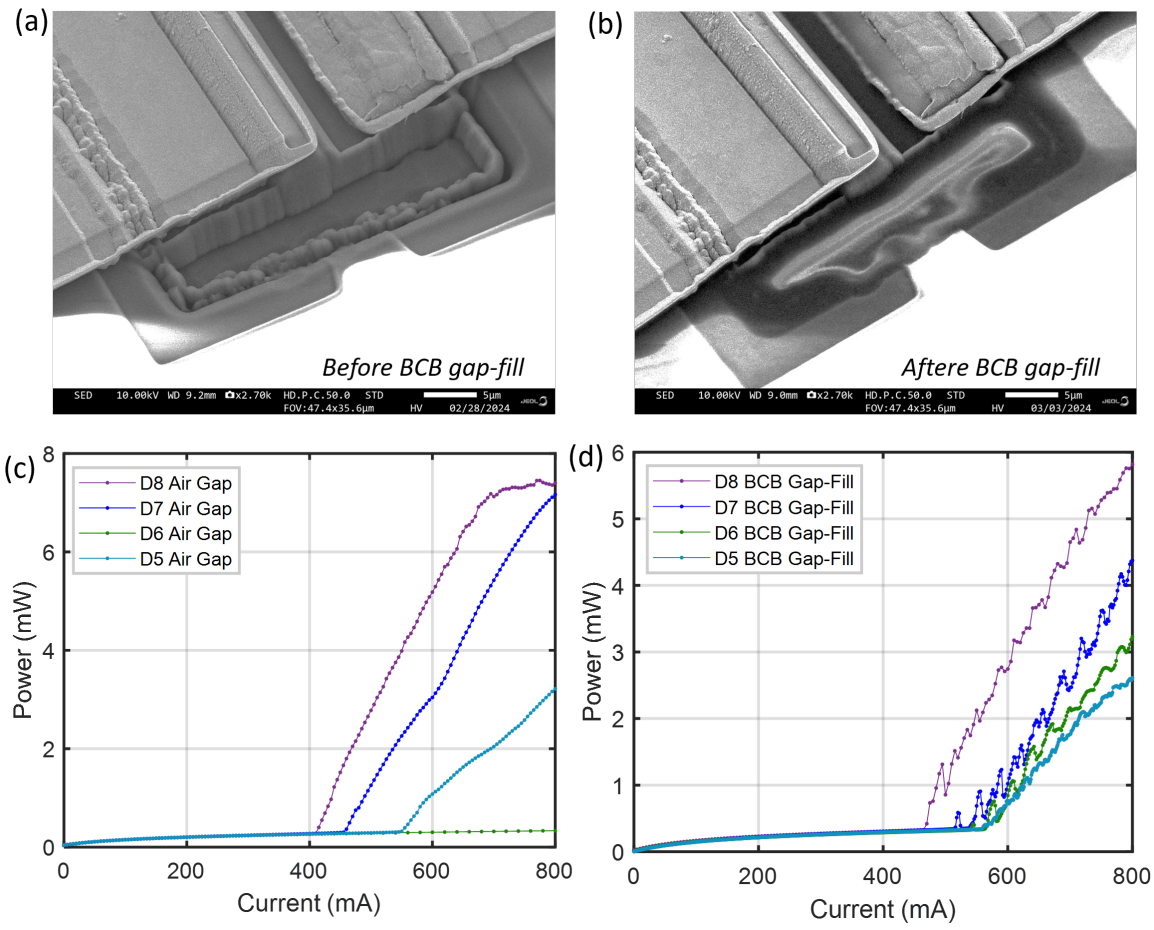

Figure 6.18: Top: SEMs of a finished etched-facet laser with external cavities (a) before BCB gap-fill with an etched and passivated air gap, and (b) after BCB gap-fill with cured and etched-back BCB in the coupling region. Bottom: Integration sphere LIVs of four etched-facet laser with external cavities on the same sample (c) with etched and passivated air-gaps, and (d) after BCB gap-fill with cured and etched-back BCB for enhanced coupling to the external cavities.

Figure 6.18 shows perspective SEMs of the coupling region of a finished in-pocket etched-facet laser coupling to external cavities, (a) before and (b) after the BCB gap-fill process. Design of the cavities were described and shown previously in Chapter 5 with Figure 5.38. Bottom of Figure 6.18 shows the integration sphere LIVs of four devices on the same sample (c) with air-gap and (d) after BCB gap-fill. The difference in LIVs with additional ripples after BCB gap-fill suggests enhanced coupling to the designed

external cavity containing silicon micro-ring resonators. In particular, D6 showed LED performance with the etched-facet air-gag and turned into a laser after BCB gap-fill, showing potentially reduced effective mirror loss with lower coupling loss to the external cavities. Further testing of these devices is currently ongoing.

MBE partial selective growth fabrication results

Early results of partial selective growth has pushed the distance from sidewall polycrystal and faceting below 3 µm. Figure 6.19 shows a cross-section SEM of the in-pocket growth.

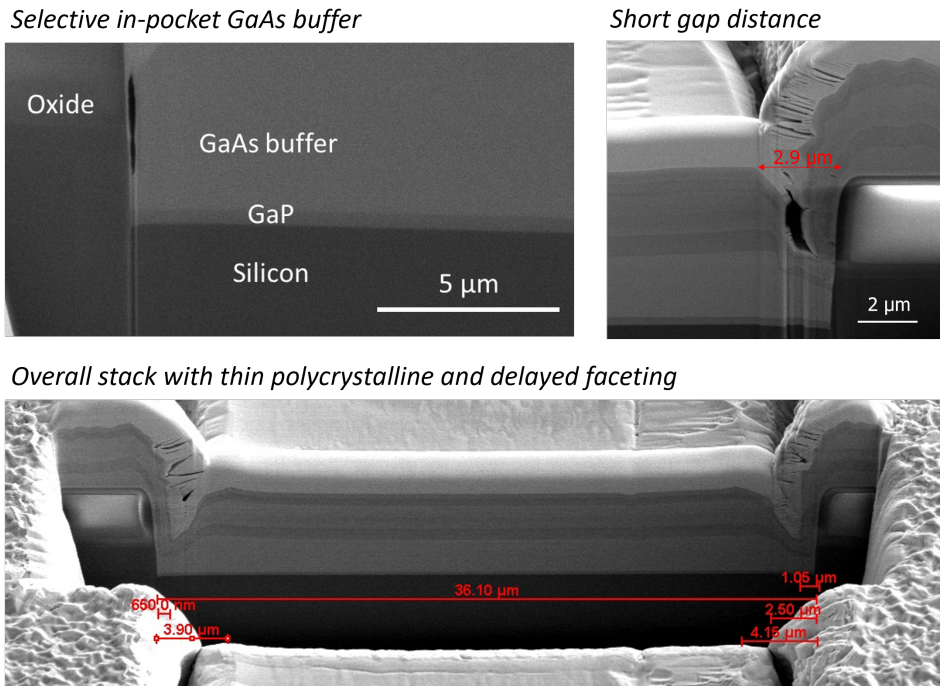

Figure 6.19: Cross-section SEMs and FIB SEM of the in-pocket partial selective MBE growth.

In the case of actual fabrication with etched facet lasers, actual distance needs to be taken into consideration including alignment clearance, the isotropic nature of wet

etch, and safety distance between the dry-etch and wet-etch boundaries. An additional expansion of at least about 0.5 µm will be added at the wet-etch window, and with the clearance, at least another 1 µm is considered to ensure a clear unaffected dry-etch boundry for the vertical facet etch. In the actual fabrication of the sample, we pushed the designed air-gap distance to be 5.5 µm. Figure 6.20 shows a comparison of the top-view microscope of the finished sample with the 5.5 µm target facet-to-boundary distance (measured about 6 µm), versus the first-batch of etched-facet coupled lasers with splits of 8 - 11 µm gap (measured about 11 µm).

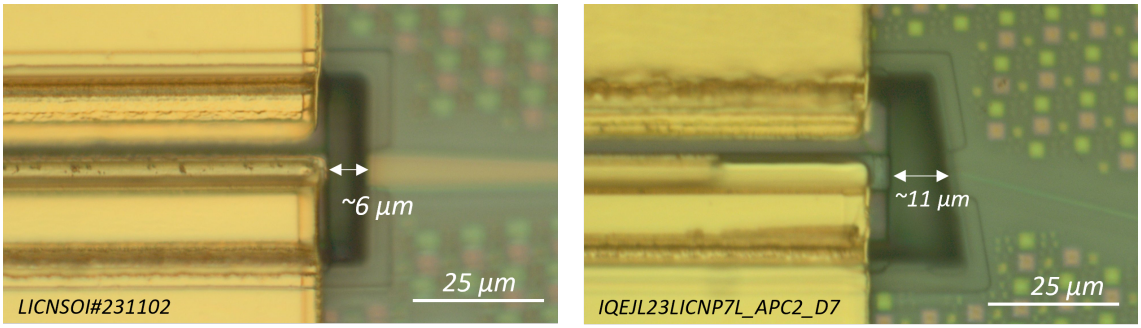

Figure 6.20: Top-view microscope images of finished samples, showing shorter facet–to-boundary distance in fabrication enabled by the shorter gap with partial selective MBE growth. Left: LICNSOI#231102 with partial selective MBE growth, 5.5 µm target facet-to-boundry distance; right: IQEJL23LICNP7L with normal 300 mm in--pocket MBE growth, 10 - 11 µm target facet-to-boundary distance.

Measurement on quantifying the improvement in coupling efficiency is currently on-going. Along with the remarks from Chapter 5 results, we expect to be able to quantify the improvements of on-chip coupling efficiency with different methods after developing the deeply etched Si trench for vertical fiber coupling to ensure a stable low loss coupling between the SiN edge coupler and optical fiber[6].

The method of partial selective regrowth may be further explored with alternative

[6]Discussions on the deeply etch Si trench for vertical fiber coupling for on-chip testing will be covered in later sections of this Chapter.

designs of the QD stack. By using an offset stack design with a in-pocket monolithic integration from QD gain section to GaAs waveguide, one may be able to enable high quality lasers made fully in-pocket. Figure 6.21 illustrates this idea. With the far separation of the laser gain section and the pocket boundary, one can enable a passive butt-coupling of GaAs and SiN waveguide at the pocket end, which will introduce less uncertainty and unwanted feedback to the laser cavity. Moreover, with partial selective growth it may be possible to grow the bottom GaAs waveguide fully selectively, restoring a "small gap" connection from the in-pocket III-V to the SiN waveguides.

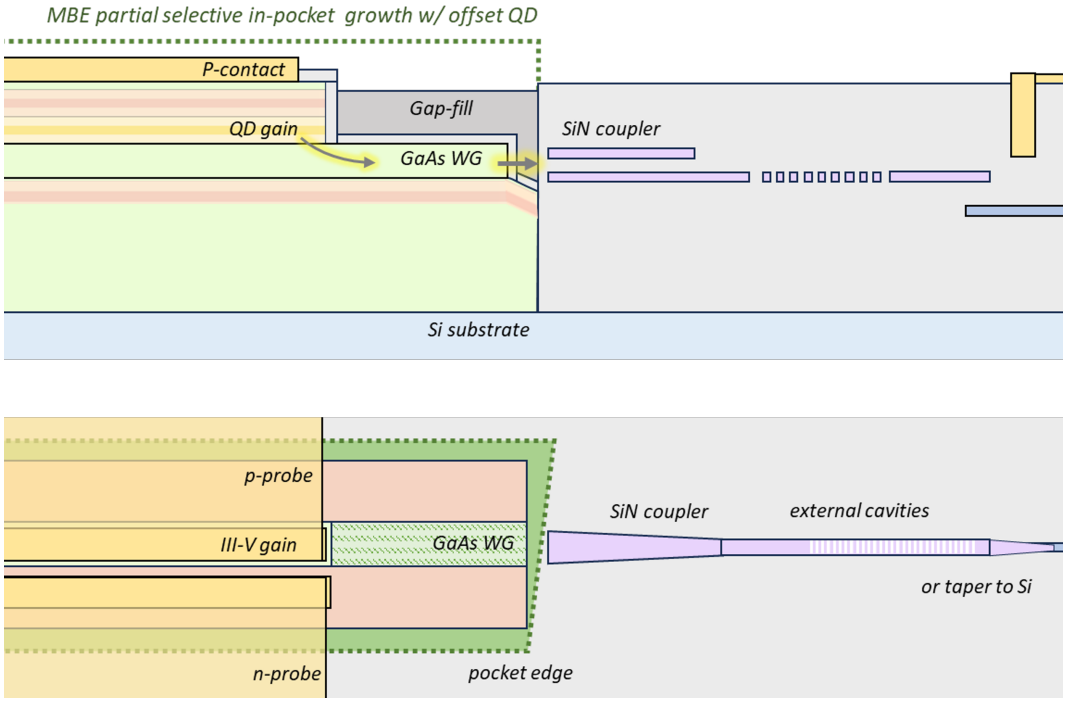

Figure 6.21: Top-view and side-view schematics of the proposed in-pocket offset QD stack with partial selective MBE growth for in-pocket QD lasers and efficient coupling from GaAs waveguide to SiN waveguides.

This scheme is particularly promising as it can possibly enable the making single wavelength lasers with in-pocket DFB grating or DBR grating on GaAs , and the coupling can be established without the complication of MBE/MOCVD hybrid handling or any

etch-and-regrowth. If the coupling loss is low enough with the GaAs waveguide to SiN waveguide transition, external reflectors with SiN grating or Si rings can be added as well. With high quality in-pocket QD growth and wafer-scale uniformity across different pattern density from MBE growth already established, it is an approach worth exploring in the very near future.

6.4.4 Discussions and future prospect

Table 6.4 shows the status of development of the proposed methods and comments on the challenges in transferring them to 300 mm scale.

Some process are considered less common on a 300 mm scale, but can be adjusted accordingly to reach the target. For instance, the BCB fill-and-etch process may be substituted by oxide fill and CMP planarization, followed by additional via opening for the metal contacts if needed. Controlled or patterned wet-etch processes of III-V layers are also a common concern, but not technically impossible and could be addressed with specific knowledge transfer and personnel training. In terms of growth aspects, MOCVD growth-rate non-uniformity is the main concern [7], along with concerns regarding cost efficiency for extended growth time or multiple regrowth.

6.5 Challenges with yield and scaling towards 300 mm scale

The transition from prototype demonstration to large scale production in a photonic foundry facility introduces new challenges in wafer handling logistics, process availability in a foundry environment, quality control methodology during and between processing

[7]We will discuss about this in detail in section "Challenges on yield and scaling towards 300 mm" later in this Chapter.

Remarks on technology readiness and compatibility with 300 mm platform			
No.	Method	Readiness	Compatibility with 300 mm
1	Gap fill w/ polymer (BCB) or oxide	BCB Fill developed at UCSB device fabrication	Oxide fill is compatible with 300 mm process µm
2	MBE partial selective growth	Developed at UCSB MBE, ready to transfer to IQE	Technically possible, yet slow growth rate may need further consideration at a 300 mm facility
3	MOCVD fill, etch and MBE regrowth	Proof-of-concept developed, further growth experiments ongoing	Compatible with 300 mm, changes to CMP for planarization will need further development
4	MOCVD selective and MBE QD hybrid growth	Hybrid growth finished, under device fabrication at UCSB	Compatible with 300 mm, but need to address growth-rate non-uniformity on MOCVD growth
5	MOCVD wet-etch and regrowth	Selective wet etch developed, under MOCVD growth at UCSB	Compatible with 300 mm, but need to develop wet etch and cleaning procedures at 300 mm scale
6	MOCVD full selective growth	Not yet demonstrated, ongoing studies at UCSB MOCVD, need to address challenges with InGaP cladding and QD growth	Compatible with 300 mm, but not demonstrated with small coupon yet

Table 6.4: Remarks on technology readiness and compatibility with 300 mm platform of the proposed methods for improving coupling efficiency.

steps and many other aspects. These factors collectively impact the overall device yield and performance uniformity, necessitating careful consideration and proactive measures to address them effectively.

In this section, we will cover several issues currently under development and the strategies to mitigate them.

6.5.1 MOCVD growth non-uniformity

Visible damages on wafers after CMP polishing

The impact of pocket geometry, including orientation and size, on the growth quality of in-pocket QD was previously covered in this Chapter. Ensuring favorable orientation for nucleation as well as wider pocket size will help managing in-pocket QD uniformity and provide repeatable and higher quality epitaxial materials.

While the previous discussions have centered on the in-pocket MBE growth aspects, there is another critical factor influencing in-pocket epitaxial layers in the final wafer, that is the growth quality of the MOCVD template layer preceding the MBE epitaxial stack growth.

The MOCVD growth was performed at $NAsP_{III\text{-}V}$ GmbH with pre-growth treatment, directly on the in-pocket Si surface selectively [9, 10]. It contains 200 nm GaP layer followed by 500 nm GaAs acting as a seed layer, a total of 700 nm III-V materials by design. The MBE growth follows the MOCVD growth, and the total stack height including the GaAs buffer and filter layers was designed to line up towards the same top surface as the oxide template, while the center of the QD mode is also designed to line up vertically with that of the SiN couplers at the pocket ends.

Starting from late 2022, the wafers that went through 300 mm full-scale MBE growth at IQE Inc. have gone through the newly developed 300 mm CMP polycrystal removal process prior to dicing and shipment to UCSB for small-sample process development.

The first batch of post-CMP wafer had a circular halo-like pattern from top-view microscopy inspection under both optical mode and Nomarski mode, as shown in Figure 6.22. A close-up look confirms that there exists a top oxide-like layer with gradual change of thickness, and the top epitaxial layer also seems to be polished off in a gradual manner, as shown by the gradual change of color for the exposed in-pocket material at pocket

ends. In the pocket with no remaining oxide, there is also a visible gradient at surface indicating a gradual change of layer thickness.

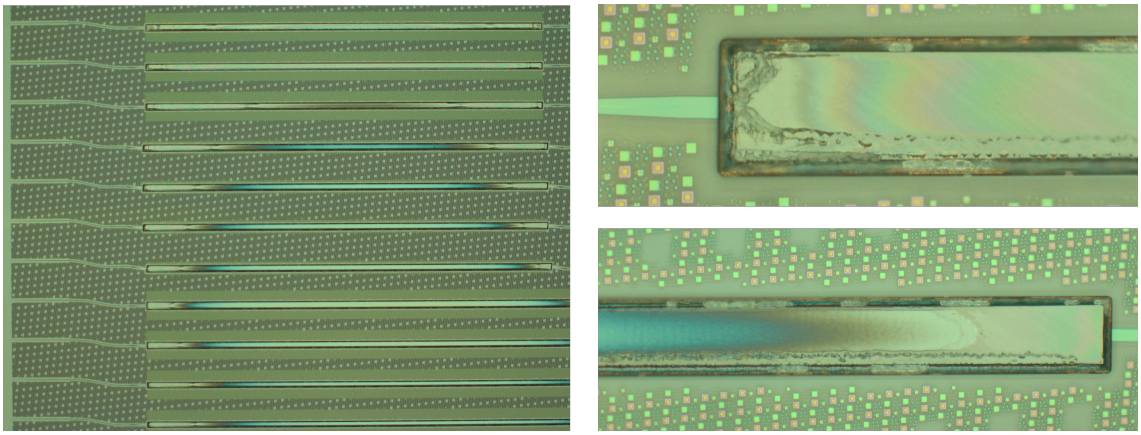

Figure 6.22: Top-view microscope images of post-CMP wafer with halo-like pattern showing surface non-uniformity.

In some extreme cases, the QD layer is also partially polished away during the CMP. This can be informed from the PL variations across the same pocket at different distances towards the pocket end[8]. As shown in Figure 6.23, the PL intensity gets weaker as the spot gets closer to the end of pocket, where the very end where visibly the stack is further damaged, there is no QD PL signal at all (orange line), indicating the entire QD layer may have been damaged.

[8]Previous PL characteristics has always shown consistent PL along the length of the pocket and no QD growth dependency on the longitudinal location has been found.

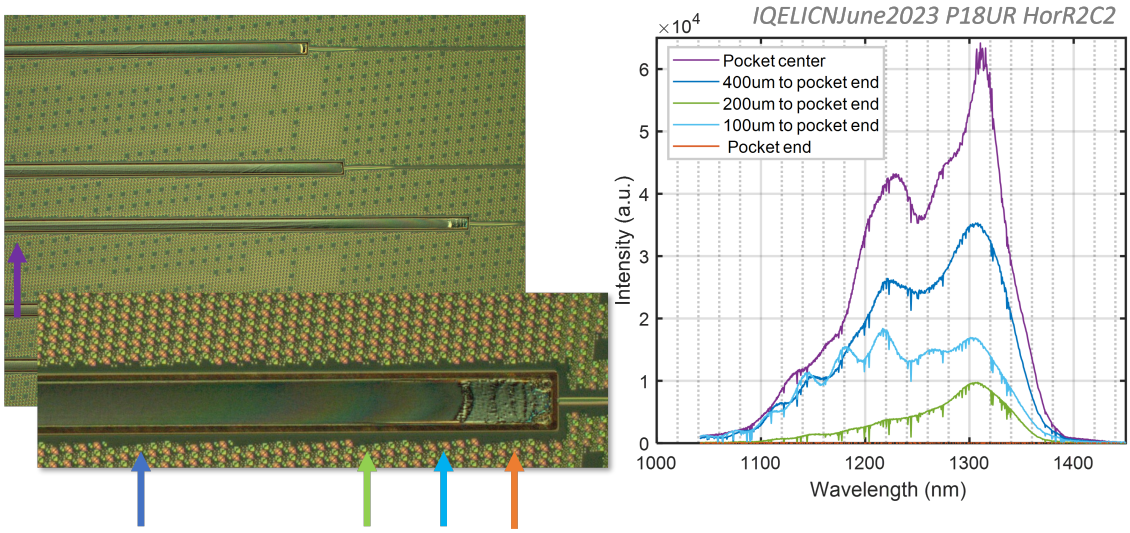

Figure 6.23: PL intensity difference along pocket length near pocket end suggesting damaged QD layer. Left: top-view Nomarski microscope images showing different spots along the pocket; right: local PL intensity taken at corresponding spots, with color of the line plot matching color of the arrows in the left figures.

Inspections showing MOCVD template thickness variation

This pattern, previously unseen in wafers without CMP treatment, indicates either a uniformity issue with the CMP step or thickness variations in the initial stack. A closer inspection was conducted by cross-section SEMs. Figure 6.24 shows two cross-sections taken at different count of the same group of pockets on same area of the same die on the same wafer (also with the same pocket width and orientation), device count #1 from top and device count #6 from top. The two pockets have different total layer thickness, so the exposed layer at the pocekt surface is different after polishing. The MOCVD GaP thickness measured is 380 nm on #D1, and 250 nm on #D6, a 90% increase and 25% increase compared to the desired thickness of 200 nm, suspected to be the cause of the issue. The thickness difference in GaP layer can be linearly projected to estimate the total MOCVD template thickness to be 1330 nm and 875 nm respectively, 630 nm and 175 nm thicker than the desired thickness of 700 nm (200 nm GaP and 500 nm GaAs).

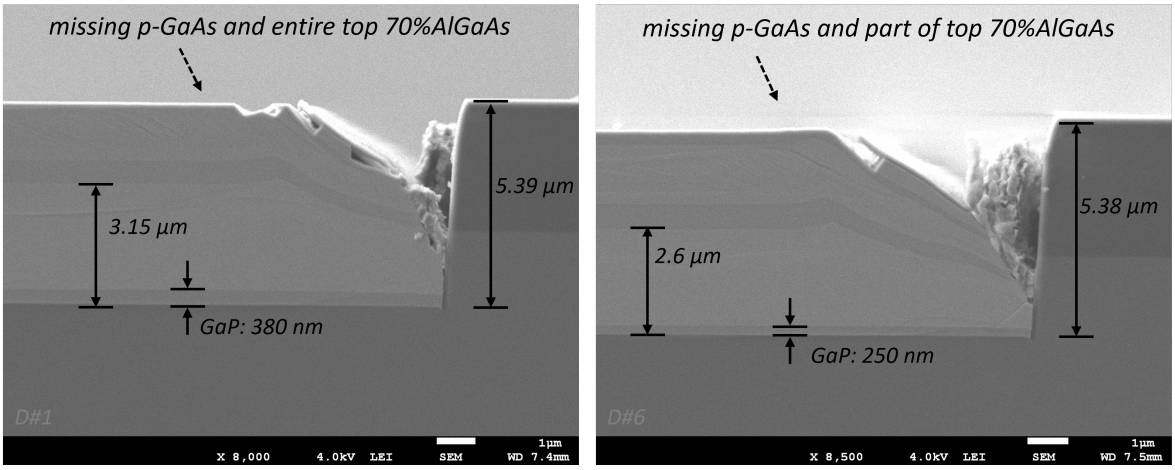

Figure 6.24: Cross-section SEMs at different pocket in the same group on the same die on the same wafer (IQE LICN June2023 P13), with same pocket width and orientation), measuring different MOCVD template thickness. Left: D#1 with 380 nm GaP; right: D#6 with 250 nm GaP.

Our collaborators also conducted on-wafer AFM line-measurement of the in-pocket template height after MOCVD growth, and thickness variations were observed with a similar trend.

Upon further discussions, it becomes evident that there has been significant non-uniformity of the MOCVD template growth rate both at different location of the same pocket and across different pockets throughout the wafer. In particular, the growth rate is higher as it gets closer to both ends of pockets and higher at pockets that are more sparsely spaced (with a higher "pitch" width). Comprehensively, this can be seen as a result of lower effective pocket density at given areas, causing higher growth rates from the nature of selective MOCVD growth.

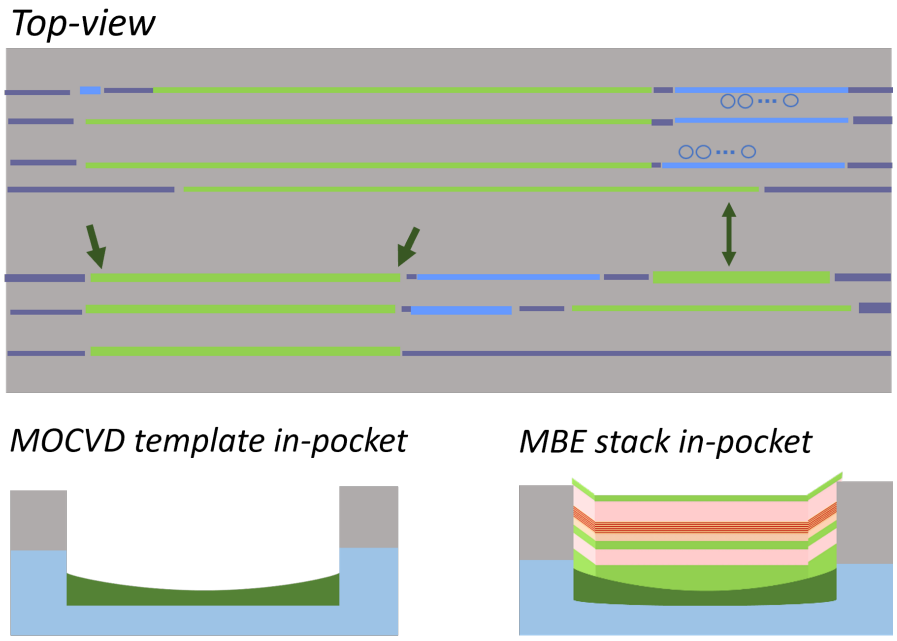

Figure 6.25: Illustrations of in-pocket MOCVD template non-uniformity and resulted stack thickness variation along pocket longitudinal direction and across different pockets.

Consequently, the template layer curves upward at pocket ends, and also appears thicker at the pockets locating at the edge of a cluster of pocket arrays, as illustrated in Figure 6.25. In the subsequent MBE growth, the growth rate remains uniform both inside the pocket and between different pockets across the wafer, which translated the thickness difference in template towards variations of total stack heights. The CMP process planarizes the wafer, and even with careful consideration of monitoring the reaction for stopping, the oxide protective layer gets polished off earlier at locations where the material is thicker, and the top epitaxial layer gets revealed and damaged even before the oxide protective layer is removed at locations where the material is thinner (the center pockets and center of the pockets), resulting in the bluiesh hue in the center with a circular edge from a zoomed-out top-view and the gradual gradient changes radiating outwards indicating gradual changes of layer thickness in subsequent layers from the

CMP acting on curved epi layer stacks.

Such thickness variation has created many obstacles in the laser fabrication phase, and much of the development included in Chapter 5 was all made with these wafers, making it extra hard to demonstrate etched-facet lasing, not to mention efficient lasing. For example, on the "Lincoln" test site, a portion of the designed circuits had a larger pocket pitch (about 510 µm) than most of the other ones (190 - 200 µm) , and the 300 nm top p-contact GaAs layer was polished away in every single one of the pockets in the 510 µm pitch areas, causing those areas to be "completely annihilated" even though there was no fault in the fabrication steps or integration design. For the areas where only the ends of the pocket had missing top layer, lasers could be made, but visible scattered light can be seen at the ragged transition line of the two layers from polishing damage during LIV screening, indicating undesired scattering loss, not to mention the inefficient pumping of the p-contact where the highly doped p-contact layer was gone and p-metal stack was made directly contact into the underneath AlGaAs cladding layer.

One might argue that, in the case where the wafer goes through an alternative process such as the polycrystal removal wet etch instead of CMP, the effect of thickness variation would not cause any missing top layer. Its impact on the fabrication process can also be mitigated by carefully design the layers and manually addressing issues such as focus shifting and PR spin-coating non-uniformity from the curved epi. This is only partially true, as even if the finishing device could exhibit uniform current injection (with thickness variation affecting mesa etch) and the bend in the ridge waveguide can be tolerated in the Fabry-Perot mode, the coupling region engineering and vertical alignment of the epitaxial stack and the SiN waveguide modes are also critically affected by the in-pocket stack thickness variation. The thickness non-uniformity is impractical for a monolithic integration platform, where uniform epitaxial layer thickness is critical for wafer-scale semiconductor processing and the vertical alignment between components needs to be

precise for the desired optical performance.

In conclusion, we have identified the local (within one pocket) and global (between pockets) variations on wafer as a direct result of MOCVD template growth non-uniformity linked to surrounding pattern density. It is crucial to mitigate these effects in order to establish a scalable heteroepitaxial platform for 300 mm Si photonics.

Methods to mitigate the MOCVD growth non-uniformity

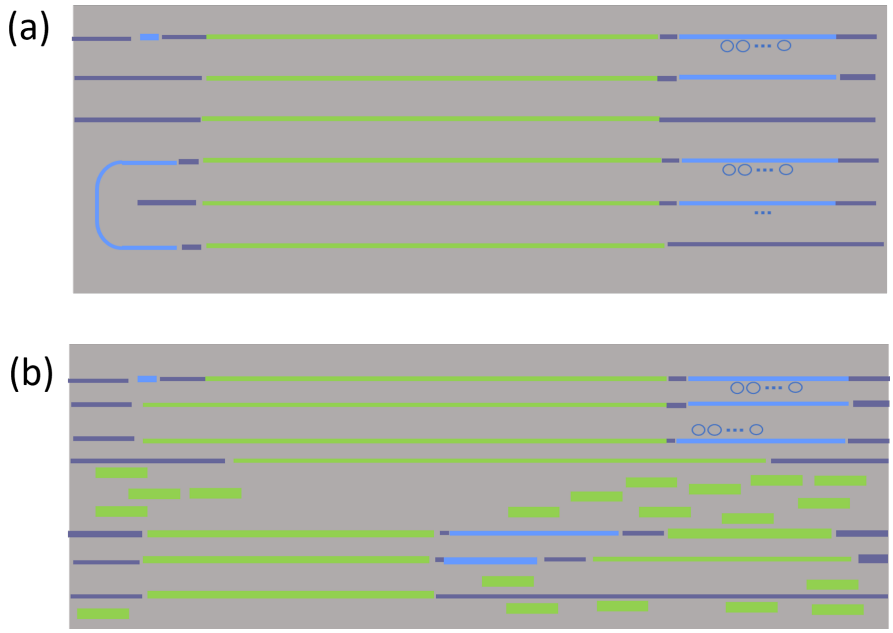

Figure 6.26: Illustrations of proposed mothods to mitigate MOCVD growth non-uniformity. (a) Fix pocket size, spacing and arrangement pattern, and (b) add "dummy fill" pockets at empty area to simulate a more uniform local pattern density.

Two methods are currently being implemented in the integration process in an effort to reduce the MOCVD non-uniformity.

The first is to arrange the pockets in a fixed pattern with the same size and spacing in order to keep the same growth rate along the pocket, as illustrated in Figure 6.26 (a). Some initial experiments from our collaborator indicated a lower density of pocket

(larger pitch size) would give a smaller template thickness variation, so the pitch size is also reduced from about 125 µm - 150 µm to 700 µm or as high as 900 µm in the upcoming development test site ("Castle").

The second is shown in Figure 6.26 (b), where many "dummy fill" is added to the empty area in the photonic circuit. Each "dummy fill" is made into a smaller rectangular pocket to adjust the local growth density during the MOCVD growth, aiming for cultivating higher growth rate uniformity. The "dummy fill" pattern is generated with automatic programs at the foundry and its effectiveness is currently being tested out.

The drawback of these two methods is the limitation of integration density, which is a betrayal of one of the original arguments of the monolithic platform for realizing low-cost, high-density integration. For example, for a suggested minimum pitch of 700 µm, there could only be 6 active lasers with 2.5 - 4 mm of active length and remaining circuits making up an area of 25 mm^2 (roughly 6 mm by 4 mm). This reduces the total gain density of single coupon measuring 26 mm x 32 mm to lower than 200 gain sections per coupon, without taking into account the space allocated for test structures intended for passive-only tests and process debugging. The effectiveness of the "dummy fill" is also a trade-off with integration density of passive structures occupying the rest of the territory. As a comparison, in the case of heterogeneous integration with die-to-wafer bonding and substrate removal, no minimum pitch is required and the active cavity length can be 500 µm or shorter with the implementation of low-loss taper couplers and Si-based external reflectors.

There are some alternative approaches to address this issue, which have not been tested in our platform yet. For example, it would also be beneficial to simply have a thinner template thickness, such as changing the 500 nm GaAs seed layer to 200 nm or 300 nm thickness, so that by so that by percentage the vertical offset that is created by MOCVD growth non-uniformity can be reduced. Though we expect the change to not

pose any negative effect on the growth quality for the template and MBE epitaxial stack, it has been difficult to try out this idea due to limitations in the overall risk management, budget control and project coordination[9].

Another way is to use one large open area for III-V growth separated and adjacent to passive-only areas instead of having many compact pockets. A comparable level of integration density can be enabled with careful routing and integration design. Though this configuration was initially considered as lack of design flexibility and compactness for full integration of functional photonic circuits, given the current status of the reduced design flexibility and density in exchange for restoring the growth quality when using long pockets as individual gain sections, it is worth reconsidering switching to large open area.

In fact, many of the growth effects presented in this project, including QD growth dependency on pocket orientation and width and MOCVD growth non-uniformity due to local density, can all be mitigated if the long narrow pocket configuration can be changed. This is considered as a price to pay in overall project flexibility when having multiple collaborators and long development cycles and limited budget and personnel, a recurring theme in many historical technology struggles and breakthroughs.

6.5.2 Wafer quality and contamination

We observe defect lines in-pocket repeatedly from both the diced MOCVD templates on Si, and the wafers with 300 mm MBE growth, as shown in Figure 6.27. The "defect" is used to describe a local denting of the III-V epitaxial stack, transferred from the unevenness at the MOCVD template level towards top surface of in-pocket MBE growth growth stack. The line is visible under both optical mode and Nomarski mode in the

[9]Being a common non-technical issues involved for technology transfer and process scaling, hopefully this could be potentially improved with better communication across different team players and overall strategy management.

microscope, and the FIB cross-section across the pocket on the right of Figure 6.27 shows the stacked denting in every layer.

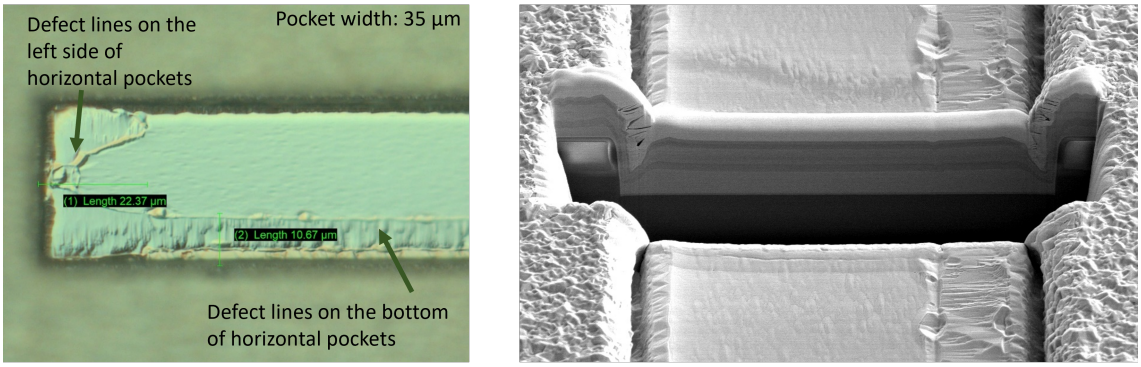

Figure 6.27: Top-view microscope image and FIB cross-section SEM of the in-pocket material with defect lines.

Defect lines at side of pocket as well as at the ends of pockets have been observed for both horizontal and vertical pockets, and there has been a repeated pattern of their placement, usually preferred in horizontal pockets at the bottom about 10 µm from the pocket side, or at the left end of forming two triangles with the left corners. It is also discernible in the vertical pocket close to the pocket left-side sidewall and at pocket ends, yet less severe than in the horizontal pockets.

During fabrication development runs in Chapter 4, the layout of the mesa and n-contact has taken into consideration the position of the defect lines to avoid overlapping with it to affect the structure, yet some still falls inside the "flat" footprint due to the narrow pocket width, as can be observed in some of the cross section SEMs shown in the initial process development section. This makes it also hard to conclude if the differences in defect lines for different pocket orientations have introduced another factor in evaluating the device performance when comparing the lasers from horizontal and vertical pockets in Chapter 4. This is distinct from differences arising from QD growth quality or pocket width.

On the other hand, the defects at the pocket ends are crucial as they add another challenge to the already complicated situation of polycrystal and faceting. As shown in Figure 6.27, the uneven surface will have a similar effect of faceting that hold sidewall oxide from hard mask deposition, and a trace of shadow will be left after the facet etch due to the under-removed sidewall oxide trapped at the defect dents. It is not preferred to solve this using a "wet-and-dry combined etch" method when clearing the III-V in the coupling gap, as the defect lines extend as far as 20 µm or longer. If fully removing the III-V materials in this scale, the area will need a complete new configuration in order to realize efficient coupling.

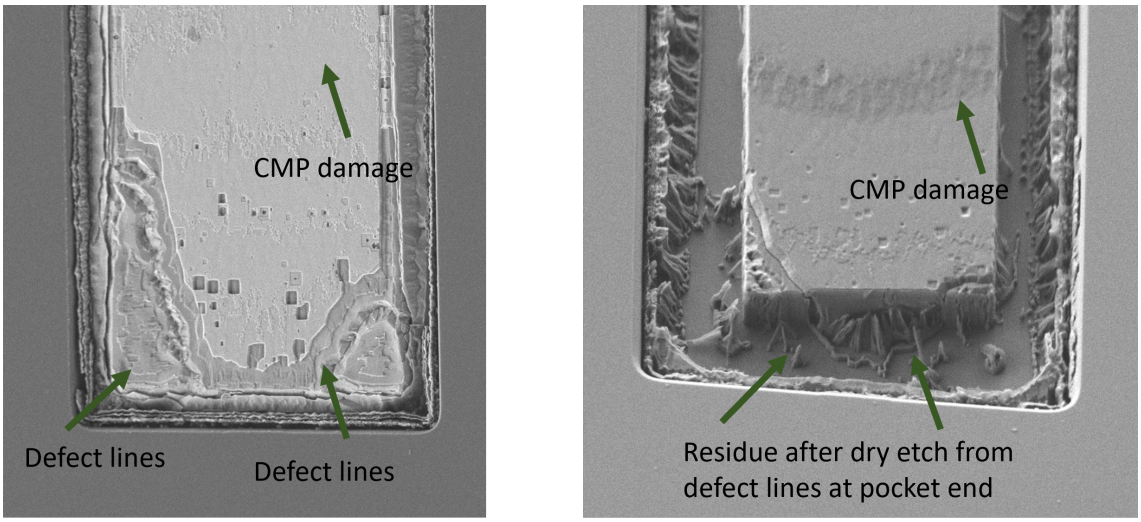

Figure 6.28: Top-view SEMs showing defect line leaving residue traces in dry etch. Left: CMP damage and defect lines visible from top of in-pocket epitaxial material. Right: residue traces from locations of CMP damage and defect lines after dry-etch.

So far, the formation mechanism of the defect lines is completely unknown. They are suspected to be either etching residues from the pocket etch at the Si photonics foundry, or some defect during the MOCVD template growth from our collaborators. The repeated local preference on one side of each orientation of the pockets hints it may be related to certain mounting angle and shadowing effect. However, inspections of the

wafer during oxide etching and pre-treatment for MOCVD growth fall outside the ability this research can operate, and unfortunately no further information was provided.

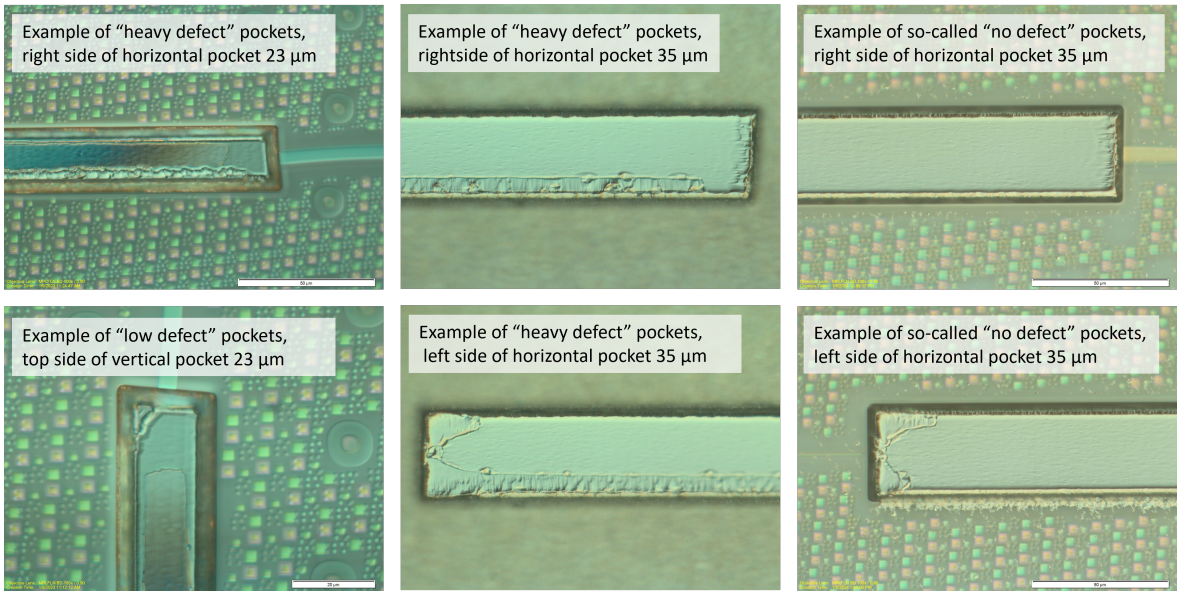

Figure 6.29: Examples of top-view microscope images of "heavy defect" and "low defect" areas for samples with 23 µm width and 35 µm width pockets.

On the bright side, or one may say two negatives make one positive, we notice that there is also wafer scale variations of the defect formation. Across different areas of 300 mm wafer, there may be heavier or lighter occurrences of the defect lines in each die (yet the location of defect lines within each pocket on the die still follows the same trend). Figure 6.29 shows examples of "heavy defect" and "low defect" for pocket of both 23 µm and 35 µm width. It is noticeable that for even for the "light defect" examples, there are still defect lines at the left side of the horizontal pocket that extend 20 - 30 µm longitudinally. However, there is at least an option of mitigating the effect by pre-screening the dies of MOCVD template before MBE growth, or by pre-screening the 300 mm MBE growth wafer before fabrication. [10]

[10]This effect was taken into consideration for the fabrications in Chapter 5. However, as mentioned

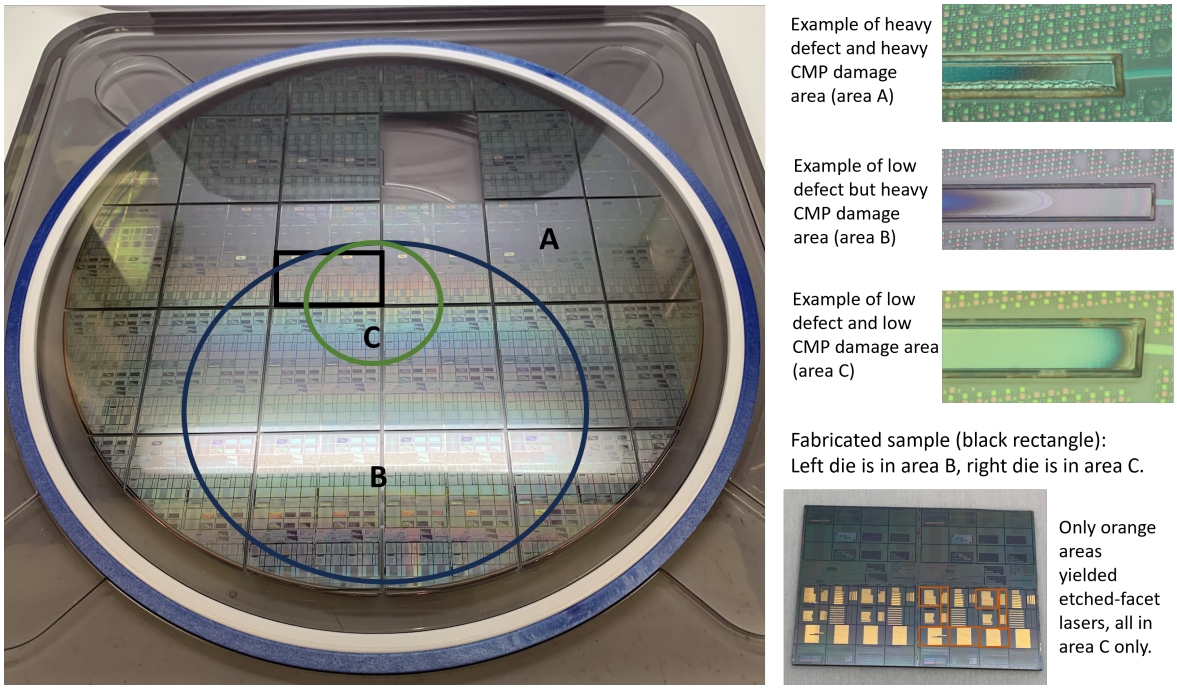

Figure 6.30: 300 mm full-wafer inspection showing ranges of (A) heavy defect and heavy CMP damage area, (B) low defect but heavy CMP damage area, and (C) low defect and low CMP damage area. Bottom right: image of fabricated sample showing on-chip laser yielding areas.

We were able to scan through the post-CMP and diced 300 mm MBE growth wafer to evaluate different severity of the defect lines in each die. Figure 6.30 shows a picture of wafer "IQELICN July 2023". "A" indicates the area outside the dark blue circle, which covers the majority of the wafer, exhibits both heavy defects and heavy CMP damages. Area "B" inside the blue circle is the bottom center part of the wafer, where the defect lines are lighter. However, for this wafer that has also gone through CMP with the MOCVD growth non-uniformity issue presented earlier, the majority parts of Area B still presents heavy CMP damage. Inside the tiny green circle in area "C", there is suspected to be a thicker oxide deposition, considered as a result of early CMP or oxide deposition

before, it is hard to conclude if the differences in defect lines for different pocket orientations have added another factor in evaluating the device performance when comparing the lasers from horizontal and vertical pockets in Chapter 4.

non-uniformity during SOI components fabrication and pocket patterning. This circle can be visible as a halo when viewing the wafer from an angle. As another "lucky" result, the slight increase in pocket oxide thickness or its effect on MOCVD tempalte growth inside circle "C" helps the area to have less CMP damage at the pocket ends, making it the most ideal or only ideal area for etched facet laser fabrication. Comparison of examples of pocket microscope images from area A, B, and C are presented in the right of Figure 6.30.

During the first fabrication attempt to demonstrate etched-facet lasers coupled to SiN waveguides, we picked the piece from the black rectangle (Piece #7CD). As it turns out, only the right side of the piece which falls into the green circle of area "C" has yielded etched-facet lasers. This result shows stark evidence of the wafer-scale yield affected by all factors including MOCVD template non-uniformity and oxide thickness variation, corresponding CMP effects, as well as defect lines and their non-uniform distribution.

Close inspections and detailed analysis have provided valuable insights regarding the current issues in-pocket both in a local variation of quality and the global variations regarding wafer-scale uniformity. Most of the issues and challenges presented here were previously unprecedented, and our understanding of the underlying science remains incomplete. The demonstrated in-pocket laser results, particularly the etched-facet lasers and their coupling to SiN waveguides, were achieved only through collective efforts to address each and every observed factor that could potentially impact the device performance, and proved the feasibility of such on-chip monolithic integration platform with QD heteroepitaxy. There is a market and hope for further expanding the results to a wafer-scale production, yet it is imperative to acknowledge the existing issues concerning uniformity and yield (in many of the cases, the hardest step is for a person in charge to acknowledge the presence of an issue). Further research should be carried out collaboratively to address these unique challenges across aspects of template preparation,

MOCVD and MBE growth, as well as device processing and post-processing.

6.6 Improvements of measurement technology on 300 mm scale for faster development cycle

The delayed incorporation of experimental results from earlier generations of device into future iterations, in the author's view, is one of the most significant challenges in the monolithic integration platform with Si photonic foundries, directly impacting the yield and scaling on a 300 mm wafer scale. Manufacture cycle from tape-out design submission and review to experimental results has been at least one year and up to three years, due to the nature of foundry process readiness, tool availability, shipment and communication between collaborators, time for post-processing and packaging, and many other unforeseen circumstances[11]. In order to push towards a faster development cycle, it becomes typical for designers to put out new generations of designs sometimes even without a chance to test the results of previous generations, which offsets the original purpose of planning for development cycles, such as the layouts of "Massive" following "Harvard", "Crestone" following "Lincoln" listed in Figure 6.2.

Such lagging is partially a result of the lack of technology readiness to cope with large-scale integration on 300 mm Si photonic platforms. Transitioning to the positive side, the circumstances have been improving dramatically in the past few years as photonic foundry service has become more commonly available, and there has been fast development in wafer-scale testing equipment as well as innovative designs for efficient implementation of process step debugging and device screening.

[11] Other circumstances can be clearance document routing in collaboration partners, import and export shipment time delays, extended tool maintenance down time due to global supply chain issues, or simply person in charge being on vacation at a critical time stamp.

Wafer-scale automated measurement



Figure 6.31: 300 mm scale automated probe system for photonic wafer. Left: at MPI booth, Optical Fiber Communication Conference and Exhibition (OFC), San Diego March 2022; right: at Bowers Lab in Henley Hall, UCSB, Aug 2022.

One example of such development is the availability of 300 mm wafer prober with photonics testing compatibility. Figure 6.31 shows an overview of the MPI TS3000 300 mm Automated Probe System, where it can load and scan chips and samples up to the scale of a full 300 mm wafer, as shown in the close-up look of the loading door in the left picture. With fully programmable hexapod holder and microscope as well as automation software solutions, the prober can directly scan, align and test selected devices of a 300 mm wafer without the need of dicing or manual shifting and alignment.

This can enable wafer-scale device screening and performance yield analysis, as well as other creative functions such as pre-programmed thermal processing with electrical contacts on wafer. It is a much desirable technology for pre-dicing testing especially for MPW wafers with full-wafer processing and no dicing or component singulation needed through complete monolithic integration as envisioned in this thesis.

Wafer-scale laser screening with on-chip integrated photodetectors

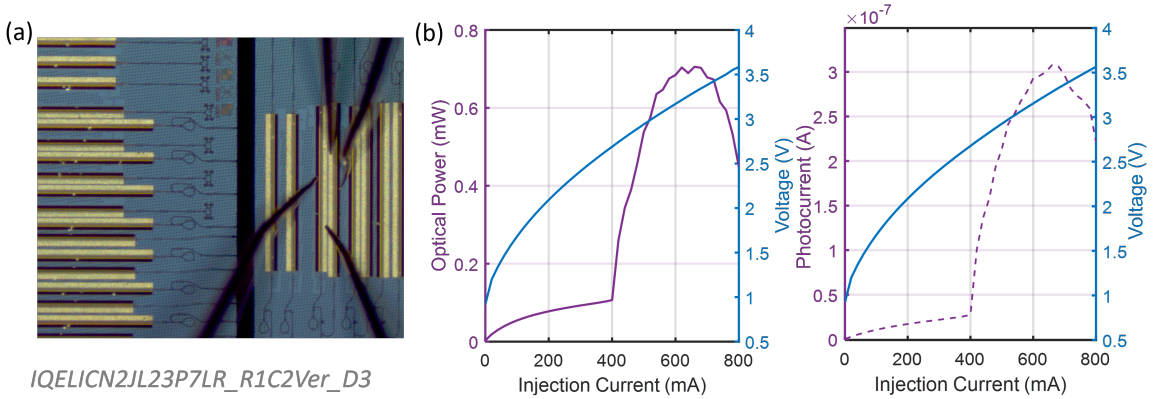

Figure 6.32: Wafer-scale laser screening. (a) Top-view microscope image of adjacent cavities on sample, (b) Left: LI from adjacent integration sphere measuring output power from increasing current; Right: Photocurrent collected from adjacent cavity at -1 V reverse bias during the current sweep.

As the 300 mm prober enabled wafer-scale testing without the need of dicing, on-chip photonic components with design-for-test (DFT) methodologies applied can enable quick screening and identifiers of device performance on the integrated platform.

To demonstrate this concept, we place two cavities in adjacent to each other, both in-pocket in a parallel configuration as shown in the top-view microscope image in Figure 6.32. Etched-facet ridge waveguide cavities were fabricated in the two pockets, respectively. Four sets of probe needles were used to apply forward bias on one cavity and reverse bias of -1 V on another, while the sample is diced out into a smaller piece and placed on a temperature-controlled testing stage next to an integration sphere. The forward-biased cavity is swept with increasing injection current from 0 - 800 mA, while the reverse-biased cavity current was read and plotted, as shown on the right side of of Figure 6.32 (b). On the left side of Figure 6.32 (b) was plotted the measured optical output power from the scattered light at the same time through the integration sphere placed in adjacent to the sample. Though the actual optical power needs further calibra-

tion to be determined, the plotted absolute value of the photocurrent on the right shows the lasing threshold (400 mA) and roll-over current for maximum power (about 650 mA) which provides critical insights on the performance of the laser under test.

Implementing a similar concept of on-chip performance monitoring, a variety of performance screening can be made possible with high efficiency on full-wafer scale. With further development of matured integrated laser with efficient on-chip coupling and fully integrated process including coupled photodetectors, improved testing scenarios with more exact numbers can be extracted with known and standardized component parameters such as laser-to-waveguide coupling loss, waveguide splitter ratio and photodetector responsivity.

Wafer-scale vertical fiber coupling with deep Si trench and edge couplers

In addition to on-chip screening with electrical probes, wafer-scale optical testing with fiber coupling can also be very desirable.

One solution is to use vertical couplers such as grating couplers in the PIC as monitoring ports for fiber coupling without dicing. However, grating couplers are usually more band-limited at low insertion loss, and they take up additional design territory when design space is rather limited in designs for a MPW project.

This issue is being addressed by creating edge couplers with coupling space made possible at boundaries of integrated circuits by extra-deep etching to create a "dicing trench" for potential fiber or fiber-array placement for edge-coupling at the dicing trench, enabling an angled vertical output. An example with details of the vertical fiber-array edge-coupling was presented by K. M. Jabon *et al.* at OFC in 2021 [11]."

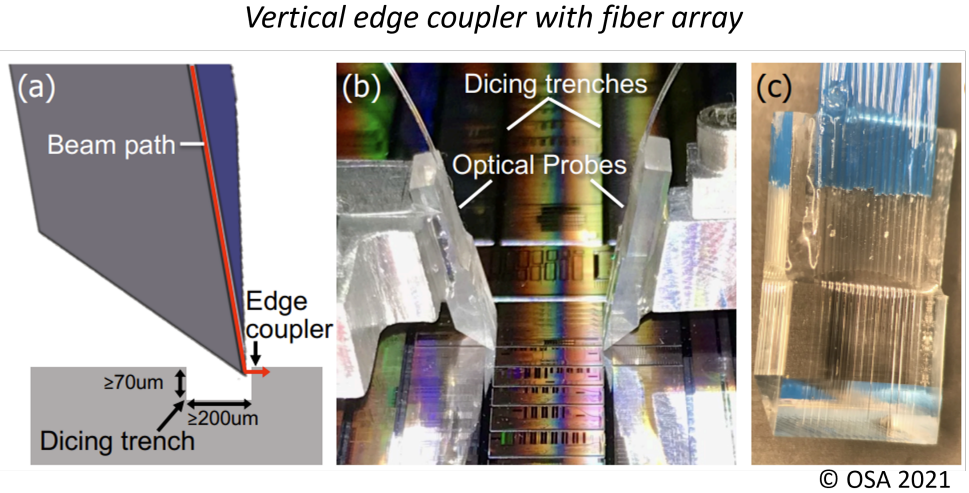

Figure 6.33: Vertical edge coupler fiber array. (a) optical probe side-view schematic showing first (40.3 °) and second (8 °) polishes. (b) Photograph of single-fiber probes in trenches. (c) Front-view photograph of 16-channel optical probe. Adapted from [11]. ©OSA 2021.

Figure 6.33 is adapted from [11]. (a) shows a side-view of the etched dicing trench and the fiber/fiber array with angled polishes. Figure 6.33 (b) shows two probes being mounted onto XYZ piezo actuators on hexapod positioners from a wafer prober and being lowered into place at the dicing trenches on sample surface. Figure 6.33 (c) shows a 16-channel probe with single-mode fiber, which demonstrates the scalability of this technology to parallel channel testing with complex optical I/O and PIC arrays. The fiber is polished on two sides to enable a transition from in-plane horizontal edge coupler emission light to the vertically tilted in-fiber light and allow for maximum mode matching [11].

A few similar wafer-scale vertical edge-coupling schemes have been presented, such as [12] at OFC in 2018 and [13] at ECTC in 2023.

The polished fiber array is commercially as products such as “trench probe fiber array units (FAUs)” available from PLC Connections, which can be made with either single-

mode (SM) or polarization-maintaining (PM) fiber with a typical tip angle of 50 °and can be used for trenches as small as 50 µm wide and 50 µm deep [14].

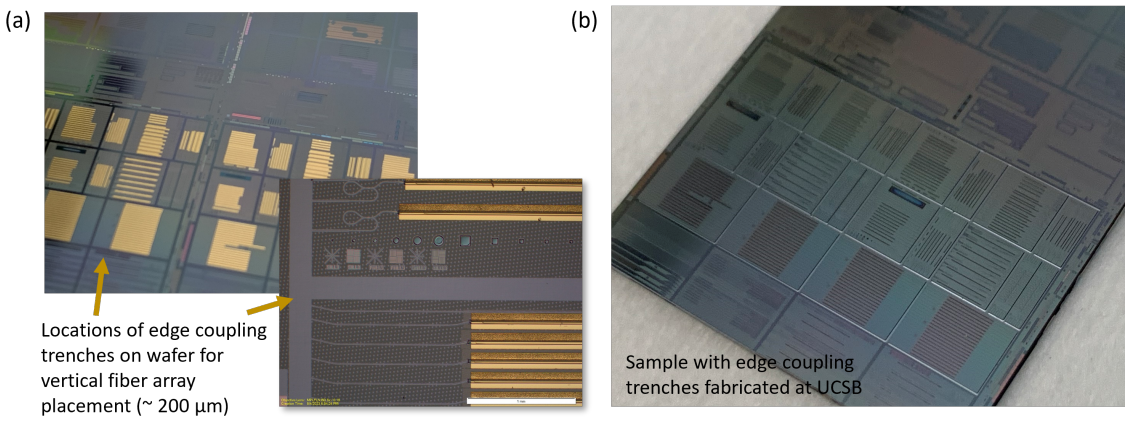

Figure 6.34: Deep Si etch trench design for on-chip vertical fiber array edge coupling. (a) Keep-out streets on chips for edge coupling trenches, (b) photograph of a die after edge coupling trench fabrication at UCSB.

Figure 6.34 (a) shows a perspective view and a top view of the "dicing trench" space on the chip in our platform. An extra-deep Si etch step will be taken to bring down over 70 µm at these 200 µm wide streets to create the trench for fiber coupling. Figure 6.34 (b) shows a photograph of a sample with an edge-coupling trench etched at UCSB. The dicing trench etch step is available at 300 mm scale in the photonic foundry and is being incorporated into the full device build III-V run-path.

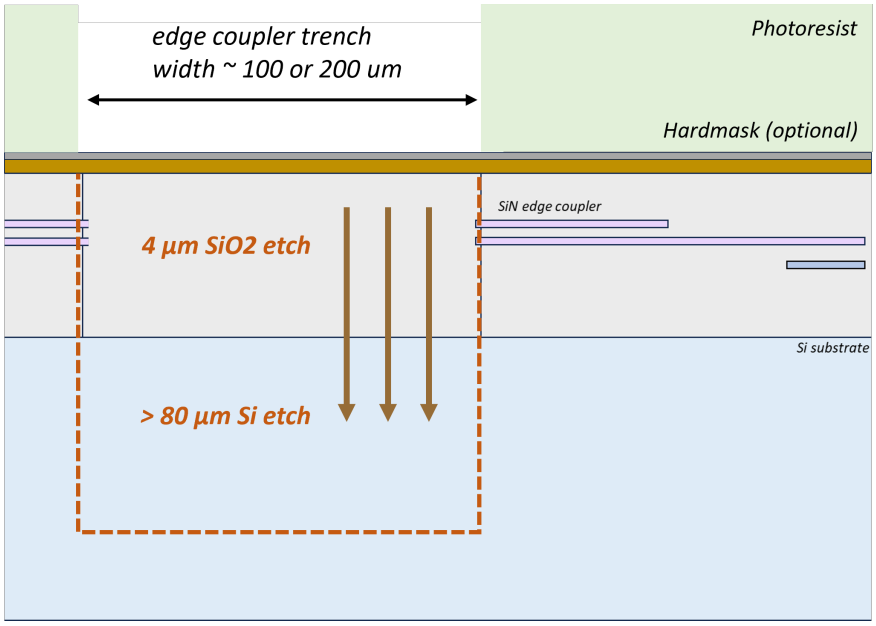

Figure 6.35: Illustration of the cross-section of the platform at edge coupling street, where an oxide etch followed by a deep Si etch process with either a thick photoresist mask or an additional hardmask is developed as a post-laser fabrication process at UCSB Nanofab.

We also develop the deep edge coupling trench etch process at UCSB Nanofab for vertical fiber array coupling after the in-pocket laser fabrication process. Figure 6.35 illustrates the two-step etches containing a SiO_2 etch and a deep Si etch. It can be processed with one thick photoresist mask (using a thick photoresist such as SPR 7.0), or with an additional prior hardmask deposition composed of Al_2O_3 and SiO_2 patterned with photoresist mask for even higher selectivity during the deep Si etch. Details of the fabrication process is included in the Appendix. Figure 6.36 shows the perspective view and cross-section view SEMs of the sample after the edge coupling trench etch and subsequent photoresist cleaning. Deep vertical trenches with 200 µm width and over 80 µm depth are fabricated with very vertical sidewalls.

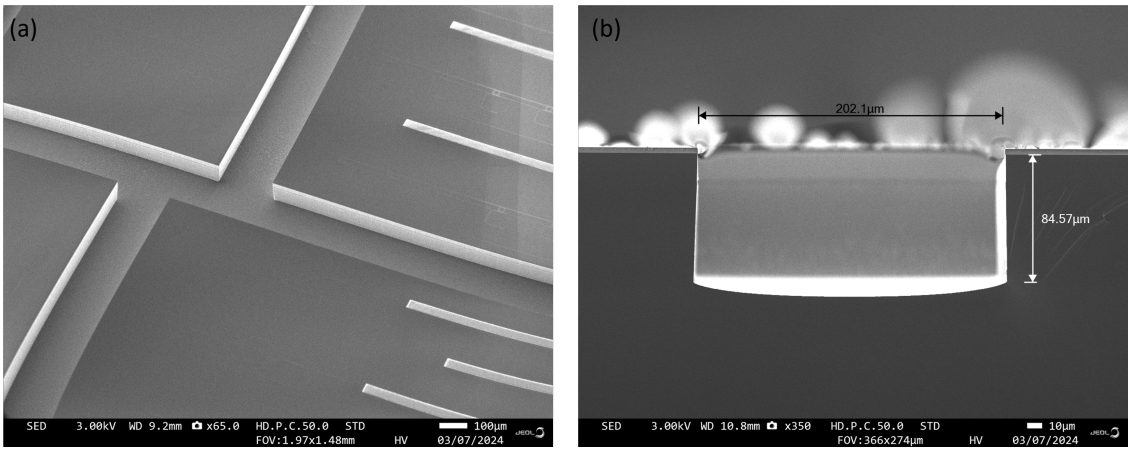

Figure 6.36: Perspective view (a) and cross-section view (b) SEMs of the sample after edge coupling trench etch and subsequent photoresist cleaning. Trenches shown here have 200 µm width and over 80 µm depth for placement of designed trench probe fiber array with vertical edge coupling for potential wafer-scale automated testing.

With the etched trench and wafer-scale coupling and testing using vertical fiber array on the automated wafer prober, there should be reduced uncertainty from the facet polishing step and better and more consistent edge coupling efficiency, which will also aid the ongoing research on quantitative characterizations of on-chip laser to SiN waveguide coupling.

In conclusion, with the development of automated wafer-prober at 300 mm scale, on-chip DFT components designed for wafer-scale fabrication process debugging and device performance screening, as well as the new technology made possible for robust low-loss wafer-scale measurement with edge-coupling to fiber or fiber arrays, a shorter development cycle and quicker turn around time for the fully monolithic integrated Si photonics platform with on-chip lasers can be made possible in the very near future.

6.7 Comments on transferring to 300 mm

The thorough development of a CMOS foundry-compatible III-V laser process presents significant challenges, yet the challenges are not insurmountable. Here are our comments on a few examples of concerns regarding the process transfer:

(1) Tool availability and process control strategies. The tools at an established foundry are different from what is used here at a university research clean room, and a few key tactics in process control may not be readily available in the same manner, such as the *in-situ* laser monitoring for the precise etch stop defining mesa and exposing top n-contact surface. This can be addressed by a case-by-case development with close collaboration between foundry engineers and photonic designers and innovative processing engineers. Usually, an alternative solution can be possible, such as etching end-point detection with optical emission spectroscopy, where the light spectra emitted by a plasma during an etch process is analyzed and a change of exposed area layer composition will be detected as a change in the spectra.

(2) Chemistry availability at a specific foundry. Similar to the case for tool availability, the given working process developed from a university research environment may not be readily replicatable in a foundry. Again using dry-etch as an example, certain combination of etching gas, available chamber temperature and pressure settings are not possible. However, most of the processes presented here in the ridge waveguide laser fabrication are not exclusively unique solutions for the given purpose. The recipe we present here for etching GaAs/AlGaAs uses Cl_2/ N_2, but there are also alternatives such as $Cl_2/BCl_3/Ar$, or BCl_3/ N_2, etc. [15, 16, 17]. Admittedly, reassessing the recipe and conducting process development to validate it for the speciic material system and intended application is necessary, but many exsiting processes operate on similar principles, and extensive research has provided substantial acacdemic resources on the underlying mechanisms. Our

efforts on transferring the Cl_2/ N_2 recipe to the new tool in our clean room in developing the facet etch in Chapter 5 may serve as a simplified example.

(2) Material compatibility. The contact metal alloys utilized in this study (Pd/Ti/Pd/Au for p-contact on GaAs and Pd/Ge/Au for n-contact on GaAs) are not compatible with a CMOS foundry. However, there has been lots of research on CMOS-compatible contacts to III-V material systems. For example, Si-fab compatible Pd/Ge contact to n-InP and Ti/W/Al contact to p-InGaAs was developed in 2012 [18]. There is also demonstrations of Ti/TiN/Al metal contacts on p-GaAs and n-InGaAs, though the extended thermal annealing applied in the process may be a concern that needs to be separately addressed [19].

(3) Wet-etching. Patterned wet-etch, or controlled wet-etch without an automated etch-stop layer is a commonly raised concern regarding making complicated structures in a large scale. For the limitation of trained personnel and the risk for handling large wafers, it is usually believed impossible to perform a wet-etch like that presented in Chapter 5. However, the anisotropic nature of wet-etch is not a show-stopper for precise controlling - for the record, there is always risk of over-etching in dry-etch as well, it is only a matter of control. The key is to understand the factors (etch rate, layer thickness, window dimension, and safety clearance, etc.) and limit the uncontrollable variations within an acceptable zone. Wafer-scale variations can also be addressed with innovative solutions in the mechanical design of handling system and chamber environment.

(4) Process uniformity across wafer and overall yield. There have been concerns that the loading effect and wafer-scale uniformity can be a serious issue for 300 mm wafer. With the experiences in the university cleanroom, it could be seen that some of the variations in etch rate or etching quality comes from the frequent switching between different material systems for various purposes in the shared facilities, and the difference in diced-out experimental sample sizes. While it's true that current Si photonics production lines

may share resources with other processes, leading to additional uncertainties in process control [20], we anticipate that the production quality and yield of large-scale wafers will ultimately improve in a foundry setting. This improvement will stem from the standardized tool operations that necessitate fewer changes. Additionally, certain technologies available at the production scale, such as oxide fill and CMP planarization steps, will aid in uniformity control. However, challenges specific to larger wafer sizes, such as wafer bowing and non-uniform thermal distribution, will require dedicated efforts to seek for innovative solutions.

Despite the specific technical concerns, the fast-paced development in the Si photonics foundry and its ecosystem shows promising capability of large-scale productions, regardless of the integration scheme for incorporating other functional materials. The improvements of measurement technology we reviewed in the previous section have shown the collective effort for accelerating the development cycle from both industrial players and academic researchers. A panel discussion under the title "Towards Standardized PIC Testing: Challenges & Roadmaps" was held for the first time at OFC 2023, reflecting the transitioning phase of establishing standards for various aspects in the chain of production, covering design, modeling, simulation, manufacturing, packaging, and testing. Additional perspectives and technological reviews on the industrial ecosystem of foundries for Si photonics can be found in [20, 21, 22, 23, 24, 25, 26].

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Chapter 7

Summary and outlook

7.1 Summary and outlook

We have demonstrated the first quantum-dot (QD) lasers heteroepitaxially integrated on Si at a 300 mm scale. Fabrication of lasers were conducted with smaller pieces within the capability of the university research cleanroom, and the detailed experimental procedures and processing improvement are presented aiming for the future technology transfer to a 300 mm scale III-V processing facility for full monolithic integration and co-processing on Si. We have shown the merits of quantum dots' tolerance to crystalline defects as an efficient gain material, and demonstrated the repeatability of MBE growth conditions irrespective of wafer sizes.

We have preliminarily established an on-chip monolithic integration platform of quantum dot for Si photonics through heteroepitaxy. First demonstration of in-pocket QD lasers with cleaved facet was a result of careful development of material growth and device fabrication with the thick oxide patterned template. The coupling comes later with more discrete steps, from a demonstration of concept with FIB-facet laser, to the development of on-chip etched facet laser, to the demonstration of on-chip butt-coupling to foundry-

processed SiN waveguides with etched facet lasers, with lots of process development and learning involved.

Some of process development presented in Chapter 3-5 can be standalone results for broader use in other contexts, such as the metal-coating as on-chip vertical reflector at etched facet, the self-aligned PMGI masked polycrystal removal wet etch, or the wet-and-dry combined hardmask facet etch. The meticulous details and experimental procedures are presented here with such intention in mind.

The discussions on results and future challenges were presented as a comprehensive review in Chapter 6, including further investigations regarding many factors affecting the performance and yield, such as template uniformity or in-pocket QD growth mechanism. Related studies or proposed future work to address the issues are presented. Coupling efficiency is a major concern for making external cavity lasers or highly functional PICs, and future research should prioritize addressing this aspect.

In particular, it could be hard to achieve lower than 3 - 5 dB loss with the current growth scheme, as re-engineering to reduce scattering and reflection at pocket-end is inevitable with the sidewall polycrystal and faceting with the presence of aluminum-containing cladding layers. In my opinion, the hybrid approach of MOCVD fill and MBE regrowth may still be highly feasible, given the supreme selective GaAs-fill result demonstrated and our initial attempts showing a promising MBE regrowth QD PL quality in the etched MOCVD in-pocket GaAs-fill template. Transitional interface at the MBE and MOCVD material boundary remains to be further investigated. Close collaboration among different epitaxial engineers and device engineers is at core for advancing in this aspect. Another immediate possible demonstration is the offset QD platform, with in-pocket QD lasers coupled to gratings or waveguides in the in-pocket GaAs waveguide, like shown in Figure 6.21 in Chapter 6. This can be achieved with the current template but a revisit of the epitaxial layers and more precised fabrication at the in-pocket geometry.

The new generation of integration design with wider pocket width finally coming to production in this project may render the task more manageable than the cases of 15 µm and 20 µm widths before. Alternatively, expanding the narrow, long pocket geometry to a wide open box, in dimensions of 3 mm × 3 mm, for example, can provide a pseudo-planar heteroepitaxy environment that would lift many constraints in growth and fabrication.

7.2 Afterword

We set out by declaring the goal of this work as "to establish an on-chip light source for 300-mm scale Si photonics with monolithic integration, especially for applications in data communications".

In my assessment, we have come closer to this goal by the conclusion of this thesis. It is still some distance from being fully established, but it is at least shown as feasible in many ways, and the pivotal challenges have come more clear through the experiment and learning process.

The topic itself is sort of a dilemma, as to do something at a large scale, especially if it is hardware, would naturally takes longer time, larger cycle, more investment and more personnel to accomplish, and that may have gone beyond the scope of a project for a doctoral degree. There have been many cases where I see what the problem is, and wish I could switch position and spend time where it occurs to find out the answers myself as soon as possible. Several new research proposals have also emerged as the project progressed, such as the hybrid regrowth approach for reduction of coupling efficiency and ideas of alternative innovative device engineering. There have been times when I irrationally feel that I want to stay at this project for as long as possible and try hard to not graduate so I can work more things out, or the urge to do another PhD in Materials Science and also get ten years of professional working experience in a foundry. I guess I

wanted to be "everything, everywhere, all at once". Nevertheless, I feel safe to state that I have tried my best to show what is currently achievable and what can be envisioned. This thesis has turned out to be much longer than I anticipated, and I hope that it proves to be somehow useful.

I have quoted this wise word from John Bowers in one of the opening slides of my defense - "Silicon Photonics is a combination of two of the most important inventions of the 20th century-the silicon integrated circuit and the semiconductor laser." [1] It is definitely not an easy combination to make, but the innovation is happening fast. I imagine the aforementioned goal will be well achieved in the near future, one way or another, and it has been and will always be exciting.

[1] The quote is also displayed at Intel's website, under "What is Silicon Photonics".

Appendix A

Process followers

A.1 Process for making monolithically integrated lasers

A.1.1 Fabrication process

(1) Sample preparation and polycrystal removal

Careful inspection of sample surface with microscope and/or SEM is highly recommended. Cross-section SEM or FIB-SEM is also recommended for verification of layer thickness. For samples without CMP, perform polycrystal removal referring to procedures introduced in Chapter 4. For samples that has gone through CMP, perform a BHF-based wet-etch to clean off remaining CMP oxide in pocket ends, timed with calibration to estimated remaining CMP oxide thickness.

(2) P-contact deposition and passivation

Lithography - PR: spin coat PMGI SF15 with recipe #5 (3000 RPM for 30s), bake at 185 - 190 °C for 2 min, cool down and spin coat SPR 3.0 with recipe #5, bake at 110 - 115 °C for 1 min 50 s, clean off edge beads with razor blade;

Lithography - loading and programming: Use mask GDS of p-contact layer. Load sample in MLA, align (preferably with FN markers, 8 sets, 2 at each corners with two rounds one follow another), exposure and focus offset: 400/-3.

Lithography - development: wait for about 30 mins before development; develop in AZ726 for 63s - 65s and inspect under microscope; expose under DUV flood exposure with rotation for 3 min; develop in 101A for 65 s. Inspect to check if sample is ready. Note that there is no post-development baking for bi-layer lift-off process to avoid thick PMGI layers cracking at sample edges and leave unwanted metal stripes and/or pattern distortion.

Pre-loading preparation: PEII 100 W for 4 min, HCl:H_2O 1:3 by volume solution for 1 min, rinse and load in deposition chamber immediately afterwards, preferably within 10 mins.

In cases of unforseable reasons causing the deposition could not start in time, it is advised to keep the sample in dry box, and repeat the HCl solution 1 min dip before the next attempt of loading.

Deposition: Use E-beam #4 with normal rotation and load samples to 4-inch carrier plates; use Kapton tape and aluminum foil to cover large areas of blank space on sample to make lift-off easier; deposit Pd/Ti/Pd/Au 100/400/400/5000 Åwith rotation on, pay attention to deposition rate and source sweeping pattern.

Lift-off: Remove sample from carrier and clean off all tapes; soak sample in Acetone until visible lifting-off happening, which usually takes 10 - 20 mins; use disposable pipette with a cut on tip (larger opening) to pump air in solution to accelerate peel-off, if needed. After lift-off completes, rinse sample with Isopropanol and dry-off. Use DUV flood exposure for 5 mins for complete exposure, and then react in AZ726 for about 2 mins for complete PR clean-off. The sample surface should be clean now, if not, further inspection and cleaning will be needed.

Passivation: After lift-off and sample cleaning, passivate surface with about 500 nm SiO_2 using PECVD. It usually takes about 17 mins in PECVD#2. Load two Si dummy wafers for thickness monitoring, which we will refer to as dummy Si-A and dummy Si-B.

In parallel, it is important to know the BHF etch rate of this specific PECVD oxide (it can be different from different tool, and can change from time to time). Deposit another single-use dummy and calibrate the etch rate with BHF, and have it possibly close to the date where the passivation layer is done. This is dummy Si-C.

(3) Facet etch hard mask

Lithography No. 1 - PR: Spin-coat SPR 3.0 with recipe #5 (following HMDS, 20 s wait and recipe #5) . Bake at 110 - 115 °C for 1 min 50 s. Inspect and clean off edge beads if there's any.

Lithography No. 1 - loading and programming: Use mask GDS of wet-etch window layer. Load sample in MLA, align, exposure and focus offset 400/-3 for small pieces. When used bigger piece (size 52 mm x 36 mm), 300/-3 seems to work well too, but the smaller pieces tend to be underexposed for 300/-3.

Lithography - development: Wait 10 - 15 min (maybe not necessary), then perform post-exposure bake at 110 - 115 °C for 1 min 50 s. Development in AZ726 developer for 60 s. Inspect under microscope. The wet etch window should show up, when adjusting the focal plane of the microscope, it should turn from clear edges to patterns of the non-uniformity of oxide surface as the focal plane goes from top-surface of PR to top-surface of oxide hardmask. Ensure the wet-etch window is open, and inside the window it should appear pink/purple-like color from the oxide. Save image and remember how it appears, as it will be good reference for after the wet-etch to check the difference and ensure the reaction is thorough. Perform another 4 min of PEII ashing (100 W) to clear off any possible remaining thin PR. The wet etch boundary seen after later PR cleaning

will be more gradual, vague and not sharply visible if the PEII step is missed.

Oxide wet etch: First, use dummy Si - C to calibrate the etch rate. Etch in BHF for 1 min, and check the thickness before and after to estimate the etch rate. I have seen etch rate of 400 nm/min, 399 nm/min, and 365 nm/min for three separate experiments, the third time performed a few months later than the first two. This is why it is very important to know the etch rate from the specific film that was deposited, so as avoid incomplete reaction or excessive overetch.

With the etch rate, calculate etch time using thickness of dummy A (or B), and add 10 s to ensure complete reaction taking into account potential thickness non-uniformity across sample. Avoid adding too much time to avoid unnecessary undercut. Rinse thoroughly. Inspect with microscope, the pink color in the window should be gone. A very slight undercut at the edge of window can be visible if inspecting very carefully, which is a great sign to assure complete reaction. In an ideal case the undercut should be about 500 nm (same as the oxide thickness), but with the extra 10 s it can be a little larger than that, but shouldn't be more than 1 µm. The wet etch window size affects how close the laser facet can be pushed towards the waveguides.

After ensure the reaction is finished, clean off PR mask using acetone and isopropanel. Take a look under the microscope again to see the actual pattern left on oxide. The window edges can be a bit wiggly from the ragged surface near pocket ensd.

Lithography No. 2 - PR: Spin-coat SPR 3.0 with recipe #5 (following HMDS, 20 s wait and recipe #5) . Bake at 110 - 115 °C for 1 min 50 s. Inspect and clean off edge beads if there's any.

Lithography No. 2 - loading and programming: Use mask GDS of the facet etch layer. Load sample in MLA, align, exposure and focus offset 400/-3 for small pieces. When used bigger piece (size 52 mm x 36 mm), 300/-3 seems to work well too, but the smaller pieces tend to be underexposed for 300/-3.

Lithography - development: Wait about 30 min, then perform post-exposure bake at 110 - 115 °C for 1 min 50 s. Development in AZ726 developer for 60 s. Inspect under microscope. The pattern should be clear and sharp. Confirm that the boolean of the mask is correct.

Oxide dry etch: Use ICP #2 recipe #101 SiOxVert etch (or other vertical SiO_2 dry etch recipe with other etchers). Calculate etch time using thickness of dummy Si-B and etch rate (estimatedly 250 nm/min for etching PECVD #2 SiO_2 using ICP #2 recipe #101) with an extra 20 % to ensure reaction complete (Etch time = thickness/etch rate *1.2). Use dummy Si-B as the monitor piece and co-load with sample to see the etch trace and ensure reaction is complete. An example of total etch time: with dummy Si B thickness of 491 nm, etch for 2 min 21s, where the trace shows reaction complete around 2 min 11s.

Sample cleaning: Use acetone and isopropanel to rinse off sample. Make sure the oil in the backside is also cleaned. Inspect with microscope to check remaining PR residues, and usually some cracks or scums would be visible, showing thin layer of remaining PR. Use YES Plasma with recipe STD-N2-O2-100C-3kW-2min to clean, and inspect again to check for differences in the area that is previously seen as dirty. If sample is not clean, try another 2 min of YES Plasma clean and check again. Usually it should be clean with just one cycle. Avoid unnecessary cleaning.

(4) Facet etch and passivation

Prior to the step, it is recommended to have sufficient tool booking time for the ICP etcher and a PECVD deposition tool connected to ensure smooth ongoing of etching and passivation.

Facet etch: Use Oxford ICP Etcher (PlasmaPro 100 Cobra) (will refer to as Cobra). Run a SF_6 then O_2 cleaning recipe if necessary, with the Si cleaning wafer (usually

available in tool). Then set tool temperature to etch recipe temperature (30 °C) with the cleaning wafer. Check GaAs etch recipe ("30C-V1-AMUAdjusted") is correct, and run a seasoning etch using the GaAs etch recipe with Si carrier wafer (usually use my own to avoid contamination and replace if getting too thin) for 6 min. Recommend to load a piece of dummy epitaxial wafer to check etch trace and laser monitor working properly at this seasoning etch. Then run the actual facet etch with samples, co-load with dummy-Si A to monitor remaining hardmask thickness. The actual facet etch time is 8 mins for the results shown in Chapter 5. The oxide is etched down about 400 nm.

In the second batch (the partial-selectively grown MBE epi on Lincoln), the facet etch time is shortened to 7 mins due to the concern of hardmask etch-through. The oxide is etched down about ? nm.

Also, the issue of sample sliding during loading raises up a few months later than the recipe development phase, which could potentially cause sample loss and break in tool. So it is changed to apply minimum oil (only at four corners) at the back of sample to avoid sliding.

After the etch, splash water on sample immediately after taking it out of the chamber, and immerse in water in beaker, use the saftey transfer box to transfer the beaker to wet benches. Rinse thoroughly with acetone, isopropanel and water. Dry sample thoroughly with N_2 gun.

Passivation: Use PECVD #2 to deposit 10 - 12 mins of oxide. Use PEII 100W for 30s before loading into PECVD chamber. Co-load dummy-Si A since it will be a record of accumulated mesa-top oxide thickness. Inspect sample after deposition finishes.

(5) Mesa etch hardmask, mesa etch and passivation

Lithography - PR: Spin-coat SPR 3.0 with recipe #5 (following HMDS, 20 s wait and recipe #5) . Bake at 110 - 115 °C for 1 min 50 s. Inspect and clean off edge beads

if there's any.

Lithography - loading and programming: Use mask GDS of mesa etch layer. Measure the deposited p-contact layer width, adjust design of mesa width if needed. Load sample in MLA, align, exposure and focus offset 300/-3 for small pieces. Note that the exposure number is reduced here for better results. Attempt with 400/-3 showed expansion of the pattern that makes the mesa narrower than design, and rework with 300/-3 solved the problem (along with the 30 mins wait before post-bake).

Lithography - development: Wait at least 30 min. Perform post-exposure bake at 110 - 115 °C for 1 min 50 s. Development in AZ726 developer for 60 s. Inspect under microscope. The pattern should be clear and sharp. Confirm that the boolean of the mask is correct.

Oxide dry etch: Use ICP #2 recipe #104 Nanoetch. Note that #104 is preferred over #101 here since it seems to produce better verticality in the mesa etch. Use half of dummy A (the other half will be kept for later oxide deposition accumulation and will be used for p-via etch monitor later) and use laser monitor to stop the etch about 15 s after the trace turns flat. Estimate of etch time can be done by dummy-A thickness / (80 nm/min) x 120 %, but the actual stopping time should be shorter than the estimated number. It is good to avoid too much overetch here to avoid etching down III-V unintentionally and potentially risk n-contact overetch.

Post dry-etch sample cleaning: Use acetone and isopropanel to rinse off sample. Make sure the oil in the backside is also cleaned. Inspect with microscope to check remaining PR residues, and usually some cracks or scums would be visible, showing thin layer of remaining PR. Use YES Plasma with recipe STD-N2-O2-100C-3kW-2min to clean, and inspect again to check for differences in the area that is previously seen as dirty. If sample is not clean, try another 2 min of YES Plasma clean and check again. Usually it should be clean with just one cycle. Avoid unnecessary cleaning.

Prior to the next step, it is recommended to have sufficient tool booking time for the ICP etcher and a PECVD deposition tool connected to ensure smooth ongoing of etching and passivation.

Mesa etch: The process here uses ICP #2, but a similar process can be done in the Oxford ICP Cobra etcher. Use recipe #113 with the settings listed in Chapter 3. Co-load a small piece of blanket epitaxial wafer with the same stack ("IQE 300 blanket") at the laser monitor spot, and co-load the remaining half of dummy Si-A to monitor oxide overetch. For all the loaded pieces, use oil in the back for better heat transfer and etching result (insufficient oil could result in grassing with certain recipes). Quickly anneal at 80 °C hot plate for a few seconds. Note that oil should cover all backside of sample, but not exceeding the edge and showing out. Cool down carrier wafer before loading. Monitor etch with trace and stop right before n-contact layer. For details, also refer to the fabrication development section in Chapter 4.

After the etch, splash water on sample immediately after taking it out of the chamber, and immerse in water in beaker, use the saftey transfer box to transfer the beaker to wet benches. Rinse thoroughly with acetone, isopropanel and water. Dry sample thoroughly with N_2 gun.

First passivation: Use PECVD #2 to deposit 10 mins of oxide. Use PEII 100W for 30s before loading into PECVD chamber. Co-load the remaining dummy-Si A since it will be a record of accumulated mesa-top oxide thickness, also co-load the dummy-Si B (should be etched off with no oxide now) to keep a record for the n-via etch. Inspect sample after deposition finishes.

(6) Extra passivation fill

Unaxis PECVD SiO_2 fill: Use recipe "SiO2 FILL 250C" to add a second passivation step for better conformal coverage of SiO_2. Run "SiO2 Season 250C" for 120 s, then

run "SiO2 FILL 250C" with the sample, co-loaded with both dummy A and dummy B. Run a PDC for 1200 s after finish. Note that there's loading effect in this step (different pieces may have different deposition rate). I recommend doing the full three steps with another dummy Si piece first, just to ensure chamber working properly, deposition rate looks normal (540s should add about 600 nm - 650 nm oxide), the ignition works and there is no large pieces of flake falling from chamber (if that happens, the tool needs a wet clean).

The recipe for "SiO2 FILL 250C" and related process development details are available at Table 4.4.

It is possible to replace this step by an ALD layer (with Al_2O_3, for example) **prior** to the PECVD #2 oxide to ensure a conformal passivation coverage. The down side would be it may add more uncertainty for the dry etch time in the n-via and p-via, but should be okay with the laser monitor and dummy pieces. I have not tried that due to tool availability at given chances, but recommend to give it a try.

It is also possible to reduce the Unaxis PECVD fill time, but 540 s was the first conclusion I had from multiple depositions and cross-section SEMs to find a good time for sidewall coverage (although, again, loading effect may make things different). If the deposition time is too short it may end up etch away more sidewall oxide than depositing, due to the high bias power. The same deposition time was then used in all my later in-pocket fabrication runs and it has been giving good passivation coverage, thus stays unchanged so far.

(7) N-via etch

Lithography - PR: Spin-coat SPR 3.0 with recipe #5 (following HMDS, 20 s wait and recipe #5) . Bake at 110 - 115 °C for 1 min 50 s. Inspect and clean off edge beads if there's any.

Lithography - loading and programming: Use mask GDS of n-via layer. Load sample in MLA, align, exposure and focus offset 400/-3.

Lithography - development: Wait at least 30 min. Perform post-exposure bake at 110 - 115 °C for 1 min 50 s. Development in AZ726 developer for 60 s. Inspect under microscope. The pattern should be clear and sharp. Since it is a narrow, long pattern, underexpose would look less rectangular at the end, and look a bit rounded up and sectionized (like a link of sausage). If that comes up, maybe the dose needs to be adjusted for higher.

Oxide dry etch: Use ICP #2 recipe #101 SiOxVert. Estimate of etch time can be done by dummy-B thickness / (250 nm/min) x 120 %, but the actual stopping time should still be shorter than the estimated number. Co-load dummy-B and use the in-situ laser monitor to watch etching progress. I will usually stop about 20 s after the trace turns flat. A little bit of overetch is considered fine or even encouraged here to ensure the via open, and clear off if there is a thin un-etched layer above n-doped GaAs contact layer from the precautious mesa etch.

Post dry-etch sample cleaning: Use acetone and isopropanel to rinse off sample. Make sure the oil in the backside is also cleaned. Inspect with microscope to check remaining PR residues, and usually some cracks or scums would be visible, showing thin layer of remaining PR. Use YES Plasma with recipe STD-N2-O2-100C-3kW-2min to clean, and inspect again to check for differences in the area that is previously seen as dirty. If sample is not clean, try another 2 min of YES Plasma clean and check again. Usually it should be clean with about two cycles in this step.

(8) N-contact deposition and RTA

Lithography - PR: spin coat PMGI SF15 with recipe #5 (3000 RPM for 30s), bake at 185 - 190 °C for 2 min, cool down and spin coat SPR 3.0 with recipe #5, bake at 110

- 115 °C for 1 min 50 s, clean off edge beads with razor blade.

Lithography - loading and programming: Use mask GDS of n-contact layer. Load sample in MLA, align, exposure and focus offset: 400/-3.

Lithography - development: Wait for about 30 mins before development; develop in AZ726 for about 62s and inspect under microscope; expose under DUV flood exposure with rotation for 3 min; develop in 101A for 65 s. Inspect to check if sample is ready. For more details, refer to "tips for better metal deposition". Note that there is no post-development baking for bi-layer lift-off process to avoid thick PMGI layers cracking at sample edges and leave unwanted metal stripes and/or pattern distortion.

Pre-loading preparation: PEII 100 W for 4 min, HCl:H_2O 1:3 by volume solution for 1 min, rinse and load in deposition chamber immediately afterwards, preferably within 10 mins.

In cases of unforeseeable reasons causing the deposition could not start in time, it is advised to keep the sample in dry box, and repeat the HCl solution 1 min dip before the next attempt of loading.

Deposition: Use E-beam #4 with normal rotation and load samples to 4-inch carrier plates; use Kapton tape and aluminum foil to cover large areas of blank space on sample to make lift-off easier; deposit Pd/Ge/Au 400/1600/5000 Åwith rotation on, pay attention to deposition rate and source sweeping pattern.

Lift-off: Remove sample from carrier and clean off all tapes; soak sample in Acetone until visible lifting-off happening, which usually takes 10 - 20 mins; use disposable pipette with a cut on tip (larger opening) to pump air in solution to accelerate peel-off, if needed. Be careful not to oversoask sample to avoid potential liquid penetration and damage - don't leave it unattended in acetone for too long. After lift-off completes, rinse sample with Isopropanol and dry-off. Use DUV flood exposure for 5 mins for complete exposure, and then react in AZ726 for about 2 mins for complete PR clean-off. The sample surface

should be clean now, if not, further inspection and cleaning will be needed. Make sure sample is completely dried after the lift-off.

RTA: Load samples on the carrier wafer in the RTA tool (Rapid Thermal Processor (AET RX6)). Check thermometer wiring is proper on the tool and carrier wafer is not contaminated. Run recipe "350 °C 1 min FG"(FG: forming gas). Take samples out and inspect. The n-contact will usually show some surface roughness (bumpiness, or a bit dark from a low-zoom top view) under the microscope from the annealing.

(9) N-probe deposition

Lithography - PR: spin coat PMGI SF15 with recipe #5 (3000 RPM for 30s), bake at 185 - 190 °C for 2 min, cool down and spin coat SPR 3.0 with recipe #5, bake at 110 - 115 °C for 1 min 50 s, clean off edge beads with razor blade.

Lithography - loading and programming: Use mask GDS of n-probe layer. Load sample in MLA, align, exposure and focus offset: 400/-3.

Lithography - development: Wait for about 30 mins before development; develop in AZ726 for about 62s and inspect under microscope; expose under DUV flood exposure with rotation for 3 min; develop in 101A for 65 s. Inspect to check if sample is ready. Note that there is no post-development baking for bi-layer lift-off process to avoid thick PMGI layers cracking at sample edges and leave unwanted metal stripes and/or pattern distortion. For the probe deposition, it is usually okay to have a slightly larger undercut.

Pre-loading preparation: PEII 100 W for 4 min. This is to ensure the PMGI underlayer is completely cleared. If EB4 is not ready by the time of lithography, it is okay to leave the developed sample overnight in a dry box. I will recommend conducting 3 mins of PEII first, and add 1 min before loading.

In case of suspecting not enough undercut or not fully developed during the AZ726 development time, one may try to add 2-3 s of AZ726 quick dip immediately followed by

rigorous and thorough water rinse, and close inspection of undercut. Or, one may add 1 mins of PEII after AZ726 development, before DUV cycles. Always check closely to see possible undercut and/or rainbows. It is also better to check different area of sample, as the liquid reaction may be non-uniform with relation to how the sample sits in the holder. In that case, I would reduce the second PEII ashing to 3 mins.

Deposition: Use E-beam #4 with planetary rotation and load samples to 4-inch carrier plates; use Kapton tape and aluminum foil to cover large areas of blank space on sample to make lift-off easier. Ask for best advice of using a planetary rotation if not experienced. Deposit Ti/Au 220/15000 Åwith rotation on, pay attention to deposition rate and source sweeping pattern. It is advised to change the crystal before this deposition due to the heavy layer thickness (to avoid wasting gold from bad dep rate calibration). It is also advised to check remaining gold weight in group source box and replenish ahead if needed.

Lift-off: Remove sample from carrier and clean off all tapes; soak sample in Acetone until visible lifting-off happening, which should take 10 - 20 mins, but usually less for probe metal lift-off. Use disposable pipette with a cut on tip (larger opening) to pump air in solution to accelerate peel-off, if needed. Be careful not to oversoask sample to avoid potential liquid penetration and damage - don't leave it unattended in acetone for too long. After lift-off completes, rinse sample with Isopropanol and dry-off. Use DUV flood exposure for 5 mins for complete exposure, and then react in AZ726 for about 2 mins for complete PR clean-off. The sample surface should be clean now, if not, further inspection and cleaning will be needed. Make sure sample is completely dried after the lift-off.

No additional annealing should be needed at this stage.

(10) P-via etch

Lithography - PR: Spin-coat SPR 3.0 with recipe #5 (following HMDS, 20 s wait and recipe #5) . Bake at 110 - 115 °C for 1 min 50 s. Inspect and clean off edge beads if there's any.

Lithography - loading and programming: Use mask GDS of p-via layer. Load sample in MLA, align, exposure and focus offset 400/-3.

Lithography - development: Wait at least 30 min. Perform post-exposure bake at 110 - 115 °C for 1 min 50 s. Development in AZ726 developer for 60 s. Inspect under microscope. The pattern should be clear and sharp. Since it is a narrow, long pattern, underexpose would look less rectangular at the end, and look a bit rounded up and sectionized (like a link of sausage). If that comes up, maybe the dose needs to be adjusted for higher.

Oxide dry etch: Use ICP #2 recipe #101 SiOxVert. Estimate of etch time can be done by dummy-A thickness / (250 nm/min) x 120 %, but the actual stopping time should still be shorter than the estimated number. Co-load dummy-A and use the in-situ laser monitor to watch etching progress. I will usually stop about 20 s after the trace turns flat.

Post dry-etch sample cleaning: Use acetone and isopropanol to rinse off sample. Make sure the oil in the backside is also cleaned. Inspect with microscope to check remaining PR residues, and usually some cracks or scums would be visible, showing thin layer of remaining PR. This etch should produce more scums than previous ethces due to the higher total oxide thickness and longer etch time. Use YES Plasma with recipe STD-N2-O2-100C-3kW-2min to clean, and inspect again to check for differences in the area that is previously seen as dirty. If sample is not clean, try another 2 min of YES Plasma clean and check again. I usually need 2 - 3 cycles in this step. If some minor

scums are still visible after a few cycles, one can evaluate and decide to move on if their locations are not critical to the electrical pathway.

(11) P-probe metal deposition

Lithography - PR: spin coat PMGI SF15 with recipe #5 (3000 RPM for 30s), bake at 185 - 190 °C for 2 min, cool down and spin coat SPR 3.0 with recipe #5, bake at 110 - 115 °C for 1 min 50 s, clean off edge beads with razor blade.

Lithography - loading and programming: Use mask GDS of p-probe layer. Load sample in MLA, align, exposure and focus offset: 400/-3.

Lithography - development: Wait for about 30 mins before development; develop in AZ726 for about 62s and inspect under microscope; expose under DUV flood exposure with rotation for 3 min; develop in 101A for 65 s. Inspect to check if sample is ready. Note that there is no post-development baking for bi-layer lift-off process to avoid thick PMGI layers cracking at sample edges and leave unwanted metal stripes and/or pattern distortion. For the probe deposition, it is usually okay to have a slightly larger undercut.

Pre-loading preparation: PEII 100 W for 4 min. This is to ensure the PMGI underlayer is completely cleared. If EB4 is not ready by the time of lithography, it is okay to leave the developed sample overnight in a dry box. I will recommend conducting 3 mins of PEII first, and add 1 min before loading. (Additional notes are the same as N-probe deposition step)

Deposition: Use E-beam #4 with planetary rotation and load samples to 4-inch carrier plates; use Kapton tape and aluminum foil to cover large areas of blank space on sample to make lift-off easier. Ask for best advice of using a planetary rotation if not experienced. Deposit Ti/Au 220/15000 Åwith rotation on, pay attention to deposition rate and source sweeping pattern. It is advised to change the crystal before this deposition due to the heavy layer thickness (to avoid wasting gold from bad dep rate calibration). It

is also advised to check remaining gold weight in group source box and replenish ahead if needed.

Lift-off: Remove sample from carrier and clean off all tapes; soak sample in Acetone until visible lifting-off happening, which should take 10 - 20 mins, but usually less for probe metal lift-off. Use disposable pipette with a cut on tip (larger opening) to pump air in solution to accelerate peel-off, if needed. Be careful not to oversoask sample to avoid potential liquid penetration and damage - don't leave it unattended in acetone for too long. After lift-off completes, rinse sample with Isopropanol and dry-off. Use DUV flood exposure for 5 mins for complete exposure, and then react in AZ726 for about 2 mins for complete PR clean-off. The sample surface should be clean now, if not, further inspection and cleaning will be needed. Make sure sample is completely dried after the lift-off.

No additional annealing should be needed at this stage.

A.1.2 Tips on better metal contact

(1) Ensure the sample contact layer is intact. Knowing the contact layer thickness and doping level is correct. If it is the top layer of epi, it's recommended to start contact metal deposition as the first step without potential contamination on the the epi contact layer. If it's a layer exposed from dry etch, it's critical to ensure the via-oxide is completely cleared, also ensure enough thickness of contact layer is left with sufficient doping level at that depth. It's also recommended to start the contact metal layer without too much rework on that exposed contact surface.

(2) Ensure the PR is completely developed. Thin layer of left-over PR would cause either metal peel off or high resistance. The PEII step in our process followed is added for that purpose.

(3) Be quick at sample loading after acid reaction. If there's tool issue that ending up leaving the sample out for too long, it may be worth the time to take it out for another acid clean and pump down the chamber again.

(4) Inspect all the source material - don't skip this step. Check abundant material even if the previous user has logged a refill - there could be another user that came in-between and used and ran without logging. Check source quality, if suspicious look suggests possible contamination, ask staff for assistant. Check the correct source is in corresponding crucibles. Check Ge/Cr interchangeable crucible has the right source in there. Also, confirm shutter is working properly. Change to new crystal if thickness precision is critical or saving source material is important (e.g. probe metal), or if crystal looks significantly used.

(5) Confirm rotation is working properly. Be patient with tool pump down (try to book abundant tool time ahead and not rush a deposition). Lower chamber pressure likely provides better deposition quality. Check the e-beam sweep location on source during deposition, if drifted to edges of crucible, adjust location back to center of source. Check the dep-rate is generally stable and the power level appears in normal range.

(6) Treat metal deposition and lift-off with abundant patience and positive attitude. It is okay to go for other tasks in the cleanroom in parallel, but be sure to keep an eye on it.

A.2 Process for BCB gap-fill

The BCB gap-fill process is credit to Zachary Nelson, for the fruitful discussions on processing and handling tips of BCB and the recipes espeically for curing and etch-back. Please refer to his thesis for more details.

(1) Sample preparation: Solvent clean and O_2 plasma recommended for good

adhesion. For example, use PEII at 100 W for 2 min immediately before the next step.

(2) AP3000: Spin coat adhesion promoter AP3000 at 2000 rpm for 40s with 400 rpm/s acceleration (recipe #3), then bake at 100 °C for 1min. (Comment: this leaves a thin 1 nm layer of organic bonding agents for the BCB to adhere to. Alternative procedures from different reference source: 3000 rpm spin-coat, then bake at 110 - 125 °C for 60 s, with 120 - 125 °C being the optimal range.)

(3) BCB spin-on: The BCB product used here is CYCLOTENE 3046-40. It should be taken out of the long-term storage freezer and warmed up to room temperature within an optimal time range prior to application (please refer to product specification for more information). Spin-on BCB with a spread-spin application. Customized spin-coating recipe: 500 rpm for 10s with 500 rpm/s acceleration, then 300 rpm for 30s with 600 rpm/s acceleration. Soft (pre) bake at 70 °C for 90 s. The temperature is taken from specification with an estimated thickness of 7 µm, so adjust when needed. (Comments on procedure from alternative source: start the spin at 500 rpm for 5 - 10 s with 100 rpm/s acceleration for the spread, and have the spinner immediately go into the spin step of 1000 rpm - 5000 rpm at the recommended time based on the spinner and with an acceleration of the chorsen rpm divided by 5 rpm/sec. Generally 3000 - 5000 rpm should be good, and it is better to do multiple thin coats than one thicker coat. Low temperature bake at 80 °C for 3 mins.)

(4) Exposure: Use DUV flood exposure to expose the entire BCB coating (as CYCLOTENE 3046-40 is a negative photoresist). Assume 10 mW/cm^2 power from the DUV flood exposure tool, the exposure time can be calculate using the desired power from spec (25 mJ/cm^2/µm) and the estimated thickness (7 µm). 25/10*7 = approximately 17.5 s. We expose the sample under DUV flood exposure iwth rotation for 30 s here to ensure thorough exposure. After exposure, post-bake at 70 °C for 60 s. (Suggestion from product specification: 60 - 90 °C, 60s.)

(5) BCB Curing: Use the BlueM Oven with the following temperature ramp cycle settings: Section #1: 2 hr ramp to 250 °C, and then 1 hr soak at 250 °C; Section #2: cool down (about 2 hr) to 20 °C, then 1 hr soak at 20 °C. In actual pracice, the sample was taken out after about 5 hr when the temperature is abotu 100 °C. (Reference suggestions from alternative source: (a) 1 hr ramp to 150 °C with a 15 mins soak, then a 1 hr ramp to 250 °C with a 1 hr soak, then ramp to room temperature for at least 2 hr; (b) 2 hours ramp to 250 °C with a 1 hr soak, then ramp to lower than 150 °C.)

(6) BCB etch back: Use ICP #2 for the BCB etch back. The recipe is as shown in Table A.1.

BCB Etching Recipe Using ICP #2 (Panasonic E640)				
Flow-rate (sccm) for CF_4	Flow-rate (sccm) for O_2	Pressure (Pa)	Bias (W)	ICP (W)
10	40	5	50	500

Table A.1: BCB etching recipe using ICP #2 (Panasonic E640).

Use in-situ laser monitor at a flat-area on sample for end-point monitoring. In our experiment, the etch time to end-point is about 9 min 38s, and the reaction is terminated at 9 min 48s with the additional 10s overetch. The majority of sample surface flat area should be clear of BCB after the etch-back.

A.3 Process for edge-coupling trench etch

(1) ALD hardmask deposition (optional): CH3-TMA+H2O-300C, 250 cycles, for approximately 30 nm Al_2O_3; then CH3-TDMAS-250W/O-300C, 50 cycles, for a thin SiO_2 coating to avoid undesired Al_2O_3 lift-off in developer.

(2) Adhesion promoter for photoresist: Use Surpass 4000 as adhesion promoter, apply on sample surface, rinse in DI water, blow dry with N_2 gun, then spin-dry on spinner

in the photoresist bench. Blue tape should be applied to the back-side of small sample prior to this step.

(3) SPR 7.0 spin-on: Use 3500 rpm for 30 s to spin-on SPR 7.0 (Recipe #6). Heat-up at 50 °C for 1 min, then bake at 115 °for 2 min.

(4) SPR 7.0 patterning: Use MLA for patterning. Suggested setting: 375 nm laser, exposure and focus offest: 2000/-20, "HAR" "Large". Wait for at least 30 min after exposure for sample rehydration. Heat-up at 55 °C for 1 min and post-bake at 115 °C for 90s. Develop in AZ726 for 2 min 30 s - 2 min 50 s with lots of agitation. Suggesting start with a shorter development time, e.g. 1 min 30 s, then alternate microscope inspection and additional development time until clear opening at patterned area. Use PEII 100 W for 4 min after development to further clean-off possible remaining photoresist in open area. Dektak shows around 6.6 µm height at this point.

(5) Oxide etch with Fluorine ICP: Etching recipe is shown in Table A.2

Oxide Etching Recipe Using Fluorine ICP (PlasmaTherm/SLR Fluorine ICP)				
Flow-rate (sccm) for CF_4	Flow-rate (sccm) for CHF_3	Pressure (mTorr)	Bias (W)	ICP (W)
35	10	3.8	50	800

Table A.2: Fast oxide etching recipe using Fluorine ICP (PlasmaTherm/SLR Fluorine ICP).

Use in-situ laser monitor to observe etching end-point. If ALD layers were applied to sample, they will be etched away prior to etching of the thick TEOS oxide, adding about 1 min of total etch time. For a sample with ALD layers and approximately 3.6 µm of TEOS oxide and, the laser monitor reached end-point around 12 min 28 s, and the reaction was terminated around 12 min 58 s with 30s of additional overetch. The selectively of this reaction using PR is estimated to be around 1:1.

(6) Deep Si Etch with DSEIII (PlasmaTherm/Deep Silicon Etcher): Use the standard deep Si etch recipe. Used 175 cycles for approximately 84 µm of etch depth

(measured by cross-section SEM after cleaving). Suggesting 250 cycles or more for a deeper etch depth.

After the deep Si etch, clean off photoresist with solvent, followed by Plasma Clean (YES EcoClean) with recipe "N2-O2-100C-3kW-3min". Usually one cycle is sufficient. Clean off the ALD hardmask if needed.