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Authors

Ataei, Samira
Stine, James E
Guthaus, Matthew R

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A 64 kb Differential Single-Port 12T SRAM Design With a Bit-Interleaving Scheme for Low-Voltage Operation in 32 nm SOI CMOS

Samira Ataei¹, James E. Stine¹ and Matthew R. Guthaus²

¹ Electrical and Computer Engineering Department, Oklahoma State University, Stillwater, OK 74078

² Department of Computer Engineering, University of California Santa Cruz, Santa Cruz, CA 95064
{ataei, james.stine}@okstate.edu, {mrg}@ucsc.edu

Abstract—In this paper, a novel differential single-port 12T SRAM bitcell is presented. This bitcell uses a read buffer to eliminate read disturbance, improves the read stability and achieves read static noise margin equal to its hold static noise margin. Using a column-based select signal this bitcell provides a half-select free feature, facilitating a bit-interleaving structure to reduce multi-bit soft errors by conventional error correcting code techniques. By boosting the wordline and select signal voltage, this bitcell can read and write with no error at 300 mV while data can be held down to 250 mV in standby mode. Bitline leakage suppression in 12T bitcell allows more bitcells per bitline for high density SRAMs and provides faster read operation. This paper also introduces OpenRAM, an open-source memory compiler, that provides a platform for the generation, characterization, and verification of fabricable memory designs across various technologies, sizes, and configurations. Using OpenRAM, a 64 kb 12T SRAM macro is designed in IBM 32 nm SOI CMOS technology that operates down to 0.3 V with 50 MHz operating frequency while it functions at 0.9 V with 2.2 GHz operating frequency, as well.

I. INTRODUCTION

Subthreshold operation enables suppressing dynamic power consumption and extends the battery life time of low power devices. SRAM scaling is one of the major bottlenecks for the reduction of supply voltage in current and future CMOS technology nodes. Although SRAM can achieve low power dissipation in the subthreshold region, it must face the ever-increasing process variation challenges for this region. With an increase in process variations for lower supply voltages, it is also becoming difficult to balance the read and write stability for a 6T SRAM bitcell due to its conflicting design requirement in read stability and writability [1]. Besides, in sub 100 nm technology nodes, subthreshold leakage power is a substantial portion of total power consumption and 6T bitcell doesn't have any mechanism to control this leakage. Moreover, during read operation subthreshold leakage leads to a read failure for 6T bitcell using small supply voltages. Although, techniques such as multi-threshold bitcells [2] and local-global bitlines [3] help to decrease leakage current of bitcells and long bitlines, these techniques degrades the performance or increase the area overhead.

Traditional 6T bitcell has a simple structure, but suffers from a half-select issue, as well. In half-select disturbance,

the bitcell in the unselected column is disturbed because the wordline is raised to turn on the access transistors for selected bitcells that need to be written to or read from [4]. Due to the half-select issue, most of the SRAM designs cannot be bit-interleaved and lose data through multi-bit soft errors.

Different configurations for SRAM bitcells have been proposed to improve the read stability, writability and subthreshold leakage control in low-voltage operation and solve the half select disturbance. 8T [5] (Figure 1(a)) eliminates charge sharing between the bitlines and internal storage nodes and improves the SRAM stability in low voltages. However, this bitcell suffers from a reduced swing on bitlines due to leakage as well as poor noise immunity due to its single-ended structure. In addition, an improvement of the access time is not expected since read operation is single-ended. Using a hierarchical bitline structure to speed up the read operation in this bitcell causes additional peripheral circuitries and hence more area overhead. [6] and [7] (Figure 1(b)) solve the 8T bitline-leakage problem during read by stacking three MOS transistors in bitcell read path. Again, although these bitcells improve the bitline leakage in low voltages, they have poor noise immunity due to their single-ended structure and read operation is slow due to full rail sensing. Besides both bitcells still have the half-select issue in write mode.

In [8] a differential-ended 10T bitcell (Figure 1(c)) makes use of the voltage difference between its bitline (BL) pair during a read operation to make this bitcell a suitable candidate for high-speed applications. This cell uses decoupled read port to improve the read stability and has two wordlines that helps to control the half-select issue and utilizes a bit-interleaving structure. To control the off-state leakage, an extra V_{GND} line for the read stack is routed horizontally and driven high for unselected rows. The drawback of this technique is the area overhead to route V_{GND} signal horizontally on the memory cell's pitch. Besides, the V_{GND} driver makes the read operation slower and increases the dynamic energy consumption (pull-down path contains extra NMOS device of V_{GND} driver). Without V_{GND} , this bitcell cannot be utilized on long bitline SRAMs because of its poor mechanism to control the leakage in read mode.

A 12T bitcell [9], as shown in Figure 1(d), employs a cross

Fig. 1. (a) Single-ended 8T [5], (b) Single-ended 10T [7], (c) Differential 10T [8], (d) Differential 12T [9] and (e) Quad-port 12T [10] bitcells.

point write structure with a data-aware, column-based write wordline to eliminate the half-select disturbance issue which can be used in bit-interleaving structures. However, this bitcell cannot be used in long bitlines due to bitline leakage current in read mode that leads to a read failure for small supply voltages. Another 12T bitcell [10], as shown in Figure 1(e), uses two differential ports for write and two single-ended ports for its read operation to be read and written simultaneously. Again, a single-ended decoupled read port improves read stability, but suffers from an increase in access time and reduction in noise immunity. This cell does not control the half-select problem and it is not suitable for bit-interleaving structures. Besides, this bitcell does not have a leakage control mechanism and cannot be used in high density SRAMs with long bitlines. In addition, due to its multiple port structure, it requires extra circuitry to be controlled that potentially leads to an increase in power and as well as a larger area penalty.

To overcome the limitations on SRAM bitcell in low-voltage and low-power operations, a novel 12T bitcell is proposed in this paper with the following features:

- 1) This bitcell provides greater improvements in the static read and write noise margins by decoupling the bitline from storage node during read and boosting the gate voltage of access transistors during write mode. Hence, it can withstand the ever increasing process variations in scaled technology nodes.
- 2) The proposed bitcell has a fully differential structure and layout, therefore, it shows better noise and mismatch immunity compared to single-ended schemes.
- 3) This bitcell utilizes differential sensing in read mode which leads to faster operations and less access time.
- 4) This cell has a row-based wordline and a column-based control signal, therefore, it eliminates the half-select issue by isolating the half-selected cells from bitlines.
- 5) This 12T bitcell can be implemented in a bit-interleaving structure and allows to solve the multi-bit soft errors by conventional error correction code (ECC) techniques.

- 6) This bitcell has a data independent leakage control ability which helps to reduce the bitline leakages in read and hold modes and provides a fast robust read operation in low voltages. Therefore, it is a suitable cell for arrays with long bitlines for high density SRAMs.

This paper also introduces OpenRAM: an open-source memory compiler as the vehicle for creating its layout [11]. Memory designs play a significant role in overall system performance and costs, so optimization is important. Thus, a memory compiler is a critical tool.

The OpenRAM project aims to provide an open-source memory compiler development framework for memories. It provides reference circuit and physical implementations in a generic 45nm technology and fabricable Scalable CMOS (SCMOS), but it has also been ported to several commercial technology nodes using a simple technology file. OpenRAM also includes a characterization methodology so that it can generate the timing/power characterization results in addition to circuits and layout while remaining independent of specific commercial tools. Most importantly, OpenRAM is completely user-modifiable since all source code is open source. In this work, a 64 kb 12T SRAM array layout is created in 32 nm SOI CMOS technology using OpenRAM.

The rest of this paper is organized as follows. Section II explains the design and operation principles of the proposed 12T bitcell. In Section III half-select disturbance free and efficient bit-interleaving features of proposed bitcell are explained. Leakage control mechanism of proposed bitcell is explained in Section IV. Section V introduces the OpenRAM memory compiler. A 64 kb SRAM array of proposed 12T bitcell with design considerations and Monte Carlo simulation results are shown in Section VI to evaluate the effectiveness of the 12T bitcell for low-voltage and low-power operations. Finally, Section VII concludes the paper.

II. PROPOSED 12T SRAM BITCELL

Figure 2(a) shows the schematic of the proposed 12T bitcell. This bitcell is fully differential, therefore, it has a good noise and mismatch immunity. The proposed 12T bitcell consists of a cross-coupled inverter pair (ML1, ML2, MR1 and MR2) that keeps the stored data, write access transistors (ML3, ML6, MR3 and MR6) and decoupled differential read ports (ML3, ML4, ML5, MR3, MR4 and MR5). The wordline signal (WL) is row-based while its SEL signal is column-based. In the proposed 12T bitcell, all the transistors are minimum sized ($W = 104$ nm and $L = 40$ nm) because read and write path does not have conflicting design requirements in this bitcell. Besides, in subthreshold operation, since the ratio of PMOS to NMOS current depends exponentially on threshold voltage, sizing is not a strong element for improving noise margin during its read or write mode. Figure 2(b) shows one possible thin cell layout of the proposed 12T bitcell. Although this 12T bitcell adds more area overhead relative to 6T SRAM bitcell, the overall area penalty is less because more bitcells can be included in the bitlines.

Fig. 2. (a) Proposed 12T bitcell, (b) One possible $1.4 \mu m^2$ layout in 32nm SOI CMOS technology.

Fig. 3. (a) Timing Diagram, Current paths in (b) read and (c) write mode.

A. Read Operation

Figure 3(a) displays the 12T bitcell timing diagram in read, write and hold modes. And, Figure 3(b) shows the 12T bitcell current path during the read mode. The bitlines (BL , BR) are precharged to V_{DD} before the cell is accessed. When its

Fig. 4. (a) Read VTC curves comparison, 6T vs. proposed 12T bitcell, (b) Write VTC curves comparison, with an without WL and SEL voltage boosting

Fig. 5. Monte Carlo simulation results for noise margin distribution in Read, Write and Hold mode for proposed 12T bitcell ($V_{DD} = 300$ mV, $25^\circ C$, TT).

wordline is enabled and SEL remains disabled ($WL = 1$ and $SEL = 0$), BL is discharged through pull-down transistors MR3, MR4 and MR5. In this case, Q has the value 0 that leads to a discharge in its BL while BR stays high. A latch-type sense amplifier is used to sense the differential swings on BL and BR in order to speed up the read operation. In the proposed 12T, the read value is an inverted signal of stored value, hence, position of the BL and BR are exchanged in this bitcell. The cell storage node is decoupled from the read bitline, therefore, Static Noise Margin (SNM) in read mode is almost equal to its Hold Noise Margin (HNM) of the 6T bitcell.

The SNM is defined as the maximum possible noise available at the gates of the cross-coupled inverters or storage element that does not flip the bitcell value [12]. The read Voltage Transfer Characteristic (VTC) of 12T bitcell can be measured by sweeping the voltage at storage node Q with BL , BR and WL biased at V_{DD} while monitoring the node voltage at QB . Three roots of intersection in VTC curves are desired to indicate bistability. The SNM can be quantified by the side of the largest square embedded between the read VTC curves. Figure 4(a) shows the VTC curves for the proposed 12T bitcell and compares it with the SNM of traditional 6T bitcell. The 12T bitcell has a SNM of 86 mV at 0.3 V while that of a 6T bitcell is 30 mV; the 12T bitcell gains %65 improvement compared with 6T bitcell.

B. Write Operation

Figure 3(c) shows the 12T bitcell during write mode; Here, Q and QB have values of 0 and 1, respectively and are tried to

Fig. 6. SNM and WNM of proposed 12T bitcell in different PVTs.

be written over by opposite values. The bitlines BR and BL charge and discharge to V_{DD} and GND , respectively. When both wordline and select-line are enabled ($WL=1$ and $SEL=1$), BR is discharged through ML3, ML6. As the position of BL and BR are exchanged in this bitcell, write data is also inverted for correct writing.

Figure 5 shows the distribution of the SNM , WNM and HNM of proposed 12T bitcell and also the SNM of a traditional 6T bitcell, in presence of local and global variations for 1000-point Monte Carlo simulation at a 300 mV supply voltage. The mean value for SNM , WNM and HNM for the proposed 12T bitcell are 86 mV, 110 mV and 86 mV, respectively, while the SNM for a 6T bitcell is 30 mV.

To evaluate the effectiveness of the proposed 12T bitcell under Process, Voltage and Temperature (PVT) variations, Monte Carlo simulations are done for both read and write modes at different process corners, supply voltages and temperatures. As shown in Figure 6, the proposed 12T bitcell has adequate values for both SNM and WNM in all process corners as well as a wide range temperature operation. As shown in this figure, even at worst case conditions, the 12T bitcell has bigger values for SNM and WNM compared to a 6T bitcell. Besides, the proposed 12T has acceptable SNM and WNM values for supply voltages in subthreshold regions.

C. Writability Improvement

Series-access transistors in 12T bitcell can degrade the writability. Boosted word-line voltage, lower or float cell supply voltage, and the negative bit-line voltage are among techniques aim to speed up the discharging process during the write mode and improve the writability of the bitcell. A higher wordline and negative bitline voltages lead to stronger access transistors [13], [14] and a lower or float cell-supply voltage leads to weaker pull-up devices during write operation [7], [15]; all these techniques improves cell writability.

In 6T bitcell, row-based control of boosting wordline voltage, increases the failures in the half-selected cells in that row. Therefore a column-based control is needed to reduce the supply voltage of the selected column during write and keep that of unselected column at nominal voltage. However, a lower cell supply voltage reduces the trip-point of the inverter and gain of the cross-coupled inverter pair which negatively impact cell writability.

A negative bitline voltage is more effective compare to lower cell supply voltage because it does not impact the cross-coupled inverters of the bitcell. There are different techniques to make a small negative voltage source. Negative voltage source can be implemented off-chip, on-chip or by using capacitive coupling to generate a transient negative voltage [14]. [14] needs large boosting devices to increase the negative voltage leads to more area overhead and also this technique is not suitable for long bitline because the negative voltage reduces as number of bitcell on bitline increases. Negative bit-line scheme also can increase the data-retention failures due to increased leakage by providing a small positive V_{GS} on the access transistor in the unselected cells.

Negative bit-line technique is less effective than boosting wordline voltage since it only increases the strength of one access transistor (bitline with low voltage) while a boosted wordline voltage makes both access transistors stronger. To improve the writability of the proposed 12T bitcell we use boosted wordline voltage technique. Unlike 6T, proposed 12T is half-select disturb free and allows boosting voltage of SEL and WL to improve the strength of MR6/ML6 and MR3/MR4 transistors. Therefore, in this work WL and SEL are boosted by 50 mV (at 300 mV supply voltage) to increase the current of series access-transistors for a writability improvement. Boosting the WL degrades the read stability, therefore WL is boosted only during write mode. Figure 4(b) shows the write VTC curves with WL and SEL voltage boosting for the proposed 12T bitcell and compares with VTC curves of bitcell without voltage boosting. This figure shows how 50 mV voltage boosting for both WL and SEL improves WNM of proposed 12T bitcell.

III. HALF-SELECT FREE BITCELL AND EFFICIENT BIT-INTERLEAVING FOR SOFT ERROR IMMUNITY

Similar to 6T bitcell, 8T [5], 10T [6], [7] and the 12T bitcell [10] configurations, still suffer from the problem associated with the half-select disturbance effect. The half-select disturbance occurs when there is a half-selected column (row) during a write operation, as shown in Figure 7. During this occurrence, the bitcell in the unselected column (row) is disturbed because WL (SEL) is raised to turn on the access transistors for selected bitcells. The bitcell current flowing in the access transistors should be large for the written bitcells to flip the data while it should not be too large for the disturbed bitcells to avoid data corruption [4].

In the proposed 12T bitcell, only the accessed bitcells in a row are activated for a write operation through their respective WL and SEL signals. As shown in Figure 8(a), although, other bitcells on the same row are selected with same wordline signals, their respective SEL are at a low level to avoid any disturbance for stored value. For the half-selected bitcells in an active column as shown in Figure 8(b), WL is at low level, so stored value cannot be disturbed by bitline voltage.

Another problem in design of robust SRAM bitcells is solving multi-bit soft errors that occur when an alpha particle or comic ray hits the memory and causes it to lose data [16].

Fig. 7. Half-select disturbance in SRAM.

Fig. 8. Write half-selected bitcells in (a) active row, (b) active column.

When SRAM operates near to the threshold region, cosmic rays can induce soft errors more easily because the critical charge is reduced. Multi-bit errors from a single strike usually occur in two to three adjacent bitcells [16]. Thus, to prevent multi-bit error from occurring in a single word, bits from different words should be interleaved. Shared-wordline and bit-interleaving (column-multiplexing) are common ways of arranging the words in SRAM [17]. In the shared-wordline scheme, which is widely used because of its simplicity, the probability of multi-bit errors is high because all the bits of a word are next to each other. Multiple bit errors are regarded as one single bit error in the bit-interleaving structure that is detectable and easy to correct with conventional ECC techniques. However, because of half-select issue, most of the SRAM designs cannot be bit-interleaved, and can only be implemented in shared-wordline architecture [8]. In [5], [6] and [7], to avoid the half-select, the entire cells on a row are written at the same time which makes these SRAMs exposed to multi-bit soft errors.

In the proposed 12T bitcell, only one word is turn on while others are not disturbed, therefore, it is possible to implement a bit-interleaving structure with the proposed bitcell. Besides, bit-interleaving in SRAM designs allows better pitch matching between the bitcell array layout and read/write circuitry that ultimately helps to increase the bitcell density.

IV. LEAKAGE CONTROL IN READ AND HOLD MODES

In the read operation, one bitline discharges and the other one stays high. As soon as the differential swing on bitlines exceeds the input voltage offset of sense amplifiers, data is ready on the data bus. Compared to the single-ended read bitline which needs a full swing to provide the correct output in the proposed 12T, differential structures speeds up the read operation with less access time. Figure 9(a) shows the worst

Fig. 9. (a) Worst case bitline leakage scenario in read mode, BL/BR voltage of a column with 256 bitcells at (b) $V_{DD} = 0.6$ V and (c) $V_{DD} = 0.3$ V.

case scenario for bitline leakage during read; when accessed cell holds value '1' and all other cells store '0'. In this case, leakage current by unselected cells is comparable to read current which may cause a read failure. Transient simulation results in Figure 9(b) and 9(c) verify the effectiveness of ML4/MR4 transistor in leakage control during read mode. The proposed bitcell has three series stacking transistors in read path which helps to reduce the leakage and allows to put more bitcells on bitline which enables less bitline partitioning and less area overhead. As shown in Figure 9(b), the 12T bitcell in [9] operates in 0.6 V supply voltages, but due to large leakage during its read mode, this cell fails at 0.3 V (Figure 9(c)) while the proposed 12T controls the leakages in small supply voltages and can be used in long bitlines. During hold mode ($WL = 0$ and $SEL = 0$), ML4/MR4 adds an off device in its leakage path through BL and BR to GND and decreases the leakage through the ML3/MR3 transistor. Besides, node L and R (Figure 2(a)) are floating above 0 and make the V_{GS} of ML3/MR4 negative, therefore, reducing the leakage current exponentially.

V. OPENRAM: AN OPEN-SOURCE MEMORY COMPILER

OpenRAM is an open-source and portable memory compiler which is implemented using an object-oriented approach in the Python programming language [11]. OpenRAM is translatable across numerous process technologies. This is accomplished by using generalized routines to generate the memory based on common features across all technologies. To facilitate user modification and technology interoperability, OpenRAM provides a reference implementation in the SRC-funded 45nm FreePDK45 [18] and a fabricable option using the MOSIS Scalable CMOS (SCMOS) design rules. FreePDK45 uses many design rules found in modern technologies, but is non-

Fig. 10. OpenRAM overall compilation and characterization methodology.

fabricable, while SCMOS enables fabrication of designs using the MOSIS foundry services. OpenRAM has also been ported to other technologies such as IBM 32 nm SOI CMOS for this work, but these are not directly included due to licensing issues.

OpenRAM is technology-independent by using a technology directory that includes the technology's specific information, rules, and library cells. Technology parameters such as the design rule check (DRC) rules and the GDS layer map are required to ensure that the dynamically generated designs are DRC clean. Custom designed library cells such as the bitcell and the sense amplifier are also placed in this directory. OpenRAM has two functions that provide a wrapper interface with DRC/LVS tools. These two functions perform DRC/LVS using the GDSII layout and SPICE netlist files. In OpenRAM, DRC/LVS are performed at all levels of the design hierarchy to enhance bug tracking. DRC/LVS can be disabled for improved run-time or if tool licenses are not available.

OpenRAM’s framework is divided into front-end and back-end methodologies as shown in Figure 10. The front-end has the compiler and the characterizer. The compiler generates SPICE models and its GDSII layouts based on user inputs. The characterizer calls a SPICE simulator to produce timing/power results. The back-end uses the generated SPICE netlists and GDSII layouts to generate annotated timing and power models using back-annotated characterizations. The characterizer has four main stages: generating the SPICE stimulus, running the circuit simulations, parsing the simulator’s output, and producing the characteristics in a Liberty (.lib) file. Results from simulations are used to produce the average power, setup/hold times, and timing delay of the memory design.

OpenRAM accepts user-provided parameters to generate the design. It decides the appropriate internal parameter dependencies which are dependent on the user-desired data word size, number of words, and number of banks. It is responsible for instantiation of the single control logic module which controls the SRAM banks. The control logic ensures that only one bank is active in a given address range. Bank is the bulk of the non-control memory layout and instantiates bit-cell arrays

Fig. 11. Final SRAM module with a multi replica bitline delay [19] to control sense amplifier timing.

and coordinates the row and column address decoders along with their precharge, sense amplifiers, and input/output data flip-flops.

VI. SRAM ARCHITECTURE AND RESULTS

Figure 11 shows the block diagram of a 64 kb (256×256 bit) SRAM array with dynamic supply headers to boost SEL and WL voltages by 50 mV in write mode.

Differential structure of proposed bitcell allows a high speed read operation by using voltage sense amplifiers which amplify the small differential swings on the bitlines at the proper timing. Accurate timing of sense amplifier with the increased in process variations and sensitivity to PVT is extremely important. In our design, to suppress the effect of random V_{TH} variations on timing of sense amplifier enable (SAE) signal, Multi Replica Bitline Delay ($MRBD$) [19] technique is used. In $MRBD$ technique, 12T memory bitcells drive delay of control path. The delay driven memory cells in control path are same as that of read path; so is the delay shift according to the PVT variation. Therefore, the $MRBD$ technique attains self-timed tracking with optimal SAE timing.

As shown in figure 11, in *MRBD*, a replica column is divided to M segment ($RBL_0, RBL_1, \dots, RBL_{M-1}$) and in each segment both bitlines (BL and BR) are tied together to drive the inverter. Therefore, compared with the conventional replica bitline design [20], with the same count of replica cells (RC), each RBL segment capacitance load and RC discharged current are doubled ($(2 \cdot C_{BL})/M$ and $2 \cdot I_{read}$). The delay of each segment of replica bitline is therefore $1/M$ of that of the conventional bitline delay and the sum of the delays of all M replica bitline is the same as that of the conventional replica bitline delay technique. *MRBD* scheme also utilizes multi replica cells (k) in each segment of replica column. Thus, the current of the replica cells each segment of replica bitline is K times of the conventional replica bitline ($(K \cdot I_{read})$). As a result, variation (σ) of the *SAE* timing is divided by $\sqrt{M}$ due to M replica bitline segments and $K \cdot \sqrt{K}$ due to K replica cell in each segment and $\sqrt{2}$ because of the using both BL

Fig. 12. Maximum operating frequency for 64 kb array of proposed 12T bitcell versus supply voltage.

Fig. 13. Read delay in different supply voltages.

and BR in discharging the replica bitline. Therefore, σ of the timing for SAE is divided by $K \cdot \sqrt{(2 \cdot M \cdot K)}$. Thus, the variation on SAE timing is considerably reduced compared to that in the conventional replica bitline. Considering the area overhead of using MRBD, the optimum value of M and K are 4 and 4 in this work.

In this paper, all of the comparisons are simulated by re-creating the circuits from scratch using OpenRAM and the results stem from the simulations using IBM 32 nm SOI CMOS technology. To have a fair comparison with the proposed 12T bitcell, an iso-configuration SRAM array is created (256×256 bit array) for 6T ($\beta = 2$), 8T [5], 10T [7], 10T [8], 12T [9], 12T [10] and the proposed bitcell. Post layout simulations include both the local and global variations that provide a complete representation of the variations during chip manufacturing.

Figure 12 shows the maximum operating frequency of a 64 kb 12T SRAM array versus different supply voltages. This figure shows that the proposed 12T SRAM array can perform at 50 MHz with 0.3 V and also functions at 2.2 GHz with 0.9 V supply voltages. Therefore, this bitcell is a good option for both subthreshold and high-performance operations. The minimum V_{DD} of the SRAM array is limited by read operation as the read current becomes weak with smaller V_{DD} .

Figure 13 compares the read delay of SRAM arrays at different supply voltages. Read delay for bitcells with differential read port is defined as the time interval from %50 of a low-

to-high transition of a wordline signal until there is a 150 mV differential swing on the bitlines, while for bitcells with single-ended read port, a full swing is needed which leads to slower read operation. As shown in figure 13, the 64 kb array has a read delay of 2.4 ns for proposed 12T bitcell at 350 mV supply voltage and room temperature while 6T bitcell does not work at this voltage and due to larger bitline leakage in other bitcell arrays, it takes more time to develop a 150 mV differential swing on their bitlines therefore they are slower. Besides, proposed 12T reads and writes at 300 mV, where other bitcells cannot work due to high leakage or inadequate SNM or WNM . However, as supply voltage increases, 10T [8] and 12T [9] becomes as fast as proposed cell, because although these bitcells have larger leakage, they have less transistors in their differential read path compared to proposed 12T bitcell.

The leakage, dynamic and total power consumption of the SRAM arrays at different operating voltages is also explored, as shown in Figure 14. At 50 MHz and 0.3 V the leakage power for proposed 12T bitcell array is 0.94 mW while other bitcell don't work at this supply voltage due to large leakage and read failure. Total power consumption is smaller using proposed 12T bitcell in different supply voltages because this bitcell has less leakage and dynamic power consumption compared to other bitcells. At 0.6 V proposed 12T array consumes %12, %26 and %46 less power compared to 10T [8], 12T [9] and 6T arrays, respectively.

Table I compares the performance of the proposed 12T with other bitcells. All SRAM arrays have same configuration and are simulated in the maximum operation frequency of minimum supply voltage. Proposed 12T bitcell shows improvement in leakage and dynamic power reduction. It has faster read operation and works in higher frequency compared to other bitcells. Due to great leakage suppression, proposed 12T bitcell can be used on long bitlines to get less area overhead. The proposed 12T array uses %5 more area compared to 10T [8], however, it consumes %65 less power at 0.35 V and works even in smaller supply voltages where 10T [8] cannot work due to read failure caused by high leakage.

VII. CONCLUSION

In this work, a differential single-port subthreshold 12T bitcell with high performance is proposed which improves read stability and writability and allows continued scaling beyond what is possible with the 6T SRAM bitcell. The proposed 12T bitcell has data-independent leakage control and helps to reduce the leakage power dissipation which is a substantial portion of the total power in subthreshold while guarantees successful read and write operations. Due to leakage control mechanism of proposed cell, more bitcells can attach to a bitline which leads to area efficiency for the SRAM. In addition, proposed cell is half-select disturbance free and allows bit-interleaving structure to reduce multi-bit soft errors by conventional error correcting code techniques.

This paper also introduced OpenRAM, an open-source and portable memory compiler. OpenRAM generates the circuit, functional model, and layout of variable-sized SRAMs. It is

Fig. 14. (a) Leakage, (b) Dynamic and (c) Total power comparison in different supply voltages for a 64 kb array (with all peripheral circuitries).

TABLE I
RESULTS FOR 64KB (256 × 256) IN IBM CMOS32SOI 32NM TECHNOLOGY.

Design	6T ($\beta = 2$)	8T [5]	10T [7]	10T [8]	12T [9]	12T [10]	Proposed 12T
Max. Frequency	100 MHz	25 MHz	25 MHz	75 MHz	75 MHz	25 MHz	50 MHz
@ Min. V_{DD}	@ 0.4 V**	@ 0.35 V*	@ 0.35 V*	@ 0.35 V*	@ 0.35 V*	@ 0.35 V*	@ 0.3 V
Leakage Power @ Min. V_{DD}	3.79 mW	2.72 mW	2.45 mW	2.15 mW	2.69 mW	2.57 mW	0.95 mW
Total Power @ Min. V_{DD}	5.31 mW	3.67 mW	3.30 mW	2.8 mW	3.34 mW	3.64 mW	1.25 mW
Bitcell area	×1	×1.3	×1.95	×2.1	×2.2	×3.5	×2.2
No. Transistors	402,672	538,024	669,088	657,898	802,658	811,534	803,482
Half-Select Free	No	No	No	Yes	Yes	No	Yes

* Fail to read at 0.3 V due to large leakage current. ** Fail to read at 0.3 V due to inadequate SNM.

anticipated that the code will be released after publication of this paper and hope to engage an active community in the future development of OpenRAM.

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