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MLB-PoL: A High Performance Hybrid Converter for Direct 48 V to Point-of-Load Applications

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***Abstract*—There is an increasing need for more efficient power conversion from 48 V_{dc} to point-of-load (PoL) applications in datacenters. This work presents a new hybrid converter with *Multi-Level Binary* (MLB) voltages on the flying capacitors that is well-suited for PoL applications with very high conversion ratios. The proposed MLB-PoL converter can be viewed as an 8-to-1 multi-phase doubler switched-capacitor (SC) converter merged with a two-phase interleaved buck converter. Compared to other two-phase hybrid SC topologies, multi-phase operation can help achieve higher conversion ratio in the SC stage with an equal or fewer number of components, and thus reduce the switch and inductor stress of the following buck stage. In addition, the output inductors in the proposed topology benefit from a frequency multiplication effect similar to that of the flying capacitor multilevel (FCML) converter. This can help further reduce the inductor size without increasing the switching frequency. A 48 V to 2.5-1.0 V converter prototype with 65 A output current was built and tested. At 48 V to 2 V, the prototype achieved 95.1% peak efficiency (94.3% including gate drive loss) and 395 W/in^3 power density.**

***Index Terms*—Hybrid, switched capacitor circuits, large converter ratio, multilevel, circuit topology, interleave, buck, data center, point-of-loads.**

I. Introduction

The recent adoption of a 48 V_{dc} bus in modern datacenters introduces the challenge of converting from 48 V_{dc} to the extreme low voltage and high current point-of-loads (PoL). To address such a high conversion ratio, a two-stage approach is commonly used. The 48 V is first converted to an intermediate bus voltage (e.g. 12 V) through a bus converter, then stepped down to 1-2 V by PoL converters [1]–[7]. However, a number of recent works have demonstrated direct 48 V to PoL conversion [8]–[12], and have shown promise for better overall efficiency, power density and reduced system cost. For such high conversion ratio, a transformer-based converter is commonly used [9], [10]. Unavoidably, there is a trade-off between conversion efficiency and voltage regulation range. To address such challenge, the high step-down and the regulation requirements can be split between a highly efficient fixed-ratio LLC converter and an upstream buck-boost converter [11] or a series-stacked buck converter with partial power processing [12].

In addition to transformer-based solutions, the hybrid topologies proposed recently comprising multi-phase buck converters merged with a fixed-ratio switched-capacitor (SC) converter have also shown attractive features for direct 48 V to PoL conversion [13]–[15]. Similar to transformers, SC converters also have excellent performance at fixed-ratio conversions, thanks to their efficient utilization of active and passive components [16]–[18]. By combining the buck and the SC stages, the total number of components (e.g. switches and decoupling capacitors) can be reduced compared to cascaded two-stage solutions. More importantly, the inductor of the buck converter can greatly reduce or eliminate the capacitor charge sharing loss of the SC converter through soft-charging operation [17], [19], leading to very efficient fixed-ratio conversion in the SC stage. However, due to the fact that the circuit complexity of SC converters increases in proportion to the conversion ratio, the SC stage in the majority of existing hybrid works can only achieve a conversion ratio of 4-to-1 or 6-to-1, with the remaining conversion burden placed on the buck stage. Given a fixed output voltage, the efficiency of a buck converter generally decreases with increasing input voltage. If the first stage SC converter can achieve a higher conversion ratio without much extra loss, the input voltage of the buck converter can be decreased, and the overall 48V-to-PoL efficiency can be improved. References [20], [21] suggest that using a highly efficient 48 V to 6 V fixed-ratio converter in conjunction with a 6 V to PoL buck converter can provide improved overall efficiency.

This work proposes and explores a new hybrid topology with *Multi-Level Binary* (MLB) voltages on the flying capcitors that can simultaneously achieve high efficiency and power density for direct 48 V to PoL applications. The proposed MLB-PoL converter consists of an 8-to-1 SC stage and a two-phase interleaved buck stage with natural current balancing. By having multiple operating phases, the SC stage can achieve a conversion ratio of 8-to-1 with the theoretical minimum number of components (10 switches and 3 capacitors). The operation of the output buck stage is merged with the SC stage without the need of additional switches, thereby reducing the conduction loss. Furthermore, the inductors of the buck stage also benefit from a frequency multiplication effect similar to that of the flying capacitor multilevel (FCML) converter [22], [23]. This can further reduce the inductor size without increasing the switching frequency of the SC stage. A 48 V

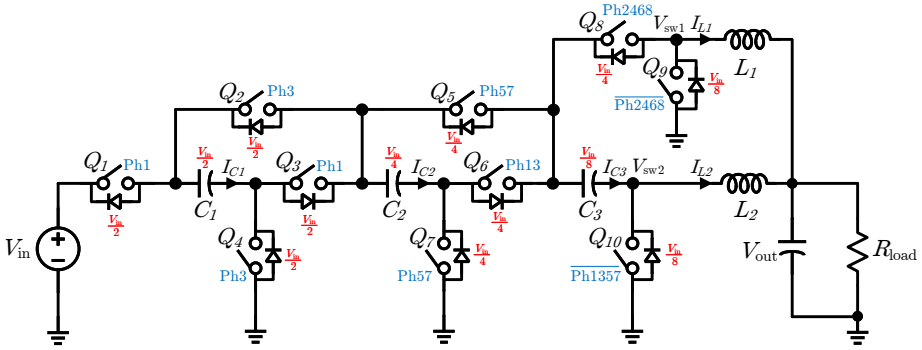


Fig. 1: Schematic drawing of the proposed hybrid SC converter. The device voltage ratings are labeled in red and the operating phases of the switches are labeled in blue.

to 2.5-1.0 V converter prototype with 65 A output current was built and tested. At 48 V to 2 V, the prototype achieved 95.1% peak efficiency (94.3% including gate drive loss), 91.3% full load efficiency (91.1% including gate drive loss), and 395 W/in^3 power density.

II. Proposed Topology

The schematic drawing of the proposed MLB-PoL converter is shown in Fig. 1, with switch and capacitor voltage ratings labeled in red and operating phases labeled in blue. The voltage, current, and PWM waveforms of the converter and the equivalent circuit model of different operating phases are shown in Fig. 2. The proposed converter can be viewed as an 8-to-1 SC converter merged with a two-phase interleaved buck converter.

The MLB-PoL converter employs multiple operating phases within each switching cycle. As discussed in [24], compared with typical SC converters that have two operating phases, multi-phase SC converters can achieve the same conversion ratio with significantly fewer switches and flying capacitors. The SC stage in the proposed topology is an 8-to-1 multi-phase voltage doubler [4], [25], which is one practical circuit implementation that achieves the theoretical maximum gain for an 8-to-1 SC converter (i.e. 10 switches and 3 capacitors).. The flying capacitors carry binary voltages: $C_1 = \frac{1}{2}V_{\text{in}}$, $C_2 = \frac{1}{4}V_{\text{in}}$ and $C_3 = \frac{1}{8}V_{\text{in}}$, as do the switches: $Q_{1,2,3,4} = \frac{1}{2}V_{\text{in}}$, $Q_{5,6,7,8} = \frac{1}{4}V_{\text{in}}$ and $Q_{9,10} = \frac{1}{8}V_{\text{in}}$.

To maintain flying capacitor charge balance in multi-phase SC converters, the lower voltage capacitors must be charged/discharged for more time than the higher voltage ones [26]. Here, in order to merge the operation of the SC stage with the buck stage, the charge/discharge cycles of C_2 and C_3 are divided into multiple phases. As shown in Fig. 2, C_1 is charged in phase 1 and discharged in phase 3, C_2 is charged in phase 1 and 3, and discharged in phase 5 and 7, whereas C_3 is charged in phases 1, 3, 5, 7 and discharged in phases 2, 4, 6, 8. The operation of the two-phase interleaved buck stage is merged with the SC stage without additional switches. This can help reduce the conduction loss compared to a two-stage approach, where the buck converter is directly cascaded with a SC converter. The two inductors are energized (i.e., current ramping up) alternately: L_1 is energized by C_3 during phases 2, 4, 6, 8, and L_2 is energized by the series combination of the flying capacitors during phases 1, 3, 5, 7. Phase 9 is the freewheeling state for output voltage regulation where the current in both inductors ramps down.

TABLE I: Voltage rating and operating frequency of the main active and passive components

	V_{blocking}	f_{sw}
Q_1 - Q_4	$\frac{V_{\text{in}}}{2}$	f_0
Q_5 - Q_7	$\frac{V_{\text{in}}}{4}$	$2f_0$
Q_8	$\frac{V_{\text{in}}}{4}$	$4f_0$
Q_9 - Q_{10}	$\frac{V_{\text{in}}}{8}$	$4f_0$ (ZVS)
C_1	$\frac{V_{\text{in}}}{2}$	f_0
C_2	$\frac{V_{\text{in}}}{4}$	$2f_0$
C_3	$\frac{V_{\text{in}}}{8}$	$4f_0$
L_1,L_2	$\frac{V_{\text{in}}}{8}$ - V_{out}	$4f_0$

There is an inherent current balancing mechanism between the two inductors. If I_{L1} is higher and over-discharges C_3, the switch node voltage of L_2 will then become higher, inducing a higher I_{L2} that can charge C_3 back to its nominal value. This operation is similar to the automatic current sharing behavior of the series-capacitor buck converter, which can be found in [27]. Here, C_3 acts as the series capacitor that creates a negative feedback loop between the capacitor voltage and the average inductor currents.

The MLB-PoL topology also benefits from an inductor frequency multiplication effect similar to that of the flying capacitor multilevel (FCML) converter. Defining f_0 as the switching frequency of C_1 and the associated switches $Q_{1,2,3,4}$, then C_2 and $Q_{5,6,7}$ operate at $2f_0$ and C_3, $Q_{8,9,10}$, and $L_{1,2}$ operate at $4f_0$. Note that out of the three switches operating at $4f_0$, only Q_8 is hard switched at $\frac{V_{\text{in}}}{4}$, while Q_9 and Q_{10} operate with zero-voltage switching (ZVS). In addition, the higher voltage rated switches operate at a lower frequency, reducing switching loss. This feature can provide inductor size reduction without increasing the frequency of all switches, particularly those with a higher voltage rating. The device voltage ratings and the corresponding switching frequencies are summarized in Table I.

In order to derive the output voltage expression, we define D as the duty cycle of signal Ph1 as shown in Fig. 2. Since the

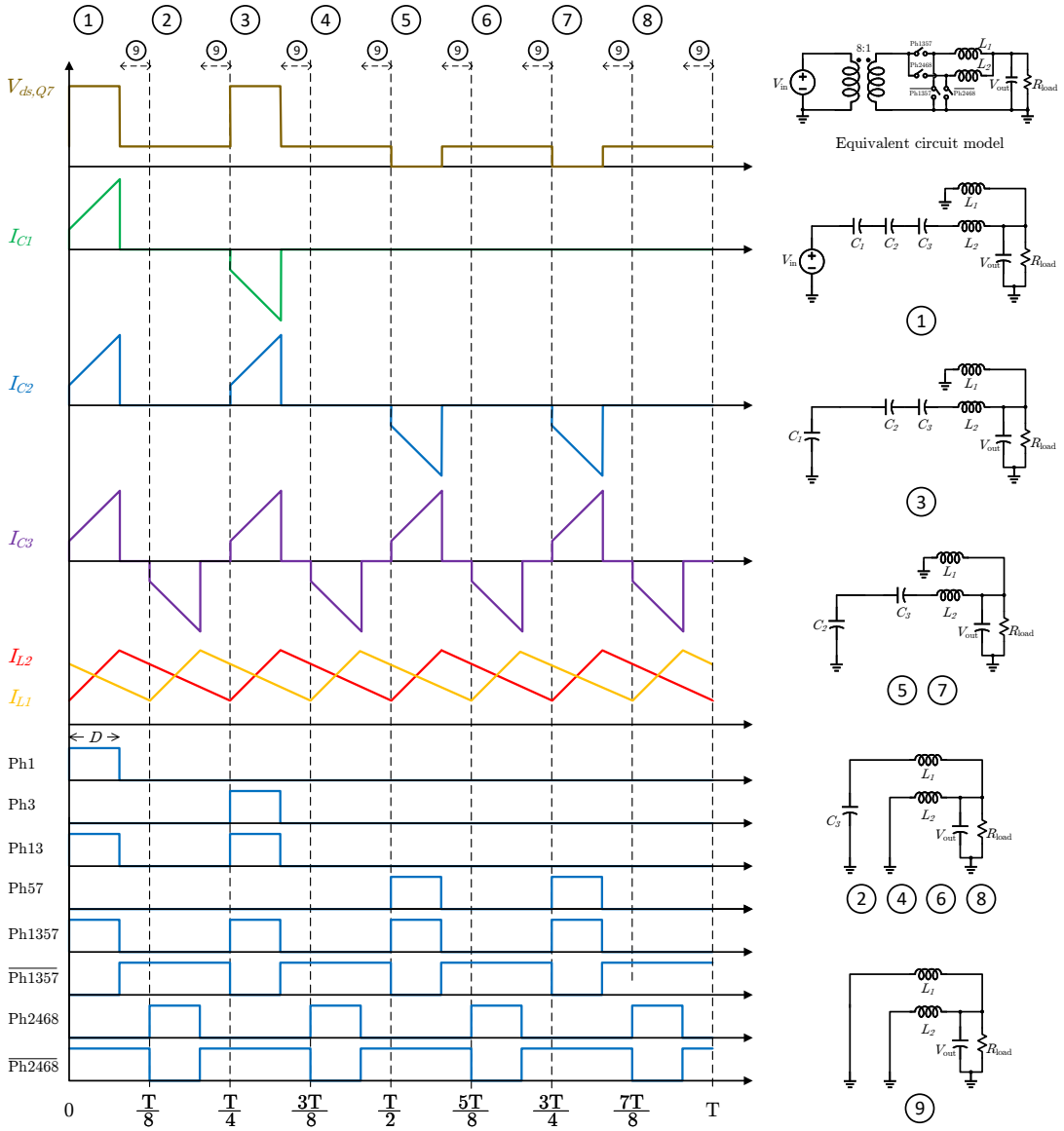


Fig. 2: Voltage, current and PWM waveforms of the proposed hybrid SC converter and equivalent circuit models.

inductors see four times the switching frequency, the effective duty cycle of the buck stage is $D_{\text{eff}} = \frac{DT}{\frac{T}{4}} = 4D$. The output voltage can then be derived by combining the conversion ratio of the fixed-ratio SC stage (DCX ratio) and the conversion ratio of the buck stage:

$$\begin{aligned} V_{\text{out}} &= V_{\text{in}} \cdot \text{DCX\_ratio} \cdot \text{buck\_ratio} \\ &= V_{\text{in}} \cdot \frac{1}{8} \cdot 4D \\ &= \frac{DV_{\text{in}}}{2}. \end{aligned} \tag{1}$$

As it is regulated with a duty cycle, the converter can share the same control techniques as that of conventional buck converters. Note that the maximum D is limited by the length of each operating phase to $\frac{1}{8}$. Thus, the highest output voltage of the proposed converter is $\frac{V_{\text{in}}}{16}$. With 48 V input, the maximum output voltage at no-load condition is 3 V, making it incapable of supplying loads at 3.3 V. This reduced output range is a trade-off compared to other hybrid topologies with 4-to-1 or 6-to-1 SC stages. Nevertheless, if a lower output voltage is

TABLE II: Comparison of the voltage conversion* strategies of the latest hybrid direct 48V-to-PoL converters

	DCX ratio	Buck ratio
This work	8:1	3:1
LEGO [13]	6:1	4:1
DIH [28]	6:1	4:1
MIH [14]	4:1	6:1
SC Buck [15], [29]	4:1	6:1

*Assuming 48 V to 2 V conversion.

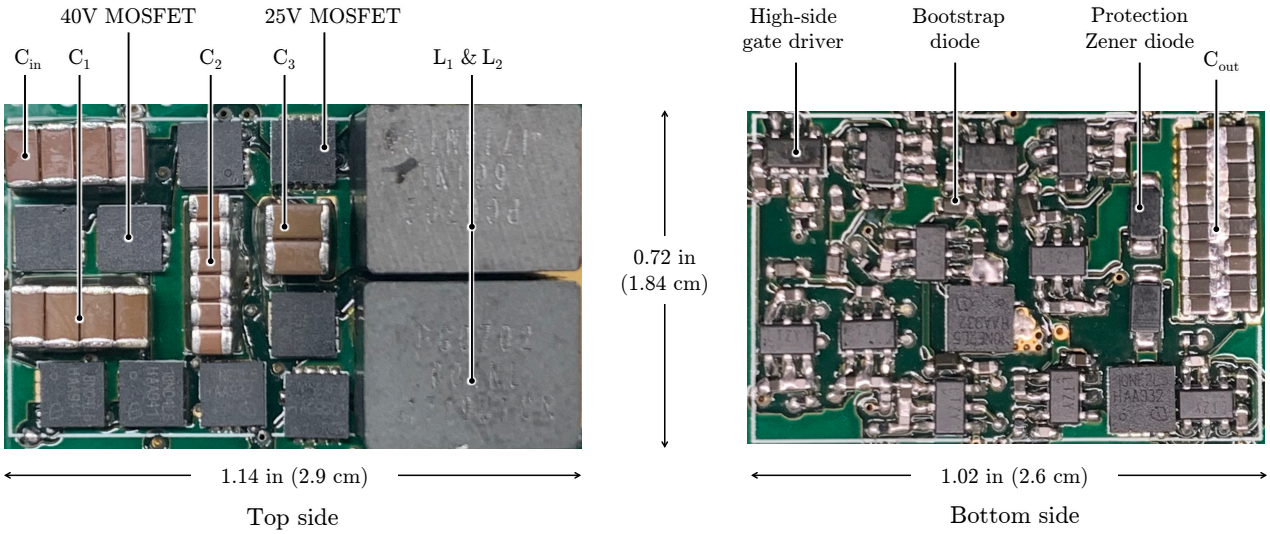


Fig. 3: Photograph of the prototype. Dimensions: 1.14 × 0.72 × 0.39 inch (2.9 × 1.84 × 1.01 cm).

TABLE III: Main component listing of the prototype

Component	Part number	Parameters
Switch Q_1-Q_4	Infineon BSZ018N04LS6	40 V, 1.8 mΩ
Switch Q_5-Q_8	Infineon BSZ010NE2LS5	25 V, 1.0 mΩ
Switch Q_9-Q_{10}	Infineon IQE006NE2LM5CG	25 V, 0.65 mΩ
Parallel Q_{10}	Infineon BSZ010NE2LS5	25 V, 1.0 mΩ
Flying capacitor C_1	TDK C3216X5R1V226M160AC	X5R, 35 V, 22 μF*×8
Flying capacitor C_2	TDK C2012X7S1E106K125AC	X7S, 25 V, 10 μF*×12
Flying capacitor C_3	TDK C3216X5R1A107M160AC	X5R, 10 V, 100 μF*×4
Inductor L_1,L_2	Pulse PG0702.601NL	600 nH, 0.91 mΩ
Input capacitor C_{in}	TDK C3216X7S2A335M160AB	X7S, 100 V, 3.3 μF*×8
Output capacitor C_{out}	TDK C1608X5R1A226M080AC	X5R, 10 V, 22 μF*×20
Gate driver	Analog Devices LTC4440-5	80 V, high-side
Bootstrap diode	Infineon BAT6402VH6327XTSA1	40 V, Schottky

* The capacitance listed here is the nominal value before dc derating.

desired, the proposed converter with its 8-to-1 SC stage has the potential to achieve better performance compared to the 4-to-1 and 6-to-1 topologies. As shown in Table II, for the desired conversion from 48 V to 2 V, the proposed converter can achieve the highest DCX ratio at the SC stage among all hybrid topologies, resulting in reduced stress at the following buck stage. This reduced stress can improve the buck stage efficiency, which can have a substantial impact on the overall system efficiency. Moreover, it is found that the total switch VA rating ($\sum V_{ds} I_{rms}$) of the proposed converter can be as low as half that of a stand-alone buck converter, indicating better switch utilization in addition to reduced inductor stress.

III. Hardware Design and Experimental Results

A 48 V to 2.5-1.0 V hardware prototype with 65 A output current was designed and tested to verify the functionality of the proposed converter. The annotated photograph of the prototype is shown in Fig. 3, and the specifications of the key components are tabulated in Table III. The main operating parameters are summarized in Table IV.

TABLE IV: Key parameters of the prototype

Input voltage	48 V
Output voltage	1.0 - 2.5 V
Output current	65 A
Switching frequency (inductor)	250 kHz
Current density	198 A/in^3

In order to report a power/current density number by box volume and to compare directly with other commercial power

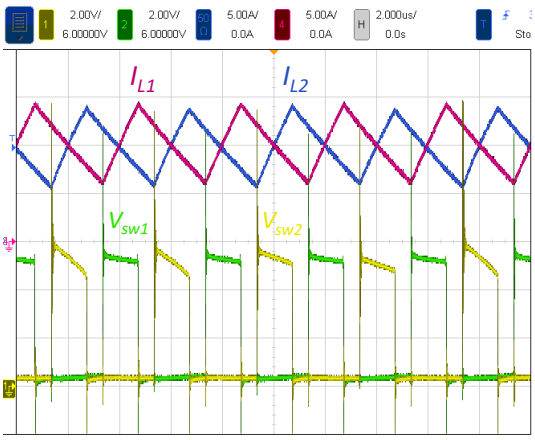


Fig. 4: Balanced interleaved inductor currents (V_{out} = 2 V, I_{out} = 20 A).

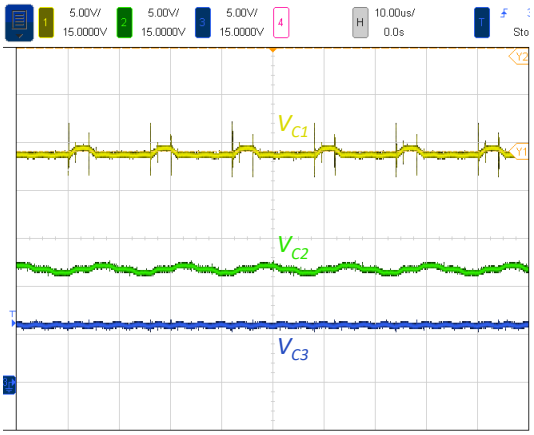


Fig. 5: Flying capacitor voltages at V_{out} = 2 V and I_{out} = 20 A.

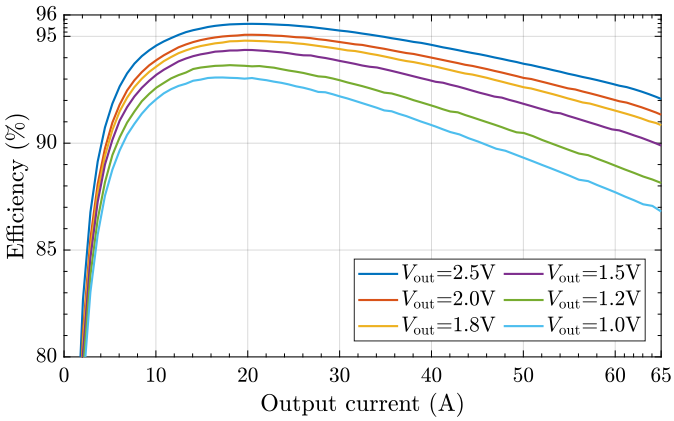


Fig. 6: Measured power stage efficiency from 48 V to 2.5-1.0 V.

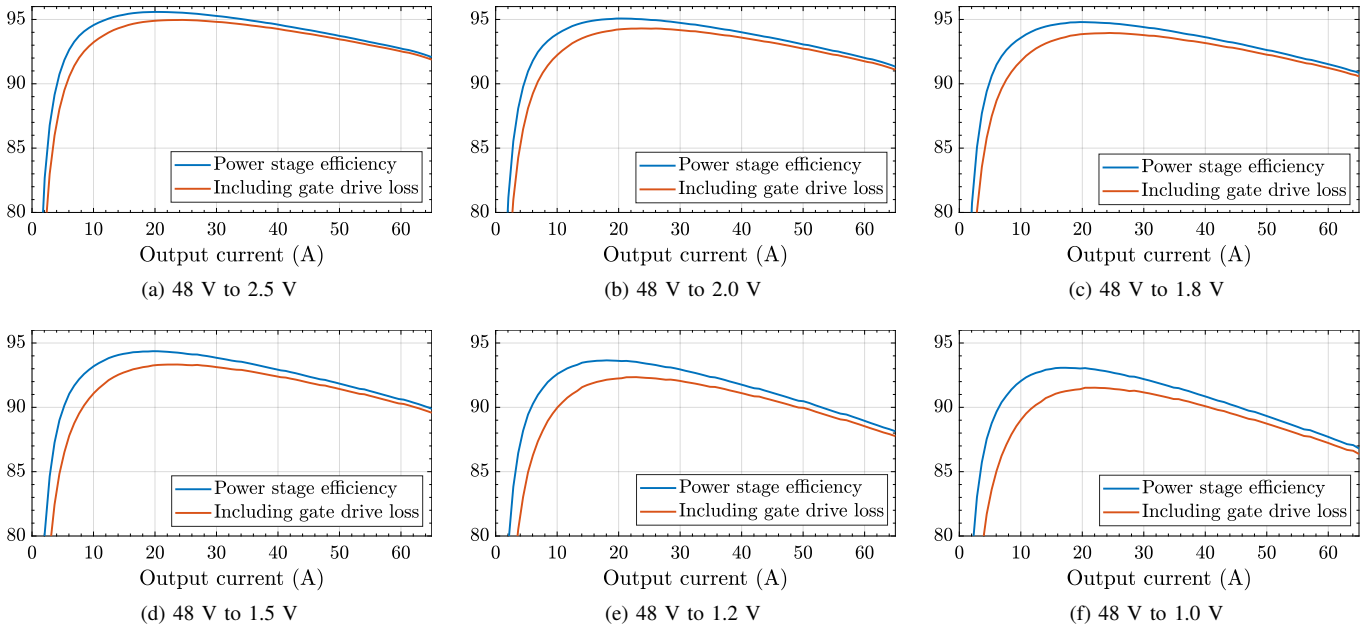
modules, all main components are tightly placed within a 1.14 inch by 0.72 inch (2.9 cm by 1.84 cm) rectangular PCB area. The switches, flying capacitors, and the inductors are on the top side, while the gate drive circuits and other protection components are placed directly underneath on the back side of the board. Input and output capacitors are also included in the box area. Due to the reduced voltage stress of the doubler SC topology, low-voltage MOSFETs can be used (40 V for Q_{1-4} and 25 V for Q_{5-10}). Since Q_{10} carries all of the output current, an additional switch is paralleled to reduce the conduction loss. High-side gate drivers with internal level-shifters are used to drive the switches, and a cascaded bootstrap circuit [30] is implemented to power the floating gate drivers. The PCB has 6 layers and is fabricated with 4 oz copper on the outer layers (where the critical conduction path is) and 2 oz copper on the inner layers.

The inductor selection is a critical design knob that affects the peak efficiency, the full-load efficiency, and the power/current density of the prototype. The Eaton HC1-1R0-R inductor used in [13] has high inductance (1 μH) and low DCR (1.23 mΩ), which may result in excellent peak and full-load efficiency. However, its bulky package size greatly limits the achievable box power/current density. The Coilcraft XAL7070-102 inductor has similar inductance and current rating, but comes in a smaller package size at the cost of higher DCR. It has the potential to achieve high peak efficiency and power density, though possibly at the expense of lower full-load efficiency compared to the Eaton inductor. Note that the peak efficiency of these hybrid converters usually appears at a very light-load condition, whereas the efficiency performance at middle to heavy load range might be more important in practical applications. Ultimately, the Pulse PG0702.601NL was selected, as it offered an attractive compromise between size and low DCR with a nominal inductance of 600 nH and a DCR of 0.95 mΩ, all in an acceptable package size. Although the peak efficiency of the prototype with this inductor was nearly 1% lower than a prototype using either of the 1 μH inductors, it achieved a good combination of high power/current density and full-load efficiency.

Compared to resonant switched-capacitor (ReSC) converters [3], the flying capacitor selection in these types of regulated hybrid SC converters is more relaxed, as the C and L values do not need to be tuned precisely so that the converter operates at the LC resonance point. The capacitance values have relatively minor effects on efficiency performance and flying capacitor voltage balancing. Nevertheless, it is important to make sure that the switches do not exceed their maximum voltage ratings and that the switch node voltage does not drop too low (i.e. to ground) due to the capacitor voltage ripple. Note that it may be possible to further reduce the amount of flying capacitance of the prototype, as the current design has not been fully optimized.

The two inductor currents and the corresponding switch node voltages are shown in Fig. 4, and exhibit good balancing. Fig. 5 shows the voltages across the C_1, C_2, and C_3 capacitors, which also exhibit good balancing, matching well with the theoretical values of 24 V, 12 V, and 6 V.

The performance of the prototype was measured with a



(a) 48 V to 2.5 V (b) 48 V to 2.0 V (c) 48 V to 1.8 V

(d) 48 V to 1.5 V (e) 48 V to 1.2 V (f) 48 V to 1.0 V

Fig. 7: Measured efficiency at various output voltages.

Yokogawa WT3000E precision power meter. The converter was tested up to 65 A output current, resulting in a current density of 198 A/in^3 (as measured by the smallest rectangular box that can contain the converter). The measured power-stage efficiencies at various commonly-used output voltages are plotted in Fig. 6, and the corresponding system efficiencies with gate drive loss included are shown in Fig. 7. Table V summarizes the peak and full-load efficiencies of each output voltage, as well as the power density by box volume and surface area. The converter operates at an effective switching frequency of 250 kHz (as seen by the inductors). At 48 V to 2 V, the prototype achieved 95.1% peak efficiency (94.3% including gate drive loss), 91.3% full load efficiency (91.1% including gate drive loss), and 395 W/in^3 power density. As shown in Fig. 8, the maximum temperature of the board at thermal equilibrium is about 85°C, when operating at full-load with 110 CFM fan cooling only.

Table VI compares this work with some of the best existing hybrid SC works with similar power ratings. As discussed previously, the proposed converter is designed to slightly trade peak efficiency at light-load for better heavy-load efficiency and power/current density. It can be seen that the proposed converter is able to carry the highest per-phase inductor current, while maintaining very good heavy-load efficiency. The comparison of current density is not straightforward, as different works use different calculation methods. Regardless, both the current density by box volume and by component volume reported in this work show the MLB-PoL's great potential. Furthermore, not only is this converter well suited to deliver tens of amperes in a very compact form factor, but it can also be easily paralleled and scaled up for use in applications requiring hundreds of amperes.

TABLE V: Summary of measured efficiency and power density results at various output voltages

Output voltage	Power stage efficiency	System efficiency (including driver loss)	Power density
2.5 V	Peak: 95.6% Full load: 92.1%	Peak: 95.0% Full load: 91.9%	494 W/in^3 196 W/in^2
2.0 V	Peak: 95.1% Full load: 91.3%	Peak: 94.3% Full load: 91.1%	395 W/in^3 157 W/in^2
1.8 V	Peak: 94.8% Full load: 90.9%	Peak: 94.0% Full load: 90.6%	356 W/in^3 141 W/in^2
1.5 V	Peak: 94.4% Full load: 89.9%	Peak: 93.3% Full load: 89.6%	296 W/in^3 118 W/in^2
1.2 V	Peak: 93.7% Full load: 88.1%	Peak: 92.4% Full load: 87.8%	237 W/in^3 94 W/in^2
1.0 V	Peak: 93.1% Full load: 86.8%	Peak: 91.5% Full load: 86.4%	198 W/in^3 79 W/in^2

Since all major components of the converter are packed into a small rectangular box, we are also able to directly compare with some of the best existing commercial power modules in this field. Although being the first proof-of-concept prototype without advanced packaging technologies, this work shows very comparable efficiency and current density performance. Note that the efficiency sweep of this work is obtained by slowly ramping up the load currents, and thus the switch resistance increases at heavy load due to higher switch temperature. In contrast, industry products are commonly tested under pulsed load conditions where the switch junction temperature is equal to the ambient temperature. Therefore, a higher efficiency number can be expected if the proposed

TABLE VI: Comparison of this work and existing hybrid SC works

Reference	Topology	Voltage ratio	Output current	Current Density	Efficiency	Notes
This Work	Hybrid 8-to-1 Multi-phase Doubler SC + two-phase Buck	48-to-1.5 V	65 A	198 A/in^3 (by box volume) 583 A/in^3 (by component volume)	System efficiency including driver loss: full load: 89.6% (I_{out}=32.5A/phase) heavy load: 91.4% (I_{out}=25A/phase) medium load: 92.4% (I_{out}=20A/phase) peak: 93.3% (I_{out}=13A/phase)	Total volume of the main power devices (switches, capacitors, inductors) is used for the "by component volume" current density calculation
LEGO PoL [13]	Hybrid 6-to-1 Dickson SC + 12-phase Buck	48-to-1.5 V	300 A	114 A/in^{3*} (by box volume)	Power stage efficiency:* full load: 87.7% (I_{out}=25A/phase) peak: 96.0% (I_{out}=4A/phase)	Current density is estimated with optimum vertical inductor stack-up
MIH [14]	Hybrid 4-to-1 Dickson SC + three-phase Buck	48-to-1.6 V	40 A	213 A/in^{3*} (by component volume)	Including *calculated* gate charge loss:* full load: 85.6% (I_{out}=13.3A/phase) peak: 93.9% (I_{out}=3.3A/phase)	Total component volume of main power devices (switches, capacitors, inductors) is used for density calculation
Crossed-coupled QSD Buck [15]	Hybrid 4-to-1 SC + two-phase Buck	48-to-1.5 V	40 A	100 A/in^3 (by component volume)	Power stage efficiency:* full load: 92.7% (I_{out}=20A/phase) peak: 95.1% (I_{out}=8A/phase)	The "by component volume" current density is estimated with the same method above

* According to direct correspondence with the author.

TABLE VII: Comparison of this work and existing commercial products

Reference	Topology	Voltage ratio	Output current	Current Density	System Efficiency	Notes
This Work	Hybrid 8-to-1 SC + two-phase Buck	48-to-1 V	65 A	198 A/in^3	full load: 86.4% 50 A: 88.7% peak: 91.5%	
ADI LTM4664 [8]	4-to-1 SC + two-phase buck	48-to-1 V	50 A	415 A/in^3	full load: 88.0% peak: 90.8%	Highly integrated power module
TI [9] LMG5200POLEVM	Transformer-based	48-to-1 V	50 A	N/A	full load: 87.7% peak: 90.7%	GaN FET
bel power stamp [10]	Transformer-based	48-to-1 V	70 A	167 A/in^3	Typical: 91%	Highly integrated power module, fixed output voltage
Vicor PRM [31] +2*VTM [32]	Buck-Boost + Sine Amplitude Converter	48-to-1 V	200 A	588 A/in^3	Typical: 90%	Highly integrated power module

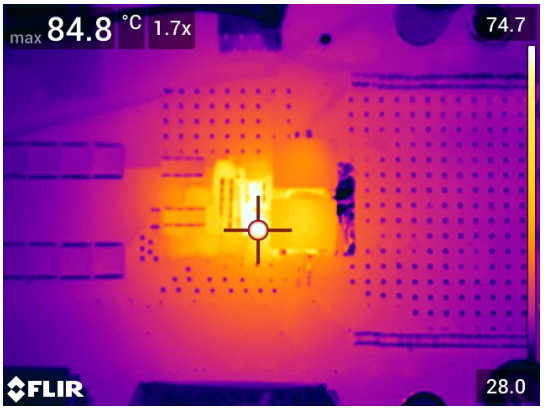


Fig. 8: Thermal performance at equilibrium with 110 CFM fan cooling only (V_{out} = 2.0 V, I_{out} = 65 A).

converter is tested under the same industry procedure. We also note that the current design has not been optimized, as the commercial off-the-shelf inductors (maximum height of 0.315 inch) are much taller than the other components (maximum height of 0.126 inch). Further optimization of the magnetic components (e.g. customized coupled inductors with PCB windings) and advanced 3D packaging technologies (e.g. board cutouts for recessing inductors) could dramatically improve the power/current density.

IV. Conclusions

This work presented a new hybrid topology with Multi-Level Binary (MLB) voltages on the flying capacitors that can simultaneously achieve high efficiency and power density for direct 48 V to PoL applications. The proposed MLB-PoL converter employs multiple operating phases to achieve 8-to-1 conversion ratio at the SC stage with the theoretical minimal number of components. This high SC conversion ratio can reduce the inductor volt-second stress of the following buck stage. Moreover, an inductor frequency multiplication effect is able to further reduce the inductor size without increasing the switching frequency of the SC stage. A 48 V to 2.5-1.0 V converter prototype with 65 A output current was built and tested. At 48 V to 2 V, the prototype achieved 95.1% peak efficiency (94.3% including gate drive loss) and 395 W/in^3 power density, demonstrating one of the best in-class performances.

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References

[1] R.Miftakhutdinov, "Improving System Efficiency with a New Intermediate-Bus Architecture," in *Texas Instruments Inc. Seminar*, 2009. [Online]. Available: http://www.ti.com/download/trng/docs/seminar/Topic_4_Rais.pdf

[2] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "48-v voltage regulator module with pcb winding matrix transformer for future data centers," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 12, pp. 9302–9310, Dec 2017.

[3] Z. Ye, Y. Lei, and R. C. N. Pilawa-Podgurski, "The cascaded resonant converter: A hybrid switched-capacitor topology with high power density and efficiency," *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4946–4958, 2020.

[4] Z. Ye, R. A. Abramson, and R. C. N. Pilawa-Podgurski, "A 48-to-6 v multi-resonant-doubler switched-capacitor converter for data center applications," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 475–481.

[5] W. C. Liu, Z. Ye, and R. C. N. Pilawa-Podgurski, "A 97% peak efficiency and 308 a/in3 current density 48-to-4 v two-stage resonant switched-capacitor converter for data center applications," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 468–474.

[6] W. C. Liu and R. C. N. Pilawa-Podgurski, "Bi-lateral energy resonant converter (berc) with merged two-stage inductor for 48-to-12v applications," in *2020 21th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2020, pp. 1–8.

[7] R. A. Abramson, Z. Ye, and R. C. N. Pilawa-Podgurski, "A high performance 48-to-8 v multi-resonant switched-capacitor converter for data center applications," in *2020 22nd European Conference on Power Electronics and Applications (EPE '20 ECCE Europe)*, 2020, pp. P.1–P.10.

[8] Analog Devices, *LTM4664 Data Sheet*, 2019. [Online]. Available: https://www.analog.com/media/en/technical-documentation/data-sheets/LTM4664.pdf

[9] Texas Instruments, *LMG5200POLEVM-10 User's Guide*, 2017.

[10] Bel Fuse Inc. , *48 V-TO-POL Power Stamp datasheet*, 2020. [Online]. Available: https://belfuse.com/resources/datasheets/powersolutions/ds-BPS-48-V-to-POL-power-stamp.pdf

[11] Vicro Inc., *Factorized Power Architecture and VI Chips White Paper*, 2013. [Online]. Available: http://www.vicorpower.com/documents/whitepapers/fpa101.pdf

[12] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "Single-stage high-efficiency 48/1 v sigma converter with integrated magnetics," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 1, pp. 192–202, 2020.

[13] J. Baek, P. Wang, Y. Elasser, Y. Chen, S. Jiang, and M. Chen, "Legopol: A 48v-1.5v 300a merged-two-stage hybrid converter for ultra-high-current microprocessors," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 490–497.

[14] R. Das, G. Seo, D. Maksimovic, and H. Le, "An 80-w 94.6%-efficient multi-phase multi-inductor hybrid converter," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 25–29.

[15] M. Halamicek, T. McRae, and A. Prodić, "Cross-coupled series-capacitor quadruple step-down buck converter," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2020, pp. 1–6.

[16] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 23, no. 2, pp. 841–851, March 2008.

[17] Y. Lei and R. C. N. Pilawa-Podgurski, "A general method for analyzing resonant and soft-charging operation of switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5650–5664, Oct 2015.

[18] Z. Ye, S. R. Sanders, and R. C. N. Pilawa-Podgurski, "Modeling and comparison of passive component volume of hybrid resonant switched-capacitor converters," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–8.

[19] R. C. N. Pilawa-Podgurski, D. M. Giuliano, and D. J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," in *2008 IEEE Power Electronics Specialists Conference*, June 2008, pp. 4008–4015.

[20] A. Lidow, "Powering graphics processors from a 48-v bus," 2019. [Online]. Available: https://www.powerelectronictips.com/powering-graphics-processors-from-a-48-v-bus/

[21] M. H. Ahmed, F. C. Lee, and Q. Li, "Two-stage 48v vrm with intermediate bus voltage optimization for data centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2020.

[22] T. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltage-source inverters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE*, 1992, pp. 397–403.

[23] Y. Lei, C. Barth, S. Qin, W. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kw single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[24] M. S. Makowski, "Realizability conditions and bounds on synthesis of switched-capacitor dc-dc voltage multiplier circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 44, no. 8, pp. 684–691, Aug 1997.

[25] I. Oota, F. Ueno, and T.Inoue, "Analysis of a switched-capacitor transformer with a large voltage-transformer-ratio and its applications," *Electronics and Comm. in Japan, Part 2*, vol. 73, no. 1, pp. 85–96, 1990.

[26] J. A. Starzyk, Ying-Wei Jan, and Fengjing Qiu, "A dc-dc charge pump design based on voltage doublers," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 48, no. 3, pp. 350–359, March 2001.

[27] P. S. Shenoy, O. Lazaro, M. Amaro, R. Ramani, W. Wiktor, B. Lynch, and J. Khayat, "Automatic current sharing mechanism in the series capacitor buck converter," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2015, pp. 2003–2009.

[28] G. Seo, R. Das, and H. Le, "Dual inductor hybrid converter for point-of-load voltage regulator modules," *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 367–377, Jan 2020.

[29] G. Roberts, T. McRae, and A. Prodić, "A multiphase series-capacitor buck converter with reduced flying capacitor volume and auxiliary start-up circuit," in *2019 21st European Conference on Power Electronics and Applications (EPE '19 ECCE Europe)*, Sep. 2019, pp. P.1–P.8.

[30] Z. Ye, Y. Lei, W. Liu, P. S. Shenoy, and R. . Pilawa-Podgurski, "Improved bootstrap methods for powering floating gate drivers of flying capacitor multilevel converters and hybrid switched-capacitor converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, 2020.

[31] Vicro Inc., *PRM48AH480x200A00 Data Sheet*, 2020. [Online]. Available: http://www.vicorpower.com/documents/datasheets/PRM48AH480T200A00_ds.pdf

[32] ——, *VTM48MP010x107AA1 Data Sheet*, 2017. [Online]. Available: http://www.vicorpower.com/documents/datasheets/VTM48M_010_107AA1.pdf