

# UC Berkeley

## Energy Use in Buildings Enabling Technologies

### Title

Reliable Fully Integrated Radios for DR

### Permalink

<https://escholarship.org/uc/item/9cp046rz>

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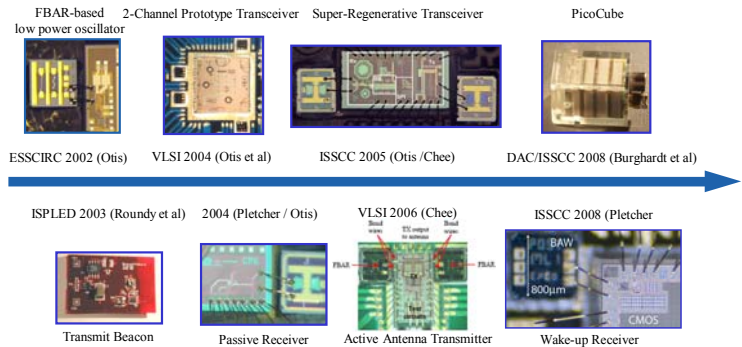
et al.

### Publication Date

2008

## Vision

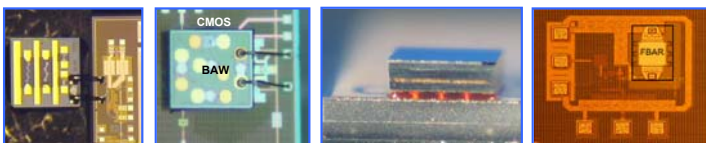
- Economical integration of CMOS and FBAR technology to achieve low cost, reliable, ultra-low power radios for DR applications
- Why FBAR?
  - provide highly accurate high Q resonance at RF
  - can be used for frequency references and RF filters
  - low power and low insertion loss due to high Q
  - small form factor
  - possible candidate to replace quartz (for frequency references) or bulky SAW (for filter applications)



## Methods

- Extending Avago Technologies' microcapping packaging technique for FBARs to include CMOS to achieve low-cost integrated solutions
- Since this integration happens at wafer level, circuits need to be designed in compatible 0.4 um CMOS
- Test chips and test structures were designed to characterize RF performance of the CMOS process
- Novel circuit architectures such as interpolative oscillators or difference oscillators were implemented to enhance reliability of FBAR based circuits while keeping the power consumption low

(pictures courtesy by B. Otis)



M. Aissi et al., ISSCC'06



courtesy: R. Ruby, Avago Technologies

## Research Questions

- Does the compatible CMOS process provide the required performance at RF (2 GHz)?
- Is the approach of integrating CMOS and FBAR technology at wafer level technological and economical feasible?
- Do the new building blocks provide the improvements we are hoping for?
- What new doors open once the large scale integration of CMOS and FBAR is possible?

## Findings

- The 0.4 um CMOS process is capable of doing designs at RF (2 GHz)
- The models available for that process are also fairly accurate at these frequencies, although there are still some open issues which might be related to problems in the simulation models
- First set of CMOS test circuits work, further building blocks currently in testing phase
- From a CMOS perspective everything is ready to go to continue the large scale integration effort

