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Towards Intrinsic Switching in Ferroelectric Oxide –

Materials Synthesis and Fabrication Process

By

Yizhe Jiang

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering - Materials Science and Engineering

in the

Graduate Division

of the

University of California, Berkeley

Committee in Charge:

Professor: Lane W. Martin, Chair

Professor: Ramamoorthy Ramesh

Professor: Jeffrey B. Neaton

Fall 2023

Towards Intrinsic Switching in Ferroelectric Oxide –
Materials Synthesis and Fabrication Process

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Abstract

Towards Intrinsic Switching in Ferroelectric Oxide –

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Doctor of Philosophy in Engineering - Materials Science and Engineering

University of California, Berkeley

Professor Lane W. Martin, Chair

This dissertation presents a systematic study on idealized electrode/ferroelectric/electrode heterostructures, from film synthesis to capacitor fabrication. Single crystal $BaTiO_3$ has shown a small switching field of ~ 1 kV cm^{-1} and small switching energy of ~ 0.1 J cm^{-3}, making it an excellent candidate for next generation non-volatile ferroelectric applications. However, when $BaTiO_3$ is incorporated into actual nanoscale devices, the ferroelectric properties get significantly worse. $BaTiO_3$ thin films show either large coercive switching field, increasing the total power consumption, or diminished remanent polarization, putting non-volatility into question. In this dissertation, I demonstrate that by carefully controlling the O_2 growth pressure in pulsed laser deposition process, we can synthesize $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures with $BaTiO_3$ ferroelectric properties comparable to bulk crystal. Thickness scaling is performed to explore the smallest coercive voltage, with $BaTiO_3$ films with thicknesses ranging from 25-50 nm exhibiting best combinations of switching voltage (< 100 mV), switching energy (< 2 J cm^{-3}) and remanent polarization (> 10 μC cm^{-2}). Depolarization field is found to play an important role in suppressing the coercive field, leading to a deviation in coercive field scaling from the Janovec-Kay-Dunn law. Lateral scaling is performed to explore the fastest switching speed, with the projection of achieving sub-nanosecond switching time in capacitor sizes as small as ~ 10 μm^2. Integration of $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures onto silicon substrate is also shown, with similar switching behavior achieved, as well as good resistance to fatigue and retention. Besides heterostructure synthesis, different fabrication methods are also explored to bring out the best $BaTiO_3$ capacitor performance in various ferroelectric functions. MgO hard mask process introduces surface defects at electrode/ferroelectric interface and results in a large imprint in the hysteresis loops. While the wet chemical etching method gives out idealized ferroelectric loops with almost no imprint, the high selectivity and isotropy makes it unsuitable for fabricating more complex device architectures with high precision. The ion mill methods, on the other hand, have better directionality and can be used to etch almost every type of material and fabricate advanced device structures. However, the Ar^+ ion beam bombardment can result in horizontal imprints in the hysteresis loop. Transport studies and deep-level transient spectroscopies reveal the introduction of Ba-related defect types ($V_{Ba}'' - V_O^{\bullet\bullet}$, V_{Ba}'') during the milling process. Post-fabrication annealing in Ba-rich environment significantly lowers the defect levels and reduces the imprints. We also discuss what can be done to further optimize the ferroelectric properties (reducing coercive field, increasing remanent polarization, etc.) in ultrathin $BaTiO_3$ films, for the ferroelectric material to function well for various application purposes.

To my parents for your unconditional love

To all my friends for your generous support

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Acknowledgements - I

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Chapter 1

Introduction and Motivation

This chapter provides the reader a brief introduction of the technological background in complementary metal-oxide-semiconductor (CMOS) scaling and the motivation for exploiting new physical parameters for next-generation switching applications. The discussion will start with a review of Moore's law and Dennard scaling in traditional metal-oxide-semiconductor field-effect transistors (MOSFETs), followed by various limitations to such scaling trend. This will, in turn, lead to an exploration of the new physical parameters to supplement (or replace) traditional electron-and-energy-barrier-based MOSFET switches, opening a new field called beyond-CMOS switching systems in both academia and industry. From there, the chapter will focus on and introduce ferroelectric materials, whose polarization can used as a computational state variable in multiple ferroelectric switching devices, which is one of the categories in the beyond-CMOS technology family. Finally, an outline of the dissertation is given at the end of the chapter.

1.1 Trends in traditional MOSFET scaling

The invention of transistors was one of the most important technical developments of the 20th century and a tremendous revolution for mankind[1]. The fast working speed, low power consumption and high reliability of the transistors have made them fundamental components for integrated circuit[2], which can be mass manufactured and are being used in almost every electronic equipment nowadays[3]. In the meantime, with the advances in semiconductor fabrication technologies, for decades, researchers have been able to fit more and more transistors on chips of the same size. In 1965, Gordon E. Moore proposed the now famous "law" predicting that the number of transistors on a microchip should double every 18 to 24 months[4]. This leads to an exponential increase in transistor densities over time, as well as a reduction in transistor sizes. Although the prediction was made based on merely six year's data (1959-1965), the law held tremendously well, spanning different technology generations[5], and have become the driving force behind the development of modern computing (Fig. 1.1).

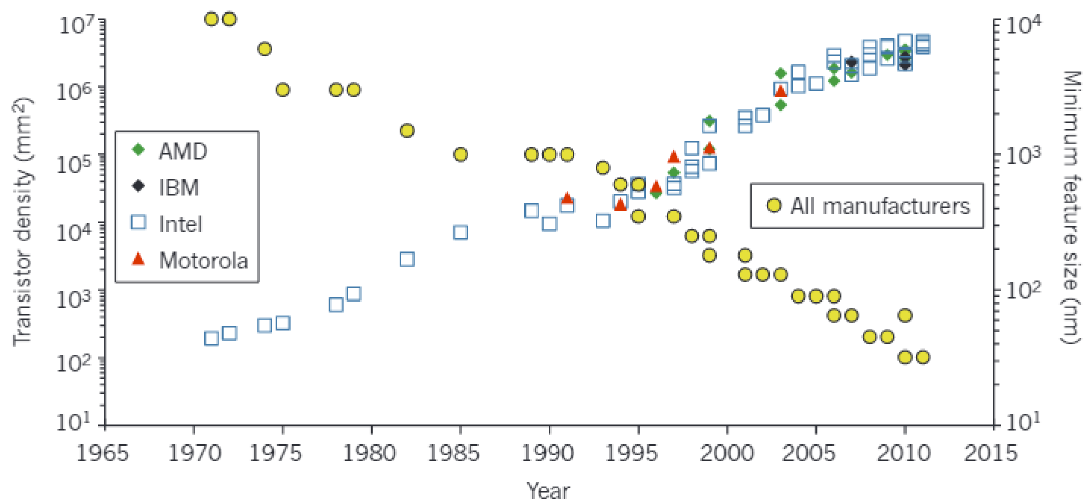


Figure 1.1 | Moore's law in metal-oxide-semiconductor integrated circuits. Following an exponential relation, the minimum feature size (gate length) in a transistor decreases with time (yellow circles, right y axis), while the density of transistors per chip increases with time (diamonds, triangles and squares, left y axis). Adapted from ref. [5].

Besides an increase in transistor densities per area described by Moore's law, in 1974, Robert H. Dennard proposed another seminal law on other benefits that transistor scaling can (and should) bring[6]. This MOSFET scaling rule, also known as the Dennard scaling law, describes how simultaneous improvements in transistor density, switching speed, and power dissipation can be obtained[7]. Between every technology node, the switching delay of a MOSFET will be reduced, leading to increased working speed (*i.e.*, clock frequency). In the meantime, while the number of transistors on the chip increases, the total power consumption per unit area (*i.e.*, power density) remains the same. This is possible because smaller transistors can switch on and off faster than larger transistors, and they (should) also require less power to operate, thus enabling the development of faster and more energy-efficient computer chips[8].

1.2 Limitations in MOSFET scaling

For many years, MOSFET scaling worked well and allowed the semiconductor industry to continue to improve chip performance. However, as transistor sizes have continued to shrink, instead of operating at a constant power density, the actual power consumption per mm^2 on the chips has increased significantly (blue curve, Fig. 1.2a), leading to a deviation from the Dennard scaling law around 2003[9]. Moreover, the trend in operating voltage reduction has also begun to slow down - if the Dennard scaling were strictly followed (blue line, Fig. 1.2b) through today, people would have achieved a drive voltage in the vicinity of 100 mV (as opposed to the 500-600 mV we use today). In reality, the operating voltages of computing devices nowadays (high performance logics, green line; low-power devices, red line, Fig. 1.2b) are much higher[10]. A lot of factors could lead to the failure of the Dennard scaling law, including the subthreshold slope (*SS*), leakage power waste, as well as physical doping limits in the substrates.

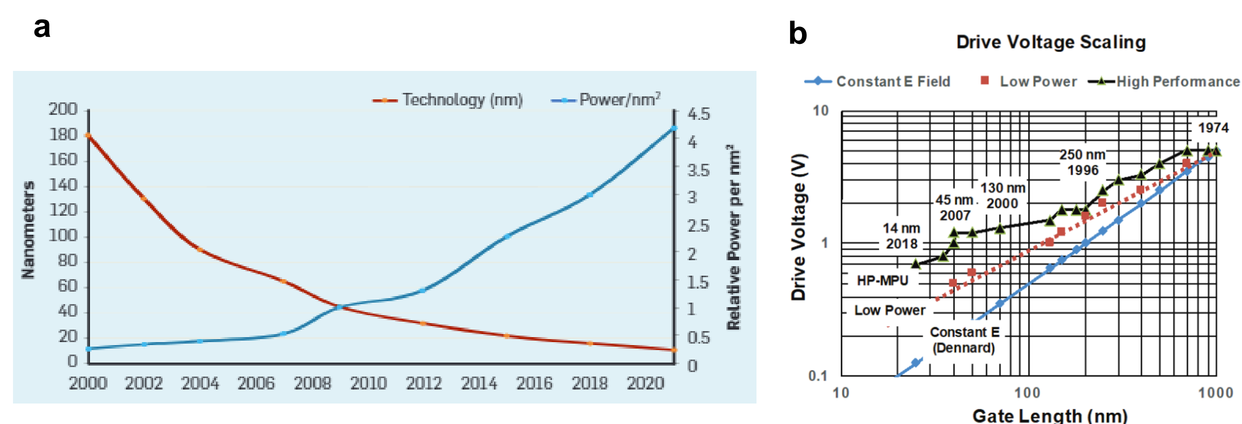


Figure 1.2 | Breakdown of Dennard scaling. a, Power density per mm^2 on the chip increases significantly over time. **b**, Voltage scaling has slowed down for both high-performance logic and low-power devices. Adapted from ref. [9,10].

One of the key factors that limits the voltage scaling in Dennard's law is the subthreshold slope (SS). In a MOSFET, when the gate voltage, V_G, is below the threshold voltage, V_{th}, the drain current, I_D, increases exponentially with the gate voltage[5]. The inverse of the slope in the logarithmic region, *1/slope*, is defined as the subthreshold slope (SS), a parameter characterizing the rate of increase in the current below the subthreshold voltage, and can be expressed by

$$SS = \frac{dV_G}{d(\log(I_D))} \qquad \text{Equation 1.1}$$

which has the unit of *mV/decade of current*. The subthreshold slope, *SS*, can also be expressed as[11]

$$SS = (\ln(10))\frac{k_B T}{q}n \qquad \text{Equation 1.2}$$

where k_B is the Boltzmann constant, T is the temperature in Kelvin, q is the charge of an electron, and n is the body factor characterizing the coupling between gate voltage and the channel region (*i.e.*, $n = 1$ for ideally coupled gate and channel region). At room temperature ($T = 298\ K$), we will have

$$SS_{minimum} = 59.1\ mV\ decade^{-1} \qquad \text{Equation 1.3}$$

This value has set a fundamental physical limit to the voltage scaling in Dennard's law - at least 59 mV has to be applied to the gate to increase the channel current by one decade (a factor of 10). To make things worse, because of the imperfect coupling between the gate and the channel region, the body factor, n, is usually larger than 1, causing the required supply voltage to be even larger[5]. Because this limiting factor, SS, originates from the Boltzmann distribution of electrons inside semiconductor bands, it is also called the Boltzmann tyranny[11].

As the size of the transistor decreases, the leakage current can also increase significantly, leading to an extra loss of power[2]. These leakage currents come from multiple sources, including short channel effect (*i.e.*, the shortening of effective channel length leading to weakened gate control, decreased threshold voltage, increased SS, and therefore, an increased off-current)[5], gate leakage (*i.e.*, the quantum tunneling of charge carriers across the gate oxide, which is reported to increase ~30 times between every technology node[12]), etc.

In addition, the doping of the substrate will also be a problem. In Dennard scaling, the doping level of the substrate needs to be increased between every technology generation. However, if the doping concentration in the channel is too high, not only the carrier mobility will degrade due to increased impurity scattering, but also the band-to-band tunneling at the junctions will increase, leading to larger source and drain leakage and lowering the performance of the integrated circuits[7].

1.3 Beyond-CMOS switching devices

To overcome the Boltzmann tyranny which sets an inevitable boundary on how low the gate voltage can go on a MOSFET, new materials, new computational state variables and new switching mechanisms must be explored as a supplement or replacement for the traditional CMOS-based switching system, and to maintain Moore's rate of transistor integration. These new, alternative types of devices are generally named beyond-CMOS switching devices[13].

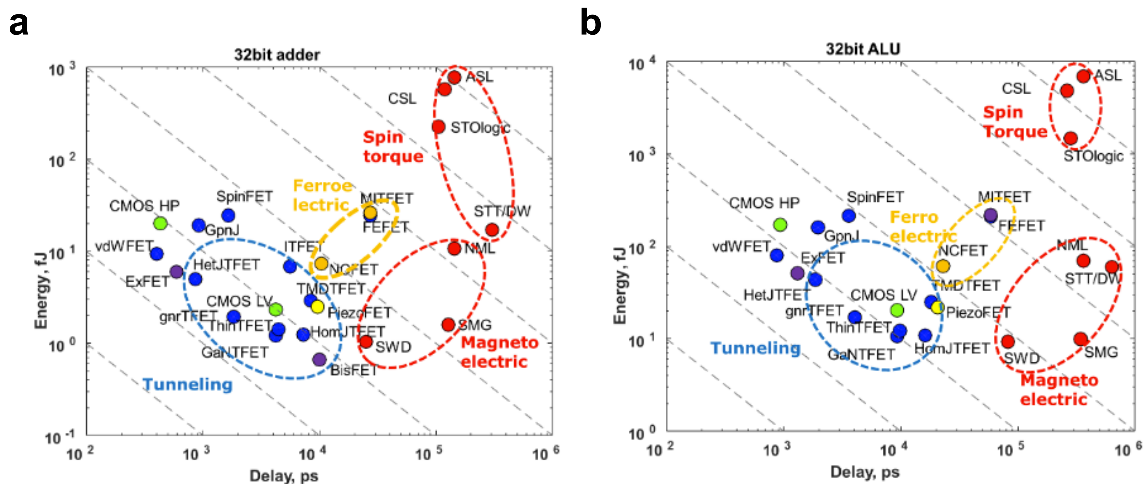


Figure 1.3 | Benchmarking of beyond-CMOS switching systems. Switching energy versus switching delay for **a**, 32-bit adder and **b**, 32-bit arithmetic logic unit (ALU). Adapted from ref. [15].

Since the beginning of the 2010s, there has been research both in academia and industry for the purpose of investigating and demonstrating feasible alternatives to CMOS. These beyond-CMOS switching devices use non-charge-based physical parameters, such as spin, magnetization, polarization, exciton, plasmon, strain as the data "tokens" to capture and transfer information[13-15]. As a result, different categories of beyond-CMOS devices have been proposed and fabricated, such as spintronics[16-18], orbitronics[14,19,20], straintronics[21], ferroelectric devices[11,22]. Also, tunneling FETs (TFETs) are another type of beyond-CMOS device based on tunneling of electrical charge which are also being investigated to bypass the Boltzmann tyranny[23]. While it is sometimes difficult to make direct comparisons between these devices to assess which one works best, because these devices work on distinct physical principles, there are some general criteria for benchmarking these devices. Specifically, there are quantitative metrics for evaluation usually including the switching time, switching energy, scalability, etc[13]. Since 2010, a few benchmarking studies have been made to assess the performance of different categories of beyond-CMOS switching systems[13-15] (Fig. 1.3a,b).

1.4 Ferroelectrics in beyond-CMOS technology

Among non-volatile beyond-CMOS devices (*i.e.*, computation state variables are magnetization, polarization, strain, etc), devices based on ferroelectrics, which take advantage of the switchable polarization as the computation variable (yellow circle, Fig. 1.3a, b), are one of the most promising classes that has the best performance. Ferroelectric transistors switch faster than most spintronic devices and have much lower switching energies than spin-transfer-torque-based devices (Fig. 1.3a, b). This makes ferroelectric materials and ferroelectric devices interesting objects to investigate.

1.4.1 Roadmap for ferroelectric materials

A ferroelectric material has a spontaneous polarization and has (at least) two stable and degenerate polarization states at zero field. The spontaneous polarization results from the displacement of certain ions (or polar polymer dipole chains in organic compounds) from their charge-neutral position, and ferroelectric materials are non-centrosymmetric in terms of lattice symmetry[24]. The magnitude of the spontaneous polarization is called the remanent polarization, P_R. Degeneration between two polarization states can occur and these different polarization states can be switched to each other by applying an external electric field larger than the coercive field, E_C.

The first discovery of ferroelectricity was in an organic molecular crystal, Rochelle salt, in 1921[25]. Later in 1935, ferroelectricity was discovered in an inorganic salt, KH_2PO_4[26]. However, these materials are too water sensitive to be of practical use. In the 1940s, ferroelectricity was reported in perovskite oxide $BaTiO_3$[27]. Because perovskite material is more chemically stable, it opened the door for additional studies on ferroelectric materials including explorations to use them in devices[28], illuminating new ways for electronic design concepts such as ferroelectric random access memories (FeRAMs), ferroelectric field effect transistors (FeFETs) and ferroelectric tunneling junctions (FTJs)[29-31]. The discovery of ferroelectricity in another perovskite material, $PbZr_xTi_{1-x}O_3$, was made in the 1950s[32]. Compared to $BaTiO_3$, $PbZr_xTi_{1-x}O_3$ has a much stronger polarization and piezoelectric coefficient, and the mixture of zirconium and titanium ions sitting on the *B*-site of the perovskite structure also brings additional chemical-tunability into the

ferroelectric material. However, at the time, the fatigue issue (*i.e.*, the reduction of remanent polarization during electrical cycles) caused a huge problem in $PbZr_xTi_{1-x}O_3$ films which has to some extent limited the development of $PbZr_xTi_{1-x}O_3$-based ferroelectric devices[26]. Later in 1990s, a layered perovskite, $Sr_2Bi_2Ta_2O_9$ was introduced. Because of the more complexed structure of $Sr_2Bi_2Ta_2O_9$, it can permit temporal dynamics of space charge and smooth out oxygen-gradient concentration near the electrode, thus avoiding the excessive charge accumulation at the electrode/ferroelectric interface, which contributes to the fatigue issue that shows up in $PbZr_xTi_{1-x}O_3$[33]. Around the same time, people discovered that by using oxide electrodes such as $SrRuO_3$, IrO_2 and RuO_2, the space charge problems near the ferroelectric/electrode interface can also be mitigated and the fatigue performance can be largely improved for ferroelectric perovskites[33-35]. Albeit with the success to solve the fatigue problem in ferroelectric oxides, the difficulty in integrating these perovskite materials into CMOS technology (*e.g.*, poor crystal quality, loosely bonded oxygen[26]) still posed a great challenge to the complete commercialization of ferroelectric based devices. The discovery of ferroelectricity in silicon-doped HfO_2 was reported in 2011[36]. By this time, HfO_2 has already been used as a gate oxide material in MOSFET[35,37], and has been successfully incorporated into the CMOS technology[26,38] due to its great compatibility[26,39]. Most recently, ferroelectricity was also reported in wurtzite-structured $Al_{1-x}Sc_xN$[40]. While $Al_{1-x}Sc_xN$ has long been used in MEMS technology for its large piezoelectricity since 2010s[41], the ferroelectricity was not observed until in 2019 because of its high coercive field (*i.e.*, larger than the dielectric breakdown field)[40,42]. Ferroelectric $Al_{1-x}Sc_xN$ has a much higher P_R than HfO_2, and can also be grown at a much lower temperature in physical vapor deposition, making it an attractive candidate in CMOS integration processes[26,43]. A timeline for the evolution of ferroelectric materials and relevant ferroelectric devices was shown in Fig. 1.4.

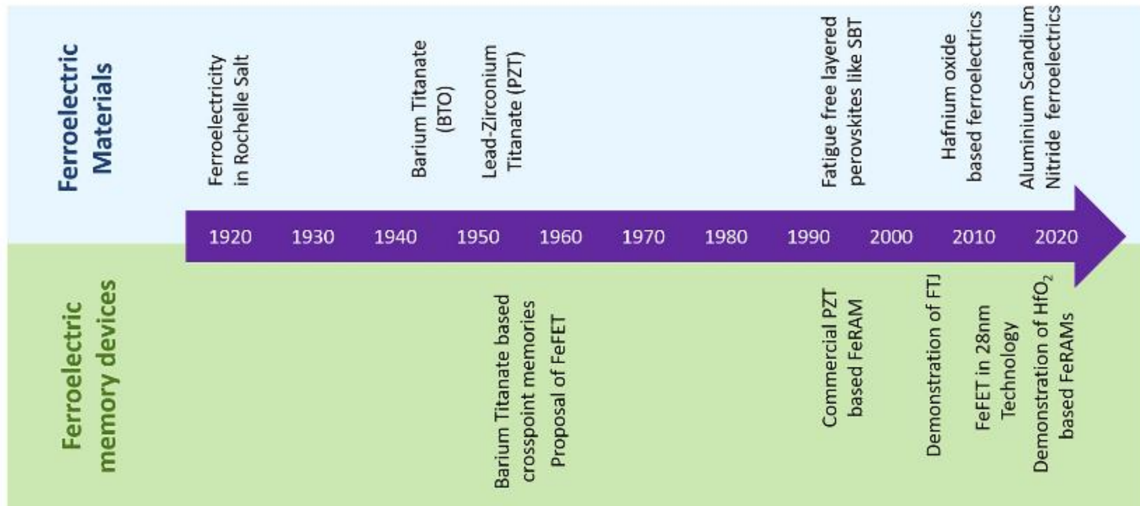


Figure 1.4 | Timeline of the evolution in ferroelectric materials and ferroelectric memory devices. Adapted from ref. [26].

To be noted, coupling between ferroelectric polarization and other different data "token"s can also occur in certain material systems. *E.g.*, ferroelectric order is coupled with (anti)ferromagnetic order in multiferroic materials, such as $BiFeO_3$. The magnetoelectric switching in multiferroics can also be combined with other physical phenomena (*e.g.*, spin-orbit transduction) to realize other types of beyond-CMOS logic functions, such as the magnetoelectric spin-orbit devices[44].

1.4.2. Ferroelectric devices

The polarization in the ferroelectrics can be used as a computational state variable to store information. However, to achieve functionality of ferroelectric materials in actual electronic devices, one needs to find ways to readout the digital information stored by the electric dipole[24]. Generally, three ways and corresponding architectural designs can be used to achieve this goal. The first and easiest way is to measure the charge-related current flow in the outside circuit when the ferroelectric materials switches. This type of readout method requires the construction of an electrode/ferroelectric/electrode capacitor structure and is typically used in FeRAMs. Ferroelectric layers are sandwiched between two electrodes, and transistors can be added to the ferroelectric capacitor to form a transistor/capacitor configuration, mimicking the structure of traditional dynamic random-access-memory[24]. FeRAMs can be used in a wide range of niche applications, including energy meters, wearable medical devices and microcontroller code storages[45].

FeFETs are another architectural design to convert the dipole moment information into electric signals, where the oxide layer in the traditional MOSFET structure is replaced by a ferroelectric layer. In FeFETs, the ferroelectric dipole dynamics are strongly coupled to the charge conductance in the semiconductor channel. The change in the direction of polarization in the ferroelectric layer will lead to a shift in the threshold voltage which can be measured in the outside circuits[24,46]. Compared to the capacitor-based FeRAM, the FeFET structure offers a non-destructive read-out process, and combines the memory function and the logic function, forming the “logic-in-memory” architecture. This combined device structure can be used to overcome the memory-logic interconnect bottleneck in traditional von Neumann architectures[45]. FeFETs can also serve as fundamental components in other functional architectures, including analogue weight cells for deep neural networks and low-power negative-capacitance field-effect transistors, providing a pathway to massive data processing with high throughput and energy efficiency[11,47,48].

The third design type to readout the ferroelectric dipole information is used in FTJs. An FTJ consists of an ultra-thin ferroelectric layer sandwiched between two different metal electrodes, where electrons can tunnel straight through the ferroelectric gap[49]. Because of the asymmetry in the electrode configuration, the screening lengths in two electrodes are different, inducing a tunneling barrier in the ferroelectric layer that can be modified by the direction of ferroelectric dipoles. By measuring the tunneling current through the ferroelectric junction in the outside circuit, the polarization direction stored as one-bit binary information (*i.e.*, *0* or *1*) can be obtained[50]. The FTJ usually operates on small tunneling current density and can be used in massive parallel operations and synapse fabrications for neuromorphic computing systems[51,52].

1.5 Organization of dissertation

This dissertation is organized as follows:

Chapter 1, as has been seen, serves as the introduction on the background and motivation related with this study. The chapter starts with the classic Moore’s law and Dennard’s law describing MOSFET scaling in traditional semiconductor industry. Then limitations in this scaling trend is discussed and the concept of beyond-CMOS switching is introduced. This chapter closes with the role that ferroelectric materials and devices can play in advanced beyond-CMOS technology.

Chapter 2 begins with a brief introduction about the materials that are studied in this thesis, namely, the oxide electrode, strontium ruthenate ($SrRuO_3$), and the ferroelectric oxide, barium titanate ($BaTiO_3$). Then the historical challenges in synthesizing idealized $BaTiO_3$ thin films are discussed. This is followed by a discussion of epitaxial heterostructure physics, and the synthesis methods to grow these materials are provided.

Chapter 3 offers a detailed description of the characterization methods that are performed on the relevant heterostructures, including characterization of the structural, dielectric, and ferroelectric properties, as well as fatigue and retention measurements to assess their performance as in ferroelectric devices. Transport measurement and deep-level transient spectroscopy are also discussed to characterize the intra-bandgap charge trapping states in the materials.

Chapter 4 discusses the effect of growth pressure on the $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructure properties, that is, by carefully adjusting the growth pressure, the heterostructures can be made with high crystallinity, and have ferroelectric properties comparable to those observed in bulk crystal. By doing thickness scaling and lateral scaling, the study explores the smallest switching voltage, lowest switching power and fastest switching speed in $BaTiO_3$ capacitors. Finally, integration of $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures onto Si substrate is demonstrated and fatigue and retention experiments are performed to assess the performance of Si-based $BaTiO_3$ capacitors.

Chapter 5 explores the effect of fabrication processes on the $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures. *Ex situ* MgO hard mask processes and *in situ* growth-and-etching processes are discussed. For the *in situ* processes, wet-chemical etching and dry-ion milling are performed and the results are compared. The milling depth can influence the amount of defects that are introduced into the $BaTiO_3$ capacitors during the process, and affect the imprint in the PE loops. Finally, post-fabrication annealing in a Ba-rich environment is performed on the fabricated capacitors, showing the ability to reduce the defect levels and the imprints.

Chapter 6 serves as a conclusion of the studies presented in this dissertation and offers the readers with directions where efforts can be made to further optimize the ferroelectric properties in $BaTiO_3$ films to enable their applications in real-life devices.

Chapter 2

Synthesis of Epitaxial Complex-Oxide Materials

This chapter provides a brief introduction of the properties of the model materials that are studied in this thesis, including the conducting complex oxide electrode strontium ruthenate ($SrRuO_3$) and the classic ferroelectric oxide barium titanate ($BaTiO_3$). Challenges are also discussed regarding producing $BaTiO_3$ thin films with comparable properties with $BaTiO_3$ single crystals. Following is a detailed discussion about the basics in heterostructure synthesis, including the concept of lattice mismatch between substrate and films, as well as the synthesis processes (*i.e.*, pulsed-laser deposition) used to produce such thin films.

2.1 Material model systems

2.1.1 $SrRuO_3$

Strontium ruthenate ($SrRuO_3$), is a common complex oxide perovskite first known for its itinerant ferromagnetism below its Curie temperature of ~160 *K*[53]. Later, the transport properties in $SrRuO_3$ have also drawn researchers' attention[54]. Because of the relatively good conductivity in $SrRuO_3$ thin films without the need for chemical alloying, it is one of the most common complex oxides that is used as an electrode material in heterostructures. Also, it has good lattice mismatch with a wide range of substrates and functional oxides which makes it relatively easy to incorporate $SrRuO_3$ in epitaxial film stacks. The relatively good chemical stability of $SrRuO_3$ also offers benefits to the synthesis and characterization of the relevant heterostructures[55].

At room temperature, the $SrRuO_3$ structure (*i,e.*, in the bulk) has orthorhombic symmetry with lattice parameters $a = 5.5670$ Å, $b = 5.5304$ Å, and $c = 7.8446$ Å (Fig. 2.1a). A pseudocubic form of the $SrRuO_3$ unit cell can be described as well (thick black lines, Fig. 2.1a), where all three axes have almost the same lengths ($a_{pc} \approx 3.93$ Å)[56].

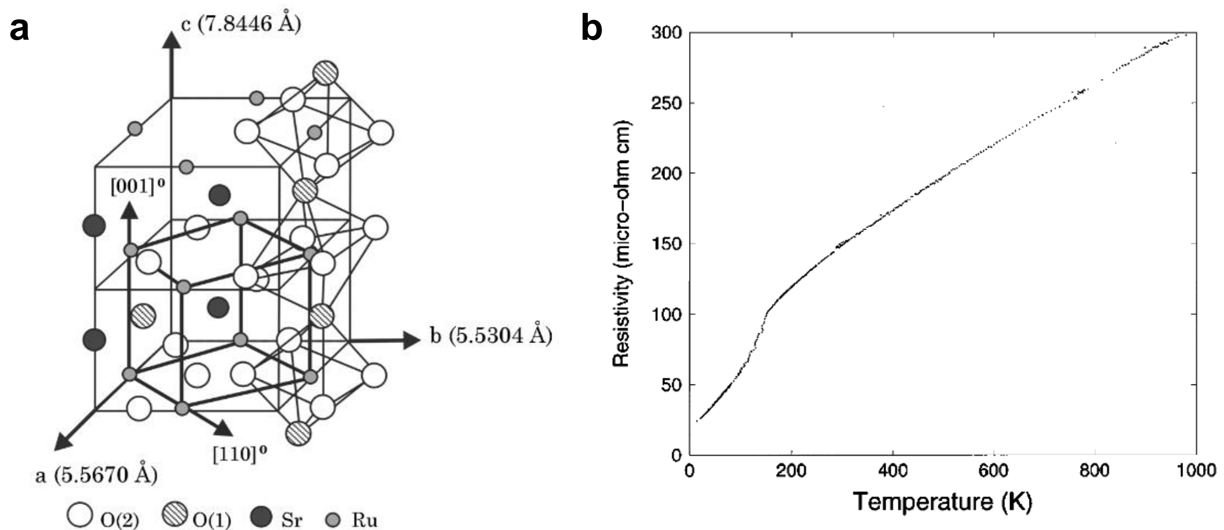


Figure 2.1 | Properties of $SrRuO_3$. a, Crystal structures of $SrRuO_3$ lattice. Thin black lines represent the orthorhombic lattice cell, and the thick black lines represent the pseudocubic unit cell. **b**, Resistivity of $SrRuO_3$ as a function of temperature. Adapted from ref. [55].

As an electrode material, and like many other metals, the resistivity of $SrRuO_3$ increases with temperature (Fig. 2.1b). At high temperatures ($T > 500$ *K*), the resistivity of $SrRuO_3$ increases beyond the Ioffe-Regel limit and the material behaves like a "bad metal"[57,58]. At low temperatures ($T < 15$ *K*), $SrRuO_3$ behaves like a Fermi-liquid, where conventional metallic behavior can be observed[59]. The drop in resistivity at $T = 160$ *K* corresponds to the ferromagnetic transition[55].

$SrRuO_3$ can be readily grown via a variety of deposition techniques on substrates with a wide range of lattice parameters (*e.g.*, $SrTiO_3$, $DyScO_3$, $GdScO_3$)[60]. Growing on different substrates will induce different strain states in the $SrRuO_3$ thin films[55]. For example, if the $SrRuO_3$ is grown on

$SrTiO_3$ (001) substrates (*i.e.*, a = 3.905 Å, ε_s = -0.59%), then it will be in the compressive strain state. If the $SrRuO_3$ is grown on $DyScO_3$ (110) substrates (*i.e.*, a_{pc} = 3.940 Å, ε_s = +0.41%) and $GdScO_3$ (110) substrates (*i.e.*, a_{pc} = 3.964 Å, ε_s = +0.97%), then it will be in the tensile strain state. Previous studies have shown that the strain state impacts the symmetry, as well as the electronic and magnetic behavior of $SrRuO_3$ films[60]. $SrRuO_3$ films grown epitaxially on $SrTiO_3$ (001) adopt orthorhombic crystal structure and have low resistivity. On the contrary, $SrRuO_3$ films epitaxially grown on $DyScO_3$ (110) and $GdScO_3$ (110) adopted a more symmetric "tetragonal" crystal structure and have higher resistivity[60,61]. This can be interpreted by understanding that the strain drives changes in the Ru-O-Ru bond angles, which is related to the bandwidth of the material[55]. Albeit with the slight reduction in conductivity resulted from the tensile strain when grown on $DyScO_3$ (110) and $GdScO_3$ (110) substrates, $SrRuO_3$ is still considered as a good complex oxide metal for these scandate substrates and is widely used as electrode materials in ferroelectric capacitors based on these substrates[62-64].

2.1.2 $BaTiO_3$

$BaTiO_3$ is another member in the perovskite family. It was first synthesized during a study focused on doping BaO into TiO_2 in 1941[65]. In the beginning, $BaTiO_3$ was used as a ceramic material for its high dielectric constant at room temperature (Fig. 2.2). Later in 1945, ferroelectricity was demonstrated in $BaTiO_3$, making it the first reported metal oxide to show ferroelectric behavior[66]. The ferroelectricity in $BaTiO_3$ results from the displacement of the center titanium cation from its balancing position (*i.e.*, the body center of the cubic perovskite unit cell). $BaTiO_3$ can exhibit multiple phase types depending on temperature (Fig. 2.2), with the titanium cations deviating along different directions (*i.e.*, the directions of polarization)[67]. Starting from low temperature, the polarization direction of the $BaTiO_3$ is along the body diagonals of the perovskite unit cell, resulting in a rhombohedral symmetry (*i.e.*, P_S // [111]). As the temperature increases, at around 190 K (-83 °C), the $BaTiO_3$ transforms into an orthorhombic structure with the polarization along the face diagonal of the perovskite cell (*i.e.*, P_S // [011]). Further increasing the temperature will result in a phase transition into a tetragonal symmetry with polarization direction pointing along one of the major axes of the perovskite cell (*i.e.*, P_S // [001]) at around 280 K (7 °C). Finally, at a temperature higher than 400 K (127 °C) the ferroelectricity in $BaTiO_3$ will vanish and a totally symmetric, cubic crystal structure will form (*i.e.*, P_S = 0). This phase of the $BaTiO_3$ is also called the paraelectric phase. At around phase transition temperatures, dielectric constant will be greatly increased, which is the typical behavior of a first order ferroelectric phase transformation[68,69].

At room temperature, the $BaTiO_3$ single crystal has tetragonal phase (a = 3.992 Å, c = 4.036 Å), and the direction of the polarization is along the c axis. When an electric field is applied to the $BaTiO_3$ crystal, it undergoes polarization switching via a nucleation and growth process wherein needle-like domains with opposite polarization first nucleate at the surface of the crystal, propagate across the material, and then grow laterally through the material to complete the switching event[70,71]. The polarization versus electric-field loop (P-E loop) are measured for $BaTiO_3$ single crystals and $BaTiO_3$ ceramics[72] (Fig. 2.3). In bulk, single-crystal $BaTiO_3$, the remanent polarization is ~25 $\mu C\ cm^{-2}$, and the ferroelectric switching process is accomplished with a small applied field (*i.e.*, coercive field ~1 $kV\ cm^{-1}$). The work of switching (*i.e.*, the switching energy), which is the area enclosed by the P-E loop, is ~0.1 $J\ cm^{-3}$ for a $BaTiO_3$ single crystal.

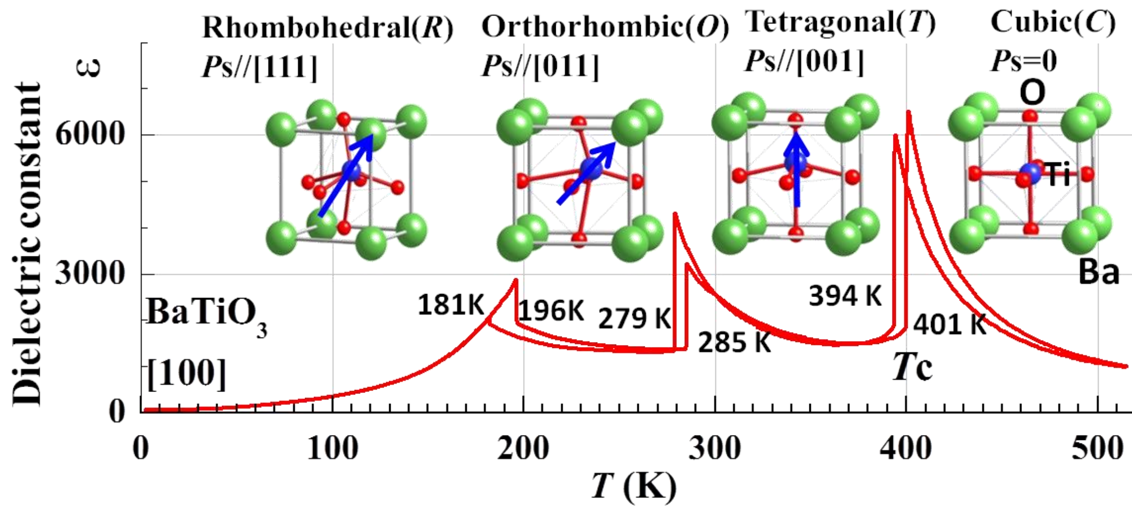


Figure 2.2 | Phase transition in $BaTiO_3$ single crystals. From low temperature to high temperature, $BaTiO_3$ single crystal will go through rhombohedral, orthorhombic, tetragonal and cubic phase symmetry. Dielectric anomaly occurs at each phase transition temperature. Adapted from ref. [67].

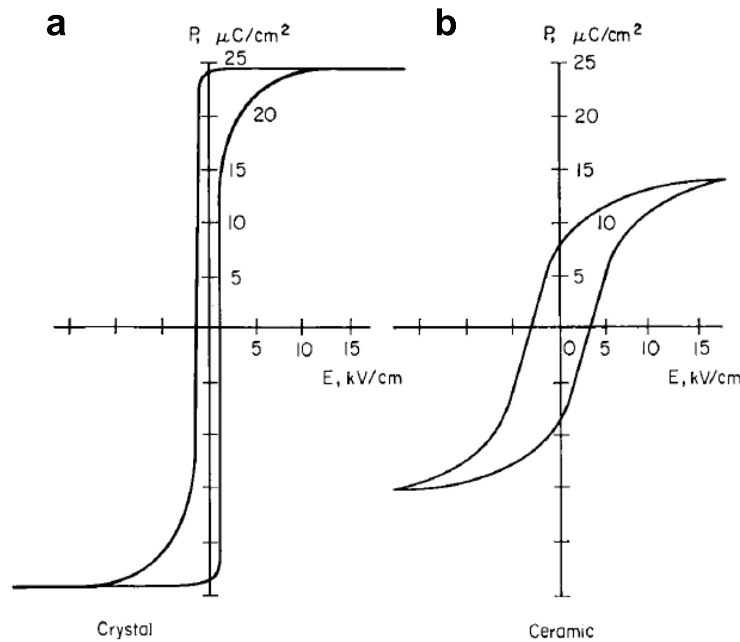


Figure 2.3 | Ferroelectric properties of $BaTiO_3$. Polarization - electric field loop for **a**, (001)-oriented $BaTiO_3$ single crystal plate, and **b**, high quality $BaTiO_3$ ceramic. From ref. [72].

$BaTiO_3$ ceramics exhibits slightly larger coercive field ~3 kV cm^{-1}, and a lower remanent polarization ~15 μC cm^{-2}. This is attributed to the fact that the grain boundaries in the $BaTiO_3$ ceramic hinders the reorientation of ferroelectric grains in the direction of the external electric field; a result arising from the collective coupling between elastic, electrostatic, and domain-wall energies[73].

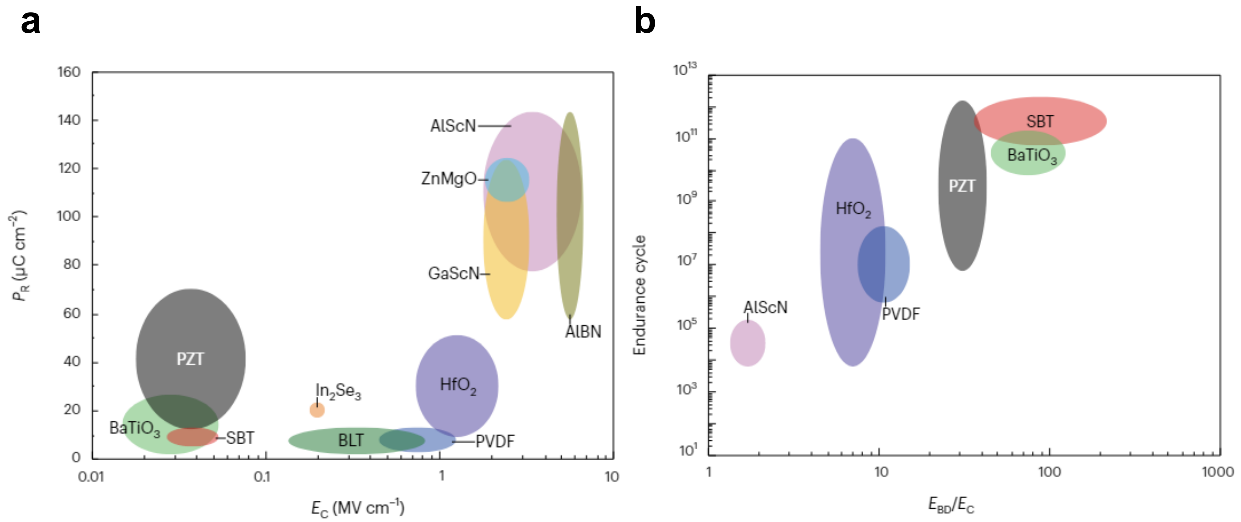


Figure 2.4 | Electrical performance of different ferroelectric materials. a, Remanent polarization versus coercive field for different ferroelectric materials. **b**, Endurance cycle number versus E_{BD}/E_C (breakdown field/coercive field) for different materials. Adapted from ref. [35].

Compared with other common ferroelectric materials, such as $PbZr_xTi_{1-x}O_3$, $Sr_2Bi_2Ta_2O_9$, HfO_2, $Al_{1-x}Sc_xN$, polyvinylidene fluoride, etc, ferroelectric $BaTiO_3$ exhibits the smallest coercive field while offering a reasonably large remanent polarization (Fig. 2.4a). Besides, the endurance cycle number (*i.e.*, the number of the electrical cycles the material can endure before showing fatigue) of the $BaTiO_3$ is excellent among all ferroelectric materials (Fig. 2.4b).

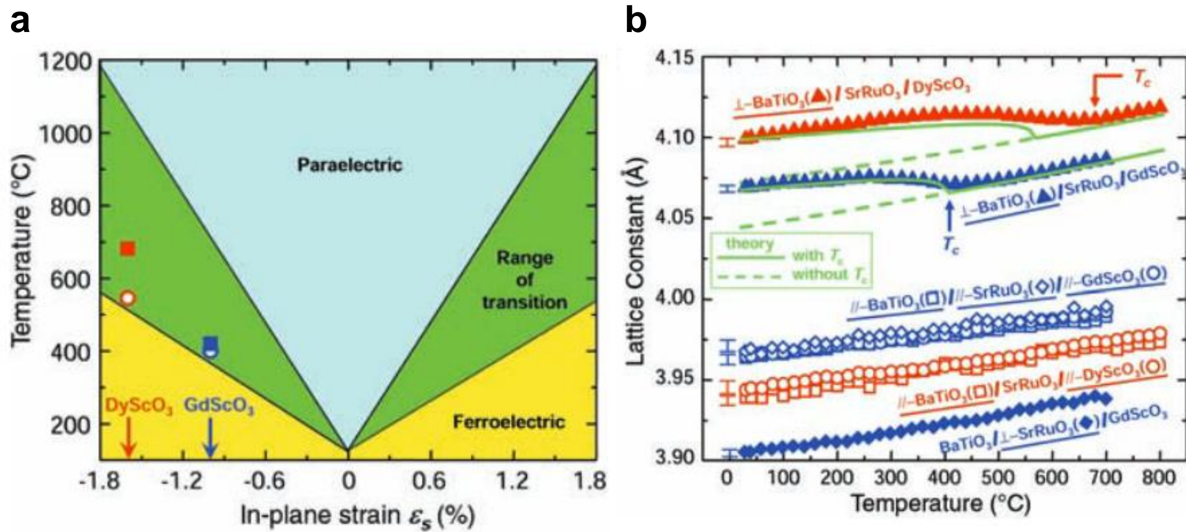


Figure 2.5 | Enhancement of ferroelectricity in $BaTiO_3$ thin films by compressive strain. a, Thermodynamic analysis of the Curie temperature in $BaTiO_3$ films under biaxial in-plane strain. **b**, Lattice constant as a function of temperature for $BaTiO_3$ films under compressive strain. The kinks in the curves represent the Curie temperature of the material where the ferroelectric-paraelectric phase transition occurs. Adapted from ref. [62].

Last but not least, $BaTiO_3$ does not contain toxic elements such as lead, and is therefore environmentally friendly. As a result, $BaTiO_3$ has drawn much attention to be used for beyond-CMOS ferroelectric switching devices.

Like the $SrRuO_3$ discussed in the previous section, strain can also affect the ferroelectric properties of $BaTiO_3$ films. Previous studies have shown that compressive strain can be used to increase the Curie temperature of $BaTiO_3$ (Fig. 2.5a), as well as enhance the tetragonality and ferroelectric polarization of the material[62,64]. The $BaTiO_3$ lattice will be compressed if grown on $DyScO_3$ (110) and $GdScO_3$ (110) substrates, with a compressive strain of -1.7% and -0.99%, respectively[64]. As a result of the compressive strain, the tetragonal lattice will be more distorted and the ferroelectric-to-paraelectric phase transition temperature (*i.e.*, the Curie temperature, T_C) will be enhanced. For example, the T_C of $BaTiO_3$ films grown epitaxially grown on $GdScO_3$ (110) and $DyScO_3$ (110) are ~400 °*C* and ~680 °*C*, respectively (Fig. 2.5b).

2.1.3 Challenges in $BaTiO_3$ thin-film synthesis

$BaTiO_3$ has the smallest coercive field among common ferroelectric materials and the strain induced in $BaTiO_3$ thin films can help stabilize or enhance the ferroelectric polarization (*i.e.*, a combination of low coercive voltage and robust remanent polarization is nearly ideal for next-generation memory and logic applications). There has been considerable interest in the study of $BaTiO_3$ thin films since the 1970s[74], and more recently, various methods have been used to synthesize $BaTiO_3$ thin films, including radio frequency magnetron sputtering[75-82], molecular beam epitaxy[62,83-86], pulsed-laser deposition[62,64,87-112], activated reactive evaporation[113-115], sol-gel methods[116], hydrothermal reaction[117], polymeric precursor methods[118], etc. The ferroelectric properties of these resulting $BaTiO_3$ thin films, however, show large variations and large deviations from the values measured in bulk single crystals. Many reports have found considerably larger coercive voltage/field[62,64,78,83,84,100,109,112,116], greatly increased work of switching (*i.e.*, the energy required to cycle through the ferroelectric hysteresis loop), and greatly diminished (or nearly zero) remanent polarization[81,94,105,113,117,118], making the switching currents hard to detect and bringing the nonvolatility into question. Thus, to realize the potential of this material requires routes to approach the "intrinsic" ferroelectric behavior (*i.e.*, small coercive field, large polarization) in $BaTiO_3$ thin films and will be discussed in following chapters of this thesis.

2.2 Epitaxial thin-film synthesis

2.2.1 Film-substrate lattice mismatch

Epitaxial thin film growth is one of the strain engineering methods to deform the material lattice by finely controlling the lattice mismatch between epitaxial thin films and substrates; therefore, controlling the magnitude of the strain induced in the system. Compared to traditional methods of inducing strain in bulk ceramics by physically applying mechanical stress to the system, induction of strain by epitaxial film synthesis is much easier. For example, to induce an 1% of deformation into sapphire (Al_2O_3) requires a hydrostatic stress value as high as 4.7 *GPa*[119], which is not an easy task to perform in a laboratory setup. Besides, since most ceramic materials are brittle, they will break long before reaching this magnitude of strain[120].

However, by synthesizing epitaxial ceramic thin films on lattice-mismatched substrates, one can easily obtain large magnitudes of strain. For example, the epitaxial strain can be as large as ~2.4% for $BaTiO_3$ films strained on $SrTiO_3$ (001) substrates[121]. With the strain induced in the materials, researchers can easily alter the crystal and domain structures[64,122] and achieve novel physical properties that cannot be realized in the bulk form[121,123].

In an epitaxial structure, the lattice mismatch between the substrate and the epitaxial film (*i.e.*, the in-plane strain felt by the thin film, ε_{ip}) is defined as

$$\varepsilon_{ip} = \frac{a_{sub} - a_{film}}{a_{film}} \qquad \text{Equation 2.1}$$

where a_{sub} and a_{film} refer to the in-plane lattice parameter of the substrate and the film, respectively. If the film and the substrate are the same material with the same crystal lattice (*i.e.*, $a_{sub} = a_{film}$), then the epitaxial structure is called homoepitaxy (Fig. 2.6a). If the film differs from the substrate in composition or lattice parameter (*i.e.*, $a_{sub} \neq a_{film}$), then the epitaxial structure is called heteroepitaxy[124] (Fig. 2.6b).

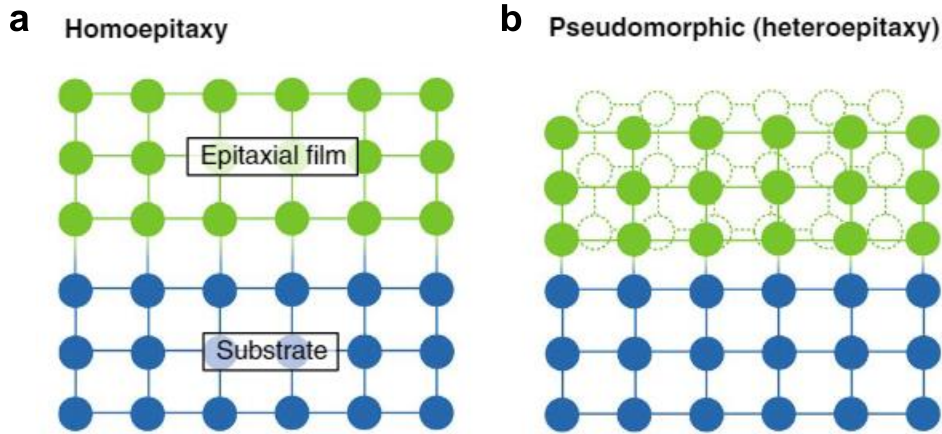


Figure 2.6 | Illustration of epitaxial relations between substrates and films. a, Homoepitaxy, and **b**, Heteroepitaxy. Adapted from ref. [124].

In the case of heteroepitaxy, the films are grown under the condition of biaxial strain and the mechanical strains in the film are governed by

$$\varepsilon_{oop} = \frac{1}{E}\left(\sigma_{oop} - \nu\sigma_{ip} - \nu\sigma_{ip}\right) = -\frac{2\nu}{E}\sigma_{ip} \qquad \text{Equation 2.2}$$

$$\varepsilon_{ip} = \frac{1}{E}\left(\sigma_{ip} - \nu\sigma_{ip} - \nu\sigma_{oop}\right) = \frac{1-\nu}{E}\sigma_{ip} \qquad \text{Equation 2.3}$$

where υ is the Poisson's ratio, E is the Young's modulus, ε_{ip} is the aforementioned in-plane strain and ε_{oop} is the out-of-plane strain which is defined as

$$\varepsilon_{oop} = \frac{c_{film} - c_{bulk}}{c_{bulk}} \qquad \text{Equation 2.4}$$

where c_{film} and c_{bulk} represent the out-of-plane lattice parameter of the thin film and its bulk counterpart, respectively. σ_{ip} is the in-plane stress assuming the in-plane anisotropy can be neglected, and σ_{oop} is the out-of-plane stress (*i.e.*, under the condition of an epitaxial film, σ_{oop} =

0). With the above equations, the out-of-plane lattice parameter of the film, c_{film}, can be expressed as

$$c_{film} = c_{bulk}\left(1 - \frac{2\nu}{1-\nu}\frac{a_{sub}-a_{film}}{a_{film}}\right) \quad \text{Equation 2.5}$$

It can be seen from Eq. 2.5, that if the film is under compressive strain (*i.e.*, $a_{sub} < a_{film}$), then its out-of-plane lattice parameter will get expanded (*i.e.*, $c_{film} > c_{bulk}$), as compared to its bulk counterpart. Otherwise, if the film is under tensile strain (*i.e.*, $a_{sub} > a_{film}$), then its out-of-plane lattice parameter will get compressed (*i.e.*, $c_{film} < c_{bulk}$). For example, if $BaTiO_3$ thin films are grown epitaxially on $GdScO_3$ (110) substrates, we can calculate

$$c_{film} = 4.067\ \text{Å} \quad \text{Equation 2.6}$$

where $\upsilon = 0.35$[125], $a_{sub} = 3.964\ Å$, $a_{film} = 3.992\ Å$, $c_{bulk} = 4.036\ Å$.

2.2.2 Pulsed-laser deposition of the heterostructures

Pulsed-laser deposition (PLD, Fig. 2.7) has long been used to produce high-quality single-crystalline films that have an epitaxial relationship with the substrates[124]. Generally, PLD systems require low-pressure to operate. Before the deposition happens, the PLD chamber will be pumped into a high vacuum state before being filled with a controlled partial pressure of gas (*e.g.*, oxygen, nitrogen, argon, etc.). Then pulses of ultraviolet laser (*i.e.*, laser shots with wavelength $\lambda = 248\ nm$; each pulse usually only lasts 10-20 ns[126]) will be used to ablate materials from ceramic or single-crystal target sources. The ablated material atoms (ions) or atom clusters (ion clusters) will gain enough kinetic energy and then transfer themselves to a heated substrate where they react with background gases to form the solid compound (via nucleation and growth) on the substrate surface. During the transfer process, ablated species will interact with each other or the background gas species to form a plasma, which is usually called the plume. The deposition rate can be well controlled by counting the number of pulses incident on the target(s). Therefore, PLD can be used to synthesize films with certain thickness requirements[127] or to synthesize alternating superlattice structure where the thickness of each layer needs to be precisely controlled[128]. PLD can be sensitive to an array of growth parameters, such as substrate temperature, background gas pressure, laser fluence (*i.e.*, the energy of the laser pulse divided by the spot size) and laser frequency (*i.e.*, the number of laser pulses generated within each second), and target-substrate distance. By carefully controlling the growth parameters, one can achieve stoichiometric transfer of materials species from the target to the substrate[64] (but it is by no means guaranteed), or one can make non-stoichiometry films on purpose and study changes in properties induced by cation (or anion) vacancies[108,129].

Like any other deposition method, different growth modes and, as a result, surface morphographies of the films, can be observed in PLD synthesis. Depending on the chemical bonding strength between the adatom species and the substrate, the kinetic energies of the adatoms and the thermal energy of the substrate surface atoms, three different growth modes are commonly observed (Fig. 2.8a) with different surface energy relations described by Young's equation[130]

$$\alpha_1 = \alpha_2 + \alpha\cos(\theta) \quad \text{Equation 2.7}$$

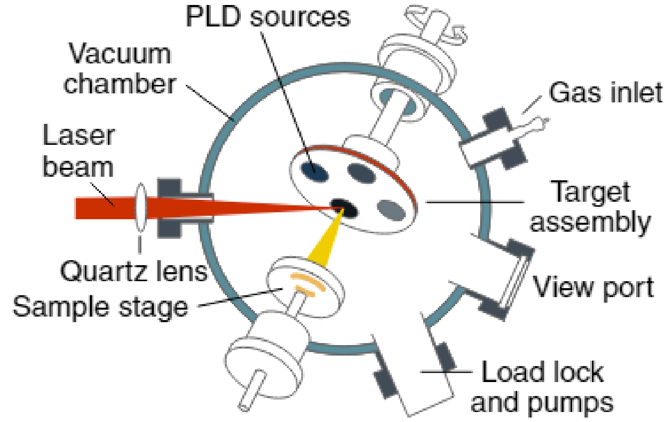


Figure 2.7 | Schematics of pulsed laser deposition (PLD) system. From ref. [124].

where α, α_1, and α_2 are the surface tension between the nucleus and the gas background, the surface tension between the substrate surface and the gas background, and the surface tension between the nucleus and the substrate surface, respectively, and θ represents the wetting angle.

If

$$\alpha_1 > \alpha_2 + \alpha \qquad \text{Equation 2.8}$$

then the bonding strength between the nucleus and the substrate is stronger than the bonding between the nucleus atoms, and in this case, the nucleus atoms form bonds with the substrate and tend to wet the substrate surface, leading to a layer-by-layer growth mode, also known as the Frank-van der Merwe growth mode (Fig. 2.8b). If the wetting angle, θ, is greater than zero, then

$$\alpha_1 < \alpha_2 + \alpha \qquad \text{Equation 2.9}$$

and in this case, the nucleus atoms tend to form bonds with themselves instead of spreading out to wet the substrate surface, leading to an island-growth mode, also known as the Volmer-Weber growth mode (Fig. 2.8c). In some cases, a third mode (a mixed-growth mode), also known as the Stranski-Krastanov mode can also occur where the growth starts in a layer-by-layer mode and transitions into the island-growth mode, due to a change of the surface energy relations with the stacking of successive monolayers (Fig. 2.8d).

To study the properties of the material itself, one needs to obtain high-quality, single-crystalline films and to keep the interfaces between different layers clean and sharp, and a layer-by-layer growth mode is required in PLD synthesized heterostructures. Therefore, careful growth control must be taken to achieve thin films with perfect structures. In this dissertation, the growth conditions for $SrRuO_3$ and $BaTiO_3$ thin films are listed in Table 2.1.

The substrate is first heated to 690 °C at a rate of 20 °C min^{-1}, then the bottom $SrRuO_3$ layer was deposited using the condition provided in Table 2.1. Afterwards, the stack is cooled at a rate of 10 °C min^{-1} to 600 °C where the $BaTiO_3$ layer is deposited. Then the stack is heated back to 690 °C at a rate of 15 °C min^{-1}, where the top $SrRuO_3$ layer is deposited. After the deposition, the PLD chamber is flooded with oxygen and the whole film stack is cooled to room temperature at a rate of 5 °C min^{-1}.

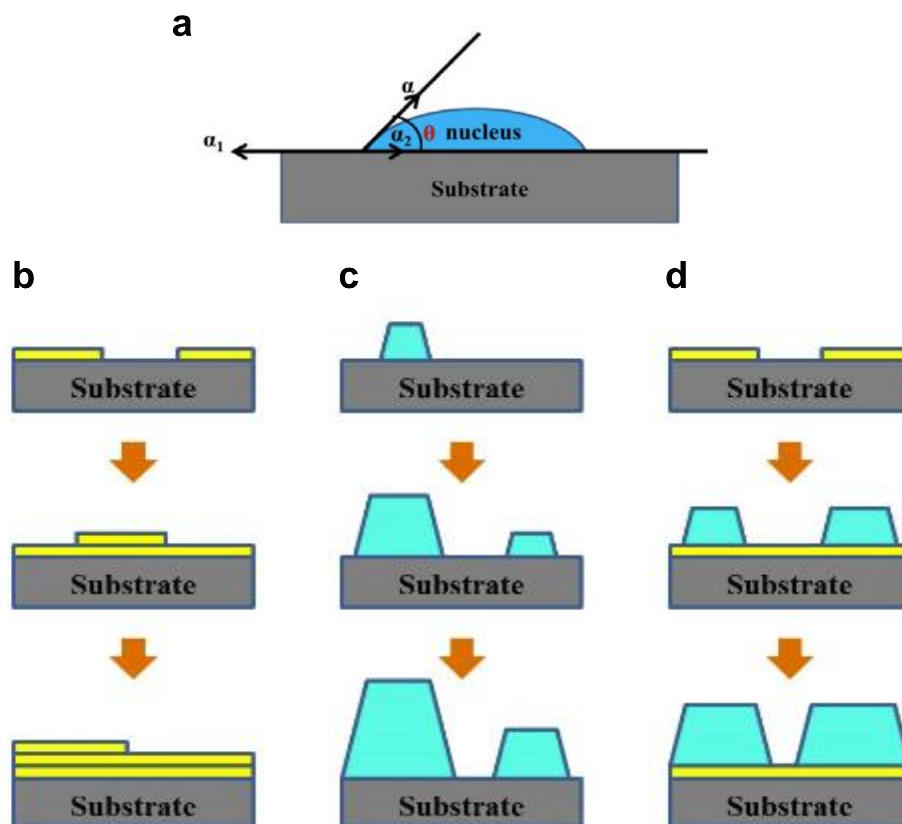


Figure 2.8 | Illustration of growth modes in PLD. a, Surface tension relations between substrate surface, nucleus and the background gas. **b**, Frank-van der Merwe (layer-by-layer) growth mode. **c**, Volmer-Weber (island) growth mode. **d**, Stranski-Krastanov (mixed) growth mode. Adapted from ref. [130].

Materials	$SrRuO_3$	$BaTiO_3$
Target type	Ceramic	Ceramic
Target composition	$Sr_{1.00}Ru_{1.00}O_{3.00}$	$Ba_{1.00}Ti_{1.00}O_{3.00}$
Substrate temperature	690 °C	600 °C
Oxygen pressure	100 mTorr	20-70 mTorr
Laser wavelength	248 nm	248 nm
Laser pulse energy	100 mJ	140 mJ
Laser spot size	0.0744 cm^2	0.0922 cm^2
Laser fluence	1.34 J cm^{-2}	1.52 J cm^{-2}
Laser frequency	15 Hz	2 Hz
Target-substrate distance	5.5 cm	5.5 cm

Table 2.1 | Growth conditions for $SrRuO_3$ and $BaTiO_3$ thin films in PLD.

2.3 Summary

To summarize, this chapter introduces the preliminary physical background for the studies performed in the thesis, including two material model systems, namely, $SrRuO_3$, and $BaTiO_3$, as well as the epitaxial synthesis mechanisms in PLD process. The advantages of $BaTiO_3$ over other common ferroelectric materials in terms of switching field, switching energy and fatigue resistance for beyond-CMOS ferroelectric applications is also discussed. The epitaxial strain can affect the structural and electrical behaviors of the materials in their thin-film forms, resulting in a large deviation in properties from their bulk counterparts. The synthesis of idealized $BaTiO_3$ thin films has long been a challenge to researchers, and to some extent has slowed down the applications of $BaTiO_3$ in next-generation devices. In this chapter, the growth parameters for high quality $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures are provided and details on characterizing their properties are discussed in the following chapter.

Chapter 3

Characterization of Ferroelectric Heterostructures

This chapter focuses on the characterization techniques used to measure our synthesized $SrRuO_3/BaTiO_3/SrRuO_3/GdScO_3(110)$ heterostructures. First, structural characterization methods are introduced, including X-ray diffraction, as well as scanning transmission electron microscopy. Then various (di)electrical characterization methods are discussed, including those that allow for the study of the dielectric and ferroelectric behavior of the capacitor structures, such as dielectric-voltage measurement, polarization-electric field/voltage measurement, fatigue and retention measurement, as well as the switching transient measurements, in an effort to examine the potential performance of $BaTiO_3$ capacitors within actual ferroelectric devices. Transport measurement and deep-level transient spectroscopy measurements are also discussed, in order to study the intra-bandgap charge carrier trapping states in $BaTiO_3$ films.

3.1 Structural characterization of the heterostructures

3.1.1 X-ray diffraction

X-ray diffraction has long been a useful non-destructive tool to examine the crystal structure of the materials. By performing X-ray diffraction, one is converting real space crystal planes into their Fourier transformed counterpart – the reciprocal space lattice points – with each crystal plane orientation (and distance) corresponding to one lattice vector in reciprocal space. The incident and diffracted X-ray beam are represented by wavevectors, $\overrightarrow{IA}$ and $\overrightarrow{AB}$, respectively, in the Ewald sphere[131] (Fig. 3.1a). Since usually X-ray diffraction is an elastic scattering process, the incident and diffracted have the same magnitude, but different directions. The angle between the incident beam and the characterized crystal plane is referred to as θ, and therefore, the angle between two wavevectors is 2θ. If the difference vector, $\overrightarrow{IA} - \overrightarrow{AB}$, between the two beams is equal to one of the reciprocal lattice vectors, $\overrightarrow{d_{hkl}^{*}}$, in the reciprocal space, then the corresponding crystal plane in the real space will be captured, and a peak (or an increase in diffracted beam intensity) will show up in the spectrum[132,133].

For X-ray diffraction measurements on thin films, depending on the crystal plane orientation and the equipment setup geometry (*i.e.*, film surface orientation), the measurements can be categorized as symmetric or asymmetric. If the crystal planes being characterized are parallel to the film/substrate surface, one will have symmetric reflection condition (Fig. 3.1b), $\theta = \omega$, where ω is the angle between the incident beam and the film surface. If the crystal planes are not parallel to the film substrate surface, one will have asymmetric condition (Fig. 3.1c) where $\theta \neq \omega$. By scanning a wide range of θ-2θ values, one can obtain a spectrum in one-dimension, which is usually referred to θ-2θ line scan. θ-2θ line scan is the most straightforward scan type in X-ray diffraction. The relation between the angle θ and the distances between the characterized planes, d, is described by the Bragg's law:

$$2d\sin(\theta) = n\lambda \qquad \text{Equation 3.1}$$

where λ is the wavelength of the X-ray beam and n is the wavenumber difference between the incident beam and the scattered beam. By applying the Bragg equation to the line-scan spectrum, one can extract the lattice parameters (*i.e.*, in one dimension, usually in the out-of-plane direction) of the thin-film and substrate materials.

Reciprocal space mapping (RSM) is another type of measurement in X-ray diffraction. In the process of obtaining an RSM spectrum, both ω axis and 2θ axis are scanned in real space, generating a two-dimensional region in the reciprocal space. The reciprocal lattice points (corresponding to crystal planes in real films) within the two-dimensional region will be captured. In the case of asymmetric RSM scan, information on both in-plane and out-of-plane lattice parameters can be recorded, and by applying the converting equations,

$$q_{\parallel} = \frac{1}{\lambda}\{\cos(\omega) - \cos(2\theta - \omega)\} \qquad \text{Equation 3.2}$$

and

$$q_{\perp} = \frac{1}{\lambda}\{\sin(\omega) - \sin(2\theta - \omega)\} \qquad \text{Equation 3.3}$$

one can extract both the in-plane and out-of-plane lattice parameters of the thin-film materials. Another use of the RSM is to examine the strain status of the thin films that are grown epitaxially on the substrate. In the case of a fully strained film, the substrate and the film will have the same in-plane lattice parameter. In the RSM spectrum, both reciprocal lattice vectors will have the same in-plane components (Fig. 3.1d). However, if the films are relaxed, then the substrate and the film will have different in-plane lattice components (Fig. 3.1e).

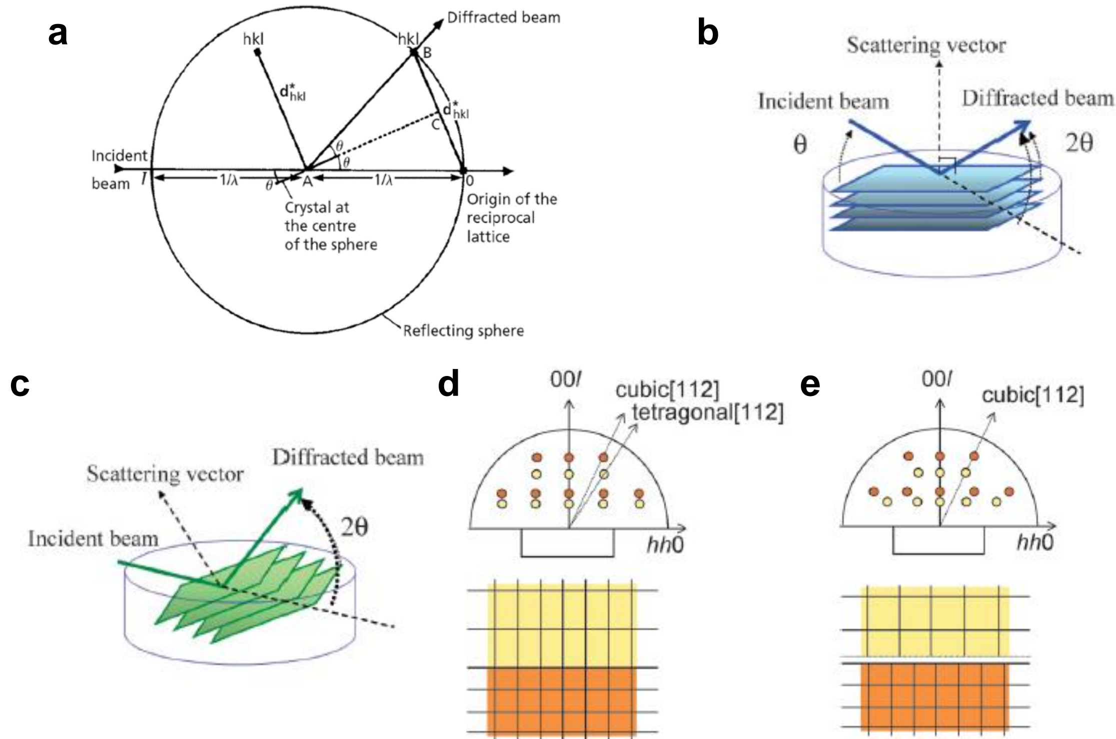


Figure 3.1 | Illustration of X-ray diffraction on thin film analysis. a, Relation between incident beam, scattered beam and crystal reciprocal lattice vector. **b**, Symmetric measurement setup. **c**, Asymmetric measurement setup. Reciprocal relation between the substrate and **d**, strained film and **e**, relaxed film. Adapted from ref. [131-133].

Another type of measurement using X-ray diffraction is the rocking-curve scan (*i.e.*, the ω scan). In this measurement, the 2θ axis is fixed at the Bragg's condition, while the ω axis was scanned in the vicinity of the Bragg angle, θ. The rocking curve measurement can be used to examine the crystallinity of each layer in the heterostructure, with broader rocking-curves peaks indicating higher level of defects or crystal mosaicity in the corresponding layer[134]. As such, the full-width at half-maximum (FWHM) value of the rocking curve peaks can be used as a quantitative characteristic number for crystal crystallinity.

In this thesis, all θ-2θ line scans and RSM scans on $SrRuO_3/BaTiO_3/SrRuO_3/GdScO_3$ (110) heterostructures were performed using a Panalytical X'Pert[3] MRD 4-circle diffractometer with Cu Kα X-ray with a wavelength of 1.54 $\AA$.

3.1.2 Scanning transmission electron microscopy

High-resolution scanning transmission electron microscopy (STEM) measurement was also performed to directly image the crystal structure of the synthesized $SrRuO_3/BaTiO_3/SrRuO_3/GdScO_3$ (110) heterostructures. While with the development of transmission electron microscopy, the resolution of such techniques have reached atomic level in recent years[135,136], it still has limitations when trying to spot tiny defects (*e.g.*, points defects) in the crystal lattice, especially when the defect concentration is low. As a result, in this thesis, STEM was only used as a supplementary method to characterize the crystallinity of the synthesized heterostructures.

For the purpose of demonstration, a representative STEM image is shown for the 30 nm $SrRuO_3$/25 nm $BaTiO_3$/30 nm $SrRuO_3/GdScO_3$ (110) heterostructure with $BaTiO_3$ layer grown at 60 mTorr O_2 pressure[137] (Fig. 3.2a,b). To prepare the sample for STEM, the heterostructure was first mechanically polished at 0.5° and subsequently argon-ion milled using a Gatan Precision Ion milling system, starting from 3.5 keV at 4° down to 1 keV at 1° for the final polish. STEM imaging was performed using a double-aberration-corrected TEAM I microscope operating at 300 kV, at the National Center for Electron Microscopy, Lawrence Berkeley National Laboratory. The probe semi-angle and beam current used for imaging were 30 mrad and 70 pA, respectively. The STEM image suggests that the film stack is free of defects and dislocations over a wide area of the measured sample. A higher resolution image suggests the highly-crystalline atomic structure of the heterostructure, and clean interfaces between the $SrRuO_3$ electrodes and the $BaTiO_3$ layer, which, to some extent, can be an indication of the high quality of the heterostructure synthesized in this work.

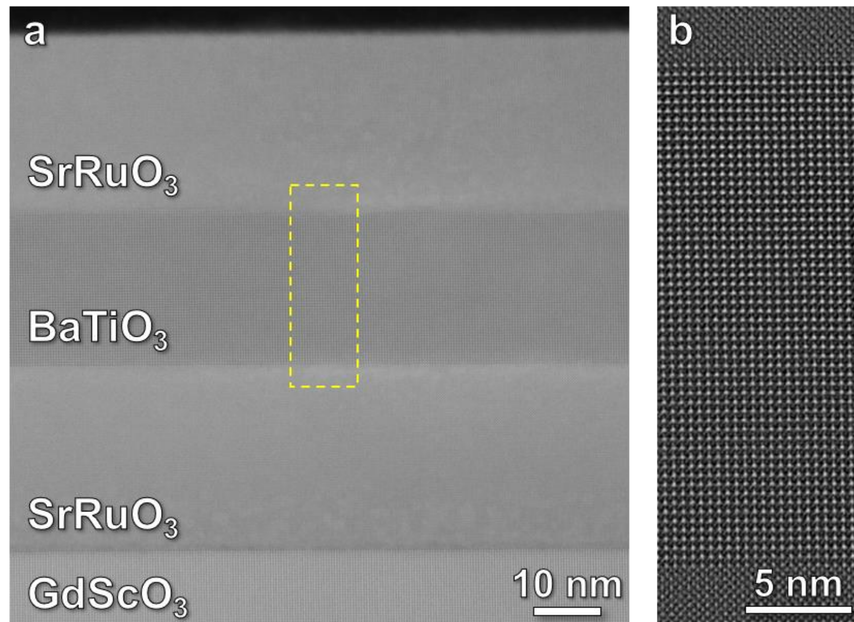


Figure 3.2 | Representative transmission electron microscopy image of the heterostructure. a, Z-contrast STEM imaging of the 30 nm $SrRuO_3$/25 nm $BaTiO_3$/30 nm $SrRuO_3/GdScO_3$ (110) heterostructure. **b**, High-resolution image of a representative portion (yellow box in **a**) of the heterostructure.

3.2 (Di-)Electrical characterization of the heterostructures

3.2.1 Dielectric measurements

Dielectric constant measures how easily the material can be polarized under the applied electric field. For a ferroelectric capacitor with spontaneous polarization, the dielectric constant can be impacted by various factors such as temperature, the magnitude of the applied DC bias and the frequency/strength of applied AC electric fields[95]. In the process of measurement, a DC bias is applied to the $SrRuO_3/BaTiO_3/SrRuO_3$ capacitors, and an AC oscillation signal (*i.e.*, small enough for the dielectric measurement to operate in the reversible regime, avoiding dielectric non-linearities caused by irreversible effects from domain-wall motion, switching, etc[138]) is added on top of the DC signal to measure the capacitive response (*i.e.*, the capacitance, *C*) from the capacitor. The dielectric constant, ε_r, is then extracted from the capacitance via the relationship,

$$\varepsilon_r = \frac{Cd}{A} \quad \text{Equation 3.4}$$

where *d* is the thickness of the $BaTiO_3$ film and *A* is the capacitor area.

In this thesis, the dielectric measurement was performed using an impedance analyzer (no. E4990A, Keysight Technologies), with a DC bias ranging from -0.5 V to 0.5 V and an AC excitation voltage of 5 mV with frequencies ranging from 1 kHz to 100 kHz, at different temperatures ranging from 20 °C to 460 °C.

3.2.2 Ferroelectric measurements

Ferroelectric hysteresis loops were obtained by applying voltage waveforms to $BaTiO_3$ capacitors to switch the ferroelectric polarization direction and measure the switching current during the process. The voltage waveform can be applied by a waveform/pulse generator and has the shape of a double-bipolar sequence (Fig. 3.3). During the switching process, the switching current at different voltages is detected and integrated with time. By doing so, one can calculate the charge produced during the switching and therefore obtain the polarization-electric field/voltage loop (*i.e.*, PE/PV loop) of the ferroelectric material.

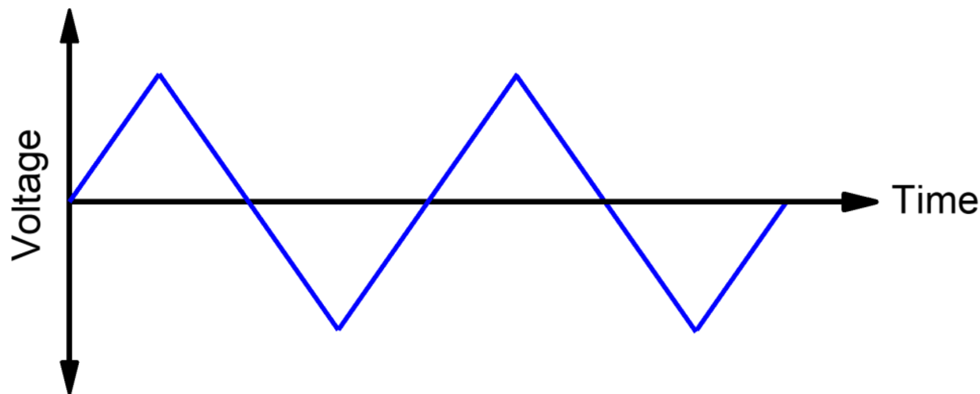


Figure 3.3 | Ferroelectric measurement of the heterostructure. Double-bipolar DC signal applied to measure the polarization switching in ferroelectric materials.

Generally, the PE loop intersects with the horizontal axis (*i.e.*, $P = 0$) at two different electric field values, E_C^+ and E_C^-. The coercive field, E_C, is extracted using

$$E_C = \frac{|E_C^+ - E_C^-|}{2} \qquad \text{Equation 3.5}$$

And the imprint (*i.e.*, the horizontal deviation of the PE loop from the origin) is calculated using

$$E_{Imprint} = \frac{E_C^+ + E_C^-}{2} \qquad \text{Equation 3.6}$$

In the meantime, the PE loop intersects with the vertical axis (*i.e.*, $E = 0$ or $V = 0$) at two different polarization value P_R^+ and P_R^-. The averaged remanent polarization, P_R, is extracted using

$$P_R = \frac{|P_R^+| + |P_R^-|}{2} \qquad \text{Equation 3.7}$$

All measurements in this work were performed using a Precision Multiferroic Tester (Radiant Technologies, Inc.), with various waveform amplitudes and periods (*i.e.*, 0.1-1000 ms, corresponding to frequencies 1-10 kHz).

3.2.3 Fatigue and retention measurements

Fatigue measures how robust the remanent polarization is against cyclic bipolar stress. A single fatigue stress signal has the same waveform (*i.e.*, double-bipolar waveform) as in the polarization-electric field measurement (Fig. 3.3). After a certain number of continuously applied fatigue signals, a Positive-Up-Negative-Down (PUND) pulse sequence (Fig. 3.4) is applied to the heterostructures to measure the remanent polarization. The PUND sequence consists of five identical pulses, with each pulse having same amplitude, V_P, and same width, t_P. The delay time between pulses is denoted as t_D. The first pulse is the preset pulse, which sets the initial polarization into the negative state. Then the second pulse switches the polarization into the positive state, and records both the switching polarization and non-switching polarization, P_2. The third pulse, same as the second pulse, records the non-switching polarization, P_3.

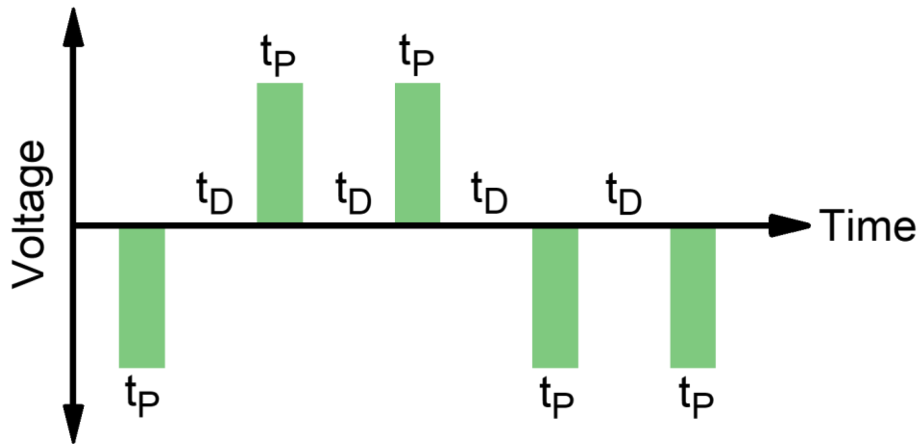


Figure 3.4 | Fatigue measurement of the heterostructure. PUND pulse sequence used to measure the remanent polarization of the capacitor.

The remanent polarization of the positive pulses, P_R^+, is calculated using

$$P_R^+ = \frac{P_2 - P_3}{2} \qquad \text{Equation 3.8}$$

Similarly, the remanent polarization of the negative pulses, P_R^- is calculated using

$$P_R^- = \frac{P_4 - P_5}{2} \qquad \text{Equation 3.9}$$

where P_4 presents the switching and non-switching polarization from the fourth pulse, and P_5 represents the non-switching polarization from the fifth pulse. The PUND measurements are performed between fatigue stress cycles, and the remanent polarization values can be calculated for each PUND testing point.

Another common performance test is the retention measurement of the heterostructure. Retention measurement shows how robust the remanent polarization is against aging (*e.g.*, during the long period of data storage). In the retention measurement, multiple modified PUND pulse sequence cycles are applied (Fig. 3.5), with each measurement cycle (purple dashed box, Fig. 3.5) consisting of three pulses with same amplitude, V_P, and width, t_P. In the nth measurement cycle, while the delay time between the second and the third pulse is fixed at t_0, the delay time between the first pulse and the second pulse, t_{Dn}, is a variable representing the retention time that is to be tested in the measurement cycle. Similar to the fatigue measurement, the second pulse, P_2, records both the switching polarization and non-switching polarization, and the third pulse, P_3, only records the non-switching polarization. The first retention cycle is used to obtain the value of initial remanent polarization before retention starts in which t_{D1} was set to equal t_0 (*i.e.*, $t_{D1} = t_0$). The initial remanent polarization value is calculated using

$$P_R^{initial} = \frac{P_2 - P_3}{2} \qquad \text{Equation 3.10}$$

where P_2 and P_3 are measured from the first retention cycle. In the nth retention cycle, a different delay time, t_{Dn}, are applied, and the remanent polarization value is calculated using

$$P_r = P_2 - P_3 - P_R^{initial} \qquad \text{Equation 3.11}$$

where P_2 and P_3 are measured from the nth cycle, and $P_R^{initial}$ is calculated from Eq. 3.10. In this work, V_P is set to be 1 V, t_P is set to be 0.15 ms, and t_{D1} and t_0 are both set to be 1 ms.

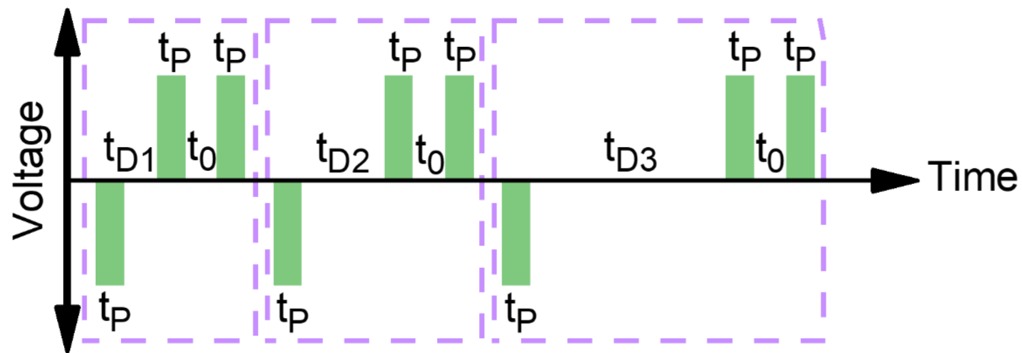


Figure 3.5 | Retention measurement of the heterostructure. Modified pulse sequence used to measure the remanent polarization of the capacitor after certain retention time.

3.2.4 Switching-transient measurements

Another important physical parameter to measure is the switching speed of the heterostructure. Generally the ferroelectric switching process is completed with domain nucleation and growth[71]. To measure the switching transient of the heterostructure, a sequence train of three pulses is applied to the $SrRuO_3/BaTiO_3/SrRuO_3$ capacitor (Fig. 3.6).

The first pulse, P_1, is a negative preset pulse which sets the polarization into a negative state. The second positive pulse, P_2, has variable amplitudes representing the different electric field applied to the capacitor. During the duration of the second pulse, the switching current as a function of time is measured using an oscilloscope[139]. The second pulse records the total current from both ferroelectric switching part and non-switching part. The third pulse, P_3, has the same amplitude and width as the second pulse and is applied 100 ns after the second pulse. P_3 only records the current from the non-switching part. By subtracting P_3 from P_2, one can obtain the transient current solely from ferroelectric switching. The polarization transient curve is calculated by integrating the transient current with time

$$\Delta P = \int_0^{+\infty} (P_2 - P_3)\, dt \qquad \text{Equation 3.12}$$

The characteristic switching time, t_{sw}, is a physical parameter extracted from the polarization transient curve. It is a representative value to measure how fast the ferroelectric material switches and can have multiple definitions. In some researches[139], t_{sw} is defined as the time needed to reach 90% of the saturation polarization, P_S,

$$t_{sw} = t(90\%\, P_S) \qquad \text{Equation 3.13}$$

while in other studies[140], t_{sw} is defined as the time needed for the polarization to start from 10% of the saturation polarization and reach 90% of the saturation polarization.

$$t_{sw} = t(90\%\, P_S) - t(10\%\, P_S) \qquad \text{Equation 3.14}$$

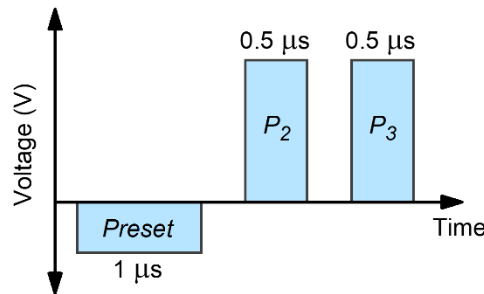


Figure 3.6 | Switching time measurement of the heterostructure. Pulse train used to measure the switching time of the heterostructure.

In the switching transient measurement in this work, the pulse sequence is generated using a pulse generator (Berkeley Nucleonics, no. BN 765). The current transient is measured using an oscilloscope (TEKTRONIX TDS 6604 Digital Storage Oscilloscope, 6 GHz, 20 GS/s). The preset pulse has an amplitude of -1 V and width of 1 μs. Both switching pulse and non-switching pulse have a width of 0.5 μs. The definition of 90% P_S - 10% P_S is used to extract characteristic switching times in $BaTiO_3$ capacitors.

3.2.5 Transport measurements

To study the transport properties and the dominant conduction mechanism inside the heterostructure, as well as the intra-bandgap trap states, current-voltage measurements (*i.e.*, the leakage measurements) were performed on the $BaTiO_3$ capacitors. The measurements were performed in both positive and negative directions by applying an unswitched triangular voltage waveform (Fig. 3.7). Pre-poling pulses are applied to prevent contributions from switching currents.

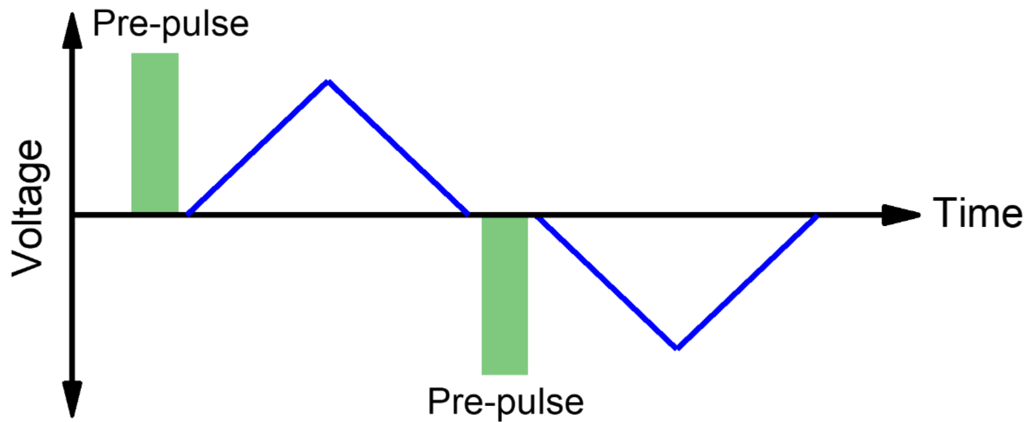


Figure 3.7 | Transport measurement of the heterostructure. Unswitched triangular voltage waveform with pre-pulses to measure the transport current (leakage current) in ferroelectric materials.

In this work, the transport measurements were performed using the Precision Multiferroic Tester (Radiant Technologies, Inc.) over a temperature range of 300-500 K, with various voltage waveform amplitude (up to 3.5 V). The pre-pulse has a height of 1.2 V and width of 0.15 ms. A number of bulk-limited or interface-limited leakage mechanisms can occur in dielectric films[141,142], with a detailed analysis provided in Chapter 5.

3.2.6 Deep-level transient spectroscopy measurements (DLTS)

Another measurement to characterize the charge trapping states in the heterostructure is the deep-level transient spectroscopy (DLTS). DLTS can be used to detect a wide range of electrically active defects that can act as charge trapping/de-trapping centers during the transportation in the materials[143]. It measures the capacitance transient caused by the thermal emission of charge carriers from trapping centers as a function of temperature. The spectrum obtained from DLTS can show the presence of trap states as peaks above a flat baseline. In the spectrum, different peaks show up at different temperature windows, with each peak corresponding to a single trap state with its own characteristic thermal emission properties[108,143]. Two types of charge carrier traps can exist in the materials. Electron traps are traps that are empty of electrons and can therefore trap electrons, while hole traps are full of electrons and can therefore trap holes by the electron-hole recombination process. The electron traps tend to be located near the conduction band (*i.e.*, in the upper half of the bandgap) while the hole traps tend to be located near the valence band (*i.e.*, in

the lower half of the bandgap). Depending on the majority carrier type in the materials and the voltage sign applied during the measurements, it is possible to distinguish whether the trap states are electron traps or hole traps. For each trap state, the intensity of the peaks showing up on the DLTS spectrum is proportional to the concentration of the trap state, while the peak maximum locations, which is determined by its characteristic thermal emission properties, can be used to extract the trap activation energy.

In the DLTS measurement, first, a trap-filling voltage pulse is applied, setting intra-bandgap traps to an accumulated states filled with charge carriers. Then, the pulse is removed, and the traps start to emit charge carriers through a thermal emission process. The capacitance transient is monitored as it relaxes to its quiescent value, while the concentration of the trapped charge carriers decays to its thermal equilibrium value[143]. The thermal emission rate of the trap states and the time constant of the emission process, is dependent on the temperature, and the energy difference between the trap states and the conduction band (electron traps) or the valence band (hole traps). It is possible to extract the activation energy by performing a temperature scan and setting up multiple time windows (t_1 to t_2) during the emission processes. As the temperature changes, the capacitance changes between the time window, $C(t_1)$-$C(t_2)$, also changes[144] (Fig. 3.8). At a certain temperature, T_M, $C(t_1)$-$C(t_2)$ will reach a maximum value for the given time window (*i.e.*, t_1 to t_2), corresponding to a maximum emission rate[108,143], which is related to the characteristic thermal emission properties of the trap state and can be used to extract the trap activation energy[145].

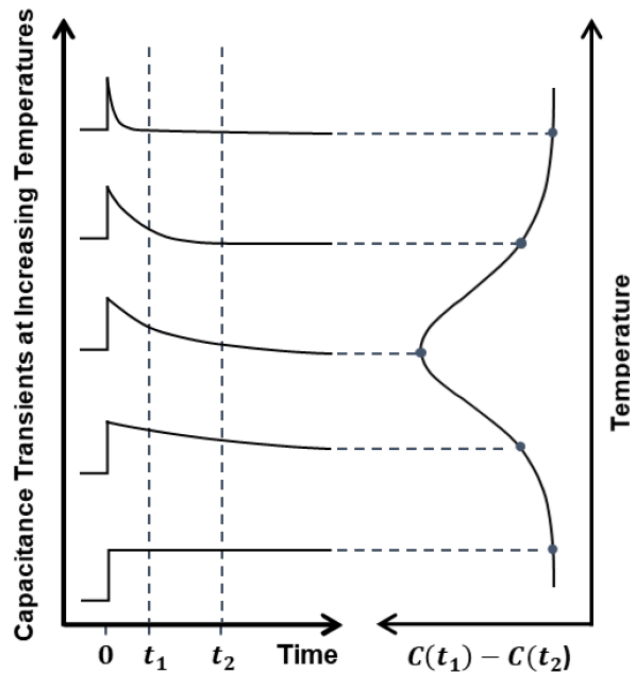


Figure 3.8 | Basic principles of deep-level transient spectroscopy. Capacitance transient as a function of temperature.

Different ways can be used to set up time windows, such as (1) fixing t_1 while varying t_2, (2) fixing t_2 while varying t_1 and (3) varying t_1 and t_2 while keeping t_1/t_2 fixed[63,143]. In this work we chose to keep t_1/t_2 fixed while varying t_1 and t_2 simultaneously, in order to only measure the change in DLTS peak maximum without disturbing the size or the shape of the peaks. DLTS measurements

in this work were performed using a Precision Multiferroic Tester (Radiant Technologies, Inc.), over a temperature range of 100-400 K, in a vacuum probe station (Lake Shore Cryotronics). The temperature interval during the measurement is 5 K, and the heterostructures were kept at each temperature for 3 min before the measurement for the trapped charge carrier population to reach its thermal equilibrium value. A voltage pulse of 3.5 V height and 8 ms width is then applied as the trap-filling pulse, and the time windows are set up as 5-10 ms, 10-20 ms, 20-40 ms, 40-80 ms, and 80-160 ms (*i.e.*, t_1/t_2 is fixed to be 0.5), respectively.

3.3 Summary

To summarize, this chapter provides the reader with a brief introduction on different types of measurement that are performed in this thesis. First, X-ray diffraction is discussed, focusing on θ-2θ line scan and reciprocal space mapping, from which one can extract both in-plane and out-of-plane lattice parameters for $SrRuO_3/BaTiO_3/SrRuO_3/GdScO_3$ (110) heterostructures. Then scanning transmission electron microscopy is introduced to directly image the crystal structures. What follow next are various types of (di)electric characterizations on $SrRuO_3/BaTiO_3/SrRuO_3$ capacitors, including capacitance-voltage measurement to extract the dielectric constants, ferroelectric-electric field/voltage hysteresis measurement to extract the coercive fields and remanent polarizations, fatigue and retention measurement to assess the performance of the capacitors against cyclic stress and aging, as well as switching transient characterization to measure the switching speeds of the capacitors. Transport measurement and deep-level transient spectroscopy are also discussed to characterize the intra-bandgap charge trapping states in the $BaTiO_3$ capacitors. These basic measurement types discussed in this chapter will be repeatedly used in the following chapters where more in-depth analyses are performed to study the physics inside the $BaTiO_3$ heterostructures.

Chapter 4

Effect of Growth Parameters on $BaTiO_3$ properties

This chapter focuses on the effect of growth parameters, especially the growth pressure on the $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures. First, a discussion is made on how the growth pressure affects the structural properties of the $BaTiO_3$ layer. Then the effect of growth pressure on the ferroelectric properties of $BaTiO_3$ layer is discussed. By carefully adjusting the growth pressure, one can achieve single-crystal-like epitaxial $BaTiO_3$ films that have ferroelectric properties comparable to bulk material. Thickness scaling and lateral scaling are done to explore the smallest switching voltage, lowest switching power and fastest switching speed in the ferroelectric $BaTiO_3$ layer. Finally, trials to integrate $BaTiO_3$ material onto silicon-based substrates are made, showing the potential for $BaTiO_3$ to be used in actual ferroelectric devices.

4.1 Growth pressure control of $BaTiO_3$ heterostructures

As has been discussed in Chapter 2, great challenges have been encountered when synthesizing $BaTiO_3$ thin films with idealized structural and ferroelectric properties. Since $BaTiO_3$ single crystals have low coercive field (~1 kV cm^{-1}) and low switching energies (~0.1 J cm^{-3}), while maintaining relatively large remanent polarization (~26 μC cm^{-2}) it makes this material an ideal candidate for next generation beyond-CMOS applications such as ferroelectric memories, logics, and logic-in-memories[62]. However, when $BaTiO_3$ is synthesized as a thin film, the ferroelectric properties can be changed including observation of large coercive voltage (>1 V)[62,64,78,83,84,100,109,112,116] or diminished remanent polarization (< 5 μC cm^{-2})[81,94,105,113,117,118], making it unsuitable for use in actual devices. Therefore, investigations are made into $BaTiO_3$ thin films as how to achieve ferroelectric properties comparable to bulk crystals. The most straightforward method is to carefully control the growth condition during the synthesize process. In PLD, changing the growth parameters, including the laser fluence and the growth pressure can have significant effects on the defect concentration[63,64]. The defect level inside the material can impact the physical properties of the synthesized films, including the lattice parameter, the imprint and the leakage current[63,64,108]. The effect of growth pressure on heterostructure properties is discussed in this chapter.

4.1.1 Effect on structural properties

Here, the effect of the growth pressure on 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) heterostructures is investigated. While the top and bottom $SrRuO_3$ layers are grown using the same growth conditions, the growth pressure for the $BaTiO_3$ was varied from 20 mTorr to 70 mTorr (Fig. 4.1). Increasing the growth pressure from 20 mTorr to 60 mTorr reduces the out-of-plane lattice of the $BaTiO_3$ layer. Previous studies have shown similar relations between the out-of-plane lattice parameters and the growth pressure for perovskite ferroelectric thin films (*e.g.*, $PbTiO_3$[63], $Ba_xSr_{1-x}TiO_3$[146,147], etc) in PLD process, with lowering the growth pressure causing out-of-plane lattice to expand in the thin films. The same studies have also suggested that the out-of-plane lattice expansion may be resulted from the defects induced during the growth because of the bombardment of high energetic species in the PLD plasma[63,146,147]. Increasing the growth pressure can increase the number of scattering events undergone by the ablated atoms as they transit to the substrate, and therefore decrease the kinetic energy they have when they impact the substrate surface, reduce the potential for knock-on damage, and lower the chance of introducing defects into the synthesized film[63,109]. In our case, the $BaTiO_3$ peaks shift to the high-angle side when increasing the oxygen growth pressure from 20 mTorr to 60 mTorr (Fig. 4.1a). RSMs were also performed to obtain the strain condition for $BaTiO_3$ thin films under various O_2 pressures. Increasing the O_2 growth pressure from 20 mTorr to 60 mTorr does not change the strain state of the $BaTiO_3$ layer, with all $BaTiO_3$ layers epitaxially strained on the $GdScO_3$ (110) substrate (Fig. 4.1b).

The level of lattice expansion is quantitively expressed using the equation

$$\frac{\Delta l}{l} = \frac{l - l_0}{l} \times 100\% \qquad \text{Equation 4.1}$$

where l represents the actual out-of-plane lattice parameter of the $BaTiO_3$ layer and can be extracted using Bragg's law (Eq. 3.1). l_0 represents the theoretically predicted out-of-plane lattice parameter of the $BaTiO_3$ materials calculated using biaxial stress-strain relations (Eq. 2.5).

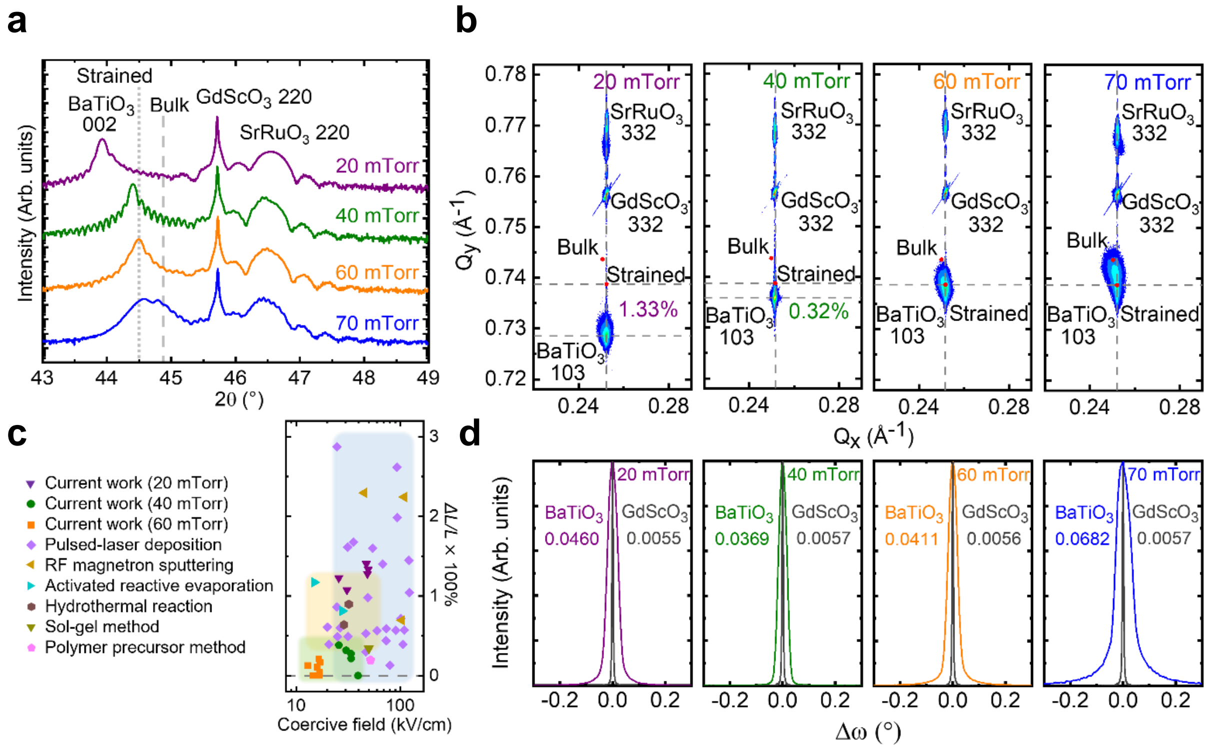


Figure 4.1 | Effect of growth pressure on the structural properties of the heterostructures. **a**, θ-2θ line scans of 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) heterostructures grown under different O_2 pressure from 20 mTorr to 70 mTorr. The dashed lines show the peak positions for the bulk materials, and the dotted lines show the theoretical peak positions for the fully strained $BaTiO_3$ films on $GdScO_3$ (110) substrates. **b**, Reciprocal space mapping of 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) heterostructures grown under different O_2 pressure. The red dots represent the peak positions for both bulk and strained version of $BaTiO_3$. **c**, Comparison of out-of-plane lattice expansion in $BaTiO_3$ thin films between the work in this thesis and previously reported ones. **d**, Rocking curves about the 002- and 220-diffraction conditions of the $BaTiO_3$ films grown under different O_2 pressure and the $GdScO_3$ (110) substrate, respectively.

A comparison is made between the out-of-plane lattice expansions in the $BaTiO_3$ films synthesized in this thesis and those films in previously reported studies (Fig. 4.1c). As the growth pressure increases from 20 mTorr to 60 mTorr, the out-of-plane lattice expansion decreases, with the films grown using 60 mTorr exhibiting almost no lattice expansion from its theoretically predicted value. Shown together is the $BaTiO_3$ out-of-plane lattice expansion data from previously reported studies, including $BaTiO_3$ films synthesized using various physical and chemical deposition methods. The out-of-plane lattice expansion in other $BaTiO_3$ thin films is significantly larger than the values in current study, in which carefully growth control is implemented in synthesizing $BaTiO_3$ thin films with idealized crystal structure.

When the growth pressure is further increased from 60 mTorr to 70 mTorr, (partial) strain relaxation occurs. This is indicated by the double peak in the θ-2θ line scan, with the peak showing

at lower and higher angle representing the strained and the relaxed $BaTiO_3$ layers, respectively (Fig. 4.1a). The strain relaxation is further confirmed with RSMs, with the $BaTiO_3$ peak broadening and expanding towards the bulk position (Fig. 4.1b). Rocking curve studies are performed around the 002-peak of the $BaTiO_3$ layer (Fig. 4.1d), showing narrow curves with low full-width-at-half-maximum (FWHM) values in films grown between 20 mTorr and 60 mTorr, indicating the high crystallinity of the $BaTiO_3$ layer in the heterostructure. The FWHM of the 70 mTorr $BaTiO_3$, however, shows a somewhat larger FWHM value indicating a slight reduction in the crystallinity because of the partial relaxation, which is consistent with the θ-2θ line scan and the RSM (Fig. 4.1a,b).

In conclusion, the study of growth pressure reveals how small changes in the growth pressure can have significant impact on the structural properties of the synthesized $BaTiO_3$ layer. Careful control of the growth conditions must be implemented to achieve $BaTiO_3$ heterostructures with idealized crystal structures.

4.1.2 Effect on ferroelectric properties

Varying the growth pressure has an impact not only on the lattice parameters of the $BaTiO_3$ films, but also on the ferroelectric properties of the heterostructures. Increasing the growth pressure from 20 mTorr to 60 mTorr reduces the coercive field/voltage of the $BaTiO_3$ heterostructure (Fig. 4.2a). This, may also be related to the defect level inside the $BaTiO_3$ layers, which is discussed in section 4.1.1. Previous studies have suggested that defects in ferroelectric thin films can act as pinning points for domain-wall motion[108,148], and as a result, they hinder the ferroelectric switching and increase the electric field needed for polarization reversal[148]. In our case, the $BaTiO_3$ films grown at pressure of 20 mTorr, 40 mTorr and 60 mTorr have coercive filed of 49 kV cm^{-1}, 30 kV cm^{-1} and 16 kV cm^{-1}, respectively. A large imprint (> 1 V) is observed for $BaTiO_3$ films grown at 20 mTorr (Fig. 4.2a). While some studies suggest that the strain gradient in $BaTiO_3$ films can lead to a horizontal imprint in the PE loops[149,150], however, this is not the case in our work since all the $BaTiO_3$ films grown between 20 mTorr and 60 mTorr are epitaxially strained on the $GdScO_3$ (110) substrates (Fig. 4.1b). On the other hand, some other studies that focus on the same heterostructures as studied in this work [*i.e.*, $SrRuO_3/BaTiO_3/SrRuO_3/GdScO_3$ (110)] have suggested that the defect-dipoles introduced during the growth process can align in the out-of-plane direction and result in a horizontal imprint in the PE loops[64,108]. Therefore, it is suggested that the imprint observed in the $BaTiO_3$ films grown at 20 mTorr could also result from the defect-dipoles introduced during the growth. Further increasing the growth pressure from 60 mTorr to 70 mTorr does not increase the quality of the $BaTiO_3$ heterostructure any further. $BaTiO_3$ films grown at 70 mTorr go through strain-relaxation during the synthesis process (Fig. 4.1a,b), and presumably have higher defect level, resulting in a slightly increased coercive field of 17 kV cm^{-1}. The remanent polarization value also decreases from 26 μC cm^{-2} to 19 μC cm^{-2}, probably because of the decrease of the crystallinity in the $BaTiO_3$ films. A comparison is made between the ferroelectric properties (*i.e.*, coercive field, remanent polarization) in the $BaTiO_3$ films grown in this thesis and those grown in previous studies via different types of synthesis methods (Fig. 4.2b). An ideal $BaTiO_3$ film would be located in the middle to upper, left-hand region of this diagram and the worst-case scenario would be a $BaTiO_3$ sample in the bottom, right-hand corner. While the latter is readily observed, the former is very challenging. The films synthesized at a growth pressure of 60 mTorr, however, represent some of the best combinations of low coercive voltage

and reasonable remnant polarization reported to date. A reference standard is the single-crystal version of $BaTiO_3$ (red star, Fig. 4.2b) and, although it has a very small coercive field (~ 1 kV cm^{-1}), the coercive voltage is large (*i.e.*, in the range of 1-10 V) simply because such samples are thick (at least several tens of microns).The $BaTiO_3$ films synthesized in this study, however, can show commensurate polarization (> 10 μC cm^{-2}) while achieving this with a coercive voltage that is an order of magnitude or more lower (50-100 mV).

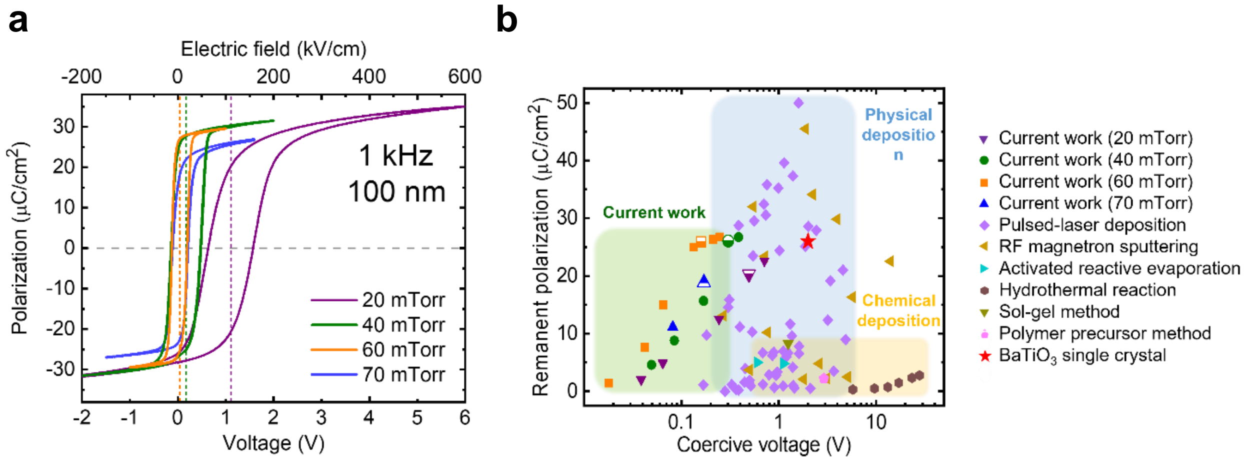


Figure 4.2 | Effect of growth pressure on the ferroelectric properties of the heterostructures. a, Polarization-electric field loops of 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) heterostructures grown under different O_2 pressure from 20 mTorr to 70 mTorr. The vertical dotted lines show the magnitude of the horizontal shift in the loops. **b**, Comparison of ferroelectricity in $BaTiO_3$ thin films between the current work and those in previously reported literature. Half-filled symbols represent the ferroelectric properties of 100-nm-thick $BaTiO_3$ layers grown under different growth pressures shown in **a**.

To summarize, by carefully controlling the growth condition in PLD process, the growth pressure of 60 mTorr offers $BaTiO_3$ heterostructures with the best structural properties with almost no out-of-plane lattice expansion and best ferroelectric properties up to date - smallest coercive voltage < 100 mV and commensurate remanent polarization with $BaTiO_3$ singly crystals.

4.2 Thickness scaling in $BaTiO_3$ heterostructures

Given the optimal growth condition discussed in Section 4.1, the next step is to explore what is the smallest coercive field that can be achieved in the $BaTiO_3$ heterostructures. The easiest way to reduce the coercive voltage of the $BaTiO_3$ thin film is to reduce the thickness of the film. Therefore, thickness scaling is performed on the $SrRuO_3$/$BaTiO_3$/$SrRuO_3$/$GdScO_3$ (110) heterostructures.

4.2.1 Coercive fields and voltages

$BaTiO_3$ films are synthesized within heterostructures of 30 nm $SrRuO_3$/*x* nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) with *x* ranging from 12.5 nm to 225 nm. X-ray θ-2θ line scans are performed on the heterostructures (Fig. 4.3a,b). For all thicknesses, the $BaTiO_3$ peaks are located

exactly at (or close to) the theoretical peak position (vertical dotted line, Fig. 4.3a,b), with almost no out-of-plane lattice expansion (*e.g.*, the out-of-plane expansion is as small as 0.16% for $BaTiO_3$ films thicker than 200 nm), indicating the high crystallinity in the $BaTiO_3$ heterostructures.

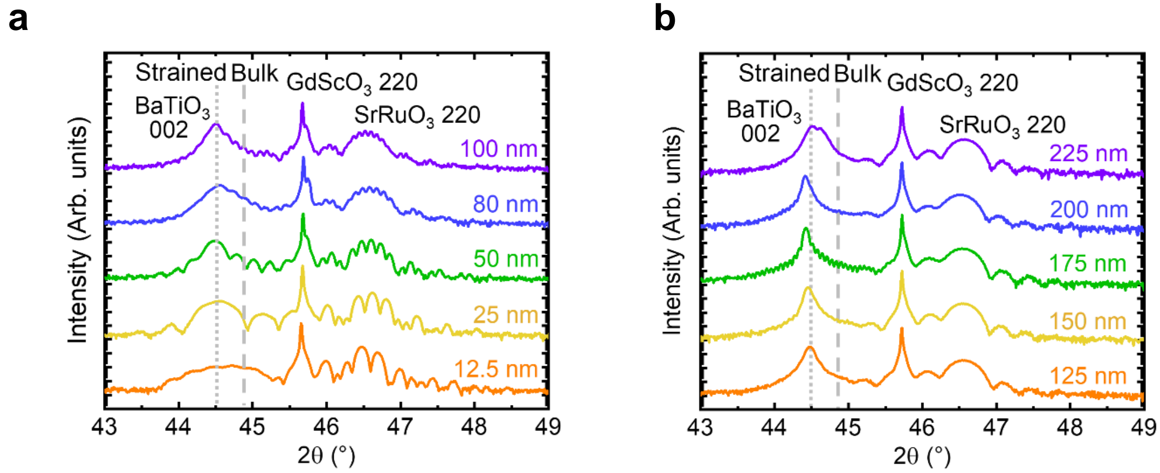


Figure 4.3 | θ-2θ line scans of 30 nm $SrRuO_3$/*x* nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) heterostructures with *x* ranging a, from 12.5 to 100, and **b**, from 125 to 225. The dashed lines show the peak positions for the bulk c-oriented $BaTiO_3$, and the dotted lines show the theoretical peak positions for the fully strained $BaTiO_3$ films on $GdScO_3$ (110) substrates.

The polarization-electric field loops are also measured for the heterostructures (Fig. 4.4a), and a plot is made for coercive field/voltage as function of $BaTiO_3$ thickness (Fig. 4.4b). The evolution of coercive field as a function of thickness reveals two different regimes. For $BaTiO_3$ films thicker than 150 nm, the coercive field reduces with thickness with a slope of -0.556, which matches the traditional Janovec-Kay-Dunn (JKD) law[151]

$$E_C \propto d^{-\frac{2}{3}} \quad \text{Equation 4.2}$$

$$V_C = E_C d \propto d^{\frac{1}{3}} \quad \text{Equation 4.3}$$

where d is the thickness of the $BaTiO_3$ film, E_C is the coercive field, and V_C is the coercive voltage.

However, in $BaTiO_3$ films thinner than 150 nm, the coercive field is essentially independent of the thickness, leading to a linear relationship between coercive voltage and film thickness which goes against the JKD scaling. Although the JKD scaling law has been observed in many ferroelectric systems[100,151,152], deviations can still occur. In some studies, the existence of interfacial dead layers between the ferroelectric material and the corresponding electrodes can introduce an extra voltage drop in the switching process[96] leading to a power index larger than 2/3 (*e.g.*, $E_C \propto d^{-1}$, V_C = constant). In other cases, a power index smaller than 2/3 can also occur. For example, epitaxial constraint can lead to structural transitions during thickness downscaling, and as a result, reduce the energy barrier for switching, thus weakening the power dependence[152]. In the ferroelectric switching process of some ultrathin ferroelectric films (*e.g.*, thickness < 15 nm), the shape of critical nuclei formed during the nucleation stage are usually cylindrical instead of the common half prolate shape that are formed in thick ferroelectric films. This can also result in a lack of

thickness dependence in the coercive field (*i.e.*, E_C = constant, $V_C \propto d$). However, this is not the case for the $BaTiO_3$ films shown in this study as the thickness of the $BaTiO_3$ films is very large (~150 nm). More often, deviations from JKD scaling can be resulted from the presence of depolarization fields caused by the incomplete screening of the corresponding electrodes[95,153,154], and therefore, lead to a measured coercive field that is smaller than the actual coercive field inside the ferroelectric films[155].

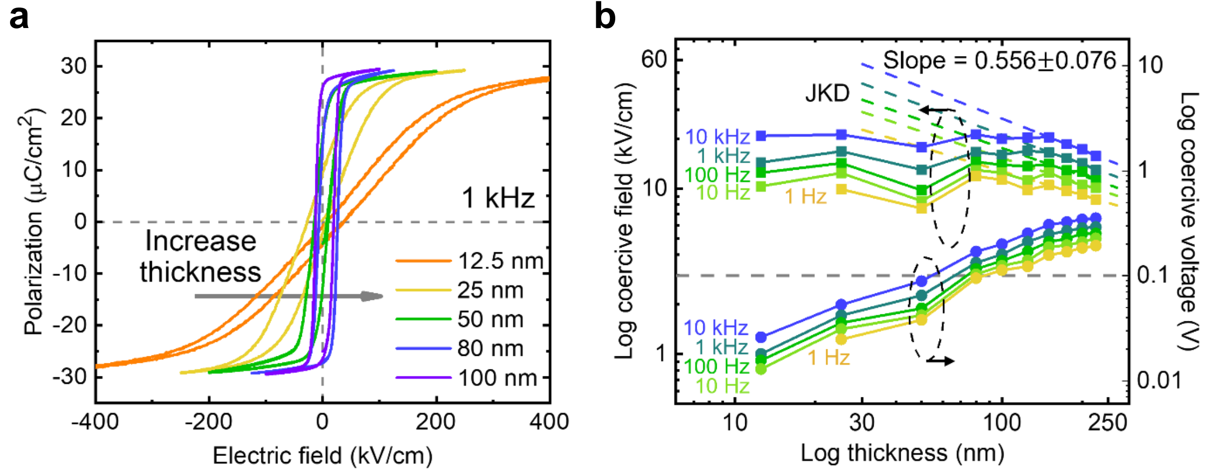


Figure 4.4 | Ferroelectric properties of 30 nm $SrRuO_3$/*x* nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) heterostructures. a, Polarization-electric field loop as a function of $BaTiO_3$ thickness. **b**, Extracted coercive field (squares, left y axis) and coercive voltage (circles, right y axis) as a function of $BaTiO_3$ thickness, measured at different frequencies. Dashed lines are linear fits for thick films (>150 nm). The horizontal dashed line marks the coercive voltage value of 100 mV.

4.2.2 Depolarization field

Depolarization field can cause a reduction in the measured coercive field smaller than the actual value in $SrRuO_3$/$BaTiO_3$/$SrRuO_3$ heterostructures. One can correct for the depolarization field value inside the ferroelectric materials and obtain the actual value of the coercive field[155]. Using the continuous condition for the electric displacement at the ferroelectric/electrode interface, we have

$$D_f = D_e \qquad \text{Equation 4.4}$$

where the subscript *f* and *e* stands for the corresponding physical quantity in film and electrode, respectively. Expressing the displacement vector, *D*, in electric field, *E*, dielectric constant, *ε*, and spontaneous polarization, P_S, we have

$$\varepsilon_f E_f - P_S = \varepsilon_e E_e \qquad \text{Equation 4.5}$$

It should be noted that in the case of an imperfect metal with incomplete screening at the interface, the metal shows some polar properties if an external electric field is applied[95,155]. The electric field, E_e, in the metal close to the interface cannot be fully screened out and therefore has a non-zero

value[155]. In addition, the dielectric constant, ε_e, in the metal will consist of two different parts[95]. One part is the contribution from free Drude carriers which can be described using a series of Lorentz oscillators[156] (as in the case of a theoretically-perfect metal), while the other part is the contribution from bound charges such as bound electrons and phonons[157], which can lead to a "polar" behavior in the electrode. In terms of correction for the depolarization field, only the bound charge contribution needs to be considered for ε_e in Eq 4.5.

The voltage drop, V, across the heterostructure, can be expressed as

$$E_f d + 2E_e\lambda = V \qquad \text{Equation 4.6}$$

where λ represents the characteristic Fermi-screening length in the $SrRuO_3$ electrodes. Combining Eq. 4.5 and Eq. 4.6, we can write the actual electric field inside the $BaTiO_3$ film as

$$E_f = \frac{V+2P_S\left(\frac{\lambda}{\varepsilon_e}\right)}{d+2\varepsilon_f\left(\frac{\lambda}{\varepsilon_e}\right)} \qquad \text{Equation 4.7}$$

It should also be noted that if the electrodes are perfect metals that can completely compensate for the charge at the ferroelectric/electrode interface, then the Fermi-screening length will no longer exist.

$$\lambda = 0 \qquad \text{Equation 4.8}$$

and Eq. 4.7 will simply reduce to

$$E_f = \frac{V}{d} \qquad \text{Equation 4.9}$$

This represents that the actual electric field inside the ferroelectric film is equal to the applied electric field.

Using Eq. 4.7, one can correct for the difference in the electric field between the measured value and the actual value and obtain the true coercive field inside the $BaTiO_3$ layer (Fig. 4.5a). V ranges in value from 0.026 to 0.355 V, and P_S ranges in value from 27.8 to 29.9 μC cm^{-2}. A screening length λ of 0.5 $\mathring{A}$ is used for $SrRuO_3$ top and bottom electrode, which is similar in magnitude to other common metal electrodes[154]. The dielectric constant of the $SrRuO_3$ electrode is set as $\varepsilon_e = 10\varepsilon_0$ (ε_0 is the dielectric permittivity of the vacuum), which is the dielectric contributions from bound charges in the $SrRuO_3$ crystal structures[95,154]. The dielectric constant of the $BaTiO_3$ film, ε_f, however, can vary from a few hundreds to a few thousands depending on the applied electric field[95,137] (Fig. 4.6). In our case, because most electrical measurements were performed with a voltage amplitude of 1 V, which corresponds to a relatively large applied field (*i.e.*, > 40 kV cm^{-1} in 100 nm film, > 75 kV cm^{-1} in 50 nm film, > 150 kV cm^{-1} in 25 nm film and > 250 kV cm^{-1} in 12.5 nm film), the dielectric constant of the film was estimated to be a relatively small value[137] (*i.e.*, $\varepsilon_f = 360\varepsilon_0$).

After the correction, the slope between the coercive field and the thickness is -0.668, matching the slope in traditional JKD scaling law (Fig. 4.5a). It is obvious that the depolarization field can have impact on ferroelectric films even with a thickness > 150 nm. This may be surprising as previous studies have introduced the concept of the "critical thickness" of the ferroelectric films, and some theoretical calculations have shown that the ferroelectric order can be maintained down to 2.4

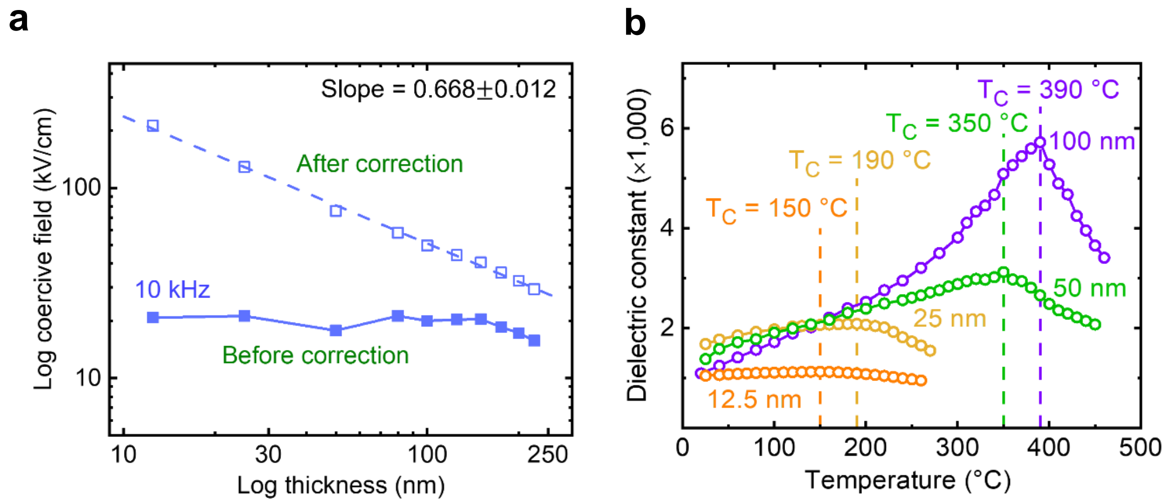


Figure 4.5 | Effect of depolarization field on the electric properties of the heterostructures. **a**, Depolarization correction of the coercive field. Coercive field as a function of $BaTiO_3$ thickness before (solid squares) and after (hollow squares) depolarization correction. The dashed line is fit to traditional JKD scaling law. **b**, Dielectric constant as a function of temperature for $BaTiO_3$ films with various thickness.

nm[153], while other experimental studies further confirmed the existence of polarization in films of just a few unit cell thick[158,159]. However, the critical thickness of the films only sets the ultimate size limit where the polarization completely disappears, they do not represent the thickness when the depolarization field starts to manifest and diminish the magnitude of the polarization. During the thickness downscaling, instead of kicking in at the critical thickness and abruptly eliminate the polarization order in a stepwise manner, the depolarization field starts to kick in at the thickness well above the critical value, and gradually reduces the polarization when the film thickness reduces, and finally eliminate the polarization value to zero when the thickness reaches the critical thickness. As has been discussed in Chapter 2, the introduction of compressive strain into the ferroelectric film will enhance the ferroelectric order, increase its stability against the depolarizing[64]. However, the depolarization field from the incomplete charge compensation at the ferroelectric/electrode interface can be so large that previous simulation studies[153] have suggested that even for $BaTiO_3$ films epitaxially grown on $SrTiO_3$ (001) substrate with a compressive strain of ~ 2.4% the polarization will still start to decrease in 15-nm-thick films (~38 unit cells) and be reduced to half when the thickness reaches 6 nm (~15 unit cells). Therefore, in the real electrode/ferroelectric/electrode heterostructures with imperfect electrode screening, the depolarization field is likely to manifest even when the ferroelectric layer is relatively thick (~ 100 nm) and its effect on Curie temperature (T_C) is expected.

To further confirm this, dielectric constant as a function of temperature measurement is performed on $SrRuO_3/BaTiO_3/SrRuO_3/GdScO_3$ (110) heterostructures with various $BaTiO_3$ thickness (Fig. 4.5b). The T_C Curie temperature for heterostructure with 100-nm-thick $BaTiO_3$ layer is 390 °*C*, which closely matches the value reported in previous studies[64,108,160]. When the thickness of the $BaTiO_3$ layer reduces, the T_C Curie temperature also decreases. For the thinnest $BaTiO_3$ layer thickness of 12.5 nm, the T_C Curie temperature reduces to 150 °*C*, which is very close to the T_C of bulk $BaTiO_3$ single crystal (~ 127 °*C*)[68,69], indicating the huge impact of the depolarization field

in thin $BaTiO_3$ film, almost eliminating the T_C enhancement introduced by the -0.99% compressive strain from the underlying $GdScO_3$ (110) substrate.

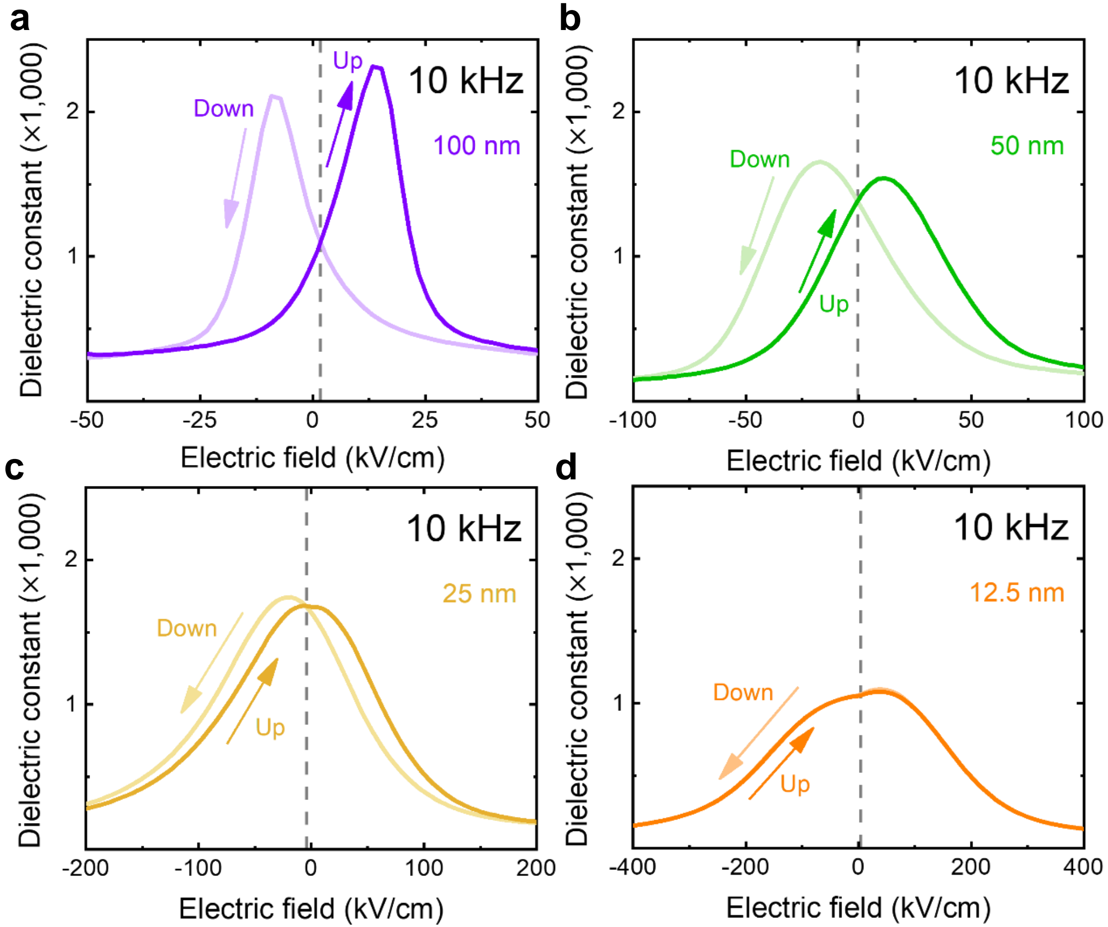


Figure 4.6 | Dielectric constant-voltage measurements. Dielectric constant as a function of applied electric field measured on **a**, 100-nm-, **b**, 50-nm-, **c**, 25-nm-, and **d**, 12.5-nm-thick $BaTiO_3$ thin films.

Although depolarization field can have deteriorative effect on the ferroelectric order stability and magnitude of remanent polarization, it also helps to reduce the coercive field of the ferroelectric materials. In $BaTiO_3$ films with thickness ranging from 25 to 50 nm, we have simultaneously achieved a low coercive voltage < 100 mV and a commensurate remanent polarization > 10 μC cm^{-2} (Fig. 4.2b), making these films strong candidate for low-voltage ferroelectric applications, such as FeFETs where low coercive voltages are needed to enable low-power operations[161] or FeRAMs where robust polarizations are needed for binary information storages[24].

In addition, the switching energy is also calculated for $BaTiO_3$ capacitors, and a comparison is made between the $BaTiO_3$ films in this study and other ferroelectric thin films in previously reported studies (Fig. 4.7a). The switching energies of the $BaTiO_3$ films grown under 60 mTorr are < 2 J cm^{-3}, corresponding to < 2 aJ per bit in a 10×10×10 nm^3 device. In comparison, the $BaTiO_3$ films in other studies, as well as $PbZr_xTi_{1-x}O_3$ thin films, have shown much larger switching energies, as well as bigger coercive voltages. This, in turn, has further indicated the

advantages of the $BaTiO_3$ films in the current study for low-voltage, low-power, non-volatile memory and logic devices, and their potential to enable the beyond-CMOS technologies.

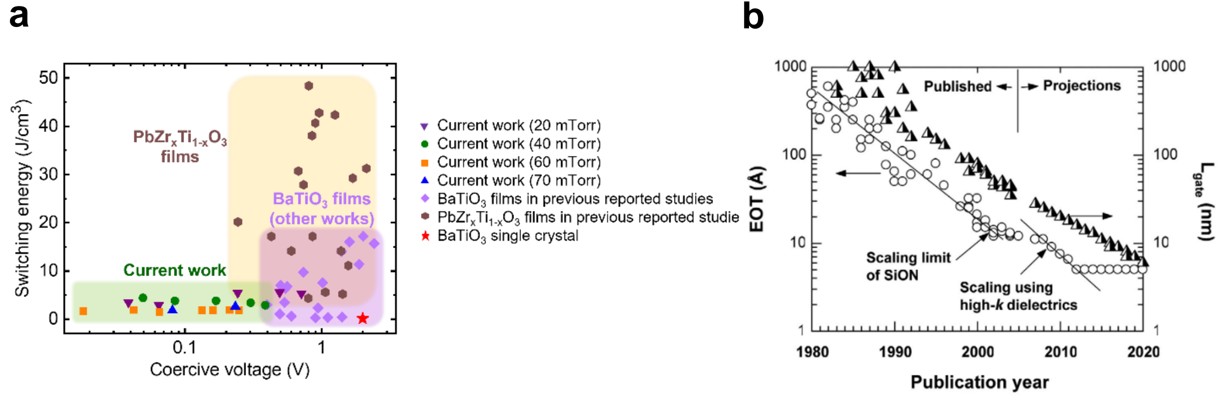


Figure 4.7 | $BaTiO_3$ thin films for device applications. a, Switching energies of the $SrRuO_3/BaTiO_3/SrRuO_3$ capacitors. A comparison is made of the switching energies between the $BaTiO_3$ films in the current work and $BaTiO_3$ films in previous reported studies, as well as those from $PbZr_xTi_{1-x}O_3$ thin films. **b**, Evolution of gate oxide thickness in MOSFET scaling. Adapted from ref. [162].

It should be noted that, as the technology node for MOSFET scaling has reached < 5 nm nowadays, gate oxides with thicknesses of only a few nanometers are needed (Fig. 4.7b)[162]. For the ferroelectric materials to be used in such devices, robust polarization must be stabilized in ultrathin film forms. The major issue, as discussed above, is the depolarization field that can drive remanent polarization to zero in ultrathin $BaTiO_3$ films. The magnitude of the depolarization field depends on the Fermi-screening length and therefore, on the free electron densities inside the electrode materials[163]. Increasing the electron density can reduce the Fermi screening length, and therefore, reduces the depolarization field inside the ferroelectric materials. Therefore, future efforts can be made in sandwiching ultrathin $BaTiO_3$ films using oxide metals with higher electron densities to maintain a robust remanent polarization in $BaTiO_3$ films < 25 nm thick. A detailed discussion is provided in Chapter 6.

4.3 Lateral scaling in $BaTiO_3$ capacitors

Besides the switching voltage and switching power, the switching voltage is another important figure of merit in industrial applications.

Previous studies have shown the switching time can be affected by both applied electric field[70] (Fig.4.8a) and the lateral size of the ferroelectric capacitor[139] (Fig. 4.8b). The effect of applied electric field on the switching time can be expressed using Merz's law

$$t_{sw} \propto e^{\frac{\alpha}{E}} \qquad \text{Equation 4.11}$$

where t_{sw} is the characteristic switching time of the ferroelectric capacitor, α is the activation energy of the switching and E is the applied electric field. As the applied electric field increases in magnitude, both the nucleation rate and the growth rate will increase for ferroelectric domains with

opposite polarization[139]. Switching-transient measurements were performed on our $SrRuO_3/BaTiO_3/SrRuO_3/GdScO_3$ (110) heterostructures using the method discussed in Chapter 3, where an switching of time ~ 2 ns can be achieved in 25-nm-thick $BaTiO_3$ films when increasing the applied electric field to ~ 2000 kV cm^{-1} (Fig. 4.8c), which is a switching time slightly faster than other ferroelectric materials with similar thickness (~2.4 ns for 20-nm-thick $BiFeO_3$ and ~2.7ns for 20-nm-thick $Bi_{0.85}La_{0.15}FeO_3$). However, at low applied electric field region, a much faster switching time is observed in $BaTiO_3$ capacitors than in $BiFeO_3$ and $Bi_{0.85}La_{0.15}FeO_3$ capacitors, indicating the advantage of $BaTiO_3$ over other ferroelectric materials.

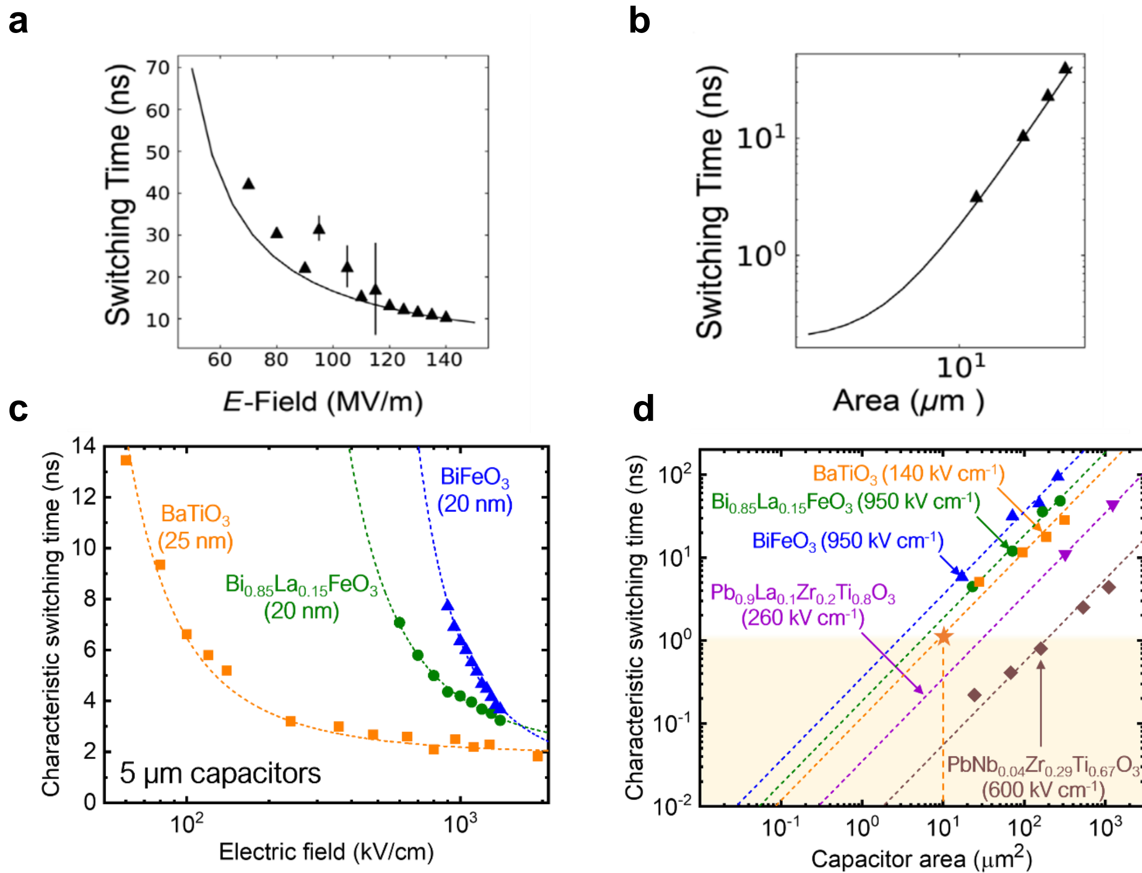


Figure 4.8 | Switching speed properties of the ferroelectric heterostructures. a, Switching time as function of electric field for 20-nm-thick $BiFeO_3$ films. **b**, Lateral scaling of switching time for 20-nm-thick $BiFeO_3$ films. **c**, Switching time as a function of electric field for common ferroelectric materials, including 25-nm-thick $BaTiO_3$, 20-nm-thick $BiFeO_3$, and 20-nm-thick $Bi_{0.85}La_{0.15}FeO_3$ films. Dashed curves are fits to Merz's law of ferroelectric switching. **d**, Lateral scaling of switching time for 25-nm-thick $BaTiO_3$ films in this study, as well as other common ferroelectric thin films. Linear fits to the data are shown as the dashed lines. Adapted from ref. [139].

Previous studies have suggested that, as the lateral size of the electrode/ferroelectric/electrode capacitor shrinks, the switching time also reduces for the whole switching process[139]. Therefore, for the purpose of reaching < 1 ns for ultrafast applications[44], it is of interest to investigate the evolution trend of the switching speed with reducing capacitor areas by performing a lateral scaling study in the $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructure (Fig. 4.8d). Shown together is the switching

speed data on lateral scaling for other common ferroelectric materials. While the $BaTiO_3$ film has similar switching time with other ferroelectrics, it requires a much less electric field (~140 kV cm^{-1}) to achieve such switching speed. According to the linear fits to the data point, sub-nanosecond switching can be achieved if the lateral size of the $BaTiO_3$ capacitor is reduced to 10 μm^2, which corresponds to a diameter of 3.5 μm (orange star, Fig. 4.8d). This has indicated the potential for $BaTiO_3$ films to be used for real ferroelectric applications.

Additionally, the switching kinetics studies were performed in order to examine the switching mechanisms in our heterostructures. Previous studies have proposed multiple models through which the ferroelectric switching process can be described, such as the classic Kolmogorov-Avrami-Ishibashi (KAI) model[164] (*i.e.*, the switching process is completed through domain nucleation and the following unrestricted growth until they coalesce with other domains), nucleation limited switching model[165] (*i.e.*, the switching is limited by the nucleation of reversed domains where the characteristic switching time follows Lorentzian distribution and differs across the ferroelectric films), etc. The KAI model is much more common and have been used to successfully describe ferroelectric switching processes in multiple thin-film ferroelectric systems[160,166]. In KAI model, the switched polarization follows[166]

$$\Delta P \propto \left[1 - \exp\left(-\left(\frac{t}{t_0}\right)^n\right)\right] \quad \text{Equation 4.12}$$

where t_0 is the characteristic switching time, and n is the dimension factor, which typically equals 2 for thin-film systems. A representative polarization-transient curve obtained from switching-transient measurement is shown and the KAI model yields a good fitting, suggesting the domain-nucleation-and-growth switching mechanism in our heterostructures (Fig. 4.9a).

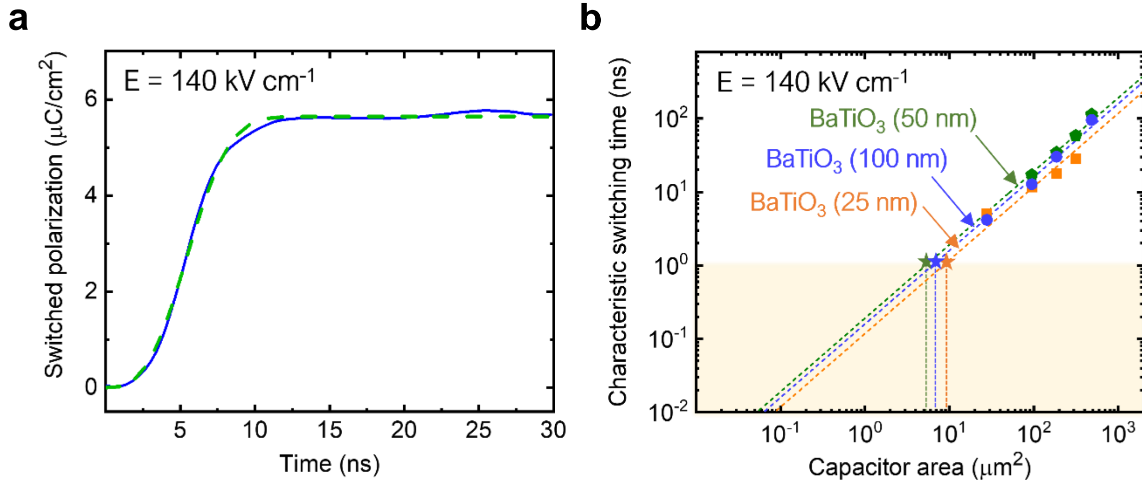


Figure 4.9 | Switching kinetic studies on the heterostructure. a, Representative polarization-transient curve obtained from switching-transient measurement (blue solid curve, from 25-nm-thick $BaTiO_3$ films on a 5 μm capacitor) and fitting using KAI model (green dashed curve). **b**, Characteristic switching time as a function of capacitor area measured on 25-, 50-, and 100-nm-thick $BaTiO_3$ films. Dashed lines are linear fits to the data. The stars are the projected capacitor areas below which sub-ns switching time can be achieved.

The ferroelectric switching process in thin films typically starts with domain nucleation, followed by forward domain growth across the thickness of the film, and subsequent sideways growth across

the capacitor area. Previous studies have suggested the timescale for forward domain growth in thin films is typically very short (<100 ps), while the sideway domain can take ~ ns or longer[71]. Therefore, the forward domain growth contributes very little to the total switching time and the sideway domain growth is the rate-limiting step in the switching process[160]. As a result, the heterostructures with different $BaTiO_3$ thicknesses should have similar switching times under same applied electric field, which agrees with our observation in the lateral scaling trend for 25, 50 and 100 nm $BaTiO_3$ films (Fig. 4.9b).

Another thing that should be noted is the asymptote behavior of the switching time at small capacitor areas is also observed (Fig. 4.8b,d; Fig. 4.9b), which would probably set a limitation to the switching speed in ultrasmall capacitor regime. This can likely result from extrinsic factors in the measurement circuits[140] as well as intrinsic limits in the switching of ferroelectric materials[139] and requires further study, which is discussed in Chapter 6.

4.4 Integration onto silicon-based substrates

If $BaTiO_3$ films are to be integrated onto the CMOS circuit for low-power, low-voltage and ultra-fast ferroelectric applications, it is also important to study the possibility of integrating such films onto silicon-based substrates, which still poses one of the greatest challenges for the applications of perovskite films onto the Si-based CMOS platform[24]. Previous studies have shown $BaTiO_3$ films grown on silicon platform that show "good" quality in TEM images[83,86] but demonstrated poor ferroelectric properties. Some of them have large coercive fields[83,84,100,109] while other have almost zero remanent polarizations[94], which puts the real utilization of $BaTiO_3$ films into question. Here, we explored the possibility of integrating $BaTiO_3$ films onto the 20-nm-thick $SrTiO_3$ buffered silicon substrate, which is readily available and manufacturable by the industry-scale molecular beam epitaxy[167]. Because of the large difference in thermal expansion coefficients between the perovskite $BaTiO_3$ and the underlying silicon substrate, as well as the large lattice mismatch between the $BaTiO_3$ and the $SrTiO_3$ buffer layer[100,168], huge elastic and thermal stress are introduced into the system, especially during the cooling down phase after the heterostructure synthesis. As a result, strain-relaxation is observed in the $BaTiO_3$ films and the θ-2θ line scan shows a mixture of strained $BaTiO_3$ phase, relaxed bulk-like c-oriented $BaTiO_3$ phase and the relaxed bulk-like a-oriented $BaTiO_3$ phase (Fig. 4.10a,b). The existence of multiple phases inside the $BaTiO_3$ films is an indication that such $BaTiO_3$ films contain high defect concentration, which manifest themselves as an imprint in the PE loop[64,108,148] (Fig. 4.10c). The coercive field for the heterostructure grown on silicon-based substrates (~16.5 kV cm^{-1}), however, is very similar to that grown on $GdScO_3$ (110) substrates (~16.0 kV cm^{-1}), and is only slightly larger than that of the freestanding heterostructure transferred onto silicon (~13.0 kV cm^{-1}).

While the large compressive strain introduced into the $BaTiO_3$ layer by the $SrTiO_3$ can increase the coercive field[62,160], and the existence of the defect, especially the point defect, can pin domain wall motion during the ferroelectric switching and therefore also increase the coercive field[148], the formation of the relaxed bulk-like $BaTiO_3$ phase, which intrinsically has a low coercive field[62] of ~1 kV cm^{-1}, would greatly reduce the measured coercive field of the whole heterostructure. All these effects would combine together, giving an average coercive field of ~16.5 kV cm^{-1}. To assess the performance of the heterostructure as an actual device on Si platform, fatigue and retention

measurement is performed on the 30nm $SrRuO_3$/100nm $BaTiO_3$/30nm $SrRuO_3$/20nm $SrTiO_3$/Si (001) heterostructure (Fig. 4.10d,e).

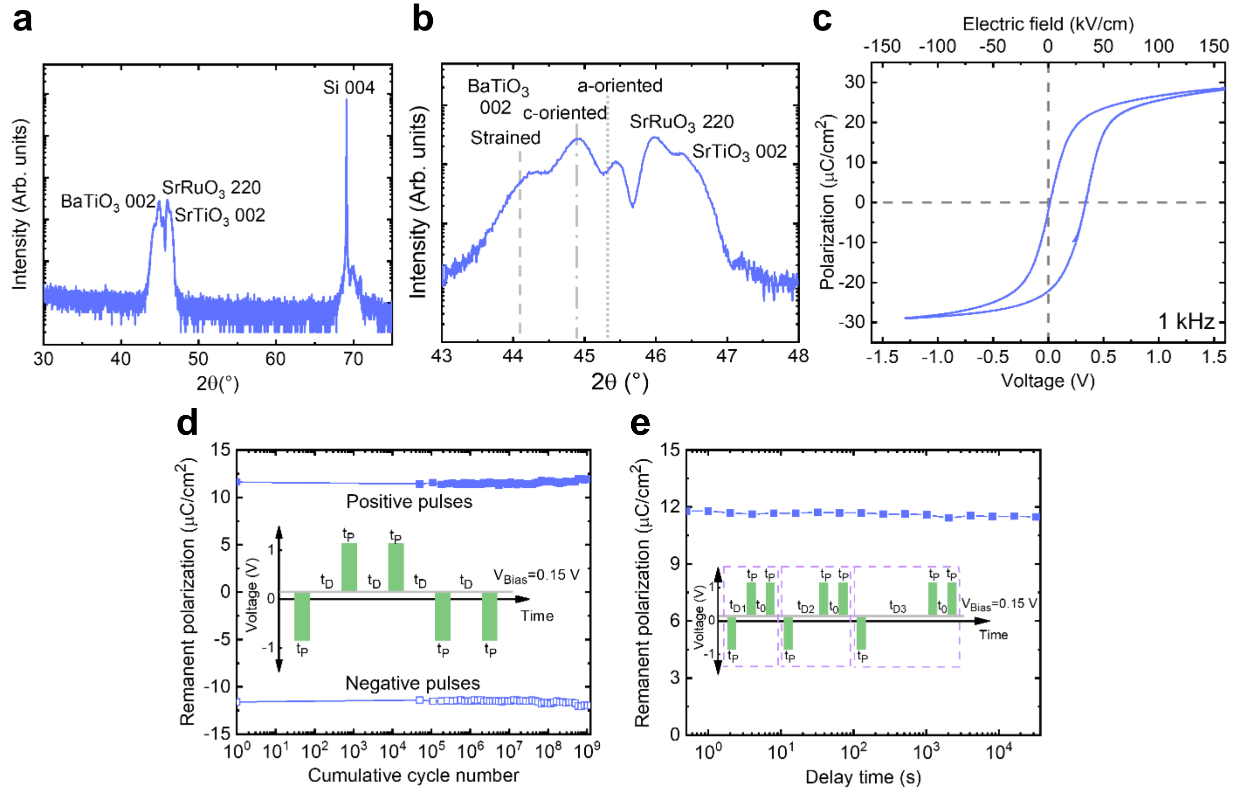


Figure 4.10 | Structural and ferroelectric characterizations of the heterostructures grown on $SrTiO_3$ buffered Si substrate. a, Long range θ-2θ line scans of 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/20 nm $SrTiO_3$/Si (001) heterostructure. **b**, Short-range scan for the heterostructure measured in **a**. **c**, Polarization-electric field loop for the heterostructure. **d**, Fatigue measurement and **e**, retention measurement of the heterostructure. The insets in **d** and **e** show the pulse train used to probe the remanent polarization during the process of fatigue and retention measurement, respectively. A bias of 0.15 *V* is applied to compensate for the imprint in the PE loop.

Similar to the fatigue and retention set up discussed in Chapter 3, pulse train is applied to the heterostructure to perform the fatigue and retention measurement. Same pulse height, pulse width and delay time are used with $V_P = 1\ V$, $t_P = 0.15\ ms$, $t_D = 1\ ms$ in fatigue set up and $V_P = 1\ V$, $t_0 = 1\ ms$ and a varying t_{Dn} in retention set up. A bias of 0.15 *V* is applied to compensate for the imprint in the PE loop. The result has shown the robustness of the remanent polarization against the cycling stress and time, indicating the possibility for the $BaTiO_3$ films to be applied to actual ferroelectric devices.

4.5 Conclusion

By carefully adjusting the growth parameters in the synthesis of $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructure, idealized structural and ferroelectric properties that are comparable to bulk single crystal can be achieved. The out-of-plane lattice parameters show almost no expansion and some of the best combination of small coercive field/voltage and relatively large remanent polarization are realized. The defects introduced during the growth can highly impact the properties of $BaTiO_3$ films, with a growth O_2 pressure of 60 mTorr gives best film performance. Thickness scaling is performed to explore the smallest coercive voltage available, with $BaTiO_3$ films with thicknesses ranging from 25-50 nm being best candidate for ferroelectric applications. Depolarization field starts to manifest in relatively thick $BaTiO_3$ films and has the effect of helping to reduce the coercive voltage and the switching energy. Lateral scaling on the $SrRuO_3/BaTiO_3/SrRuO_3$ capacitors is performed to explore the smallest switching speed, with a projection area of 10 μm^2 for nanosecond switching speed. Finally, integration of $BaTiO_3$ capacitors onto Si-based substrate is explored, with similar ferroelectric properties observed with those grown on scandate substrates. To summary, we have shown the great advantages of the $BaTiO_3$ over other common ferroelectric materials in terms of ferroelectric applications and the great potential of $BaTiO_3$ films to be integrated into such devices.

Chapter 5

Effect of Fabrication Processes on $BaTiO_3$ Properties

This chapter explores the effect that different fabrication processes have on the ferroelectric properties of the prototypical $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures studied in this dissertation. First, an *ex situ* MgO hard-mask process is explored and the resulting polarization-electric field hysteresis loops from capacitors made in this manner exhibit significant horizontal imprints. From there, I discuss two different types of *in situ* growth followed by etch processes, namely, wet etching of the top contact using $NaIO_4$ and dry etching using an ion beam (*i.e.*, ion milling). The polarization-electric field hysteresis loops for both the *ex situ* and *in situ* methods are compared. For the ion-milling process, it is found that the Ar^+ beam can introduce defects into $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures and that the milling depth can influence the defect concentration inside the heterostructures and, as a consequence, can change the imprint of the fabricated capacitors as well as the leakage current. Finally, to reduce the horizontal imprint of the $BaTiO_3$ capacitors, defects can be removed by adding additional barium into the ferroelectric material via a CVD-style process, thus "fixing" the problems induced by the fabrication processes.

5.1 *Ex situ* hard-mask processes

To obtain $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures with idealized electrical properties for real applications, simply adjusting the growth parameter during the synthesis process is not enough. In fact, for the heterostructures to be successfully integrated into real devices based on electrode/ferroelectric/electrode capacitor structures one must be able to fabricate the materials in exacting ways[24]. While different fabrication processes can be implemented, these processes can introduce defects at different locations within the capacitor structures, including the electrode/film interface[169], as well as the body of the ferroelectric films itself[170,171]. Therefore, these fabrication processes can have significant impacts on the ferroelectric properties of the measured capacitors.

One of the processes used to define and fabricate $SrRuO_3/BaTiO_3/SrRuO_3$ capacitor structures is to utilize an *ex situ* grown MgO hard mask (Fig. 5.1). This process was developed in 2012[169], in an effort to enable high performance ferroelectric capacitors with low leakage, excellent fatigue resistance, and great endurance to high temperatures, overcoming the deleterious effects brought by poor metal contacts. The MgO hard mask is compatible with elevated temperature and can offer selective area epitaxy for top electrode depositions and fabrications. It has been used to fabricate features as small as 8 μm in lateral size and can be used to define top contact in nanoscale ferroelectric devices[169]. In this process, instead of growing the tri-layer $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructure *in situ*, the first step is to grow only the 30-nm-thick bottom $SrRuO_3$ layer and the ferroelectric $BaTiO_3$ layer on the substrate. After the growth, the sample is removed from the chamber and photoresist is then spun on to the bi-layer heterostructures and circular capacitor patterns are made to define the final location for the top $SrRuO_3$ electrodes. A 300-nm-thick MgO hard mask is then deposited on the bilayer in the same PLD system using the growth condition provided in Table 5.1. Following the room-temperature growth, the photoresist and the unwanted MgO are then removed using acetone, leaving an MgO layer with holes (where the future electrodes will be located) on the top of the bilayer heterostructure. Oxygen plasma cleaning is performed to remove any residual photoresist at the top of the $BaTiO_3$ surface. Then the heterostructure is returned to the PLD chamber and a 30-nm-thick top $SrRuO_3$ layer is deposited using the condition provided in Table 5.1, which is the same growth condition used to deposit the bottom $SrRuO_3$ layer. After the growth, the heterostructure is dipped into a 15% phosphoric acid (*i.e.*, H_3PO_4) solution to selectively remove the remaining MgO hard mask and the unwanted top $SrRuO_3$[169].

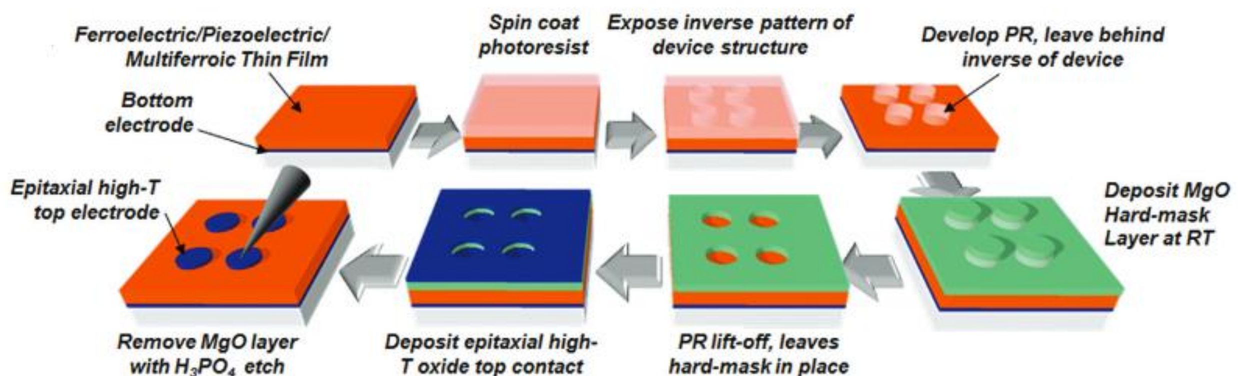


Figure 5.1 | Process flow for *ex situ* MgO hard mask in $SrRuO_3/BaTiO_3/SrRuO_3$ capacitor fabrication. From ref. [169].

Materials	MgO	Top $SrRuO_3$
Target type	Ceramic	Ceramic
Target composition	MgO	$SrRuO_3$
Substrate temperature	Room temperature	690 °C
Oxygen pressure	20 mTorr	100 mTorr
Laser wavelength	248 nm	248 nm
Laser pulse energy	150 mJ	100 mJ
Laser spot size	0.0520 cm^2	0.0744 cm^2
Laser fluence	2.89 J cm^{-2}	1.34 J cm^{-2}
Laser frequency	15 Hz	15 Hz
Target-substrate distance	5.5 cm	5.5 cm

Table 5.1 | Growth conditions for MgO hard mask and top $SrRuO_3$ electrode in PLD.

Following the growth processes, the ferroelectric properties are measured for the 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) capacitor structures (Fig. 5.2). As can be seen, the polarization-electric field hysteresis loops of the capacitor fabricated via *ex situ* MgO hard-mask process exhibit horizontal imprint (~0.7 V), which is likely caused by exposing the top $BaTiO_3$ interface to an array of environmental factors during the fabrication process (*e.g.*, photoresist, acetone, pollutants in the air). While an oxygen plasma cleaning is performed, it seemingly cannot fully heal the surface contamination and the defects introduced in the process. Similar capacitor structures are also fabricated via *in situ* growth and subsequent etching processes, in which the top $BaTiO_3$ surface is not exposed to the environment, which will be discussed in the next section.

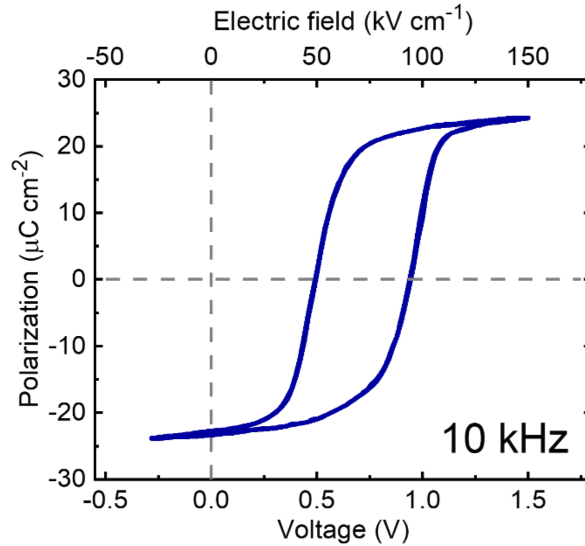


Figure 5.2 | Ferroelectric properties of 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) capacitor structures. Polarization-electric field loop for capacitor structures fabricated via *ex situ* MgO hard mask process.

5.2 *In situ* growth and etching processes

As has been discussed, the *ex situ* MgO hard mask process can introduce unwanted surface defects during the fabrication processes, leading to a reduction in the quality of the top $SrRuO_3/BaTiO_3$ surface which results in a horizontal imprint in the ferroelectric loops. Naturally, one would explore the option where all the layers of the tri-layers are deposited in one single growth in the PLD chamber. By limiting the contact between the films and the outside environment, one could avoid the introduction of unnecessary contamination in the heterostructures. After the synthesis, $SrRuO_3/BaTiO_3/SrRuO_3$ capacitor structures are defined using etching methods, either via wet chemical etching or dry ion milling.

5.2.1 Wet-chemical etching

Complex metal oxides such as $La_{0.67}Sr_{0.33}MnO_3$ and $SrRuO_3$ are widely used as electrodes material in ferroelectric capacitors for their good conductivity and high compatibility with the perovskite ferroelectric material lattice[64,108,152,172]. Additionally, their resistance to moisture and alkaline aqueous solutions to which they can be exposed during photolithography makes them good candidates for ferroelectric capacitor fabrication[173]. After photolithography, selective chemical etching methods can be used to remove the top electrode materials to define circular capacitor structures[174] (Fig. 5.3). The chemical reactions are usually based on reduction or oxidation of certain elements in the electrode from an insoluble solid state into a more soluble aqueous state. To etch $La_{0.67}Sr_{0.33}MnO_3$, for example, the Mn^{4+}, as in insoluble MnO_2, needs to be reduced to Mn^{2+}, which is soluble in water. Different reducing agents can be used to achieve this purpose, such as HCl solution with KI[172], and NH_3-buffered HF solutions[175]. In this dissertation, both the bottom and top electrodes are $SrRuO_3$, and to etch $SrRuO_3$, instead of using reducing agents, the Ru^{4+}, as in insoluble RuO_2, needs to be oxidized to Ru^{8+}, as in RuO_4, which is volatile and can easily be dissolved by water molecules[174].

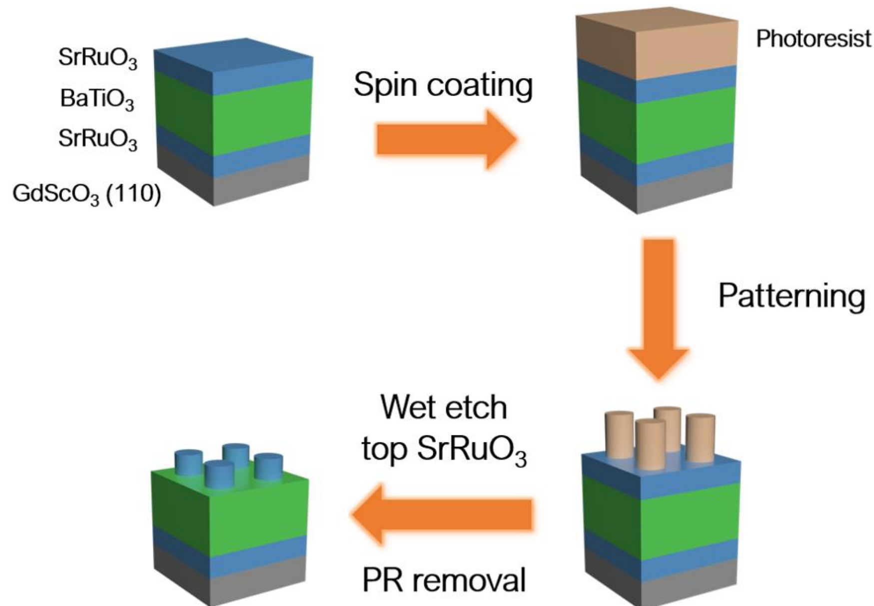
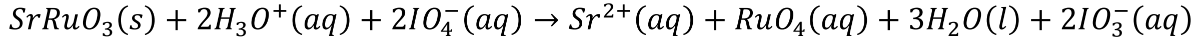


Figure 5.3 | Process flow in $SrRuO_3/BaTiO_3/SrRuO_3$ capacitor structure fabrication using wet chemical etching.

The oxidizing agent used in this study is a 0.1 mol L^{-1} $NaIO_4$ solution and the most common reaction during the etching process is[174]:



$$SrRuO_3(s) + 2H_3O^+(aq) + 2IO_4^-(aq) \rightarrow Sr^{2+}(aq) + RuO_4(aq) + 3H_2O(l) + 2IO_3^-(aq)$$

Equation 5.1

During the wet etching, the surface resistivity was measured using an ohmmeter every 5 s to control the etching progress. After 30 s, the surface resistivity is measured to be out-of-range, which indicates that the top $SrRuO_3$ layer is etched away. This results in a wet etch rate for $SrRuO_3$ thin films of ~1 nm s^{-1} in our study. An over-etching of 5 s was performed. After the wet etching, the ferroelectric properties are measured for 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) capacitor structures (blue curve, Fig. 5.4a). The polarization-electric field hysteresis loops are centered with close to zero horizontal imprint (~0.01 V). Therefore, the *in situ* growth and wet chemical etching appear to be advantageous as compared to the *ex situ* MgO hard-mask process in terms of fabricating symmetric capacitor structures, presumably because of a more symmetric interface between $BaTiO_3$ layer and top/bottom $SrRuO_3$ electrodes in the process.

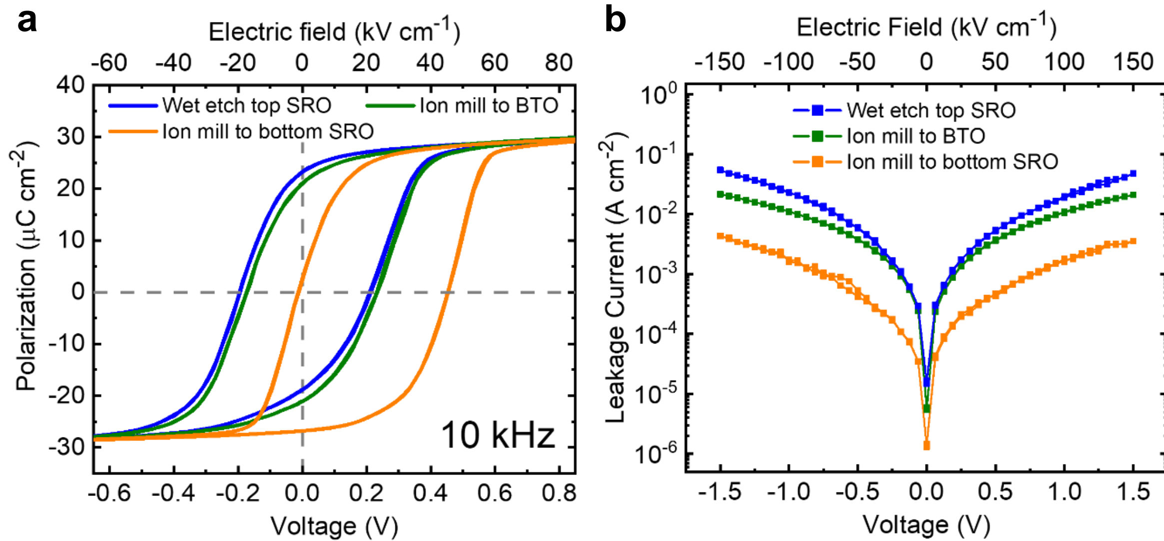


Figure 5.4 | Electrical properties of the capacitor structures fabricated using different methods. a, Polarization-voltage/electric field loops are measured for 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) heterostructures fabricated by wet etching top $SrRuO_3$, ion milling to $BaTiO_3$ and ion milling to bottom $SrRuO_3$. **b**, Room temperature leakage current-voltage/electric field measurements for the corresponding heterostructures.

5.2.2 Dry-ion milling

While wet-chemical etching can be used to define simple capacitor structures by removing unwanted top electrode material with highly selective etchants, in most cases, more complex 3D device structures are needed for measuring the structural, electrical properties of the ferroelectric materials, such as pyroelectric and electrocaloric devices[176,177], Hall bars[178], as well as wire bonded structures used for *in operando* X-ray diffraction[179] and, looking forward, realistic devices in commercial electronics. In the fabrication of these devices, not only the top electrode, but also the

ferroelectric films need to be etched[24]. Because of the high selectivity of the wet etching, it is sometimes difficult to find the right chemical etchant for the ferroelectric films. Besides, the non-directional isotropy nature of the wet etching can often lead to poor maintenance of feature sizes – especially for small features, as well as curved sidewalls, which are not desired in fabrication processes for such devices[174].

Therefore, it is necessary to explore alternative methods to compensate for the wet-chemical-etching processes, namely, dry-ion-milling, to remove unwanted material. One of the common types is argon-ion milling wherein Ar^+ ions are generated inside an ion gun. These Ar^+ ions are accelerated by an applied electric field and can gain enough kinetic energy to bombard the sample surface. With the bombardment, atoms or atom clusters are removed from the heterostructures and the capacitor structures can be fabricated. The highly energetic Ar^+ beams can be used to etch almost any type of material and can result in relatively flat sidewalls which is beneficial for fabricating complex device structures[180]. In this study, after the photolithography, the

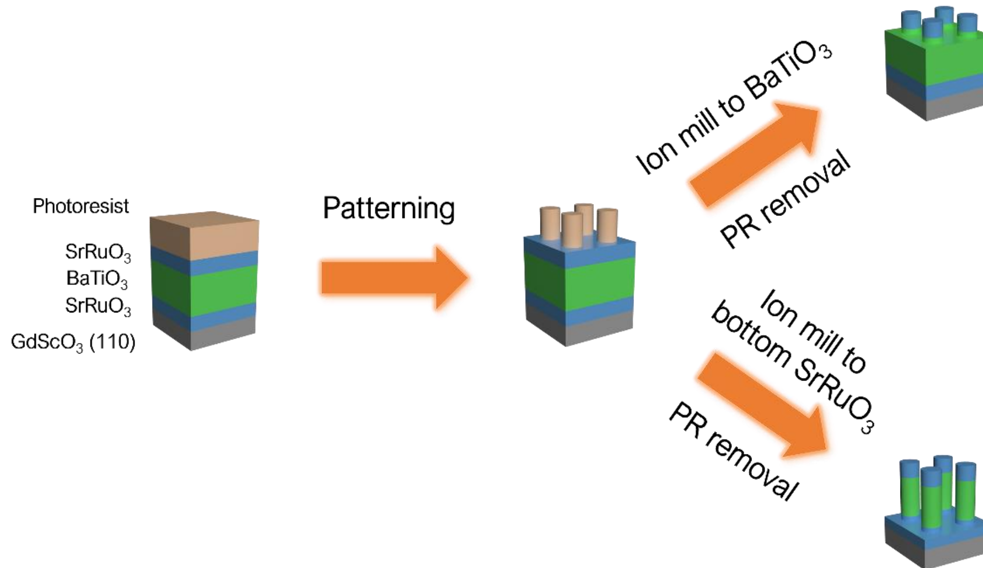


Figure 5.5 | Process flow in $SrRuO_3/BaTiO_3/SrRuO_3$ capacitor structure fabrication using dry-ion milling. Two different milling depth, namely, ion milling to $BaTiO_3$ layer and ion milling to bottom $SrRuO_3$ are shown.

$SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures were ion milled, and different milling times are explored (Fig. 5.5) to study the effect of milling damage to the capacitor properties.

Since ion milling is not a selective etching method, and metal oxide materials tend to have similar etching rates, care must be taken to control the process. To control the milling depth, a full milling profile was measured for the whole 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3/GdScO_3$ (110) heterostructure using *in situ* end-point detection via secondary ion mass spectroscopy (SIMS). During the ion milling process, the SIMS detector is placed near the sample surface to accept the ion species sputtered from the heterostructures, and the intensity of strontium and barium signals are monitored in real-time (Fig. 5.6).

The interface locations can be (roughly) determined from the SIMS profile. The Ar^+ ion beam reaches the top $SrRuO_3/BaTiO_3$ interface at around $t \approx 135\ s$ and, in turn, reaches the $BaTiO_3$/bottom $SrRuO_3$ interface at $t \approx 605\ s$ (Fig. 5.6). It should be noted that anomalous peaks

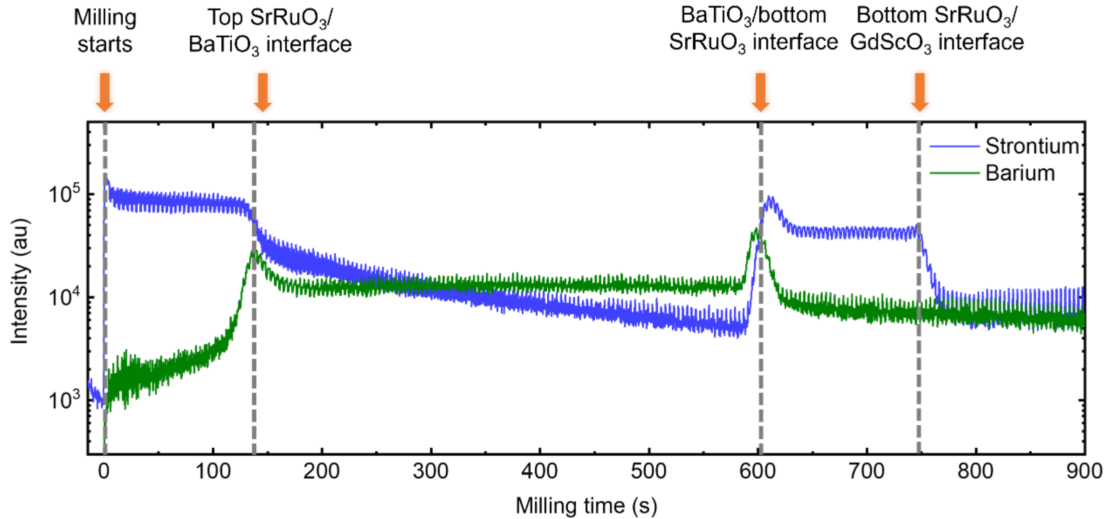


Figure 5.6 | Secondary ion mass spectroscopy profile during the ion milling. SIMS signals of strontium and barium are monitored for ion milling through 30 nm $SrRuO_3$/100 nm $BaTiO_3$/30 nm $SrRuO_3$/$GdScO_3$ (110) heterostructure. A polar milling angle of 45° is used, and the sample stage spins at a constant speed of 15 rounds per minute.

are observed at the interfaces during the milling process. These peaks arise from the so-called matrix effect in the SIMS measurement. The uneven milling front, atomic mixing between different sputtered ion species, different sputtering yields for sample species at the interface, as well as radiation-enhanced diffusion at the interface can broaden the SIMS profile and lead to features such as interfacial peaks or a long decay tail in ion signals[181,182]. These anomalous features have been widely observed[181,183,184], and as a result, the resolution of the SIMS at the interface is usually not perfect and it makes determining the exact interface locations difficult. As such, one should probably slightly over mill the layer to ensure all the unwanted material is removed from the heterostructure. In this case, an extra milling time of 40 *s* was used, corresponding to a total milling time of t = 175 *s* for the heterostructures that are milled just through the top $SrRuO_3$ layer into the $BaTiO_3$ layer and t = 645 *s* for the heterostructures that are milled entirely through the $BaTiO_3$ layer into the bottom $SrRuO_3$ layer. Atomic force microscopy scanning on capacitors reveals an over-milling depth of ~8 nm into the $BaTiO_3$ layer and ~10 nm into the bottom $SrRuO_3$ layer, respectively.

Ferroelectric properties of the ion-milled $SrRuO_3$/$BaTiO_3$/$SrRuO_3$ capacitors are measured (green and orange curves, Fig. 5.4a). Compared to the polarization-electric field hysteresis loops obtained from the wet-etched capacitor which shows a small horizontal shift of ~0.01 V (1 kV cm^{-1}), the ion-milled capacitors show a slightly increased imprint in the polarization-electric field hysteresis loop measurements, where upon milling to the $BaTiO_3$ layer and milling to bottom electrode the loops are shifted by ~0.03 V (3 kV cm^{-1}) and ~0.22 V (22 kV cm^{-1}), respectively. Room temperature (*i.e.*, 300 K) leakage current-voltage measurements were also performed on the heterostructures, and the wet-etched heterostructures show the highest leakage currents while the heterostructures that are ion milled to the bottom $SrRuO_3$ show the lowest leakage currents (Fig. 5.4b).

It should also be noted that, in some other studies, an imprint value of ~0.22 V (22 kV cm^{-1}; *i.e.*, the largest imprint observed in our study) would have be considered "insubstantial" in terms of the polarization-electric field hysteresis loop symmetry, where ferroelectric films with similar

thicknesses exhibit very wide polarization-electric field hysteresis loop widths ($|E_c^+ - E_c^-|$; *e.g.*, > 140 kV cm^{-1} in $BaTiO_3$[64,108], > 200 kV cm^{-1} in $PbZr_{0.2}Ti_{0.8}O_3$[152,185], > 300 kV cm^{-1} in $BiFeO_3$[166], etc.). In these cases, an imprint of ~22 kV cm^{-1} would not cause significant impact on the polarization-electric field hysteresis loop symmetry (and remnant polarization values). In our case, however, since the $BaTiO_3$ films grown at the optimal growth pressure of 60 mTorr shows a very small coercive field (~23 kV cm^{-1} at 10 kHz), even an imprint of 22 kV cm^{-1} completely shifts the polarization-electric field hysteresis loops to the positive side (Fig. 5.4a). Therefore, the small imprint can no longer be ignored and an analysis of the imprint (and how to remove it) is required.

5.2.3 Transport measurement

The kinetic energy of the incident Ar^+ ion is ~800 eV (beam current density ~0.72 mA cm^{-2}) during the milling processes, which is comparable (and perhaps a bit higher) to the kinetic energy of the plasma species during the PLD synthesis (*i.e.*, average of 10s-100s eV depending on the growth parameters)[186] and both can introduce knock-on defects (*i.e.*, point defects, defect dipoles, etc.)[63] into the heterostructures[174,187,188]. Previous studies have suggested the degradation of electric properties in ferroelectric capacitors caused by the Ar^+-ion-milling process, including increased coercive field[189,190], increased imprint[191-194], and suppressed remanent polarization[193-195]. Imprint > 0.8 V was reported in $PbZr_{1-x}Ti_xO_3$ capacitors fabricated using Ar^+-ion milling[190,191,193], and is thought to be caused by charged defects (and defect dipoles) and charge-carrier traps introduced by Ar^+ bombardment[191,194]. The imprint was also observed to increase with the milling depth[191], probably due to an increase in the defect density during the Ar^+ over milling. Compared to the wet-etched heterostructures, the different electrical behaviors observed in our ion-milled heterostructures are likely to be caused by such defects (*i.e.*, $V_{Ba}'' - V_O^{\bullet\bullet}$, V_{Ba}'', etc.)[64,108] introduced during Ar^+-ion milling. These defects (or defect dipoles) can influence the electrical properties in the ferroelectric capacitors, with studies suggesting they can cause horizontal imprints in the polarization-electric field hysteresis loops[64,196,197] as well as a reduction in the leakage current[63,142,148].

To further study the defects introduced into the heterostructures during processing, transport measurements were performed and leakage currents were measured under different voltages up to 3.5 V. A number of leakage mechanisms can occur in dielectric films and the most common ones include Ohmic conduction, space-charge-limited conduction, Schottky emission, and Poole-Frenkel emission[141]. The simplest mechanism is Ohmic conduction where the leakage current density, *J*, is directly proportional to the applied electric field, *E*,

$$J = \sigma E \qquad \text{Equation 5.2}$$

where σ is the electric conductivity. Another possible leakage mechanism in oxide films is space-charge-limited conduction, where the leakage current density is governed by the movement of bulk space charges within the dielectric films under the applied electric field as[141]

$$J = \frac{9\mu\varepsilon_0\varepsilon_r}{8d}E^2 \qquad \text{Equation 5.3}$$

where μ is the charge carrier mobility, ε_0 is the electrical permittivity of the vacuum, ε_r is the optical relative dielectric constant of the material and d is the film thickness.

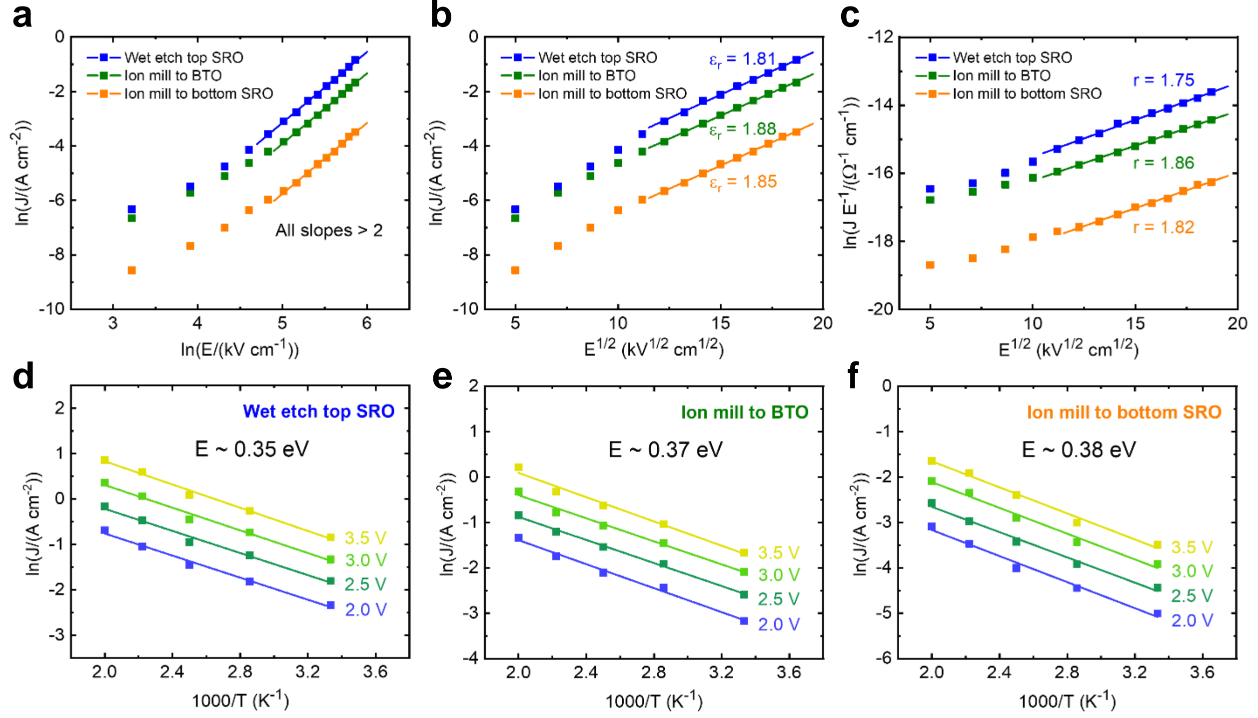


Figure 5.7 | Transport measurement and leakage mechanism study. Fitting of leakage current as a function of electric field using **a**, Ohmic and space-charge-limited conduction mechanisms, **b**, Schottky emission mechanism and **c**, Poole-Frenkel emission mechanism. Good fittings are obtained using Poole-Frenkel equation suggesting this is the governing leakage mechanism in the heterostructures. Leakage current density is measured as a function of temperature under various voltages from 2.0 V to 3.5 V to extract the intra-bandgap trap energies inside the heterostructures fabricated by **d**, wet etching top $SrRuO_3$, **e**, ion milling to $BaTiO_3$ and **f**, ion milling to bottom $SrRuO_3$.

In the above two cases, since J is a power function of E, $ln(J)$ should be a linear function of $ln(E)$, and for Ohmic conduction, the slope between $ln(J)$ and $ln(E)$ should be 1, while for space-charge-limited conduction, the slope between $ln(J)$ and $ln(E)$ should be 2. Therefore, $ln(J)$ is plotted as a function of $ln(E)$ (Fig. 5.7a), and fittings are done to extract the slopes from each curve. The fittings show all the slopes have values > 2 at large electric field, based on which we can rule out the Ohmic and space-charge-limited leakage mechanism.

The third leakage mechanism is the Schottky-emission mechanism, where the charge carriers are injected into the film by overcoming a Schottky barrier at the dielectric/electrode interfaces, and the leakage current density, J, is governed by[141]

$$J = AT^2 \exp\left(\frac{-q\phi_B + \sqrt{\frac{q^3 E}{4\pi\varepsilon_0\varepsilon_r}}}{k_B T}\right) \quad \text{Equation 5.4}$$

where A is the effective Richardson constant, T is the absolute temperature, q is charge of an electron, Φ_B is the Schottky barrier height at the interface, and k_B is the Boltzmann constant. From Eq. 5.4, it can be seen that $ln(J)$ should be a linear function of $E^{1/2}$ and the optical relative dielectric constant, ε_r, can be extracted. Linear functions are indeed obtained by plotting the data (Fig. 5.7b),

however, the extracted ε_r values from the slopes fall within the range between 1.81 and 1.88, which is much lower than the reported optical dielectric constant for $BaTiO_3$ (*i.e.*, ε_r = 5.9)[108,198]. Therefore, the Schottky emission mechanisms can also be ruled out.

The last commonly considered leakage mechanism for such oxide films is the Poole-Frenkel-emission mechanism, where there are defect states inside the bandgap of the material. These defect states can acts as trap centers for charge carriers in the dielectric films and the leakage is governed by a charge-trapping/detrapping mechanism[141] as governed by the equation,

$$J = q\mu N_c E \exp\left(\frac{-q\phi_T + \sqrt{\frac{q^3 E}{\pi\varepsilon_0\varepsilon_r}}}{rk_B T}\right) \qquad \text{Equation 5.5}$$

where N_c is the effective energy of states of the energy band, Φ_T is the trap energy of the intra-bandgap defect states, and r is a scaling factor (*i.e.*, $1 \leq r \leq 2$) to accommodate for the large concentration of donor and acceptor states. From Eq. 5.5, it can be seen that $ln(J/E)$ should be a linear function of $E^{1/2}$. The data is plotted (Fig. 5.7c) and scaling factors are extracted from the slopes (*i.e.*, the ε_r is set to be 5.9 in the fitting). The extracted r values for three heterostructures all fall within the range between 1 and 2. The good fittings suggest that Poole-Frenkel emission mechanism is (likely) the dominant mechanism for leakage in our $BaTiO_3$ films in all cases.

To extract the trap energy of the intra-bandgap defect states, temperature-dependent measurements were performed on all three heterostructures across the temperature range from 300-500 K, under various applied voltages from 2.0-3.5 V. $ln(J)$ is subsequently plotted as a function of $1000/T$ and the trap energy, Φ_T, is extracted from the slopes (Fig. 5.7d-f). The results show similar trap energies (*i.e.*, 0.35 eV, 0.37 eV, and 0.38 eV) for all three heterostructures, suggesting the same type of intra-bandgap defect state dominates the leakage current in all $BaTiO_3$ films. This is logical since the $BaTiO_3$ films are all identical and only have been processed into device structures differently. Since $BaTiO_3$ is commonly reported to be p-type[108,199] and holes are the majority charge carriers, the resulting trap state is therefore likely to be located at ~0.38 eV above the valence band and act as trap for holes inside the $BaTiO_3$. Previous studies have reported different types of defects that can exist in $BaTiO_3$ films, including $V_{Ba}'' - V_O^{\bullet\bullet}$, V_{Ba}', and V_{Ba}'' which are thought to be located at ~0.4 eV, ~0.6 eV, and ~1.2 eV above the valence-band edge, respectively[108,200,201], while others such as $V_O^{\bullet}$ and $V_O^{\bullet\bullet}$ are thought to be located ~0.1 eV and ~1.3 eV below the conduction-band edge, respectively[200,201], etc. Therefore, the ~0.38 eV trap state observed in this study is proposed to be of the type $V_{Ba}'' - V_O^{\bullet\bullet}$, which can likely give rise to an internal bias (*i.e.*, imprint) in the polarization-electric field hysteresis loops[64,108].

5.2.4 Deep-level transient spectroscopy

To further differentiate and understand how the processing impacts our films I have studied the defect concentrations inside the heterostructures and their relations to the observed electric properties (*i.e.*, imprint, leakage, etc.) using DLTS (a powerful technique used to detect a wide variety of electrically active defects, or charge carrier traps inside the bandgap of a material) which was measured with temperature ranging from 100-400 K (Fig. 5.8a-c).

For heterostructures that are fabricated by wet etching the top $SrRuO_3$, the trap state peaks are too small to be measured (*i.e.*, the signal cannot be distinguished from the background noise in the DLTS setup) under the conditions used. This is likely because of the fact that the heterostructures does not go through the Ar^+-ion bombardment during the milling process and thus the defects are just those "grown-in." In addition, the wet chemical etchant, $NaIO_4$, is high selectively and it does not attack and cause damage in the $BaTiO_3$ layer (a point which is supported by the DLTS). As a result, only a minimal level of defects exists in the $BaTiO_3$ film (*i.e.*, the as-grown defects which are relatively low in concentration). For the heterostructures that are ion milled to the $BaTiO_3$ layer (only through the top $SrRuO_3$), two weak trap-state peaks can be observed in the DLTS, suggesting a slight increase in the defect concentration in the $BaTiO_3$ films. For this heterostructure, because of the over-milling at the top $SrRuO_3$/$BaTiO_3$ interface to ensure the top $SrRuO_3$ layer is fully removed, some of the $BaTiO_3$ film is also bombarded by the Ar^+ ions, leading to a slight introduction of defects in the $BaTiO_3$ layer. For the heterostructures that are ion milled to the bottom $SrRuO_3$ (entirely through the $BaTiO_3$) two relatively strong trap-state peaks are observed

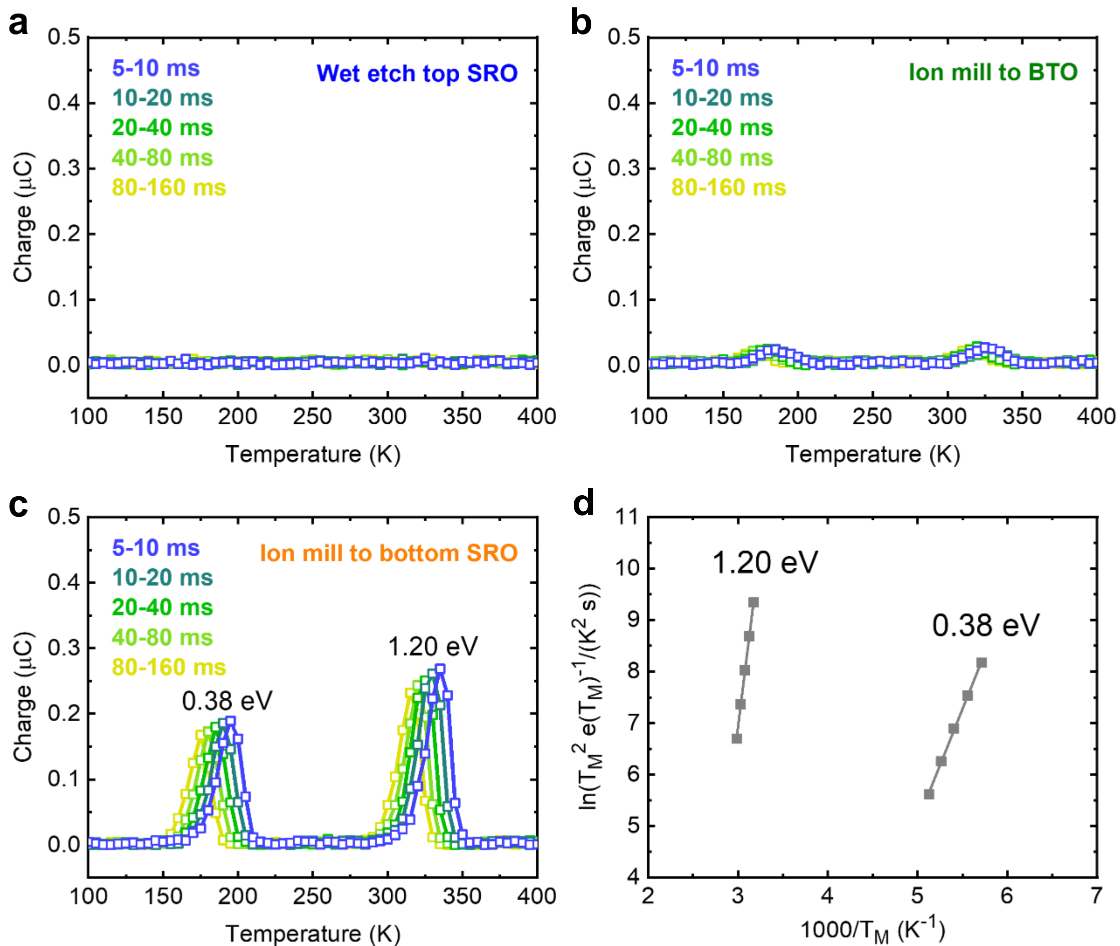


Figure 5.8 | Deep-level transient spectroscopy. Deep-level transient spectroscopy measured from 100 K to 400 K for heterostructures fabricated by **a**, wet etching top $SrRuO_3$, **b**, ion milling to $BaTiO_3$, and **c**, ion milling to bottom $SrRuO_3$. **d**, Fittings to extract the trap state energies inside the heterostructure fabricated by ion milling to bottom $SrRuO_3$.

in the DLTS, suggesting a relatively high concentration of defects in the $BaTiO_3$ layer, probably because of the milling in the $BaTiO_3$ film in order for the Ar^+ ion to reach the bottom $SrRuO_3$.

In the DLTS setup, first, a voltage pulse (3.5 V, 8 ms) is applied to the capacitor, setting it to an accumulated state where intra-bandgap traps are filled with charge carriers. Then, the pulse is removed and the traps start emitting charge carriers through thermal emission process. A time window is defined from t_1 to t_2 and the capacitance change between the time window, $C(t_1)$-$C(t_2)$, is monitored. At a certain temperature, T_M, $C(t_1)$-$C(t_2)$ will reach a maximum value for the given time window, corresponding to a maximum emission rate[108,143], $e(T_M)$, which is related to the characteristic thermal emission properties of the trap states[145],

$$e(T_M) = \frac{ln\left(\frac{t_2}{t_1}\right)}{t_2 - t_1} \quad \text{Equation 5.6}$$

$$e(T_M) = \sigma\gamma T_M^2 \exp\left(-\frac{E_d}{k_B T_M}\right) \quad \text{Equation 5.7}$$

where σ is trap capture cross section, γT^2, as a whole, represents the product of the density of states in the energy band and the thermal velocity of the charge carriers, E_d is the trap energy of the defects, and k_B is the Boltzmann constant.

To extract the trap energies, fittings on trap state peaks were performed. From Eq. 5.6 and Eq. 5.7, it can be seen $ln(T_M^2/e(T_M))$ should be a linear function of $1/T_M$ (or $1000/T_M$). The data is plotted and the trap energies are extracted from the slope (Fig. 5.8d). The two trap state peaks in the heterostructures that are ion milled to bottom electrode correspond to a trap energy of ~0.38 eV and ~1.20 eV, which confirms the results from the transport measurement and matches the trap energies of of $V_{Ba}'' - V_O^{\bullet\bullet}$ defect-dipole and V_{Ba}'' vacancy in previous studies[108,200,201]. For the heterostructures that are ion milled only to the $BaTiO_3$ layer, the trap state peaks, though hard to fit because of low defect concentrations, show up at roughly the same temperatures in the DLTS spectrum as those in the ion-mill-to-bottom-$SrRuO_3$ heterostructure, implying the same type of defects (*i.e.*, $V_{Ba}'' - V_O^{\bullet\bullet}$ and V_{Ba}'') inside the $BaTiO_3$ layer, but present in considerably lower concentrations.

In conclusion, as the milling depth increases, the defect concentration in the $BaTiO_3$ films increases. Previous studies have also suggested the increase of imprint in polarization-electric field hysteresis loops with increasing defect density[64,108,196,197], which matches the observation in our study (Fig. 5.4a), with the heterostructures that are ion milled to the bottom $SrRuO_3$ (through the entire $BaTiO_3$ layer) showing the largest imprint (~0.22 V) and the wet-etched heterostructures showing the smallest imprint (~0.01 V). This observation also offers a possible explanation for the decrease in the leakage current in the heterostructures which is related to the increasing defect concentration (Fig 5.4b). Previous studies have suggested that increasing the non-donor trap state density inside the dielectric film can lead to a reduction of the mean free path for the charge carrier[63,108,202], making it easier for them to be captured by the trap states, therefore reducing the leakage current, which also matches the observation in our study.

This leaves the problem, however, that ion milling does not seem to be a suitable method to be used in the production of devices based on these materials. This would be a huge limitation for their further consideration in this regard if it was true. As such, I explored different post-fabrication treatments that could effectively "fix" the imprint which could be applied to alleviate this concern. Here, I focused on the heterostructures that were ion milled to bottom $SrRuO_3$ (through the entire

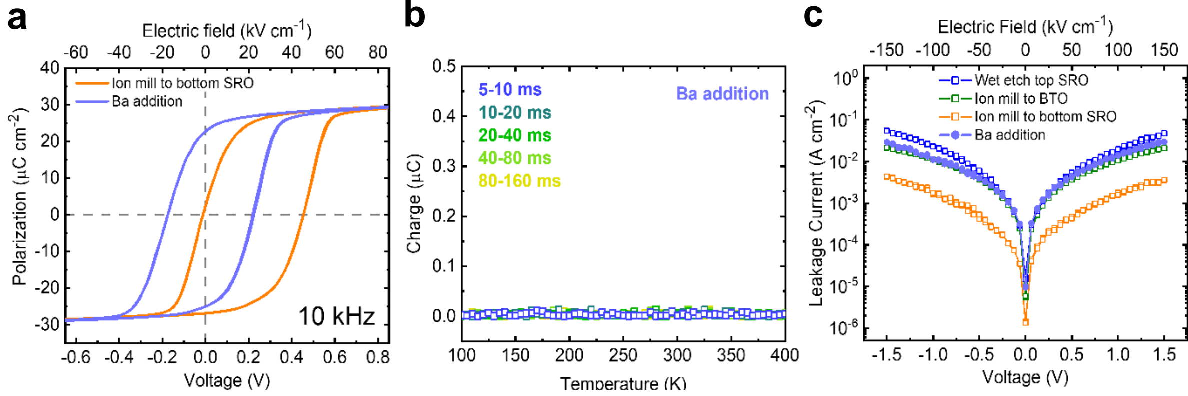


Figure 5.9 | Post-fabrication treatment. a, Evolution of polarization-voltage/electric field loop for the heterostructure fabricated by ion milling to bottom $SrRuO_3$, before and after Ba addition via CVD-style process in the furnace. **b**, Deep-level transient spectroscopy measured for the same heterostructure after Ba addition. **c**, Comparison of room temperature leakage current-voltage/electric field measurements for heterostructures with different fabrication and treatment processes.

$BaTiO_3$ layer). Annealing the heterostructures at 700°C at an oxygen partial pressure of 760 Torr for 60 mins showed no change in the polarization-electric field hysteresis loops, probably because of the strong coupling between V_{Ba}'' and $V_O^{\bullet\bullet}$ in the formation of energetically-favorable $V_{Ba}'' - V_O^{\bullet\bullet}$ defect-dipoles due to electrostatic and strain considerations[203-207], and the fact that barium-related defects could not be eliminated in an environment rich only in oxygen. With this knowledge and considering other studies which have shown the reintroduction of cations into ferroelectric materials via a chemical-vapor-deposition-like process can greatly reduce the defect density and ease the degradation of electrical properties in $BaTiO_3$ films[108] and has also been used to counter lead loss in $PbZr_{1-x}Ti_xO_3$ films grown with sol-gel methods[208,209], here, the heterostructure was placed in an Al_2O_3 ceramic boat at the end of the hot zone in a tube furnace while another Al_2O_3 ceramic boat with BaO powder was placed up-wind at the beginning of the hot zone. Oxygen was flowed through the furnace tube, first over the BaO powder and then over the heterostructure. The temperature of the furnace was set to ramp up at 25°C min^{-1} to 700°C, stay at 700°C for 60 min. and cool down to room temperature at 5°C min^{-1}. The heterostructure was then sonicated in 0.1 M HCl for 5 mins to remove any excess BaO on the surface. After the process, hysteresis loops were measured and the imprint was reduced significantly (from 22 kV cm^{-1} to ~2.5 kV cm^{-1}; Fig. 5.9a). Subsequent DLTS measurements also reveal the suppression/removal of the trap-state peaks (*i.e.*, $V_{Ba}'' - V_O^{\bullet\bullet}$ and V_{Ba}'') (Fig. 5.9b). And, finally, a corresponding increase in the leakage current was observed in the treated heterostructures (Fig. 5.9c), likely related to the decrease in the concentration of the defects that can act as trapping/de-trapping centers for charge carriers, leading to an increase in the charge carrier mean free path and an increase in the leakage current[63,108,202]. The post-fabrication treatment method shows the possibility of repairing the defects introduced by Ar^+ ion milling in ferroelectric capacitors.

5.3 Conclusion

Different processing methods for $SrRuO_3$/$BaTiO_3$/$SrRuO_3$ heterostructures have been investigated as an effort to explore the best way to fabricate idealized $BaTiO_3$ capacitor structure with idealized ferroelectric properties. *Ex situ* MgO hard mask methods have been found to contaminate the $BaTiO_3$ surface and introduce defects at the top $SrRuO_3$/$BaTiO_3$ interface, resulting in a large imprint in the hysteresis loops. *In situ* growth-and-wet-etch methods are highly selective and isotropic and can produce capacitor structure with the best ferroelectric properties with almost no imprint, but such methods alone are likely not suitable for fabricating more complexed device architectures. *In situ* growth-and-dry-ion-milling methods are directional and can be used to etch different types of metal oxide materials at similar speeds. However, due to the lack of precision in end-point determination, over milling is often required to fully remove the unwanted material. Moreover, because of the high kinetic energy of the incident Ar^+ ion beams, milling damage can occur in the ferroelectric capacitors, leading to hysteresis loops with degraded electrical behavior. An imprint as large as 22 kV cm^{-1} (which fully shifts the loops) is observed for the heterostructures that are ion milled to the bottom $SrRuO_3$ (through the entire $BaTiO_3$ layer). While the magnitude of this imprint may not seem significant at first glance, it can still cause significant impact in the ferroelectric capacitor performance, especially when the coercive field of the ferroelectric film is also small. Post-fabrication treatments are also performed. Annealing the heterostructure in barium-and-oxygen-rich environment via a CVD-style process can be useful in reducing the imprint of the polarization-electric field hysteresis loop, as well as reducing the density of the defects that are related to barium deficiency.

Chapter 6

Summary and Future Prospects

This chapter summarizes the findings presented in this dissertation, followed by some suggestions where further efforts can be made to improve the ferroelectric performance of $BaTiO_3$ films and to enable its applications in real-life devices.

6.1 Summary of work

Following the development of Moore's law in 1965 and the Dennard scaling law in 1974, it was set forth that the number of transistors per chip should double every 18-24 months (*i.e.*, the size of the transistor reduces 30% every year), while keeping the total power consumption per chip constant. This trend has, however, become more difficult to follow as the transistor dimensions approach the fundamental physical limits. The Boltzmann tyranny dictates a lower boundary of ~59 mV $decade^{-1}$ in gate voltage scaling while the increased leakage current (*e.g.*, short channel effect, gate leakage, tunneling current at the PN junctions, etc.) from the size scaling can cause extra power loss during transistor operation. Since around 2003, Dennard scaling has come to an end and keeping up with Moore's law has become extremely challenging. As a result, the concept of beyond CMOS-based switching systems is proposed and researchers have started to explore new materials, new computational state variables, and new switching mechanisms to enable such devices; thus trying to find pathway to continue Moore's law into the following decades. These new computational variables include spin, magnetization, polarization, strain, etc. and are hoped to provide a pathway to bypass Boltzmann tyranny for memory and logic (or logic-in-memory) applications, where low operation voltage (< 100 mV), low operation power (< 10 aJ/bit) and small switching time (< 0.1 ns) can be achieved.

Among all types of beyond CMOS switching systems, ferroelectric-based devices (*e.g.*, ferroelectric-RAMs, ferroelectric-FETs, ferroelectric tunneling junctions, negative-capacitance FETs, etc.) stand out because of their fast-switching speeds and low switching energies, making ferroelectric materials an interesting object to investigate. Once again, among all common ferroelectric materials, single crystal $BaTiO_3$ stands out because of its low switching field (~ 1 kV cm^{-1}), low switching power (~ 0.1 J cm^{-3}) and a relatively large remanent polarization (~25 μC cm^{-2}), making it a perfect candidate for next-generation ferroelectric applications. However, great challenges are met when downscaling materials such as $BaTiO_3$ into ultrathin films, resulting in significantly degraded ferroelectric properties such as large coercive fields/voltages or reduced remanent polarization, making it unsuitable for use in actual ferroelectric devices. Therefore, questions remain as how to synthesis idealized $BaTiO_3$ thin films and how to fabricate idealized capacitor structure.

In this dissertation, I present a systematic study on the $SrRuO_3/BaTiO_3/SrRuO_3$ capacitor heterostructures, from film synthesis at the beginning all the way to the device fabrications in the end. PLD was used for material synthesis, and structural characterizations were performed on the heterostructure revealing high crystallinity of the materials, as well as smooth and sharp interfaces between different layers. After fabrication, electrical measurements are performed on the capacitors, revealing superior ferroelectric performance, behind which the physical mechanisms are explored and discussed.

First, I investigate the growth parameter, especially the growth pressure, in the PLD process, and the effect it can bring to the $BaTiO_3$ layer in the heterostructures. The growth pressure is found to have significant impacts on the structural and ferroelectric properties of the heterostructures, as varying the growth pressure can change the kinetic energy of the ablated atoms that land on the substrate surface. As a result, the level of knock-on damage (or the defect concentration) inside the $BaTiO_3$ layer can be different, and the out-of-plane lattice expansion, the coercive field and the horizontal imprint in the hysteresis loop can also be impacted. By carefully adjusting the growth pressure, idealized epitaxial $BaTiO_3$ layers can be synthesized. At a dynamic oxygen growth

pressure of 60 mTorr, almost no out-of-plane expansion is observed, and the smallest coercive field/voltage can be achieved in the $BaTiO_3$ capacitors, which is comparable to its single-crystal counterpart. Thickness scaling was performed on the $BaTiO_3$ films to explore the lower limit of the coercive voltage. At $BaTiO_3$ thickness < 150 nm, depolarization fields start to impact the coercive-field scaling, leading to a constant coercive field (*i.e.*, E_C = constant, $V_C \propto$ thickness). The depolarization field results from the imperfect screening at the ferroelectric/electrode interface, where the $SrRuO_3$ electrode cannot provide enough free surface electrons to compensate for the bound charge from the ferroelectric polarization, leading to a decrease in the T_C transition temperature in $BaTiO_3$ films. From a practical perspective, for $BaTiO_3$ films with thicknesses ranging from 25-50 nm, the depolarization field has the beneficial effect of reducing the coercive field/voltage during the switching, with films show some of the best combinations of coercive voltages < 100 mV and remanent polarization > 10 $\mu C\ cm^{-2}$, which makes them idealized candidate for ferroelectric applications. As the $BaTiO_3$ gets thinner (*i.e.*, < 25 nm in thickness), however, the effect of the depolarization field is so large that the remanent polarization can be greatly suppressed (< 5 $\mu C\ cm^{-2}$), making them not suitable for real applications.

In addition, lateral scaling was performed on the $SrRuO_3/BaTiO_3/SrRuO_3$ capacitor structures to explore the fastest switching speed. With the capacitor areas becoming smaller, the switching time of $BaTiO_3$ capacitors becomes shorter. To achieve a switching time < 1 nanosecond in $BaTiO_3$ capacitor, a lateral size < 10 μm^2 (< 3.5 μm in diameter) is needed. In addition, compared to other common ferroelectric materials such as $BiFeO_3$ and $Bi_{0.85}La_{0.15}FeO_3$, the fast switching time measured in $BaTiO_3$ capacitors has revealed the great potential for it to be applied into real ferroelectric devices. Moreover, the integration of $BaTiO_3$ capacitors onto Si-based substrate is also shown, with a similarly small coercive field being observed, indicating the possibility of transferring the optimized growth conditions from the laboratory PLD chamber to the industry manufacturing equipment.

Last, but not least, different fabrication methods for $SrRuO_3/BaTiO_3/SrRuO_3$ heterostructures are also investigated, in an effort to find the best way to fabricate capacitors that are compatible with complex device architectures serving different purposes. *Ex situ* MgO hard mask process introduces surface defects and results in a horizontal imprint in the hysteresis loop. While the *in situ* growth-and-wet-etch process produces best hysteresis loops with almost no horizontal imprint, because of the high selectivity in the wet etching, it is often difficult to find the appropriate chemical etchant for certain ferroelectric materials, especially for perovskite materials such as $BaTiO_3$ and $PbZr_xTi_{1-x}O_3$ that are chemically stable. As a result, without proper chemical etching agents, it is barely possible to fabricate complex device structures. Moreover, the isotropic nature of the wet etching can often lead to shrinked feature sizes, as well as curved sidewalls. Another most common method used for capacitor fabrication is the *in situ* growth-and-dry-ion-milling process. While Ar^+ ion beam is directional and can be used to etch almost any type of materials, the long bombardment time of the $BaTiO_3$ heterostructures under the ion beam can introduce defects inside the $BaTiO_3$ layer, especially when over milling is required to fully remove the unwanted materials, leading to an imprint (~0.2 V) in the ferroelectric capacitors. An imprint of this magnitude may not cause significant impact on hysteresis loop symmetry (or the remanent polarization) in some other cases where the ferroelectric materials exhibit large loop width (> 3V). However, in our case, because of the small coercive field of the $BaTiO_3$ films (~0.2 V), this magnitude of imprint can completely shift the loop to the positive side, leading to a decrease in the remanent polarization in one direction. Following transport measurement was performed

confirming the existence of the same type of defect in all heterostructures with a trap energy of ~0.38 eV above valence band and is attributed to the $V_{Ba}'' - V_{O}^{\bullet\bullet}$ defect-dipole which can cause imprint in hysteresis loop. Deep level transient spectroscopy reveals the defect concentration increases with the milling depth. Post-fabrication treatments are also explored to reduce the defect amount. Annealing in 760 Torr O_2 pressure at 700 °C shows no improvement to the imprint of the PE loop, probably because Ba-related defects cannot be eliminated in an environment rich only in oxygen. Reintroduction of Ba element via a CVD-style process eliminates the Ba-related defects and greatly reduces the imprint of the loop, indicating the possibility to repair the damage introduced by Ar^+ ion milling in $BaTiO_3$ capacitors.

6.2 Suggestions for future prospects

6.2.1 Reducing coercive field via orientation control

Recently, reduction in coercive field has been reported in ferroelectric $PbZr_{0.2}Ti_{0.8}O_3$ thin films via orientation control[152]. When $PbZr_{0.2}Ti_{0.8}O_3$ films are deposited with a (001) out-of-plane orientation, it takes the form of tetragonal phase. However, if the $PbZr_{0.2}Ti_{0.8}O_3$ films are deposited with a (111) out-of-plane orientation, as the thickness gets smaller, the structure goes through a tetragonal-monoclinic-rhombohedral evolution at thickness < 165 nm. The structural transition, in turn, leads to lower c/a ratio and lower switching energy barrier in (111)-oriented $PbZr_{0.2}Ti_{0.8}O_3$ films than their (001)-oriented counterpart. Therefore, compared to (001)-oriented $PbZr_{0.2}Ti_{0.8}O_3$ films, the (111)-oriented $PbZr_{0.2}Ti_{0.8}O_3$ films show smaller coercive fields. Because of the structural resemblance between $BaTiO_3$ and $PbZr_{0.2}Ti_{0.8}O_3$, here I propose a hypothesis that the coercive field of the $BaTiO_3$ thin films can also be reduced via orientation control. This study can likely be focused on multiple $SrRuO_3/BaTiO_3/SrRuO_3$/substrate heterostructures synthesized using pulsed laser deposition with different $BaTiO_3$ orientations (001- and 111-oriented) and thicknesses (*e.g.*, 12.5-250 nm). Crystal structure of the heterostructures can be examined using X-ray diffraction and lattice parameters can be extracted to reveal the structural transition during thickness scaling. Ferroelectric properties (coercive field, remanent polarization) can also be characterized to further support the hypothesis.

6.2.2 Multistate switching behavior via orientation control

Besides the reduction in coercive field in (111)-oriented ferroelectric $PbZr_{0.2}Ti_{0.8}O_3$ films, another exotic switching behavior, the multistate switching, can also occur[123]. In (111)-oriented tetragonal $PbZr_{0.2}Ti_{0.8}O_3$ films, a stable intermediate polarization state can be obtained by applying a low or moderate bias. Two types of competing switching mechanisms in (111)-oriented $PbZr_{0.2}Ti_{0.8}O_3$ films are present and are associated with two different dominant energy types. When the applied bias is high, the electrostatic energy dominates and direct switching without intermediate state is favored because of the huge electrostatic energy gain during this process. However, if the applied bias is low, the elastic energy dominates, and a 50-percent-switched intermediate state is favored in the switching process because of the low elastic-energy barrier which is accompanied by a reconfiguration in domain structures. At a moderate applied bias, two mechanisms are activated simultaneously, enabling one to finely tune the intermediate polarization state into any arbitrary level. Since multistate switching behavior is of great importance to the realization of next-generation, high-density non-volatile memories, and the structural resemblance between $BaTiO_3$

and $PbZr_{0.2}Ti_{0.8}O_3$, here I propose a study on the switching behavior in (111)-oriented $BaTiO_3$ films. As has been proposed above in 6.2.1, (001) and (111)-oriented $SrRuO_3$/12.5-to-250-nm-$BaTiO_3$/$SrRuO_3$/substrate heterostructures can be synthesized and structural and ferroelectric properties can be characterized. For the purpose of multi-state switching studies, piezo-response force microscopy can be performed to examine the change in domain configurations during switching under different applied bias. PUND sequences with different pulse heights and pulse widths can likely be applied to obtain transient curves with intermediate polarization states to show the possibility of multi-state switching.

6.2.3 Reducing depolarization field in ultrathin $BaTiO_3$ films

Metal oxide electrodes, such as $SrRuO_3$, have been widely studied and used to sandwich ferroelectric films because of their high compatibility with perovskite ferroelectric lattices, as well as their capability to reduce imprint and fatigue behavior of the capacitor, and enhancing the performance of the ferroelectric devices[34]. However, the free electron concentrations inside these materials are not very high[95] (*i.e.*, ~1.2×10^{22} cm^{-3}) and are considered to be rather poor metals when compared to common metals such as platinum or gold[210] (with free electron densities 6 to 7 times larger than that in $SrRuO_3$). When using $SrRuO_3$ as an electrode for $BaTiO_3$ films, the incomplete screening at the ferroelectric/electrode interface can lead to a depolarization field that can significantly reduce the remanent polarization of the ferroelectric layer[137]. Therefore, efforts must be made to search for the better metal oxide electrodes among a range of materials, to minimize the effect brought by the depolarization field and to enable next-generation ferroelectric devices in ultrathin regime (*i.e.*, < 25 nm). For example, metal oxide electrodes with higher free electron concentrations, such vanadates, niobates, and molybdates (*e.g.*, studies have shown that the free electron densities can be as high as ~9.2×10^{22} cm^{-3} in $SrMoO_3$ films[211,212], which is ~8 times as large as that in $SrRuO_3$ electrodes) can be used as the top and bottom contacts for the ferroelectric films. In the metal electrodes, the relation between the characteristic Fermi-screening length, λ, and the free electron density, n_e, follows[163]

$$\lambda \propto \left(\frac{1}{n_e}\right)^{\frac{1}{6}} \qquad \text{Equation 6.1}$$

In the meantime, the magnitude of depolarization field, E_d, inside the $BaTiO_3$ films follows[155]

$$E_d \propto \frac{\lambda}{d} \qquad \text{Equation 6.2}$$

where d is the thickness of the film. From Eq. 6.1 and Eq. 6.2, we can hypothesize that, based on our estimation, if $SrMoO_3$ were used as top and bottom contact for $BaTiO_3$ films, it is possible to reduce the Fermi screening length by ~30%, which corresponds to a 30% decrease in the minimal $BaTiO_3$ thickness (*i.e.*, if 25 nm with $SrRuO_3$ electrodes, then ~18 nm with $SrMoO_3$ electrodes) before the depolarization field becomes large enough to suppress the remanent polarization. In addition, $SrMoO_3$ has a cubic lattice parameter of 3.975 Å[211], which matches closely with that of $BaTiO_3$ film and $GdScO_3$ (110) substrate, making it a potential candidate to replace $SrRuO_3$ electrodes. Therefore, it is interesting to study what actual benefits the $SrMoO_3$ electrodes would likely bring to the $BaTiO_3$ capacitor. The study can be focused on synthesizing multiple $SrMoO_3$/$BaTiO_3$/$SrMoO_3$/substrate heterostructures using pulsed laser deposition with $BaTiO_3$ thicknesses varying from 6-250 nm. Crystal structures and ferroelectric properties can be characterized to verify the hypothesis.

6.2.4 Increasing remanent polarization via interface engineering

Another potential way to increase the remanent polarization for ultrathin $BaTiO_3$ films < 25 nm is via interface engineering. Previous theoretical studies have shown the interfacial atomic structure and chemical bonding can have significantly impacts on the ferroelectric polarization[213,214]. The RuO_2-BaO termination sequence at the $SrRuO_3$/$BaTiO_3$ interfaces can have detrimental effect on the polarization stability. At the $SrRuO_3$/$BaTiO_3$ interfaces, the large Ba^{2+} in the $BaTiO_3$ unit cell can displace the Ru^{4+} in the adjacent $SrRuO_3$ unit cell[213], resulting in a pinned interface dipole in the opposite direction of the polarization, and thereby, an exacerbation in the depolarization effects. Following experimental studies suggests this detrimental effect can be alleviated by inserting an $SrTiO_3$ layer between the $SrRuO_3$/$BaTiO_3$ interfaces[213]. In this case, the pinned dipole at the interfaces can be eliminated because of the introduction of new interfacial termination sequence (*i.e.*, TiO_2-BaO, the same as the layer structure in normal $BaTiO_3$ crystals), and the depolarization effect can be reduced. The hysteresis loops show the remanent polarization increased by a factor of 3, which indicates that the interface engineering can be used to enhance remanent polarization in ultrathin ferroelectric capacitors. Therefore, it is interesting to study if the inserting $SrTiO_3$ layers could bring any benefits to our heterostructures. The study would likely focus on $BaTiO_3$ films with ultrathin thickness (*i.e.*, < 25 nm). $SrTiO_3$ layers with various thicknesses (*i.e.*, 2-10 unit cells) can be inserted between top or (and) bottom $SrRuO_3$/$BaTiO_3$ interfaces. Following ferroelectric characterization and piezo-response force microscopy measurement can be performed to examine the change in the remanent polarizations.

6.2.5 Lateral scaling in ultrasmall $BaTiO_3$ capacitors

Another future study I propose is to study the further downscaling in the lateral size of $BaTiO_3$ capacitors. Previous studies have reported the switching time of the ferroelectric capacitor decreases linearly with reducing capacitor areas[137,139,140]. However, it is also reported that as the capacitor diameters shrink to < 1 nm (*i.e.*, a few hundreds of nanometers), the decreasing rate of the switching time as a function of capacitor area becomes slower (*i.e.*, the decreasing trend starts to asymptote)[139,140]. The most likely reason is that the rising time of the pulse stimulus in the external circuit or (and) the RC charging time of the capacitor cannot keep up with the intrinsic switching time of the ferroelectric material and has therefore become the extrinsic limiting factor for measured switching times. As the capacitor size continues to decrease into ultrasmall regime (*i.e.*, diameter of a few tens of nanometers) the switching time could also be limited by the intrinsic switching process of the ferroelectric material itself (*i.e.*, the time needed for nucleation and domain growth)[96,139]. In the meantime, some other studies suggest that, in this ultrasmall regime, the nucleation and domain growth mode may no longer be the dominant switching mechanism in the ferroelectric layers[139,215], and new models are needed to describe the switching phenomenon in the ultrasmall regime. Therefore, it is interesting to study the switching behavior when further downscaling our $BaTiO_3$ capacitors laterally, as well as to explore the switching speed limit in ultrasmall $BaTiO_3$ capacitors. The study can likely be focused on $BaTiO_3$ capacitors with varies thicknesses (*i.e.*, 12.5-100 nm) and different sizes (*i.e.*, 50-1000 nm). Ferroelectric measurements and ultrafast switching kinetic measurements can be performed to further explore the switching characteristics in $BaTiO_3$ capacitors of each size.

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