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Miniaturizing DC-DC Converters for Mobile Applications via Hybrid and Inductor-First Topologies

A dissertation submitted in partial satisfaction of the requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

Abdullah Amgad Abdulaziz Abdulslam

Committee in charge:

Professor Patrick P. Mercier, Chair
Professor Gert Cauwenberghs
Professor Tzu-Chien Hsueh
Professor Gabriel Rebeiz
Professor Tajana Rosing

2021

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The dissertation of Abdullah Amgad Abdulaziz Abdulslam is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California San Diego

2021

DEDICATION

To my Mother: Sahar Mahmoud

To my Father: Amgad Abdulaziz

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Looking back at the past four years, I am very grateful and thankful for all the people who made this thesis possible and I hope I do not miss anyone.

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Abdullah Amgad Abdulaziz Abdulslam
Jan 14th, 2021

The material in this dissertation is mostly based on the following published papers. Chapter 2 is based on and mostly a reprint of the following publications:

- A. Abdulslam and P. P. Mercier, "A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter Achieving 0.7 W/mm^2 Power Density and 94% Peak Efficiency," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2019, pp. 148-150.

- A. Abdulslam and P. P. Mercier, "A Passive-Stacked Third-Order Buck Converter With Inherent Input Filtering Achieving 0.7-W/mm^2 Power Density and 94% Peak Efficiency," *IEEE Solid-State Circuits Letters*, vol. 2, no. 11, pp. 240-243, Nov. 2019.

Chapter 3 is based on and mostly a reprint of the following publications:

- A. Abdulslam and P. P. Mercier, "A 98.2%-Efficiency Reciprocal Direct Charge Recycling Inductor-First DC-DC Converter," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2021.

Chapter 4 is based on and mostly a reprint of the following publications:

- A. Abdulslam, B. H. Lam and P. P. Mercier, "A Battery-Connected Symmetric Modified Multilevel Ladder Converter Achieving 0.45 W/mm^2 Power Density and 90% Peak Efficiency," *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, 2019, pp. 1-4.

- A. Abdulslam and P. P. Mercier, "A Symmetric Modified Multilevel Ladder PMIC for Battery-Connected Applications," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 767-780, March 2020.

Chapter 5 is based on and mostly a reprint of the following publications:

- A. Abdulslam and P. P. Mercier, "A Battery-Connected Inductor-First Flying Capacitor Multilevel Converter Achieving 0.77 W/mm^2 and 97.1% Peak Efficiency," *IEEE Custom Integrated Circuits Conference (CICC)*, 2021, pp. 1-4.

The dissertation author is the primary investigator and author of the work in these papers, and coauthors (Prof. Patrick P. Mercier, and Bao Huu Lam) have approved the use of the material for this dissertation.

VITA

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PUBLICATIONS

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ABSTRACT OF THE DISSERTATION

Miniaturizing DC-DC Converters for Mobile Applications via Hybrid and Inductor-First Topologies

by

Abdullah Amgad Abdulaziz Abdulslam

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California San Diego, 2021

Professor Patrick P. Mercier, Chair

As the size of the electronics in mobile and IoT devices scales down while performance demands scale up, power management integrated circuits (PMICs) face increasing pressure to provide highly efficient conversion in increasingly small areas. Most modern mobile devices are powered from Li-ion batteries that operate between $\sim 3-5$ V. However, the system-on-chips (SoCs) that are powered in such systems are typically operating at $\lessapprox 1.2$ V, requiring DC-DC converters that can provide high continuous conversion ratios up to $15\times$. Ideally, this DC-DC converter should both be efficient in order to maximize battery lifetime, and also small in order to minimize device volume. Unfortunately, for a given topology and packaging technology, there is typically a direct trade-off between efficiency and power density making the achievement of an acceptable trade-off point for a DC-DC converter more challenging.

This thesis introduces new topologies and techniques that help ease this trade-off between efficiency and power density while providing additional benefits like enhanced

light load efficiency and reduced input noise and EMI. The first part of the thesis introduces a passive-stacked 3rd order buck (PS3B) converter that offers loss-, structure-, and noise-related benefits as compared to a conventional buck converter. Specifically, all the passives including two inductors are stacked in a packaging-friendly manner at the converter input, allowing for the inductors to process lower current than a conventional buck converter while inherently filtering input current noise. In the second part, a charge recycling technique is applied to the PS3B converter which enables direct reciprocal recycling of gate charge from one power MOSFET to the other, all without affecting converter operation or control. To directly power an SoC from a Li-ion battery while using low-voltage transistors, the third part introduces a symmetric modified multilevel ladder converter that, as compared to conventional flying-capacitor multilevel converters, features reduced conduction losses, naturally balanced flying capacitors, and internal generation of all the supplies required for drivers and level shifters. To combine the benefits of the PS3B converter (inductors processing continuous current on the low-current side of the converter) with the benefits of multilevel converters (Li-ion battery compatibility with low-voltage transistors, and reduced inductor size), an inductor-first flying-capacitor multi-level (FCML) converter is introduced. Prototypes of the presented topologies and techniques achieve state-of-the-art numbers in terms of efficiency, power density, light load efficiency and noise performance.

Chapter 1

Introduction

1.1 Power Management for Mobile Devices

Power management integrated circuits are used in many applications that varies widely starting from industrial and automotive to mobile and consumer electronics. The power management circuits are essential parts in these systems that are used to convert and regulate the output voltage to the value needed to power the target system. As shown in Fig. 1.1, power managements circuits have a huge market of $19.1 billion which is expected to continue to grow in the coming years. Among the different applications shown in Fig. 1.1, power management circuits for consumer and mobile applications have the largest market share due to the wide use of these applications.

DC-DC converters are the main power management circuit used in mobile devices and play an important role in determining the device characteristics in terms of cost, form-factor, and battery life. Mobile devices are usually powered by Li-ion batteries which provide a voltage in the range of 2.8 to 4.2 V depending on the charge level of the battery. On the other hand, the system-on-chips (SoCs) employed in these mobile devices typically run at a voltage lower than the battery voltage which can be around 1.8 V to 0.8 V or even lower down to 0.3 V for some memory blocks and low-power circuits. Due to this voltage discrepancy, DC-DC converters are needed to convert down the battery voltage to a voltage appropriate to power the SoCs employed in these devices. Modern SoCs have a complex design where a single SoC can have separate blocks each performing a different function. Due to this complexity, SoCs typically require many supply rails, each with a different current rating and, possibly, an inde-

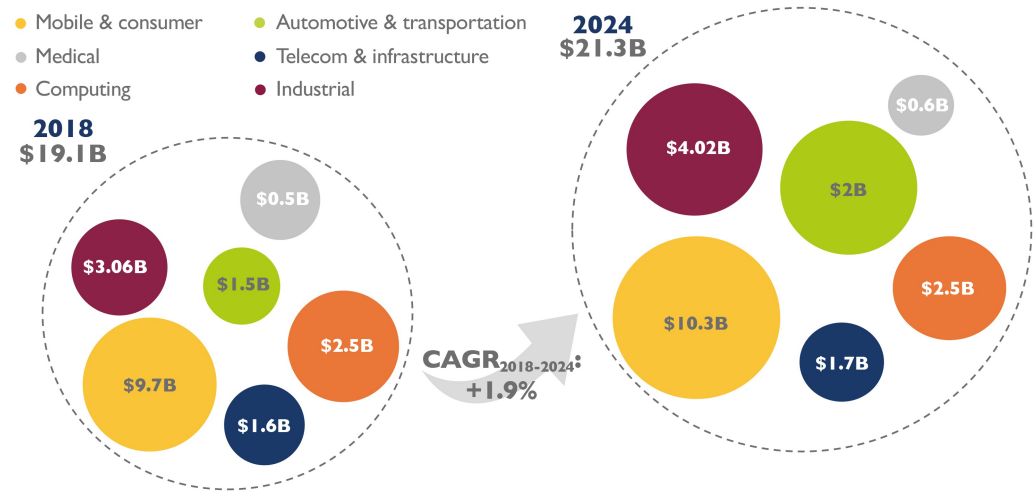


Figure 1.1: Power management market evolution split by application.

pendent control, as illustrated in Fig. 1.2. In most cases, a dedicated DC-DC converter (linear or switched-mode) is assigned to each of these voltage rails. Linear regulators can consume less space, but they are lossy and can generate excessive heat specially when used for blocks with large current requirements like the core digital block. On the other hand, switch-mode converters can be more efficient, but each converter comes its associated passives that consume a large space on the board. While other components in the system continues to scale down, the DC-DC converters do not exactly follow this trend due to the passives used in them.

1.2 Recent Challenges for DC-DC Converters

The recent trends in mobile devices introduce increasing challenges and requirements on DC-DC converters. First, DC-DC converters need to be small in size to help building small-factor mobile devices. Second, DC-DC converters need to have a light weight by using a fewer number of passives specially the bulky inductors. Third, DC-DC converters are usually desired to have high efficiency preferably across the full desired operation range of the converter to increase the battery life of the mobile devices.

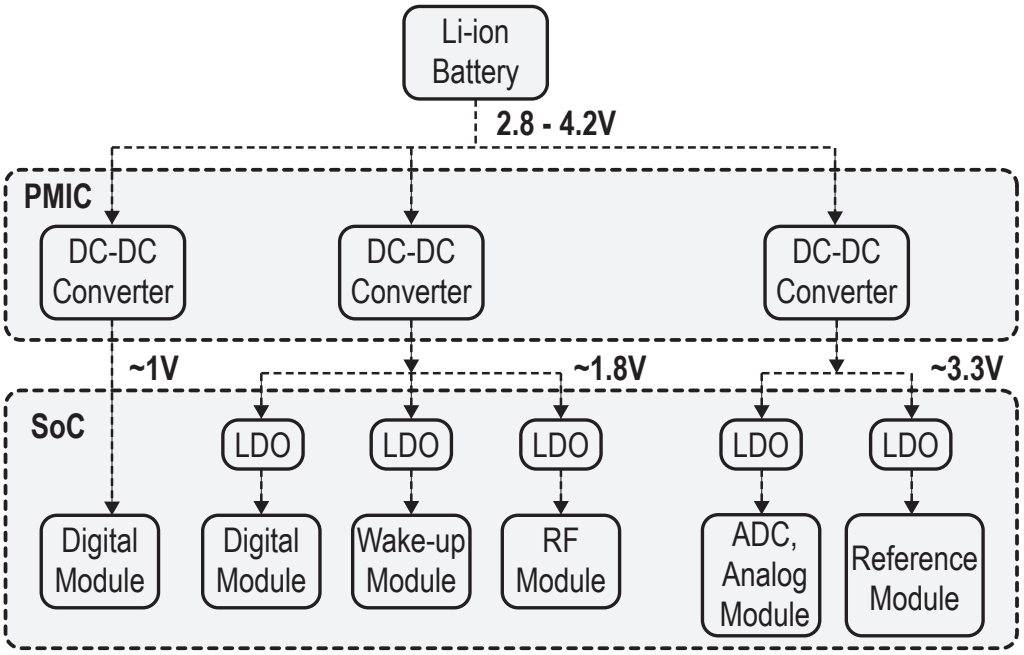


Figure 1.2: An example of the power management structure for an SoC.

Ideally, a flat high efficiency curve over the load current is desired. However, due to trade-offs in the converter design, the efficiency curve will have peaks and valleys with respect to the input voltage, the output voltage, and the load current. In addition, DC-DC converters need to have a fast response to changes in the load current in order to reduce decoupling capacitor requirement and ensure reliable SoC operation. Moreover, in some applications, the DC-DC converter is required to have low noise and EMI so that it does not interfere with other noise-sensitive circuits in the same system or in the surrounding environment. All of these requirements introduce vast challenges on the design of DC-DC converters where some of these requirements tend to trade-off with each other.

The coming subsections highlight some of these challenges that are considered the most important for DC-DC converters used in mobile devices, and provide some hint of the developments in this work to address these challenges.

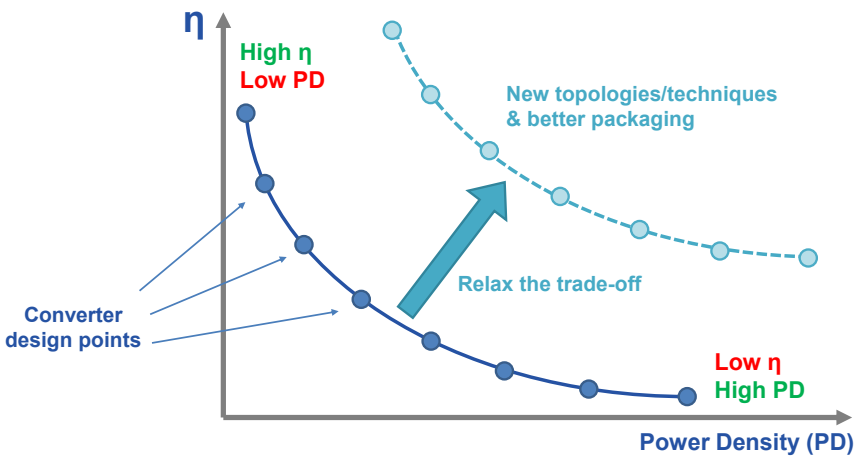


Figure 1.3: Trade-off between efficiency and power density in a DC-DC converter illustrated by some example design points.

1.2.1 Trade-off between Efficiency and Power Density

Longer battery life and smaller form factor are key requirements in mobile devices. These requirements are directly related to the DC-DC converters used in these mobile devices. To satisfy these requirements, DC-DC converters need to have high efficiency to maximize the device battery life and also have high power density for a small form-factor device. Unfortunately, there is always a trade-off between efficiency and power density when designing DC-DC converters as illustrated in Fig. 1.3. If the converter is designed to have high power density mainly by using smaller passives that occupy less area, it will suffer from lowered efficiency reducing its battery life. Since in most mobile applications maintaining a longer battery life is often more prioritized, DC-DC converters are usually designed to have high efficiency even at the cost of low power density. The power density of a DC-DC converter can be calculated by dividing the converter output power by the converter total footprint (*i.e.,* W/mm^2) or by dividing the output power by the converter bounding box (*i.e.,* W/mm^3). The power management integrated circuit (PMIC), that integrates the converter power stage along with the control circuitry, can itself achieve high power density. However, when including all the converter discrete passive components in the power density calculation, the total power

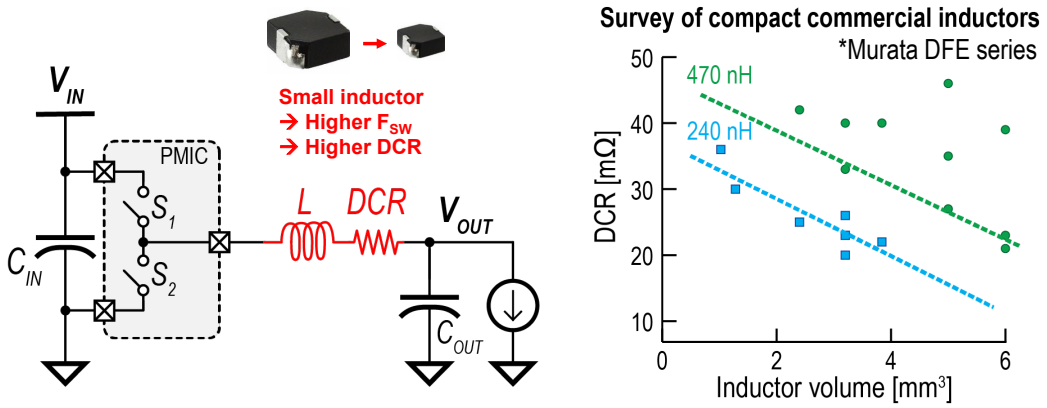


Figure 1.4: Challenges for miniaturizing a conventional buck converter where small-size inductors have a higher DC resistance (DCR).

density of the converter becomes much lower.

This trade-off between efficiency and power density is well-illustrated in a conventional buck converter where to minimize the converter losses, usually bulky inductors are employed. To increase the buck converter power density, a smaller less-bulky inductor is needed which can be achieved either by directly reducing the inductor physical dimensions while keeping its inductance value the same, or by reducing the needed inductance value itself to enable physically smaller inductors. Employing an inductor that has smaller physical dimensions while keeping its inductance value unchanged would directly result in a higher inductor DC resistance (DCR) as illustrated in Fig. 1.4. This higher DCR would hinder the converter efficiency specially because of the high DC current flowing through the inductor in a conventional buck converter. To overcome this challenge, an inductor-first buck topology is introduced in chapters 2, 3 and 5, which allows for employing smaller inductors of higher DCR by having the inductors process lower DC current as compared to a conventional buck converter.

On the other hand, reducing the inductance value, to enable physically smaller inductors, requires the converter to switch at higher switching frequencies to reduce the current ripple in the inductor. Higher switching frequencies usually result in higher switching losses hindering the converter efficiency. Chapter 3 of this thesis addresses this challenge through a charge-recycling technique that can reduce the gate charge

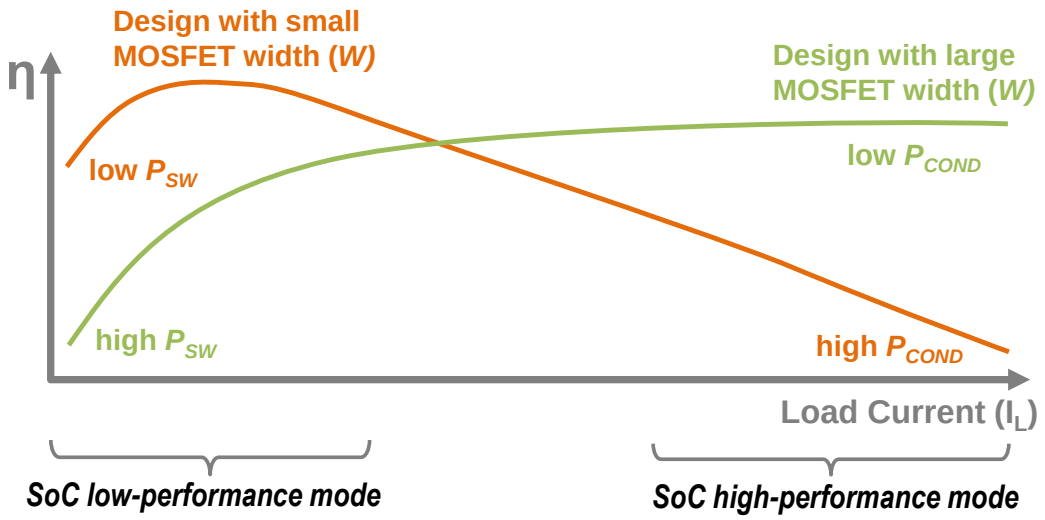


Figure 1.5: The design choice of the MOSFET width (W) affects the converter efficiency profile across the load current (I_L).

switching losses by up to 80% by reciprocally recycling the charges between the power transistors.

1.2.2 Maximizing Efficiency Across a Wide Operating Range

DC-DC converters are usually expected to operate across a wide range of input voltages to cover the Li-ion battery voltage range, across a wide range of output voltages to support dynamic voltage and frequency scaling (DVFS) for the SoC, and across a wide range of load currents to cover the different operating modes of an SoC. In fact, the power demand of an SoC varies dramatically depending on whether the SoC is operating in a low-performance mode or in a high-performance mode. These different operating modes require efficiency to be maximized over a wide range of load currents to maximize the device battery life regardless of the SoC operating mode. Achieving this high efficiency across a wide load range is challenging since DC-DC converters are fundamentally limited by a trade-off between switching losses and conduction losses.

This trade-off is dependent on the sizing of the power MOSFETs as shown in

Fig. 1.5. Each power MOSFET has its intrinsic parasitic on-resistance that is inversely proportional to the MOSFET width (W) and results in conduction losses. The power MOSFET also has switching losses related to the charging or discharging of its gate capacitance and these losses are proportional to the MOSFET width (W). These relations of the losses with W results in a trade-off between conduction losses and switching loss when making a design choice of W. If MOSFETs of relatively large W are selected, the converter will have high efficiency at the high current range due to the low on-resistance of the power MOSFETs. However, this efficiency quickly degrades when moving to the low current range due to the increased switching losses. On the other hand, if power MOSFETs of relatively small W are selected, the efficiency at the low current range is maximized due to the low switching losses but the efficiency degrades quickly when moving to the high current range due to the high on-resistance of the power MOSFETs. To maximize the converter efficiency across a wide load range, techniques to reduce these traditional losses of the power MOSFETs are needed.

Chapter 3 addresses this challenge by introducing a gate charge recycling technique, applied to the inductor-first buck converter of chapter 2. Theoretically, the introduced recycling technique can allow for zero gate switching losses for the power MOSFETs. In a practical implementation, up to 80% of the gate charges can still be recycled. This major saving in the switching losses of the power MOSFETs allows for maximizing the efficiency across a wide range of load currents.

1.2.3 Powering an SoC Directly from a Li-ion Battery

Li-ion batteries are the most common power source for several mobile devices due to their higher energy density, lighter weight, and lower self-discharge rate. They typically provide a voltage in the range of 4.2 V when fully charged which goes down to 2.8 V when almost depleted. However, most of the SoCs used in mobile applications typically require a voltage in the range of 1.2 V or even lower down to 0.3 V for some memory circuits. This voltage discrepancy requires DC-DC converters that can provide

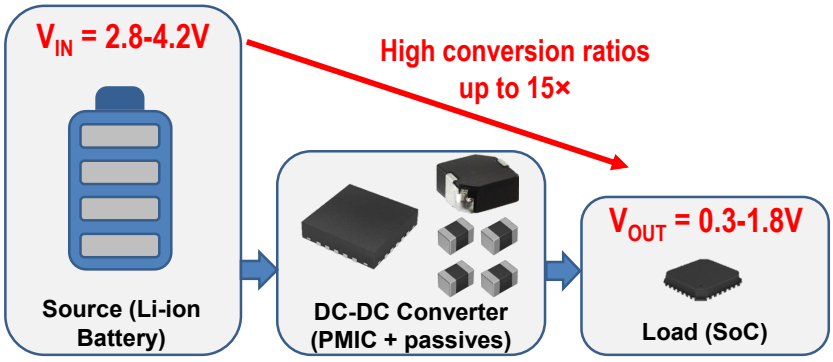


Figure 1.6: Powering an SoC directly from a Li-ion battery requires high conversion ratios of up to 15× along with high blocking voltages for the power transistors of the PMIC.

high conversion ratios of up to 15× as shown in Fig. 1.6. The relatively high voltages provided by Li-ion batteries require transistors of high-voltage rating, typically not available in modern CMOS technologies, to be used in the power stage of these DC-DC converters. Chapters 4 and 5 address these challenges by presenting multilevel hybrid converters that can directly convert a Li-ion battery voltage down to SoC voltages as low as 0.3 V, all while employing low-voltage MOSFETs of modern CMOS technologies.

1.2.4 Self-generated Noise and EMI

DC-DC converters are by nature noisy circuits due to their switching behavior. They generate interference that adversely affect other noise-sensitive circuits used inside the device. This interference issue becomes more challenging as the dimensions of the device are reduced putting the noisy DC-DC converters in a close proximity to other noise-sensitive circuits like analog and wireless communication circuits typically needed in internet of things (IoT) and mobile devices. In addition, a conventional buck converter has by nature a pulsated input current that can introduce noise for other circuits powered by the same input source. Large input decoupling capacitors or more complex filtering circuits might be required to suppress this noise. The inductor-first topology, introduced in chapter 2 and used in chapters 3 and 5, addresses these challenges where the noise at the converter input is substantially reduced by having a continuous input

current instead of the pulsated input current of a conventional buck converter. In addition, in the inductor-first topology, all the converter passives are stacked at the input allowing for a minimum board routing area for the converter switching nodes resulting in a reduced EMI from the converter.

1.3 Hybrid DC-DC Converters

The two conventional ways to build a DC-DC converter are either by using a switched-inductor approach or a switched-capacitor approach. A switched-inductor converter or a conventional buck converter can generally achieve a high efficiency but this high efficiency usually involves the use of a bulky inductor that greatly hinder the converter power density. Using smaller inductors to improve the power density quickly degrades the converter efficiency. On the other hand, in a switched-capacitor converter [2–4], since only capacitors are used in the power conversion process, these converters can usually achieve very high power densities as capacitors have an energy density that is up to 100$\times$ higher than inductors. However, switched-capacitor converters suffer from fundamental charge sharing losses between the capacitors which greatly hinder their efficiency specially when the output voltage deviates from the nominal conversion ratios provided by the employed switched capacitor (SC) topology [5].

One way to break these trade-offs in conventional DC-DC converters is by developing new hybrid DC-DC topologies where both capacitors and inductors are involved in the power conversion process. Hybrid DC-DC converters [6–29] are nowadays a growing research area and are considered a potential to overcome the limitations associated with conventional switched-capacitor or switched-inductor DC-DC converters. Usually, hybrid DC-DC converters are built by using a SC network followed by an inductor placed at the output along with a decoupling capacitor to form an output LC filter [8–24]. Although a group of extra flying capacitors are added to the hybrid converter to build the SC network, this SC network can be used to reduce the size requirement of the inductor resulting in a net saving in the total volume of the needed passives, and

hence increasing the power density of the converter [25].

Generally, there are two approaches to build or operate a hybrid DC-DC converter which can be through a resonant approach [8–13] or a multilevel approach [14–24]. If the switched capacitor network is configured to provide a single conversion ratio, the resulting converter is a resonant hybrid DC-DC converter where a form of a sinusoidal voltage waveform is generated at the inductor input. The resonant hybrid DC-DC converters can eliminate or reduce the charge sharing losses existent in a conventional switched-capacitor converter. However, resonant hybrid converters still have limited regulation capabilities in terms of the output voltage. To enable better output regulation that is purely PWM-based, the switched capacitor network can be configured to provide two (or more) conversion ratios or voltage levels to generate a switching voltage waveform at the inductor input. The reduced voltage swing of this switching voltage waveform results in reduced inductor ripple/size/loss as compared to a conventional buck converter. There are multiple conventional SC topologies (e.g. FCML, ladder, series-parallel, and Dickson) that can be used to build a multilevel hybrid converter. However, each of these SC topologies has some limitations or challenges (e.g. ensuring the flying capacitor stability) that hinder their use in practical applications. In chapter 4, a symmetric modified multilevel ladder (SMML) topology is introduced that offers several benefits as compared to other conventional SC topologies when used to build a multilevel converter. Appendix A provides a general analytical model to compare between the performance of the different SC topologies that can be used to build a multilevel converter, including the SMML topology introduced in chapter 4.

A recent direction in hybrid DC-DC converter involves the use of multiple switching inductors along with a single or multiple switching flying capacitors. Inductors are usually considered bulkier than capacitors and employing multiple of them in a single topology can hinder the power density of the converter. However, through the help of the flying capacitors and by changing the position of these inductors inside the topology, the DC current and the ripple requirement in each of these inductors can be substantially reduced resulting in an overall total reduction in the converter volume as compared to

using a single bulky inductor. This trend of using multiple inductors in hybrid DC-DC converters has been recently adopted by academia and industry [26–29]. In this work, chapters 2 and 3 introduce an inductor-first topology in which two inductors are placed at the converter input allowing them to process lower DC current. In addition, through applying a multilevel approach to this inductor-first topology, the inductors can also process lower current ripple allowing for an even more reduction in the inductor loss/size. This approach is illustrated in chapter 5 where an inductor-first multilevel converter is introduced.

1.4 Thesis Organization and Contribution

To address all of the aforementioned challenges in DC-DC converters, this thesis introduces new DC-DC topologies and techniques that can, considerably, ease the trade-off between efficiency and power density and achieve some state-of-the-art numbers in terms of power density and efficiency, all while covering the wide range of conversion ratios and load currents needed in mobile applications. This thesis is organized as follows:

- Chapter 2 introduces an inductor-first 3rd-order buck converter that has loss-related, noise-related and structure-related benefits as compared to a conventional buck converter. Specifically, all the passives including two inductors are stacked in a packaging-friendly manner at the converter input, allowing for the inductors to process lower current than a conventional buck converter while inherently filtering input current noise. A prototype shows that the converter achieves a peak efficiency of 94% and a peak power density of 0.7 W/mm^2.

- Chapter 3 builds upon the topology presented in chapter 2 and introduces a charge-recycling inductor-first 3rd-order buck converter that enables a direct reciprocal recycling of the gate charge from one power MOSFET to the other by the addition of only a single inductor and two switches, all without affecting

converter operation or control and while ensuring non-overlap conditions. The implemented converter achieves a peak efficiency of 98.2%, a peak power density of 0.72 W/mm^2, and efficiency of 88.4% down to 1% of the maximum load current.

- Chapter 4 describes a symmetric modified multilevel ladder (SMML) converter that is capable of directly converting down from Li-ion battery voltage ranges to SoC-compatible voltage ranges while using low-voltage power MOSFETs in the power stage. As compared to conventional flying-capacitor multilevel (FCML) converters, the SMML converter features reduced conduction losses, naturally balanced flying capacitors, and internal generation of all the supplies required for drivers and level shifters. A prototype shows that the converter achieves a peak efficiency of 90% and a peak power density of 0.52 W/mm^2, while providing up to 16.7x conversion ratios at still acceptable efficiencies.

- Chapter 5 presents the design of an inductor-first flying-capacitor multi-level (FCML) converter that combines the benefits of the inductor-first topology introduced in chapter 1 (inductors processing continuous current on the low-current side of the converter) with an FCML topology (Li-ion battery compatibility with low-voltage transistors, and reduced inductor size). The design operates across the entire Li-ion battery range, and achieves a power density of 0.77 W/mm^2, and a peak efficiency of 97.1%.

- Appendix A introduces a general model to analyze the losses in multilevel converters. Different SC topologies can be used to build a multilevel converter where a straightforward comparison between the performance of these topologies is challenging due to the relatively high number of components (switches and capacitors) used in these topologies. The model developed in this appendix introduces a consistent and a systematic approach to analyze the losses in any given SC multilevel topology. Additionally, the same model provides a design

optimization method to minimize the losses in a given topology. By using the general model, a comparison between different optimized SC topologies when used to build a multilevel converter is performed. The results show the SMML topology, introduced in chapter 4, achieves a competitive or a better performance as compared to the other conventional SC topologies.

A summary of the introduced topologies and techniques in this thesis is shown in Fig. 1.7 which also illustrates the relations and the links between the introduced topologies and techniques considering the basic conventional buck converter as the starting point. The main topology introduced in this thesis is the inductor-first buck converter presented in chapter 2 which has several benefits as compared to a conventional buck converter. This new inductor-first buck converter motivates chapter 3 which exploits the new structure of the inductor-first topology to apply a gate charge recycling technique in an efficient way, not otherwise possible with a conventional buck converter.

Mobile applications usually utilize a Li-ion battery as their power source and when employing a basic buck converter with low-voltage transistors (*i.e.,* $<$2 V), stacking of the transistors would be required. The conventional FCML topology exploits these stacked transistors to reduce the voltage swing on the inductor offering lower inductor size/ripple/loss. However, the FCML topology still suffers from some implementation limitations that hinders its adaptation in real applications. Chapter 4 introduces an SMML converter that overcomes some of these limitations in FCML converters, enabling a more practical implementation in real applications. To better adapt the inductor-first converter, presented in chapters 2 and 3, for Li-ion battery applications, an inductor-first FCML converter is introduced in chapter 5. The inductor-first FCML converter combines the benefits of the inductor-first topology (presented in chapter 2 and chapter 3) with the benefits of a multilevel topology (like the topology presented in chapter 4) to ultimately enable lower inductor loss/size while using low-voltage MOSFETs, and having a continuous input current for reduced noise and EMI.

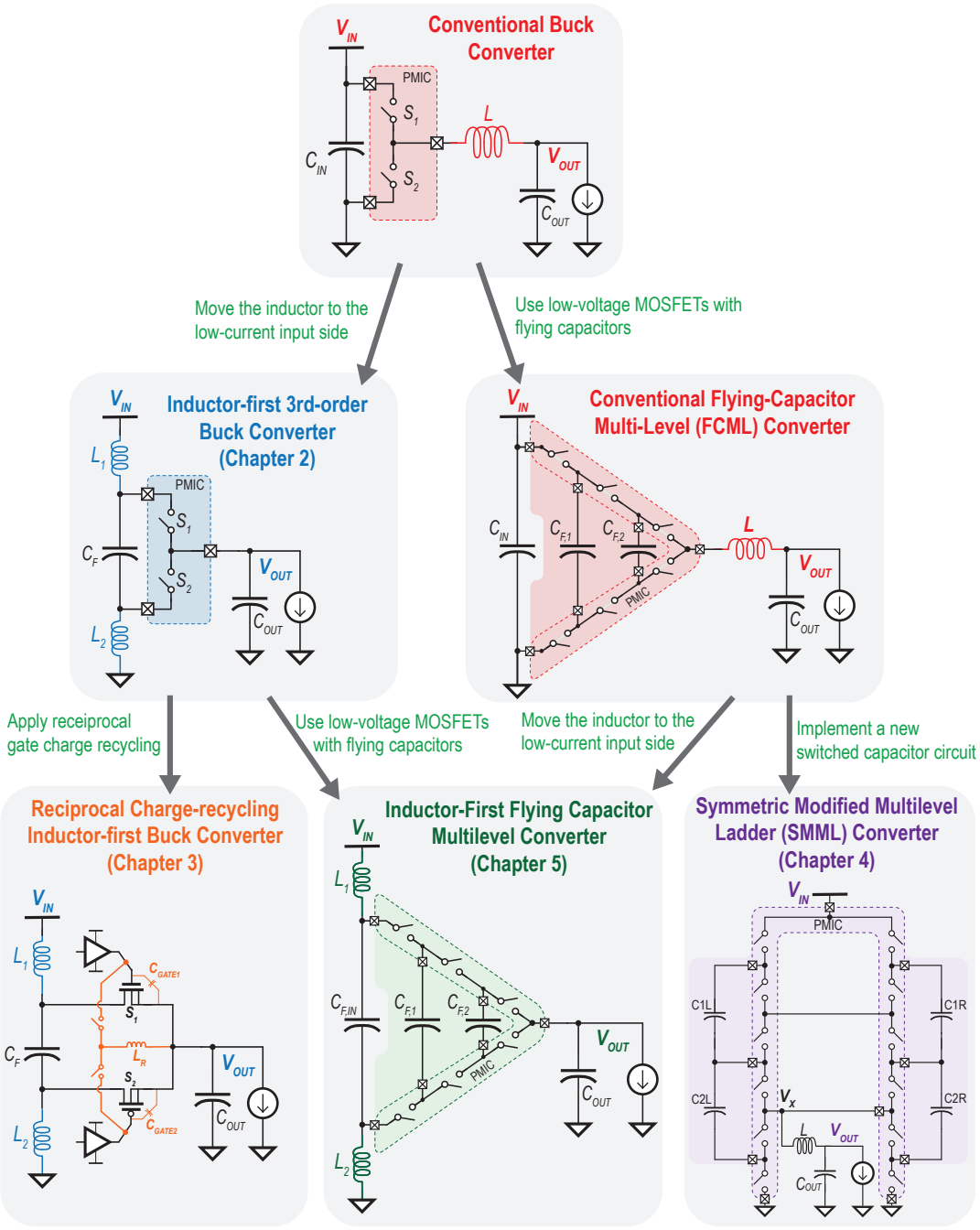


Figure 1.7: Summary of thesis contribution illustrating the relation between the introduced topologies and techniques.

Chapter 2

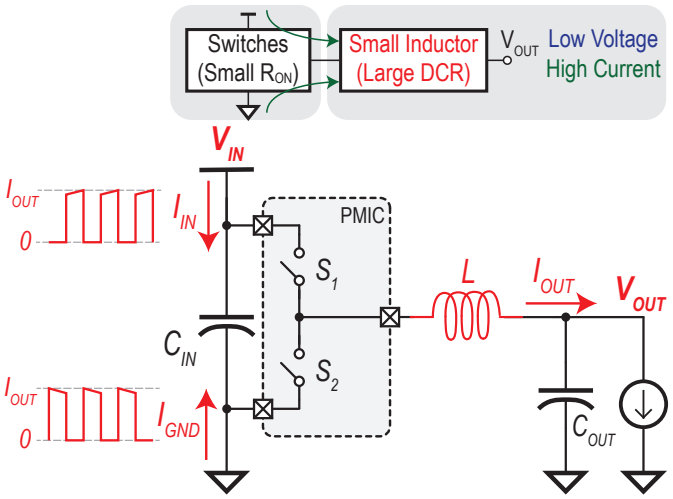
A Passive-stacked Third-order Buck Converter

2.1 Introduction

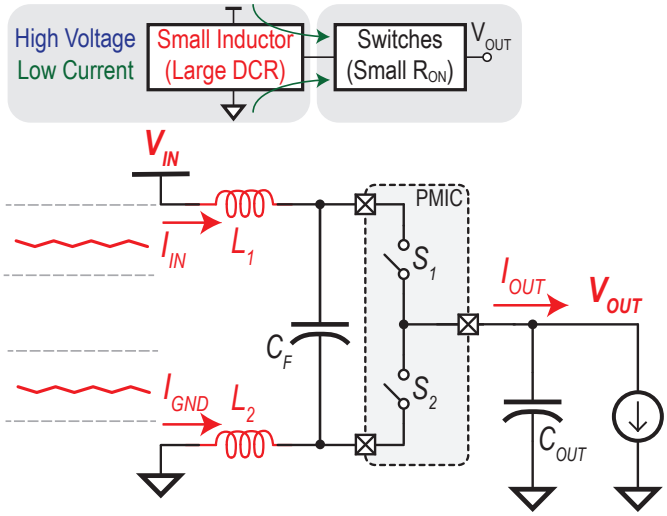
As the size of the electronics in mobile and IoT devices scale down while performance demands scale up, power management integrated circuits (PMICs) face increasing pressure to provide highly-efficient conversion in increasingly small areas. Unfortunately, efficiency and power density tend to trade-off with each other for a given topology.

This trade-off is well-illustrated in a conventional buck converter [30, 31]. To minimize losses, inductors that have low DC resistance (DCR) are typically employed; unfortunately, such inductors are physically large. Choosing a smaller inductor to increase power density directly results in increased DCR and decreased efficiency. Besides building better passives or enabling tighter packaging integration, the best way to break this trade-off is to explore other converter topologies. Topologies such as switched capacitor [32], resonant [9], or multilevel hybrid converters [23] can help in addressing these challenges. While potentially impactful in a number of applications, they do have limitations like increased circuit complexity and/or limited output regulation range which can hinder the power density or the efficiency for some applications.

To help break the efficiency-power density trade-off, this chapter presents another topology, termed a passive-stacked 3^{rd} order buck (PS3B) converter [33], that has some benefits (and some trade-offs) over the aforementioned topologies.



(a)



(b)

Figure 2.1: (a) A conventional buck converter with a small-size inductor that is processing a high load current. (b) The proposed PS3B converter with small-size inductors that are processing the low input current.

2.2 Building-up the PS3B Converter

To understand the PS3B converter, first consider a conventional buck converter, shown in Fig. 2.1(a). Here, switches S_1 and S_2 chop the voltage left of the inductor between V_{IN} and GND, causing large pulses of current between 0 and I_{OUT} to flow out of the V_{IN} and GND terminals, while capacitor C_{IN} is used to decouple the input.

As a step-down converter, V_{IN} is larger than V_{OUT}, and thus $< I_{IN} >$ is smaller than $< I_{OUT} >$. This means that the inductor, which is designed to be small to support high power density and therefore has high DCR, is processing high current, leading to large I^2R losses.

The main idea of the PS3B converter is to swap the locations of the switches and the inductor, so that the high-DCR inductor can process low current [33, 34], while the switches are moved to the output side and still process the same current. This idea is accomplished by splitting the inductor into two half-sized inductors, and placing them in series with the V_{IN} and GND terminals, as illustrated in Fig. 2.1(b). In this case, the input capacitor becomes flying and all the passives except the output capacitor are stacked at the input. Since the power conversion process is achieved through three passive elements, it is called a 3^{rd} order buck [35], in this case with stacked passives.

Figure 2.2 shows the operation principle of the PS3B converter. Since the average voltage on the inductors should be zero, the voltage on the flying capacitor, V_F must be equal to V_{IN}. The converter has two switching nodes at the top and bottom plates of the capacitor: V_{X1} and V_{X2}. In phase Φ_1, S_1 is turned on for a duration of DT_{SW}. Here, $V_{X1} = V_{OUT}$ and accordingly, V_{X2} must be $(V_{OUT} - V_{IN})$. In phase Φ_2, S_2 is turned on, and $V_{X2} = V_{OUT}$ and $V_{X1} = (V_{IN} + V_{OUT})$.

To ensure the topology is well-defined according to Kirchoff's voltage law, inductor volt-second balance can be computed. Assuming the voltage on L_1 switches between $(V_{IN} - V_{OUT})$ and $(V_{IN} - V_F - V_{OUT})$ and L_2 switches between V_{OUT} and $(V_{OUT} - V_F)$, solving the volt-second relations of the two inductors yield that $V_F = V_{IN}$ which is the same value assumed before, and more importantly $V_{OUT} = DV_{IN}$. Interestingly, this is the same relation as a buck converter, hence the name 3^{rd} order buck.

2.3 PS3B Topology Features

The PS3B converter offers several benefits in terms of losses, noise, and structure that will be described below.

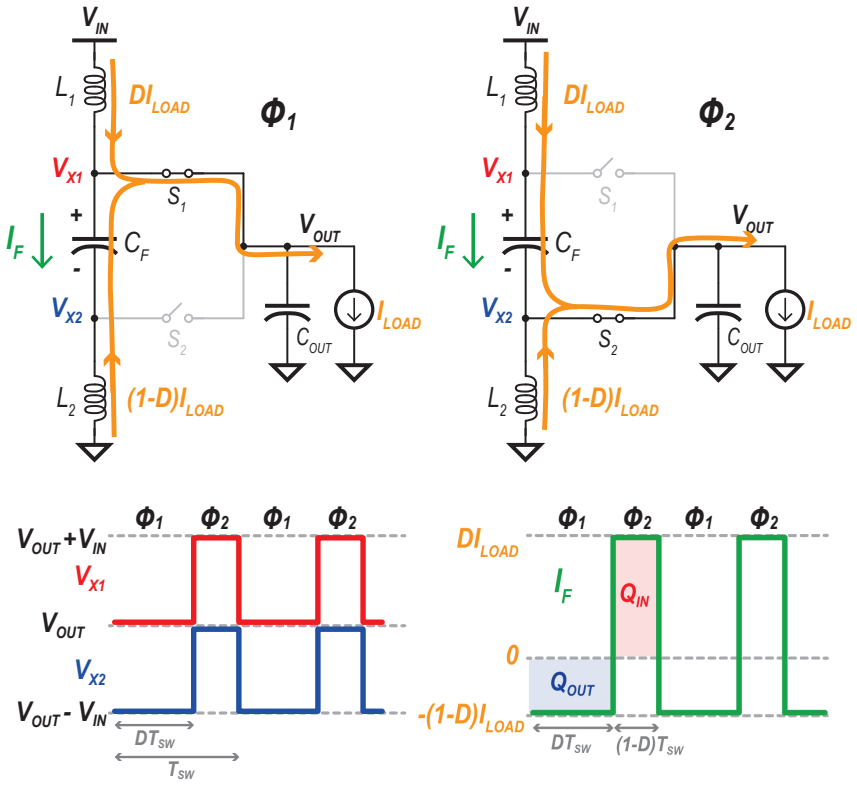


Figure 2.2: The two phases of operation of the PS3B converter showing the voltage at the two switching nodes of the converter.

Losses

The losses of a conventional buck that uses a small, high-DCR inductor are dominated by the $I_{LOAD}^2 \times$ DCR losses. The total losses, including MOSFET losses, for a specific design example are shown in Fig. 2.3. On the other hand, the inductors at the input of the PS3B divide their current contributions, and therefore process lower current. In this case, the total inductor losses are going to be lower by a factor of n, and are given by $nI_{LOAD}^2 \times$ DCR, where $n = (1 - 2D + 2D^2)$ and is between 0.5 and 1 depending on the duty ratio, D.

To compare between the PS3B converter and the conventional buck converter, the same total inductor volume is allocated for both converters, which means that the DCR of each of the PS3B converter inductors is going to be larger by 25% according to the data shown in Fig. 2.3 for commercial compact inductors. For the same MOSFET

characteristics, the total conduction losses of the PS3B are also shown in Fig. 2.3. Here, it can be seen that for duty-ratios centered around 0.5, which corresponds to the useful SoC voltage range for an input voltage of 1.8 V, the PS3B achieves lower losses than a conventional buck converter thanks to the inductors processing lower current, even despite the increased DCR. However, it should be noted that when the duty cycle becomes extreme, the conduction losses of the PS3B converter are worse than a conventional buck converter, since most of the current flows through only one of the inductors, which has a larger DCR.

Interestingly, at a duty-ratio of 0.5, the PS3B achieves the same theoretical losses as a 2-phase buck converter when using the same two inductors. However, when including the losses and complexity needed for current sensing and/or current balancing, the estimated conduction losses of a 2-phase buck increase [36], potentially beyond that of the PS3B near $D = 0.5$. It should be noted, however, that the PS3B converter also comes with other benefits that do not exist in conventional or 2-phase buck converters that will be described next.

Noise

In conventional buck converters, the input current swings fully between zero and I_{LOAD}, both at the input rail and the ground rail as shown in Fig. 2.1(b). This switching introduces noise and EMI at the input, which can be problematic to other circuits powered from the same supply. On the other hand, the input current in the PS3B converter is continuous from both the input and ground rails, with only small ripples imposed on them, which means substantially reduced noise and EMI at the input. In order to overcome this problem in conventional buck converters, additional input filtering using inductors or extra-large capacitors might be required.

It should be noted, however, that the trade-off for reduced input current ripple is that, for the same value of the output decoupling capacitor, the output voltage ripple is doubled compared to that of a conventional buck converter since the inductor currents

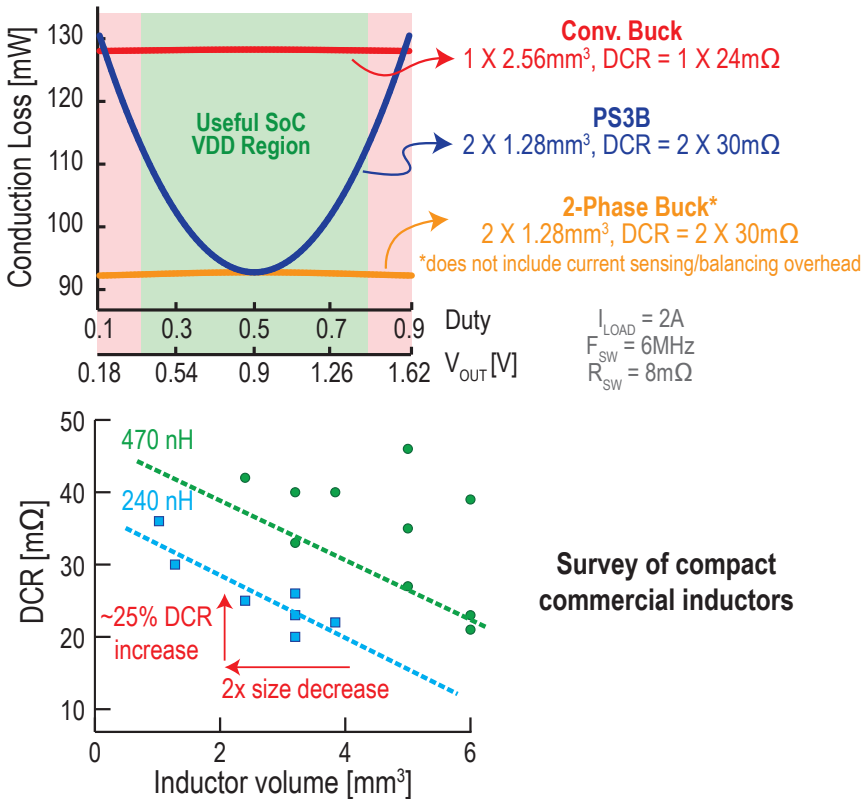


Figure 2.3: Comparison between the losses of the conventional buck converter, 2-phase buck converter and the PS3B converter using a same total allocated inductor volume for the three converters.

add in phase. Since the area of the output capacitor is much less than that of the inductors, doubling the amount of capacitance does not necessarily lead to a significant increase in overall converter area, and thus this is a welcome trade-off in most cases. The measurement results in Section 2.5 will show, for example, that reasonable ripple can be achieved at a state-of-the-art power density.

Structure

In a conventional buck converter, the input voltage is filtered by an input capacitor (and potentially an inductor), and then brought into the PMIC. The PMIC's switches connect to an off-chip inductor, whose output is then connected to a load (i.e., the PMIC and the load are separated by the inductor as depicted in Fig. 2.4). In the PS3B con-

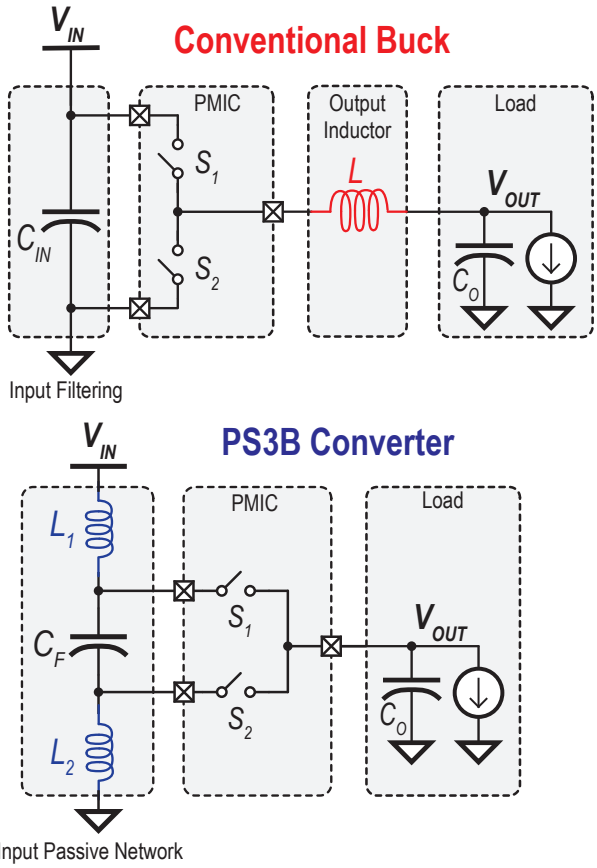


Figure 2.4: Comparison between the structures of the conventional buck converter and the PS3B converter.

verter, the input filtering block is replaced by an input passive network which includes all the passives required for the power conversion process and for input filtering, which, depending on the employed packaging solution and desired layout, may result in a more compact implementation area.

Transient Response

Although detailed analysis of the transient behavior of the PS3B converter is outside the scope of this chapter, preliminary state-space analysis of a voltage-mode PS3B power stage (when neglecting the parasitic resistances of the individual components) reveals that the converter has two main poles that are generally located at frequencies higher than that of the conventional buck converter for the same inductor and output ca-

pacitor values. In addition, due to having the inductors placed at the input, there are two other poles and two zeros that tend to cancel each other near $D = 0.5$. When $D = 0.5$, the extra two poles exactly cancels the two zeros and the system frequency response becomes a second order with the two main poles located at $(1/2\pi\sqrt{0.5LC})$, where the effective inductance is reduced by half. As a result, the PS3B converter transient response might have potential benefits by having reduced effective inductance, but there are challenges related with the additional zeros and poles which can be mitigated by careful selection of the component values. These trade-offs will be explored in a future publication.

2.4 Circuit Implementation

Figure 2.5 shows the full schematic of the implemented PS3B converter. The circuit operates as follows. In phase Φ_1, M1 is turned on by connecting its gate to $(V_{OUT} + V_{IN})$ and M2 is turned off by connecting its gate voltage to V_{OUT}. In phase Φ_2, M2 is turned on by connecting its gate to $(V_{OUT} - V_{IN})$ and M1 is turned off by connecting its gate to V_{OUT}. This means that non-standard voltage levels are required to drive the power MOSFETs. Fortunately, these voltage levels are already available at the switching nodes V_{X1} and V_{X2}, albeit in the wrong switching phases. Bootstrapping capacitors are thus needed to capture these voltages during the right phases.

To accomplish this, the driver of the upper power MOSFET is implemented with bootstrapping capacitor, C_{boot1}, that stores $(V_{OUT} + V_{IN})$. Similarly, the driver of the lower power MOSFET is implemented with bootstrapping capacitor, C_{boot2} that stores $(V_{OUT} - V_{IN})$. Figure 2.6 shows the driver operation in each of the two phases. Normally, the bottom plate of these bootstrapping capacitors would be connected to ground. However, since the top plates would extend above V_{IN} and below GND, this would cause undue stress across the capacitors. Thus, the bottom plate of C_{boot1} and the top plate of C_{boot2} are instead connected to V_{OUT}, so that each of them only ever experience a voltage of V_{IN}, which allows for up to 4x saving in their implementation

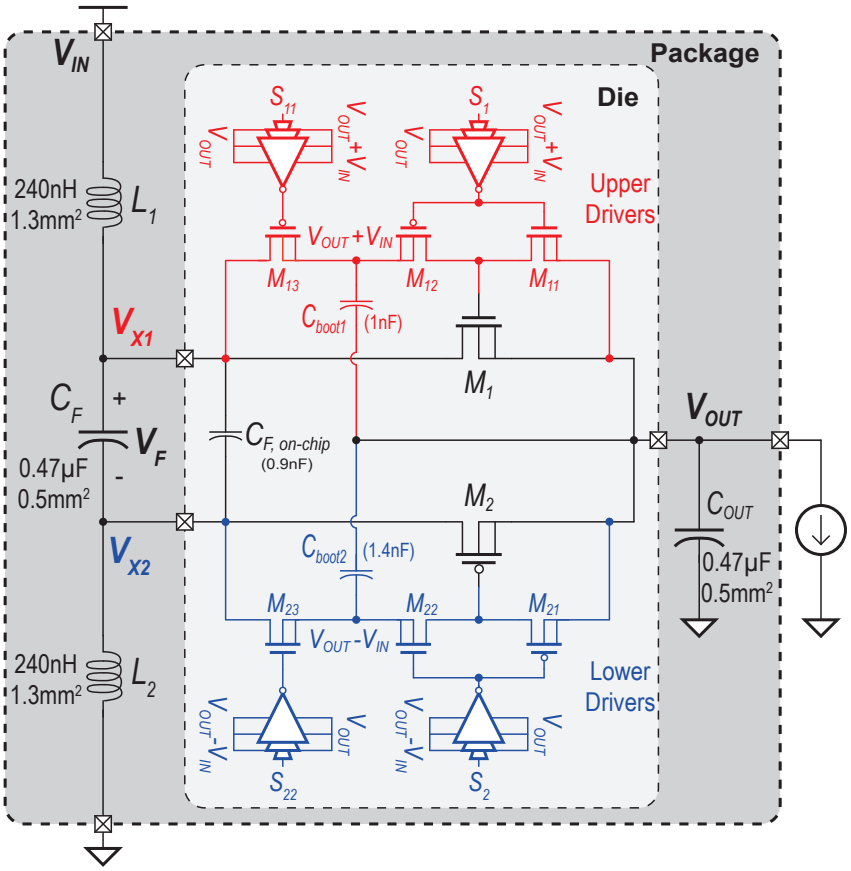


Figure 2.5: The converter full schematic showing the drivers for the upper and the lower switches.

area on chip. To enable high capacitance density, C_{boot1} is implemented as a standard MOS capacitance, while C_{boot2} is implemented as a MOS capacitor in a deep n-well as illustrated in Fig. 2.7.

It is important to note that, as shown in Fig. 2.5, all the drivers are powered only from the internal nodes of the converter: V_{OUT}, $(V_{OUT}+V_{IN})$, or $(V_{OUT}-V_{IN})$, with no need for external supplies, in contrast to many recent hybrid multi-level designs that require auxiliary DC-DC converters for their drivers. Figure 2.8 shows the controller used to generate the four control signals of the converter. Two-stage level-shifters, shown in Fig. 2.9 shift the control signals from 0,V_{IN} to the appropriate levels for the drivers. All of the drivers and the level shifters are powered by either V_{OUT} or by one of the two bootstrapping capacitors, and thus no external voltage sources are needed. The timing

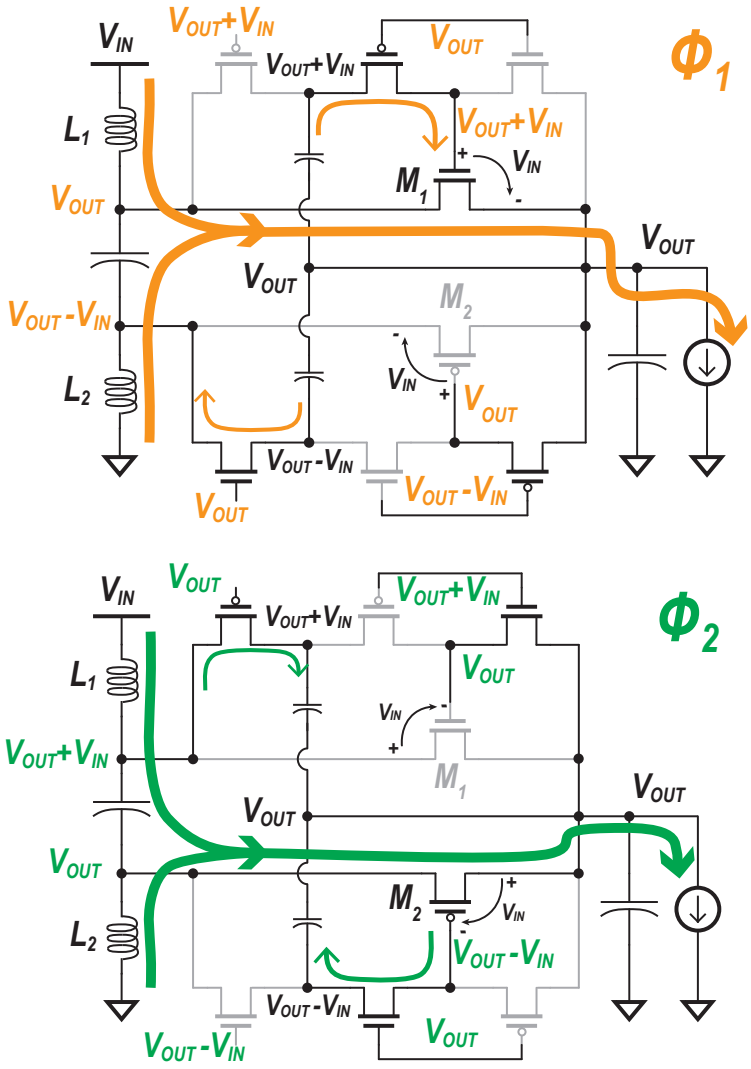


Figure 2.6: The two operating phases of the converter showing the driver status in each phase.

between the different control signals is adjusted carefully through a deadtime circuit so that the dis/charging of MOSFETs' gate capacitance and the bootstrapping capacitors is done in the proper sequence.

It can be noted that inside the PMIC, there are no MOSFETs nor capacitors referenced to ground as depicted in Fig. 2.5. Instead, there are multiple MOSFETs and capacitors referenced to V_{OUT}. Therefore, the chip bulk in this implementation is biased to V_{OUT} instead of ground. In this case, the upper-side components of the converter were

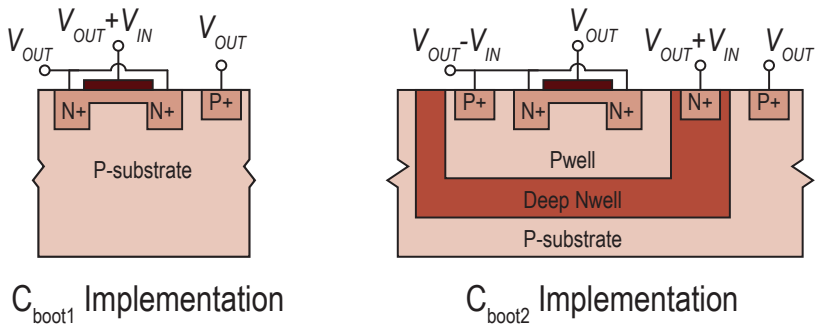


Figure 2.7: Cross-section for the bootstrap capacitor implementation.

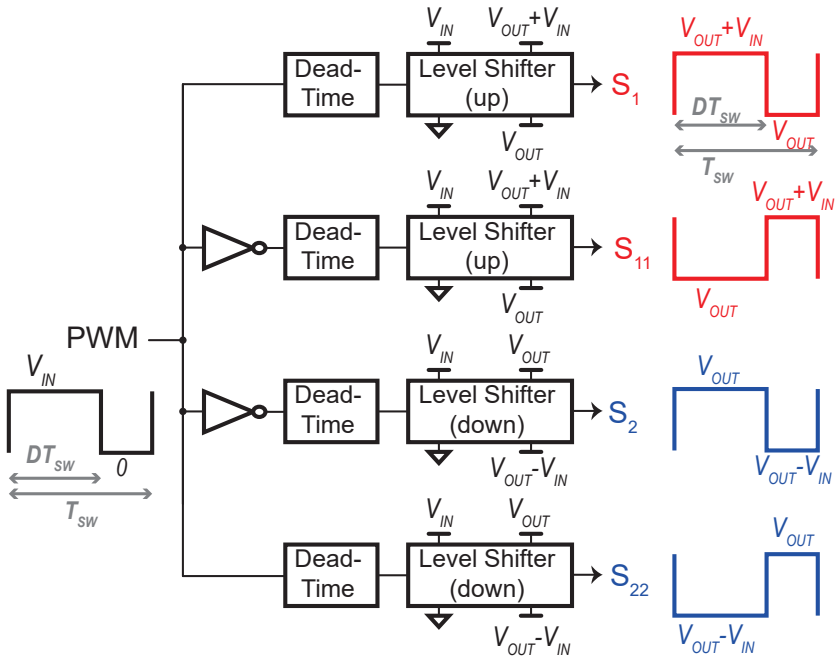


Figure 2.8: Generation of level-shifted signals from an input PWM signal.

implemented directly as standard bulk devices instead of deep n-well devices, while the lower-side components are implemented in deep n-wells. It should be noted that this is not strictly required, and the chip bulk could still have been biased to ground, but with the upper-side devices instead implemented in the deep n-well.

Although the voltage at some nodes in the PS3B converter is boosted over or below V_{IN}, all the switches and capacitors have a blocking voltage that does not exceed V_{IN}, just like a buck converter. Also, the parasitic capacitances of the power MOSFETs

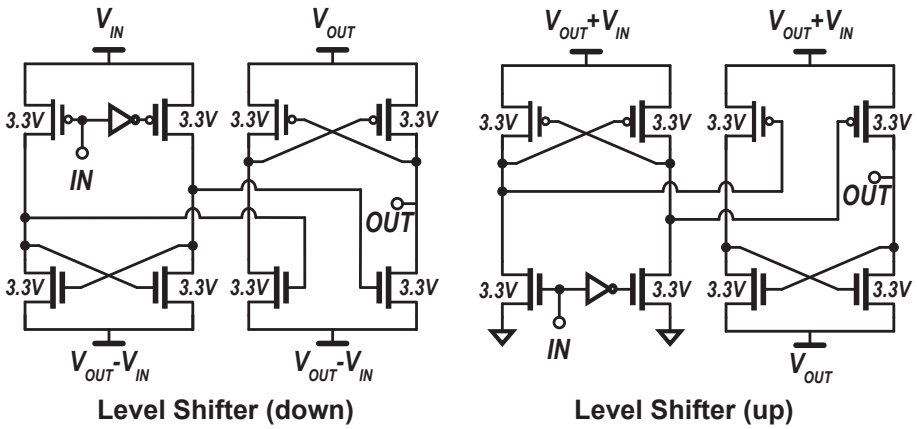


Figure 2.9: Schematics of the level-shifters.

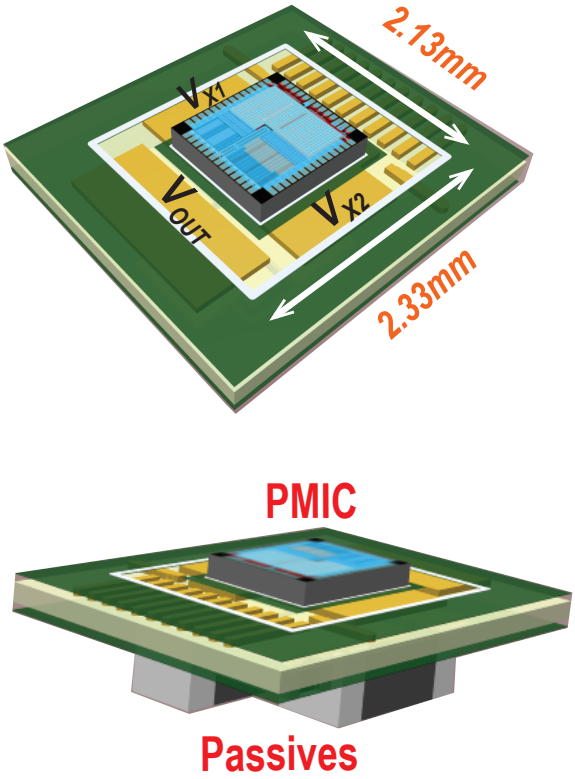


Figure 2.10: 3D render of the converter packaging on a small interposer.

experience the same voltage difference as in the buck converter, and hence both converters have similar switching losses. Figure 2.10 shows a 3D render of the converter packaging on a small interposer.

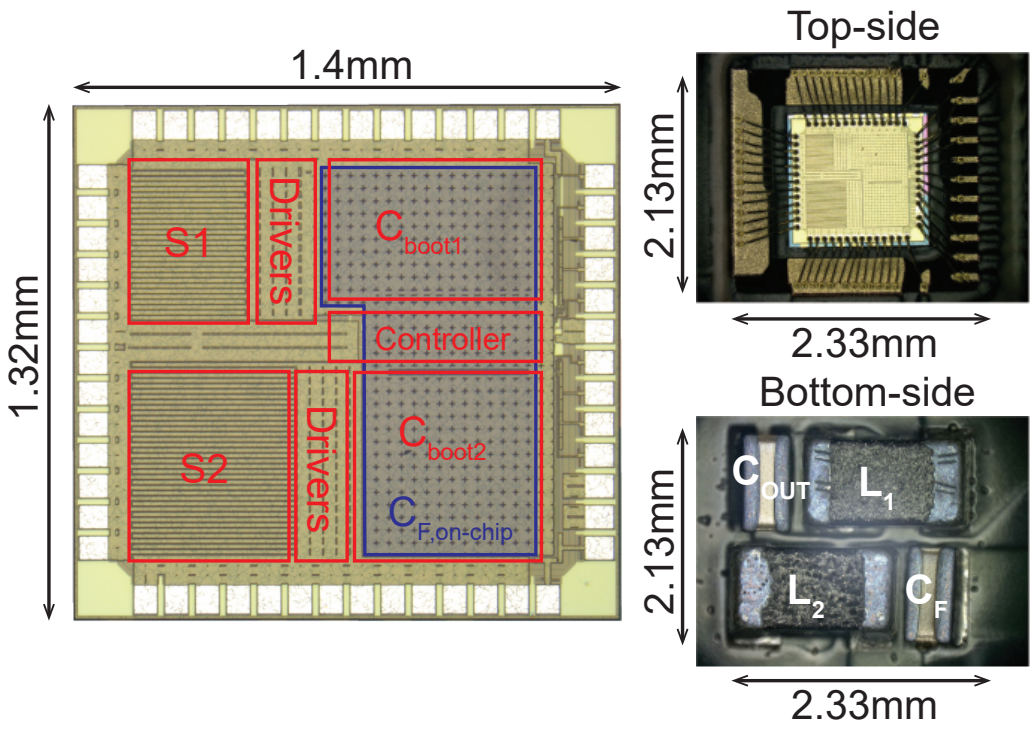


Figure 2.11: Die photo and converter assembly.

2.5 Measurement Results

The PMIC was implemented in a 0.18 μm CMOS process. A die photo and photo of the assembled converter are shown in Fig. 2.11, where the PMIC is placed and wirebonded to one side of an interposer, while the passives are placed and soldered on the underside. The converter has a total footprint of 5 mm^2, which including all the passives, the routing between the passives, and the routing between the two converter sides. Thanks to the passive-stacked approach, routing complexity was low, which helped facilitate the low implementation area. The converter operates with a V_{IN} of 1.8 V, a V_{OUT} between 0.5 V and 1.5 V, and a maximum I_{LOAD} of 2.5 A while switching at 6.5 MHz. In this implementation, no input decoupling capacitor was used at V_{IN}.

Figure 2.12 shows the measured waveforms of the two internal switching nodes of the converter. For $V_{IN} = 1.8$ V and V_{OUT} of 1 V, V_{X1} is switching between 1 V and 2.8 V, while V_{X2} is switching between -0.8 V and 1 V, which are the correct voltage

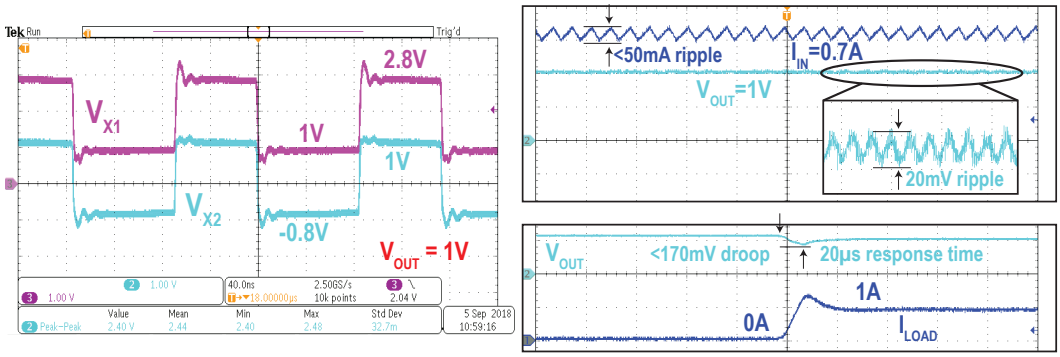


Figure 2.12: Measured waveforms of the converter switching nodes, input current and output voltage.

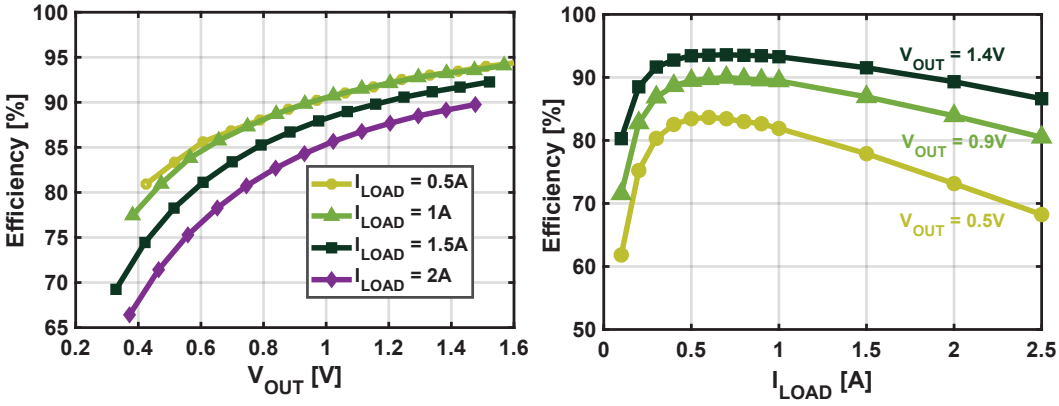


Figure 2.13: Measured efficiency versus I_{LOAD} and versus V_{OUT}.

levels for the switching nodes. Figure 2.12 also shows the measured waveform of the input current where it is continuous with less than 50mA ripple for $I_{IN} = 0.7$ A. At $V_{OUT} = 1$ V, the voltage ripple is measured to be 20 mV when employing a 0.47 μF 0.5 mm^2 output decoupling capacitor. The converter responds to a 1 A step change in the load current in less than 20 μs without any implemented feedback compensation (improvements are expected with a compensation scheme that takes into account the converter's frequency response).

The measured efficiency of the converter versus I_{LOAD} and V_{OUT} is shown in Fig. 2.13. The converter achieves a peak efficiency of 94% at a power density of 0.18 W/mm^2 or 60 W/cm^3, and it achieves a peak power density of 0.7 W/mm^2 or

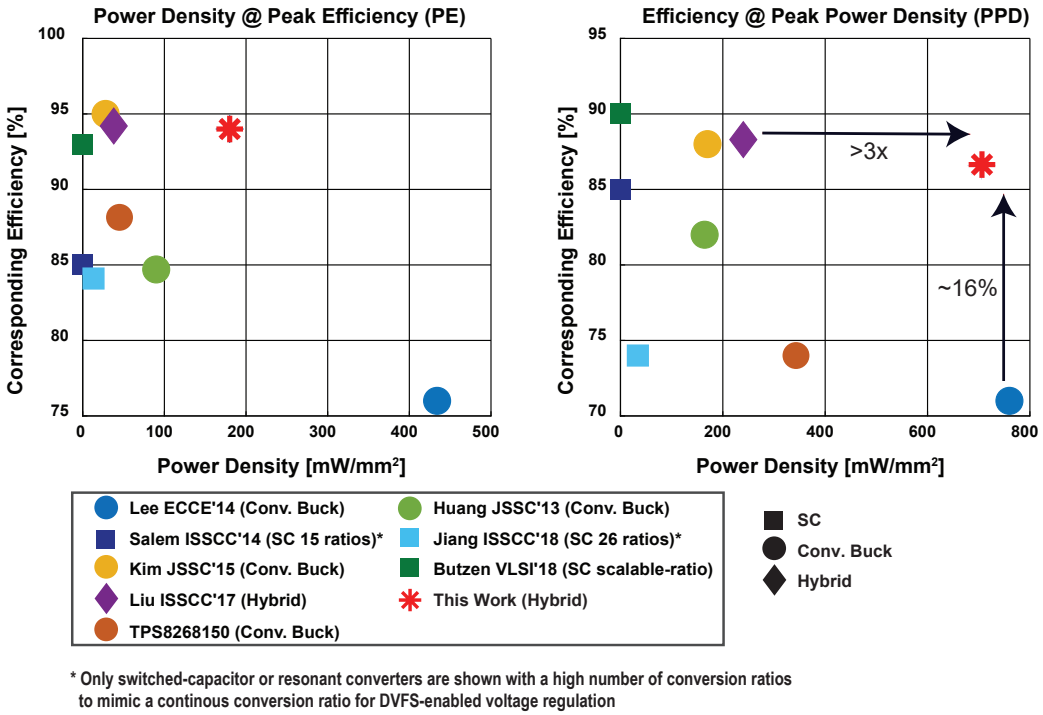


Figure 2.14: Measured efficiency and power density compared to prior-art converters that can efficiently regulate across SoC-compatible voltages and that report the total converter area (including the area of the passives and the interconnection between them).

233 W/cm^3 at a 86.6% efficiency. If the area of only the passives are taken into account, as some other work in the literature report (presumably in the event that better packaging technology could be available), then the peak power density increases to 1 W/mm^2.

Table 2.1 shows a comparison with previous work. The PS3B converter has a unique feature of continuous input current, can help reduce the area needed for on-board filtering in certain applications. Compared to previous converters that operate with continuous conversion ratios across the SoC-compatible voltage range, the PS3B converter achieves a higher peak power density, while also achieving a comparable peak efficiency of 94% but at a 4$\times$ higher power density, albeit in some cases for lower conversion ratios. Figure 2.14 shows a comparison to prior-art that report the total converter area (including the area of the passives and the interconnection between them).

Table 2.1: Table of comparison to prior-art.

	Kim JSSC'15	Lee ISSCC'17	Liu ISSCC'17	Jia JSSC'18	Jiang ISSCC'18	TI TPS8268150	This Work
Topology	Buck	Buck (4-phase)	Hybrid (Multilevel)	Buck	SC (26 ratios)	Buck	**Hybrid (PS3B)**
Technology	65nm	350nm	65nm	65nm	65nm	NR	**180nm**
Inductor	220 nH	4 × 200 nH	470 nH	(3 + 8.2) nH	-	NR	**2 × 240 nH**
Flying Capacitor	-	-	3 × 22 µF	-	8 nF	-	**0.47 µF**
Output Capacitor	4.7 µF	2.5 µF	22 µF	0.12 nF	6 nF	NR	**0.47 µF**
Input Voltage [V]	1.8	3.3	3.0 – 4.5	1.1	0.22 – 2.4	2.3 - 5.5	**1.8**
Output Voltage [V]	0.6 – 1.5	0.3 – 2.5	0.3 – 1.0	0.3 – 0.86	0.85 – 1.2	1.5	**0.5 – 1.5**
F_{SW} [MHz]	11 - 25	25	1	2000	NR	5.5	**6.5**
I_{LOAD} (MAX) [A]	0.6	6	1.53	0.04	0.08	1.6	**2.5**
Input Current	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	**Continuous**
PMIC Area [mm²]	5	1.88	4.05	0.13	2.42	6.67	**1.85**
Total Footprint [mm²]	5	NR	6**	0.13	2.42	6.67	**5**
Peak Efficiency (PE)	95.5%	88.1%	94.2%	73%	84.1%	88%***	**94%**
Power Density @ PE * [W/mm²]	0.03***	NR****	0.04**	NR	0.013	0.045***	**0.18 (0.25**)**
Peak Power Density (PPD) * [W/mm²]	0.17	NR****	0.24	0.27	0.034***	0.36***	**0.7 (1.0**)**
Efficiency @ PPD	88%	NR****	88.3%	NR	74%***	74%***	**86.6%**

NR – Not Reported
* Unless otherwise specified, power densities are computed with respect to the total converter footprint including the passives and routing
** Computed by summing the area of the passive component footprints
*** Estimated from measurement results
**** The area of the passives are not reported

2.6 Acknowledgement

Chapter 2 is based on and mostly a reprint of the following publications:

- A. Abdulslam and P. P. Mercier, "A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter Achieving 0.7W/mm^2 Power Density and 94% Peak Efficiency," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2019, pp. 148-150.

- A. Abdulslam and P. P. Mercier, "A Passive-Stacked Third-Order Buck Converter With Inherent Input Filtering Achieving 0.7-W/mm ^{2} Power Density and 94% Peak Efficiency," *IEEE Solid-State Circuits Letters*, vol. 2, no. 11, pp. 240-243, Nov. 2019.

The dissertation author is the primary investigator and author of the work in these papers.

Chapter 3

A Charge-recycling Inductor-first Buck Converter

3.1 Introduction

The losses related to the power MOSFETs in inductive DC-DC converters are a main contributor to the total converter losses and play an important role in determining the power conversion efficiency. Each power MOSFET has its intrinsic on-resistance R_{ON} causing conduction loss that is inversely proportional to the MOSFET width (W). In addition, each power MOSFET has also switching loss related to the charging/discharging of its gate capacitance (C_{GATE}) and this loss increases linearly with W as shown in Fig. 3.1. For a given load current, there is an optimum W that results in minimum losses but this optimum W changes as the load current (I_L) changes and there is no certain design choice of W that can give minimum losses for a wide range of load currents. Therefore, the design of inductive DC-DC converters is fundamentally limited by this trade-off between conduction losses and switching losses. Miniaturized converters used in applications such as mobile devices suffer badly from this trade off, as a small inductor has a large DCR, which contributes larger $I_L^2 DCR$ conduction losses, while a small inductance desires high frequency operation, which implies higher $C_{GATE}V^2F_{SW}$ hard charging switching losses from the power MOSFET gate drivers. To maximize the converter efficiency across a wide range of the load current, techniques to reduce these traditional MOSFET losses are needed.

Normally, power MOSFETs are driven by hard-charging or hard-discharging

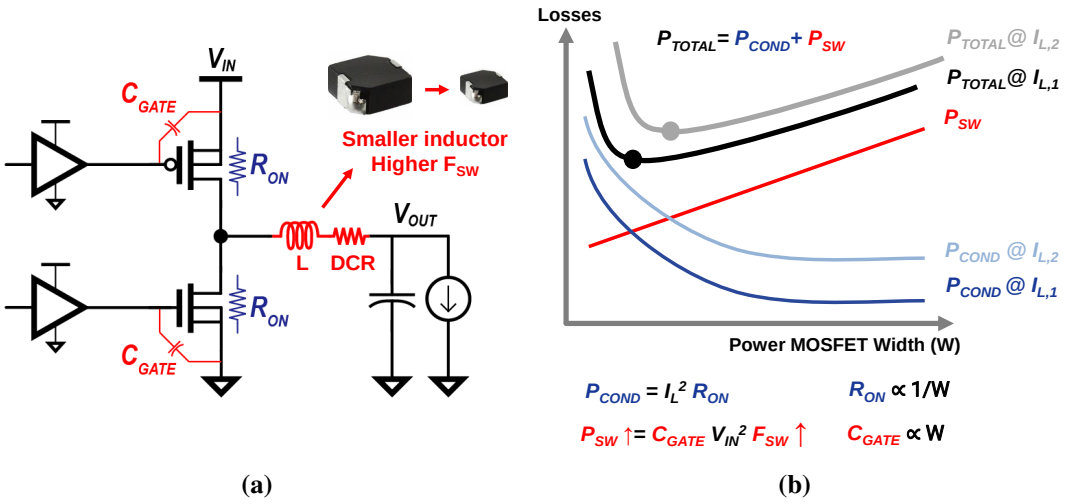


Figure 3.1: (a) Using a smaller inductor results in a higher inductor DCR and requires a higher switching frequency (F_{SW}). (b) Trade-off between MOSFET conduction losses and switching losses where the optimum MOSFET width moves around with the load current (I_L).

their gate capacitance through a driver, as shown in Fig. 3.2 (a), which results in the well-known switching losses of $C_{GATE}V^2F_{SW}$. To ease the conduction/switching loss trade-off, it is possible to replace the conventionally hard-switching gate drivers with adiabatic charge-recycling (CR) gate drivers as depicted in Fig. 3.2 (b). CR can, through the help of an inductor L_R, recycle the charge stored on the MOSFET C_{GATE} to another capacitance, C_{STORE} (and vice-versa), theoretically with 100% efficiency.

This technique of resonant charging/discharging of C_{GATE} can be applied to a conventional buck converter by AC-coupling the power NMOS to the resonant gate driver as in Fig. 3.3 [56]. One advantage is that this technique uses only one resonant inductor. However, the non-overlap time cannot be precisely controlled, leading to potentially large overlap losses, and limited duty-cycle control through driver slope modulation prevents robust regulation across a wide output range. In addition, the converter has to switch at the resonant frequency of the recycling loop which can be very high in the gigahertz range.

In order to avoid these limitations with the traditional resonant operation, an intermittent resonant charging/discharging of C_{GATE} can be done by adding a recycling

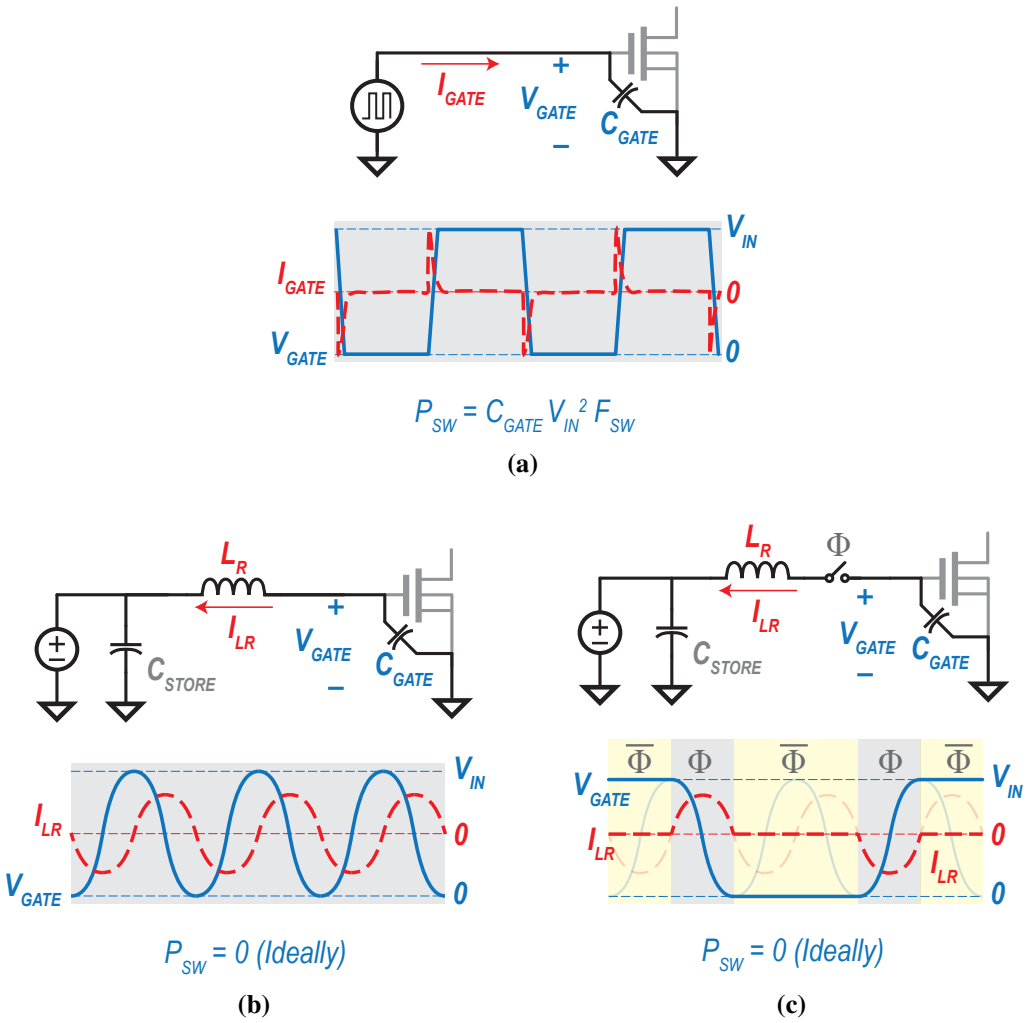


Figure 3.2: (a) Hard charging/discharging of the MOSFET gate capacitance. (b) Continuous resonant charging/discharging of the MOSFET gate capacitance. (c) Intermittent resonant charging/discharging of the MOSFET gate capacitance.

switch in the resonant loop as depicted in Fig. 3.2 (c). To trigger one recycling phase, the switch is turned ON to transfer the charges from C_{GATE} to C_{STORE} (or vice-versa) and then, the switch is turned OFF when the current in the recycling inductor reaches zero. In this case, zero switching losses are still ideally achieved but with a better control on the timing of the resonant operation.

However, it can be noted that this intermittent resonant operation requires some finite rise/fall time for the gate signals of the power MOSFETs to perform the charge

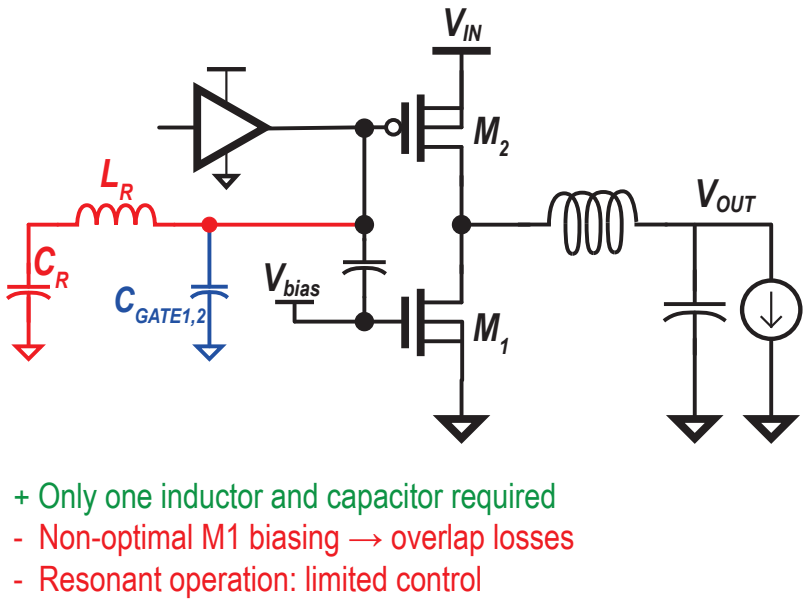


Figure 3.3: Resonant gate charge recycling applied to a conventional buck converter.

recycling which can lead to increased V-I overlap losses in the power MOSFETs. Interestingly, the rise/fall time of such drivers cannot be too rapid, regardless of switching frequency, due to inductive ringing causing potential voltage stresses for the power MOSFETs [23, 29] as illustrated in Fig. 3.4. Therefore, it is possible to exploit the requirement for finite rise/fall time to apply the charge recycling without degrading the converter performance.

This approach of intermittent resonant recycling was demonstrated in [57], where the charge on the power MOSFET gates are recycled to two auxiliary capacitors through two separate inductors as shown in Fig. 3.5. However, besides the overhead of two inductors, recycling with separate storage capacitors introduces indirect losses, while the separated duty-cycled resonate gate drivers makes non-overlap timing control between power MOSFETs difficult.

This chapter presents the design of an inductor-first 3rd order buck converter that elegantly and effectively enables direct, reciprocal recycling of gate charge from one power MOSFET to the other by the addition of only a single inductor and two switches, all without affecting converter operation or control and while ensuring non-

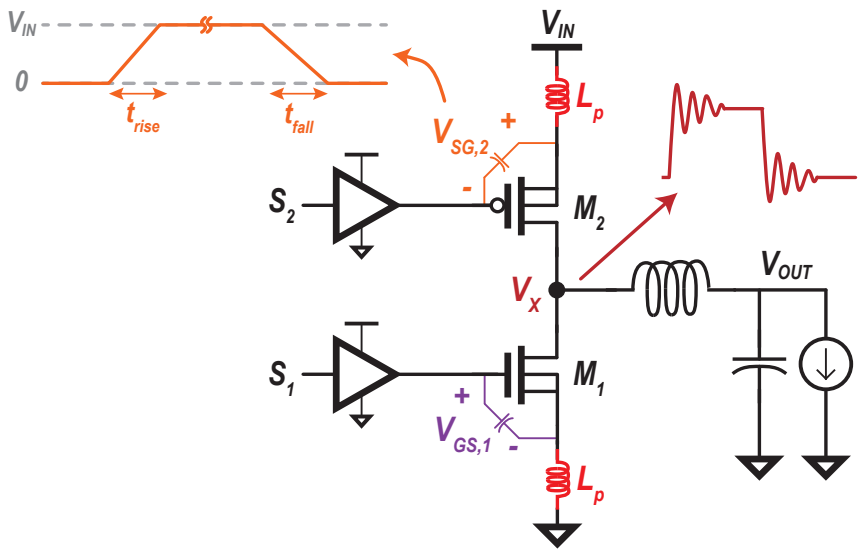
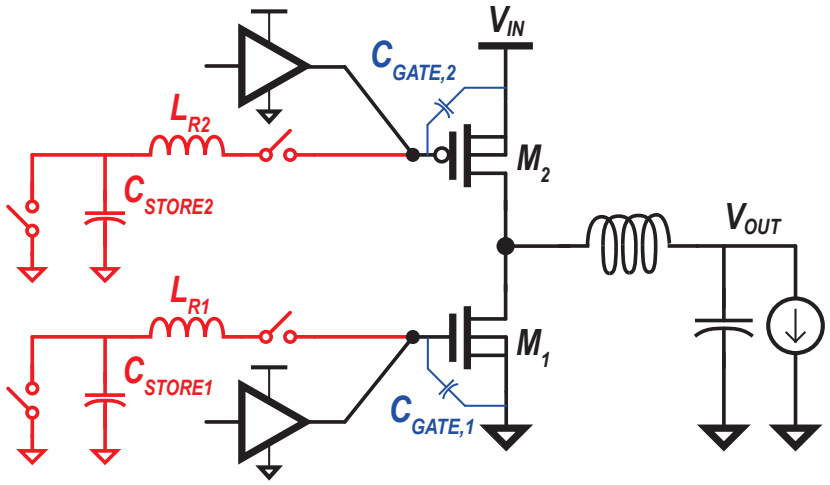


Figure 3.4: Voltage ringing at the switching node (V_X) due to rapid rise/fall time of the drivers.



- Extra inductor and capacitor per power MOSFET
- Recycling with storage cap ⟶ indirect losses
- Two independent drivers ⟶ overlap issues

Figure 3.5: Intermittent resonant charge recycling applied to a conventional buck converter.

overlap conditions.

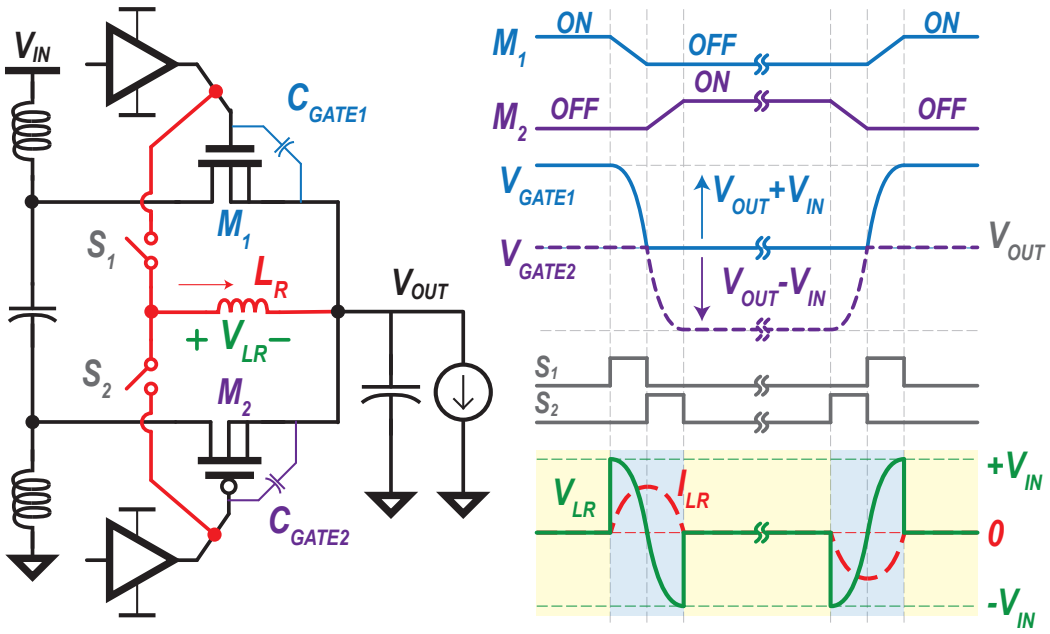


Figure 3.6: Proposed direct reciprocal charge recycling applied to an inductor-first 3rd order buck requiring only a single inductor and two switches that do not interfere with normal control.

3.2 Charge-recycling Inductor-first Converter

The proposed charge-recycling inductor-first buck converter is shown in Fig. 3.6. The gates of M_1 and M_2 in a 3rd order buck switch with amplitude V_{IN} above and below V_{OUT}, respectively. Instead of hard switching M_1 and M_2 through flying inverter-based drivers, the proposed design first asserts S_1 to charge recycling inductor L_R via the gate charge stored on M_1, until C_{GATE1} is fully depleted (i.e., $V_{GATE1} = V_{OUT}$, $V_{LR} = 0$, and I_{LR} is maximal). At this point, S_1 turns off and S_2 is asserted, using the stored energy in the inductor to charge C_{GATE2}; the reverse scenario occurs when turning off M_2. By using this technique, direct reciprocal charge recycling between power MOSFETs can be performed.

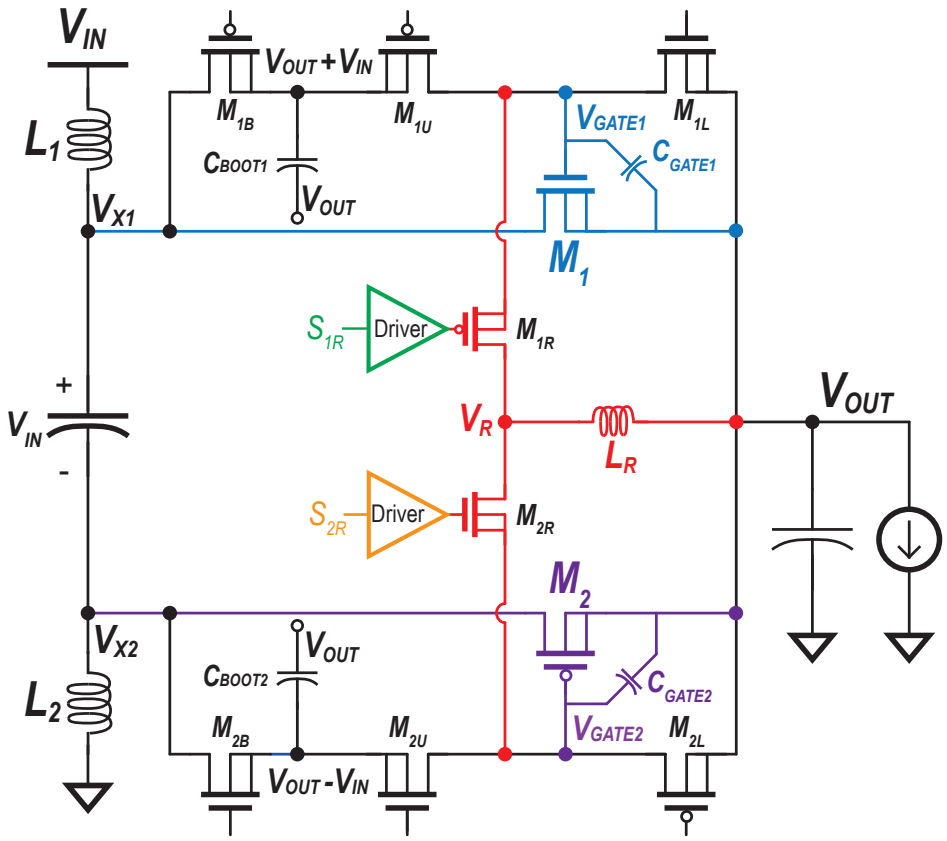


Figure 3.7: Schematic of the inductor-first 3rd buck converter with direct reciprocal charge recycling.

3.2.1 Normal Circuit Operation

Fig. 3.7 shows a detailed schematic for the converter. During normal operation of the 3rd order buck, M_1 and M_2 switch with duty cycle D, leading V_{X1} to switch between V_{OUT} and (V_{OUT}+V_{IN}), and V_{X2} to switch between (V_{OUT}-V_{IN}) and V_{OUT}. Inductor volt-second balancing then ensures the flying capacitor is balanced at V_{IN}, and V_{OUT} = DV_{IN}. Two bootstrapping capacitors, $C_{BOOT1,2}$ are used to internally generate two level-shifted rails V_{OUT}+V_{IN}, V_{OUT}-V_{IN} needed to drive M_1 and M_2, which turn ON by connecting their gate terminals to C_{BOOT1}, C_{BOOT2} through M_{1U}, M_{2U}, and turn OFF by dumping their gate charges to the V_{OUT} node through M_{1L}, M_{2L}; hence, their gates are nominally hard charged with a swing of V_{IN}.

3.2.2 Applying Gate Charge Recycling

To instead recycle these gate charges, a small PCB-trace charge recycling (CR) inductor, L_R, is placed between V_{OUT} and internal node V_R; thus only one addition pin on the PMIC is needed as shown in Fig. 3.7. Here, V_R is connected to the gate of power MOSFETs M_1, M_2 through CR MOSFETs M_{1R}, M_{2R} to form a charge recycling loop that involves C_{GATE1} and C_{GATE2} where M_{1R} is implemented as a PMOS while M_{2R} is implemented as an NMOS. By having a minimum number of passives (L_R) and active components (M_{1R}/M_{2R}) in the CR loop, the total parasitic resistance is low, yielding a CR efficiency up to 80%.

CR control can be employed on top of normal converter operation. Fig. 3.8 shows the converter operating phases under the CR technique with the key waveforms illustrated in Fig. 3.9. When M_1 is normally ON, its gate is tied to (V_{OUT}+V_{IN}) through M_{1U}. When M_1 begins to turn off, M_{1U} is deactivated and M_{1R} is activated so that C_{GATE1} discharges completely in L_R. At this point, M_{2R} is turned ON to charge C_{GATE2} from the stored energy in L_R. Then, the regular gate drivers are activated to tie the power MOSFET gate terminals to the appropriate voltages, while M_{1R} is turned on to discharge any residue charges in L_R that might occur due to imperfect control timing. Similarly, the same process can be applied when M_2 turns OFF to recycle the charge back from C_{GATE2} to C_{GATE1}. Therefore, to apply gate CR, four additional phases of small duration are added to the converter two basic operating phases and without affecting the converter normal operation.

3.3 Recycling Efficiency

The charge recycling efficiency represents the percentage of the power MOSFET gate charges that was recycled and not dissipated when the power MOSFETs are

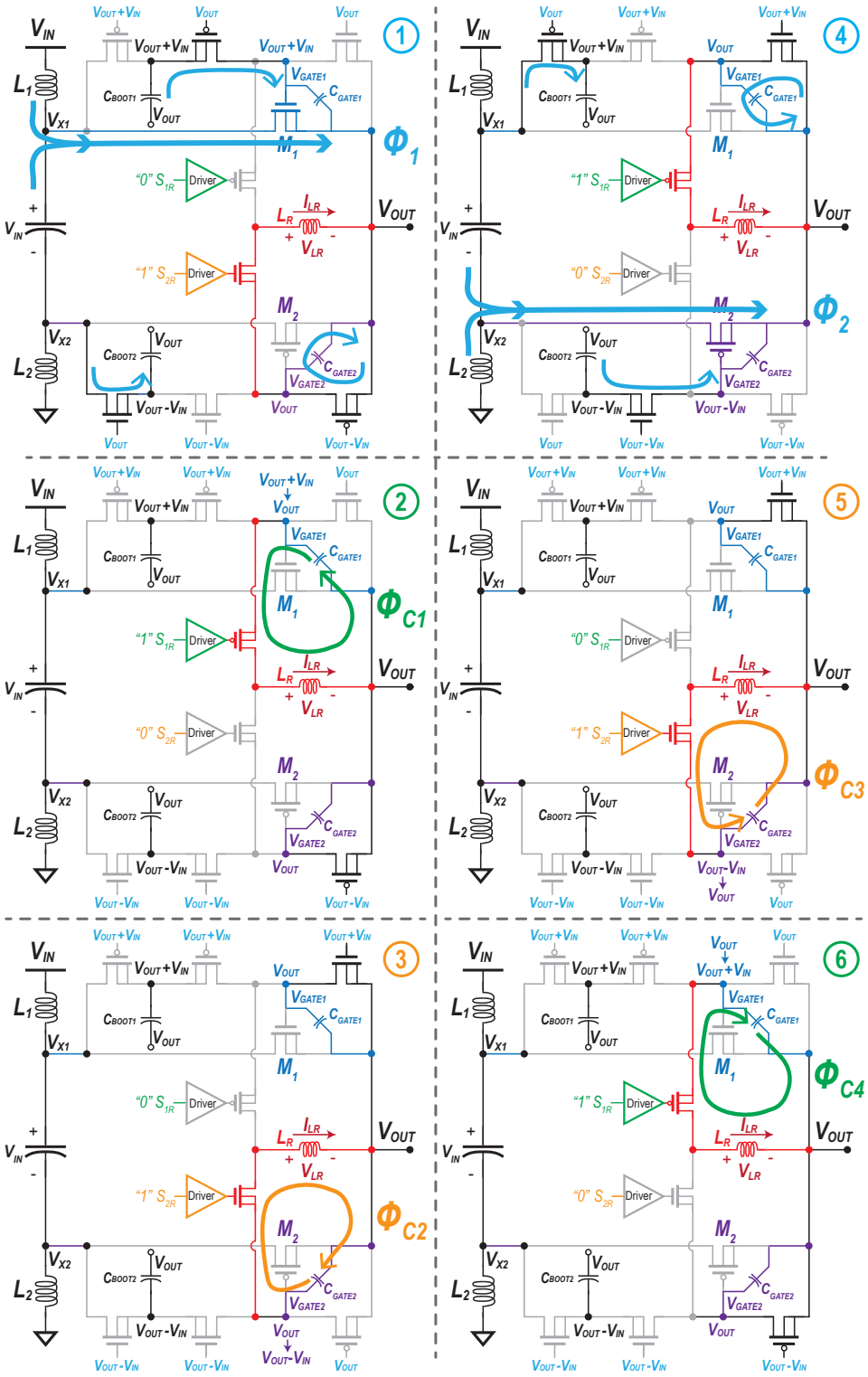


Figure 3.8: Illustration of the current flow and the driver configuration during the 6 states.

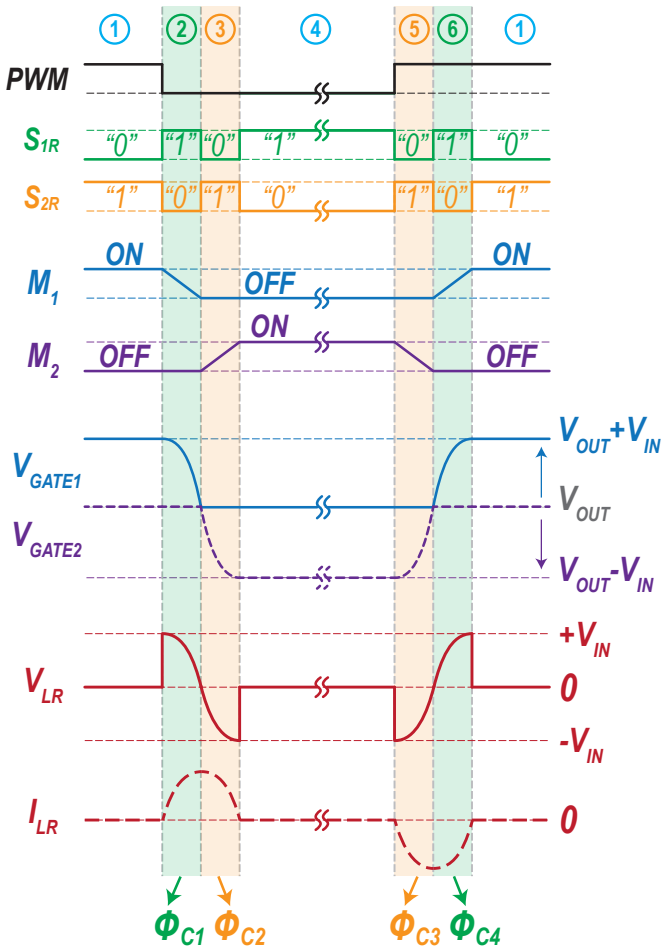


Figure 3.9: Converter key waveforms during the converter states that consist of 2 normal states and 4 recycling states.

changing their states. The recycling efficiency (η_R) can be defined as:

$$\eta_R = 1 - \frac{P_{SW,Recycle}}{P_{SW,Hard}} = 1 - \frac{P_{SW,Recycle}}{(C_{GATE1} + C_{GATE2})V_{IN}^2 F_{SW}} \tag{3.1}$$

, where $P_{SW,Recycle}$ is the total gate drive losses when recycling is applied, $P_{SW,Hard}$ is the gate drive losses without recycling (i.e. hard charging/discharging of the gate capacitance), F_{SW} is the switching frequency, and C_{GATE1} and C_{GATE1} are the gate capacitance of M_1 and M_2, respectively.

The CR loop has its own parasitics, shown in Fig. 3.10. These parasitics mainly include the equivalent DCR of the recycling inductor and the switching and the conduc-

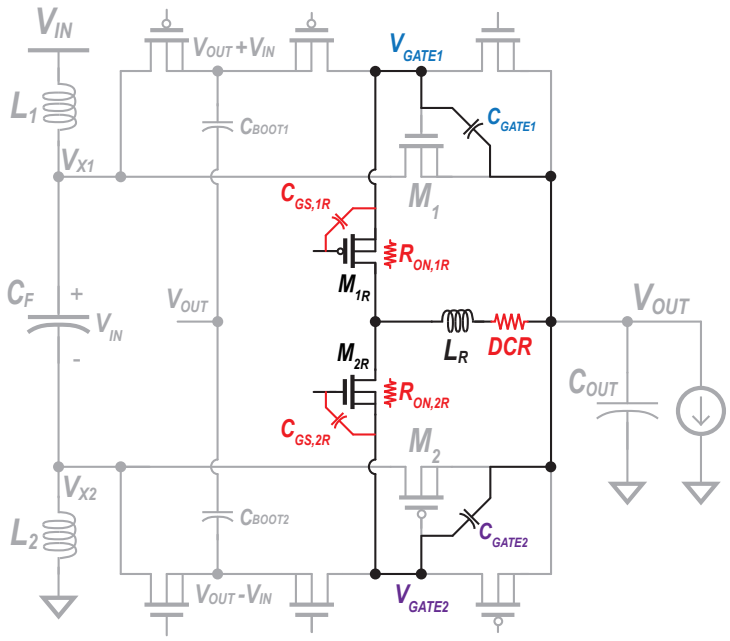


Figure 3.10: Losses in the charge recycling loop due to the parasitics of the recycling MOSFETs and the recycling inductor.

tion losses of the recycling MOSFETs due to their ON-resistance and gate capacitance. These CR loop parasitics can degrade the CR efficiency. However, increasing the recycling inductor (L_R) size, which helps recycle a larger amount of charge (with lower RMS current in the loop), can help to reduce gate driver losses and improve the CR efficiency. As illustrated in Fig. 3.11, for 50mΩ DCR, $C_{GATE1,2}$ = 200 pF, and while including the conduction and switching losses of M_{1R} and M_{2R} (which are 3% of the size of M_1 and M_2), 60-80% recycling efficiency is achievable with L_R ranging from 1-10 nH thanks to the relatively low losses in the charge recycling loop. However, increasing L_R too high results in too slow rise/fall time of $V_{GATE1,2}$, leading to higher V-I overlap losses in M_1 and M_2.

Fig. 3.12 illustrates the trade-off between the gate driver losses and V-I overlap losses for a representative light load current. When combining the overlap losses with the gate drive losses (while charge recycling is applied) the total losses will have a shallow optimum illustrating reduced overall losses (even when overlap losses are increasing

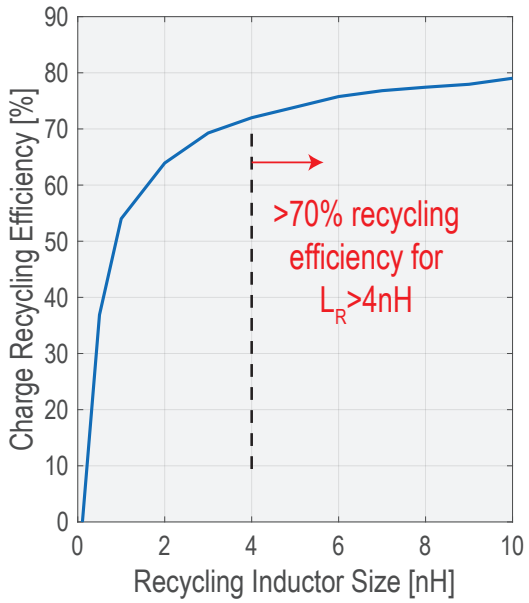


Figure 3.11: Charge recycling efficiency versus recycling inductor size showing >70% recycling efficiency for >4 nH recycling inductors.

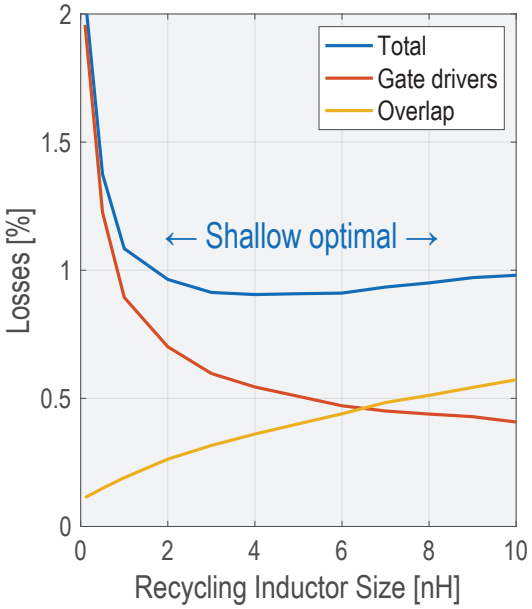


Figure 3.12: Trade-off between the gate driver losses and V-I overlap losses for a representative light load current illustrating a shallow optimum.

with the recycling inductor size). At higher load currents, partial CR can be applied by reducing the pulse duration of the CR signals. It is also important to recall that, practi-

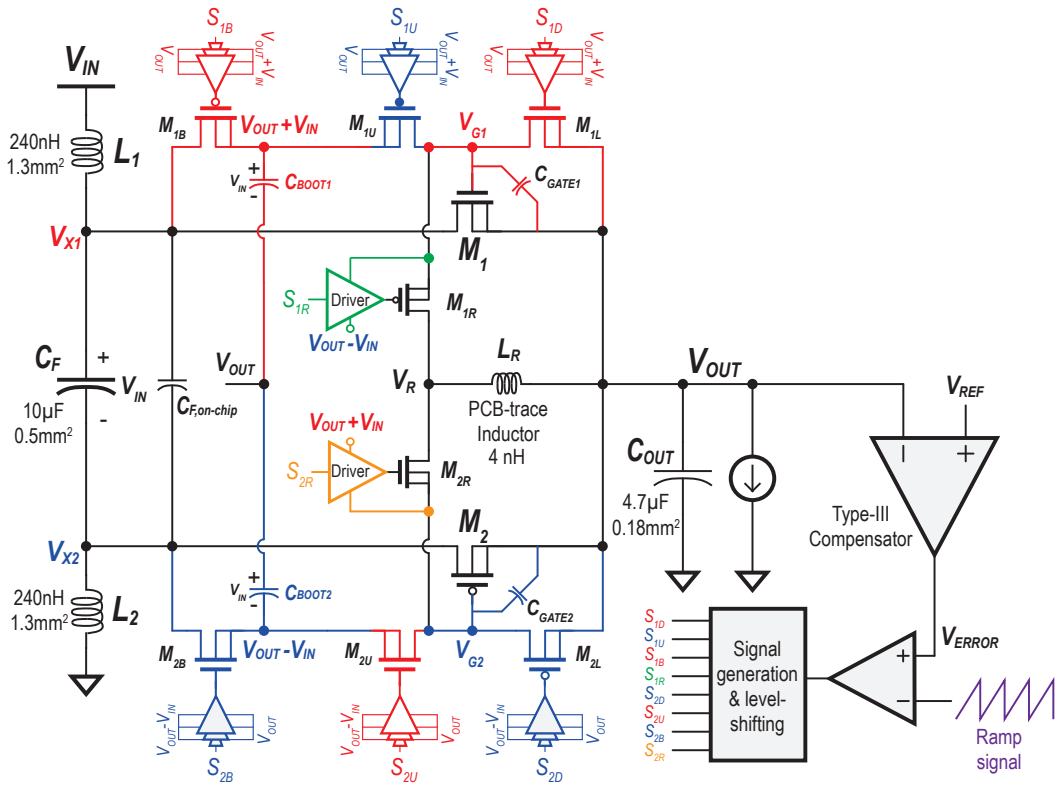


Figure 3.13: Full schematic of the proposed charge-recycling inductor-first buck converter.

cally, a minimum rise/fall time is needed anyway for the gate signals to prevent ringing at the switching nodes. Therefore, regardless of the load current value, activating the CR circuit always only ever reduces losses.

3.4 Circuit Implementation

Fig. 3.13 shows the converter full schematic. Small-size passive components were used for the power inductors and capacitors. The charge recycling inductor was realized using a PCB trace. A closed-loop controller with a type-III compensator was implemented which generates a PWM signal. The PWM signal is used to generate all the eight control signals for the normal and the recycling drivers.

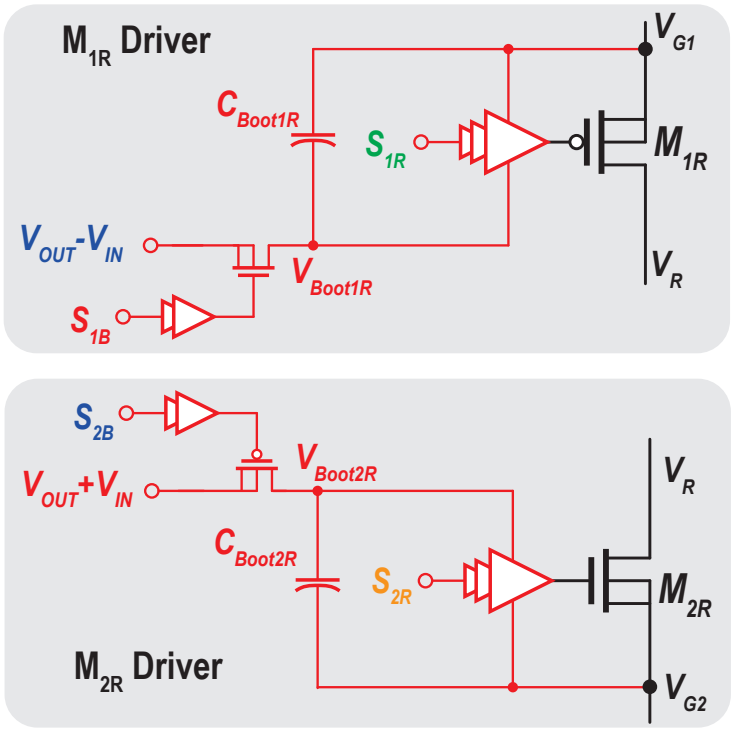


Figure 3.14: Implementation of the drivers for the charge recycling MOSFETs, M_{1R} and M_{2R}.

3.4.1 Drivers of Recycling MOSFETs

Driving the CR MOSFETs, M_{1R} and M_{2R} can be challenging due to the varying voltage at their source and drain terminals. When M_{1R} is activated to charge/discharge C_{GATE1}, it needs to bypass a voltage that varies between V_{OUT} and $(V_{OUT}+V_{IN})$ (i.e., a voltage swing of V_{IN}). Similarly, when M_{2R} is activated to charge/discharge C_{GATE2}, it needs to bypass a voltage that varies between V_{OUT} to $(V_{OUT}-V_{IN})$ with a total voltage swing of V_{IN}. M_{1R} and M_{2R} need to bypass these varying voltages while, at the same time, their on-resistance needs to be kept minimum in order to minimize the losses in the recycling loop. Fig. 3.14 shows the employed drivers, which have local bootstrapping capacitors connected to the gate terminals of the power MOSFETs (V_{G1} and V_{G2}) to generate the appropriate internal flying rails. By using these drivers, several benefits are achieved. First, the CR MOSFETs are implemented using the core 1.8 V MOSEFETs of the employed technology although they are bypassing large varying voltages. Second,

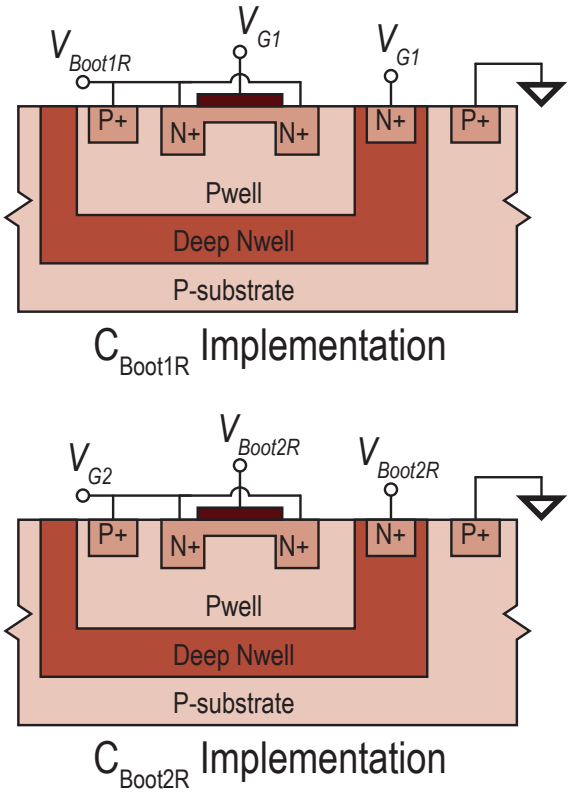


Figure 3.15: Cross-section of the recycling bootstrapping capacitors implemented in deep N-well.

the CR MOSFETs are always driven with the maximum overdrive voltage (i.e., V_{IN}), minimizing the losses in the recycling loop even when bypassing a varying voltage with a V_{IN} swing. Third, the CR MOSFETs are completely driven from the converter internal nodes with no need for external supplies to drive them.

3.4.2 Control Signal Generation

To generate the eight signals required for controlling the eight driver MOSFETs and to ensure appropriate timing for the control signals, two PWM-input delay lines are formed. The delayed versions of the PWM signal work as triggers for SR registers to generate the control signals for the drivers. Selected delay cells are configurable to control the duration of the CR pulses to best suit the value of the employed L_R. The eight control signals are level-shifted to the appropriate levels for the drivers by capacitively

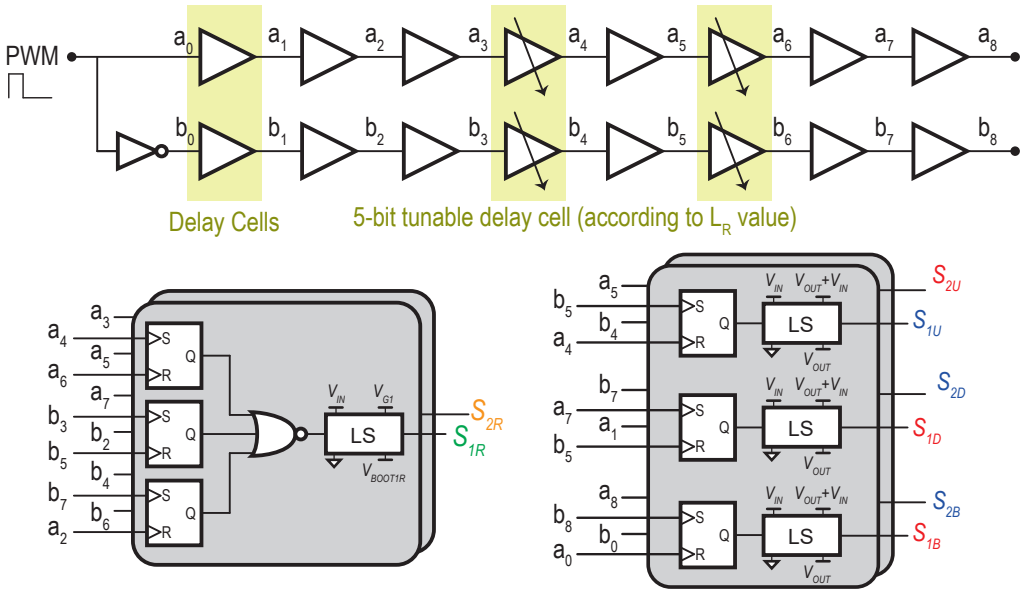


Figure 3.16: The control circuit used to generate the control signals for the normal drivers and the recycling drivers.

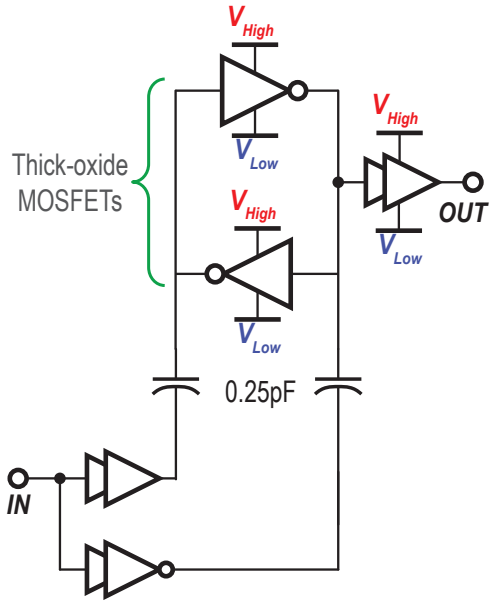


Figure 3.17: The schematic of the level shifter used for all the control signals where V_{HIGH} and V_{LOW} are always connected to the converter internal nodes.

coupling into flying-domain latches as shown in Fig. 3.17. It is worth mentioning that V_{HIGH} and V_{LOW} in all of these needed level shifters are self-generated from the

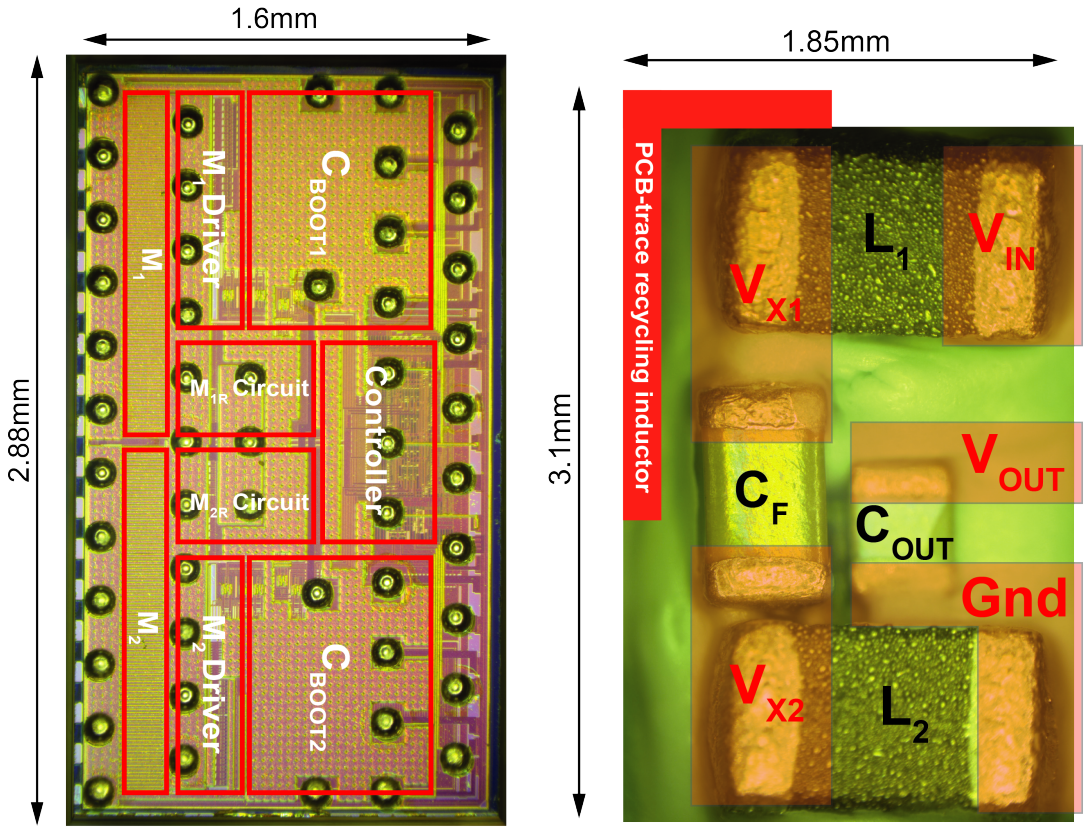


Figure 3.18: (a) Micrograph of the fabricated converter chip assembled on one interposer side. (b) The other side of the interposer showing the assembled passives including a PCB-trace charge-recycling inductor.

converter internal nodes without the need for any additional external supplies.

3.5 Measurement Results

The PMIC of the proposed converter, shown in Fig. 3.18 (a), was implemented in a 180 nm CMOS technology with a total area of 4.6 mm^2. The PMIC was flip-chip bonded to an interposer where the passives (C_F = 10 μF, $L_{1,2}$ = 240 nH, C_{OUT} = 4.7 μF) are mounted on the backside, as shown in Fig. 3.18 (b). The total converter area, including all routing and the 4 nH PCB-trace recycling inductor, occupies 5.7mm^2.

When switched at 3 MHz, measurement results of efficiency versus load current

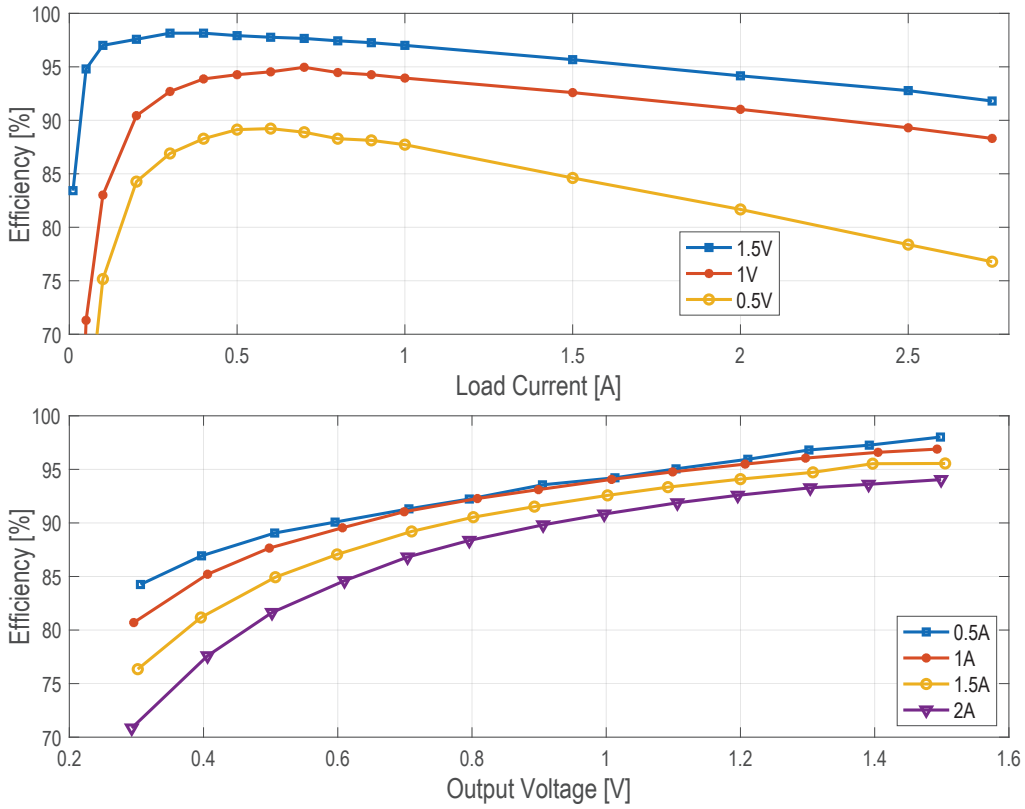


Figure 3.19: Measured efficiency curves versus load current and output voltage.

(I_{LOAD}) in Fig. 3.19 reveal measured peak efficiencies of 98.2%, 95%, and 89.2% for V_{OUT} = 1.5, 1, and 0.5 V, respectively. The converter has a high peak power density of 0.72 W/mm^2 (or 0.4 W/mm^3) achieved at an efficiency of 91.8%. Thanks to the CR technique, the converter achieves a high measured peak efficiency of 88.4% even at 1% of the maximum load current (I_{LOAD}). Fig. 3.19 also shows the measured efficiency versus (V_{OUT}) at different load currents where a peak efficiency of 95% is achieved at V_{OUT} = 1 V, and a peak efficiency of 89% is achieved at V_{OUT} as low as 0.5 V.

Fig. 3.20 illustrates that the nodes $V_{X1,2}$ switch as expected where for a V_{IN} of 1.8 V and a V_{OUT} of 1 V, V_{X1} is switching between 1 V and 2.8 V, and V_{X2} is switching between -0.8 V and 1 V. Fig. 3.21 shows the CR transistors turning on and off during a switching cycle where, at the positive edge of the PWM signal, the recycling switch, S_{2R}, is activated to discharge the gate capacitance of the power MOSFET M_2,

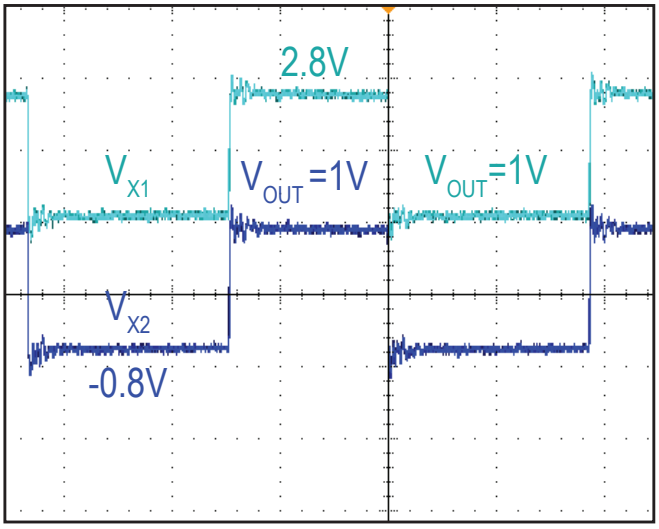


Figure 3.20: Measured steady-state waveform of the internal switching nodes of V_{X1} and V_{X2}.

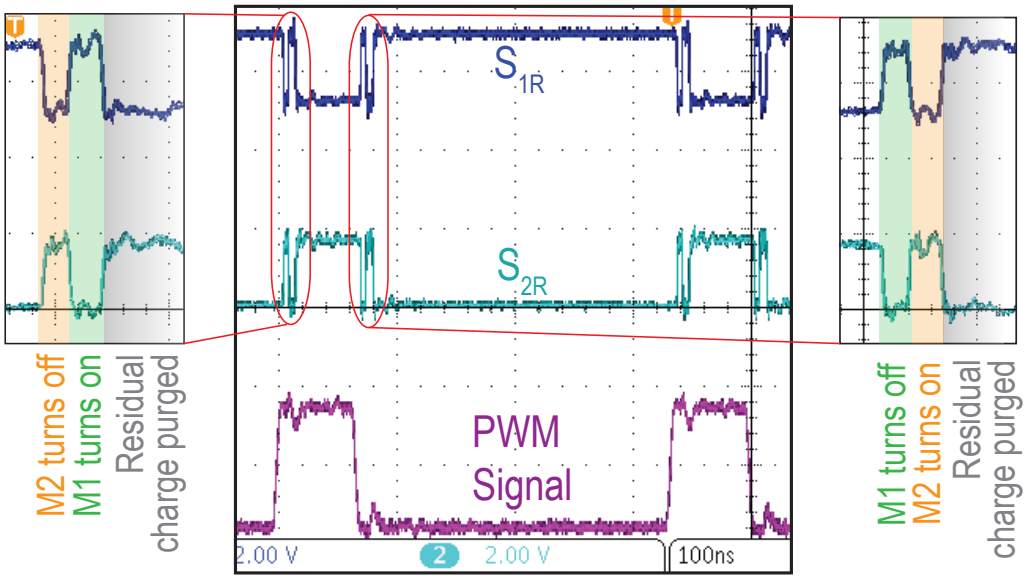


Figure 3.21: Measured waveform of the S_{1R} and S_{2R} signals controlling the charge recycling transistors.

then the other recycling switch, S_{1R}, is activated to charge the gate capacitance of the power MOSFET M_1 and turn it ON. Similarly, at the negative edge of the PWM signal, the recycling switches, S_{1R} and S_{2R}, are activated in a reversed sequence to first turn M_1 off, and then turn M_2 ON. Fig.3.22 shows the measured load step response of the

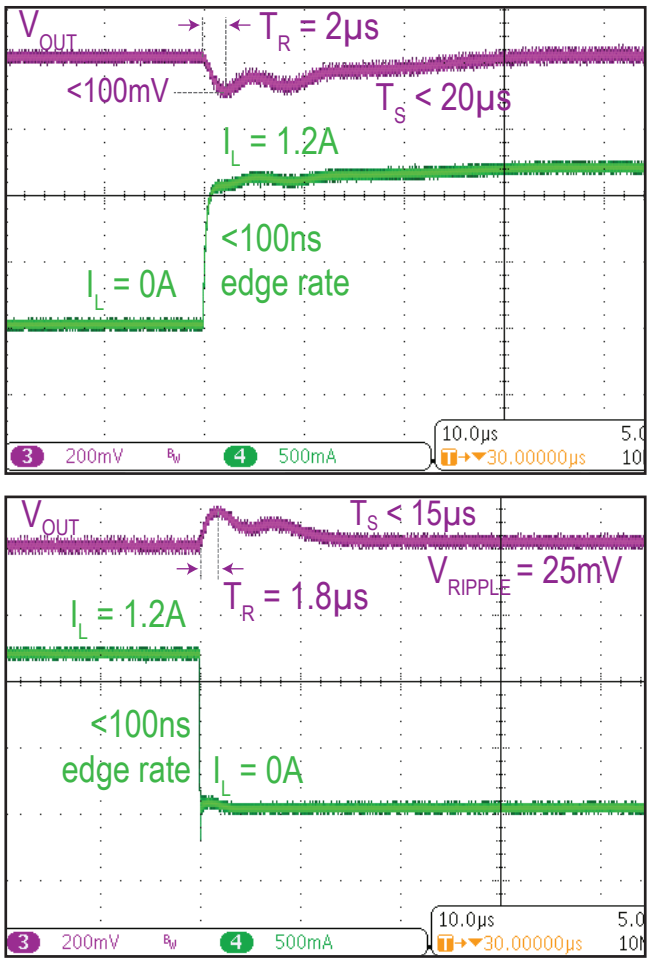


Figure 3.22: Measured waveforms of the closed-loop control load step response.

converter with ΔI_L = 1.2 A in <100 ns reveal a response and settling time of <2 and <20 μs, respectively, demonstrating that the CR technique does not impact the control of the circuit.

Table 3.1 summarizes the performance in comparison to prior-art CR converters, along with converters that mostly operate with similar input/output voltage ranges over continuous conversion ratios. Unlike most of the previous work, the inductor-first buck converter has a continuous input current resulting in significantly lower noise and EMI at the input voltage. The proposed CR technique helps achieve state-of-the-art efficiency, light load efficiency, and competitive power density.

Table 3.1: Comparison to prior-art converters that offer continuous conversion ratios across SoC-compatible voltages.

	Mulligan ISSCC'07	Kim JSSC'15	Jia JSSC'18	TPS8268150	C. Schaef ISSCC'19	Abdulslam ISSCC'19	This Work
Topology	Buck	Buck	Buck	Buck	Buck	Hybrid (PS3B)	**Hybrid (PS3B)**
Charge Recycling?	YES	NO	YES	NO	NO	NO	**YES**
Technology	500nm	65nm	65nm	N.R.	14nm	180nm	**180nm**
Passives	External	External	Integrated	External	In-package	External	**External**
Input Voltage [V]	3.6	1.8	1.1	2.3 - 5.5	1.6	1.8	**1.8**
Output Voltage [V]	1 – 1.8	0.6 – 1.5	0.3 – 0.86	1.5	1.2	0.5 – 1.5	**0.3 – 1.5**
I_{LOAD} (MAX) [A]	1	0.6	0.04	1.6	0.5	2.5	**2.75**
Input Current	Pulsed	Pulsed	Pulsed	Pulsed	Pulsed	Continuous	**Continuous**
PMIC Area [mm^2]	5.3	5	0.13	N.R.	2.16	1.85	**4.6**
Total Footprint [mm^2]	N.R.	5	0.13	6.67	2.16	5	**5.7**
Peak Efficiency (PE)	89.1%	95.5%	73%	88%**	88%	94%	**98.2%**
Efficiency @ 10% of MAX I_{LOAD}	88%**	95%**	N.R.	87%**	82%**	90%	**98%**
Efficiency @ 1% of MAX I_{LOAD}	66%**	N.R.	N.R.	65%**	72%	N.R.	**88.4%**
Power Density @ PE * [W/mm^2]	N.R.	0.03**	N.R.	0.045**	0.28	0.18	**0.11**
Peak Power Density (PPD) * [W/mm^2]	N.R.	0.17	0.27	0.36**	0.28	0.7	**0.72**
Efficiency @ PPD (OR @MAX I_{LOAD})	N.R.	88%	N.R.	74%**	88%	86.6%	**91.8%**

N.R. – Not Reported
* Nominally computed by the total converter footprint including the passives and the area necessary to route to them
** Estimated from measurement results

3.6 Conclusion

In this work, it was demonstrated that a pragmatic charge recycling of the gate charges of the power MOSFETs can be achieved with recycling efficiencies of up to 80%. The charge recycling technique was applied to an inductor-first buck converter without affecting the circuit control law or the output regulation. A prototype for this technique achieves a state-of-the-art peak efficiency of 98.2% and a power density of 0.72W/mm^2. Thanks to the recycling technique, the efficiency is generally improved over a wide range of load currents, and specially at light load currents with still 88.4% efficiency even at 1% of the maximum load current.

3.7 Acknowledgement

Chapter 3 is based on and mostly a reprint of the following publications:

- A. Abdulslam and P. P. Mercier, "A 98.2%-Efficiency Reciprocal Direct Charge Recycling Inductor-First DC-DC Converter," *IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, 2021.

The dissertation author is the primary investigator and author of the work in these papers.

Chapter 4

A Symmetric Modified Multilevel Ladder DC-DC Converter for Battery-Connected Applications

4.1 Introduction

Most modern mobile, wearable, and Internet of Things (IoT) devices are powered from Li-ion batteries that operate between $\sim 3-5$ V. However, the system-on-chips (SoCs) that are powered in such systems are typically implemented in a scaled CMOS process that operate at $\lessapprox 1.2$ V, even perhaps down to 0.3 V for some ultra-low-power processors or memory units. The inherent voltage discrepancy between the battery and the SoC requires a power management integrated circuit (PMIC) that can provide continuous conversion ratios between $3\times$ and $16.7\times$ as depicted in Fig. 4.1.

Ideally, this DC-DC converter should both be efficient in order to maximize battery lifetime, and also small in order to minimize device volume. Unfortunately, for a given topology and packaging technology, there is typically a direct trade-off between efficiency and power density [37]. To make matters worse, the overall performance of a DC-DC converter tends to degrade as the conversion ratio increases as illustrated in Fig. 4.1, making achievement of an acceptable trade-off point for a Li-ion-to-SoC DC-DC converter more difficult.

Unfortunately, most deep sub-micron CMOS technologies do not support transistors with sufficiently high voltage ratings to natively process Li-ion battery voltages.

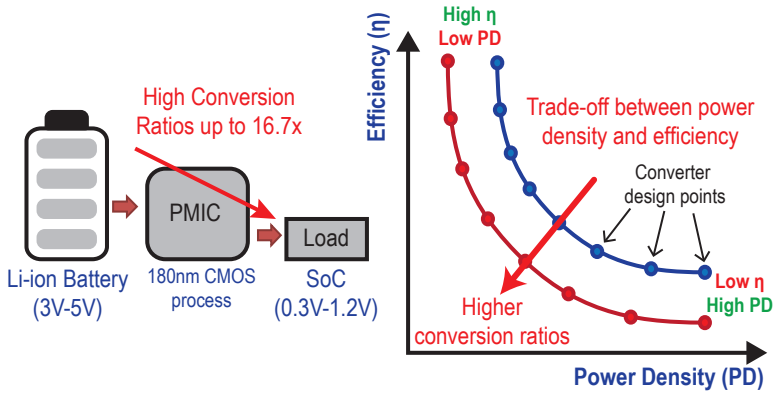


Figure 4.1: High conversion ratios and high-voltage MOSFETs are required when powering an SoC directly from a Li-ion battery, and worsen the trade-off between efficiency and power density.

This means that a conventional buck converter cannot be implemented directly without special process options. Instead, low-voltage transistors must be stacked on top of one another to help increase the effective blocking voltage capability [38–44]. However, doing so degrades the on resistance of the stack, while also introducing difficult design issues related to body-biasing, level-shifting, and the need to generate auxiliary supply rails.

Even if transistor stacking was possible without additional losses or complexity (or if high voltage transistors were available), a conventional buck converter requires a relatively large inductor to process power efficiently, leading to a relatively poor efficiency-power-density trade-off. To address this issue, prior work has suggested incorporating additional passive elements in the power-transfer process to create hybrid converters, which can potentially lead to an improved trade-off via reduced inductor size [6, 7, 12–24, 26]. In particular, flying-capacitor multi-level (FCML) converters exploit the need for stacked transistors to easily add flying capacitors that aid the power conversion process and reduce the overall implementation area [18–20]. However, such converters still suffer from poor conduction losses of the stacked switches, still require auxiliary supply rails to generate drive signals of the stacked switches, and require special capacitor charge balancing circuits [15, 16, 19, 47, 48].

This chapter describes a symmetric modified multilevel ladder (SMML) converter that helps address the conduction losses, capacitor balancing, and auxiliary rail needs of FCML converters through inherent topological properties, while providing state-of-the-art performance for a Li-ion-to-SoC voltage PMIC. These enhancements do not come for free, however, and trade-off with an increased number of capacitors and some internal charge sharing losses. The implemented converter was first described in [49]; this paper introduces more details and analysis to better understand the converter's operation and design optimization.

This chapter is organized as follows. Section II describes conventional buck and FCML solutions that build up towards the proposed SMML converter. Then, the basic operation and detailed analysis of the SMML topology are presented in Section III. Implementation details of a prototype converter are then described in Section VI, while measurement results and a comparison to previous work are presented in Section V followed by a discussion in Section IV.

4.2 Background

4.2.1 Conventional and Cascode Buck Converters

The most straightforward way to build a Li-ion-to-SoC DC-DC converter is via a conventional buck converter. Normally, a single power MOSFET is employed for the high-side switch, and a single power MOSFET is employed for the low-side switch as shown in Fig. 4.2(a). However, this basic converter topology comes with several challenges. First, the large conversion ratio required in Li-ion-to-SoC applications necessitates very low duty cycles for the V_X node (e.g., down to $\sim$5%). These low duty cycles result in smaller on-time/off-time of the switches which introduces difficult controller and driver design challenges that tend to introduce additional losses, especially when operating at relatively high switching frequencies. For low switching frequencies, small duty cycles might not be a limitation in Li-ion-to-SoC applications, but can be a

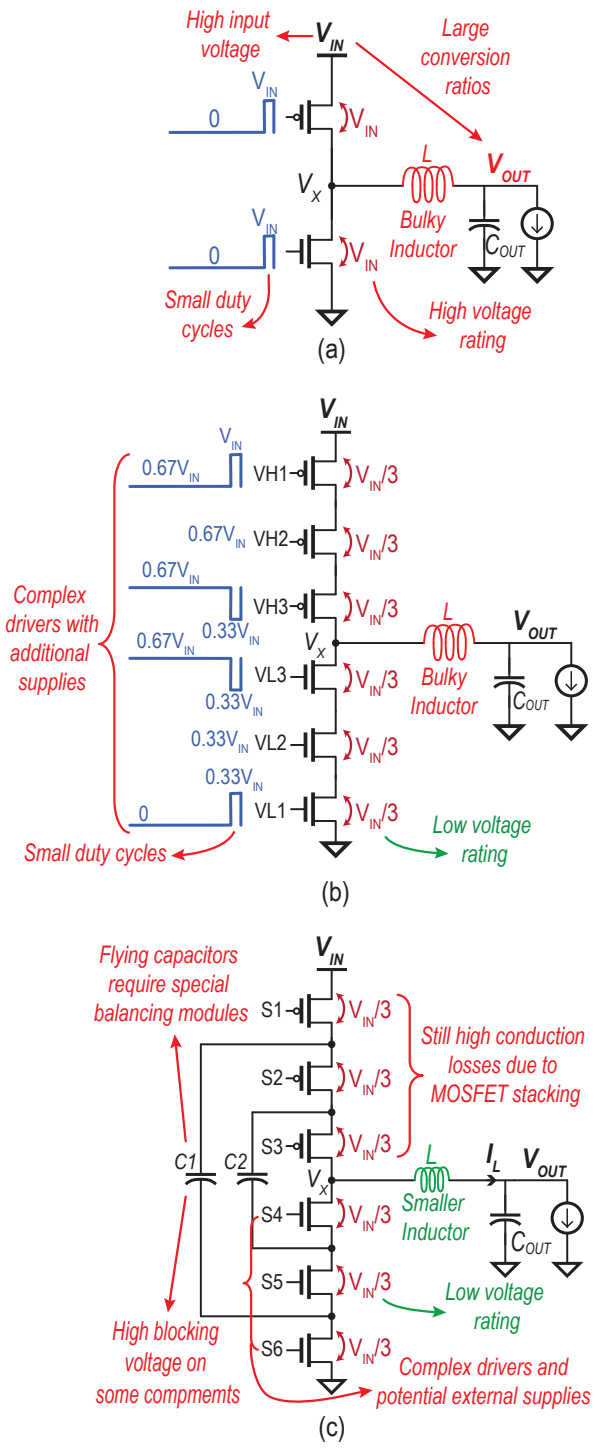


Figure 4.2: A conventional buck converter realized with (a) single high-voltage MOSFETs, and (b) cascoded low-voltage MOSFETs. (c) An FCML multilevel hybrid converter built upon the cascoded buck topology.

limitation in some other applications that require higher conversion ratios (e.g., 48V-to-1V conversion [26]). Second, each power MOSFET is required to block a high voltage equal to the entire Li-ion battery voltage. Unfortunately, high voltage MOSFETs are typically not available in modern CMOS technologies, and even in processes where they are, they tend to have worse characteristics than lower voltage rating MOSFETs. However, it should be noted that some modern technologies like BCD technologies can offer transistors of relatively high voltage (e.g., 5V), yet still of good characteristics, which can be a good option if using standard CMOS technologies is not required. The third (and most important) challenge will be discussed shortly.

In order to overcome the first two challenges, cascode buck converters with multiple stacked MOSFETs for both the low-side and the high-side switches have been proposed in prior art [38–44]. In the example shown in Fig. 4.2(b), three stacked MOSFETs are used to realize each of the two switches, where each MOSFET blocks only one third the input voltage, thereby allowing use of readily available low voltage rating MOSFETs that typically have better performance than their larger thicker-oxide counterparts. For example, it has been shown that using cascoded low-voltage devices can result in lower switching losses due to the reduced voltage swing at the gate of each single MOSFET [44].

Although the cascoded switches arrangement does enable implementation of Li-ion-to-SoC converters in scaled CMOS processes, stacking devices comes with several additional challenges. For example, the driving scheme of the power MOSFETs becomes much more complicated than that of a conventional buck converter, as each transistor requires its own specialized switching signal at non-standard voltages to ensure that each transistor is never voltage overstressed. In the 3-stacked-MOSFET cascode converter example shown in Fig. 4.2(b), additional supplies of $0.33V_{IN}$ and $0.67V_{IN}$ are required to drive the power MOSFETs. Although these voltages might be available at the converter internal nodes when the power MOSFETs are turned off, these internal nodes are usually of high impedance and cannot be used as an internal supply for the drivers. It thus turns out that generating these additional voltage levels for the drivers

is not a straightforward process and requires additional overhead circuits and possibly other auxiliary DC-DC converters [39–41]. Additionally, cascode buck converters still require operation at very small duty cycles in order to provide high conversion ratios, just like a conventional buck converter.

The third challenge that is faced by both the conventional and cascoded buck converter relates to the size of the inductor. The basic buck structure relies exclusively on the inductor to process and condition power, which necessitates a large inductor to achieve high efficiency, resulting in a difficult efficiency-power-density trade-off. For example, reducing the inductance value would require a high switching frequency and/or a higher current ripple, which would eventually increase the converter losses. Shrinking the inductor size without decreasing its inductance value would result in higher DC resistance which again would result in more conduction losses. As a result, the inductor remains as the bottleneck in relaxing the trade-off between efficiency and power density in these converters.

4.2.2 Hybrid and Multilevel Converters

The key to reduce the size of the inductor in Li-ion-to-SoC converter applications is to include other passive elements in the power transfer process, for example by building a hybrid converter. Perhaps the most straightforward way to do this is to build directly upon the cascoded-device buck converter: if the MOSFETs are going to be stacked anyway, it is beneficial to exploit the internal nodes between the transistors by installing some flying capacitors between them, as depicted in Fig. 4.2, which enables some extra features in the converter. The resulting FCML topology can be constructed as a three-level [14–17], four-level [18, 19], modified four-level [24], or even as a higher level topology [20]. Other SC converters that satisfy certain topological conditions can also be used to build a multilevel converter, for example the series-parallel [21, 22] or Dickson topologies [23, 26].

The structure shown in Fig. 4.2(c) is a four-level FCML converter, where two fly-

ing capacitors are added to the cascode buck converter of Fig. 4.2(b). In this case, when operating in the lowest-voltage region, the inductor switching node, V_X is switched between $0.33V_{IN}$ and zero instead of V_{IN} and zero. This lower voltage swing at the switching node results in smaller current ripple in the inductor as compared to a conventional buck converter. Additionally, the effective switching frequency of the inductor can be higher than the switching frequency of the switches, resulting in savings in the MOSFET switching losses without decreasing the switching frequency of the inductor. These features can be translated into lower conduction losses or a smaller inductor, along with reduced switching losses. It should be noted that although multilevel converters utilize additional capacitors as compared to buck converters, capacitors are usually not bulky like inductors, and have a lower impact on the converter volume, resulting in an overall higher power density [52].

Importantly, the required duty cycle of the V_X node in a multilevel converter is more relaxed (i.e., the same output voltage can be provided by a larger duty cycle) than in a conventional buck converter when both converters have the same V_X switching frequency. This larger duty cycle in multilevel converters is mainly because the voltage swing at the switching node (V_X) is reduced. For example, in a 4-level converter operating in the lowest-voltage region, V_X switches between $0.33V_{IN}$ and zero. In this case, the duty cycle (D) of the V_X node for a desired output voltage (V_{OUT}) at an input voltage of (V_{IN}) is given by:

$$D = 3 \times \frac{V_{OUT}}{V_{IN}}. \tag{4.1}$$

Therefore, a four-level converter can give the same output voltage at a $3\times$ larger duty cycle for the V_X node than a conventional buck converter for the same V_X switching frequency. This translates to larger on-time/off-time of the switches, allowing the four-level converter to effectively operate at larger conversion ratios than conventional buck converters.

Despite these features, conventional multilevel converters, like the FCML converter, suffer from one or more of the following limitations. They still have relatively

high conduction losses due to the multiple switches stacked in series. For example, in the four-level FCML converter shown in Fig. 4.2(c), three MOSFETs are stacked in series in each phase of operation, resulting in relatively high conduction losses. Moreover, due to having multiple MOSFETs that are not referenced to ground or V_{IN}, the driving scheme in most multilevel converters is very complex, with the possible need for external power supplies for the drivers and/or the level shifters [23, 24].

Additionally, having the flying capacitors balanced at the correct voltages is very crucial for correct and efficient operation of multilevel converters [45, 46]. Since the voltage on these capacitors is not always enforced at a certain value as in SC converters, the flying capacitors in multilevel converters need some special balancing modules to ensure their stability at the correct voltages resulting in more control overhead [19, 47, 48].

Finally, multilevel converters can have voltage rating limitations. In an N-level multilevel converter, the minimum voltage rating on any component is usually equal to V_{IN}/N. However, in some multilevel converters, the voltage rating of some switches/-capacitors exceeds this minimum voltage rating which requires additional stacking of switches and/or increased implementation area/size of the capacitors. For example, in the four-level FCML, the voltage on one of the flying capacitors is equal to $0.67V_{IN}$, which exceeds the $0.33V_{IN}$ minimum. If that capacitor were implemented on-chip, this may require capacitor stacking, and thus a $4\times$ capacitor area increase. A modified four-level topology suitable for on-chip implementations was introduced in [24].

All of these issues limit the direct pragmatic adoption of multilevel converters in practical applications, and extra engineering effort is required to get them to work efficiently and reliably. For example, there are several recently published multilevel converters that have attempted to address one or more of these challenges [21–24, 26].

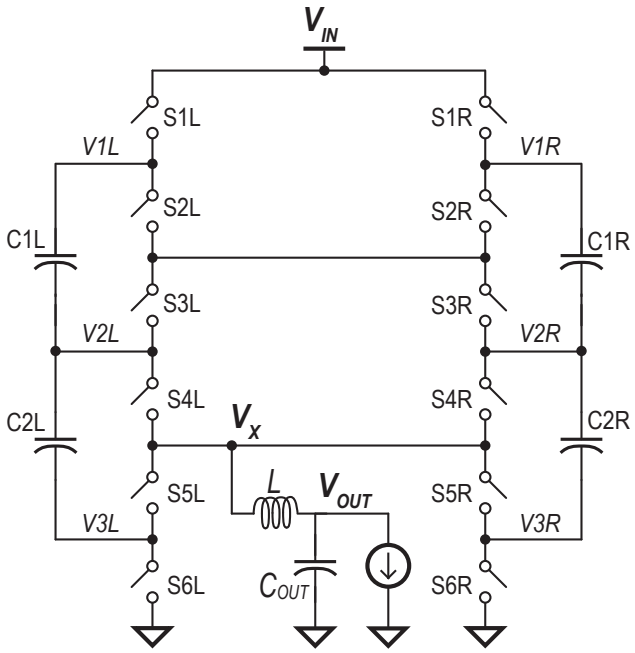


Figure 4.3: Schematic of the proposed symmetric modified multilevel ladder (SMML) converter.

4.3 Symmetric Modified Multilevel Converter

Instead of engineering switches, control structures, and auxiliary DC-DC converters to address the conduction losses, capacitor balancing, and driver supply rail issues in conventional FCML converters, this chapter describes a symmetric modified multilevel ladder (SMML) converter that inherently addresses these issues through the topology itself.

The proposed SMML converter is shown in Fig. 4.3. It is built based on a modified symmetric ladder SC topology, and consists of two sides, each with two capacitors and six switches, with an inductor connected in series with the combined output.

Beneficially, the SMML converter can mitigate the relatively high conduction losses due to the stacked MOSFETs via the inherent two-phase operation where current is supplied from both the input rails in each phase. The SMML converter also has minimum voltage ratings on all switches and capacitors (specifically, $0.33V_{IN}$). The flying capacitors in the SMML converter are naturally balanced at their correct voltages with

no need for any balancing modules, though it should be noted that charge sharing losses occur as a result (fortunately with minimal impact on efficiency for a well-engineered design). Additionally, the drivers and the level shifters in the SMML converter are completely driven by internal rails that are generated with minimal overhead circuits. With all that said, it is worth mentioning that the implementation techniques described in this chapter are well-presented in the SMML topology, but are not limited to this topology and can potentially be applied to other multilevel topologies as well. The operation of the SMML converter, along with a detailed explanation of each of these features, will be discussed in the following subsections.

4.3.1 Basic Operation

The converter operates in a sequence of four phases, illustrated in Fig. 4.4, that naturally balance the four flying capacitors to $0.33V_{IN}$. In phase Φ_1, the positive terminal of C1L is connected to V_{IN}, while the negative terminal of C2R is connected to ground. In this case, C1L and C2L are charging, C1R and C2R are discharging, and the V_X node has a voltage of $0.33V_{IN}$. Phase Φ_3 is similar to Φ_1, but with the positive terminal of C1R connected to V_{IN} and the negative terminal of C2L connected to ground. In this case, C1R and C2R are charging, C1L and C2L are discharging, and V_X is also connected to $0.33V_{IN}$. In phase Φ_2 and Φ_4, V_X is connected to ground by turning on switches S5L, S6L, S5R and S6R, while the flying capacitors are kept idle. Under normal operation, the V_X node is switching between $0.33V_{IN}$ and zero by going through the following repeating sequence of phases: Φ_1 followed by Φ_2, then Φ_3 and then Φ_4, with a duty cycle between these phases according to the desired output voltage as shown in Fig. 4.4.

From the waveforms of the converter's internal switching nodes, shown in Fig. 4.4, it can be noted that the blocking voltage of all the MOSFETs and capacitors does not exceed $0.33V_{IN}$, which is the minimum possible voltage rating for a 4-level topology. This minimal voltage rating on the switches and the capacitors would help in keeping

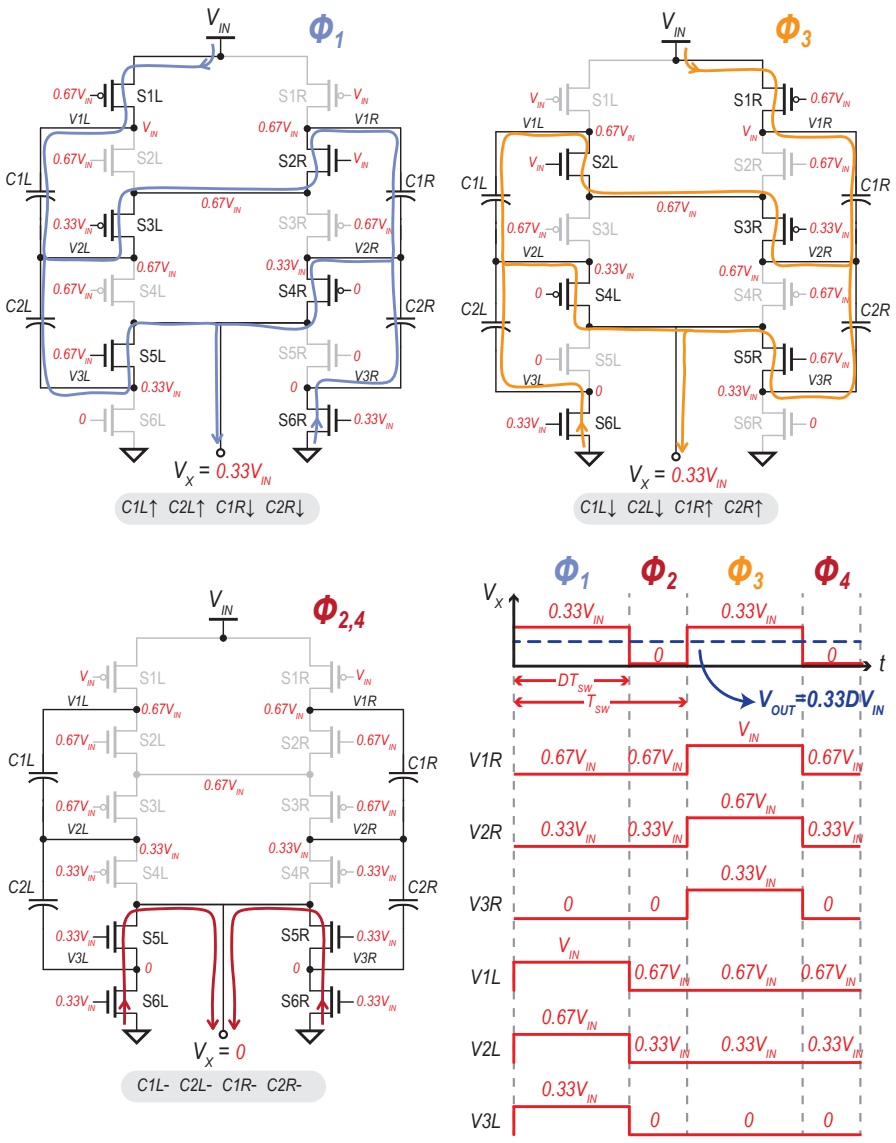


Figure 4.4: Operating phases of the Symmetric Modified Multilevel Ladder (SMML) converter.

their implementation area/losses at minimum. For a V_{IN} up to 5 V and when using the 1.8 V core MOSFETs in the employed 180 nm CMOS technology, no stacking of MOSFETs for any of the switches is required.

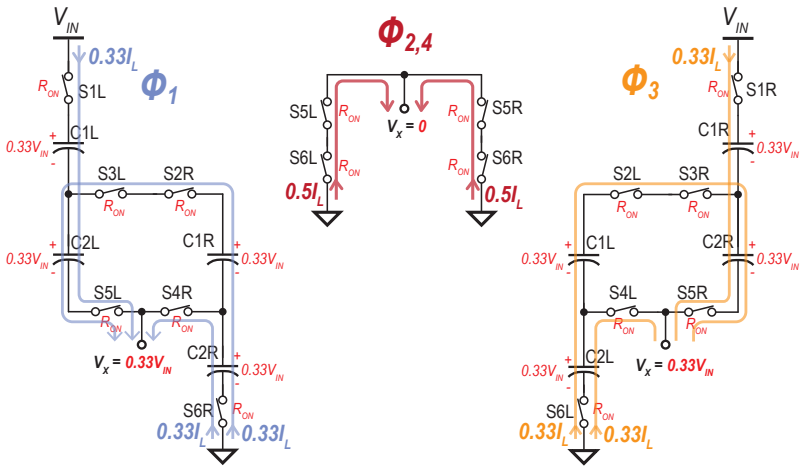


Figure 4.5: The equivalent circuit and the average current paths in each operating phase.

4.3.2 Capacitor Stability and Internal Charge Sharing

In Φ_1 and Φ_3, the four flying capacitors are involved in the power conversion process. As depicted in Fig. 4.5, there are three current paths that go through these capacitors to deliver charge to the output. Under steady state operation, C1L and C1R are being charged/discharged with an average current of $0.33I_L$, while C2L and C2R are being charged/discharged with an average current of $0.67I_L$, as shown in Fig. 4.5. Since the average charging and subsequent discharging current for each flying capacitor is ideally the same between phases, all flying capacitors should remain balanced. This is in contrast to most other multilevel converters, where discrepancies in the phases duration and/or the charging/discharging current can result in an improperly balanced flying capacitors, thereby necessitating flying capacitor balancing modules [45]. However, in the SMML converter, it can be noted that in each of the phases $\Phi 1$ and Φ_3, three flying capacitors are stacked in series between V_{IN} and ground with the fourth capacitor shorted to the middle capacitor. This stacking of capacitors in the two phases forces the average voltage on each of the flying capacitors to be $0.33V_{IN}$, allowing the flying capacitors to be naturally balanced without the need for any balancing modules.

It can be noted, however, that connecting the fourth capacitor to the middle capacitor can result in direct charge-sharing losses if their voltages are different at the

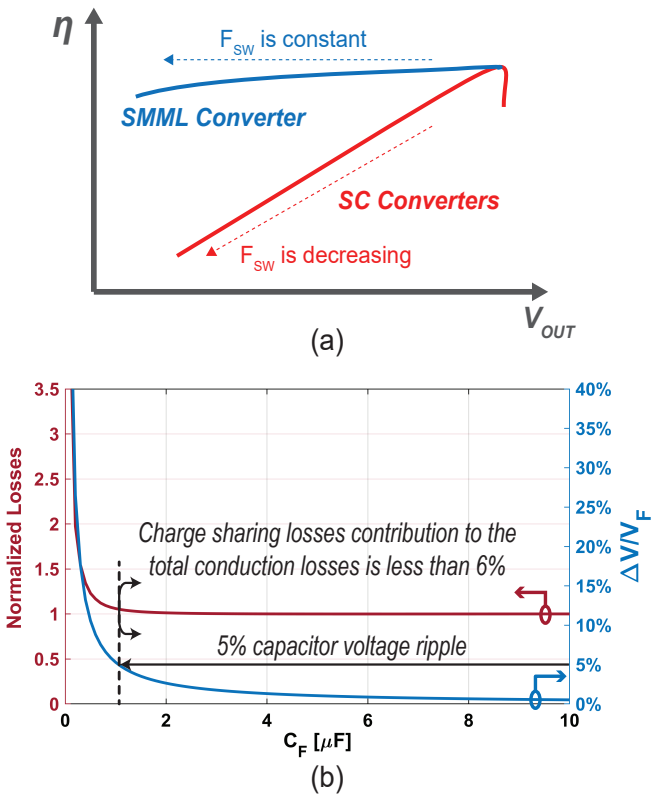


Figure 4.6: (a) A Comparison between the V_{OUT} regulation technique in the SMML converter and in SC converters. (b) Simulated internal charge sharing losses in the SMML converter versus the flying capacitor size (C_F).

start of each phase (voltage difference given by ΔV). Fortunately, the internal charge sharing loss in the SMML converter, and in multilevel converters in general, are not typically as significant as in conventional SC converters due to several reasons. First, in SC converters, the main charge sharing loss occurs between the flying capacitors and the output capacitor. However, in multilevel converters, there is an inductor between the flying capacitors and the output capacitor that converts this hard-charging process to a soft-charging process. Second, in SC converters, regulation of output voltage, V_{OUT}, is usually accomplished by changing the switching frequency, F_{SW}, where the capacitor ΔV and hence the charge sharing losses increase when decreasing F_{SW} as shown in Fig. 4.6 (a). On the other hand, V_{OUT} regulation in multilevel converters is done using a PWM control scheme where F_{SW} remains almost constant, and hence ΔV between the capacitors ideally does not increase when regulating V_{OUT} and can be designed to

be low across operating conditions. Third, as a design consideration in multilevel converters, ΔV on capacitors should be limited anyway by using reasonably large enough flying capacitors in order not to overstress the low-voltage power MOSFETs.

To illustrate the effect of internal charge sharing on the total conduction losses of the converter, Fig. 4.6 (b) shows simulation results for the normalized conduction losses of the SMML converter versus the flying capacitor size, which is directly related to the charge sharing losses, especially when operating at high load currents. If reasonably sized capacitors are used to limit ΔV on capacitors to be less than 5% in order not to overstress the switches by large voltage swings, the internal charge sharing loss is less than 6% of the total conduction losses and therefore is negligible compared to other types of losses like the MOSFET losses and the inductor losses.

If the physical size of the flying capacitor sizes is limited and/or the total internal charge sharing losses are not satisfactory for a given design, the internal charge sharing losses can be further reduced by a coarse dead-time management techniques, where the turn on time of switches S2R and S2L is delayed so that the capacitor voltages become closer before turning on the switches, similar to the split-phase technique used in [50]. However, this technique has to be applied carefully since a very large dead-time can lead to more conduction losses because one of the current paths is cut during this dead-time of S2R and S2L as can be noted in Fig. 4.5. It is also worth mentioning that a capacitor mismatch between the two converter sides has no effect on the flying capacitor stability since the capacitors are forced to their nominal voltage regardless of the individual capacitance value.

4.3.3 Equivalent On-resistance

The SMML converter has reduced equivalent on-resistance compared to a baseline FCML design due to inherent phase interleaving between the two sides of the converter where multiple parallel current paths from both the input rails provide charges to the output, thereby reducing the conduction losses of the converter. For example, in Φ_1

and Φ_3, one current path of an average value of $0.33I_L$ from V_{IN} and two similar current paths from the ground rail deliver charges to the output. To calculate an equivalent on-resistance for the converter switches, all the switches are assumed to have the same on-resistance, R_{ON}, for simplicity. By taking into account the current percentage going through each switch, the total equivalent on-resistance can be calculated to be $1.33R_{ON}$ in each of the phases Φ_1 and Φ_3, and only R_{ON} in Φ_2 and Φ_4. The total equivalent on-resistance of the converter, in this case, is between $1 \times R_{ON}$ and $1.33 \times R_{ON}$ depending on the duty cycle.

To compare the total equivalent on-resistance of the SMML converter with that of the FCML converter, a same total area for the switches is allocated for both converters. In this case, the switches of the SMML converter will have a doubled on-resistance (i.e. $2R_{ON}$) as compared to the switches of the FCML converter since the SMML converter has 12 switches while the FCML converter has 6 switches. In this case, the SMML converter will have a total equivalent resistance between $2 \times R_{ON}$ and $2.67 \times R_{ON}$ depending on the duty cycle, while the FCML converter always has an equivalent on-resistance of $3 \times R_{ON}$ which is still higher than that of the SMML converter. Hence, the SMML converter can achieve a lower equivalent on-resistance than the FCML converter.

4.3.4 Converter Losses Modeling

The modeling of multilevel converters is typically quite complicated due to the relatively high number of components used in these converters and the multi-phase operation [24, 51, 52]. A simplified yet systematic method, inspired by the model developed for SC converters [5], is developed in this chapter to estimate the losses in the SMML converter. The dominant losses in the converter under normal operation are the MOSFET conduction losses, the MOSFET switching losses, the flying capacitor losses, and the inductor losses, which will all be modeled in the following subsections.

MOSFET Conduction Losses

When operating in the continuous conduction mode (CCM), the current ripple in the inductor is given by:

$$\Delta I = \frac{V_{IN}}{3} \frac{D(1-D)}{L \times F_{SW}} \tag{4.2}$$

where V_{IN} is the input voltage, D is the duty cycle, L is the inductor value, and F_{SW} is the switching frequency of the V_X waveform (which is not necessarily the switching frequency of the individual MOSFETs). The $\frac{1}{3}$ factor is due to the multilevel operation, which results in lower current ripple in the inductor.

In this case, the switch conduction losses in the SMML converter are given by:

$$P_{Cond} = \left(I_L^2 + \frac{\Delta I^2}{12} \right) \sum_{\substack{1 \le i \le 4 \\ 1 \le j \le 12}} a(i,j)^2 R_j \left(\frac{T_i}{T_t} \right) \tag{4.3}$$

where I_L represents the load current, R_j represents the on-resistance of switch S_j, T_i represents the time duration of the phase ϕ_i, and T_t represents the total duration of the four phases of the converter. Resistance R_j can be defined as ($W_j \times r_{ON}$), where W_j is the width of switch S_j and r_{ON} is the switch on-resistance per unit width. T_t represents the duration of one switching sequence (i.e., Φ_1, Φ_2, Φ_3 and then Φ_4), and is typically equal to twice the switching period of the inductor. The coefficient $a(i,j)$ represents the percentage of the inductor current going through switch S_j in phase ϕ_i. Each individual coefficient $a(i,j)$ is an element in a 4×12 matrix $\mathbf{A}$, where four represents the number of the SMML converter phases and twelve represents the number of the SMML switches, and is given by:

$$\mathbf{A} = \left[\begin{array}{cccccc|cccccc} \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{2}{3} & 0 & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{2}{3} \\ 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{2}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{2}{3} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} \end{array}\right]. \tag{4.4}$$

For example, the current going through switch S_3 in phase Φ_1 is $[a(1,3) \times I_{IND}]$, where $a(1,3)$ equals $\frac{1}{3}$ and I_{IND} is the inductor current.

When assuming that all the power MOSFETs have the same size (i.e., $R_j = R_{ON} = r_{ON}/W_j$, since all W_j's are equal) for simplicity, (4.3) can be reduced to:

$$\begin{aligned} P_{Cond} &= \left(I_L^2 + \frac{\Delta I^2}{12}\right)\left(\frac{4}{3}\frac{T_1}{T_t} + \frac{T_2}{T_t} + \frac{4}{3}\frac{T_3}{T_t} + \frac{T_4}{T_t}\right) R_{ON} \\ &= \left(I_L^2 + \frac{\Delta I^2}{12}\right)\left(1 + \frac{1}{3}D\right) R_{ON}. \end{aligned} \tag{4.5}$$

In this case, an effective total on-resistance of the MOSFETs in the SMML converter (R_{eff}) is given by:

$$R_{eff} = (1 + \frac{1}{3}D)R_{ON}. \tag{4.6}$$

This result agrees with the derivation done in the previous subsection. However, to get an optimum design, each MOSFET can be sized independently according to its conduction and switching losses.

MOSFET Switching Losses

MOSFET switching losses occur due to the charging/discharging of each MOSFET's parasitic capacitances: C_D, C_G, and C_J, which represents the drain-to-source, gate-to-source, and the junction parasitic capacitance, respectively. To represent these losses in a systematic way, characterizing matrices for the voltage on these parasitic capacitors are developed. When a MOSFET switch turns ON/OFF, its blocking voltage, V_D, changes from $0.33V_{IN}$ to zero or vice versa. This change in V_D results in the charging/discharging losses of C_D. V_D of each MOSFET can be represented in the following

matrix:

$$\mathbf{V_D} = \left[\begin{array}{cccccc|cccccc} 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 \\ \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 \end{array}\right] \tag{4.7}$$

Here, $\mathbf{V_D}$ is a 4×12 matrix where each element, $v_d(i,j)$, is the blocking voltage on switch (S_j) in phase (Φ_i), as a fraction of V_{IN}. When a MOSFET switch is ON, its corresponding $v_d(i,j)$ is zero.

Similarly, the gate-to source voltage or the overdrive voltage for a switching MOSFET changes from 0 to the maximum drive voltage or vice versa. In the employed SMML converter, the MOSFETs are driven directly from the converter internal nodes. Therefore, the overdrive voltage of the power MOSFETs is equal to $0.33V_{IN}$ when the MOSFET is ON and zero when the MOSFET is OFF. Since the blocking voltage of all the MOSFETs in the SMML converter is $0.33V_{IN}$, which is the same as the overdrive voltage value, the same matrix $\mathbf{V_D}$ can then be used to represent the MOSFET overdrive voltage in each phase where a V_D of zero means an overdrive voltage of $0.33V_{IN}$ for the corresponding switch, and vice versa.

Additionally, changes in the absolute value of the MOSFET source voltage results in charging/discharging of the parasitic junction capacitor, C_J, between the source terminal of a MOSFET and the chip bulk. A $\mathbf{V_S}$ matrix represents the MOSFET source voltage in each phase, as a fraction of V_{IN}, and can be given by:

$$\mathbf{V_S} = \left[\begin{array}{cccccc|cccccc} 1 & \frac{2}{3} & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 \\ 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 & 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 \\ 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 & 1 & \frac{2}{3} & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 \\ 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 & 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 \end{array}\right]. \tag{4.8}$$

By using the aforementioned matrices, the total switching loss of the MOSFETs

(P_{SW}) can be given by:

$$\begin{aligned} P_{SW} = 0.5V_{IN}^2 F_{SW} \sum_{\substack{1\le i\le 4\\ 1\le j\le 12}} \Delta v_d(i,j)^2 C_{D,j} \\ + 0.5V_{IN}^2 F_{SW} \sum_{\substack{1\le i\le 4\\ 1\le j\le 12}} \Delta v_d(i,j)^2 C_{G,j} \\ + 0.5V_{IN}^2 F_{SW} \sum_{\substack{1\le i\le 4\\ 1\le j\le 12}} \Delta v_s(i,j)^2 C_{J,j}, \end{aligned} \tag{4.9}$$

where $\Delta v_d(i,j)$ represents the difference between a MOSFET blocking voltage in the current phase (ϕ_i) and the MOSFET blocking voltage in the preceding phase (ϕ_{i-1}) (i.e., $v_d(i,j) - v_d(i-1,j)$), which is calculated using the $\mathbf{V_D}$ matrix. $\Delta v_d(i,j)$ will be zero if the switch remains ON or OFF when transitioning from ϕ_{i-1} to ϕ_i. Similarly, $\Delta v_s(i,j)$ represents the difference between the MOSFET source voltages when going from one phase to the next and is calculated using the $\mathbf{V_S}$ matrix. The parasitic capacitors $C_{D,j}$, $C_{G,j}$, and $C_{J,j}$ of a switch S_j are assumed to scale linearly with the switch width for simplicity.

Inductor and Capacitor Losses

The conduction loss in the inductor, which has a DC resistance of DCR, is given by:

$$P_{Inductor} = \left(I_L^2 + \frac{\Delta I^2}{12}\right) \times DCR. \tag{4.10}$$

The conduction loss due to the equivalent series resistance (ESR) of the flying capacitors is given by:

$$P_{Capacitor} = \left(I_L^2 + \frac{\Delta I^2}{12}\right) \sum_{\substack{1\le i\le 4\\ 1\le j\le 4}} (c_{i,j})^2 ESR_j \left(\frac{T_i}{T_t}\right), \tag{4.11}$$

where $c_{i,j}$ is an element of a 4-by-4 matrix, $\mathbf{C}$, that represents the percentage of the

inductor current going through each of the flying capacitors. $\mathbf{C}$ is given by:

$$\mathbf{C} = \begin{bmatrix} \frac{1}{3} & \frac{2}{3} & \frac{1}{3} & \frac{2}{3} \\ 0 & 0 & 0 & 0 \\ \frac{1}{3} & \frac{2}{3} & \frac{1}{3} & \frac{2}{3} \\ 0 & 0 & 0 & 0 \end{bmatrix}. \tag{4.12}$$

Total Losses

By combining the losses of the individual components, the total losses of the converter can be given by:

$$\begin{aligned} P_{Losses} = P_{Cond} + P_{SW} + P_{Inductor} \\ + P_{Capacitor} + P_{others}, \end{aligned} \tag{4.13}$$

where P_{others} includes other losses like the routing losses which can be significant if the PMIC is built on modern CMOS technologies that has limited routing or packaging resources. P_{Losses} represents the total losses of the converter at a given operating point and is a function of the switching frequency, F_{SW}, and switch sizes, W_j.

Optimization

To minimize the converter losses, the design parameters to be optimized are the switching frequency and the switch widths. If the switching frequency is predetermined according to some other design considerations, like the transient response and the output ripple, the switch widths are the only parameters to be optimized for minimum losses. Each of the 12 switches in the SMML topology has its corresponding conduction and switching losses, which are a function in the switch width, and are calculated as:

$$P_{switch,j} = \left(I_L^2 + \frac{\Delta I^2}{12} \right) \frac{\alpha}{W_j} + V_{IN}^2 F_{SW} W_j \beta. \tag{4.14}$$

α and β are two coefficients related to the conduction and the switching losses of each switch throughout the four phases, respectively, and are given by:

$$\begin{aligned}\alpha &= \sum_{1\leq i\leq 4} a(i,j)^2(\frac{T_i}{T_t})r_{ON} \\ \beta &= \sum_{1\leq i\leq 4} \left(\Delta v_d(i,j)^2 c_D + \Delta v_d(i,j)^2 c_G + \Delta v_s(i,j)^2 c_J\right),\end{aligned} \tag{4.15}$$

where r_{ON}, c_D, c_G, and c_J are the switch on-resistance, drain capacitance, gate capacitance, and junction capacitance, all per unit width. By differentiating the total switch losses with respect to the switch width W_j, and equating to zero, the optimum width for each MOSFET can be found as:

$$W_{opt,j} = \sqrt{\left(I_L^2 + \frac{\Delta I^2}{12}\right)\frac{1}{V_{IN}^2 F_{SW}}\frac{\alpha}{\beta}}, \tag{4.16}$$

where $W_{opt,j}$ is the optimum width of switch j at a given switching frequency and operating point (i.e. V_{OUT} and I_{LOAD}). If a comprehensive optimization of the converter that includes both the switching frequency and the switch sizes as design parameters is desired, the equations derived in this section can be used in an optimization process by the help of some analysis tools, for example, MATLAB.

4.4 Circuit Implementation

4.4.1 Power MOSFET Realization

In the employed 180 nm CMOS technology, each switch is realized with a 1.8 V core MOSFET and can be implemented as NMOS or PMOS. The required voltage swings across each switch, in conjunction with the corresponding gate switching voltages, are evaluated for minimized switching losses and driver complexity; the resulting implemented switch makeup is shown in Fig. 4.7 (a). It can be noted that S2L, S2R, S5L and S5R are NMOS power switches whose source terminal is not referenced to ground;

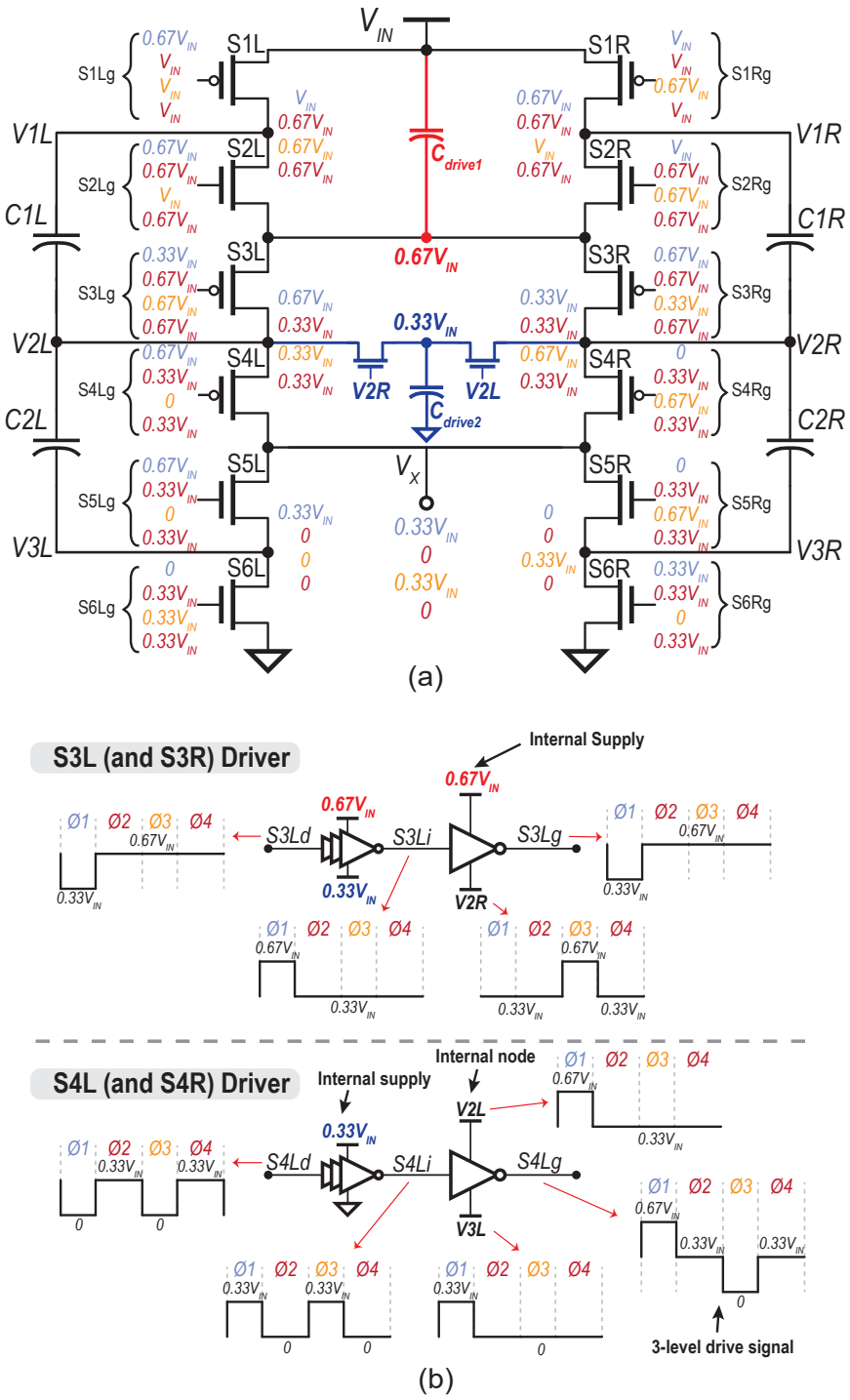


Figure 4.7: (a) Drive voltages for each power MOSFET in each phase, and the extra capacitors needed to capture the internal supply rails needed in the drivers. (b) A detailed schematic for the drivers of switches S3L and S4L.

as a result, they are implemented in deep n-well.

Fig. 4.7 (a) also shows the four gate voltage signals required to drive each power MOSFET in each of the four phases. By carefully inspecting the gate signals of each power MOSFET, it can be noted that non-standard voltage levels, e.g., $0.33V_{IN}$ and $0.67V_{IN}$, are required to drive the power MOSFETs. In addition, some of these MOSFETs, like S4L and S4R, dynamically require 3 different voltage levels. Fortunately, the internal nodes of the SMML converter can be exploited to generate these extra voltage levels and also to simplify the implementation of the MOSFET drivers.

4.4.2 Internal Generation of Driver Rails

Thanks to the complimentary feature between the two sides of the converter, the two voltage levels rails needed for MOSFET driving, namely $0.67V_{IN}$ and $0.33V_{IN}$, can be generated directly from the converter internal nodes.

Interestingly, the required $0.67V_{IN}$ voltage rail is already available at one internal node of the converter continuously through all phases as can be noted in Fig. 4.7 (a). A small bootstrapping capacitor, C_{drive1}, is thus placed between this node and V_{IN}, to stabilize the voltage on this node.

The other voltage level, $0.33V_{IN}$, is not directly available at one of the converter internal nodes continuously throughout all phases. However, this $0.33V_{IN}$ voltage level is available at the V2L and V2R internal nodes, but only in some phases. Therefore, two small MOSFETs and one decoupling capacitor (C_{drive2}) are used to capture the $0.33V_{IN}$ voltage level from these internal nodes. These two small MOSFETs are directly driven from the converter internal nodes V1L and V1R as shown in Fig. 4.7 (a), and thus no additional control signals are needed.

As a result of these small additions to the topology, the $0.33V_{IN}$ and $0.67V_{IN}$ required for the drivers and the level shifters are generated internally with minimum overhead, thereby omitting any need for external supplies or auxiliary DC-DC converters.

4.4.3 Switch Drivers

As noted in Fig. 4.7 (a), power switches S1L and S1R require a gate control signal switching between V_{IN} and $0.67V_{IN}$. To implement a gate driver that satisfies this condition, a set of cascaded inverters powered directly from V_{IN} as VDD and the internal $0.67V_{IN}$ node as VSS, are employed.

Next, it can be noted that the voltage levels of the gate control signal of switch S2L and switch S2R are the same as the converter internal nodes V1R and V1L, respectively. Therefore, these two internal nodes are used to drive S2L and S2R directly, and no explicit switch drivers are needed.

For the subsequent switches, S3L and S3R, it can be noted that they require control signals switching between $0.33V_{IN}$ and $0.67V_{IN}$. Like the top switches, cascaded drivers are used to drive S3L and S3R, but this time, the first driver stage is powered from the internal nodes V2R or V2L, not from the constant voltage $0.33V_{IN}$, as shown in the top of Fig. 4.7 (b), in order not to overload C_{drive2} and keep it small.

Next, switches S4L, S4R, S5L and S5R require 3-level gate drive signals that switch between $0.67V_{IN}$, $0.33V_{IN}$ and zero. Although these switches require the same 3-level gate drive signals, they are driven using separate control signals for dead-time consideration as depicted in Fig. 4.9 (to be discussed in more detail shortly). The 3-level driver for these power MOSFETs is implemented as shown in the bottom of Fig. 4.7 (b). The first stage in the cascaded inverters is powered from the internal nodes V2L (or V2R) and V3L (or V3R), while the remaining inverters are powered from $0.33V_{IN}$ and ground.

The full schematic of the implemented converter including the drivers is shown in Fig. 4.8. Parallel on-chip flying capacitors, implemented using MIM capacitors, are used to mitigate potential ringing on the driver lines since some of the drivers are powered from the converter internal nodes.

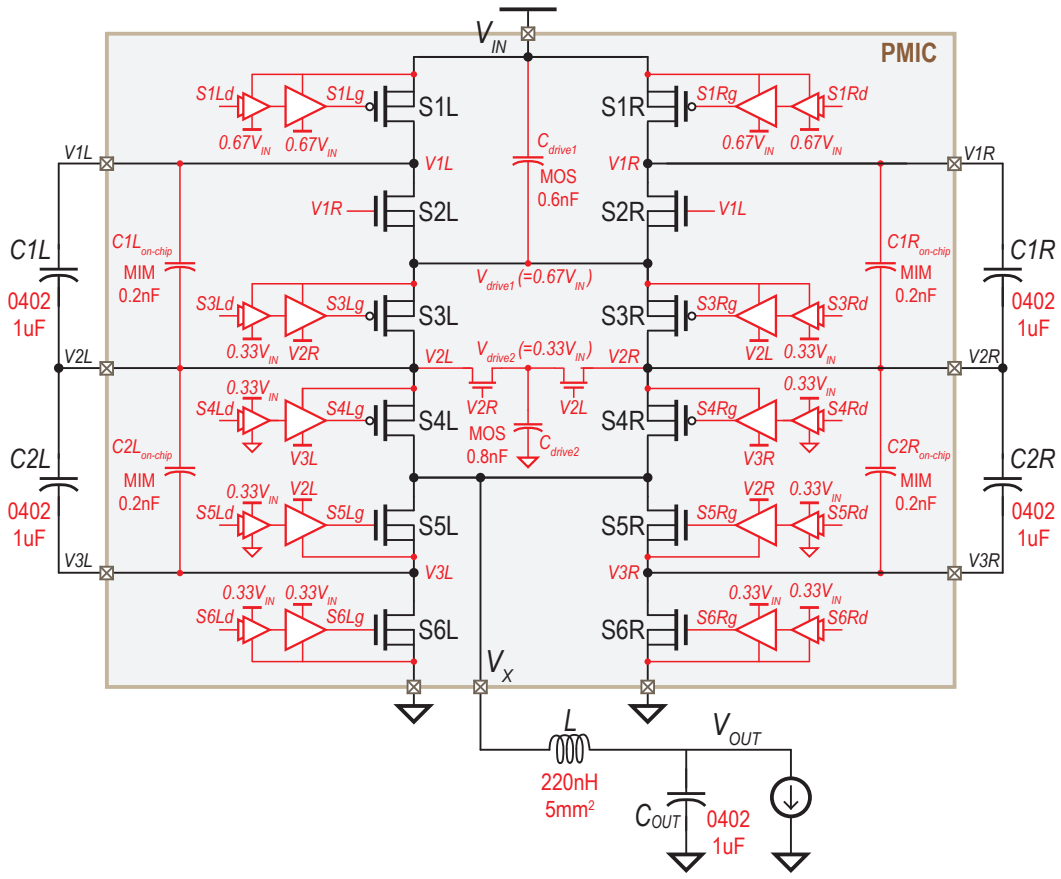


Figure 4.8: Full schematic of the prototyped converter.

4.4.4 Level Shifter and Control Logic

Figure 4.9 shows the control logic used to generate the ten control signals required for the power MOSFET drivers from a single PWM signal. A one-bit counter generates a Ph_Ctrl signal that is used to toggle the PWM signal between the left-side control signals (S1Ld, S3Ld, S4Ld, S5Ld and S6Ld) and the right-side control signals (S1Rd, S3Rd, S4Rd, S5Rd and S6Rd). Dead times between the control signals are then added via a simple delay circuit.

For S1R, S1L, S3R, and S3L, level shifters are required to shift the control signals of these switches to the appropriate levels. The schematic of the same level shifter used for all of theses control signals is shown in Fig. 4.10. For the S1L and S1R level shifters, V_{HIGH} is connected to V_{IN} while V_{LOW} is connected to $0.67V_{IN}$. For the S3L

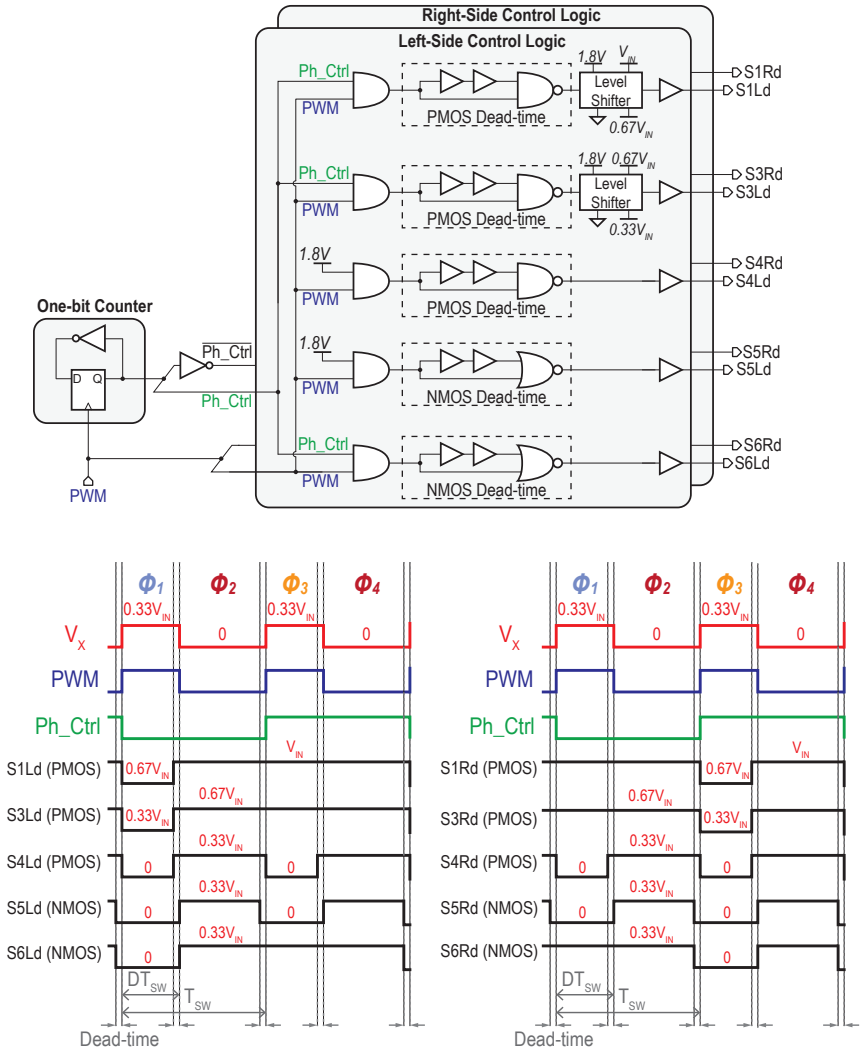


Figure 4.9: Schematic of the control logic used to generate the drive signals from a single PWM input signal, along side the resulting waveforms for the left and right sides of the converter.

and S3R level shifters, V_{HIGH} is connected to $0.67V_{IN}$ while V_{LOW} is connected to $0.33V_{IN}$. It can be noted that all of these power supplies are available internally as mentioned before.

During the converter start-up process, V_{IN} is increased gradually from zero until it reaches 1.8 V. At this point, $0.33V_{IN}$ is 0.6 V and $0.67V_{IN}$ is 1.2 V and the MOSFET drivers, powered from these internal supplies, start functioning. From this point on, the SMML converter is actually self-driven from its internal supplies. The control signals

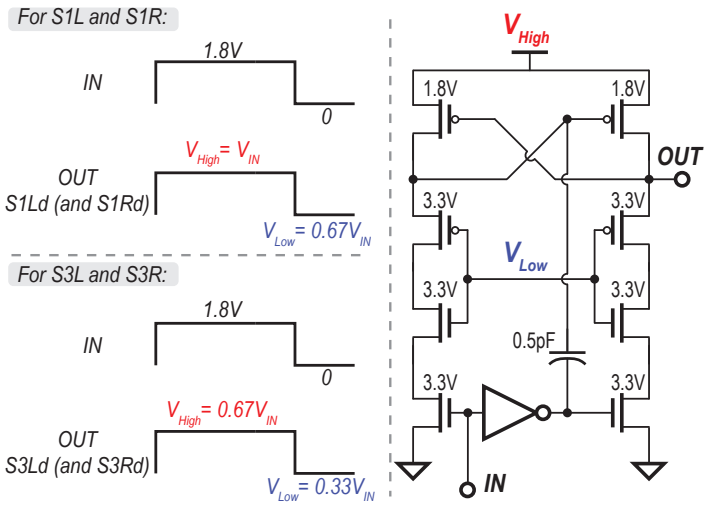


Figure 4.10: Schematic of the level shifter and its output waveform.

can then be asserted and the converter can start working properly from a V_{IN} as low as 1.8V where each of the MOSFETs has a sufficient overdrive voltage (i.e. $\approx$0.6 V) to turn them on/off. The initial 1.8 V input voltage does not violate any of the MOSFETs voltage rating (because some of the switches might need to block the whole 1.8V during the start-up since the flying capacitors can have zero voltage at start-up). After this initialization sequence, the input can be increased to the desired voltage while the converter and the flying capacitors are switching normally.

4.5 Measurement Results

The proposed SMML converter was implemented in a 180 nm CMOS process. A photo of the die, alongside the assembled converter, is shown in Fig. 4.11. In this implementation, C1R, C2R, C1L, and C2L were implemented using 1 μF 0.5 mm^2 capacitors that were mounted on the top of and wirebonded to the chip, while a 5 mm^2 220nH inductor and a 1 μF 0.5 mm^2 output capacitor were assembled on the bottom side of the interposer. The converter receives an input voltage of 3 to 5 V and provides an output voltage between 0.3 and 1.2 V with a maximum load current of 2.5 A. The converter operates in the continuous conduction mode (CCM), or in the forced CCM

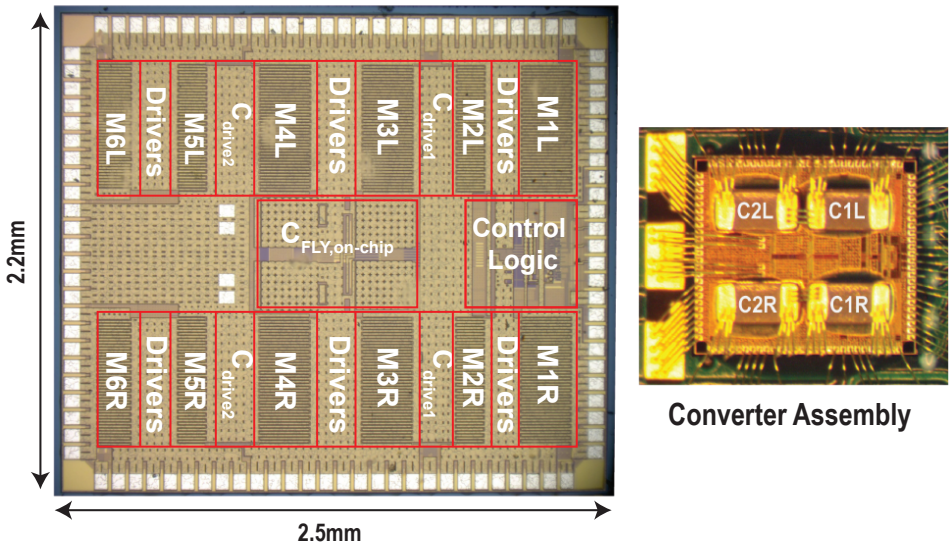


Figure 4.11: Die photo and converter assembly.

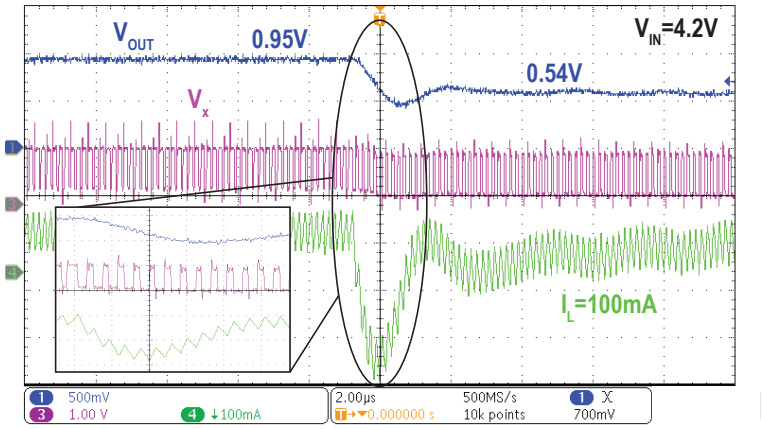


Figure 4.12: Measured waveforms of the converter response during a Vref step change by changing the duty cycle value.

if the load current is lower than half the inductor current ripple, with a main switching frequency of 5 MHz for the switching node (V_X).

Measurements during transient tests in Fig. 4.12 for V_{IN} =4.2 V reveal that node V_X switches with an amplitude of approximately 1.2 V as measured through a resistive debugging trace (used for attaching the current probe and has some IR drops prior to the measurement point), indicating correct operation of the internal rail generation. As also shown in Fig. 4.12, the converter responds in approximately 1.5 μs during a reference

step transient. The peak-to-peak output ripple under steady state operation is around 30-40 mV.

Measured efficiency results across various input voltages, output voltages and load currents that covers the operation range of the converter are shown in Fig. 4.13. The converter achieves a peak efficiency of 90% at a power density of 0.11W/mm^2, and an efficiency of 72% at a maximum power density of 0.52W/mm^2, where power density is computed by measuring the area of a rectangle that envelops the entire converter, including the chip and passives. It should be noted that an additional measurement data at V_{IN} of 5 V is included in this chapter compared to the original work in [49]. The converter losses are mainly proportional to the load current and are slightly dependent on the output voltage. Therefore, for similar load currents, the efficiency at lower output voltages drops as shown in Fig. 4.13 since the output power is reduced while the losses roughly remain the same. Fig. 4.14 shows the converter efficiency when sweeping over the switching frequency at different load currents which reveals that the optimum range of switching frequencies is around 3 to 5 MHz. As the switching frequency increases above the optimum range, the efficiency starts to degrade due to the increased switching losses while as the switching frequency decreases below the optimum range, the efficiency starts to degrade due to the increased current ripple and the increased internal charge sharing losses. Although being outside the intended operation range, the converter can still work at input voltages below 3.5 V and as low as 1.8 V. Fig. 4.15 shows the efficiency at low input voltages. It can be noted for input voltages lower than 3 V, the converter might not provide full SoC-compatible voltages (i.e. up to 1 or 1.2 V) since the maximum output voltage is limited to $0.33V_{IN}$. However, the output voltage range of the SMML converter can be extended through a modified topology as discussed in the following section.

To illustrate the impact of each loss component on the total efficiency, the estimated losses breakdown at different operating points is shown in Fig. 4.16. At high load current, the losses are dominated by the parasitic resistance of the on-chip and the package routing. This indicates that improving the packaging technology can enhance

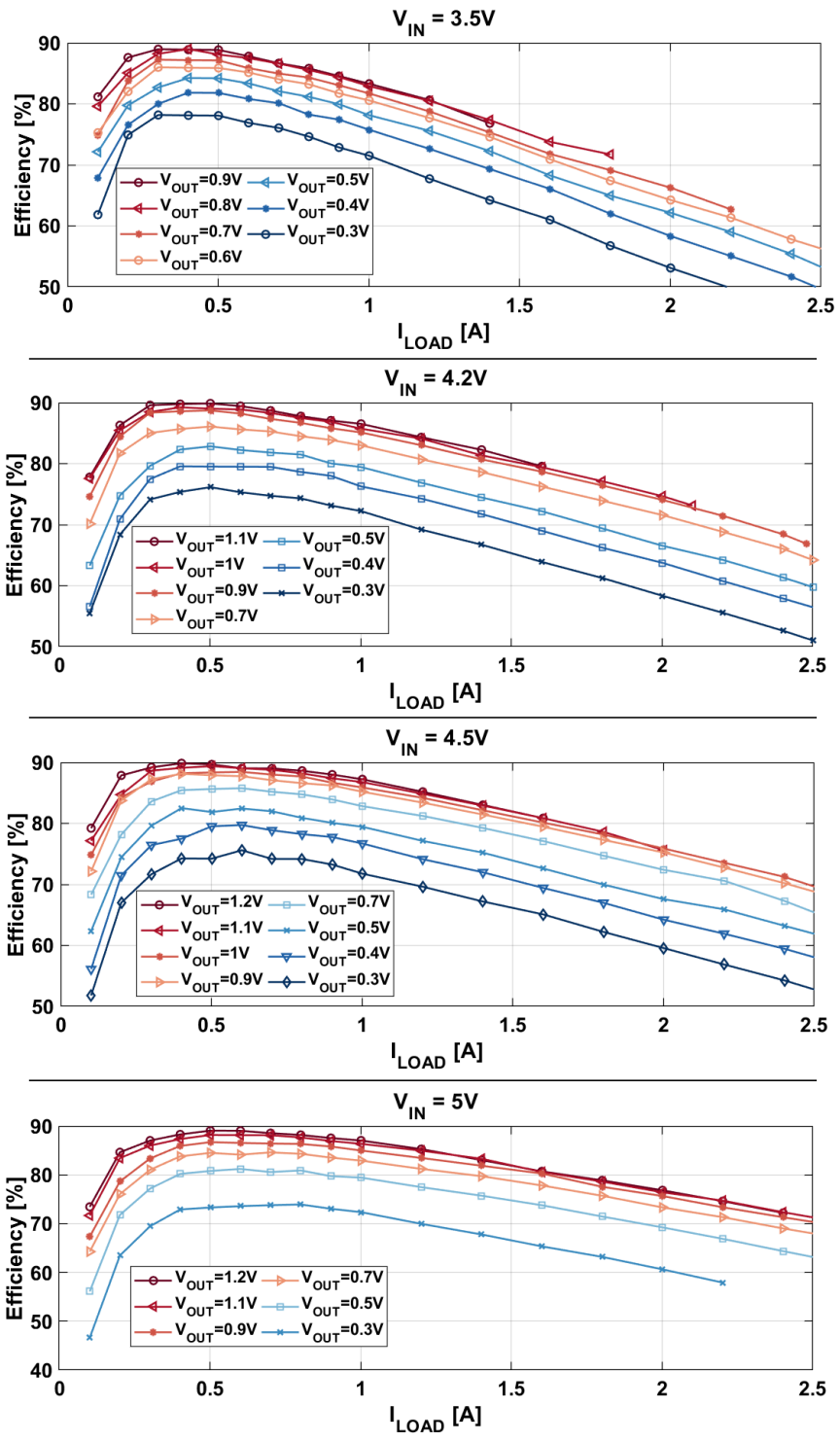


Figure 4.13: Measured efficiency across various input voltages, output voltages, and load currents.

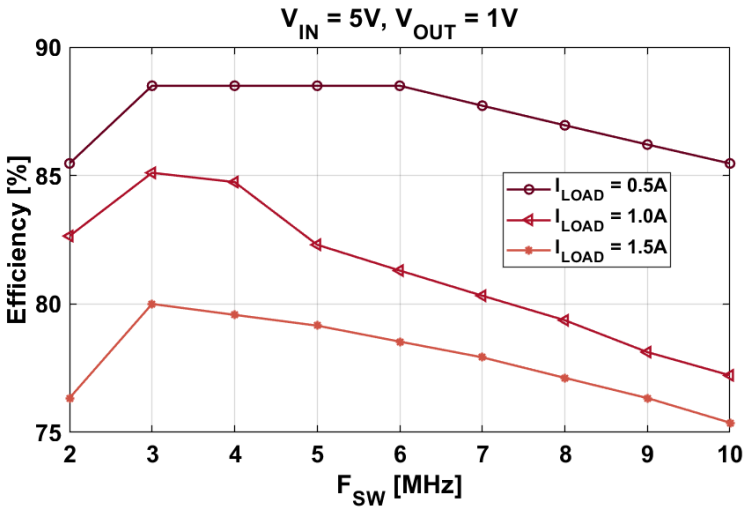


Figure 4.14: Measured efficiency versus the switching frequency of the V_X node at different load currents.

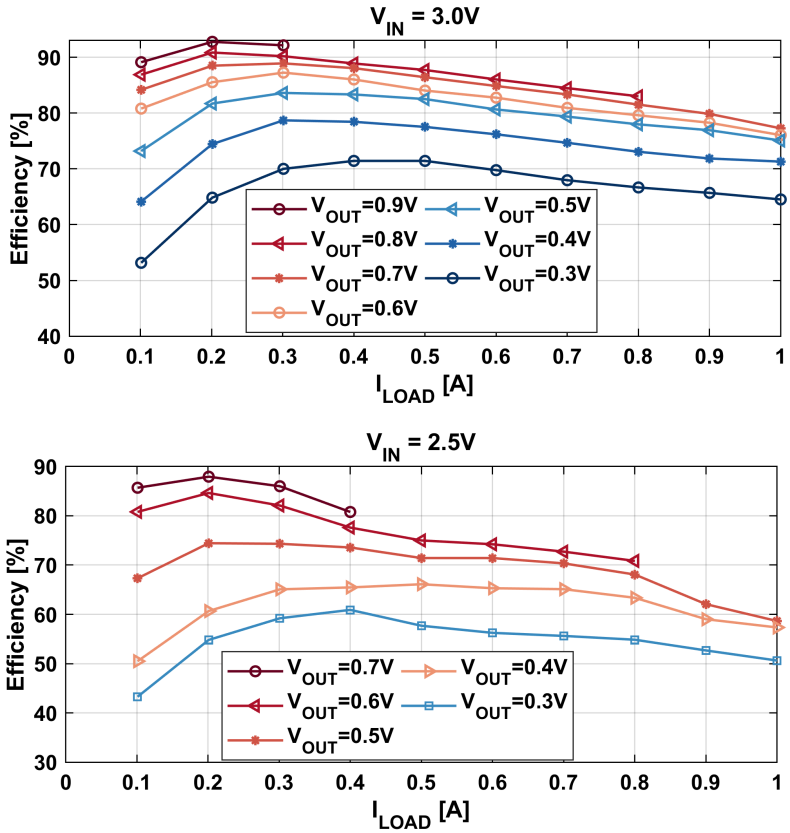


Figure 4.15: Measured efficiency for low input voltages ($V_{IN} \leq 3\ V$).

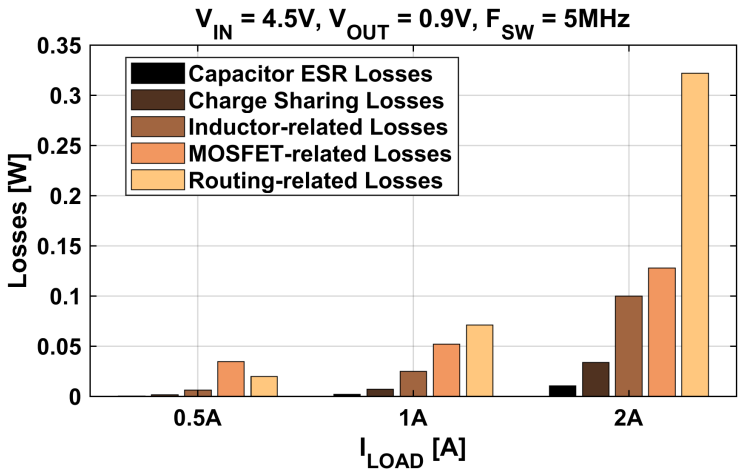


Figure 4.16: Estimated loss breakdown for a V_{IN} of 4.5 V and a V_{OUT} of 0.9 V.

the efficiency at high load currents significantly.

Table 4.1 summarizes the performance of the SMML converter, and compares with prior-art converters that are Li-ion-compatible and provide continuous conversion ratios in the SoC-compatible voltage range, including conventional buck converters and hybrid converters. The SMML converter achieves the highest power density per the converter total footprint of 0.52 W/mm^2 at a reasonably large conversion ratio of 4.2$\times$. At the peak efficiency point, the SMML converter has a power density of 0.11 W/mm^2. With that being said, it should be noted that there are other ways to define power density - by the total area of the converter (which is what is quoted above), by the summed total area of the individual passives only, or by the total volume of the converter. Table 4.1 also includes these numbers for the proposed design, along with prior-art (when sufficient information is available). For example, when calculating the power density per the summed total passives footprint, this work achieves 1.75$\times$ higher power density than [23], even if the capacitors were to be placed on the same side of the PCB as the inductor in this work. When calculating the power density per the converter total volume, this work achieves higher power density than the commercial parts EN6310QI and TPS826809, but has a slightly lower power density than TPS8268120. However, this work can achieve around 9% higher peak efficiency than TPS8268120. It should

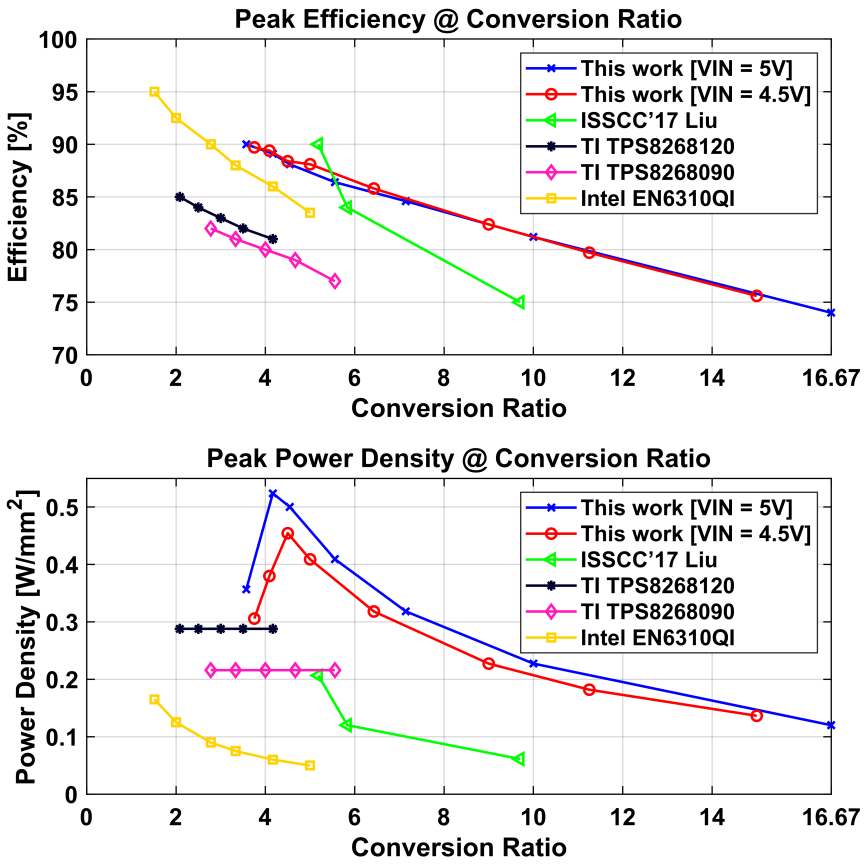


Figure 4.17: Measured peak efficiency and peak power density at various conversion ratios compared with prior converters.

be noted that unlike most other multi-level converters, the SMML converter does not require external supplies for drivers or level shifters.

The comparison is shown graphically in Fig. 4.17, where the top figure shows the peak efficiency achieved at each conversion ratio, and the bottom figure shows the peak power density achieved at each conversion ratio (computed by total converter area when possible). Compared to other converters, the SMML converter can maintain mostly higher efficiency and around 2× or more higher power density. At the same time, the SMML converter can provide conversion ratios up to 16.7×, which is higher than the maximum conversion ratio other converters can provide, all at comparable efficiencies to prior art operating at lower conversion ratios.

Table 4.1: Comparison with prior Li-ion compatible DC-DC converters with continuous conversion ratios

	Intel EN6310QI	**TI TPS8268090**	**TI TPS8268120**	**[22] Liu, ISSCC'17**	**[12] Li, JSSC'18**	**This Work**
Structure	Buck	Buck	Buck	Hybrid (Multilevel Dickon)	Hybrid (Stacked resonant)	**Hybrid (SMML)**
Process	NR	NR	NR	65nm	150nm	**180nm**
Input Voltage [V]	2.7 - 5.5	2.3 - 5.5	2.3 - 5.5	3.0 – 4.5	3.2 – 4.2	**3.0 – 5.0**
Output Voltage [V]	0.6 – 3.3	0.9	1.2	0.3 – 1.0	0.8 – 1.5	**0.3 – 1.2**
Max. Load Current [A]	1	1.6	1.6	1.53	1.5	**2.5**
Total Converter Area [mm^2]	20	6.67	6.67	6†	14.4	**5.5**
Inductor	NR	NR	NR	180 nH (Discrete)	3 x 4.2 nH (PCB Trace)	**220 nH (Discrete)**
Flying Capacitor	N/A	N/A	N/A	3 x 22 µF (Ceramic 0402)	6 x 0.47 µF (Ceramic 01005)	**4 x 1 µF (Ceramic 0402)**
Output Capacitor	NR	NR	NR	22 µF (Ceramic 0402)	20 nF (On-chip)	**1 µF (Ceramic 0402)**
External rails for drivers?	NO	NO	NO	YES ($0.5V_{IN}$)	NO	**NO**
Maximum Output Power [W] @ V_{IN}, conv. ratio	1 @ 5V, 5	1.44 @ 5V, 5.6	1.92 @ 5V, 4.2	1.24 @ 4.2V, 5.2	1.56† @ 4.2V, 3.5	**2.88 @ 5V, 4.2**
Peak Power Density per Passives Total Footprint [W/mm^2]	NR	NR	NR	0.22†,††	NR	**0.384**
Peak Power Density per Converter Total Volume [W/mm^3]	0.027	0.216	0.288	NR	NR	**0.233**
Peak Power Density per Converter Total Area [W/mm^2]	0.05† @ 5V, 5	0.22† @ 5V, 5.6	0.29† @ 5V, 4.2	0.22†,†† @ 4.2V, 5.2	0.11 @ 4.2V, 3.5	**0.52 @ 5V, 4.2**
Efficiency @ Peak Power Density	79%†	65%†	72%†	64%†,††	83.4%	**72%**
Peak Efficiency (PE) @ V_{IN}, conv. ratio	84%† @ 5V, 5	78%† @ 5V, 5.6	81%† @ 5V, 4.2	90%†,†† @ 4.2V, 5.2	87.2% @ 3.8V, 3.2	**89.5% @ 5V, 4.2 90% @ 4.2V, 3.8**
Power Density per Converter Total Area [W/mm^2] @ PE	0.02†	0.047†	0.063†	0.04†,††	0.083†	**0.11**
Peak Efficiency @ max. conv. ratio	NR	78%† @ 5.6	81%† @ 4.2	75% @ 9.7	70%† @ 4.5	**74% @ 16.7**

† **Estimated from plotted data**
†† **Using a 180nH inductor; other measurements mentioned in the paper utilized a 470nH inductor of unspecified size**
NR – Not Reported N/A – Not Applicable

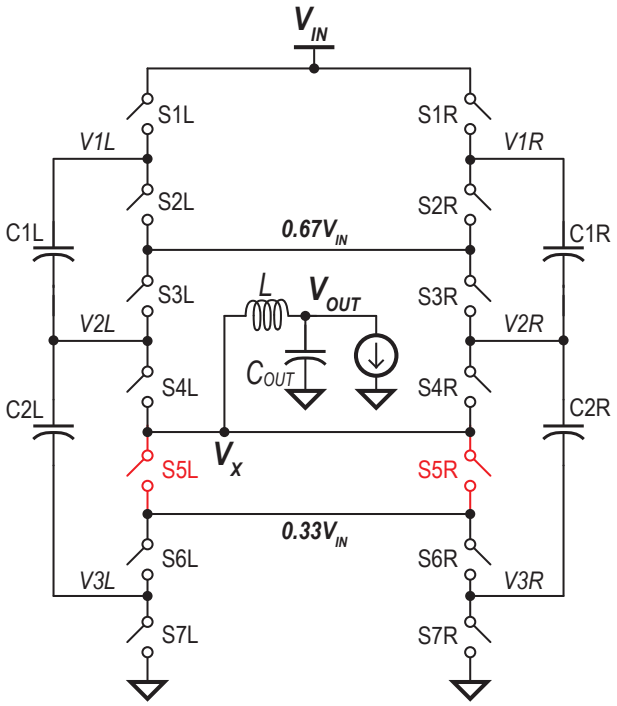


Figure 4.18: An extended-range SMML topology that can operate in both the first region ($0 < V_{OUT} < 0.33V_{IN}$) and the second region ($0.33V_{IN} < V_{OUT} < 0.67V_{IN}$).

It is important to note that the SMML converter requires four flying capacitors, which might be higher compared to some other multilevel converters that utilize fewer capacitors. However, since only a portion of the load current (I_L) goes through each capacitor, (e.g. $0.33I_L$ in C1L and C1R, and $0.67I_L$ in C2L and C2R), these capacitors can be sized smaller as compared to capacitors in some other multilevel converters.

4.6 Discussion of Other Level Operation

It is worth mentioning that the presented converter operates in the lowest region only, which means that the theoretical maximum output voltage is $0.33V_{IN}$. This can be a limitation when the battery input voltage goes extremely small (i.e., less than 3V) where the converter might not provide the full output range needed for SoC applications (e.g. $V_{OUT} \geq 1\,V$). If it is desired to extend the operation range of the SMML topology, a modified SMML topology, shown in Fig. 4.18, can be used which can operate in

two regions (i.e. $0 < V_{OUT} < 0.33V_{IN}$ and $0.33V_{IN} < V_{OUT} < 0.67V_{IN}$). Two switches, S5L and S5R, are added to allow for more switching phases that can introduce a $0.67V_{IN}$ voltage at the switching node V_X. It is also worth mentioning that this is the case in most multilevel converters, except the FCML topology, where operation in other regions requires the addition of more switches to enable more switching phases [21, 24] which might incur additional area overhead and/or losses.

4.7 Conclusion

A Symmetrical Modified Multilevel Ladder (SMML) converter is presented that can operate from Li-ion battery voltages and provide continuous conversion ratios down to SoC-compatible voltages. The converter offers reduced conduction losses, flying capacitors that are naturally balanced, and no need for external supplies for drivers or level shifters, which topologically solves important challenges in baseline multi-level converters. The converter achieves state-of-the-art power density at high efficiencies, where it can provide conversion ratios up to 16.7 at efficiencies $> 74\%$.

4.8 Acknowledgement

Chapter 4 is based on and mostly a reprint of the following publications:

- A. Abdulslam, B. H. Lam and P. P. Mercier, "A Battery-Connected Symmetric Modified Multilevel Ladder Converter Achieving 0.45 W/mm^2 Power Density and 90% Peak Efficiency," *IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, 2019, pp. 1-4.

- A. Abdulslam and P. P. Mercier, "A Symmetric Modified Multilevel Ladder PMIC for Battery-Connected Applications," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 767-780, March 2020.

The dissertation author is the primary investigator and author of the work in these papers.

Chapter 5

A Battery-Connected Inductor-First Flying Capacitor Multilevel Converter

5.1 Introduction

Modern mobile and IoT devices require power management solutions that are efficient, compact, and can operate directly from Li-ion battery voltages (2.8-4.5V). Unfortunately, it is difficult to achieve both high power density and high efficiency from a conventional buck converter, in part since the inductor, which must be miniaturized for power density reasons, has a large DCR and thus has large conduction losses when placed on the high-current side of the converter as depicted in Fig. 5.1. To reduce inductor DCR losses, an inductor-first buck was shown in [33] that split the output inductor into two half-sized inductors placed in series with the input, where they process lower current and thus have lower net conduction losses as shown in Fig. 5.2. Importantly, this arrangement provides a continuous, non-chopped input current, and thus reduces EMI which is an important concern in power management [34, 53]. However, processing Li-ion voltages with conventional or inductor-first buck structures require either 5V transistors, which are not available in all CMOS processes, or requires transistor stacking. It is now well known that if transistor stacking is needed, then a flying capacitor multilevel (FCML) structure can reduce the voltage swing seen by the inductor, which offers size, ripple, and loss advantages as shown in Fig. 5.3 [54, 55]. Despite the advantages, however, the FCML structure still places the inductor at the high-current side of the converter, where its high DCR can contribute significant losses. In addition, the

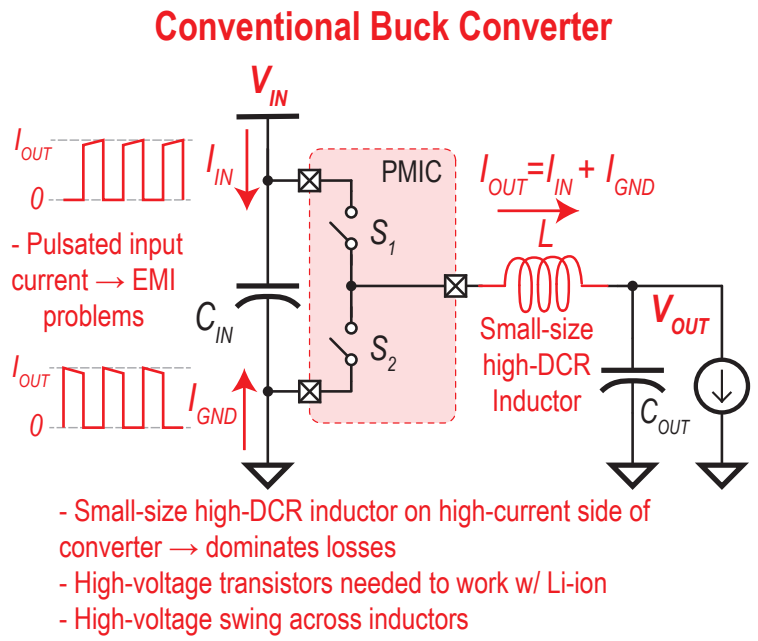


Figure 5.1: A conventional buck converter where the small-size large-DCR inductor is placed at the high-current side of the converter.

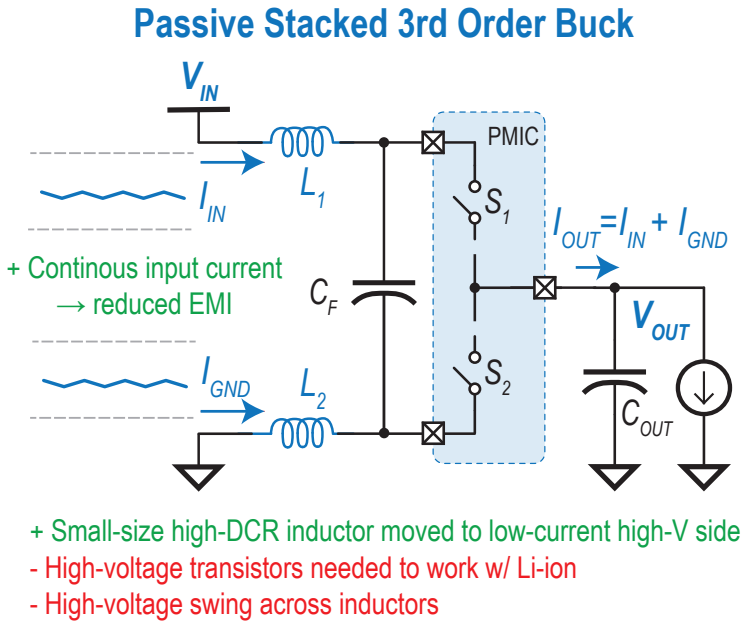


Figure 5.2: An inductor-first buck converter where the small-size large-DCR inductors are placed at the low-current side of the converter.

pulsated input current results in the same EMI issues as conventional buck converters.

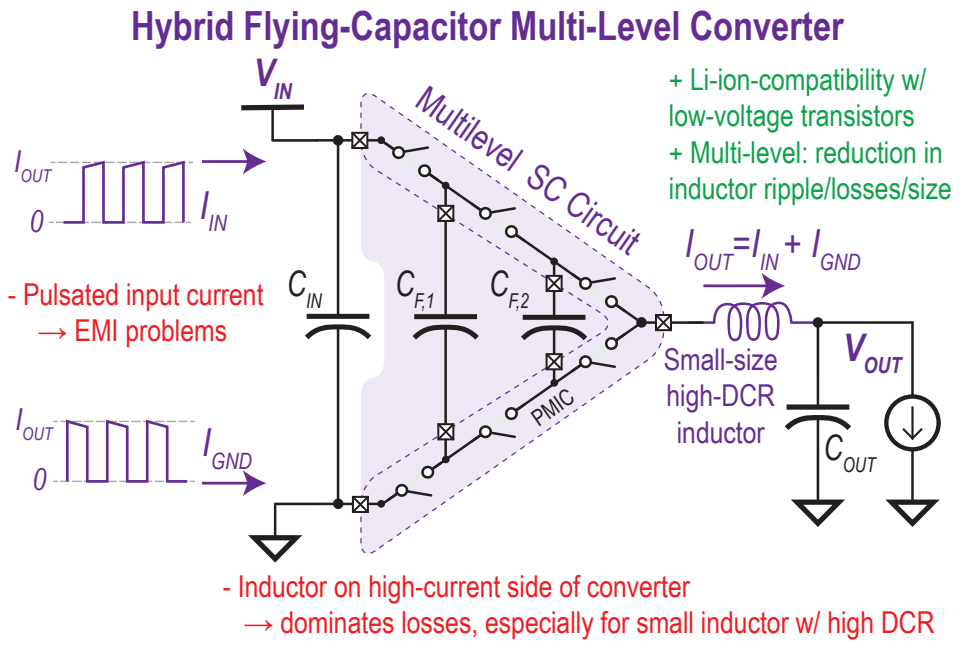


Figure 5.3: A hybrid flying capacitor multilevel (FCML) converter where the voltage swing seen by the inductor is reduced.

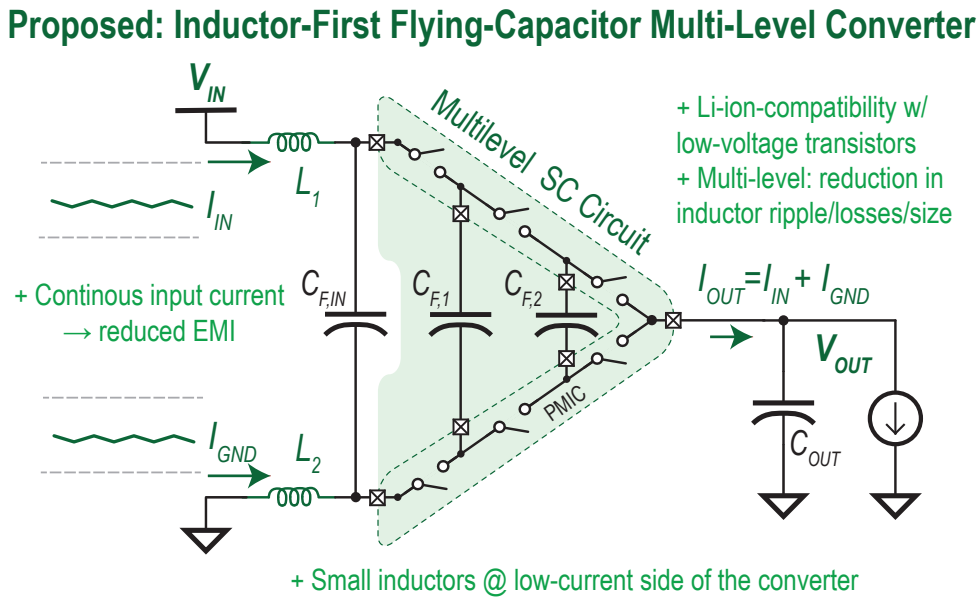


Figure 5.4: Proposed inductor-first FCML converter which combines the advantages of an FCML converter with the advantages of an inductor-first structure.

5.2 Inductor-first Flying Capacitor Multilevel Converter

To address these issues, this chapter presents an inductor-first FCML converter, shown in Fig. 5.4, which combines the advantages of an FCML converter (Li-ion compatibility with low-voltage transistors and reduced inductor size/losses) with the advantages of an input-side inductor structure (inductors on the low-current side of the converter for further loss reduction and input current filtering for reduced EMI).

The detailed circuit of the proposed inductor-first FCML converter is shown in Fig. 5.5. It can generate arbitrary output voltages between V_{IN} and GND through three operating regions: $\{0,V_{IN}/3\}$, $\{V_{IN}/3, 2/3V_{IN}\}$, and $\{2/3V_{IN}, V_{IN}\}$. As illustrated in Fig. 5.6, the employed flying capacitors reduce the voltage swing on the inductor to $1/3V_{IN}$ across all operating regions, enabling a reduction of inductor size/losses relative to a conventional inductor-first buck. The blocking voltage of all power MOSFETs is limited to $1/3V_{IN}$, enabling use of 1.8V MOSFETs for V_{IN} up to 5V. The input decoupling capacitor in an FCML converter is in this case converted into a flying capacitor, C_{FIN}, which is naturally balanced at V_{IN} according to the volt-second relationships of inductors $L_{1,2}$, while the two other flying capacitors, C_{F1} and C_{F2}, are balanced at $2/3V_{IN}$ and $1/3V_{IN}$, respectively. One switching cycle for each region has six phases, where in each phase the flying capacitors are either charging, discharging, or idle. The V_{X1} node is switching above and below V_{IN}, allowing L_1 to de-energize/energize and, similarly, V_{X2} is switching above and below GND allowing L_2 to energize/de-energize, with load current continuously supplied to the output across both switching phases. Figure 5.7 shows the inductor current ripple of an inductor-first FCML converter as compared to a conventional inductor-first buck converter where at least $3\times$ reduction in the current ripple is achieved.

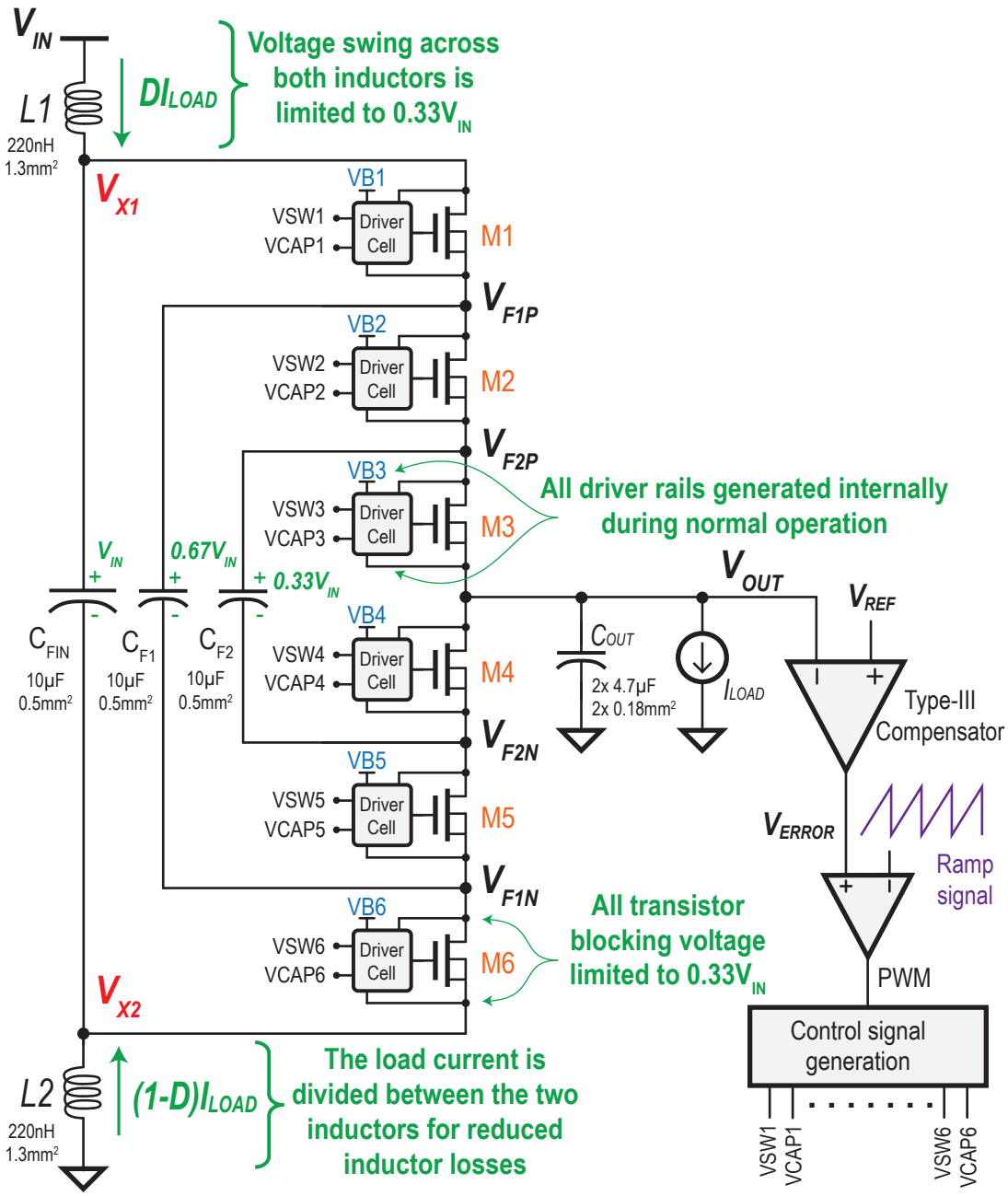


Figure 5.5: Detailed schematic of the proposed inductor-first FCML converter.

5.3 Converter Losses Modeling

Modeling the losses of the converter can help in optimizing the converter design and maximizing its efficiency around the desired operating points. Usually, the modeling

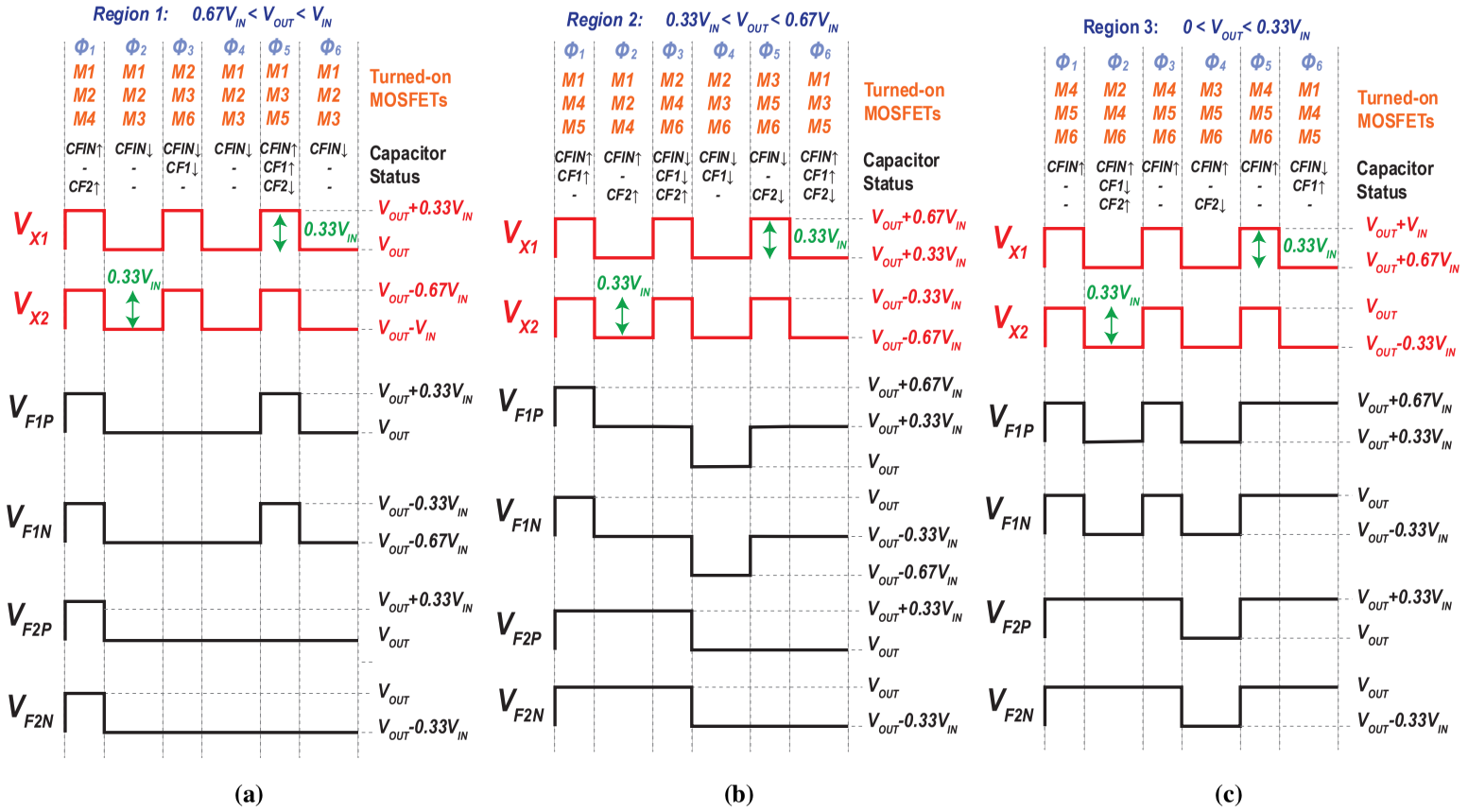


Figure 5.6: Converter timing diagram illustrating the waveforms of the converter switching nodes in the (a) first, (b) second, and (c) third operating regions.

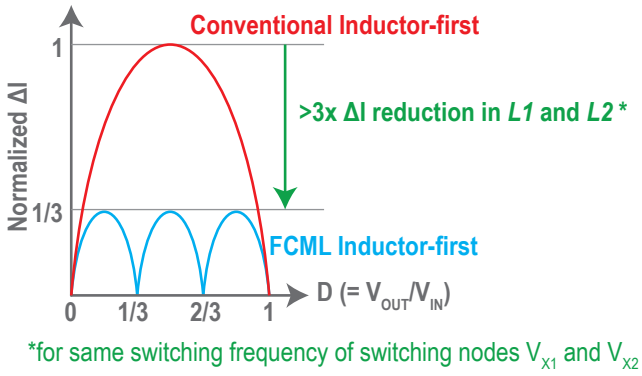


Figure 5.7: Comparison between the inductor current ripple in a conventional inductor-first converter and an inductor-first FCML converter.

of multilevel hybrid converters with multiple inductors, capacitors, and switches can be complicated [24, 51, 52]. A systematic method is developed in this chapter to estimate the losses in the inductor-first FCML converters. The dominant losses in the converter under normal operation are the inductor losses, the MOSFET conduction losses, the MOSFET switching losses, and the flying capacitor losses, which will all be modeled in the following subsections.

5.3.1 Inductor Losses

The main duty cycle of the converter (D) is related to the relation between V_{IN} and V_{OUT} and is defined as V_{OUT}/V_{IN}. However, the switching nodes V_{X1} and V_{X2} have a different duty cycle which is given by D_X. The range of D_X goes between zero and one in each operating region as depicted in Fig. 5.6. The relationship between the main duty cycle ($D = V_{OUT}/V_{IN}$) and the the duty cycle (D_X) of the switching nodes V_{X1} and V_{X2} is dependent on the operating region of the converter and is given by:

$$D_X = \begin{cases} 3 \times (D - \frac{2}{3}) & \text{1st region: } \frac{2}{3} \leq D < 1 \\ 3 \times (D - \frac{1}{3}) & \text{2nd region: } \frac{1}{3} \leq D < \frac{2}{3} \\ 3 \times D & \text{3rd region: } 0 \leq D < \frac{1}{3} \end{cases} \tag{5.1}$$

. The switching voltage of V_{X1} and V_{X2} generates a current ripple in both inductors $L1$ and $L2$. When operating in the continuous conduction mode (CCM), the current ripple in each inductor is given by:

$$\Delta I = \Delta V \frac{D_X(1-D_X)}{L \times F_{SW}} = \frac{V_{IN}}{3} \frac{D_X(1-D_X)}{L \times F_{SW}} \tag{5.2}$$

where V_{IN} is the input voltage, D_X is the duty cycle of V_{X1} or V_{X2}, L is the inductor value, and F_{SW} is the switching frequency of the V_{X1} and V_{X2} (which is not necessarily the switching frequency of the individual MOSFETs). ΔV is the voltage swing of both V_{X1} and V_{X2} which is equal to $\frac{1}{3}V_{IN}$, as illustrated in Fig. 5.6. The $\frac{1}{3}$ factor is due to the multilevel operation, which results in a lower current ripple in the inductor.

The average current in $L1$ is the same as the current form the input source (V_{IN}) and is equal to DI_{LOAD} while the average current in $L2$ is equal to $(1-D)I_{LOAD}$. The summation of both currents in $L1$ and $L2$ is equal to the load current I_{LOAD} according to Kirchhoff's current law (KCL). In this case, the conduction loss in the inductor $L1$, which has a DC resistance of DCR, is given by:

$$P_{L1} = \left([DI_{LOAD}]^2 + \frac{\Delta I^2}{12} \right) \times DCR. \tag{5.3}$$

Similarly, the conduction loss in the inductor L2 is given by:

$$P_{L2} = \left([(1-D)I_{LOAD}]^2 + \frac{\Delta I^2}{12} \right) \times DCR. \tag{5.4}$$

5.3.2 MOSFET Conduction Losses

The current in both inductors $L1$ and $L2$ is summed either at the V_{X1} node or at the V_{X2} node and then flows through the flying capacitors and the power switches. In each region, the converter has six operating phases as illustrated in Fig. 5.6. In this case,

the switch conduction losses in the inductor-first FCML converter are given by:

$$P_{Cond} = \left(I_{LOAD}^2 + \frac{(2\Delta I)^2}{12} \right) \sum_{\substack{1 \le i \le 6 \\ 1 \le j \le 6}} a(i,j)^2 R_j (\frac{T_i}{T_t}) \tag{5.5}$$

where I_{LOAD} represents the load current, R_j represents the on-resistance of switch S_j, T_i represents the time duration of the phase ϕ_i, and T_t represents the total duration of the six phases of the converter. Resistance R_j can be defined as (r_{ON}/W_j), where W_j is the width of switch S_j and r_{ON} is the switch on-resistance per unit width. T_t represents the duration of one switching sequence (i.e., Φ_1 to Φ_6), and is typically equal to triple the switching period of the inductor. The coefficient $a(i,j)$ represents the percentage of the summed inductor current going through switch S_j in phase ϕ_i. Each individual coefficient $a(i,j)$ is an element in a 6×6 matrix $\mathbf{A}$ which represents the number of the switches and the number of the operating phases. In each operating region, the switches have different configurations in the six phases, and hence there are three matrices $\mathbf{A_1}$, $\mathbf{A_2}$, and $\mathbf{A_3}$ representing the switch configuration in the the first, the second and the third operating regions, respectively. These matrices are given by:

$$\mathbf{A_1} = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 \end{bmatrix}, \tag{5.6}$$

$$\mathbf{A_2} = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}, \tag{5.7}$$

$$\mathbf{A_3} = \begin{bmatrix} 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 \end{bmatrix}. \tag{5.8}$$

Depending on the operating region, the corresponding matrix can be selected to calculate the MOSFET conduction losses according to (5.5).

5.3.3 MOSFET Switching Losses

MOSFET switching losses occur due to the charging/discharging of each MOSFET's parasitic capacitances: C_D, C_G, and C_J, which represents the drain-to-source, gate-to-source, and the junction parasitic capacitance, respectively. To represent these losses in a systematic way, characterizing matrices for the voltage on these parasitic capacitors are developed. When a MOSFET switch turns ON/OFF, its blocking voltage, V_D, changes from $0.33V_{IN}$ to zero or vice versa. This change in V_D results in the charging/discharging losses of C_D. V_D of each MOSFET can be represented in a 6×6 matrix, $\mathbf{V_D}$, where each element, $v_d(i,j)$, is the blocking voltage on switch (S_j) in phase (Φ_i), as a fraction of V_{IN}. When a MOSFET switch is ON, its corresponding $v_d(i,j)$ is zero. Due to the different switch configurations in each region, there are three matrices, $\mathbf{V_{D1}}$,

$\mathbf{V_{D2}}$, and $\mathbf{V_{D3}}$, representing the three operating regions, respectively, and are given by:

$$\mathbf{V_{D1}} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ 0 & \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \end{bmatrix}, \tag{5.9}$$

$$\mathbf{V_{D2}} = \begin{bmatrix} \frac{1}{3} & 0 & 0 & \frac{1}{3} & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & 0 \\ 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} \\ 0 & \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} \\ 0 & 0 & \frac{1}{3} & 0 & \frac{1}{3} & \frac{1}{3} \\ \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 \end{bmatrix}, \tag{5.10}$$

$$\mathbf{V_{D3}} = \begin{bmatrix} 0 & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \\ 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} \\ 0 & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \\ 0 & 0 & \frac{1}{3} & 0 & \frac{1}{3} & \frac{1}{3} \\ 0 & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \\ \frac{1}{3} & 0 & 0 & \frac{1}{3} & \frac{1}{3} & 0 \end{bmatrix}. \tag{5.11}$$

Similarly, the gate-to source voltage or the overdrive voltage for a switching MOSFET changes from 0 to the maximum drive voltage or vice versa. In the employed inductor-first FCML converter, the MOSFETs are driven directly from the converter internal nodes. Therefore, the overdrive voltage of the power MOSFETs is equal to $0.33V_{IN}$ when the MOSFET is ON and zero when the MOSFET is OFF. Since the blocking volt-

age of all the MOSFETs in the inductor-first FCML converter is $0.33V_{IN}$, which is the same as the overdrive voltage value, the same matrix $\mathbf{V_D}$ can then be used to represent the MOSFET overdrive voltage in each phase where a V_D of zero means an overdrive voltage of $0.33V_{IN}$ for the corresponding switch, and vice versa. Additionally, changes in the absolute value of the MOSFET source voltage results in the charging/discharging of the parasitic junction capacitor, C_J, between the source terminal of a MOSFET and the chip bulk which is biased to ground. A $\mathbf{V_S}$ matrix represents the MOSFET source voltage in each phase, as a fraction of V_{IN} and referenced to V_{OUT}, and can be given by either of the following three matrices depending on the operating region of the converter:

$$\mathbf{V_{S1}} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & 0 & 0 & -\frac{1}{3} & -\frac{2}{3} \\ 0 & 0 & 0 & -\frac{1}{3} & -\frac{2}{3} & -1 \\ 0 & 0 & 0 & -\frac{1}{3} & -\frac{2}{3} & -\frac{2}{3} \\ 0 & 0 & 0 & -\frac{1}{3} & -\frac{2}{3} & -1 \\ \frac{1}{3} & 0 & 0 & -\frac{1}{3} & -\frac{1}{3} & -\frac{2}{3} \\ 0 & 0 & 0 & -\frac{1}{3} & -\frac{2}{3} & -1 \end{bmatrix}, \tag{5.12}$$

$$\mathbf{V_{S2}} = \begin{bmatrix} \frac{2}{3} & \frac{1}{3} & 0 & 0 & 0 & -\frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & 0 & 0 & -\frac{1}{3} & -\frac{2}{3} \\ \frac{1}{3} & \frac{1}{3} & 0 & 0 & -\frac{1}{3} & -\frac{1}{3} \\ 0 & 0 & 0 & -\frac{1}{3} & -\frac{2}{3} & -\frac{2}{3} \\ \frac{1}{3} & 0 & 0 & -\frac{1}{3} & -\frac{1}{3} & -\frac{1}{3} \\ \frac{1}{3} & 0 & 0 & -\frac{1}{3} & -\frac{1}{3} & -\frac{2}{3} \end{bmatrix}. \tag{5.13}$$

$$\mathbf{V_{S3}} = \begin{bmatrix} \frac{2}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 \\ \frac{1}{3} & \frac{1}{3} & 0 & 0 & -\frac{1}{3} & -\frac{1}{3} \\ \frac{2}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 \\ \frac{1}{3} & 0 & 0 & -\frac{1}{3} & -\frac{1}{3} & -\frac{1}{3} \\ \frac{2}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 \\ \frac{2}{3} & \frac{1}{3} & 0 & 0 & 0 & -\frac{1}{3} \end{bmatrix}. \tag{5.14}$$

By using the aforementioned matrices, the total switching loss of the MOSFETs (P_{SW}) can be given by:

$$\begin{aligned} P_{SW} = &\frac{1}{6} V_{IN}^2 F_{SW} \sum_{\substack{1 \le i \le 6 \\ 1 \le j \le 6}} \Delta v_d(i,j)^2 C_{D,j} \\ &+ \frac{1}{6} V_{IN}^2 F_{SW} \sum_{\substack{1 \le i \le 6 \\ 1 \le j \le 6}} \Delta v_d(i,j)^2 C_{G,j} \\ &+ \frac{1}{6} V_{IN}^2 F_{SW} \sum_{\substack{1 \le i \le 6 \\ 1 \le j \le 6}} \Delta v_s(i,j)^2 C_{J,j}, \end{aligned} \tag{5.15}$$

where $\Delta v_d(i,j)$ represents the difference between a MOSFET blocking voltage in the current phase (ϕ_i) and the MOSFET blocking voltage in the preceding phase (ϕ_{i-1}) (i.e., $v_d(i,j) - v_d(i-1,j)$), which is calculated using the $\mathbf{V_D}$ matrix. $\Delta v_d(i,j)$ will be zero if the switch remains ON or OFF when transitioning from ϕ_{i-1} to ϕ_i. Similarly, $\Delta v_s(i,j)$ represents the difference between the MOSFET source voltages when going from one phase to the next and is calculated using the $\mathbf{V_S}$ matrix. The parasitic capacitors $C_{D,j}$, $C_{G,j}$, and $C_{J,j}$ of a switch S_j are assumed to scale linearly with the switch width for simplicity.

5.3.4 Capacitor Losses

The inductor-first FCML converter has one input flying capacitor C_{FIN} and two normal flying capacitors C_{F1} and C_{F2}, each with an equivalent series resistance (ESR)

that causes conduction losses. The conduction losses in C_{FIN} due to its ESR is given by:

$$P_{CFIN} = \left([(1-D)I_L]^2 + \frac{\Delta I^2}{12} \right) ESR_{IN} D + \left([DI_L]^2 + \frac{\Delta I^2}{12} \right) ESR_{IN}(1-D), \tag{5.16}$$

The conduction losses in the two normal flying capacitors, C_{F1} and C_{F2}, are given by:

$$P_{CF} = \left(I_L^2 + \frac{\Delta I^2}{12} \right) \sum_{\substack{1 \le i \le 6 \\ 1 \le j \le 2}} (c_{i,j})^2 ESR_j (\frac{T_i}{T_t}), \tag{5.17}$$

where $c_{i,j}$ is an element of a 6-by-2 matrix, $\mathbf{C}$, that represents the percentage of the summed inductor currents going through each of the flying capacitors. Depending on the operating region of the converter, $\mathbf{C}$ can be one of three matrices, $\mathbf{C_1}$, $\mathbf{C_2}$, or $\mathbf{C_3}$, representing the three operating regions, respectively, and are given by:

$$\mathbf{C_1} = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 \end{bmatrix}^T, \tag{5.18}$$

$$\mathbf{C_2} = \begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}^T, \tag{5.19}$$

$$\mathbf{C_3} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 \end{bmatrix}^T. \tag{5.20}$$

5.3.5 Total Losses

By combining the losses of the individual components, the total losses of the converter can be given by:

$$P_{Losses} = P_{Cond} + P_{SW} + P_{L1} + P_{L2} + P_{CFIN} + P_{CF} + P_{others}, \tag{5.21}$$

where P_{others} includes other losses like the routing losses which can be significant if the PMIC is built on modern CMOS technologies that has limited routing or packaging resources. P_{Losses} represents the total losses of the converter at a given operating point and is a function of the switching frequency, F_{SW}, and switch sizes, W_j.

5.3.6 Optimization

To minimize the converter losses, the design parameters to be optimized are the switching frequency and the switch widths. If the switching frequency is predetermined according to some other design considerations, like the transient response and the output ripple, the switch widths are the only parameters to be optimized for minimum losses. Each of the 6 switches in the inductor-first FCML topology has its corresponding conduction and switching losses, which are a function in the switch width, and are calculated as:

$$P_{switch,j} = \left(I_L^2 + \frac{\Delta I^2}{12}\right)\frac{\alpha}{W_j} + V_{IN}^2 F_{SW} W_j \beta. \tag{5.22}$$

α and β are two coefficients related to the conduction and the switching losses of each switch throughout the four phases, respectively, and are given by:

$$\begin{aligned} \alpha &= \sum_{1\le i\le 6} a(i,j)^2 (\frac{T_i}{T_t}) r_{ON} \\ \beta &= \sum_{1\le i\le 6} \left(\Delta v_d(i,j)^2 c_D + \Delta v_d(i,j)^2 c_G + \Delta v_s(i,j)^2 c_J\right), \end{aligned} \tag{5.23}$$

where r_{ON}, c_D, c_G, and c_J are the switch on-resistance, drain capacitance, gate capacitance, and junction capacitance, all per unit width. By differentiating the total switch losses with respect to the switch width W_j, and equating to zero, the optimum width for each MOSFET can be found as:

$$W_{opt,j} = \sqrt{\left(I_L^2 + \frac{\Delta I^2}{12}\right)\frac{1}{V_{IN}^2 F_{SW}}\frac{\alpha}{\beta}}, \tag{5.24}$$

where $W_{opt,j}$ is the optimum width of switch j at a given switching frequency and operating point (i.e. V_{OUT} and I_{LOAD}). If a comprehensive optimization of the converter that includes both the switching frequency and the switch sizes as design parameters is desired, the equations derived in this section can be used in an optimization process by the help of some analysis tools, for example, MATLAB.

5.4 Circuit Implementation

Generating the appropriate driving rails for stacked transistors is often challenging; in this design, each transistor is implemented using the same 1.8V core NMOS transistor, with all needed rails generated directly from the switching nodes. Each driver cell consists of two level-shifters and cascaded buffers as shown in Fig. 5.8. One control signal (VSWx) is used to control the on/off time of the power MOSFET, while the other control signal (VCAPx) is used to control the charging/discharging of the bootstrapping capacitor. A bootstrapping capacitor is used in each driver cell to generate the boosted voltage required to drive the associated power MOSFET. When a power MOSFET is off, it is blocking a voltage of $1/3V_{IN}$, and hence its drain voltage is higher than its source voltage by $1/3V_{IN}$. The bootstrapping capacitor is then connected to the power MOSFET drain to pre-charge. The stacked drivers are powered from the boosted voltage of the bootstrapping capacitor, and therefore, all drivers for all the power MOSFETs are completely powered from the converter internal nodes.

The control logic for the converter is shown in Fig. 5.9. A state machine takes as an input a digital word for the desired operating region and generates outputs that are used to control a group of multiplexers, which in turn generate the three basic control signals for the switches. The 12 control signals are generated from these 3 basic signals with appropriate deadtime added between them. During startup, a ramp V_{IN} is applied to the converter input with $2/3V_{IN}$ and $1/3V_{IN}$ generated through a resistive divider and used to pre-charge the internal bootstrapping capacitors. The startup circuit is deactivated when V_{IN} reaches to 1.8V which is a sufficient voltage for the converter to start

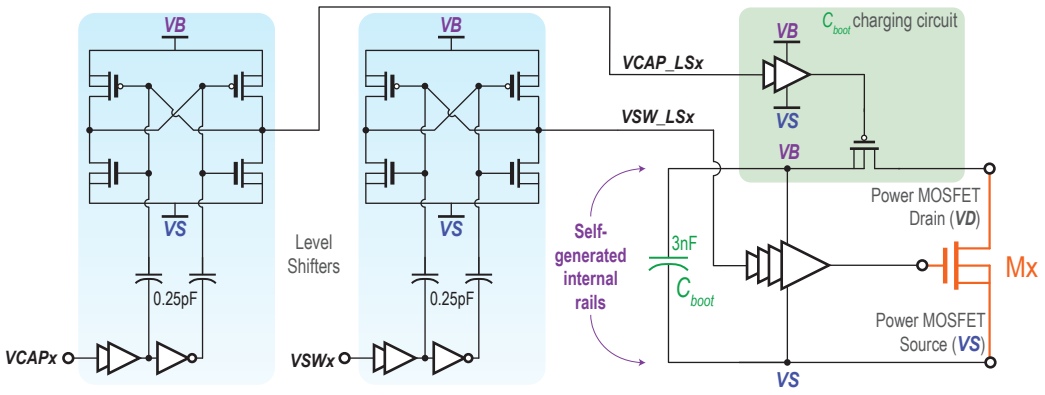
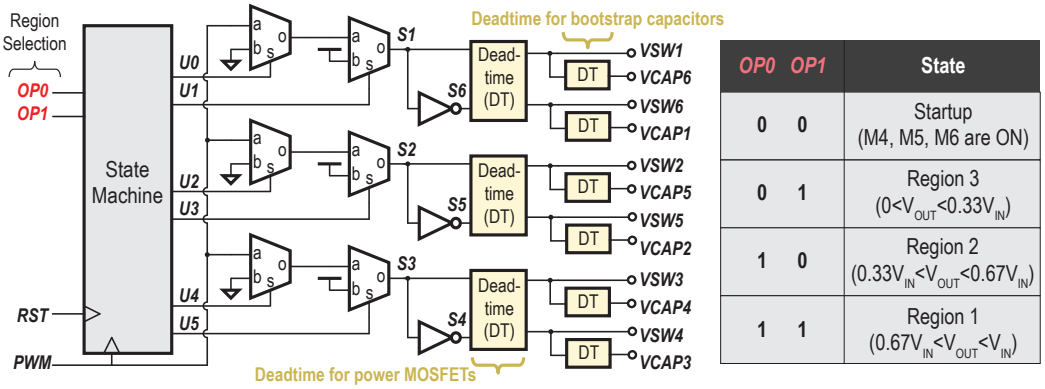


Figure 5.8: Level shifters and power transistor driver circuits.



OP0	OP1	State
0	0	Startup (M4, M5, M6 are ON)
0	1	Region 3 ($0<V_{OUT}<0.33V_{IN}$)
1	0	Region 2 ($0.33V_{IN}<V_{OUT}<0.67V_{IN}$)
1	1	Region 1 ($0.67V_{IN}<V_{OUT}<V_{IN}$)

Figure 5.9: PWM-based control generation circuits illustrating operation across all three output regions.

switching normally.

5.5 Measurement Results

The converter is implemented in standard 180nm CMOS, with a die area of 2.6x2.8mm^2 as illustrated in Fig. 5.10. The chip is flip-chip bonded to an interposer, where a 220 nH inductor (DCR = 19m Ω), three 0402 10 μF flying capacitors, and two 0201 4.7 μF output capacitors are soldered within the chip boundary on the backside of the interposer as shown in Fig. 5.11. Since the input current is continuous and inherently filtered by the input inductors, no input decoupling capacitance is required. The internal

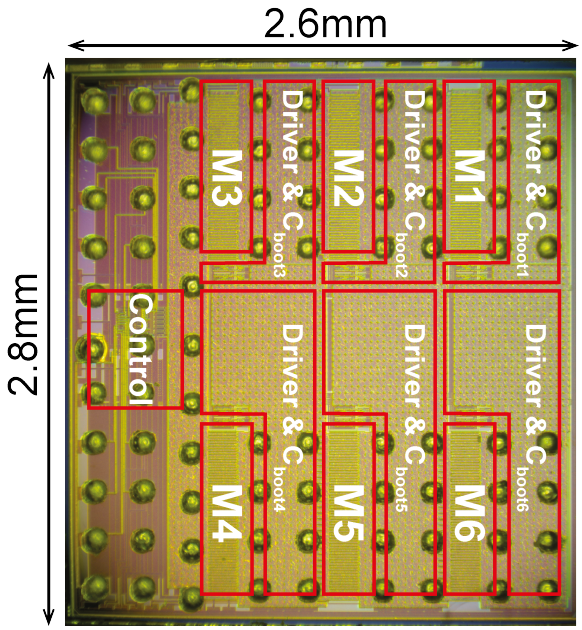


Figure 5.10: Die photo with the main circuit blocks highlighted.

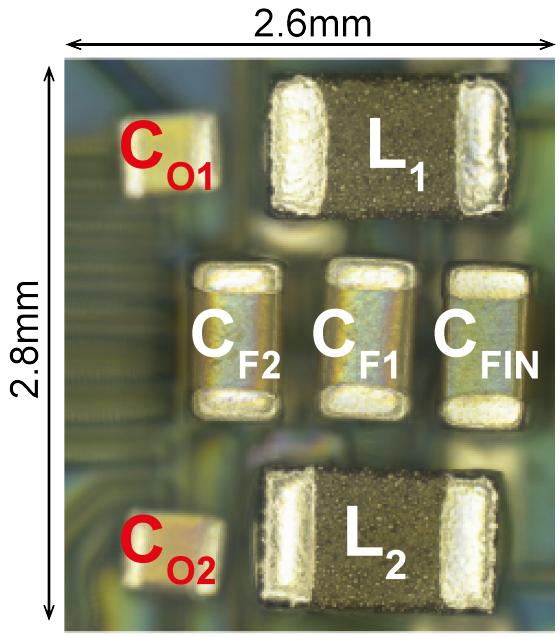


Figure 5.11: Passives assembled on the backside of the interposer.

nodes of the converter, namely V_{X1} and V_{X2}, switch at 9 MHz. Measured efficiency curves are shown in Fig. 5.12, indicating peak efficiencies of 97.1% and 95% at V_{IN}

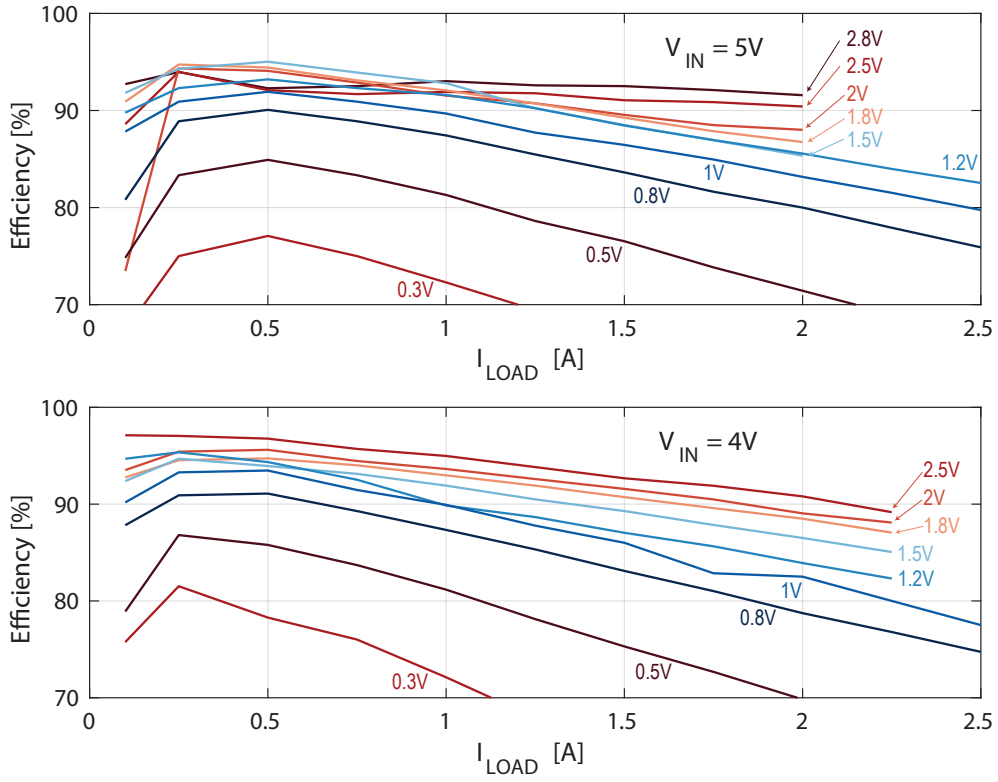


Figure 5.12: Measured efficiency curves across load current for various output voltages, for V_{IN}=5V (top) and V_{IN}=4V (bottom).

= 4 V and 5 V, respectively. The converter achieves a peak area-based power density of 0.77 W/mm^2 (or a volumetric power density of 0.43 W/mm^3) at an efficiency of 91.6%. The converter can operate with a large conversion ratio of up to 16.7× while still providing an efficiency of 77.1%.

Fig. 5.13 shows steady-state waveforms of the internal nodes V_{F2N} and V_{F2P} demonstrating operation across all three regions with correct and balanced voltage levels. A type-III compensated closed loop controller is implemented, and load step response curves with ΔIL = 1.2 A show a response and settling time of ¡2μs and ¡20μs, respectively, as demonstrated in Fig. 5.14. Fig. 5.14 also shows measured input voltage ripples compared with a commercial conventional buck converter under a similar test setup and loaded with 1.2 A, where ¿3× reduction in the input voltage ripple is demonstrated thanks to the continuous input current.

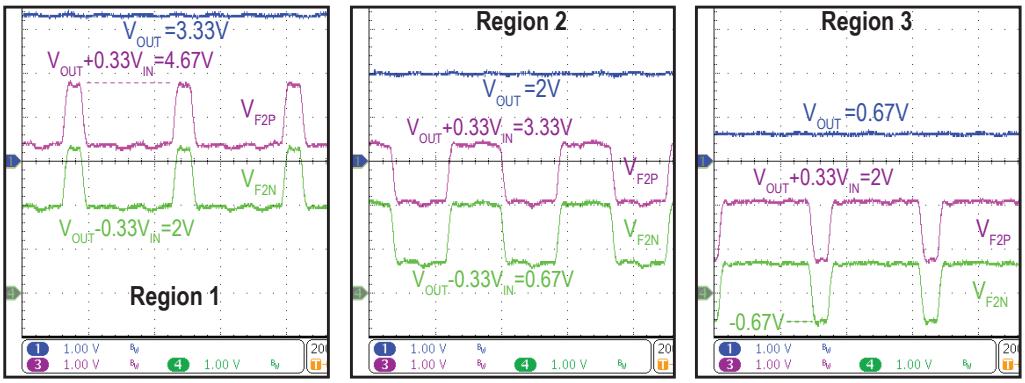


Figure 5.13: Measured converter steady-state waveforms in all three regions of operation.

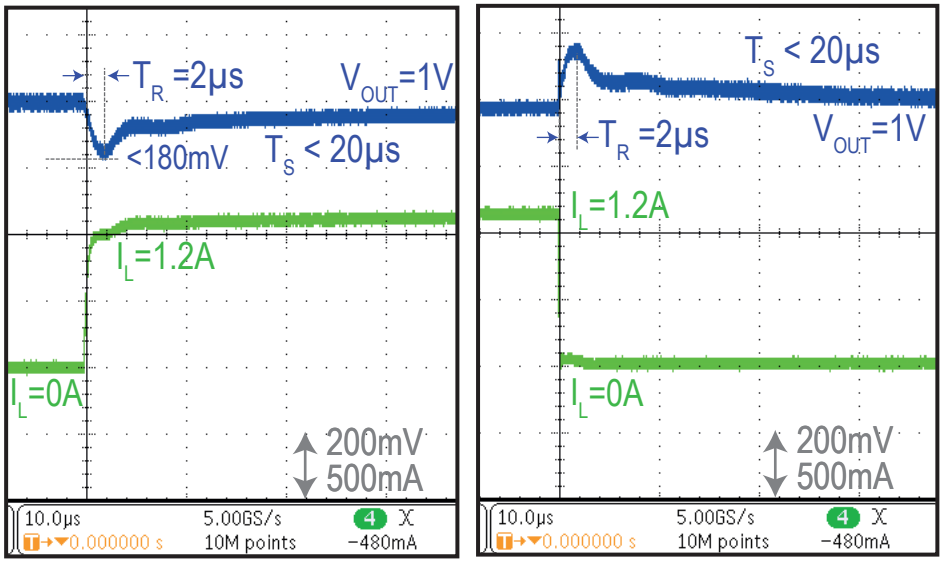


Figure 5.14: Measured closed-loop control load step response.

Table 5.1 and Fig. 5.16 summarize the performance of the converter in comparison to state-of-the-art, where it achieves the highest power density and peak efficiency amongst prior Li-ion-compatible work. summarizes the performance of the converter. Unlike some prior art, the large range of conversion ratios ensures the proposed converter can generate a full range of output voltages operating across the entire input Li-ion battery voltage range, even at the low end of battery voltages. In addition, the continuous input current provides inherent filtering towards reducing EMI which is one of the top concerns for many PMIC customers.

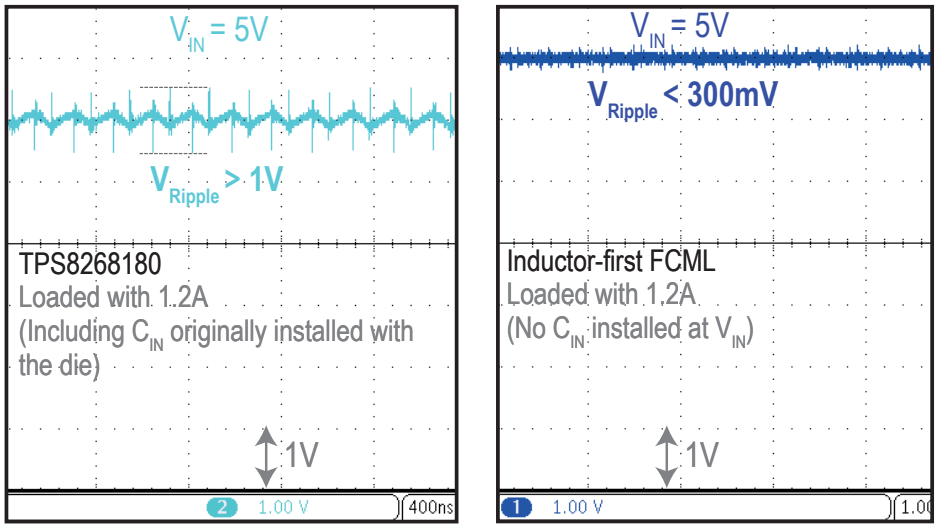


Figure 5.15: comparison of V_{IN} voltage ripple between TPS8268180 and the inductor-first FCML converter.

5.6 Conclusion

An inductor-first FCML converter was introduced. The proposed converter combines the benefits of an inductor-first topology (inductors processing continuous current on the low-current side of the converter) with an FCML topology (Li-ion battery compatibility with low-voltage transistors, and reduced inductor size). The design operates across the entire Li-ion battery range, and achieves a power density of 0.77W/mm^2, and a peak efficiency of 97.1%.

5.7 Acknowledgement

Chapter 5 is based on and mostly a reprint of the following publications:

- A. Abdulslam and P. P. Mercier, "A Battery-Connected Inductor-First Flying Capacitor Multilevel Converter Achieving 0.77 W/mm^2 and 97.1% Peak Efficiency," *IEEE Custom Integrated Circuits Conference (CICC)*, 2021, pp. 1-4.

The dissertation author is the primary investigator and author of the work in these papers.

Table 5.1: Comparison to prior-art Li-ion compatible buck converters and continuous-conversion-ratio hybrid converters.

	Intel EN6310QI	TI TPS8268180	Liu, ISSCC'17	Li, JSSC'19	Schaef, ISSCC'19	Abdulslam, JSSC'20	Rentmeister, CICC'20	This Work		
Structure	Buck	Buck	Hybrid (4:1 Dickon)	Hybrid (Stacked resonant)	Hybrid (4L FCML)	Hybrid (4L Ladder)	Hybrid (5L FCML)	*Hybrid (Inductor-first FCML)*		
Process	NR	NR	65nm	150nm	22nm	180nm	180nm	*180nm*		
Input Voltage [V]	2.7 - 5.5	2.3 - 5.5	3.0 – 4.5	3.2 – 4.2	5	3.0 – 5.0	5.5	*2.0 – 5.0*		
Output Voltage [V]	0.6 – 3.3	1.8	0.3 – 1.0	0.8 – 1.5	1.8	0.3 – 1.2	0.4 – 1.2	*0.3 - 4.8*		
Output Voltage Range	Full	Full	Limited	Limited	Full	Limited	Limited	***Full***		
Total Converter Area [mm^2]	20	6.67	6†	14.4	75.66	5.5	10	*7.3*		
Inductor	NR	NR	180 nH (Discrete)	3 x 4.2 nH (PCB Trace)	10 nH	220 nH (Discrete)	240 nH (Discrete)	*2 X 220 nH (Discrete)*		
Flying Capacitor	N/A	N/A	3 x 22 µF (Ceramic 0402)	6 x 0.47 µF (Ceramic 01005)	2 x 13.2 µF	4 x 1 µF (Ceramic 0402)	3 x 4.7 µF (Ceramic 0402)	*3 x 10 µF (Ceramic 0402)*		
Output Capacitor	NR	NR	22 µF (Ceramic 0402)	20 nF (On-chip)	18.8 µF (part of load)	1 µF (Ceramic 0402)	10 µF (Ceramic 0402)	*2 x 4.7 µF (Ceramic 0201)*		
Input Current	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	***Continuous***		
External rails for drivers?	NO	NO	YES	NO	YES	NO	NO	***NO***		
Peak Power Density per Total Volume [W/mm^3]	0.027	0.43	NR	NR	0.198	0.23	NR	***0.43***		
Peak Power Density per Total Area [W/mm^2]	0.05†	0.43†	0.22†,††	0.11	0.24	0.52	0.10	***0.77***		
@ Efficiency	79%†	78%†	64%†,††	83.4%	89.4%	72%	84%†	***91.6%***		
Peak Efficiency (PE)	84%†	84%†	90%†,††	87.2%	93.8%	90%	92.4%	***97.1%***	***95%***	***91.9%***
Power Density [W/mm^2] @ PE	0.02†	0.175†	0.04†,††	0.083†	0.071	0.11	0.03†	*0.03*	*0.1*	*0.07*
@ V_{IN}, conv. ratio	5V, 5	5V, 2.8	4.2V, 5.2	3.8V, 3.2	5V, 2.8	4.2V, 3.8	5V, 4.2	*4V, 1.6*	*5V, 3.3*	*5V, 5*
Peak Efficiency @ max. conv. ratio	NR	84%† @ 2.8	75% @ 9.7	70%† @ 4.5	87.5%† @ 6.3	74% @ 16.7	80.2% @ 13.75	***77.1% @ 16.7***		

† Estimated from plotted data †† Using a 180nH inductor N/A – Not Applicable NR – Not Reported

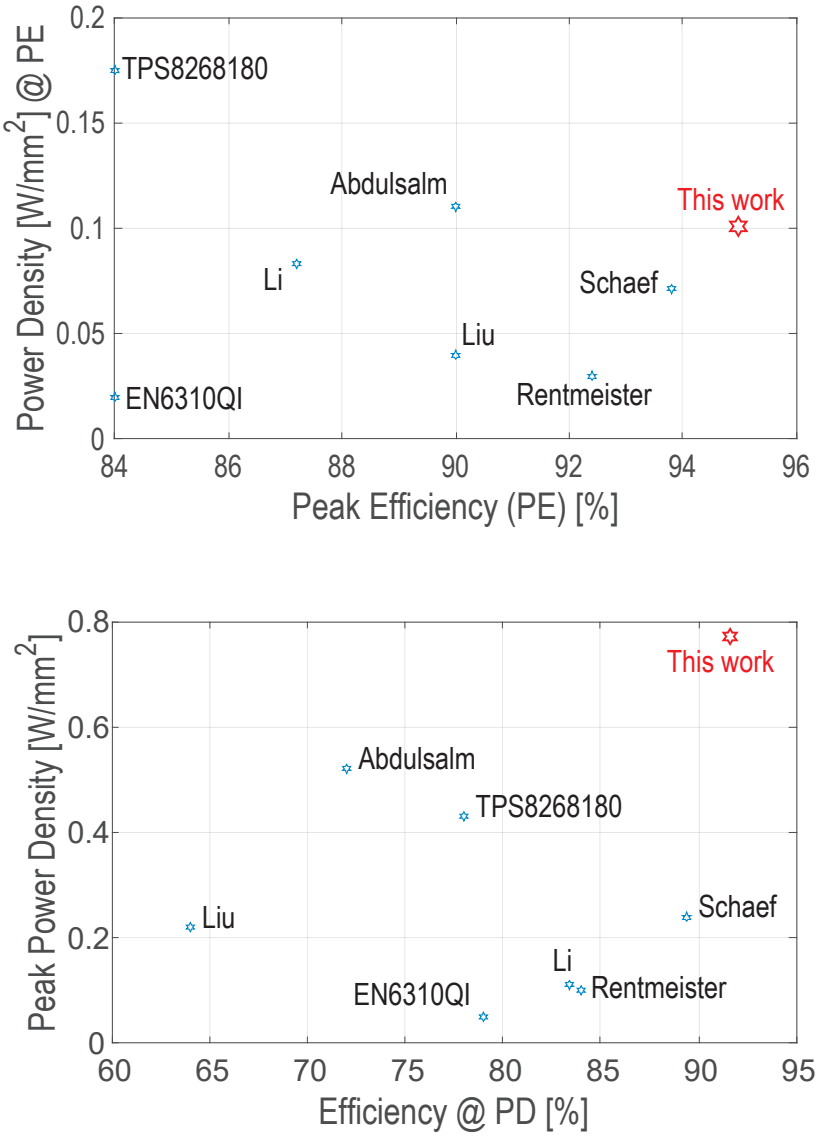


Figure 5.16: Measured peak efficiency and peak power density vs. their corresponding operating points with a comparison to prior work.

Chapter 6

Conclusion

In this thesis, new topologies and techniques were developed to address recent challenges in DC-DC converters used in modern mobile devices.

In the first part of the thesis, an inductor-first 3rd order buck converter was introduced in chapter 2 that has loss-related, noise-related and structure-related benefits as compared to a conventional buck converter. Specifically, all the passives including two inductors are stacked in a packaging-friendly manner at the PS3B converter input, allowing for the inductors to process lower current than a conventional buck converter while inherently filtering input current noise. A prototype shows that the converter achieves a peak efficiency of 94% and a peak power density of 0.7 W/mm^2. Chapter 3 demonstrated that a pragmatic charge recycling of the gate charges of the power MOSFETs can be achieved with recycling efficiencies of up to 80%. The charge recycling technique was applied to an inductor-first buck converter without affecting the circuit control law or the output regulation. A prototype for this technique achieves a state-of-the-art peak efficiency of 98.2% and a power density of 0.72W/mm^2. Thanks to the recycling technique, the efficiency is generally improved over a wide range of load currents, and specially at light load currents with still 88.4% efficiency even at 1% of the maximum load current.

Chapter 4 presented a symmetrical modified multilevel ladder (SMML) converter that can operate from Li-ion battery voltages and provide continuous conversion ratios down to SoC-compatible voltages. The converter offers reduced conduction losses, flying capacitors that are naturally balanced, and no need for external supplies for drivers or level shifters, which topologically solves important challenges in baseline

multi-level converters. The converter achieves state-of-the-art power density at high efficiencies, where it can provide conversion ratios up to 16.7 at efficiencies $> 74\%$.

Chapter 5 presented an inductor-first FCML converter was introduced. The proposed converter combines the benefits of an inductor-first topology (inductors processing continuous current on the low-current side of the converter) with an FCML topology (Li-ion battery compatibility with low-voltage transistors, and reduced inductor size). The design operates across the entire Li-ion battery range, and achieves a power density of 0.77W/mm^2, and a peak efficiency of 97.1%.

Fig. 6.1 provides a summary for the contribution made in this thesis where all or most of the DC-DC converter challenges presented in the introduction chapter were addressed through the introduced topologies and techniques.

As a future work, the use of the inductor-first topology can be further explored for other applications like automotive and industrial applications where EMI and noise is a top concern and the continuous input current feature of the inductor-first topology would be an outstanding merit. The prototypes of the inductor-first buck converter presented in this thesis are always operating in the continuous conduction mode (CCM). Operating the inductor-first buck converter topology in the discontinuous conduction mode can be investigated for enhanced light load efficiency. It is worth noting that the charge recycling technique presented in chapter 3 can still be applied on top of a DCM mode resulting in an even more enhanced light load efficiency. A charge recycling technique similar to that presented in chapter 2 can be applied to buck converters by still using one inductor although this would require more switches that might hinder the charge recycling efficiency but it is still worth investigating.

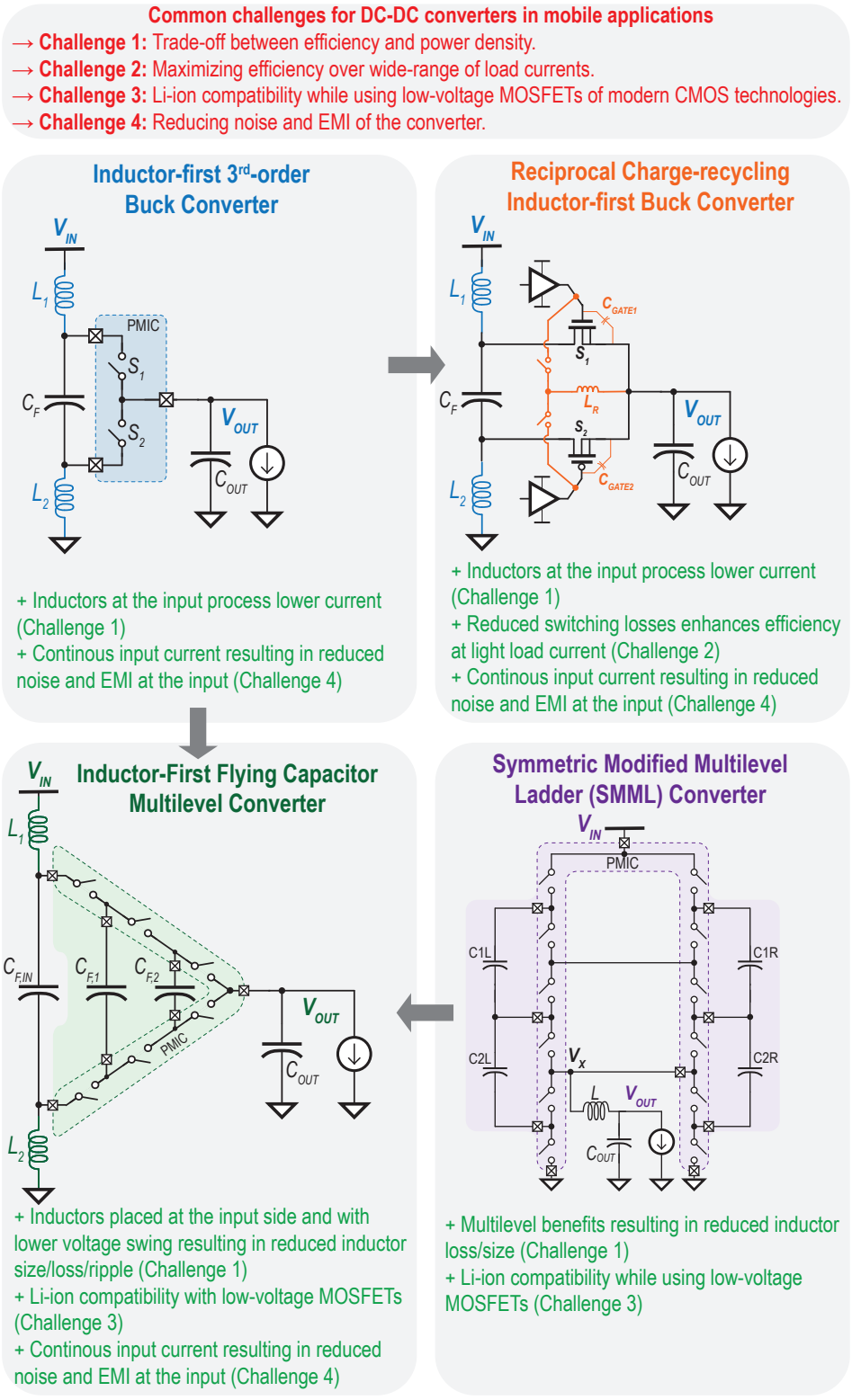


Figure 6.1: Summary of the thesis contribution.

Appendix A

A General Analytical Model to Design and Evaluate Multilevel DC-DC Converters

Multilevel hybrid converters can be realized using different switched capacitor (SC) topologies. Each SC topology can lead to a multilevel converter of a different performance and different characteristics. In order to compare between the performance of these topologies, a general model for analyzing the losses in multilevel converters is needed. However, analyzing the losses in multilevel hybrid converters can be complex due to the relatively high number of passive and active components used in these converters in addition to the multi-phase operation.

In this appendix, a general loss model for multilevel converters is developed that takes into account all the dominant losses in a multilevel converter including the conduction and the switching losses of the switches as well as the losses related to the capacitors and the inductors. The developed model can be used to first optimize the design of a single multilevel topology, and then compare between different optimized multilevel topologies for a given application and a target technology. The model derivation is done in section A.1 where the losses is analyzed based on some characterizing matrices that can be easily extracted for any single SC topology. Some common SC topologies that can be used to build a multilevel converter are investigated in section A.2 where their characterizing matrices are presented. A comparison between these SC topologies when used to build a multilevel converter is performed in section A.3 for an example Li-ion-to-SoC application.

A.1 Model Derivation

Generally, a multilevel hybrid DC-DC converter consists of a switched capacitor (SC) circuit, generating a switching voltage waveform (V_X), followed by an inductor and an output decoupling capacitor, forming a low pass filter at the converter output as shown in Fig. A.1.

Some multilevel converters, like FCML topology, can have multiple operating regions depending on the two level of the switching waveform (V_X). A general relation to calculate the output voltage (V_{OUT}) in any operating region is given by:

$$V_{OUT} = V_2 + D \times (V_1 - V_2), \tag{A.1}$$

where V_1 and V_2 are the higher and the lower voltage levels of the switching node (V_X), respectively, and D is the duty cycle of the switching node (V_X).

In this analysis. the multilevel converter is assumed to be operating in the region providing the highest conversion ratio between V_{IN} and V_{OUT} which is the region of concern in most SoC applications. The current flowing in the output inductor current has an average value equal to the load current I_{LOAD} with a current ripple imposed on top of this DC value due to the switching voltage at the inductor input. The peak-to-peak current ripple in the inductor is given by:

$$\Delta I = \Delta V \frac{D(1-D)}{L \times F_{SW}} \tag{A.2}$$

where ΔV is the voltage difference between the two levels of the switching node ($\Delta V = V_1 - V_2$), D is the duty cycle of the switching node (V_X), L is the inductor value, and F_{SW} is the switching frequency of the V_X node (which is not necessarily the switching frequency of the individual MOSFETs).

During each operating phase of the SC circuit. the continuous current in the inductor is delivered through one or more parallel paths starting from the converter input rails and going through the switches and the capacitors that are configured to be ON

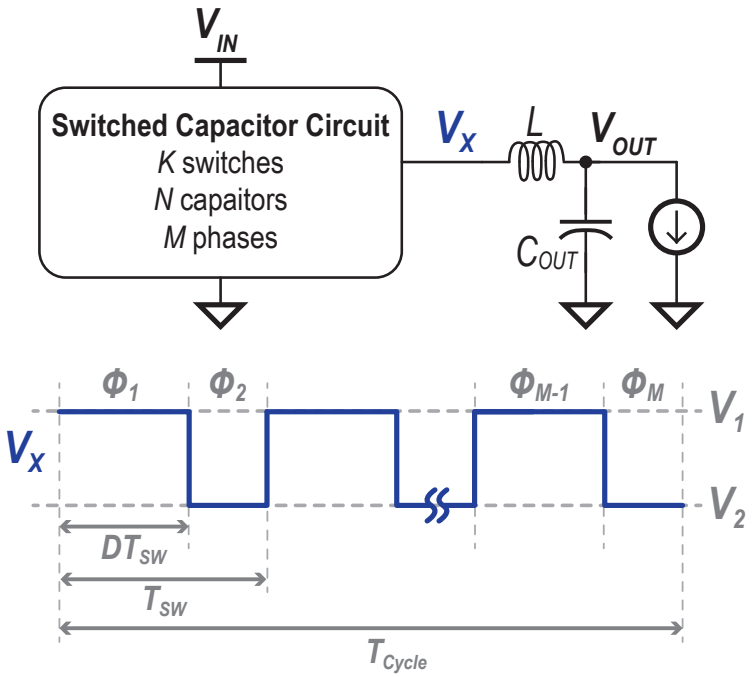


Figure A.1: General structure of a multilevel hybrid DC-DC converter.

during that phase. Therefore, the current flowing through each of these switches or flying capacitors is equal to or is as a portion of the inductor current, assuming there is no internal charge sharing occurring between the flying capacitors as an approximation. The average current flowing through each capacitor during all the phases should be equal to zero so that this flying capacitor is ideally balanced at a certain voltage. This portion of the inductor current flowing through each power MOSFET or each flying capacitor can be used to calculate the conduction losses in these elements. The dominant losses in a multilevel converter under normal operation are the MOSFET conduction losses, the MOSFET switching losses, the flying capacitor losses, and the inductor losses, which are all modeled in the following subsections.

MOSFET Conduction Losses

For a SC topology that has a total of K switches and M phases, the switch conduction losses are given by:

$$P_{Cond} = \left(I_L^2 + \frac{\Delta I^2}{12}\right) \sum_{\substack{1 \le i \le M \\ 1 \le j \le K}} a(i,j)^2 R_j \left(\frac{T_i}{T_{Cycle}}\right) \tag{A.3}$$

where I_L represents the load current, R_j represents the on-resistance of switch S_j, T_i represents the time duration of the phase ϕ_i, and T_{Cycle} represents the total duration of the N phases of the converter. Resistance R_j can be defined as ($r_{ON} \times W_j$), where W_j is the width of switch S_j and r_{ON} is the switch on-resistance per unit width.

T_{Cycle} represents the duration of one switching sequence which includes all the M phases of the SC circuit, and is typically equal to multiples of the switching period of the inductor (T_{SW}). The coefficient $a(i,j)$ represents the percentage of the inductor current going through switch S_j in phase ϕ_i. Each individual coefficient $a(i,j)$ is an element in a $M \times K$ matrix $\mathbf{A}$, and is given by:

$$\mathbf{A} = \begin{array}{c} \\ \phi_1 \\ \phi_2 \\ \vdots \\ \phi_M \end{array} \begin{array}{c} \begin{array}{cccc} S_1 & S_2 & \dots & S_K \end{array} \\ \begin{bmatrix} a(1,1) & a(1,2) & \dots & a(1,K) \\ a(2,1) & a(2,2) & \dots & a(2,K) \\ \vdots & \vdots & \ddots & \vdots \\ a(M,1) & a(M,2) & \dots & a(M,K) \end{bmatrix} \end{array} \tag{A.4}$$

.

For example, the current going through switch S_3 in phase Φ_1 is [$a(1,3) \times I_{IND}$], where I_{IND} is the inductor current. By using (A.3) along with the matrix $\mathbf{A}$, the total conduction losses in all the MOSFETs can be calculated.

MOSFET Switching Losses

MOSFET switching losses occur due to the charging/discharging of each MOSFET's parasitic capacitances: C_D, C_G, and C_J, which represents the drain-to-source, gate-to-source, and the junction parasitic capacitance, respectively. To represent these losses in a systematic way, characterizing matrices for the voltage on these parasitic capacitors are developed. When a MOSFET switch turns ON/OFF, its blocking voltage, V_D, changes from the maximum value to zero or vice versa. This change in V_D results in the charging/discharging losses of C_D. V_D of each MOSFET can be represented in the following matrix:

$$\mathbf{V_D} = \begin{array}{c} \\ \phi_1 \\ \phi_2 \\ \vdots \\ \phi_M \end{array} \begin{array}{c} \begin{array}{cccc} S_1 & S_2 & \dots & S_K \end{array} \\ \begin{bmatrix} v_d(1,1) & v_d(1,2) & \dots & v_d(1,K) \\ v_d(2,1) & v_d(2,2) & \dots & v_d(2,K) \\ \vdots & \vdots & \ddots & \vdots \\ v_d(M,1) & v_d(M,2) & \dots & v_d(M,K) \end{bmatrix} \end{array}. \tag{A.5}$$

Here, $\mathbf{V_D}$ is a $M \times K$ matrix where each element, $v_d(i,j)$, is the blocking voltage on switch (S_j) in phase (Φ_i), as a fraction of V_{IN}. When a MOSFET switch is ON, its corresponding $v_d(i,j)$ is zero.

Similarly, the gate-to-source voltage or the overdrive voltage for a switching MOSFET changes from 0 to the maximum drive voltage or vice versa. To calculate the switching losses of each MOSFET, a matrix $\mathbf{V_G}$ can be used to indicate the status of

each MOSFET in each operating phase as follows:

$$\mathbf{V_G} = \begin{array}{c} \\ \phi_1 \\ \phi_2 \\ \vdots \\ \phi_M \end{array} \begin{array}{c} \begin{array}{cccc} S_1 & S_2 & \dots & S_K \end{array} \\ \begin{bmatrix} v_g(1,1) & v_g(1,2) & \dots & v_g(1,K) \\ v_g(2,1) & v_g(2,2) & \dots & v_g(2,K) \\ \vdots & \vdots & \ddots & \vdots \\ v_g(M,1) & v_g(M,2) & \dots & v_g(M,K) \end{bmatrix} \end{array}. \tag{A.6}$$

Additionally, changes in the absolute value of the MOSFET source voltage results in charging/discharging of the parasitic junction capacitor, C_J, between the source terminal of a MOSFET and the chip bulk. A $\mathbf{V_S}$ matrix represents the MOSFET source voltage in each phase, as a fraction of V_{IN}, and can be given by:

$$\mathbf{V_S} = \begin{array}{c} \\ \phi_1 \\ \phi_2 \\ \vdots \\ \phi_M \end{array} \begin{array}{c} \begin{array}{cccc} S_1 & S_2 & \dots & S_K \end{array} \\ \begin{bmatrix} v_s(1,1) & v_s(1,2) & \dots & v_s(1,K) \\ v_s(2,1) & v_s(2,2) & \dots & v_s(2,K) \\ \vdots & \vdots & \ddots & \vdots \\ v_s(M,1) & v_s(M,2) & \dots & v_s(M,K) \end{bmatrix} \end{array}. \tag{A.7}$$

By using the aforementioned matrices, the total switching loss of the MOSFETs (P_{SW}) can be given by:

$$\begin{aligned} P_{SW} = & \frac{0.5}{T_{Cycle}} V_{IN}^2 F_{SW} \sum_{\substack{1 \le i \le M \\ 1 \le j \le K}} \Delta v_d(i,j)^2 C_{D,j} \\ & + \frac{0.5}{T_{Cycle}} V_D^2 F_{SW} \sum_{\substack{1 \le i \le M \\ 1 \le j \le K}} \Delta v_g(i,j)^2 C_{G,j} \\ & + \frac{0.5}{T_{Cycle}} V_{IN}^2 F_{SW} \sum_{\substack{1 \le i \le M \\ 1 \le j \le K}} \Delta v_s(i,j)^2 C_{J,j}, \end{aligned} \tag{A.8}$$

where $\Delta v_d(i,j)$ represents the difference between a MOSFET blocking voltage in the

current phase (ϕ_i) and the MOSFET blocking voltage in the preceding phase (ϕ_{i-1}) (i.e., $v_d(i,j) - v_d(i-1,j)$), which is calculated using the $\mathbf{V_D}$ matrix. $\Delta v_d(i,j)$ will be zero if the switch remains ON or OFF when transitioning from ϕ_{i-1} to ϕ_i. Similarly, $\Delta v_s(i,j)$ represents the difference between the MOSFET source voltages when going from one phase to the next and is calculated using the $\mathbf{V_S}$ matrix. The parasitic capacitors $C_{D,j}$, $C_{G,j}$, and $C_{J,j}$ of a switch S_j are assumed to scale linearly with the switch width for simplicity.

Inductor and Capacitor Losses

The conduction loss in the inductor, which has a DC resistance of DCR, is given by:

$$P_{Inductor} = \left(I_L^2 + \frac{\Delta I^2}{12} \right) \times DCR. \tag{A.9}$$

For a SC capacitor circuit with K capacitors, the conduction loss due to the equivalent series resistance (ESR) of the flying capacitors is given by:

$$P_{Capacitor} = \left(I_L^2 + \frac{\Delta I^2}{12} \right) \sum_{\substack{1 \le i \le M \\ 1 \le j \le K}} (c_{i,j})^2 ESR_j (\frac{T_i}{T_t}), \tag{A.10}$$

where $c_{i,j}$ is an element of a M-by-K matrix, $\mathbf{B}$, that represents the percentage of the inductor current going through each of the flying capacitors. $\mathbf{B}$ is given by:

$$\mathbf{B} = \begin{array}{c} \\ \phi_1 \\ \phi_2 \\ \vdots \\ \phi_M \end{array} \begin{array}{c} \begin{array}{cccc} C_1 & C_2 & \dots & C_K \end{array} \\ \begin{bmatrix} b(1,1) & b(1,2) & \dots & b(1,K) \\ b(2,1) & b(2,2) & \dots & b(2,K) \\ \vdots & \vdots & \ddots & \vdots \\ b(M,1) & b(M,2) & \dots & b(M,K) \end{bmatrix} \end{array} \tag{A.11}$$

Total Losses

By combining the losses of the individual components, the total losses of the converter can be given by:

$$\begin{aligned} P_{Losses} = P_{Cond} + P_{SW} + P_{Inductor} \\ + P_{Capacitor}. \end{aligned} \tag{A.12}$$

P_{Losses} represents the total losses of the converter at a given operating point and is a function of the switching frequency, F_{SW}, and switch sizes, W_j.

Design Optimization

To minimize the converter losses, the design parameters to be optimized are the switching frequency and the switch widths. If the switching frequency is predetermined according to some other design considerations, like the transient response and the output ripple, the switch widths are the only parameters to be optimized for minimum losses. Each of the 12 switches in the SMML topology has its corresponding conduction and switching losses, which are a function in the switch width, and are calculated as:

$$P_{switch,j} = \left(I_L^2 + \frac{\Delta I^2}{12} \right) \frac{\alpha}{W_j} + F_{SW} W_j \beta. \tag{A.13}$$

α and β are two coefficients related to the conduction and the switching losses of switch S_i throughout the four phases, respectively, and are given by:

$$\begin{aligned} \alpha_i &= \sum_{1 \le i \le M} a(i,j)^2 (\frac{T_i}{T_t}) r_{ON} \\ \beta_i &= \sum_{1 \le i \le M} \left(V_{IN}^2 \Delta v_d(i,j)^2 c_D + V_D^2 \Delta v_g(i,j)^2 c_G + V_{IN}^2 \Delta v_s(i,j)^2 c_J \right), \end{aligned} \tag{A.14}$$

where r_{ON}, c_D, c_G, and c_J are the switch on-resistance, drain capacitance, gate capacitance, and junction capacitance, all per unit width. By differentiating the total switch

losses with respect to the switch width W_j, and equating to zero, the optimum width for each MOSFET can be found as:

$$W_{opt,j} = \sqrt{\left(I_L^2 + \frac{\Delta I^2}{12}\right) \frac{1}{V_{IN}^2 F_{SW}} \frac{\alpha}{\beta}}, \tag{A.15}$$

where $W_{opt,j}$ is the optimum width of switch j at a given switching frequency and operating point (i.e. V_{OUT} and I_{LOAD}). If a comprehensive optimization of the converter that includes both the switching frequency and the switch sizes as design parameters is desired, the equations derived in this section can be used in an optimization process by the help of some analysis tools, for example, MATLAB.

It is worth noting that all the optimum width of each power MOSFET is dependent on the load current and it actually changes as the load current changes.

A.2 Characterization of Multilevel Topologies

Common SC topologies used to build a conventional SC converter are FCML, ladder, Dickson, series-parallel, and the SMML topology presented in chapter 4. In this section, these topologies are investigated when used to build a multilevel hybrid converter. Additionally, the characterizing matrices of the switches and the capacitors of each topology are derived. These matrices can be applied directly to the general model of the previous section to analyze the losses in each of these topologies and optimize their design accordingly.

A.2.1 FCML Topology

The flying capacitor multilevel (FCML) topology is a common SC topology and one of the earliest topologies used to build multilevel DC-DC converters. Fig. A.2 shows the topology schematic when used to build a multilevel converter along with the switch status in each operating phase and the required blocking voltage on the capacitors

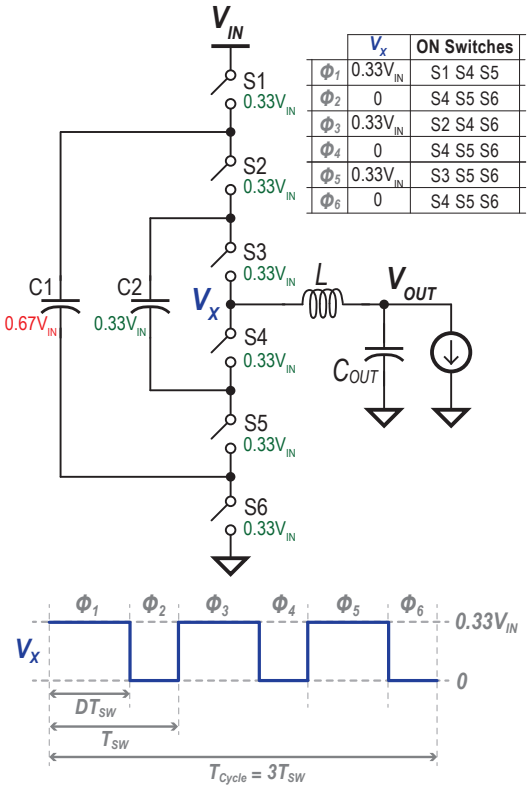


Figure A.2: FCML multilevel topology illustrating the operating phases and the switch configuration in each of these phases.

and the switches. The converter is assumed to be operating in the lowest region where the V_X waveform is switching between $0.33V_{IN}$ and zero, providing an output voltage between these two levels depending on the duty cycle of V_X. In this operating region, a one operating cycle contains six phases where the switch configuration in each of these phases is shown in Fig. A.2.

Regarding the switch voltage rating, one of the features of this topology is that all the switches have a minimum blocking voltage of $0.33V_{IN}$ on them and hence, no additional stacking is needed if appropriate low-voltage MOSFETs are employed. To analyze the losses in this topology, the characterizing matrices of the switches are given

by:

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix}, \mathbf{V_D} = \begin{bmatrix} \frac{1}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ 0 & \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \end{bmatrix},$$

$$\mathbf{V_G} = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 1 & 1 \end{bmatrix}, \mathbf{V_S} = \begin{bmatrix} \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ \frac{2}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 \\ 1 & \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 \\ \frac{2}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 \\ \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 \\ \frac{2}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 \end{bmatrix}.$$

For the voltage rating of the flying capacitors, one flying capacitor, C1, require a blocking voltage of $0.67V_{IN}$ which is higher than the topology minimum blocking voltage of $0.33V_{IN}$. This higher blocking voltage on C1 can translate to a larger implementation area of this capacitor.

One attractive feature of this topology is that it can cover the full output voltage range (i.e., $0 < V_{OUT} < V_{IN}$) without the need for additional switches or capacitors to be added to the topology. In addition, it can switch almost seamlessly between different regions by changing the levels of the V_X waveform. This wide output range is an important feature not existent in most of the other multilevel topologies. This feature becomes especially important if the input voltage is dropping too low while the output voltage needs to be regulated at a voltage larger than $0.33V_{IN}$ which can be the case in some Li-ion-to-SoC applications.

To analyze if the flying capacitors in the FCML topology are naturally balanced, the V_X node is assumed to be floating since it is decoupled from the V_{OUT} node through the output inductor. Kirchhoff's voltage law (KVL) can then be applied to each operating phase of the topology resulting in the following equations:

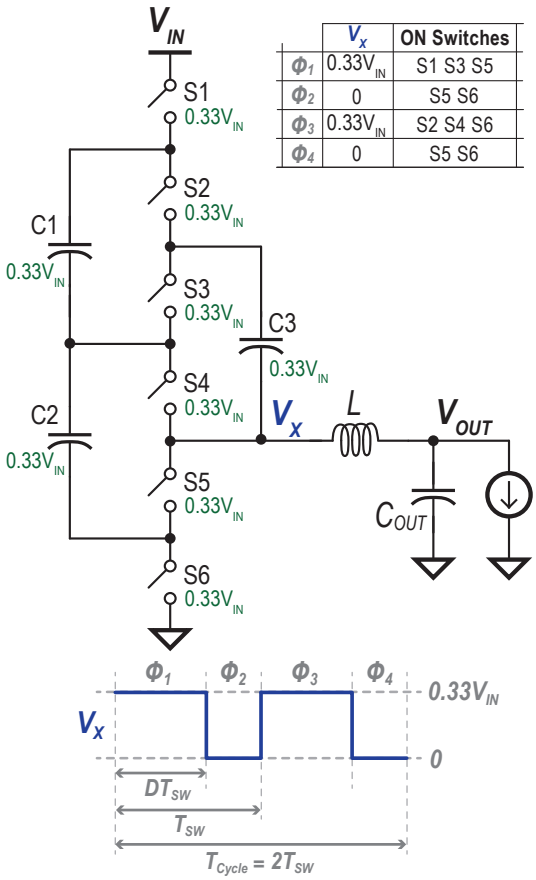
$$\begin{aligned} \phi_1: &\quad V_{IN} - V_{C1} = V_{X1}, \\ \phi_3: &\quad V_{C1} - V_{C2} = V_{X3}, \\ \phi_5: &\quad V_{C2} = V_{X5}, \end{aligned} \tag{A.16}$$

where V_{X1}, V_{X3}, and V_{X5} are the switching node voltage at ϕ_1, ϕ_3, and ϕ_5, which is assumed to be floating in each phase. Since there is no solution for the previous equations, the flying capacitors in the FCML topology are not naturally balanced and capacitor balancing modules are needed for a reliable implementation of the topology. The flying capacitor can be intuitively anticipated since there is no internal charge sharing losses between the flying capacitors of an FCML topology where all the capacitors are soft-charged or soft-discharged. The ESR characterizing matrix for the flying capacitors is given by:

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 \end{bmatrix}^T. \tag{A.17}$$

A.2.2 Ladder Topology

The ladder topology is commonly used to build conventional SC converters and can be used to build a multilevel converter as shown in Fig. A.3. A main advantage of the ladder topology is that all the switches have a minimum blocking voltage of $0.33V_{IN}$ on them and hence, no stacking is needed if appropriate low-voltage MOSFETs are employed. Similarly, all the capacitors have a minimum blocking voltage of $0.33V_{IN}$ on them reducing their implementation area. To analyze the losses in this topology, the



	V_x	ON Switches
Φ_1	$0.33V_{IN}$	S1 S3 S5
Φ_2	0	S5 S6
Φ_3	$0.33V_{IN}$	S2 S4 S6
Φ_4	0	S5 S6

Figure A.3: The ladder SC topology when used to build a multilevel hybrid converter illustrating the operating phases and the switch configuration in each of these phases.

characterizing matrices of the switches are given by:

$$\mathbf{A} = \begin{bmatrix} 1 & 0 & 1 & 0 & 2 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & \frac{1}{2} & 0 & \frac{3}{2} & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}, \mathbf{V_D} = \begin{bmatrix} 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & 0 \\ \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & 0 \end{bmatrix},$$

$$\mathbf{V_G} = \begin{bmatrix} 1 & 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 \\ 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}, \mathbf{V_S} = \begin{bmatrix} 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 \\ \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \\ \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 \\ \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 \end{bmatrix}.$$

In the ladder topology, there is internal charge sharing between the flying capacitors. To analyze if the flying capacitors in the ladder topology are naturally balanced, the V_X node is assumed to be floating. Kirchhoff's voltage law (KVL) can then be applied to each operating phase of the topology resulting in the following equations:

$$\begin{aligned} \phi_1: \quad & V_{C2} = V_{C3} \\ & V_{IN} - V_{C1} - V_{C2} = V_{X1} \\ \phi_3: \quad & V_{C1} = V_{C3} \\ & V_{C2} = V_{X3}, \end{aligned} \tag{A.18}$$

where V_{X1}, and V_{X3} are the switching node voltage at ϕ_1 and ϕ_3, respectively. This KVL analysis shows 4 equations with 5 variables which indicates no solution. This result means the flying capacitors are not forced to their nominal voltages through the internal charge sharing and balancing modules might be needed. The ESR characterizing matrix for the flying capacitors is given by:

$$\mathbf{C} = \begin{bmatrix} 1 & 2 & 1 \\ 0 & 0 & 0 \\ 0.5 & 1 & 0.5 \\ 0 & 0 & 0 \end{bmatrix}. \tag{A.19}$$

A.2.3 SMML Topology

The SMML topology introduced in chapter 4 is included in this comparison. Fig. A.4 shows the topology configuration where V_X is switching between $0.33V_{IN}$ and zero. The topology has four operating phases forming a one cycle. To analyze the losses in

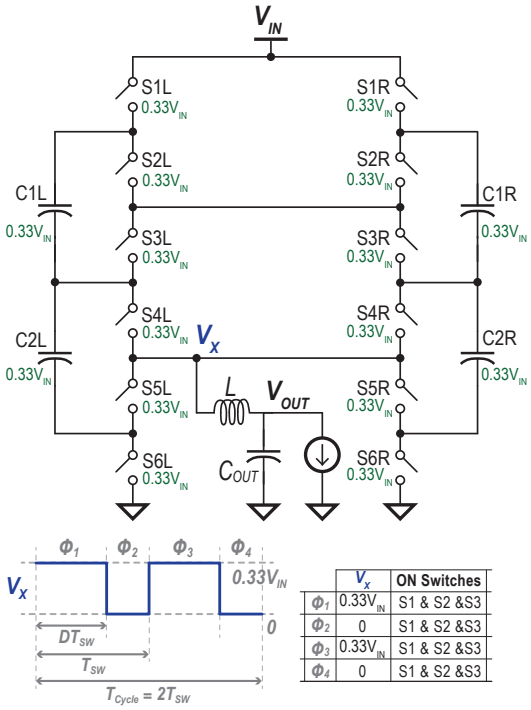


Figure A.4: The SMML topology used as a multilevel hybrid converter illustrating the operating phases and the switch configuration in each of these phases.

this topology, the characterizing matrices of the switches are given by:

$$\mathbf{A} = \left[\begin{array}{cccccc|cccccc} \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{2}{3} & 0 & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{2}{3} \\ 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{2}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{2}{3} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} \end{array}\right],$$

$$\mathbf{V_D} = \left[\begin{array}{cccccc|cccccc} 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 \\ \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & 0 & \frac{1}{3} & 0 & \frac{1}{3} & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 \end{array}\right],$$

$$\mathbf{V_G} = \left[\begin{array}{cccccc|cccccc} 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 \\ 1 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 1 & 1 & 1 & 1 & 0 & 0 & 1 & 1 & 1 & 1 & 0 & 0 \end{array}\right],$$

$$\mathbf{V_S} = \left[\begin{array}{cccccc|cccccc} 1 & \frac{2}{3} & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 \\ 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 & 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 \\ 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 & 1 & \frac{2}{3} & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 \\ 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 & 1 & \frac{2}{3} & \frac{2}{3} & \frac{1}{3} & 0 & 0 \end{array}\right].$$

In the SMML topology, there is internal charge sharing loss between the flying capacitors where the capacitors are either hard-charged or hard-discharged in each operating phase. To analyze if the flying capacitors in the SMML topology are naturally balanced, the V_X node is assumed to be floating since it is decoupled from the V_{OUT} node through the output inductor. Kirchhoff's voltage law (KVL) can then be applied to each operating phase of the topology resulting in the following equations:

$$\begin{aligned} \phi_1: \quad & V_{C1L} + V_{C2L} + V_{C2R} = V_{IN} \\ & V_{C2L} = V_{C1R} \\ \phi_3: \quad & V_{C1R} + V_{C2R} + V_{C2L} = V_{IN} \\ & V_{C1L} = V_{C2R} \end{aligned} \tag{A.20}$$

,

The KVL in each phase resulted in 4 equations with 4 variables. Solving these equations yields:

$$V_{C1L} = V_{C2L} = V_{C1R} = V_{C2R} = \frac{1}{3}V_{IN}. \tag{A.21}$$

This result indicates that the flying capacitors in the SMML topology are naturally balanced at their nominal voltages and this balancing is enforced phase by phase. There-

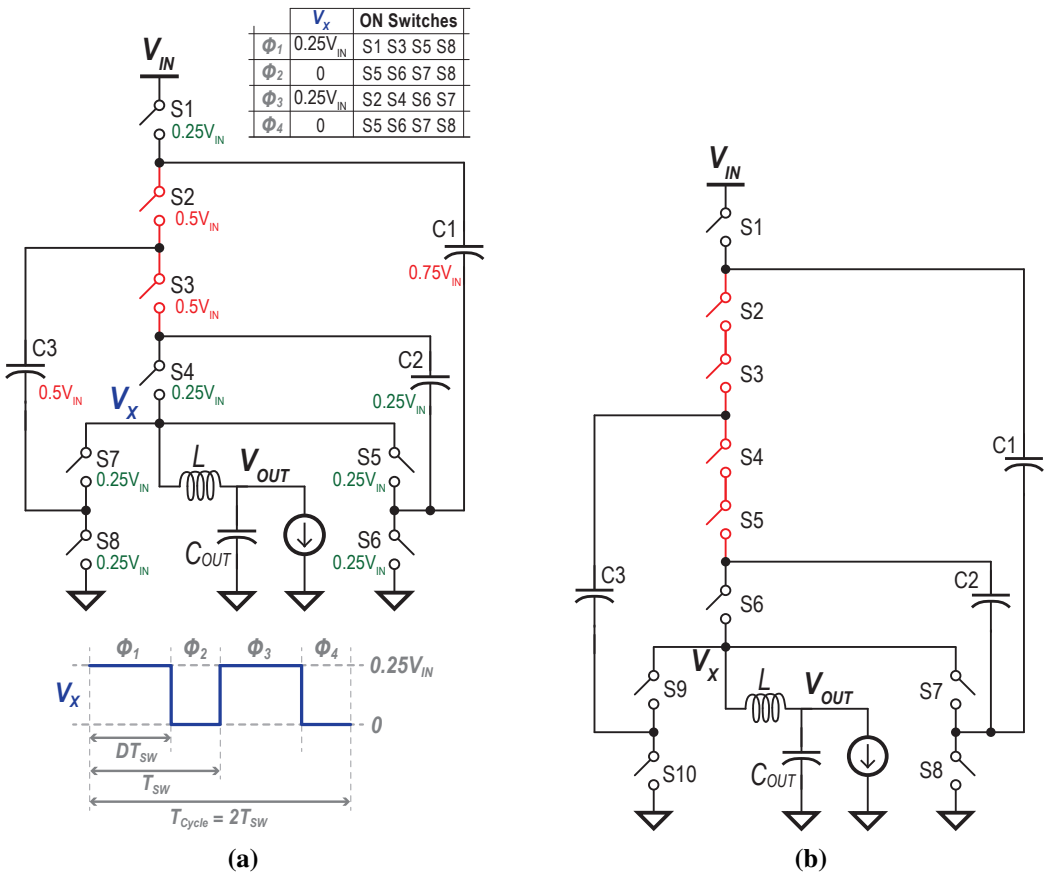


Figure A.5: (a) Dickson SC topology when used to build a multilevel hybrid converter. (b) Dickson multilevel converter with stacked switches to reduce the blocking voltage on some switches.

fore, in the SMML topology and unlike other topologies, there is no need for balancing modules for the flying capacitors. The ESR characterizing matrix for the flying capacitors is given by:

$$\mathbf{C} = \begin{bmatrix} \frac{1}{3} & \frac{2}{3} & \frac{1}{3} & \frac{2}{3} \\ 0 & 0 & 0 & 0 \\ \frac{1}{3} & \frac{2}{3} & \frac{1}{3} & \frac{2}{3} \\ 0 & 0 & 0 & 0 \end{bmatrix}. \tag{A.22}$$

A.2.4 Dickson Topology

Fig. A.5 (a) shows the Dickson SC topology implemented as a multilevel converter where V_X is switching between 0 and $0.25V_{IN}$. All the switches in this topology have a minimum blocking voltage of $0.25V_{IN}$, except for S2 and S3 which have a blocking voltage of $0.5V_{IN}$. Each of these two switches needs to be replaced by two stacked switches, as shown in A.5 (b), so that the blocking voltage on all switches in the topology is equal to $0.25V_{IN}$. To analyze the losses in this topology, the characterizing matrices of the switches are given by:

$$\mathbf{A} = \begin{bmatrix} \frac{1}{2} & 0 & 0 & \frac{1}{2} & \frac{1}{2} & 0 & 1 & 0 & 0 & \frac{1}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 & \frac{1}{2} & 0 & 1 & \frac{1}{2} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}, \mathbf{V_D} = \begin{bmatrix} 0 & \frac{1}{4} & \frac{1}{4} & 0 & 0 & \frac{1}{4} & 0 & \frac{1}{4} & \frac{1}{4} & 0 \\ \frac{1}{4} & \frac{1}{8} & \frac{1}{8} & \frac{1}{8} & \frac{1}{8} & \frac{1}{4} & 0 & 0 & 0 & 0 \\ 0 & \frac{1}{2} & \frac{1}{2} & 0 & 0 & \frac{1}{2} & 0 & 1 & \frac{1}{2} & 0 \\ \frac{1}{4} & \frac{1}{8} & \frac{1}{8} & \frac{1}{8} & \frac{1}{8} & \frac{1}{4} & 0 & 0 & 0 & 0 \end{bmatrix},$$

$$\mathbf{V_G} = \begin{bmatrix} 1 & 0 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 \end{bmatrix}, \mathbf{V_S} = \begin{bmatrix} 1 & \frac{3}{4} & \frac{1}{2} & \frac{1}{2} & \frac{1}{2} & \frac{1}{4} & \frac{1}{4} & 0 & 0 & 0 \\ \frac{3}{4} & \frac{5}{8} & \frac{1}{2} & \frac{3}{8} & \frac{1}{4} & 0 & 0 & 0 & 0 & 0 \\ \frac{3}{4} & \frac{3}{4} & \frac{3}{4} & \frac{1}{2} & \frac{1}{4} & \frac{1}{4} & 0 & 0 & \frac{1}{4} & 0 \\ \frac{3}{4} & \frac{5}{8} & \frac{1}{2} & \frac{3}{8} & \frac{1}{4} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}.$$

Regarding the flying capacitors, the blocking voltages on C1 and C3 are $0.75V_{IN}$ and $0.5V_{IN}$, respectively, which exceeds the minimum requiring a potentially larger implementation area. The flying capacitors in the Dickson topology has internal charge sharing losses between them since some capacitors are hard-charged or hard-discharged in each phase. To analyze if the flying capacitors in the Dickson topology are naturally balanced, the V_X node is assumed to be floating since it is decoupled from the V_{OUT} node through the output inductor. Kirchhoff's voltage law (KVL) can then be applied to

each operating phase of the topology resulting in the following equations:

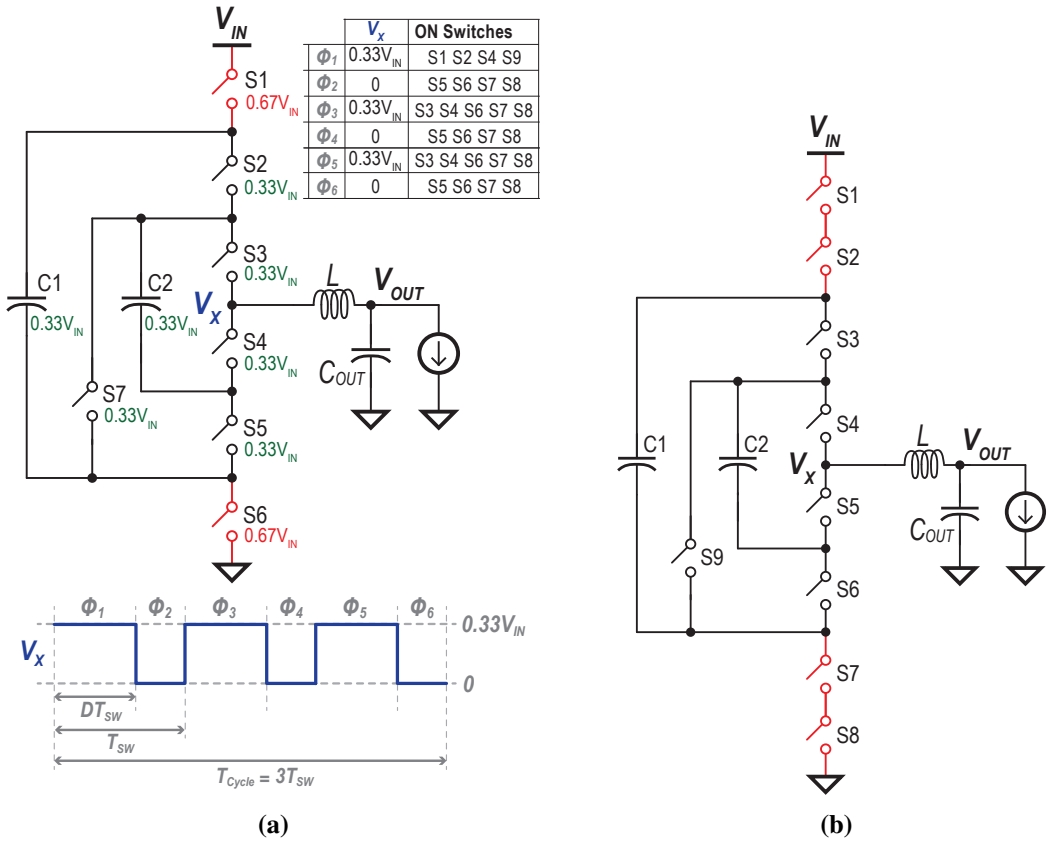
$$\begin{aligned} \phi_1: &\quad V_{C1} - V_{C2} + V_{C3} = V_{IN} \\ \phi_3: &\quad V_{C1} - V_{C2} - V_{C3} = 0. \end{aligned} \tag{A.23}$$

Since there is no solution for the previous equations (2 equations and 3 variables), the flying capacitors in the Dickson topology are not forced to be balanced at their nominal voltage and balancing modules can be needed. This result indicates that even if there is internal charge sharing losses between the flying capacitors of a certain multilevel topology, the flying capacitors can still not be naturally balanced. The ESR characterizing matrix for the flying capacitors is given by:

$$\mathbf{C} = \begin{bmatrix} \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ 0 & 0 & 0 \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \\ 0 & 0 & 0 \end{bmatrix}. \tag{A.24}$$

A.2.5 Series-parallel Topology

Fig. A.6 (a) shows the series-parallel SC topology used to build a multilevel converter where V_X is switching between $0.33V_{IN}$ and zero. The topology has six operating phases forming a one cycle. All the switches in this topology have a minimum blocking voltage of $0.33V_{IN}$, except for S1 and S6 which have a blocking voltage of $0.67V_{IN}$. Each of these two switches needs to be replaced by two stacked switches, as shown in A.6 (b), so that the blocking voltage on all the switches is equal to $0.33V_{IN}$. To analyze



	V_X	ON Switches
Φ_1	$0.33V_{IN}$	S1 S2 S4 S9
Φ_2	0	S5 S6 S7 S8
Φ_3	$0.33V_{IN}$	S3 S4 S6 S7 S8
Φ_4	0	S5 S6 S7 S8
Φ_5	$0.33V_{IN}$	S3 S4 S6 S7 S8
Φ_6	0	S5 S6 S7 S8

Figure A.6: (a) The series-parallel SC topology when used to build a multilevel hybrid converter. (b) A series-parallel multilevel converter with stacked switches to reduce the blocking voltage on some switches.

the losses in this topology, the characterizing matrices of the switches are given by:

$$\mathbf{A} = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & \frac{1}{2} & 1 & 0 & \frac{1}{2} & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & \frac{1}{2} & 1 & 0 & \frac{1}{2} & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \end{bmatrix}, \mathbf{V_D} = \begin{bmatrix} 0 & 0 & \frac{1}{3} & 0 & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} & 0 & 0 & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & 0 & 0 & \frac{1}{3} & 0 & 0 & 0 & \frac{1}{3} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 & \frac{1}{3} \end{bmatrix},$$

$$\mathbf{V_G} = \begin{bmatrix} 1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 1 & 0 \end{bmatrix}, \mathbf{V_S} = \begin{bmatrix} 1 & 1 & \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & \frac{2}{3} & \frac{1}{3} & 0 & \frac{2}{3} \\ \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 & 0 \\ \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 & 0 & 0 \\ \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 & 0 \\ \frac{2}{3} & \frac{1}{3} & \frac{1}{3} & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}.$$

In the series-parallel topology, in ϕ_1, there is no internal charge sharing between the flying capacitors but in ϕ_3 and ϕ_5, there is some internal charge sharing that occurs between the flying capacitors. To analyze if the flying capacitors in the ladder topology are naturally balanced, the V_X node is assumed to be floating. Kirchhoff's voltage law (KVL) can then be applied to each operating phase of the topology resulting in the following equations:

$$\begin{aligned} \phi_1: \quad & V_{IN} - V_{C1} - V_{C2} = V_{X1} \\ \phi_3: \quad & V_{C1} = V_{X3} \\ & V_{C1} = V_{C2} \\ \phi_5: \quad & V_{C1} = V_{X5} \\ & V_{C1} = V_{C2}, \end{aligned} \tag{A.25}$$

where V_{X1}, V_{X3}, and V_{X5} are the switching node voltage at ϕ_1, ϕ_3, and ϕ_5, respectively. This KVL analysis shows 4 independent equations with 5 variables which indicates no solution. This result means the flying capacitors are not forced to their nominal voltages through the internal charge sharing and balancing techniques for the flying capacitors might be needed. The ESR characterizing matrix for the flying capacitors is given by:

$$\mathbf{C} = \begin{bmatrix} 1 & 0 & 0.5 & 0 & 0.5 & 0 \\ 1 & 0 & 0.5 & 0 & 0.5 & 0 \end{bmatrix}^T. \tag{A.26}$$

A.3 Comparison Between Multilevel Topologies

The characterizing matrices derived for each SC topology in section A.2 can be applied directly to the general model presented in section A.1 to analyze the losses in each single SC topology. An example application, which has operating ranges similar to that used in Li-ion-to-SoC applications, is used to compare between the SC topologies. Table A.1 shows specifications of this application along with the converter design parameters including the characteristics of the employed CMOS technology. The sizing of the switches of each single SC topology were optimized according to the mechanism shown in section A.1 at a target operating point of V_{IN} = 5 V, V_{OUT} = 1 V, and I_{Load} = 1 A. After optimizing each SC topology at this target operating point, the same model is used to calculate the losses in each topology over a load current range from 0.1 A to 3 A.

Fig. A.7 shows a comparison between the five SC topologies in terms of the MOSFET conduction losses versus the load current. The SMML topology has the lowest conduction losses followed by the Dickson, the FCML, the ladder, and then the series-parallel topology. The high conduction losses in the series-parallel topology is mainly due to the high number of turned-on MOSFETs connected in series in each phase resulting in a high equivalent parasitic on-resistance. Besides the MOSFET conduction losses, it is also important to take into account the MOSFET switching losses since some topologies can have a higher number of MOSFETs changing their state when going from a phase to the next. Fig. A.8 shows a comparison between the MOSFET switching losses of the five SC topologies. The series-parallel topology has the highest switching losses due to the relatively large number of MOSFETs changing between on/off when going from one phase to the next. Fig. A.9 shows a comparison between the efficiency of the five SC topologies including the losses of the MOSFETs, the flying capacitors, and the inductor.

Table A.1: Design specifications for an example converter.

Operating Points	
Input voltage (V_{IN})	5 V
Output voltage (V_{OUT})	1 V
Load current (I_{LOAD})	0.1 – 3 A
MOSFET sizing optimization point: @ I_{LOAD} @ V_{IN} @ V_{OUT}	 1 A 5 V 1 V
Power MOSFETs	
Technology node	180 nm
Maximum overdrive voltage (V_D)	1.8 V
r_{ON} (parasitic on-resistance per one meter)	0.58 mΩ.m
C_G (gate-to-source capacitance per unit width)	1.75 nF/m
C_D (drain-to-source capacitance per unit width)	0.4 nF/m
C_J (junction capacitance per unit width)	0.3 nF/m
Voltage rating	1.8 V
Design Parameters	
Switching frequency (F_{SW}) of V_X node	2.5 MHz
Inductor size (L)	500 nH
Inductor DC resistance (DCR)	30 mΩ
Flying capacitor equivalent series resistance (ESR)	5 mΩ

The SMML topology and the Dickson topology achieve the highest efficiency with the SMML topology having a slightly better efficiency. For a more detailed comparison between these two specific topologies, both topologies has internal charge sharing losses between the flying capacitors. However, this internal charge sharing losses in the SMML topology allow the flying capacitors to be naturally balanced and this balancing is ensured phase-by-phase. In the Dickson topology, despite the internal charge sharing, the flying capacitors are not naturally balanced and balancing circuits might be needed. Designing these balancing circuit can be complicated specially if they are required to react quickly when the converter undergoes large transients in the load current. If the flying capacitors deviate from their nominal voltages, even for a brief amount of time, this can still cause critical reliability issues for the power MOSFETs. Regarding the count of the needed flying capacitors, the SMML topology employs four capacitors

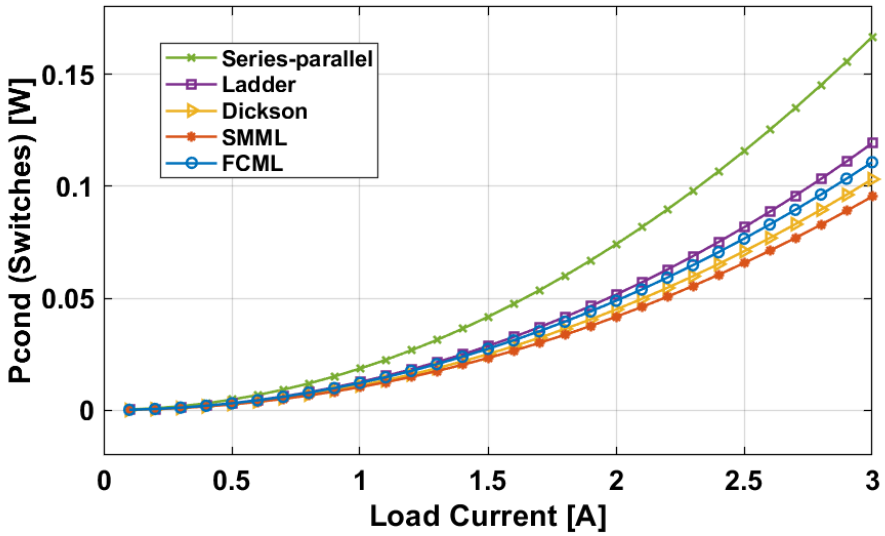


Figure A.7: Comparison between different SC multilevel topologies in terms of the conversion efficiency.

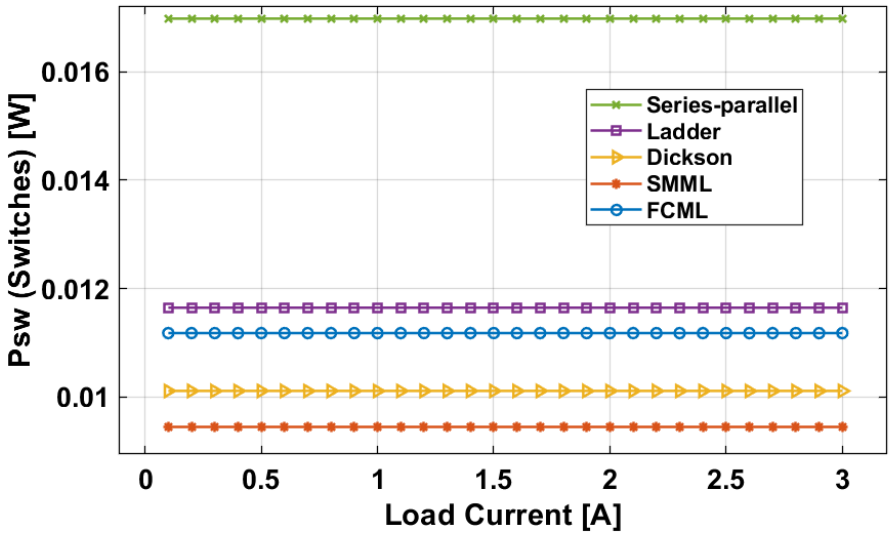


Figure A.8: Comparison between different SC multilevel topologies in terms of the total conduction losses in the converter.

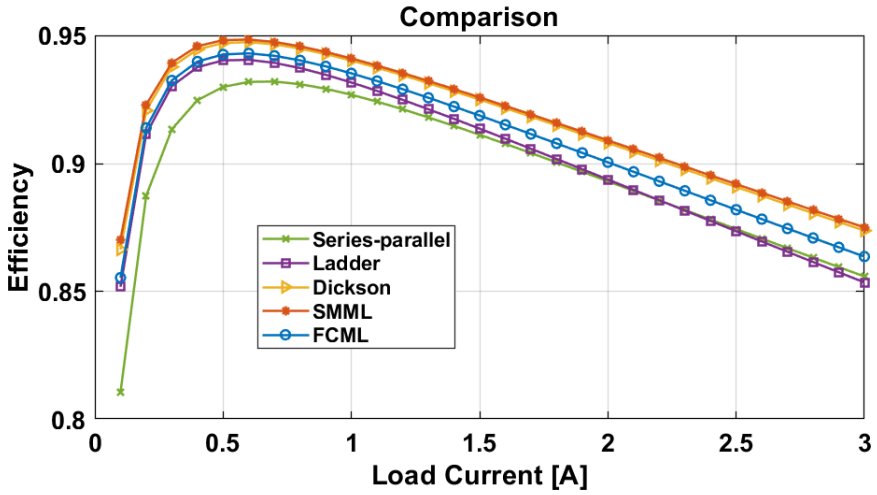


Figure A.9: Comparison between different SC multilevel topologies in terms of the total switching losses in the converter.

while the Dickson topology employs three capacitors. However, the voltage rating on some capacitors in the Dickson topology is higher than that of the SMML topology.

Fig. A.9 shows the FCML has some moderate performance among other SC topologies. However, a main attractive feature of the FCML topology is that it can theoretically provide an output voltage across the full range of V_{IN} without the need of any modification in the topology, and with a simple direct PWM control of the switches. If it is desired to operate across a wide output range, most of the other SC topologies would require the additions of more switches and capacitors to the topology which will eventually degrade their performance.

Almost each SC topology has its own advantages that can make it more suited for a certain application. The model derived in this appendix provides more insight on the performance of different SC topologies when employed in multilevel converters and can help selecting the best suited SC topology for the target application.

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