UNIVERSITY OF CALIFORNIA, SAN DIEGO

A Wideband High Dynamic Range Frequency Hopping Hardware Front-End for the Joint Tactical Radio System

A thesis submitted in partial satisfaction of the requirements for the degree of Master of Science

in

Electrical Engineering (Applied Physics)

by

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2010

The Thesis of Anton Arriagada is approved and it is acceptable in quality and form for the publication on microfilm and electronically:

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University of California, San Diego

2010

DEDICATION

I dedicate this work partially to my parents, Alex and Kyong, and my grandparents, Carlos and Frieda, for their support and interest in my education. Knowing that you all cared so much was inspiration to press on when times became difficult.

I also dedicate this work to my wife, Ann, for her unending patience and support throughout my unusually long tenure as a student. Although my days of learning are far from over, let this be the end of my days as a student.

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LIST OF ABBREVIATIONS

ADC	Analog-to-Digital Converter
ADI	Analog Devices Incorporated
BB	Baseband
BPF	Band-pass Filter
Calit2	California Institute for Telecommunication and Information Technology
CG	Conversion Gain
DAC	Digital-to-Analog Converter
DDS	Direct Digital Synthesizer
DOD	Department of Defense
DR	Dynamic Range
EVM	Error Vector Magnitude
FPGA	Field Programmable Gate Array
GCPW	Grounded Coplanar Waveguide
GIG	Global Information Grid
I/Q	In-phase/Quadrature
IC	Integrated Circuit
IF	Intermediate Frequency
IIP2	Input Second-order intercept point
IIP3	Input Third-order Intercept Point
IL	Insertion Loss

IP1dB	Input 1-dB Compression Point
JAN-TE	Joint Airborne Networking-Tactical Edge
JPEO	Joint Program Engineering Office
JTRS	Joint Tactical Radio System
LNA	Low Noise Amplifier
LO	Local Oscillator
MUOS	Mobile User Objective System
OBW	Occupied Bandwidth
OIP3	Output Third-order Intercept Point
OP1dB	Output 1-dB Compression Point
PLL	Phase-Locked Loops
RF	Radio Frequency
RFFE	Radio Frequency Front-End
RFIC	Radio Frequency Integrated Circuit
SDR	Software Defined Radio
SMA	SubMiniature Version A
SMD	Surface Mount Device
SNR	Signal-to-Noise Ratio
SRW	Solider Radio Waveform
SD4T	Single-Pole-4-Throw
SPDT	Single-Pole-Double-Throw
UHF SATCOM	Ultra-High Frequency Satellite Communications

USAF	United States Air Force
USMC	United States Marine Corps
USN	United States Navy
VCO	Voltage-Controlled Oscillator
VGA	Variable Gain Amplifier
WNW	Wideband Networking Waveform

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ACKNOWLEDGEMENTS

I would like to acknowledge Professor Lawrence Larson for his support as my thesis committee chair and his role as an advisor both technically and professionally. His show strong of support in making the most of my time at UCSD when I was looking for options was *the* turning point that brought me here.

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Finally, I would like to thank Richard North for his support in the Joint Tactical Radio System here at UCSD. The Joint Tactical Radio System at UCSD is a unique opportunity for students to gain valuable experience on a project that has a real stake in the communication capabilities of the United States military.

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ABSTRACT OF THE THESIS

A Wideband High Dynamic Range Frequency Hopping Hardware Front-End for the Joint Tactical Radio System

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Professor Lawrence Larson, Chair

The Joint Tactical Radio System project is the Department of Defense's effort to create and organize a communication network that links a variety of radio platforms (e.g. handheld, naval, and aircraft). This goal can be achieved by developing a family of interoperable software defined radios with its members optimized for specific platforms.

Realistic software defined radios utilize two systems to enable flexible and interoperable communications: software and hardware. The software system is

responsible for converting transduced real information (e.g. text, voice, and video) into digitally modulated information and performing data impairment correction and synchronization. The hardware system, also known as a radio frequency front end, performs the physical conversion between relatively low-frequency digital data and high frequency carriers for practical and realizable communication system implementations.

This thesis describes the design and implementation of a wideband high dynamic range frequency hopping hardware front-end for the Joint Tactical Radio System software defined radio. The front-end realizes a transceiver that utilizes radio frequencies from 200 MHz to 3.2 GHz and provides a 78 dB maximum dynamic range. The frequency hopping local oscillator is achieved by direct digital synthesis and successive frequency multiplications. Additionally, a low-noise amplifier and band-pass filter bank in support of the radio frequency front-end implementation have been developed and tested.

The system features a high level of discrete integration and has been implemented entirely through the use of commercially available integrated circuits and surface-mount devices. The complete system was constructed using manufacturer evaluation kits and custom designed boards.

Chapter 1: Introduction

The Joint Tactical Radio System (JTRS) was introduced by the Department of Defense (DOD) in 1997 as a means to replace the older United States military radios that typically featured limited ability to cross-communicate with other platforms [1]. The scope of JTRS has widened to include the planning and development of a network of wireless communication systems designed for cross-platform (e.g. hand held, land vehicles, aircraft, naval vessels, satellites) interoperability and access to the Global Information Grid (GIG). The interoperability of a wireless multi-platform communication system provides an essential function in delivering real-time battlefield awareness to the tactical user (often referred to as the "last tactical mile") [2]. However, interoperability places steep demands on the capabilities and performance of the system. Wideband radio frequency (RF) carrier transmission and reception are necessary to accommodate various military communication waveforms such as the Soldier Radio Waveform (SRW), Wideband Networking Waveform (WNW), Joint Airborne Networking-Tactical Edge (JAN-TE), Mobile User Objective System (MUOS), and Ultra-High Frequency Satellite Communications (UHF SATCOM). Additionally, radio operation in the battlefield can be susceptible to RF interference from other allied communications or enemy signal jamming attempts, necessitating high dynamic range, dynamic front-end filtering and frequency hopping capabilities. Figure 1 shows the JTRS Increment 1 Tactical Network, where rapid communication between forces of the United States military such as the Army, Marine Corps (USMC),

Navy (USN), and Air Force (USAF), residing in different domains (land, maritime, air, and satellite) is made possible by JTRS [3].

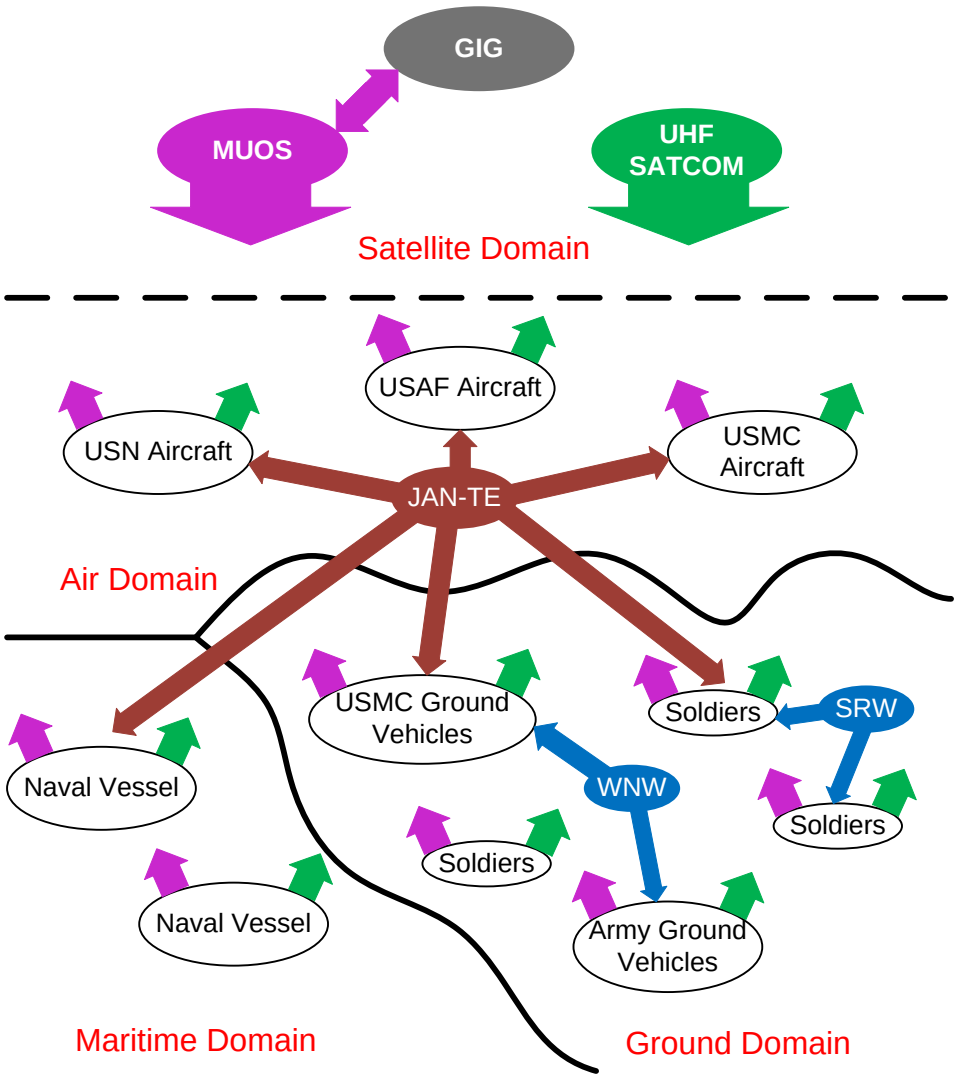

Figure 1: JTRS Increment 1 Tactical Network

The goals of JTRS can be achieved by utilizing a software defined radio (SDR) architecture. SDRs can, in principle, provide coverage of multiple waveforms and standards by employing a flexible hardware configuration that is under the control of

software. The ideal SDR shown in Figure 2 is simply an antenna connected directly to a digital signal processor (DSP) or field programmable gate array (FPGA) through an extremely high speed analog-to-digital converter (ADC) and digital-to-analog converter (DAC).

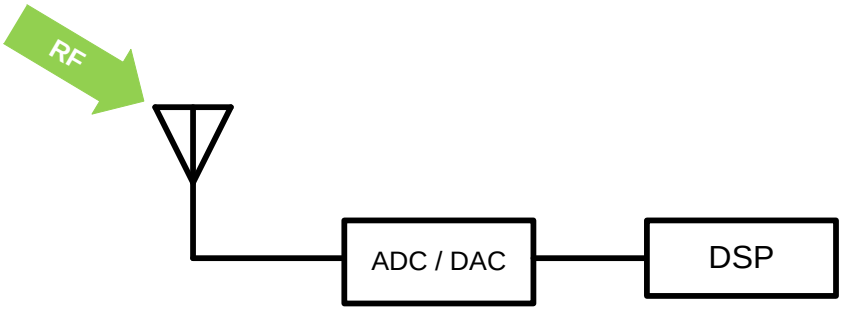

Figure 2: The Ideal SDR

Consider the ideal SDR receiver: this system would directly digitize and demodulate data present on RF signals into useful information. However, ADC sampling speeds required to digitize RF signals are usually limited in sampling resolution. Additionally, the subsequent processing speeds required for digital demodulation of RF signals are unachievable from modern processors and would consume an enormous amount of power, rendering the ideal SDR impractical.

The conventional implementation of an SDR receiver avoids these problems by utilizing a radio frequency front-end (RFFE) to down-convert the RF signal to an intermediate frequency (IF) or baseband (BB). Figure 3 shows the conventional SDR utilizing a reconfigurable RFFE for realizable implementation.

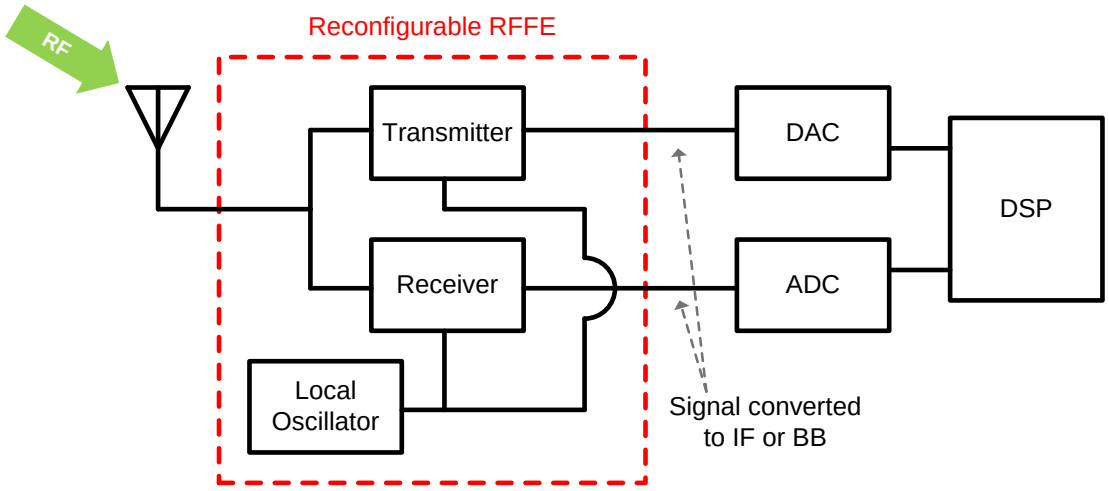

Figure 3: The Conventional SDR

This strategy places the frequency of digitally modulated signal well into the range of current ADC and DSP technology. However, RFFE must contain provisions that allow for dynamic RF chain reconfiguration by a software system, such as automatic gain control, filter tuning, and wideband component matching. This thesis describes the design and implementation of a reconfigurable RFFE that can be easily controlled by DAC or digital inputs for JTRS SDR applications.

Chapter 2: System Overview

The primary objective of the JTRS SDR is to transmit and receive a large variety of waveforms. Support for UHF (300 MHz - 3 GHz) satellite communications (e.g. MUOS and UHF-SATCOM) necessitate wideband RF capability, therefore wideband performance is the primary design goal of the JTRS RFFE. The JTRS RFFE target RF frequency range is 200 MHz to 3.2 GHz. Wideband frequency hopping capability is another goal for the JTRS SDR. Some wideband SDR RFFE often apply wideband voltage-controlled oscillators (VCO) [4, 5] and phase-locked loops (PLL) [4] to obtain excellent phase noise performance with the sacrifice of longer settling time in up- and down-conversion. Conversely, the use of a direct-digital synthesizer (DDS) provides faster switching response, but with limited output frequencies. The JTRS RFFE solution to enable rapid frequency hopping involves combining both a PLL and DDS to obtain the benefits of both.

The JTRS RFFE utilizes a wideband direct in-phase/quadrature (I/Q) conversion architecture. The entire RFFE consists of three subsystems: transmitter, receiver, and a DDS-based local oscillator (LO) synthesizer. All subsystems are designed with purchasable commercial discrete components such as radio frequency integrated circuits (RFIC), surface mount devices (SMD), and SubMiniature Version A (SMA)-connectorized coaxial components. A deliberate focus of Calit2's JTRS project is to implement as much of the system as possible in the form of manufacturer evaluation boards and kits to evaluate realistic performance of subsystems. The transmitter and receiver are constructed almost entirely from evaluation kits and are

ready to be integrated onto a single RF board. The local oscillator has been implemented with a combination of evaluation boards and connectorized RF components.

Components have been selected primarily from Analog Devices Incorporated (ADI), Mini-circuits, and Skyworks Solutions Incorporated due to the availability of thoroughly detailed application notes for discrete components and evaluation board design details regarding materials and trace dimensions. This allows future efforts on the JTRS RFFE to have an abundance of reference materials to facilitate the integration of the whole RFFE onto a single board. The final form factor goal for Calit2's JTRS project is a signal RF board integrating the configurable RFFE (transmitter, receiver, and local oscillator), software system (e.g. ADC, DAC, FPGA/DSP, etc.), and human interface.

Chapter 3: Receiver

Figure 4 shows a block diagram of the wideband receiver implemented in the JTRS RFFE.

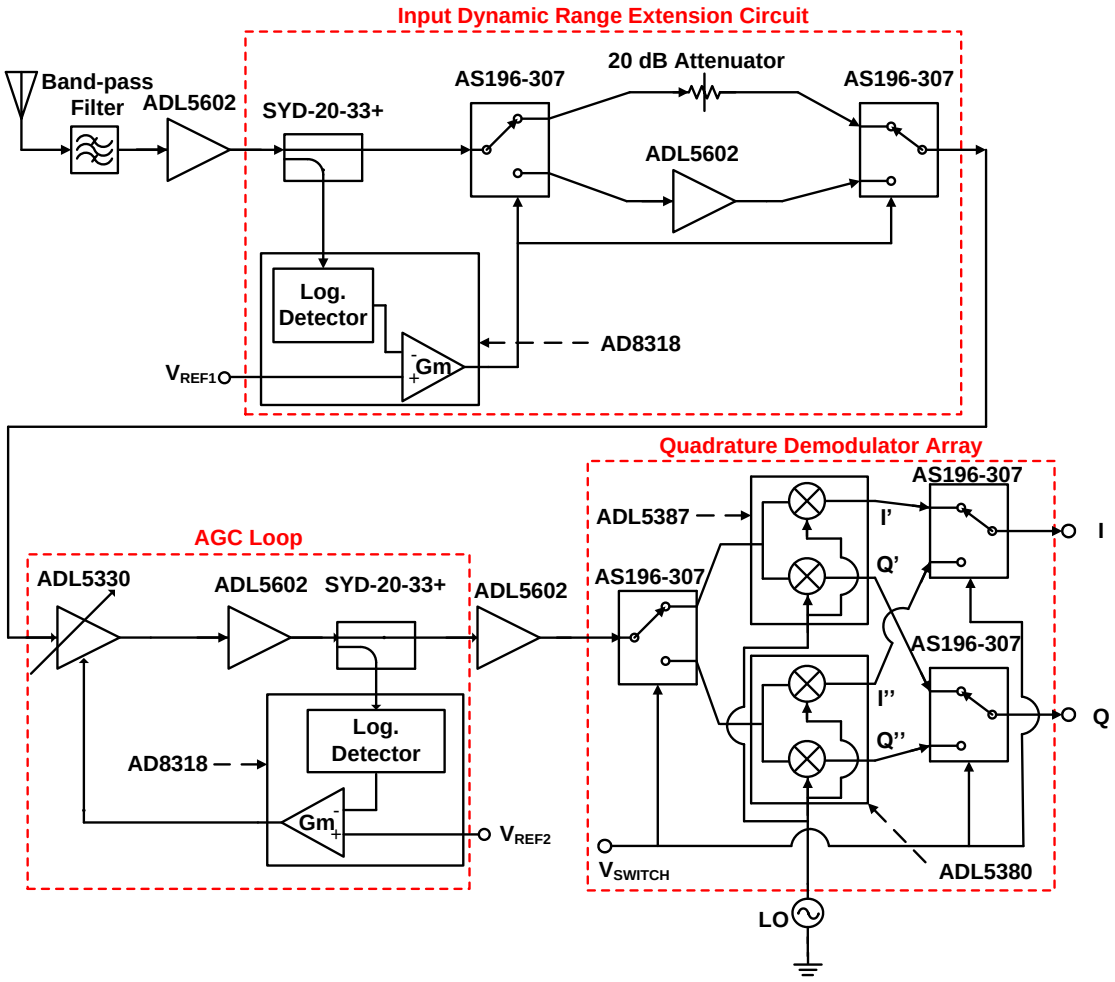

Figure 4: Block Diagram of the JTRS Receiver

An incoming RF signal received by an antenna is amplified by the ADI ADL5602 gain block which features a low noise figure to set a high signal-to-noise-ratio (SNR) for the receiver. The ADL5602 serves as a low noise amplifier (LNA) and

is an all-purpose 20 dB gain block that is internally matched (50 Ω) across a wide frequency range (5 MHz – 4 GHz) with a noise figure as high as 4.2 dB at 4 GHz. Following the LNA, the signal's power is monitored and adjusted by an input dynamic range extension circuit. The extension circuit detects the incoming power level and switches an amplifier (another ADL5602) or attenuator (20 dB) into the RF chain based upon a comparison to a power threshold determined by V_{REF1}. A Mini-Circuits SYD-20-33+ wideband direction coupler (bandwidth from 30 MHz to 3 GHz, 20 dB coupling) is used to split a small portion of the signal to the ADI AD8318. The AD8318 is a logarithmic controller (bandwidth from 1 MHz to 8 GHz, 1.5 V linear voltage output range from a 70 dB input power range) that features a logarithmic power detector and integrated comparator with DC output voltage capability of 0 V to 4.9 V. The integrated comparator compares V_{REF1} to the logarithmic detector's output voltage to determine the power threshold. Changing V_{REF1} allows the power threshold of the extension circuit to be set. Figure 5 shows a plot of the configurable power threshold versus V_{REF1}. If the signal power is higher than the set threshold power, the logarithmic controller synchronously toggles a pair of Skyworks Solutions AS196-307 single-pole-double-throw (SPDT) RF switches (bandwidth from DC to 6 GHz, absorptive) to bring the attenuator into the RF chain. If the signal power is lower than the threshold, the ADL5602 is instead cycled into the RF chain. The power threshold shown in Figure 5 features approximately 2 dB of hysteresis. The hysteresis is an integrated feature of the AD8318 and helps to avoid rapid switching states of the extension circuit from small power fluctuations of the input signal.

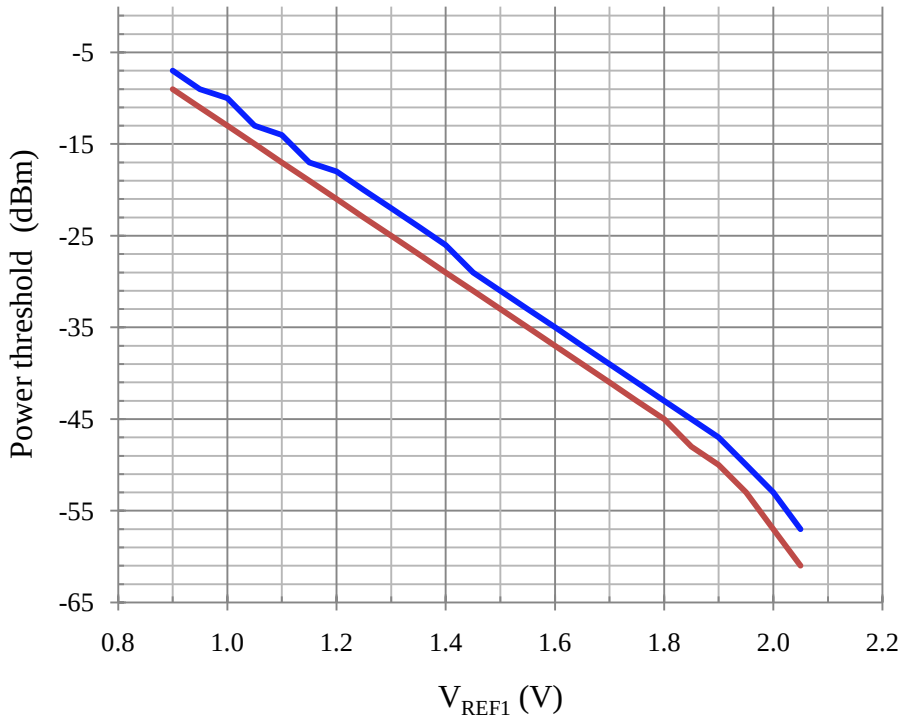

Figure 5: Extension Circuit Power Threshold vs. V_{REF1}. The blue curve is the power threshold approaching from lower power. The red curve is the threshold approaching from higher power

By strategically setting the threshold power, the dynamic range extension circuit adjusts the RF signal to an optimal power level that allows maximum utilization of the automatic gain control (AGC) loop dynamic range, extending the dynamic range of the entire receiver. The AGC loop uses the ADI ADL5330 variable-gain amplifier (VGA) (bandwidth from 10 MHz to 3 GHz, 60 dB gain control range) controlled by another logarithmic controller to maintain the loop's output level through a comparison to another reference target voltage, V_{ref2}. The VGA output is amplified by the ADL5602 gain block, after which a small portion of the signal (-20 dB) is coupled by another SYD-20-33+ wideband directional coupler to the AD8318 logarithmic controller. The

function of the logarithmic controller in the AGC loop is exactly the same as in the extension circuit except that the closed loop (formed by the VGA, gain block, wideband directional coupler, and logarithmic controller) forces the AGC loop output to a power level determined by V_{REF2}. Figure 6 shows the AGC loop output power vs. V_{REF2} with a 400 MHz 8-ary phase shift keying (8PSK) signal at the receiver input (P_{in}= -10 dBm, 7.776 mega-symbols per second, root-Nyquist filter, α=0.25) generated by an Agilent E4438C ESG Vector Signal Generator. The LO is provided by an Agilent N5181A MXG Analog Signal Generator for testing. An Agilent N9020A MXA Signal Analyzer was used for all receiver measurements. The AGC loop exhibits approximately 30 dB of output power control range to a fixed power input signal.

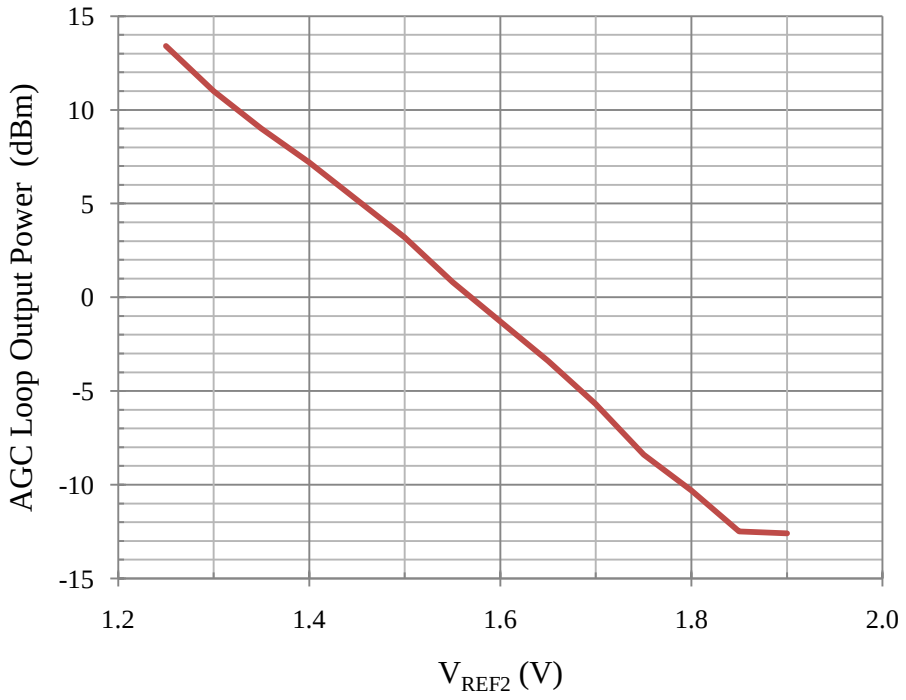

Figure 6: AGC Loop Output Power vs. V_{REF2}

Fluctuations in power caused by transmission path losses of incoming wireless signals and gain/insertion loss (IL) variations vs. frequency of the receiver's components (e.g. VGA, gain block, directional couplers, RF switches, etc.) before demodulation can lead to clipping (large signals) or a loss of useful digitization bits (small signals) at the ADC inputs, reducing the overall dynamic range of the radio. The AGC loop's primary function is to maintain a constant power before down-conversion to I/Q baseband. The AGC loop's output is amplified by a final ADL5602 before down-conversion by the demodulator array. The array utilizes three synchronized AS196-307 RF switches to switch one of two demodulators into the RF chain for down-conversion. The ADI ADL5387 quadrature demodulator (bandwidth from 50 MHz to 2 GHz, 240 MHz demodulation bandwidth), with low-band outputs I' and Q', is utilized as the low-band demodulator while the ADI ADL5380 (bandwidth from 400 MHz to 6 GHz, 390 MHz demodulation bandwidth), with high-band outputs I'' and Q'', is used as the high-band demodulator. The switch at the array input directs the signal to one of the demodulators. The switches at the array's output combine appropriate I/Q signals for digital demodulation (e.g. one switch selects either the low- or high-band I output while the other selects either the low- or high-band Q output). Wideband demodulation is achieved by using V_{SWITCH} to select the frequency-band appropriate demodulator. Although there is a large band coverage overlap between the two demodulators, best performance is obtained by using the low-band demodulator for frequencies between 200 and 400 MHz, and the high-band demodulator for all frequencies greater than 400 MHz.

All measurements below 400 MHz were performed with the low-band demodulator switched into the RF chain, while frequencies above 400MHz utilize the high-band demodulator. V_{REF1} was set to 1.85 V and V_{REF2} was set to 1.50 V. The receiver's output power, P_{OUT}, vs. RF input power, P_{IN}, is shown in Figure 7. The receiver achieves a maximum conversion gain (CG) of 80 dB. The output power exhibits a relatively constant level as the input power is varied, exhibiting the AGC loop's ability to compensate for varying input power. As the frequency of the RF input signal is increased, the maintainable output level and compensation range becomes reduced due to bandwidth limitations of the VGA and is eventually dominated by the wideband directional couplers. A gain compensation range of 65 (from 10 dBm to -55 dBm) dB with respect to input power is observed at 3.2 GHz.

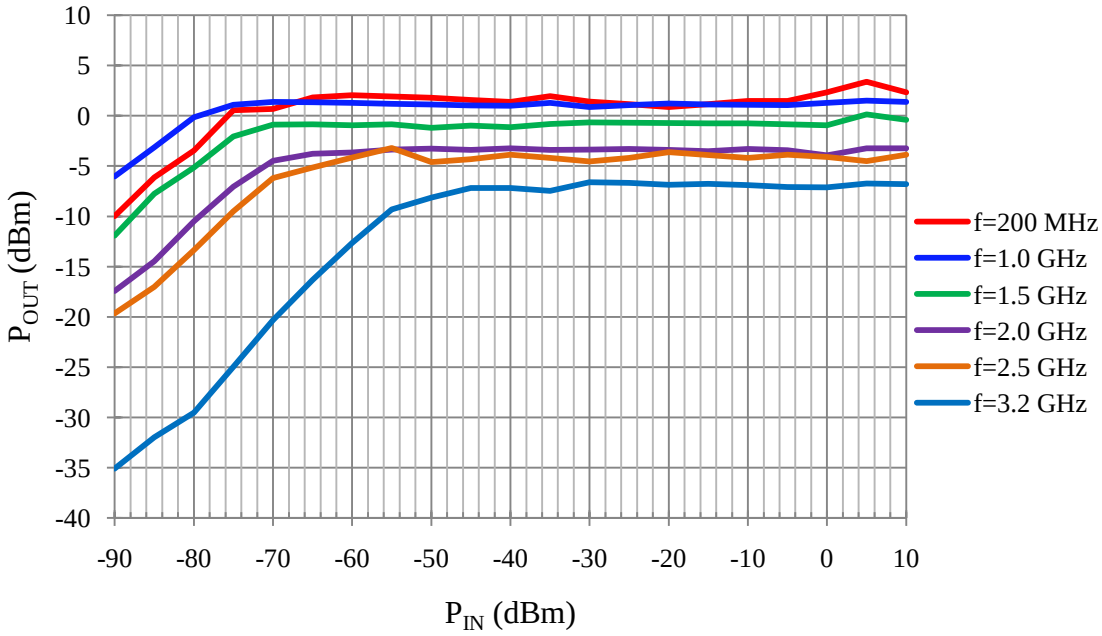

Figure 7: Receiver P_{OUT} vs. P_{IN}. Results for sever input signal frequencies are shown

The highest power at the receiver input for which the Adjacent Channel Power (ACP) in the receiver *before* down-conversion is -40dBc or lower defines the highest acceptable receiver input level, P_{HIGH}. A channel bandwidth of 8.6 MHz was determined by measuring Occupied Bandwidth (OBW) at low power. A channel spacing of 10.56 MHz was used to determine ACP. Input powers corresponding to a 3dB drop with respect to the AGC's maintainable output level indicate the lower useful power threshold, P_{HIGH}. The receiver's dynamic range (DR) is defined as the difference between P_{HIGH} and P_{LOW} and is shown vs. center frequency in Figure 8. The receiver demonstrates a maximum input dynamic range of 78 dB at 400 MHz and rolls off to 46 dB at 3.2 GHz.

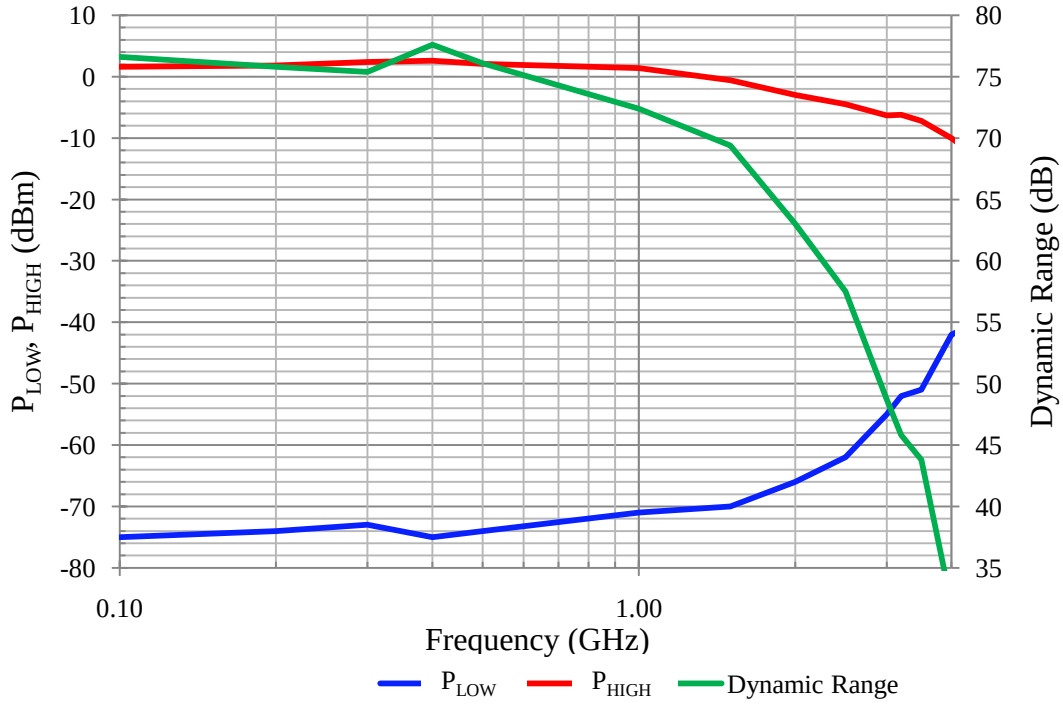

Figure 8: Receiver P_{HIGH}, $P_{LOW,}$ and Dynamic Range vs. Frequency. P_{HIGH} (red) and P_{LOW} (blue) are plotted with respect to the left vertical axis while the Dynamic Range is plotted with respect to the right vertical axis

The small break in discontinuity of the gain at low frequencies is caused by the switch between the low- and high-band demodulators in the array.

The Error Vector Magnitude (EVM) of the receiver output vs. frequency for various input powers is shown in Figure 9. EVM Measurements were taken at a low-IF of 10 MHz. Optimal EVM performance is obtained for input power between -40 dBm and -10 dBm. The EVM remains approximately -45 dB and becomes no worse than -36 dB at 3.2 GHz in this optimum power range.

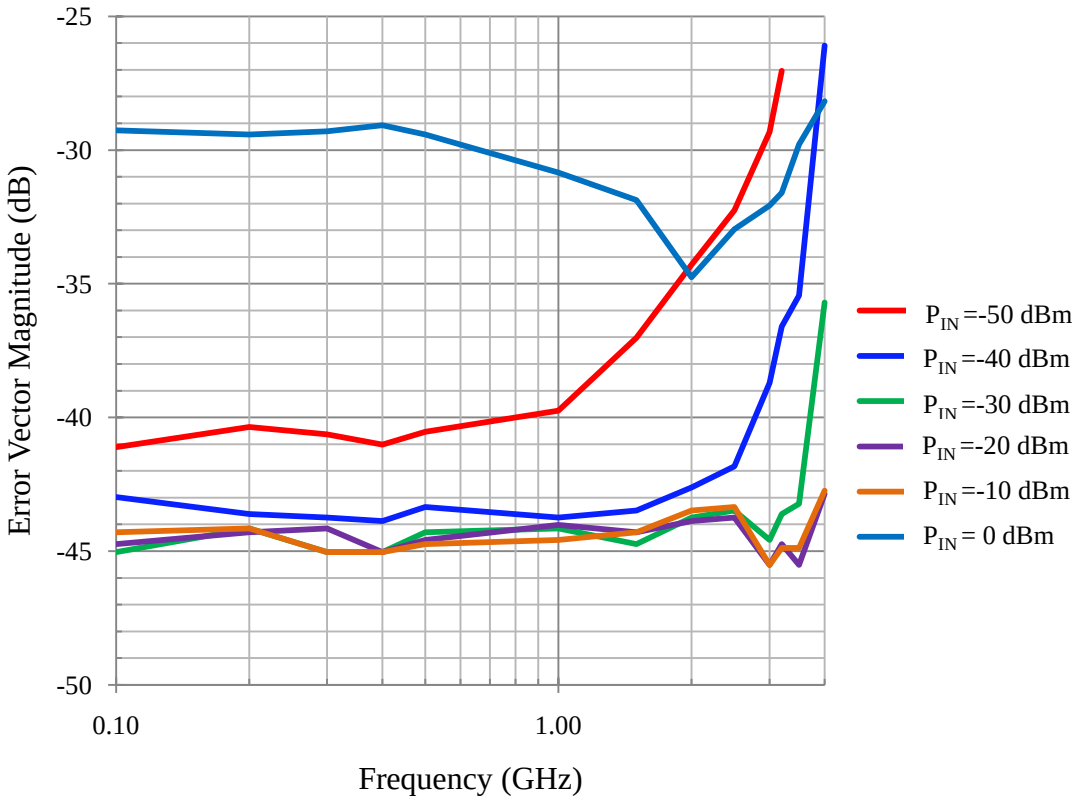

Figure 9: Receiver Error Vector Magnitude vs. Frequency. Results for several input powers are shown

EVM degradation above -10 dBm input power results from distortion of saturated linear gain stages in the RF chain. The EVM remains excellent (~ -30 dB) up to an input power of 0 dBm. EVM performance below -40 dBm input power begins to degrade due to the limited dynamic range, and ultimately SNR, of the MXA signal analyzer.

The receiver Noise Figure (NF), shown in Figure 10, is measured under maximum gain conditions by breaking the AGC loop and manually setting the VGA to its maximum gain setting. The receiver achieves a NF of less than 4.5 dB below 1 GHz and degrades to as high as 6.3 dB at 3.2 GHz. The NF does not change when using either the low- or high-band demodulators due to high gain (~ 80 dB at low frequencies) preceding them.

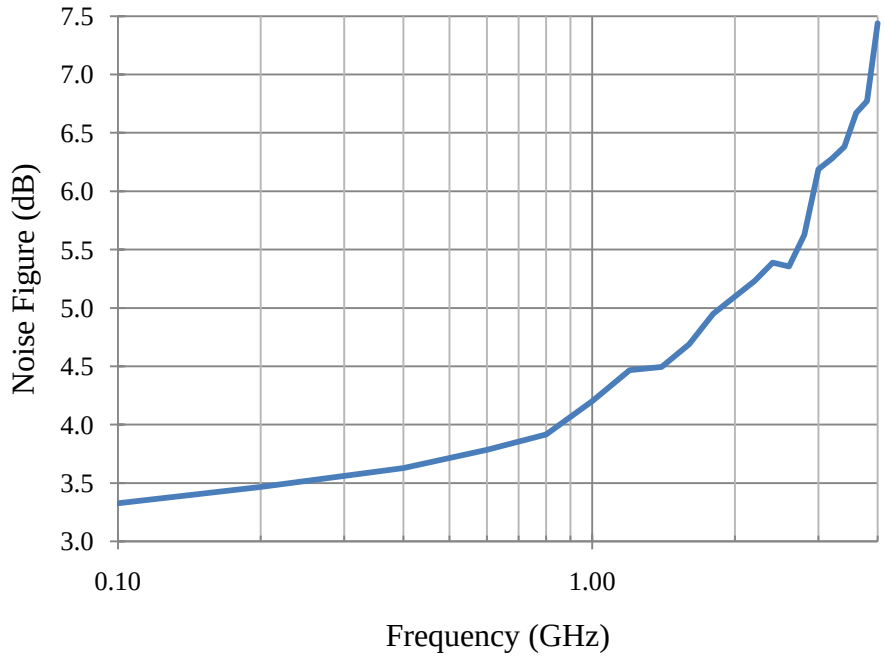

Figure 10: Receiver Noise Figure

The receiver features 3 points of RF chain reconfiguration: power threshold adjustment in the dynamic range extension circuit (V_{REF1}), receiver chain output power level adjustment (V_{REF2}), and demodulator array switch control (V_{SWITCH}). V_{REF1} and V_{REF2} can be controlled by DAC outputs (0.9 V to 2.1 V and 1.2 V to 1.9 V, respectively), while V_{SWICTH} can be controlled with 5V CMOS/TTL logic levels. These control points can be adjusted by software systems for SDR control. The power consumptions for all subsystems in the JTRS RFFE are listed in Appendix A.

Chapter 4: Band-Pass Filter Bank

A challenge facing wideband receivers is to provide just enough filtering of potential high-power interferers near the RF signal of interest to prevent large inter-modulation products from being generated by subsequent gain stages *while* having the ability to tune the band-pass filter (BPF) characteristics (e.g. bandwidth, center frequency, or both). A static center-frequency BPF cannot be used because it will either limit the useable RF bandwidth, or allow too much interference to propagate down the RF chain. Therefore, it is appropriate to think of the receiver as wide-band "capable", where the BPF provides strategic band limiting (filtering) while the remaining components in the RF chain are truly wideband.

A BPF bank RF board has been developed at Calit2 to address the issues listed above. Figure 11 shows the block diagram for the filter board. The board features 10 Skyworks Solutions SKY13322-375LF single-pole-4-throw RF switches (bandwidth from 100 MHz to 6 GHz, reflective) used to route the incoming RF signal (bandwidth from 200 MHz to 3.2 GHz) to one of 16 band pass filters. The two outer switches are synchronized to split the entire RFFE frequency range into 4 bands. Each of these bands is further divided into 4 more sub-bands for a total of 16 possible RF paths for signal filtering. The BPF in each path is constructed from cascaded Mini-Circuits high- and low-pass discrete 7 segment filters (all matched to 50 Ω). Appendix B shows a circuit schematic of the filter with all of the part names listed). The high- and low-pass filters (HPF and LPF) were chosen to create BPF responses with equal width, equal

center frequency spacing, and pass-band overlap with adjacent filters to ensure that no gaps in the RFFE target frequency range exist.

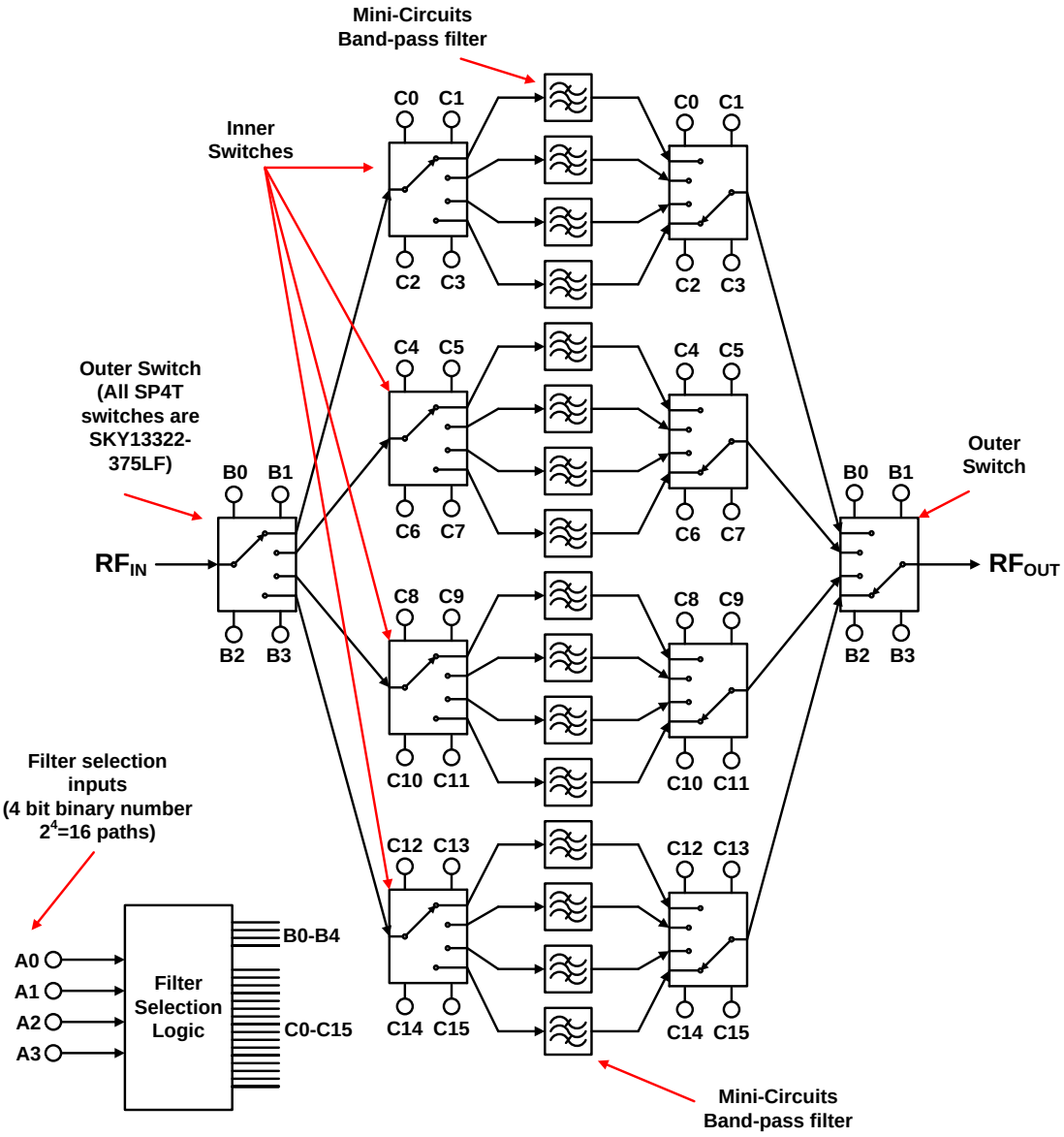

Figure 11: Block Diagram of the JTRS Band-Pass Filter Bank

Figure 12 shows the BPF selection logic diagram. The control logic is designed so that exactly one path from RF_{IN} to RF_{OUT} exists at any given time. This condition ensures that a 50 match is maintained at the input and output at all times.

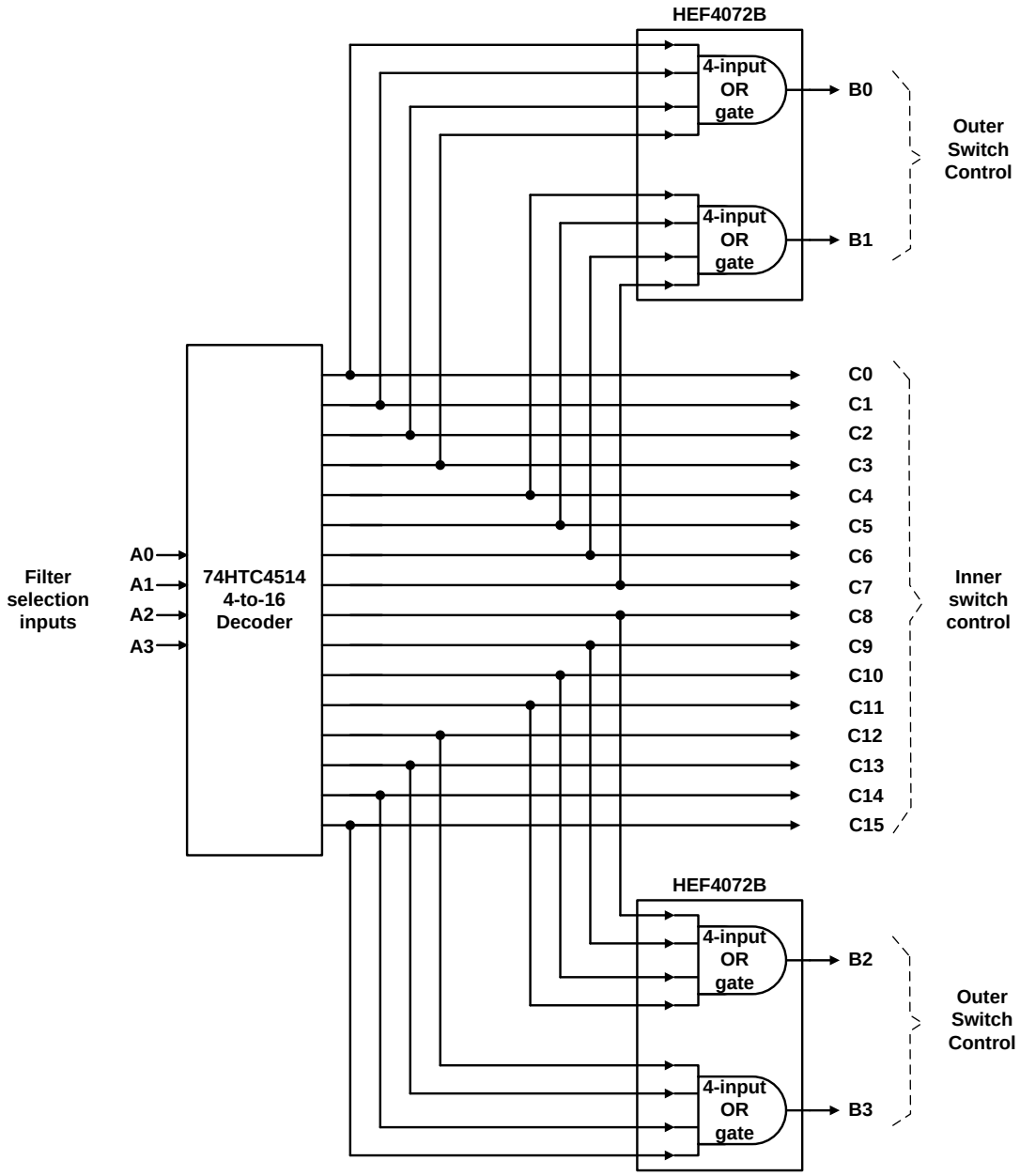

Figure 12: Band-Pass Filter Selection Logic Diagram

The filter board accepts a 4-bit binary input on bits A0-A3 (5V CMOS/TTL) to select from one of the 16 filter paths. The 4-bit binary input is converted into 16 minterms, C0-C15, by a Philips 74HCT4514 4-to-16 decoder (2^4=16). C0-C15 act as inner switch controls. Consecutive groups of 4 minterms, (e.g. C0- C3, C4-C7, etc.) are split off to a different 4-input OR gate to produce binary outputs B0-B3. B0-B3 act as outer switch controls. B0, B1 and B2, B3 are the outputs of separate a Philips HEF4072B Dual 4-input OR gates. The 4-to-16 decoder ensures that only one of the 16 minterms, C0-C15, can be logic level high at any given time. Therefore only one of the four outer switch outputs can be active. C0-C15 operate in the same way to open one path between the inner switch rows to route the RF signal through a BPF.

Figure 13 shows a photo of the front of Calit2's fabricated and assembled BPF bank. The RF board layout was designed with PADS Layout software. The board features 4 metal layers with 1 oz. copper and 10 mil Rogers 4350 top dielectric. All RF traces were confined to the top metal layer and utilize grounded coplanar waveguide design (GCPW) to enhance isolation between RF traces. The top metal layer uses a gold emulsion mask for corrosion resistance and solder mask has been excluded from all RF traces to reduce trace losses. The second (from the top) metal layer is a ground plane necessary for GPWG performance. All digital logic components are mounted on the reverse side of the board as shown in Figure 14. Digital traces are confined primarily to metal layer 4 with few routes diverted to metal layer 3. The remaining metal on layer 3 serves as a second ground plane for improved isolation between the

RF and digital switching traces. High frequency SMA end-launch connectors are used for optimal connector-to-RF trace connection (avoids impedance mismatches).

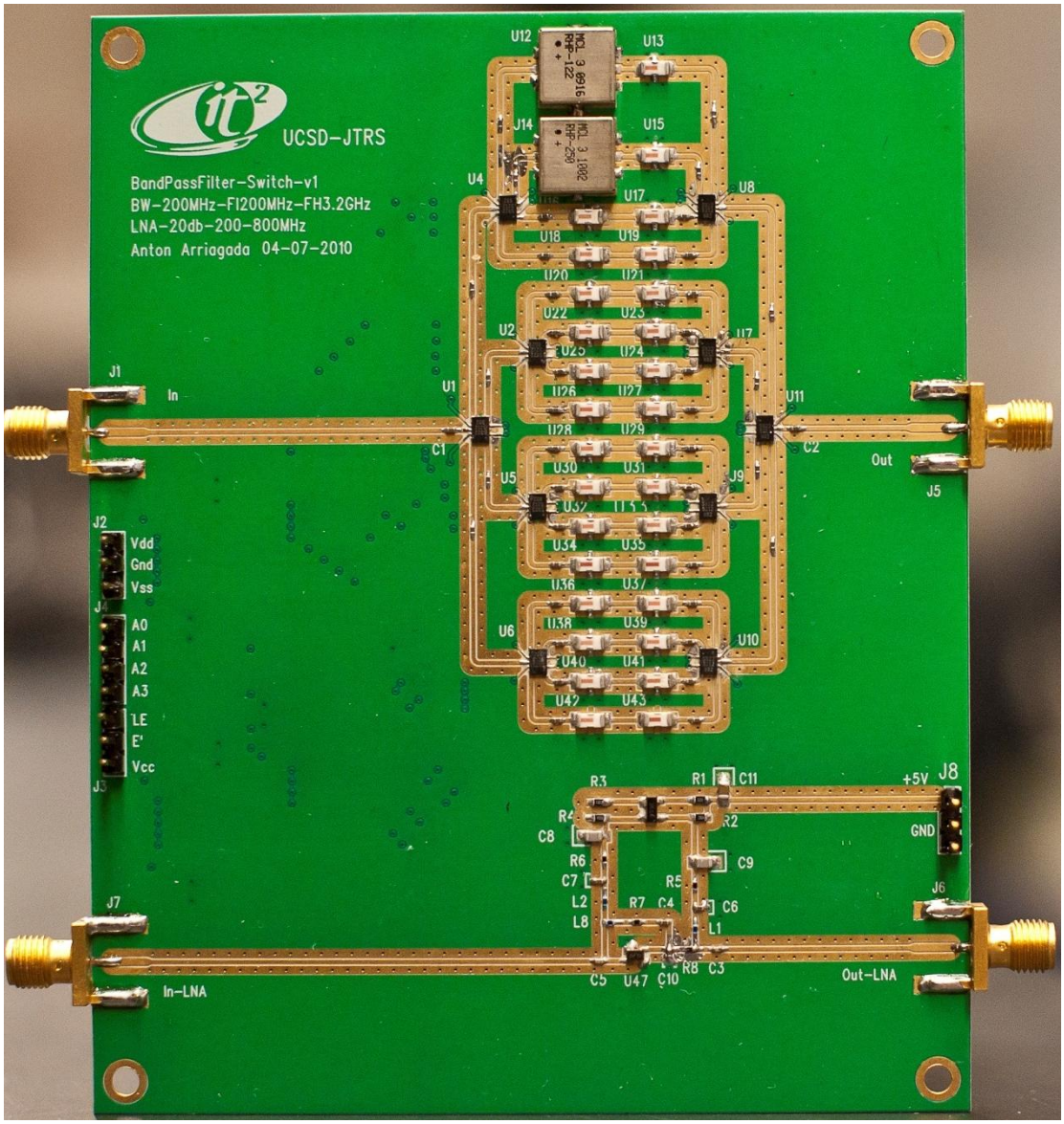

Figure 13: Photo of the JTRS Band-Pass Filter Bank (front). Only RF components are mounted on the front side of the board

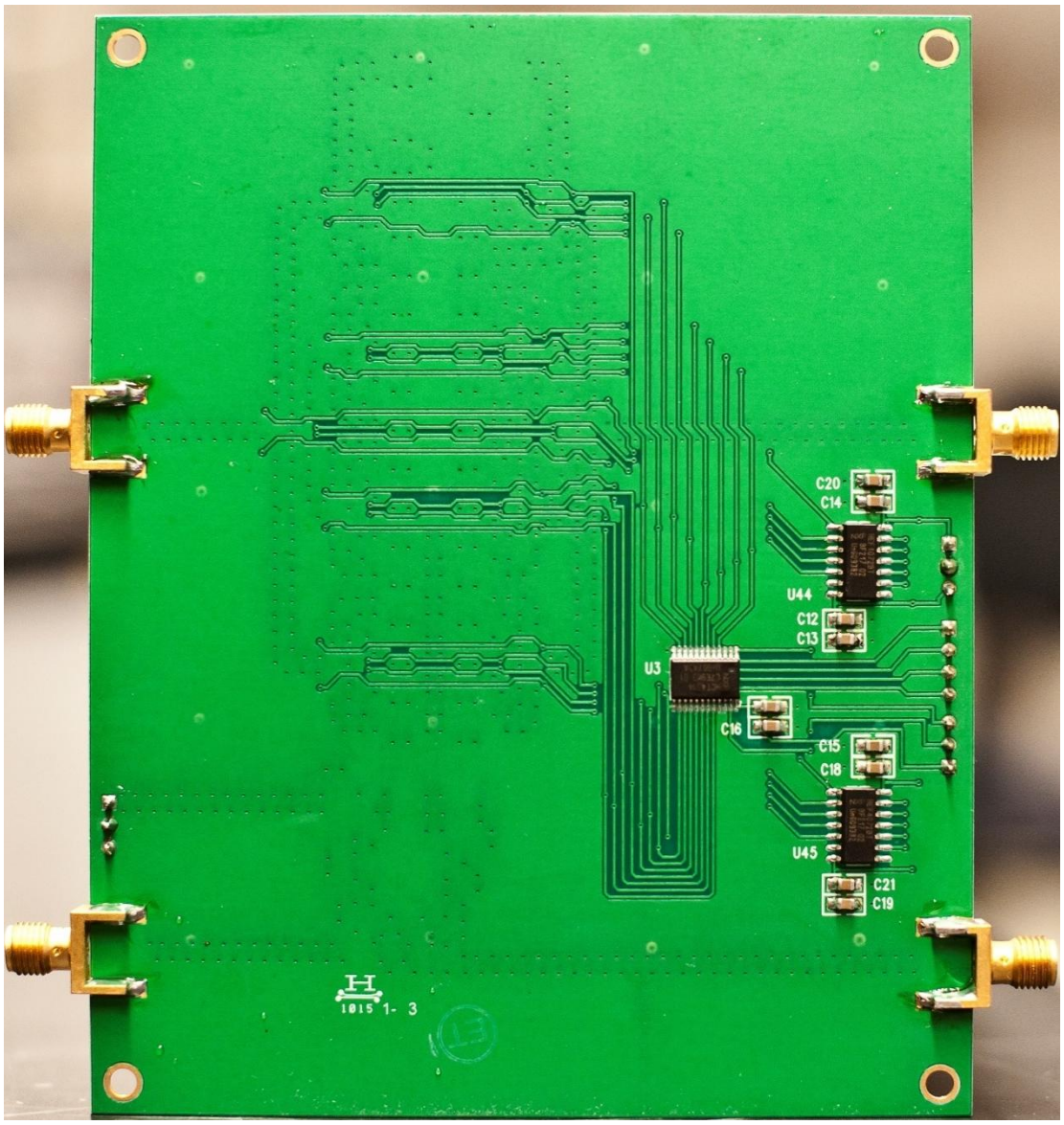

Figure 14: Photo of the JTRS Band-Pass Filter Bank (back). Only digital components are mounted on the back side of the board

Figure 15 shows the measured S11 parameter for the BPF. Several (non-consecutive) responses have been superimposed for comparison (all 16 responses are shown separately in the Appendix C). All measurements were taken with an Agilent N5242A PNA-X Network Analyzer. RF_{IN} was port 1 and RF_{OUT} was port 2. While the filter clearly exhibits the ability to vary the center frequency, the bandwidth does not remain constant. This is due to the limited selection of Mini-Circuits low- and high-pass filter available to construct BPF responses. An IL of approximately 3.5 dB is observed in the pass-band at the lowest center frequency and rolls off steadily to 6 dB at the highest center frequency. The insertion loss is dominated primarily by the RF switches (~0.5 dB IL per switch, 4 per path) at low frequency.

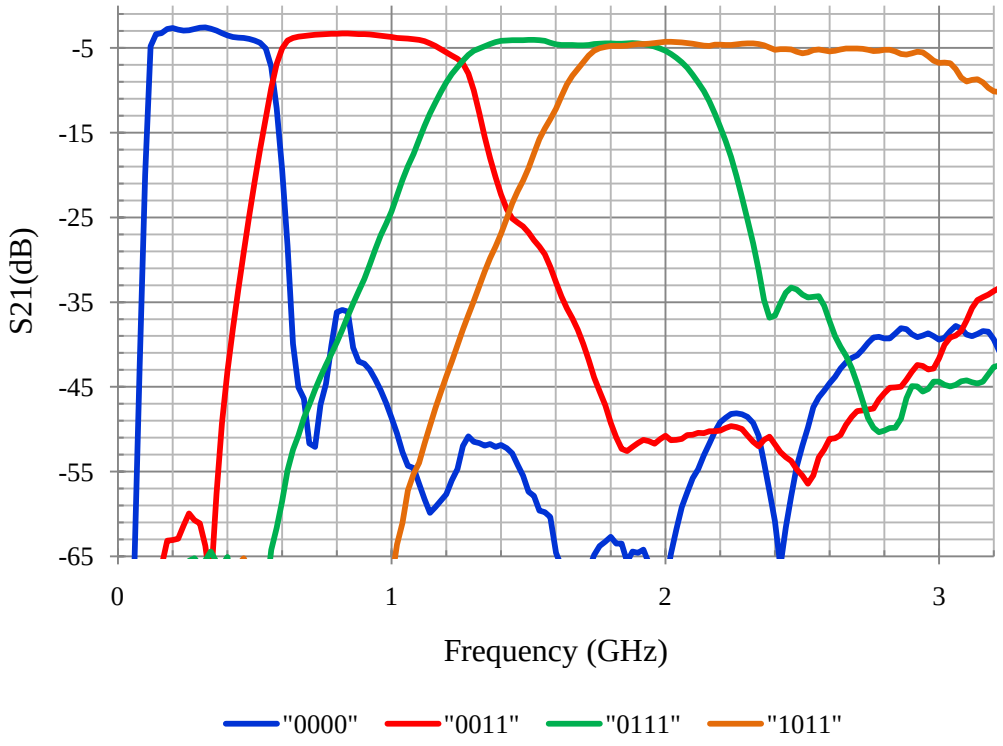

Figure 15: Measured BPF S21. BPF responses for 4-bit digital inputs corresponding to "0000" (blue), "0011" (red), "0111" (green), "1011" (orange), are superimposed

Figure 16 shows the measured S11 of the filter in a similar format to Figure 15. Measurements show almost no difference in the S11 and S22 parameters, therefore S22 parameters have been omitted. The RL is approximately -10 dB or better for the in-band performance of the different BPF responses, indicating a sufficient match.

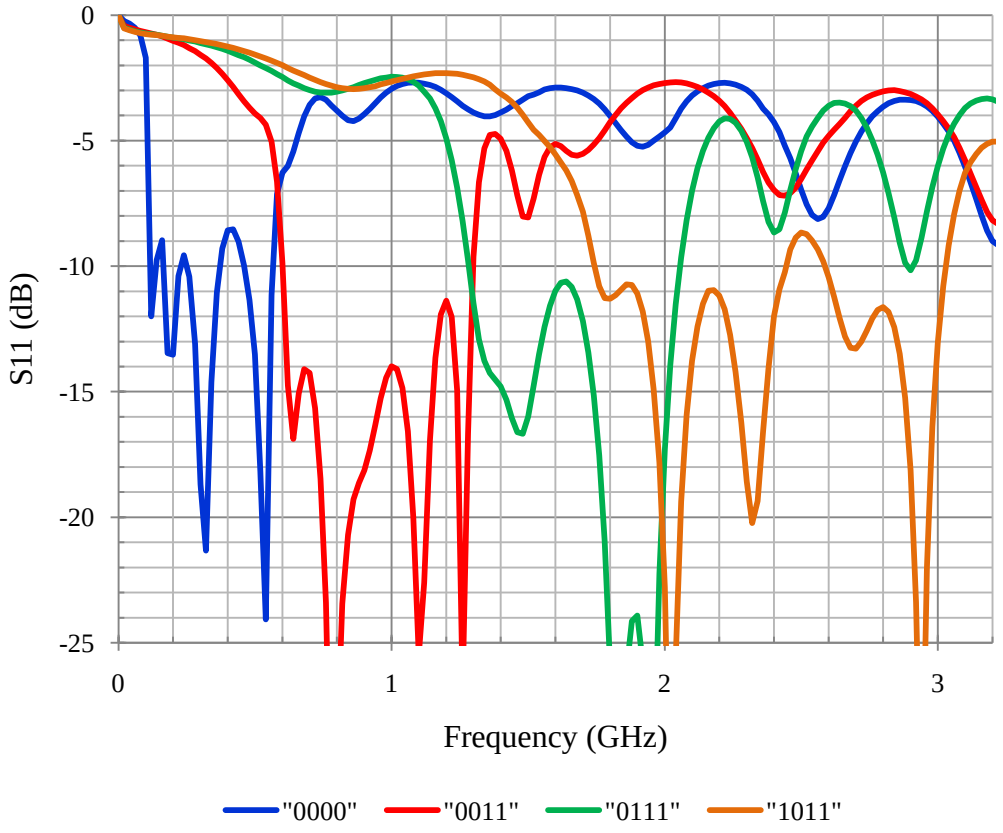

Figure 16: Measured BPF S11. BPF responses for 4-bit digital inputs corresponding to “0000” (blue), “0011” (red), “0111” (green), “1011” (orange), are superimposed

The BPF bank board can easily be controlled by a 4-bit 5 V CMOS/TTL input for filter control in JTRS RFFE. The filter control must be synchronized with the

demodulator array to achieve proper RF signal path through the receiver. Addition of the BPF bank to the receiver will degrade the NF by the IL of the filter (i.e. the NF will be 3.5 dB to 6 dB higher over the 200 MHz to 3.2 GHz range).

Chapter 5: Transmitter

Figure 17 shows the JTRS Transmitter Block Diagram. Baseband I/Q signals feed into a quadrature modulator array of similar construction to the receiver demodulator array. A pair of SPDT AS196-307 RF switches route the I/Q signal to a low-band modulator (I' and Q') or high-band modulator (I'' and Q''). Low-band modulation is achieved with an ADI ADL5385 quadrature modulator (bandwidth from 50 MHz to 2.2 GHz, 500 MHz modulation bandwidth). The high-band modulator is an ADI ADL5375 (bandwidth from 400 MHz to 6.0 GHz). A third AS196-307 RF switch routes the up-converted signal back into the RF chain. The three RF switches are synchronized so that only one of the modulators is in the RF chain at a time.

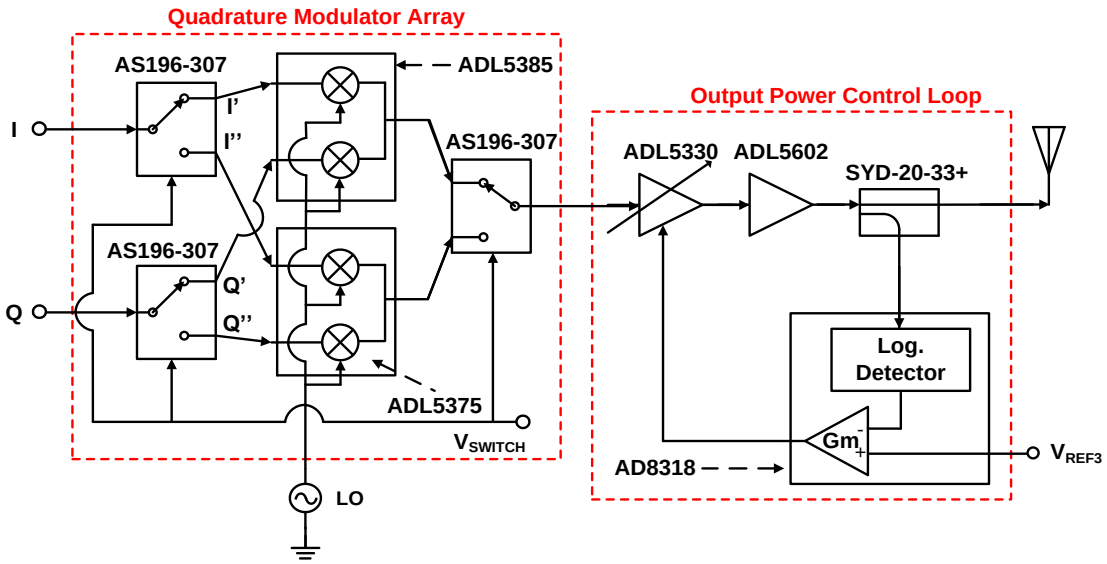

Figure 17: Block Diagram of the JTRS Transmitter

The RF signal power level is controlled by the output power control loop. The power control loop is essentially the same design as the AGC loop in the receiver. Following the modulator array, the RF signal is amplified by the ADL5330 VGA and an ADL5602 gain block. A portion of the signal is split towards the AD8318 logarithmic controller by the SYD-20-33+ wideband direction coupler. An integrated comparator in the AD8318 compares the logarithmic detector's voltage output with V_{REF3}. The closed loop formed by the ADL5330, ADL5602, SYD-20-33+, and the AD8318 settles the output power at the antenna to a level determined by V_{REF3}. The implementation of a wideband power amplifier has not been integrated in the JTRS transmitter. Therefore a limitation in output power and linearity is expected from the transmitter. Figure 18 shows the output power with respect to V_{REF3}.

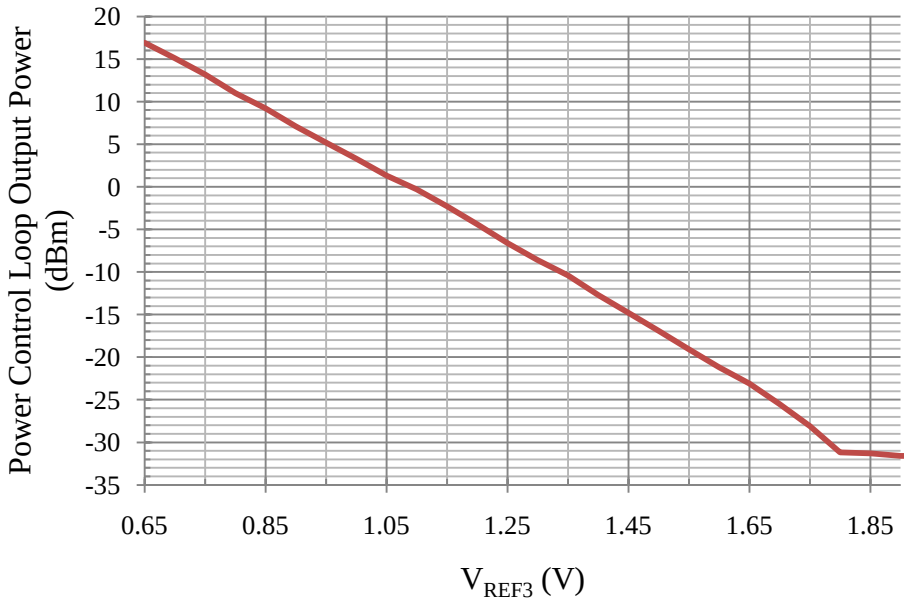

Figure 18: Power Control Loop Output Power vs. V_{REF3}

An I/Q baseband 8PSK (V_I & V_Q = 100 mV_{p-p} differential, 7.776 mega-symbols per second, root-Nyquist filter, α=0.25) signal was used as an input. A 400 MHz LO was used for up-conversion. An output power control range of approximately 48 dB is observed at 400 MHz.

Single-tone and two-tone measurements were performed to evaluate the linearity performance of the transmitter. Figure 19 shows the output 1 dB compression point (OP1dB) and the output third-order intercept point (OIP3) versus frequency. OP1dB achieves a maximum of 19 dBm (at 500 MHz) and remains 15 dB or better out to 2 GHz. OP1dB degrades to 13 dBm at 3.2 GHz.

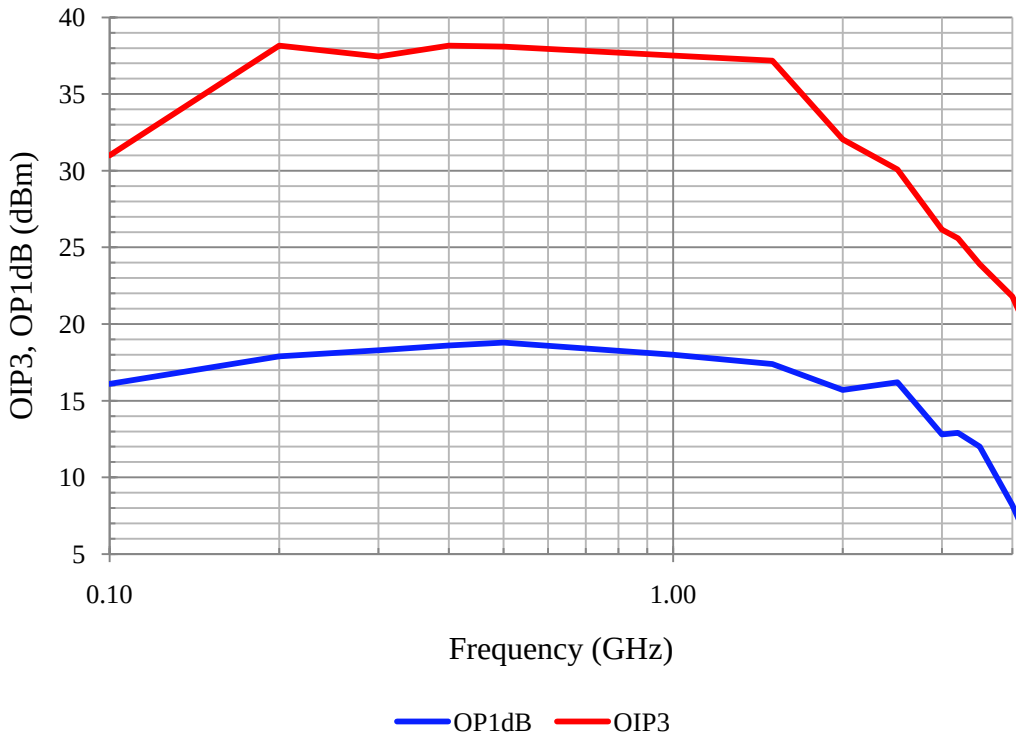

Figure 19: OP1dB and OIP3 vs. frequency

OIP3 achieves a maximum of 38 dBm at 200 MHz and 400 MHz, and remains above 37 dBm out to 1.5 GHz. The OIP3 degrades to 26 dBm at 3.2 GHz. The primary source of OP1dB and OIP3 degradation is from the ADL5330 VGA. The JTRS transmitter suffers in linearity performance at approximately the same frequencies as the ADL5330. The ADL5330 was designed primarily for variable gain control applications (the ADL5330's OIP3 drops from 31.5 dBm at 900 MHz to 21.2 dBm at 2.2 GHz, and OP1dB drops from 22.3 dBm at 900 MHz to 14 dBm at 2.2 GHz).

Figure 20 shows the low- and high-power limits and the DR of the transmitter versus frequency. P_{HIGH} is the maximum output power of the transmitter at the antenna which maintains an ACP of -40 dBc with the same 8PSK input signal used in the power control loop output power measurements and channel definitions used for the receiver measurements (primary and adjacent channel bandwidths of 8.6 MHz and channel spacing of 10.56 MHz). P_{LOW} is the lowest output power the control loop can be driven to. The lower power limitation originates from the limited dynamic range of the ADL5330. The dynamic range of the transmitter is defined here as the difference between P_{HIGH} and P_{LOW}. The maximum output power that avoids unacceptable adjacent channel contamination (-40 dBc) is 17 dBm at 400 MHz. The transmitter output power is capable of being maintained at 12 dBm or greater out to 2.5 GHz where it begins to experience degradation caused by the ADL5330 VGA maximum output power limitations. This same degradation is observed to affect the lower attainable output power threshold. However, the dynamic range remains fairly constant throughout the JTRS RFFE frequency range.

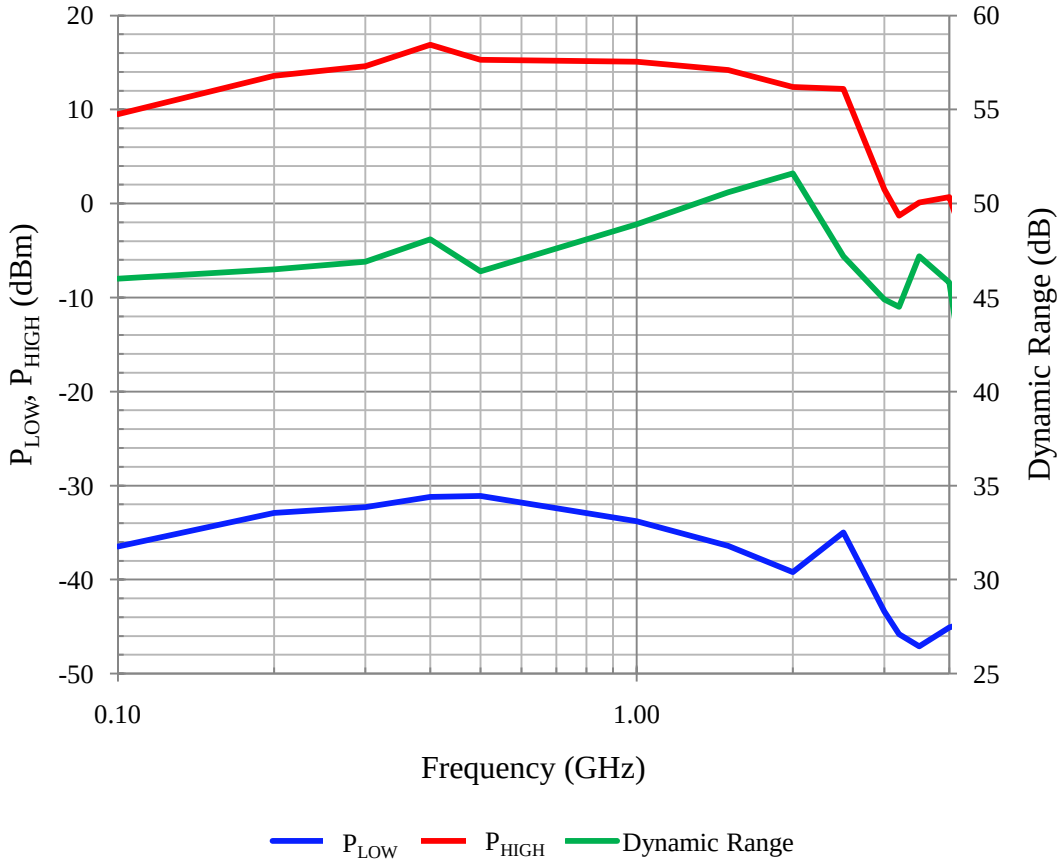

Figure 20: Transmitter P_{HIGH}, $P_{LOW,}$ and Dynamic Range vs. Frequency. P_{HIGH} (red) and P_{LOW} (blue) are plotted with respect to the left vertical axis while the Dynamic Range is plotted with respect to the right vertical axis

The dynamic range remains higher than 44 dB throughout the entire frequency range (200 MHz to 3.2 GHz) and obtains its maximum value of 52 dB at 2 GHz.

The EVM of the transmitter versus frequency for several output powers is shown in Figure 21. The EVM performance of the transmitter is excellent, remaining below -40 dB for higher output powers greater than -10 dBm. The MXA signal analyzer exhibits a limitation in its low input signal range which increases SNR of the measured signal and degrades EVM measurements at low transmitter output powers.

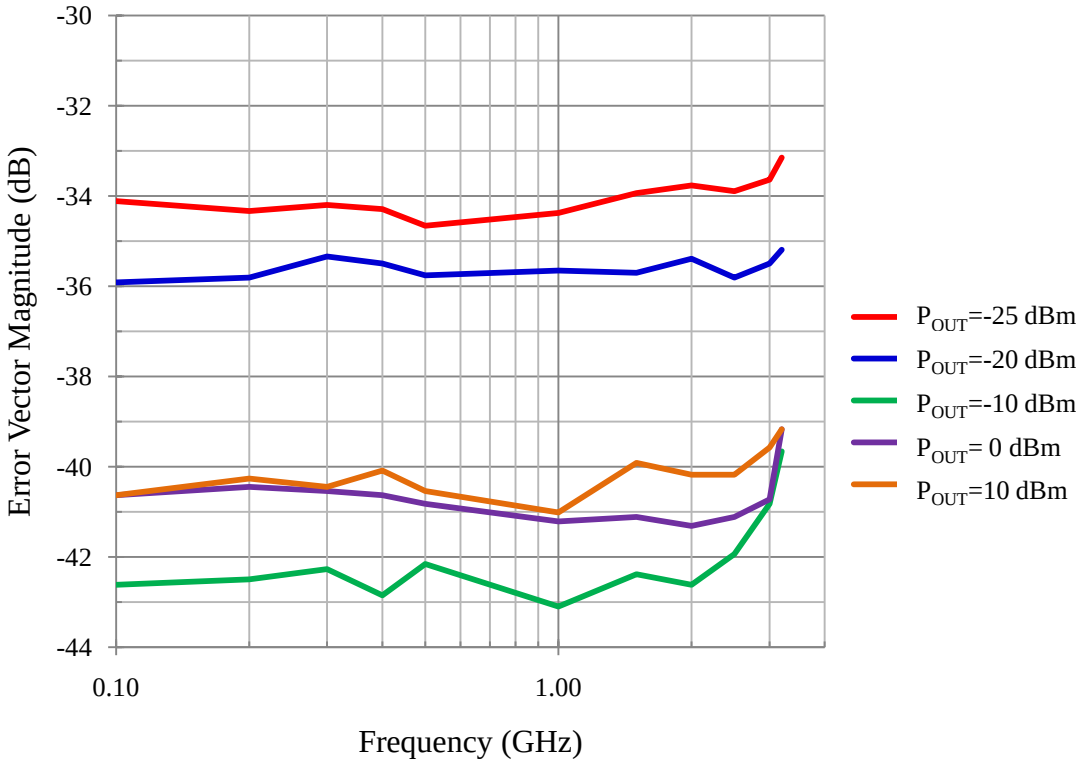

Figure 21: Transmitter Error Vector Magnitude vs. Frequency. Results for several output powers are shown

The transmitter demonstrates excellent wideband performance across the entire JTRS RFFE frequency range and features two points of control for SDR application. The quadrature modulator array can be configured for low- or high-band modulation by providing a 5V CMOS/TTL signal to V_{SWITCH}. The output power level of the transmitter can be adjusted by a DAC output at V_{REF3} (0.65 V to 1.8 V) for up to 52 dB of power control.

Chapter 6: Local Oscillator Synthesizer

Wideband frequency hopping of the JTRS RFFE can be achieved by switching the LO frequency during signal transmission and reception. True end-to-end frequency hopping (from transmitted data to received data) can only be achieved once a software transmitter and receiver have been properly configured to interface with a frequency hopping-*capable* RFFE. The software system would synchronize data transmission, reception, digital demodulation, and error-correction with LO-controlled frequency hopping while taking into account the performance capabilities and limitations of a frequency hopping-capable RFFE. The LO synthesizer presented here has been designed to enable frequency hopping of the JTRS RFFE.

Figure 22 shows a block diagram of the Local Oscillator Synthesizer. An ADI AD9959 Direct Digital Synthesizer (4 channels, 4 DDS cores, 4 10-bit DACs, 500 mega samples per second) is used to create a signal between 100 MHz and 200 MHz. The AD9959 uses a static frequency low-phase noise 500 MHz sine wave generated by an ADI ADF4350 Phase-Locked Loop Wideband Synthesizer as a reference clock. The 100 MHz – 200 MHz signal propagates through 4 octave doubling chains, doubling the range of available frequencies at the end of each chain (i.e. 200 MHz to 400 MHz at the end of the first, 400 MHz to 800 MHz at the end of the second, etc.). Using this LO synthesizer architecture, LO signals with frequencies from 200 MHz to 3.2 GHz can be obtained.

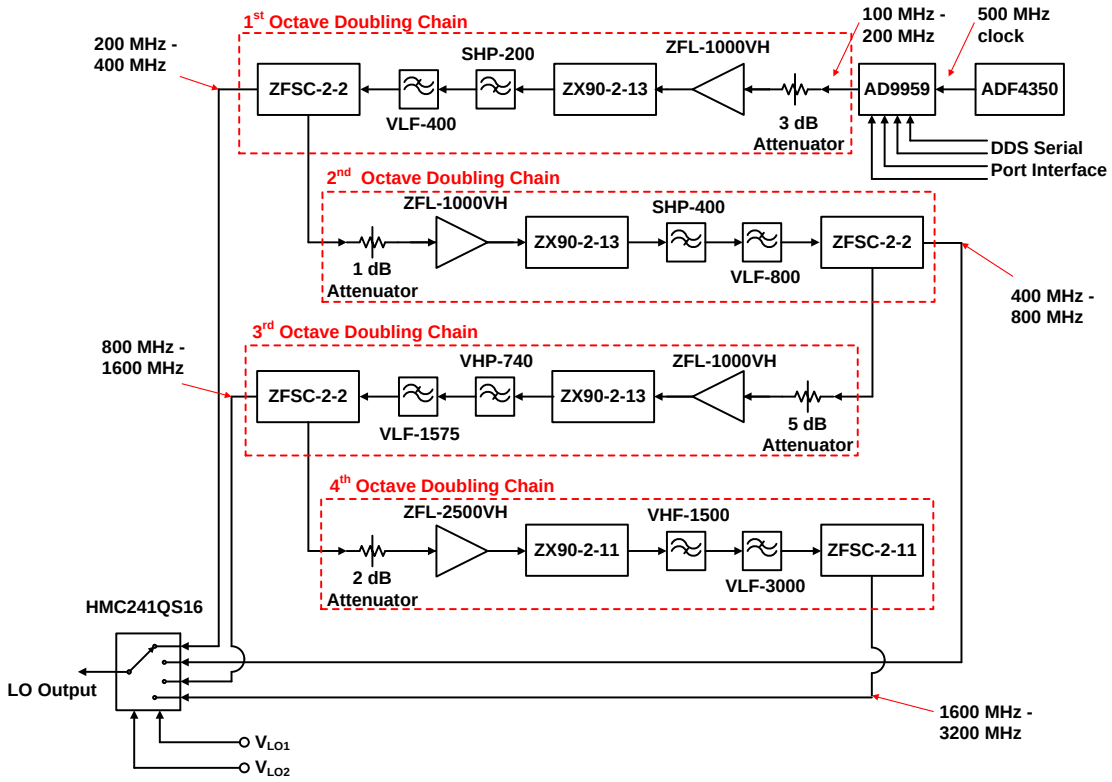

Figure 22: Block Diagram of the Local Oscillator Synthesizer

Each doubling chain consists of an attenuator, wideband amplifier, wideband frequency multiplier (which provides doubling), high- and low-pass filters, and a wideband power-splitter. All components in the doubling chains are manufactured by Mini-Circuits (see bill of materials in the appendix for details). The frequency multipliers are designed to provide a large second harmonic output from a fundamental input frequency. However, the frequency multipliers are capable of generating large spurs if an optimal power in not used at its input. The attenuator and amplifier cascades before the multipliers were chosen to minimize spurs in each octave chain. The HPF and LPF cascade after the multipliers help to further minimize undesired spurious content generated by the multipliers. A wideband power-splitter at the end of each

chain is used to create a tap to access the octave chain outputs. The octave chain outputs are routed to a Hittite Microwave HMC241QS16 SP4T absorptive RF switch (bandwidth from DC to 3.5 GHz) to enable LO synthesizer octave selection. The switch's absorptive inputs maintain a 50 Ω termination at inactive switch throws for the split port output of the octave chain power-splitters. Using a reflective switch instead would cause a mismatch at all of the inactive switch throws, leading to large standing-waves generated throughout the LO synthesizer RF chain and unacceptable spurious content at the LO output. The HMC241QS16 RFIC features an integrated 2-to-4 decoder to simplify active throw selection. Therefore, no additional switch logic was necessary to chose the LO octave output. V_{LO1} and V_{LO2} are 5V CMOS/TTL inputs available for throw selection. Table 1 shows the LO octave chain output selection truth table.

Table 1: LO Octave Chain Output Selection Truth Table

V_{LO1}	**V_{LO2}**	**LO Output**
Low	Low	200 MHz - 400 MHz (1st octave doubling chain)
Low	High	400 MHz - 800 MHz (2nd octave doubling chain)
High	Low	800 MHz - 1600 MHz (3rd octave doubling chain)
High	High	1600 MHz - 3200 MHz (4th octave doubling chain)

Measurements of the 4th octave doubling chain were obtained by using the AD9959 evaluation kit. The evaluation kit consisted of a evaluation board with universal serial bus (USB)-to-serial port interface circuitry, manual control profile

headers, and a Microsoft Windows application featuring a graphical user interface (GUI) to program the DDS output (via USB). 2-level LO frequency hopping (between f_1 and f_2) was obtained by programming the DDS core to switch between 2 frequencies via the USB interface using the supplied AD9959 Windows GUI. 2-level frequency hopping required only one bit of the profile header to be toggled. The manual-control jumpers on the AD9959 evaluation board were enabled and a square wave generator was used to drive the frequency switching between the two stored frequencies. Consequently, the square wave frequency corresponded directly to the hopping rate.

Figure 23 shows the LO settling time versus frequency hopping distance in the 4^{th} octave chain. The frequency hopping occurred between f_1 and f_2; f_1 was fixed at 1.6 GHz and f_2 varied from 1.7 GHz to 3.2 GHz. A steadily increasing settling time with respect to hop distance can be observed in the 4^{th} octave LO signal. The primary cause of the settling time increase comes from the band-limiting effect of the LPFs in the cascade. LPFs are known to cause ringing in response to impulse and step inputs [6]. The ringing is caused from filtering of high frequency components which are present in impulse and step response outputs. The magnitude of ringing, and consequently settling time, increases as the band-limiting becomes more severe. The 4 octave pass-band is fixed between 1.55 GHz and 3.6 GHz (3 dB cutoffs: $f_{C\text{-}LOW}$=1.550 GHz and $f_{C\text{-}HIGH}$=3.6 GHz). As the hop distance is increased, the frequency of the second hop (f_2) increases. Therefore, f_2 sees more band-limiting and experiences more ringing and a larger settling time as it approaches the static low-pass cut-off frequency. Despite the

presence of ringing, the settling time was measured to be as low as 13 ns for a 100 MHz hop and 700 ns for a 1.6 GHz hop.

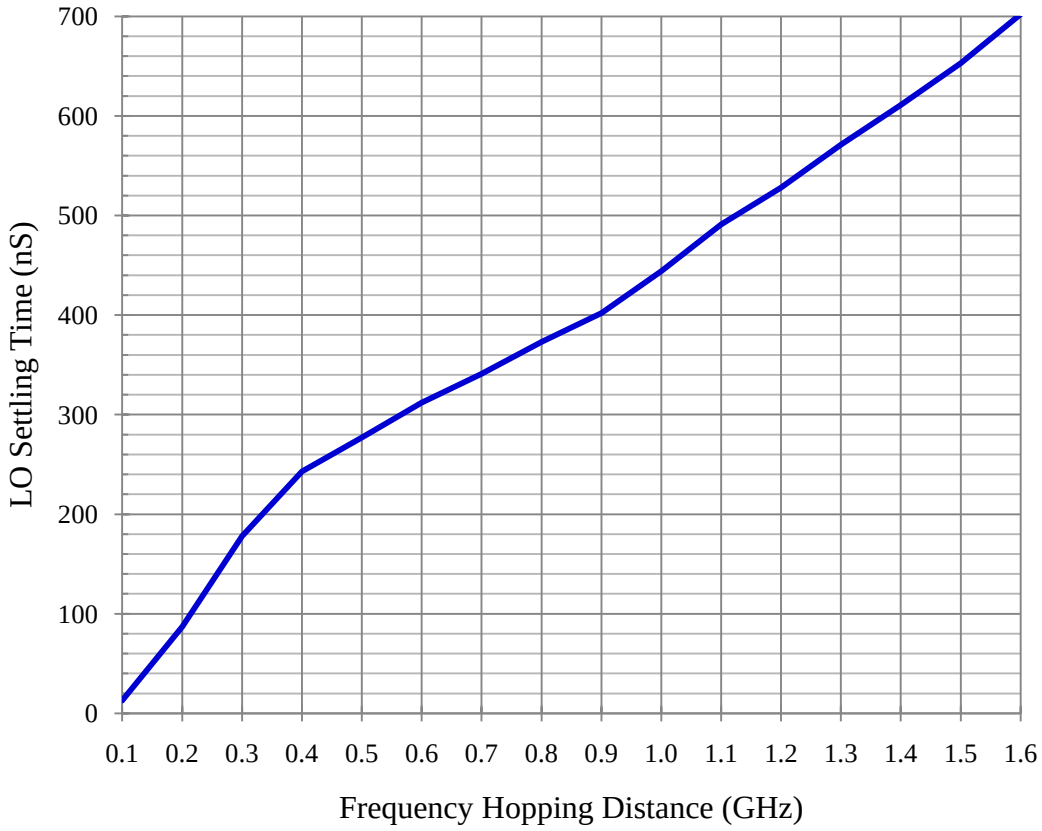

Figure 23: LO Settling Time vs. Frequency Hopping Distance

Figure 24 shows the LO phase noise versus the carrier frequency measured with a 1 MHz offset. The phase noise was measured in the pass-band of each octave chain and concatenated in Figure 23. The phase noise increases as the carrier frequency increases due to the large amount of gain (up to 80 dB) the initial DDS output (100 MHz to 200 MHz) experiences as it propagates down all 4 octave chains. The ZFL-

1000VH and ZFL-2500VH amplifiers exhibit a noise figure of 5 dB (each), adding both amplitude and phase noise to the LO output. The LO phase noise is -138 dBc/Hz at a carrier frequency of 100 MHz and increases to -120 dBc/Hz at 3.2 GHz.

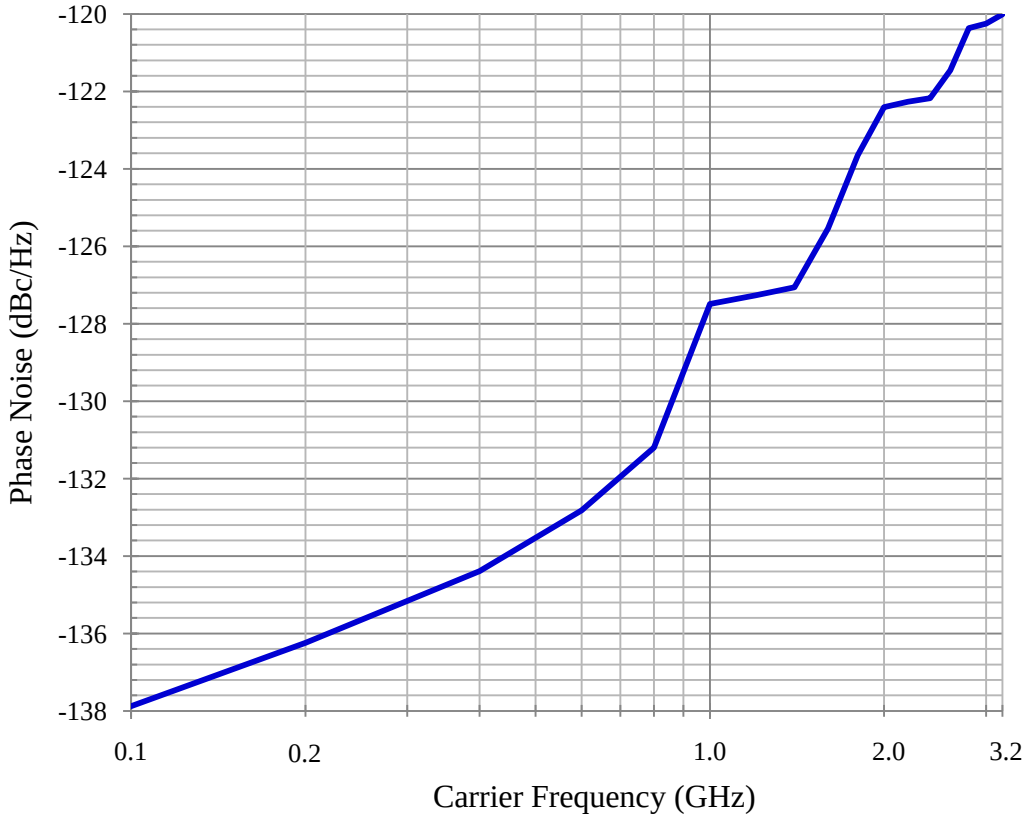

Figure 23: LO Phase Noise vs. Carrier Frequency

The LO synthesizer features two points for SDR control. The DDS core can be programmed to generate a sine wave from 100 MHz to 200 MHz through a serial port interface. The SP4T HMC241Q16 RF switch allows selection of one of the four octave chains to be routed to the LO synthesizer output through two 5V CMOS/TTL inputs,

V_{LO1} & V_{LO2}. The synthesizer is capable of producing a sine wave output across the entire JTRS frequency range (from 200 MHz to 3.2 GHz). Measurements were performed demonstrating the synthesizer's capability to hop up to a 1.6 GHz distance in frequency. In principal, the LO synthesizer is capable of hopping between the entire JTRS frequency range if the frequency hop is synchronized with a change in V_{LO1} and V_{LO2} to switch the output between octaves chains.

Chapter 7: System Performance Summary

Table 2 shows a table summarizing the performance of the JTRS RFFE. The table provides a comparison to other wideband SDR transceivers. Note that frequency hopping is a unique capability of the Calit2 JTRS RFFE design among the comparisons.

Table 2: JTRS RFFE Performance Summary and Comparison

Ref.	**[5]**	**[7]**	**[8]**	**This work**
Freq.	1.8 & 5~6 GHz	0.1~6 GHz	0.1~2.5 GHz	0.2~3.2 GHz
Rx NF	4~8 dB	4.8~8.5 dB	7 dB	3.3~6.3 dB
Rx Gain	10~90 dB	10~90 dB	48 dB	-8~86 dB
Rx IIP2	Not available	Not available	60 dBm	Not measured
Rx IIP3	-9 dBm	-8.2 ~ -3 dBm	-6 dBm	Not measured
Rx EVM	Not available	Not available	Not available	8PSK < -40 dB
Rx current	62~120 mA	27~82 mA	40 mA	1.23 A
Tx Pout	-13~ -17 dBm	1~5.8 dBm	6 dBm	-31.2 ~17 dBm
Tx OIP3	-1~ -5 dBm	12~15.5 dBm	Not available	>25.6 dBm
Tx Id	56~89 mA	53.7~83.1 mA	40~90 mA	840 mA
Tx EVM	64QAM : -33 dB	64QAM: -29.5~ -30.6 dB	DPQSK: -40 dB	8PSK: < -33 dB
Chan. BW	Rx:350 KHz ~23 MHz Tx:1MHz~16MHz	20 MHz	8 KHz~20 MHz	25 KHz~100 MHz
LO phase Noise	-119~ -114 dBc/Hz @ 1MHz	-119~ -114 dBc/Hz @ 1MHz	-123 dBc/Hz @ 25 KHz	< -120 dBc/Hz @ 1 MHz
LO Frequency hop distance	Not available	Not available	Not available	1.6 GHz (with < 700 ns settling time)
LO Current	2.12~7.68 mA	2.12~7.68 mA	80 mA	1.68 A

Chapter 8: Future Work and Conclusion

A variety of implementation and design tasks remain to integrate the JTRS RFFE onto a single printed circuit board. While the receiver system is essentially complete, the transmitter lacks a power amplifier for high-power transmission of a wireless signal. Care must be taken to find either a single wideband power amplifier or a method to network several power amplifiers to provide complete coverage of the JTRS frequency range. Additionally, discrete filters in the BPF bank should be designed to provide sharper pass-band roll-off, improved isolation, and tighter band-pass response overlap with respect to adjacent filters in the frequency domain. This can allow for improved channel selection and rejection of interfering signals. Finally, the LO synthesizer should be implemented in an evaluation board form utilizing an improved version of the BPF bank at the LO output to eliminate spurs created by the frequency multipliers in the octave doubling chains. Lower LO synthesizer power consumption can also be expected from utilizing discrete SMD components.

Additional measurements remain to completely characterize the JTRS RFFE. Measurements of the receiver's input second-order intercept point (IIP2) and IIP3 can help provide a thorough characterization of the receiver linearity performance. Although effort was taken to choose RF switches with high linearity performance in the BPF bank, measurements (e.g. IP2, IP3, EVM, ACP, etc.) should be performed to verify linearity. Finally, measurements of the settling time vs. frequency hop distance in the 1^{st}, 2^{nd}, and 3^{rd} octaves should be performed to completely characterize the hopping performance between different octave bands.

The JTRS RFFE demonstrates a wideband high-dynamic range frequency hopping-capable hardware system for application in JTRS SDR platforms. The RFFE features several points of control for dynamic reconfiguration and adjustment of the RF chains which can be easily controlled by software through 5V CMOS/TTL, serial, or ADC outputs. The JTRS RFFE possesses the ability to frequency hop if controlled by a software system that can synchronize signal transmission/reception, demodulation, and perform error corrections.

Appendices

Appendix A: Bill of Materials and Systems Power Consumption

Table 3: Receiver Bill of Materials and Power Consumption

Manuf.	Part name	Description	#	Supply Current (A)	Supply Voltage (V)	Power (W)	Total Power (W)
Analog Devices Inc.	ADL5602	Gain Block	4	1.06E-01	5	5.30E-01	2.12E+00
Analog Devices Inc.	AD8318	Logarithmic Controller	2	8.20E-02	5	4.10E-01	8.20E-01
Analog Devices Inc.	ADL5330	Variable Gain Amplifier	1	2.15E-01	5	1.08E+00	1.08E+00
Analog Devices Inc.	ADL5387	Low-band Demodulator	1	1.80E-01	5	9.00E-01	9.00E-01
Analog Devices Inc.	ADL5380	High-band Demodulator	1	2.45E-01	5	1.23E+00	1.23E+00
Skyworks Solutions	AS196-307	RF SPDT Switch	5	1.00E-04	5	5.00E-04	2.50E-03
Mini-Circuits	SYD-20-33+	Directional Coupler	2				
Mini-Circuits	LAT-20+	20 dB SMD Attenuator	1				
Total Receiver Power							6.14 W

Table 4: Transmitter Bill of Materials and Power Consumption

Manuf.	Part name	Description	#	Supply current (A)	Supply Voltage (V)	Power (W)	Total Power (W)
Skyworks Solutions	AS196-307	RF SPDT Switch	3	1.00E-04	5	5.00E-04	1.50E-03
Analog Devices Inc.	ADL5385	Low-band Modulator	1	2.40E-01	5	1.20E+00	1.20E+00
Analog Devices Inc.	ADL5375	High-band Modulator	1	2.00E-01	5	1.00E+00	1.00E+00
Analog Devices Inc.	AD5530	Variable Gain Amplifier	1	2.15E-01	5	1.08E+00	1.08E+00
Analog Devices Inc.	ADL5602	Gain Block	1	1.06E-01	5	5.30E-01	5.30E-01
Analog Devices Inc.	AD8318	Logarithmic Controller	1	8.20E-02	5	4.10E-01	4.10E-01
Mini-Circuits	SYD-20-33+	Directional Coupler	1				
Total Transmitter Power							4.22 W

Table 5: Band-Pass Filter Board Bill of Materials and Power Consumption

Manuf.	Part name	Description	#	Supply current (A)	Supply Voltage (V)	Power (W)	Total Power (W)
NXP	74HTC4514	4-to-16 decoder	1	8.00E-06	5	4.00E-05	4.00E-05
NXP	HEF4072B	Dual 4-input OR gate	2	5.00E-06	5	2.50E-05	5.00E-05
Skyworks Solutions	SKY13322-375LF	RF SP4T Switch	10	5.00E-06	5	2.50E-05	2.50E-04
Mini-Circuits	RHP-122	SMD HPF	1				
Mini-Circuits	RHP-250	SMD HPF	1				
Mini-Circuits	HFCN-440+	SMD HPF	1				
Mini-Circuits	HFCN-650+	SMD HPF	1				
Mini-Circuits	HFCN-880+	SMD HPF	2				
Mini-Circuits	HFCN-1200+	SMD HPF	1				
Mini-Circuits	HFCN-1300+	SMD HPF	1				
Mini-Circuits	HFCN-1500+	SMD HPF	1				
Mini-Circuits	HFCN-1600+	SMD HPF	1				
Mini-Circuits	HFCN-1810+	SMD HPF	1				
Mini-Circuits	HFCN-1910+	SMD HPF	1				
Mini-Circuits	HFCN-2000+	SMD HPF	1				
Mini-Circuits	HFCN-2275+	SMD HPF	1				
Mini-Circuits	HFCN-2700+	SMD HPF	2				
Mini-Circuits	LFCN-400+	SMD LPF	1				
Mini-Circuits	LFCN-600+	SMD LPF	1				
Mini-Circuits	LFCN-800+	SMD LPF	1				
Mini-Circuits	LFCN-1000+	SMD LPF	1				
Mini-Circuits	LFCN-1200+	SMD LPF	1				
Mini-Circuits	LFCN-1400+	SMD LPF	1				
Mini-Circuits	LFCN-1700+	SMD LPF	1				

Table 5: Continued

Manuf.	Part name	Description	#	Supply current (A)	Supply Voltage (V)	Power (W)	Total Power (W)
Mini-Circuits	LFCN-1800+	SMD LPF	1				
Mini-Circuits	LFCN-2000+	SMD LPF	1				
Mini-Circuits	LFCN-2250+	SMD LPF	1				
Mini-Circuits	LFCN-2400+	SMD LPF	1				
Mini-Circuits	LFCN-2600+	SMD LPF	1				
Mini-Circuits	LFCN-3000+	SMD LPF	2				
Mini-Circuits	LFCN-3400+	SMD LPF	1				
Mini-Circuits	LFCN-3900+	SMD LPF	1				
Total Band-Pass Filter Board Power							340 μW

Table 6: Local Oscillator Synthesizer Bill of Materials and Power Consumption

Manuf.	Part name	Description	#	Supply current (A)	Supply Voltage (V)	Power (W)	Total Power (W)
Analog Devices Inc.	ADF4350	Phase-Locked Loop	1	7.00E-02	3.3	2.31E-01	2.31E-01
Analog Devices Inc.	AD9959	Direct-Digital Synthesizer	1	2.20E-01, 1.00E-02	1.8, 3.3	4.30E-01	4.30E-01
Mini-Circuits	ZFL-1000VH	Med. Power Amplifier	3	3.20E-01	15	4.80E+00	1.44E+01
Mini-Circuits	ZFL-2500VH	Med. Power Amplifier	1	3.00E-01	15	4.50E+00	4.50E+00
Mini-Circuits	ZX90-2-11	Frequency Multiplier	1				
Mini-Circuits	ZX90-2-13	Frequency Multiplier	3				
Mini-Circuits	ZFSC-2-2	Power Splitter	3				
Mini-Circuits	ZFSC-2-11	Power Splitter	1				
Mini-Circuits	UNAT-1	1 dB Coaxial Attenuator	1				
Mini-Circuits	UNAT-2	2 dB Coaxial Attenuator	1				
Mini-Circuits	UNAT-3	3 dB Coaxial Attenuator	1				

Table 6: Continued

Manuf.	Part name	Description	#	Supply current (A)	Supply Voltage (V)	Power (W)	Total Power (W)
Mini-Circuits	UNAT-5	5 dB Coaxial Attenuator	1				
Mini-Circuits	SHP-200	Coaxial HPF	1				
Mini-Circuits	SHP-400	Coaxial HPF	1				
Mini-Circuits	VLF-740	Coaxial HPF	1				
Mini-Circuits	VHF-1500	Coaxial HPF	1				
Mini-Circuits	VLF-400	Coaxial LPF	1				
Mini-Circuits	VLF-800	Coaxial LPF	1				
Mini-Circuits	VLF-1575	Coaxial LPF	1				
Mini-Circuits	VLF-3000	Coaxial LPF	1				
Hittite Microwave	HMC241QS16	RF SP4T Switch	1				
Total Local Oscillator Synthesizer Power							19.6 W

Appendix B: BPF Circuit Schematic

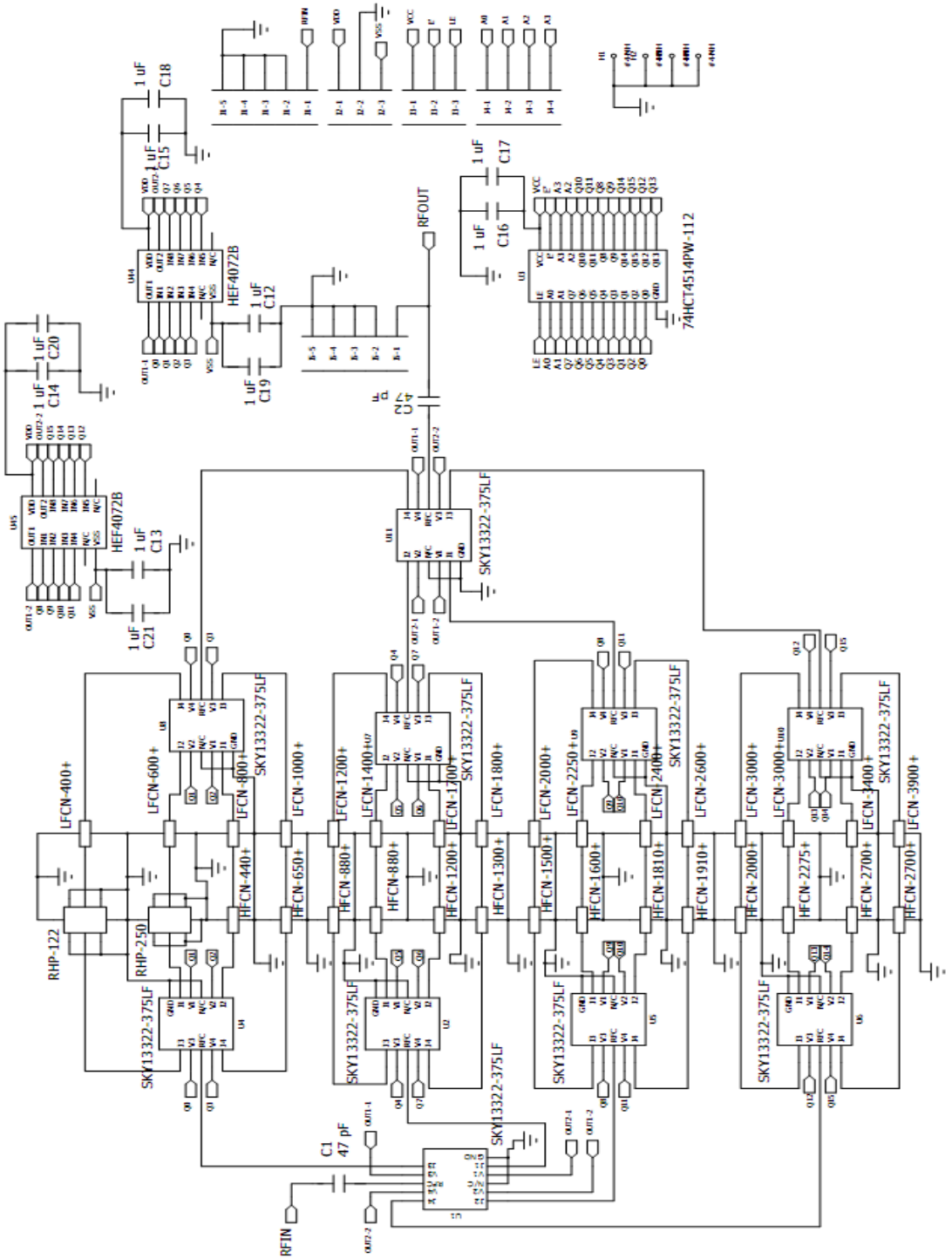

Figure 25: Band-Pass Filter Schematic

Appendix C: Band-Pass Filter S11 and S22

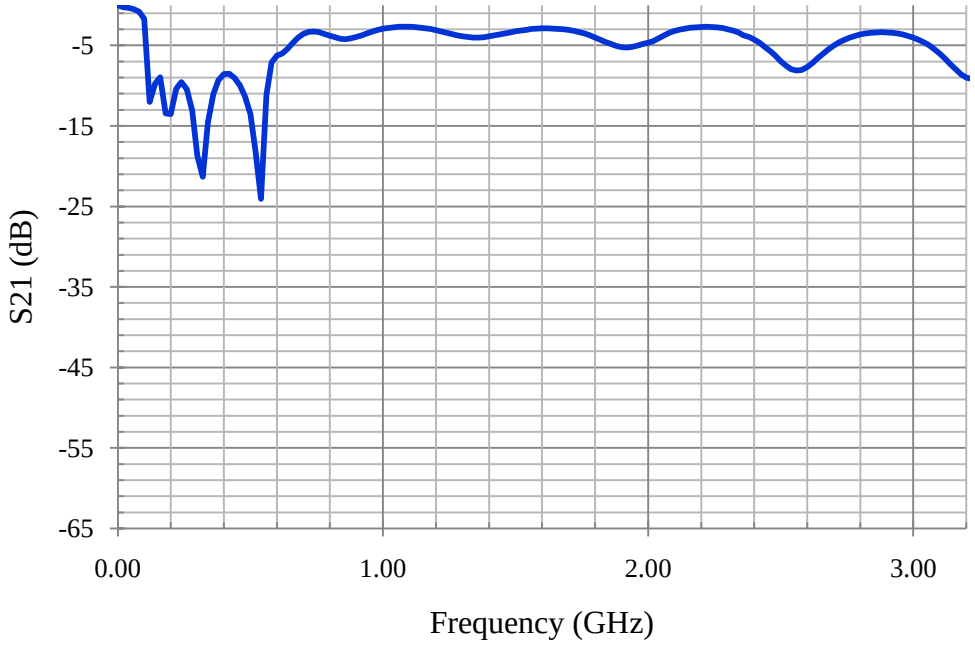

Figure 26: Band-Pass Filter S21, “0000”

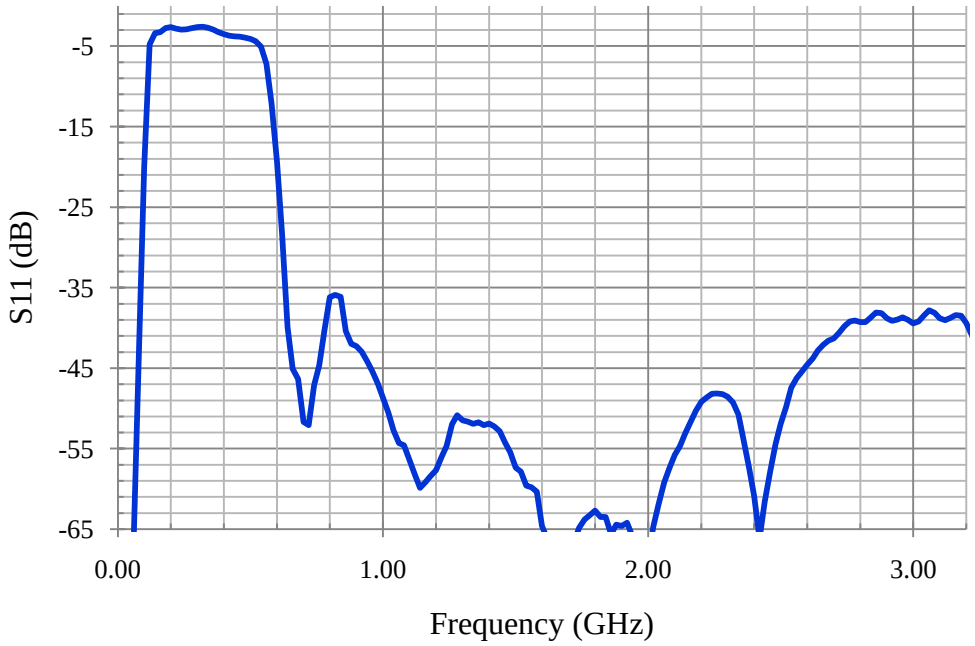

Figure 27: Band-Pass Filter S11, “0000”

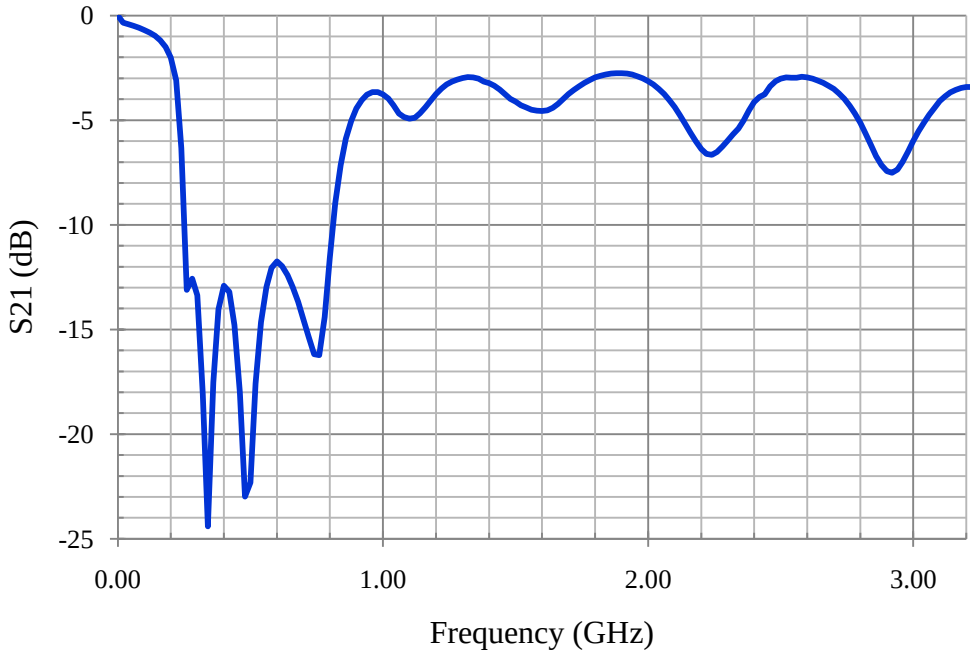

Figure 28: Band-Pass Filter S21, “0001”

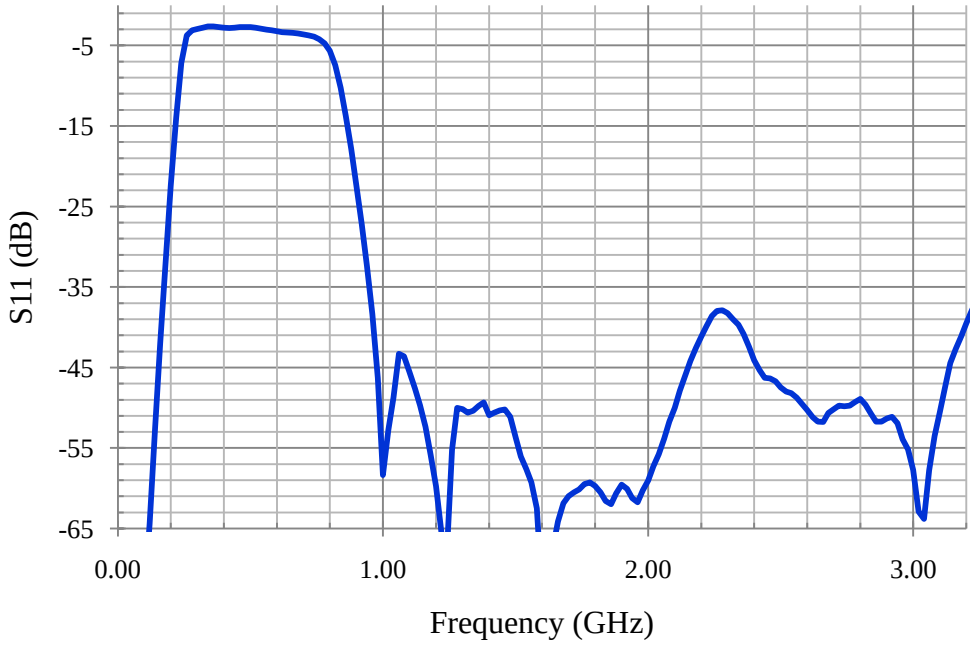

Figure 29: Band-Pass Filter S11, “0001”

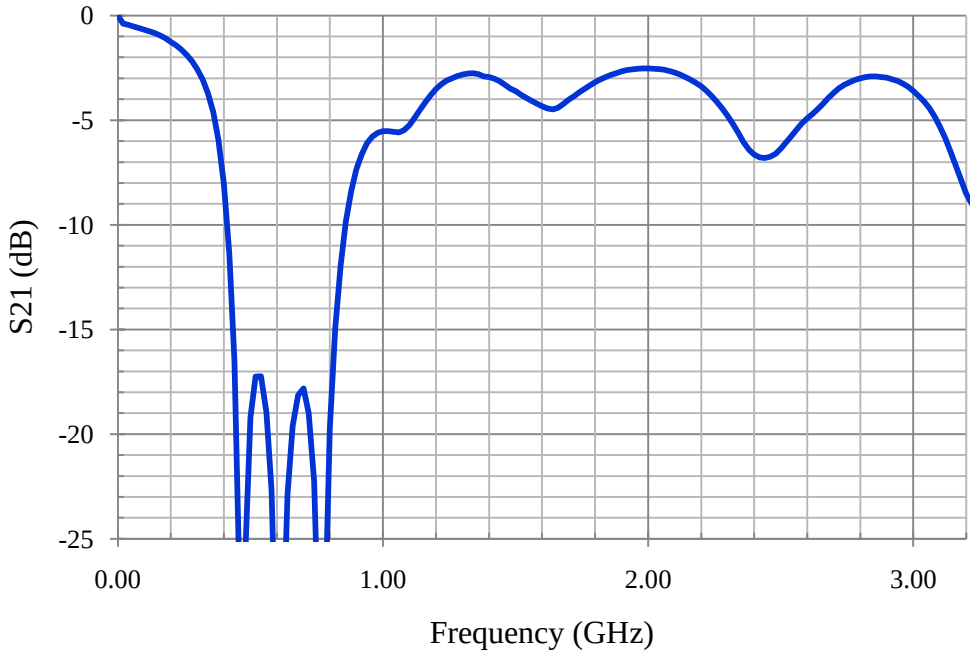

Figure 30: Band-Pass Filter S21, “0010”

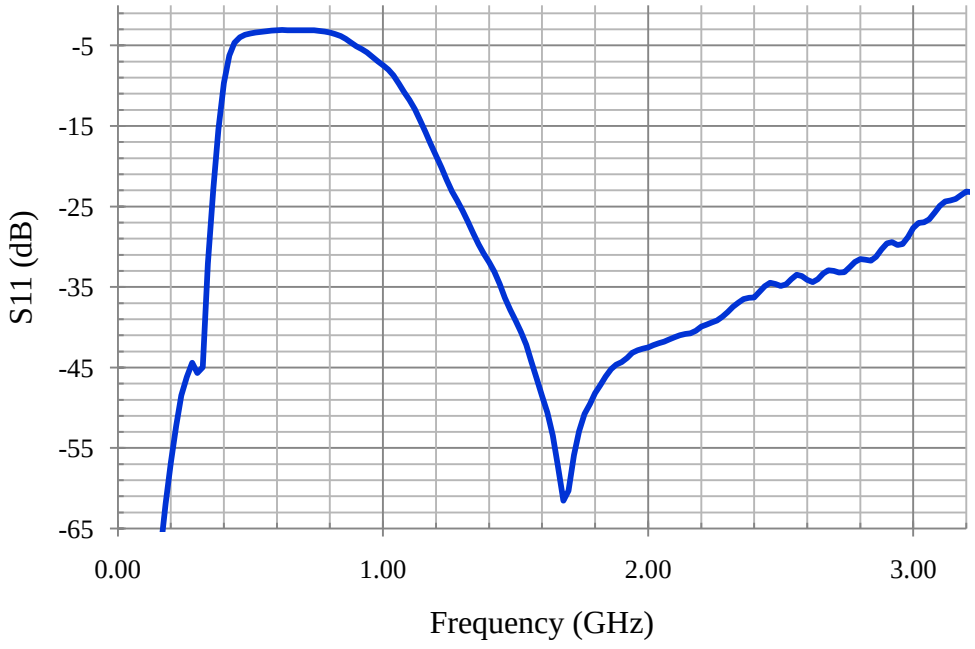

Figure 31: Band-Pass Filter S11, “0010”

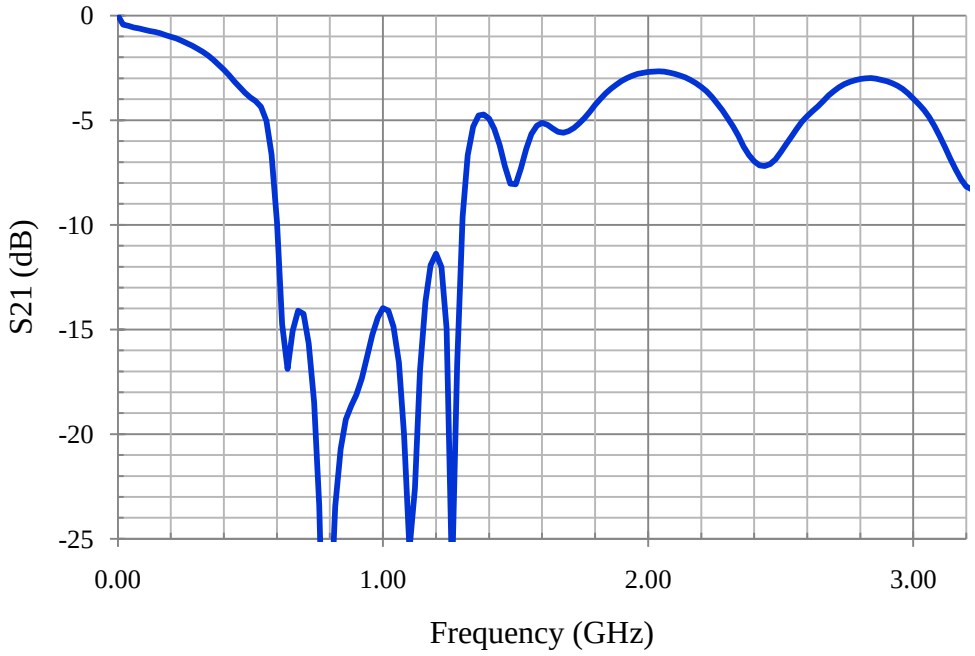

Figure 32: Band-Pass Filter S21, “0011”

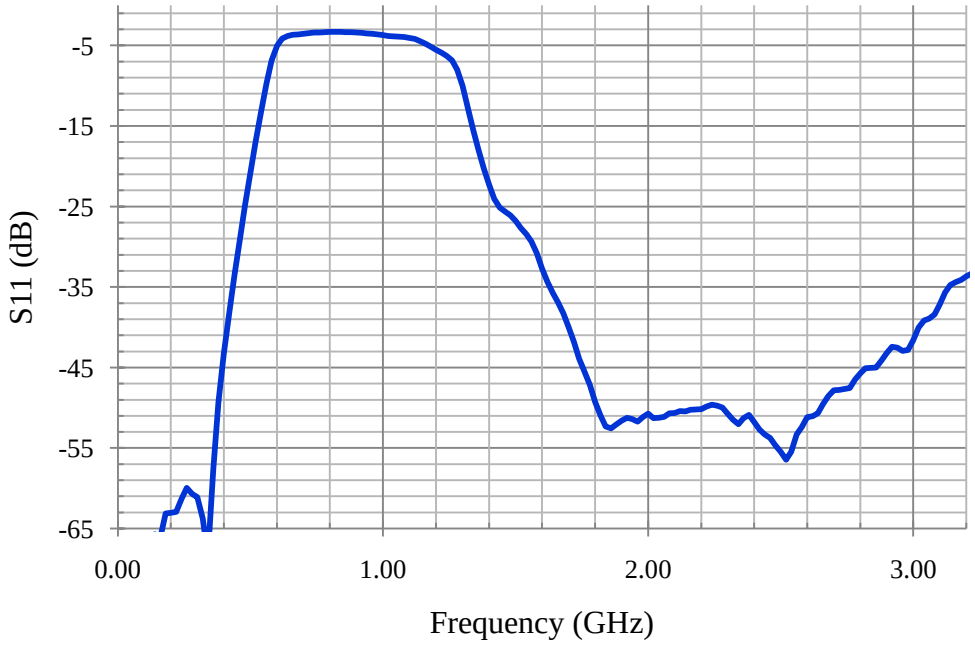

Figure 33: Band-Pass Filter S11, “0011”

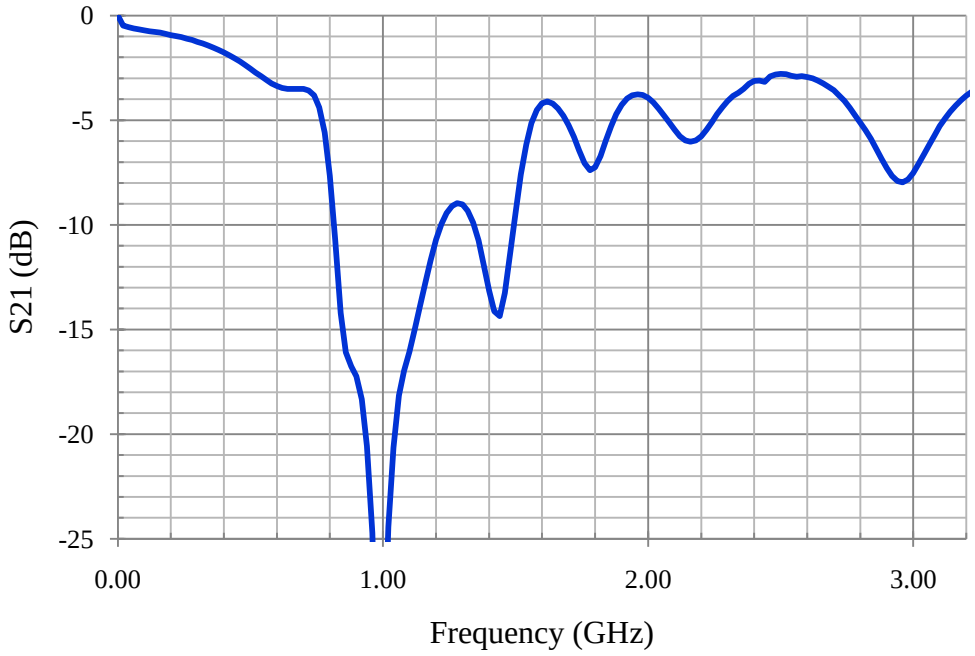

Figure 34: Band-Pass Filter S21, “0100”

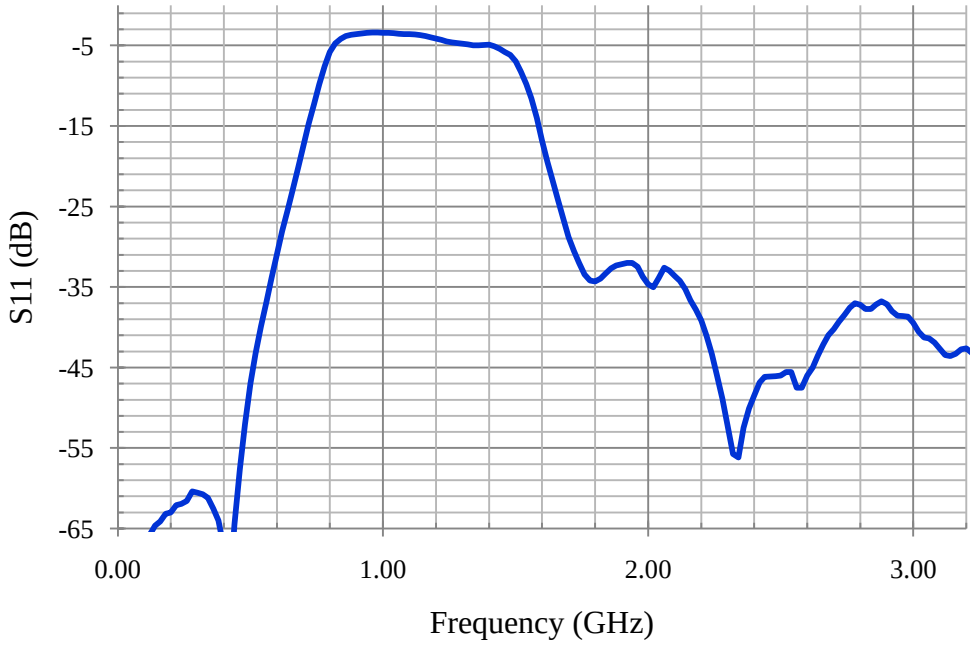

Figure 35: Band-Pass Filter S11, “0100”

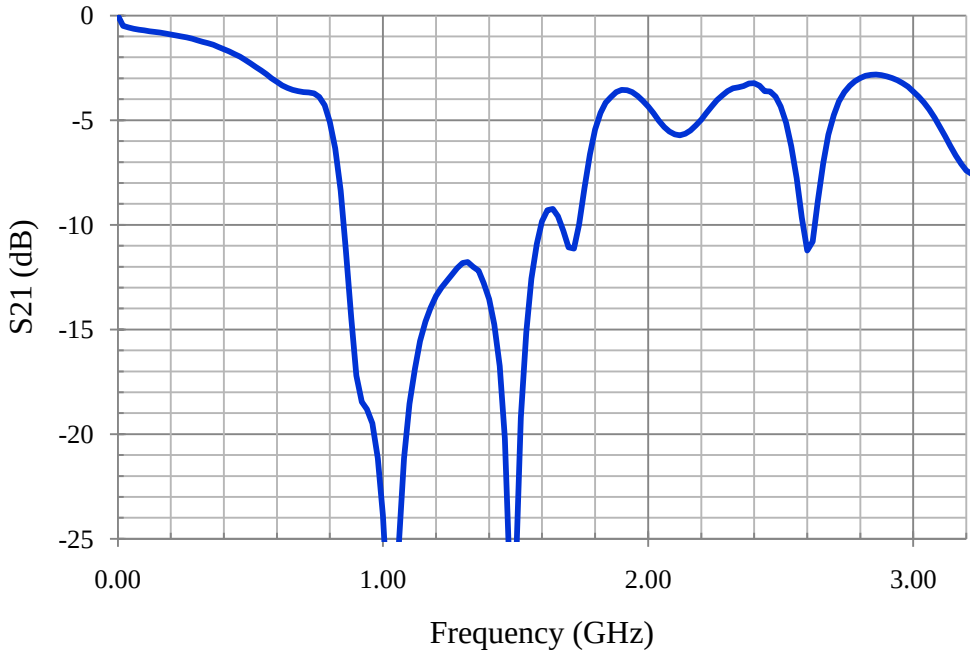

Figure 36: Band-Pass Filter S21, “0101”

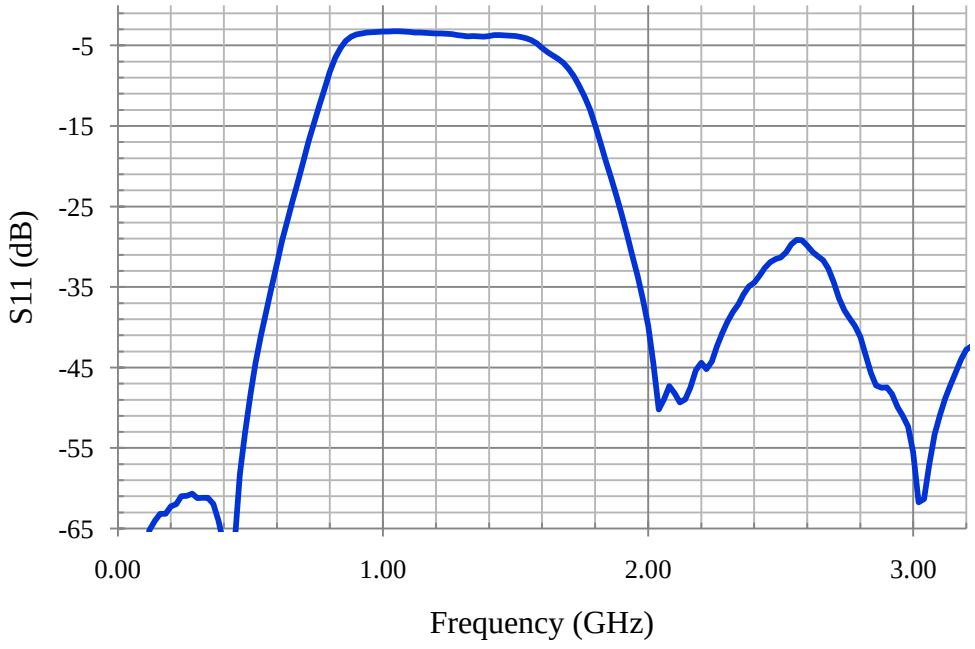

Figure 37: Band-Pass Filter S11, “0101”

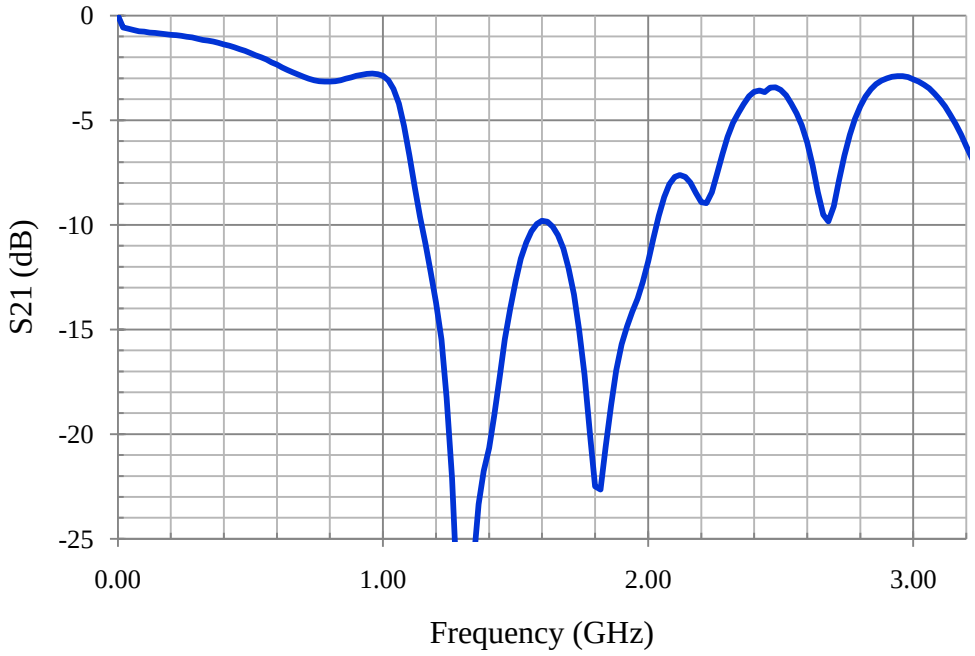

Figure 38: Band-Pass Filter S21, “0110”

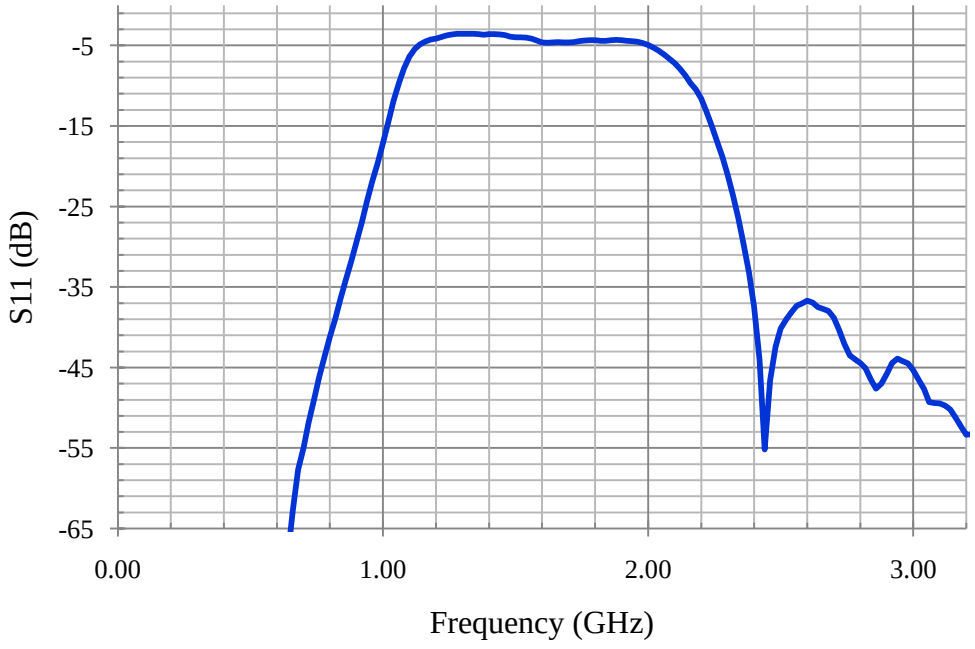

Figure 39: Band-Pass Filter S11, “0110”

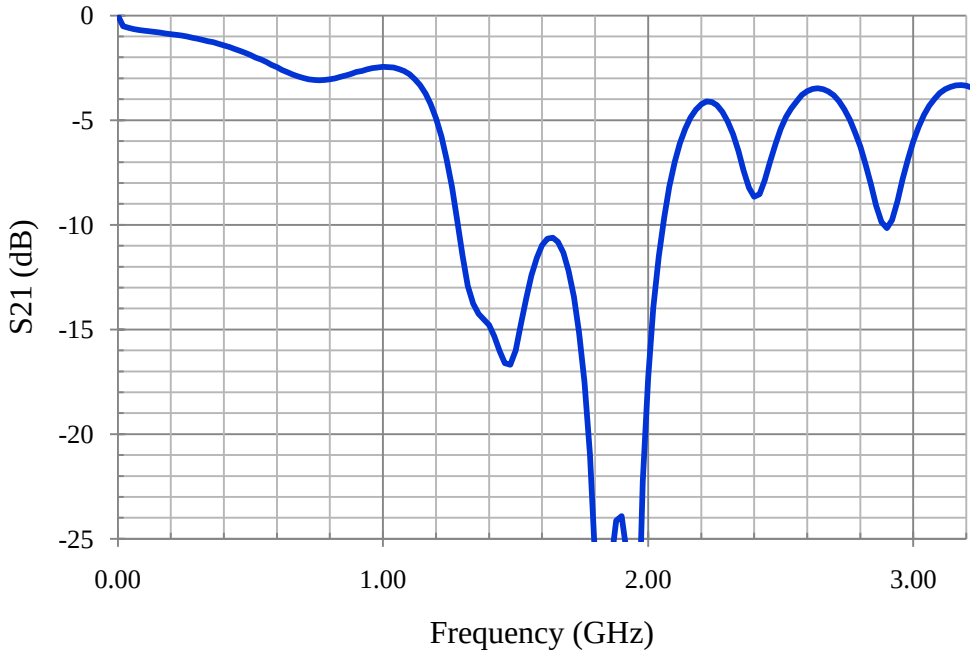

Figure 40: Band-Pass Filter S21, “0111”

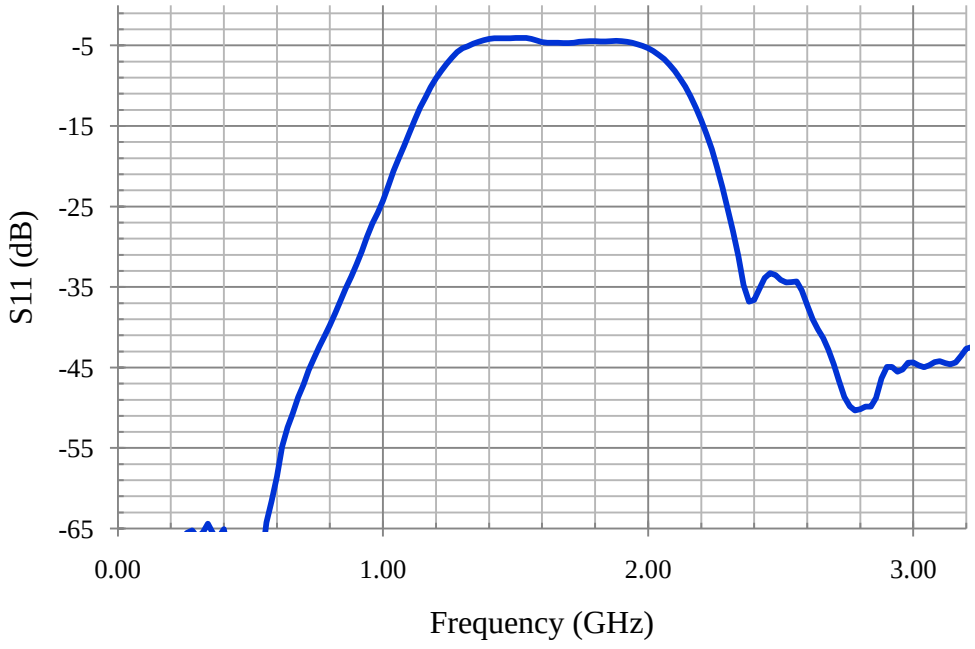

Figure 41: Band-Pass Filter S11, “0111”

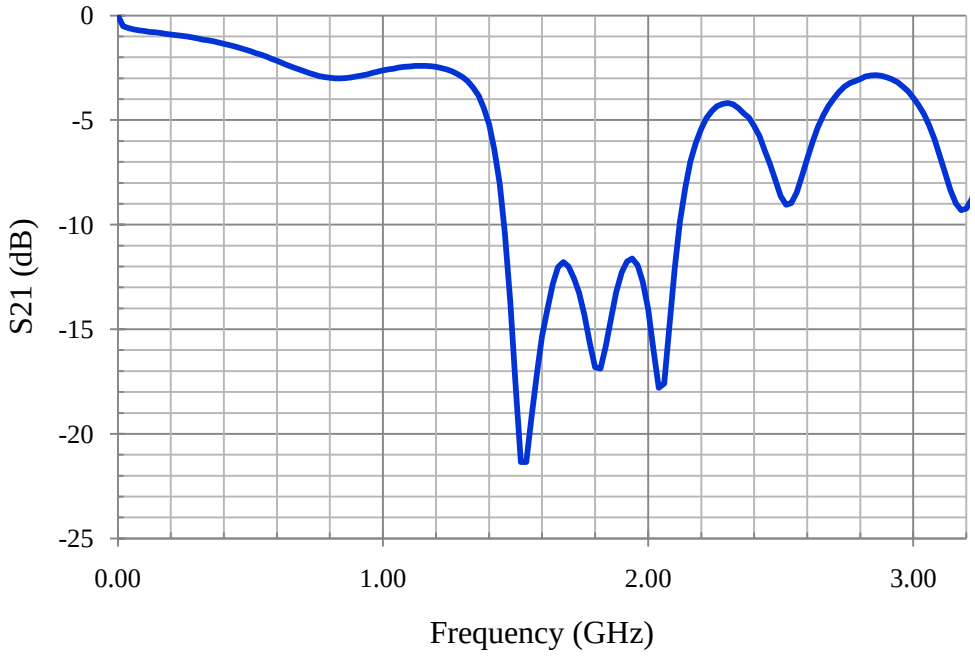

Figure 42: Band-Pass Filter S21, “1000”

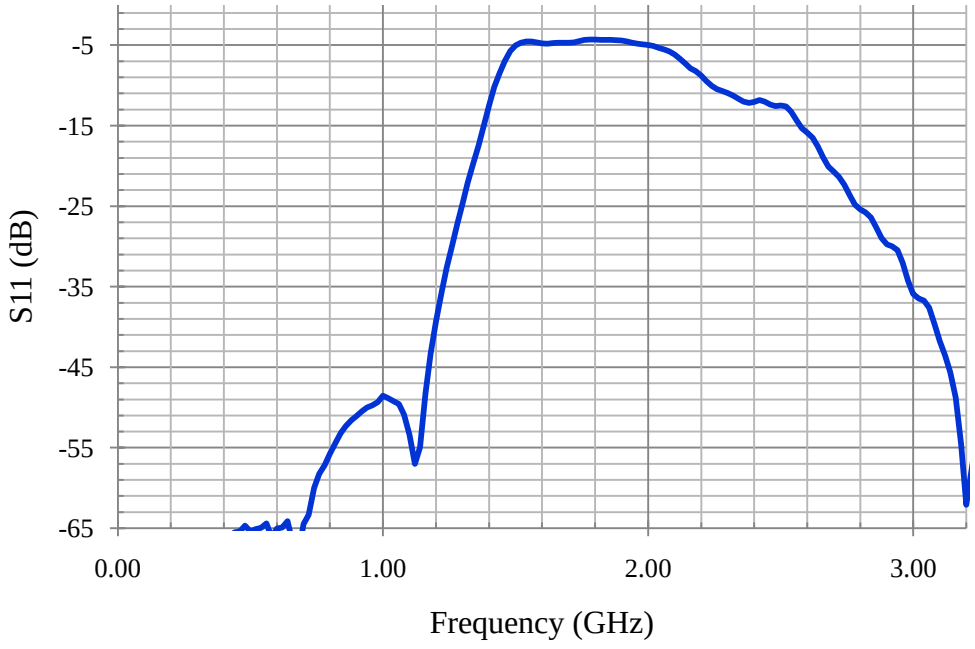

Figure 43: Band-Pass Filter S11, “1000”

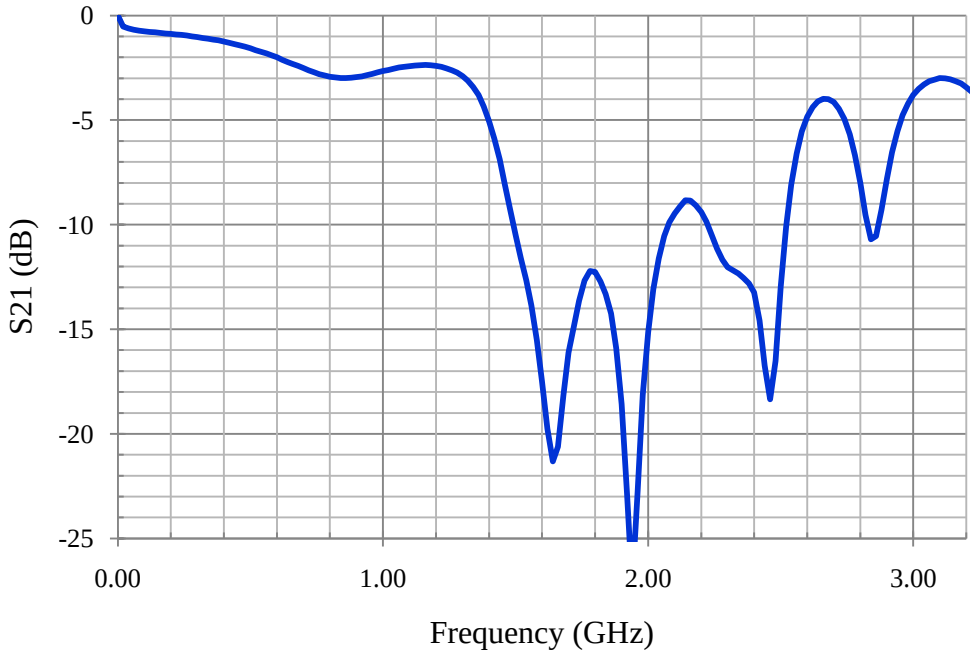

Figure 44: Band-Pass Filter S21, “1001”

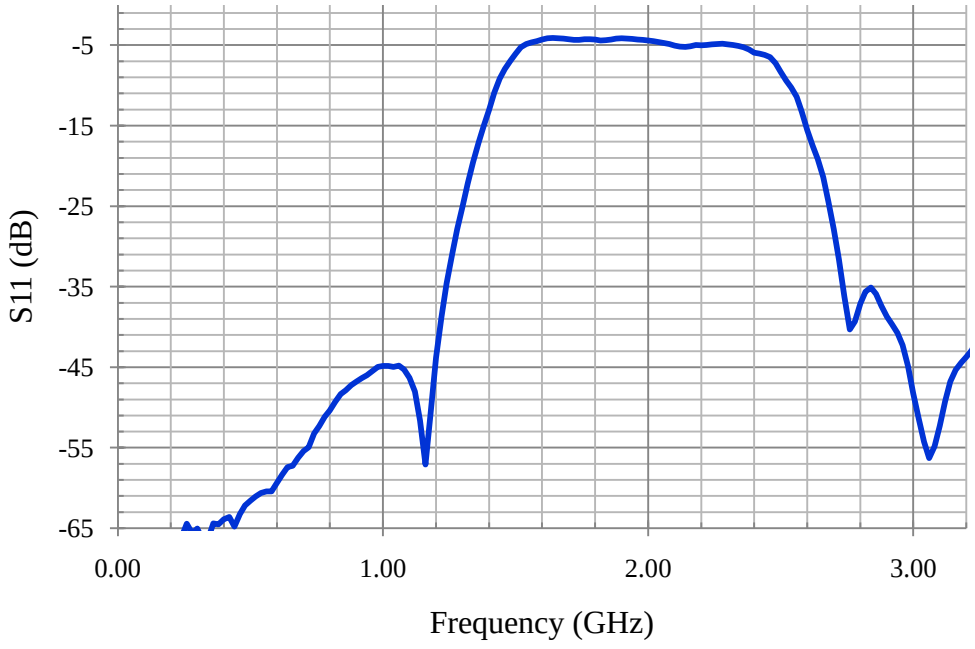

Figure 45: Band-Pass Filter S11, “1001”

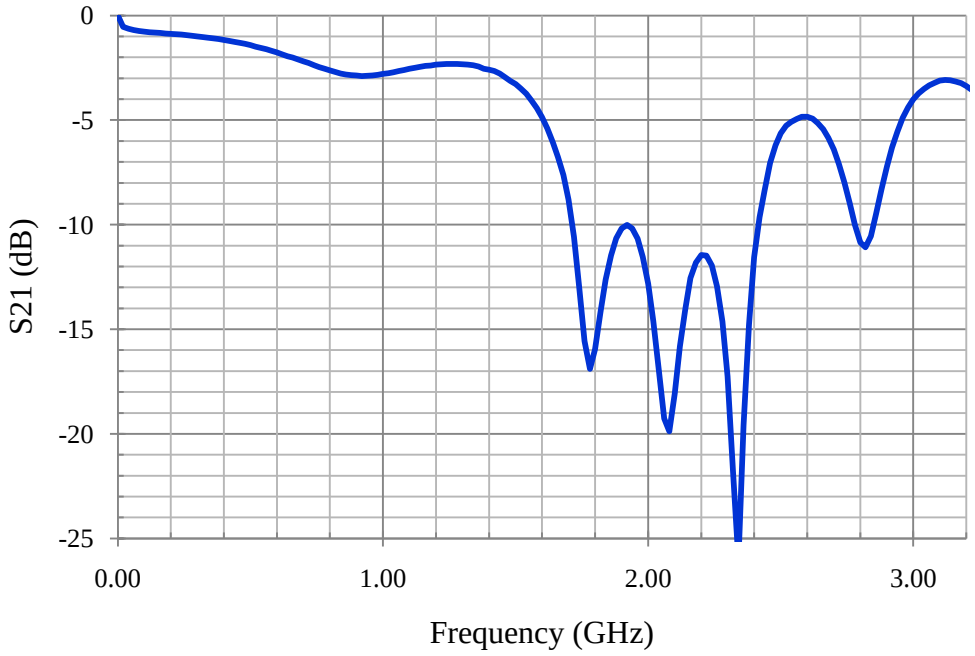

Figure 46: Band-Pass Filter S21, “1010”

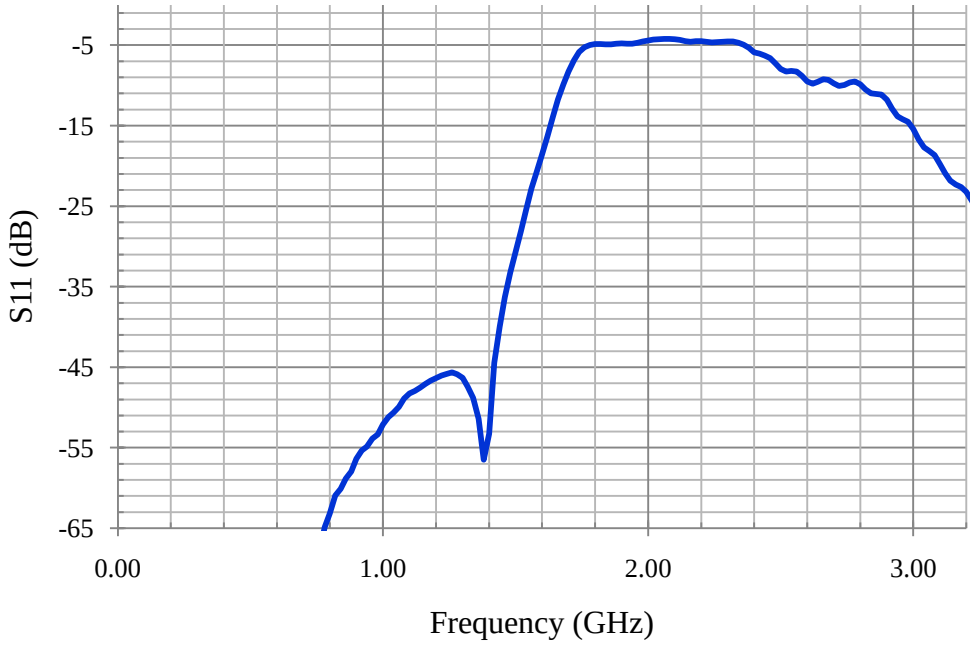

Figure 47: Band-Pass Filter S11, “1010”

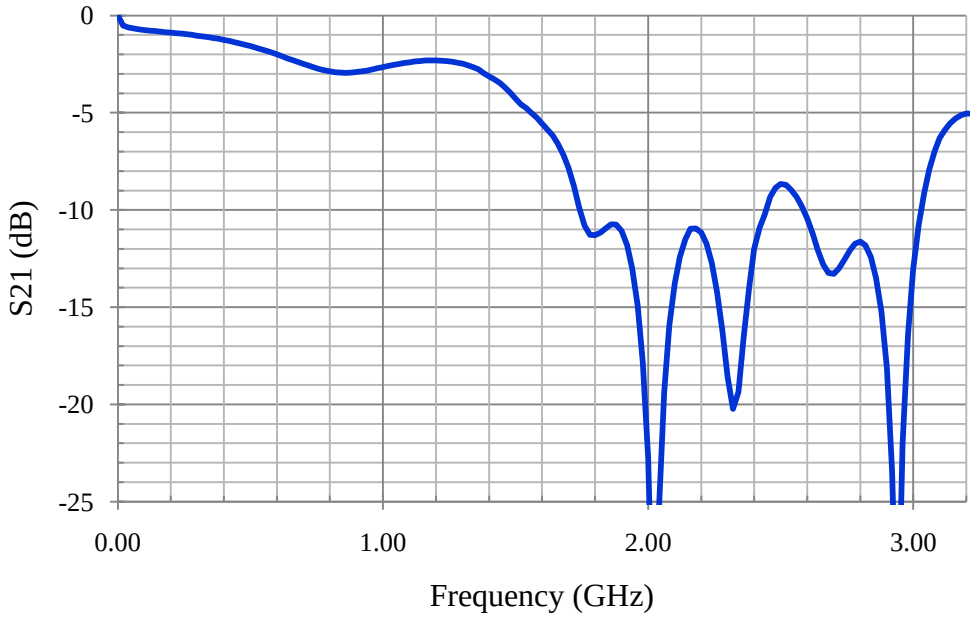

Figure 48: Band-Pass Filter S21, “1011”

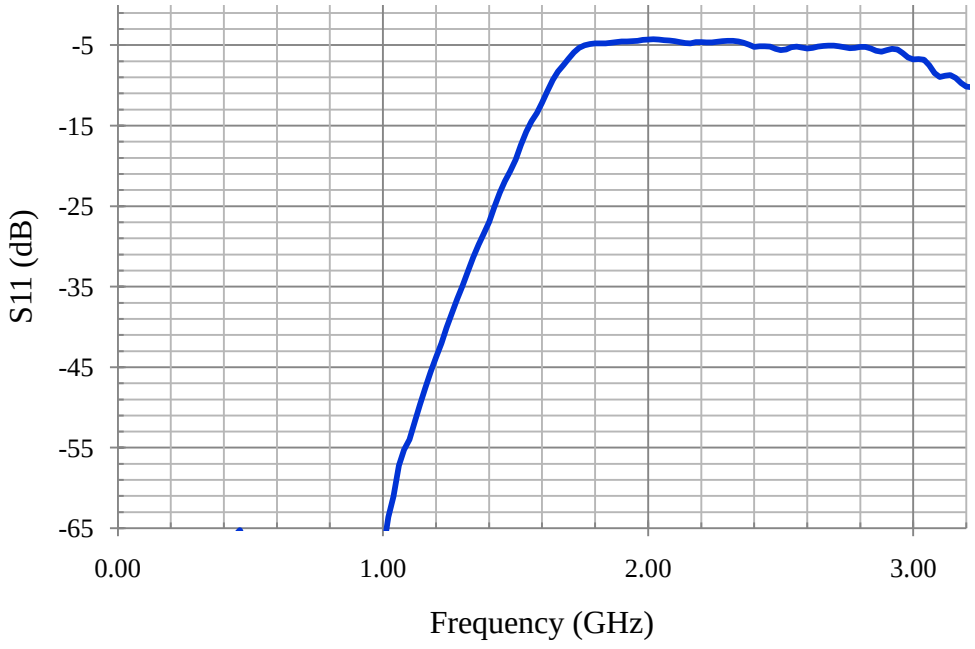

Figure 49: Band-Pass Filter S11, “1011”

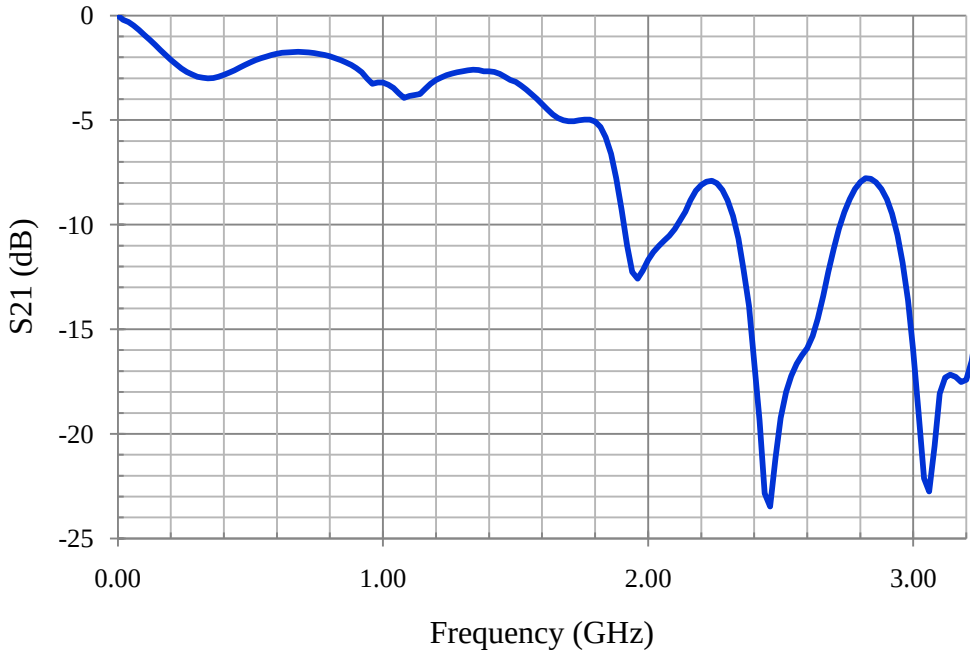

Figure 50: Band-Pass Filter S21, “1100”

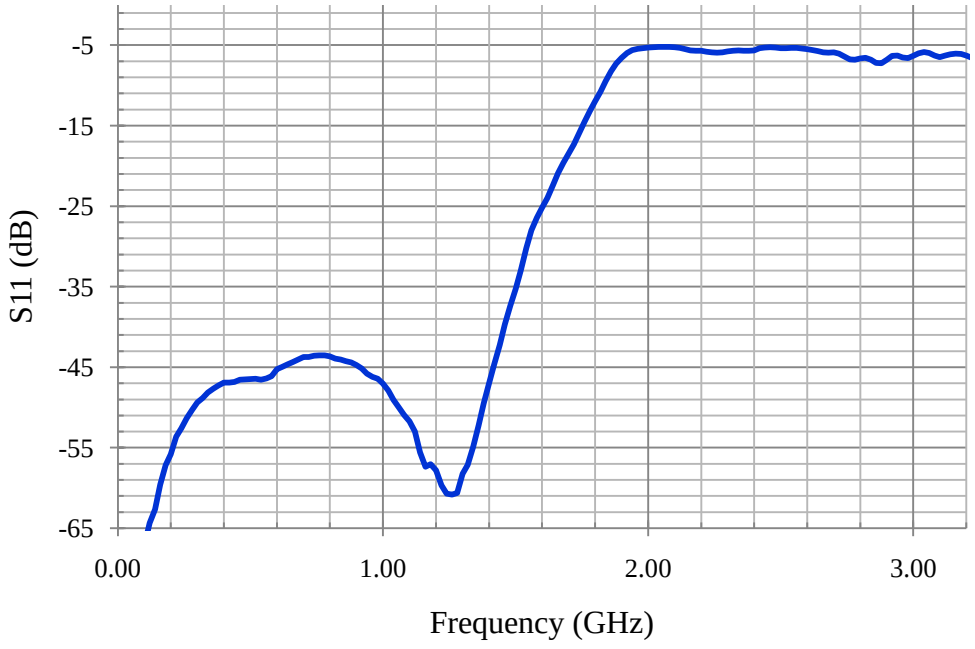

Figure 51: Band-Pass Filter S11, “1100”

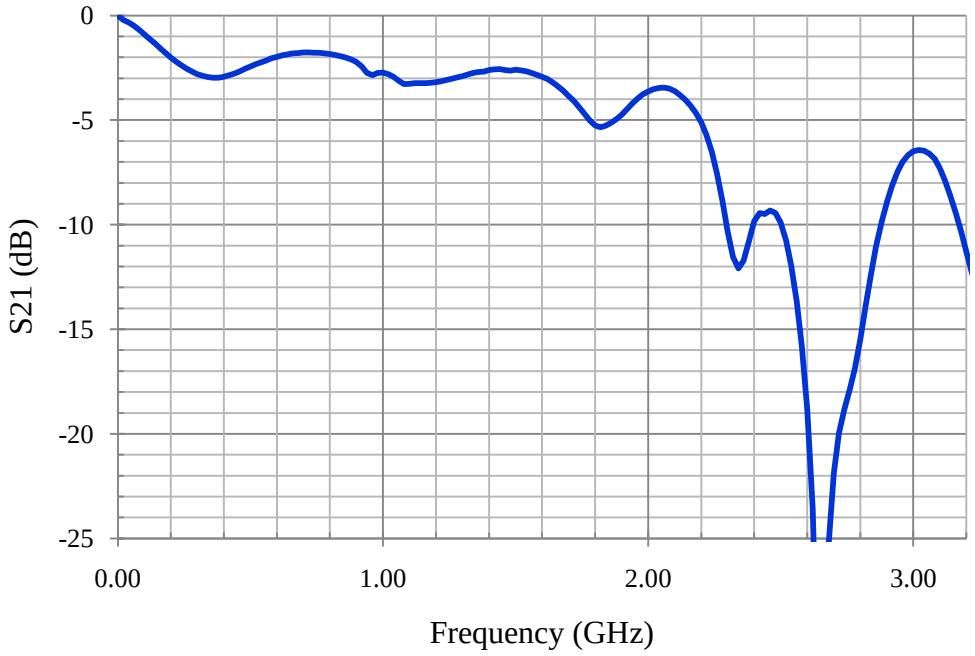

Figure 52: Band-Pass Filter S21, “1101”

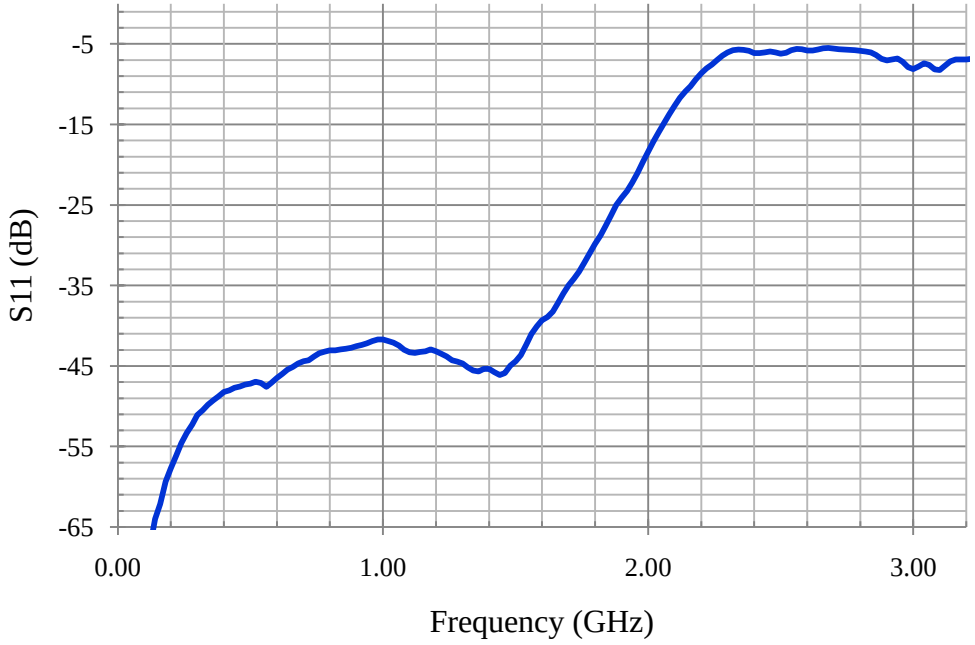

Figure 53: Band-Pass Filter S11, “1101”

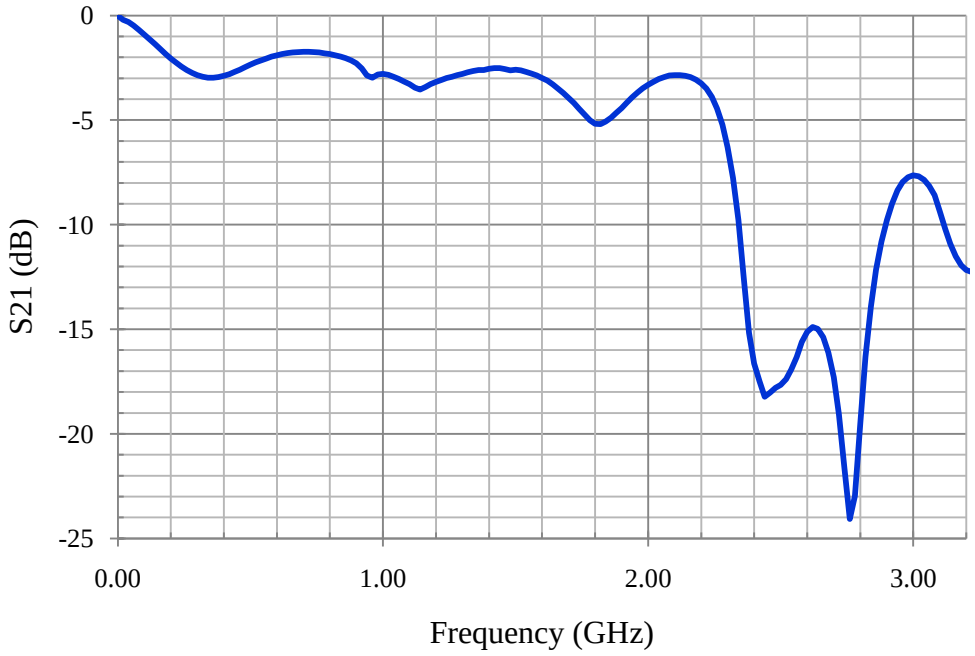

Figure 54: Band-Pass Filter S21, “1110”

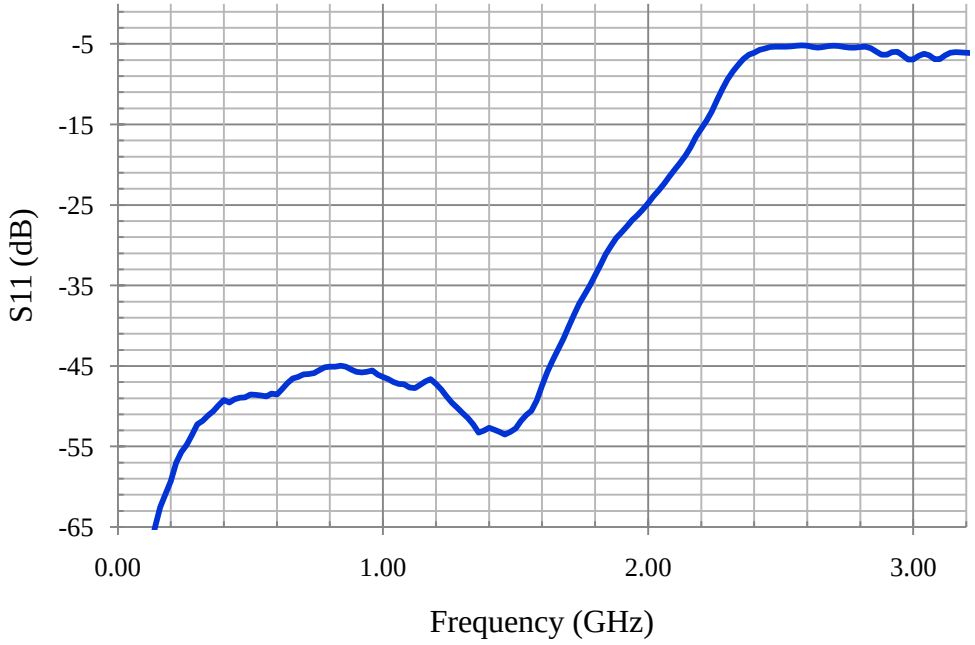

Figure 55: Band-Pass Filter S11, “1110”

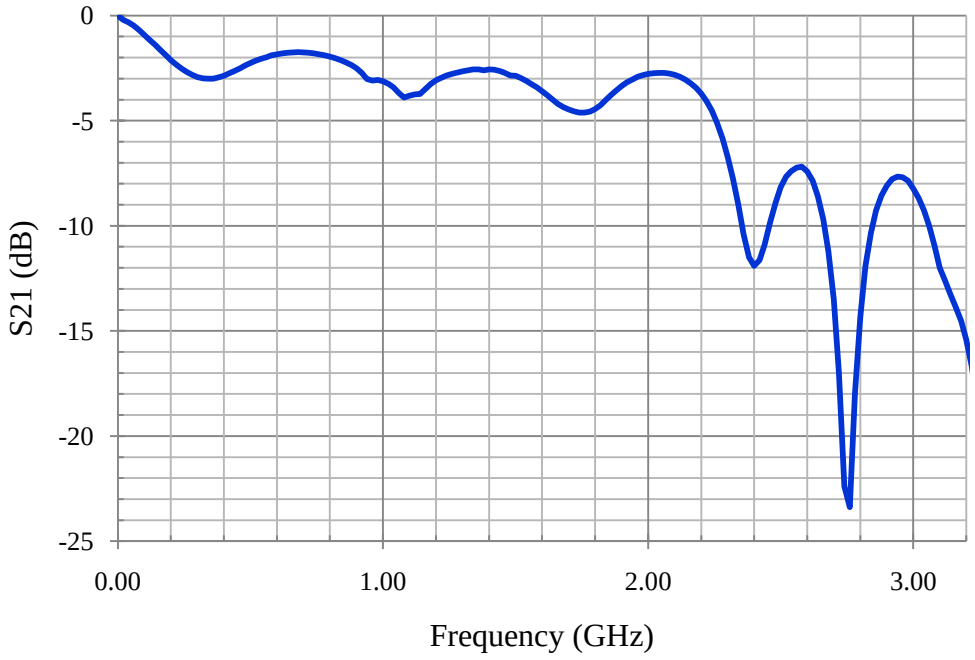

Figure 56: Band-Pass Filter S21, “1111”

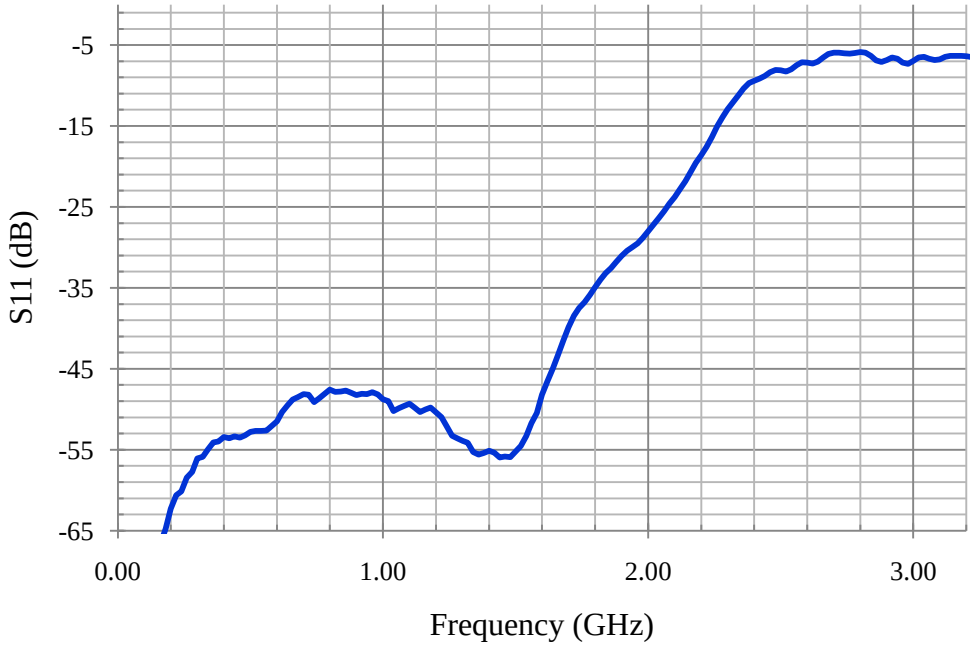

Figure 57: Band-Pass Filter S11, “1111”

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