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Analysis and Design of Multi-Port Oscillators for mm-Wave Imaging Systems

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Analysis and Design of Multi-Port Oscillators for mm-Wave Imaging Systems

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering and Computer Science

by

Saman Jafarlou

Dissertation Committee:
Professor Michael Green, Chair
Professor Nader Bagherzadeh
Professor Ender Ayanoglu

2019

DEDICATION

To my Mom and Dad ...

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ACKNOWLEDGMENTS

First, I would like to thank my academic advisor Prof. Michael Green for his incredible support and priceless comments throughout the project. He provided me with the freedom and trust I needed to pursue my research interests, and patiently shared his invaluable technical insight with me.

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A broadband low-loss 60 GHz die to rectangular waveguide transition **2015**
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IEEE Transactions on Antennas and Propagation

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ABSTRACT OF THE DISSERTATION

Analysis and Design of Multi-Port Oscillators for mm-Wave Imaging Systems

By

Saman Jafarlou

Doctor of Philosophy in Electrical Engineering and Computer Science

University of California, Irvine, 2019

Professor Michael Green, Chair

Frequency synthesizers are critical building blocks of many communication systems, including mm-wave imaging. The performance specification of frequency synthesizers, such as phase noise, quadrature phase accuracy, and frequency tuning, directly impacts the overall performance. In many practical applications the frequency synthesizer is realized as a phase-locked loop (PLL), which is a control system whose output follows the input reference signal's phase. The core block in a PLL is the voltage-controlled oscillator (VCO) whose frequency is adjustable by an input voltage. The resonator used in a VCO is generally realized as an LC tank, which can be replaced by a multi-port passive network that may lead to superior performance.

In this dissertation, a systematic method to analyze and design multi-port quadrature VCOs (QVCOs) is introduced and compared with conventional QVCOs. The method is based on multi-port oscillator theory that provides necessary and sufficient conditions for oscillation start-up, as well as finding an expression for the frequency of oscillation. Moreover, trade-offs between quadrature phase accuracy and power consumption are derived. The phase noise performance of such oscillators is studied and a technique to minimize it is proposed. As a demonstration a low phase-noise 40 GHz QVCO is designed and optimized based on this analysis and fabricated using a 65 nm CMOS process.

In the second part of this dissertation, a 55 – 67 GHz integer-N PLL is designed using a multi-mode VCO. The oscillation modes of the VCO are varied by modulating the coupling factor of a pair of coupled inductors using CMOS switches. The oscillation modes correspond to different frequency ranges, which enable wide frequency tuning with minimum impact on the other performance specifications. The PLL also includes an eight-stage of frequency divider that is carefully designed to cover the wide frequency range of the VCO output. The PLL is fabricated using 65 nm CMOS technology.

In the final chapter, the design of an oscillator based on degenerate band edge (DBE) is presented. The DBE occurs at certain infinite periodic structures that can be used in VCOs to reduce their sensitivity to the load. Multiple double-ladder networks with lumped and distributed elements to produce the DBE are studied. Moreover, active components that can be used in such oscillators including cross-coupled differential pair and tunnel diode are investigated. A design of a VCO based on a DBE structure and cross-coupled pair with transient-time simulation results is reported.

Chapter 1

Introduction

Processing massive amounts of information, from physical sensors to computers using various artificial intelligence algorithms has been a prevailing trend in today's technology. Imaging – or other types of perception – of the surrounding environment is particularly valuable in many applications. For example, collecting data from millimeter-wave radar systems stands out as a method employed for imaging – examples include visual light camera and ultrasound – because of their long range, high speed, and accuracy. However, implementation of such mm-wave imaging systems is challenging.

Millimeter-wave imaging systems of various complexity have been investigated for applications such as concealed weapon detection [1], gesture recognition [2] and automotive radars [3].

1.1 mm-wave Imaging Systems

A conventional and rigorous method of mm-wave 3D imaging is explained in [1] although novel methods have recently been proposed to construct the image with fewer measurements

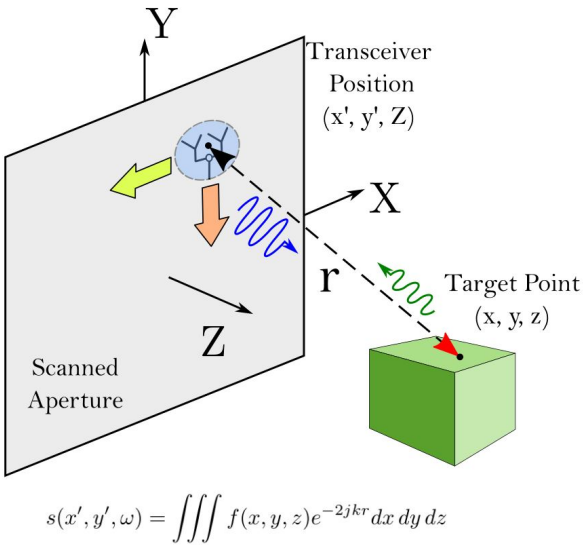


Figure 1.1: Typical configuration for a mm-wave 3D imaging system

[4]. Fig. 1.1 shows a typical 3D imaging system, which consists of a transmitter/receiver unit located at (x', y', Z) moving along the scanned aperture in the $Z = 0$ plane. For each measurement point on the scanned aperture, the transmitter sends the signal towards the object that is reflected from different points on the object at coordinate (x, y, z). The geometry of the object is determined by the reflection function $f(x, y, z)$ defined as the ratio of the reflected signal to the incident signal at that point. The sum of all reflected waves is received at the receiver, which is located at the same location as the transmitter. Therefore, the received signal, s, can be expressed as:

$$s(x', y', \omega) = \iiint f(x, y, z) e^{-2jr(2\pi f_o/c)} dx\, dy\, dz \tag{1.1}$$

where the exponential term indicates the phase changes due to the free space propagation of the wave; c is the speed of light; and f_o is the carrier frequency of the system. As explained in [1], $f(x, y, z)$ can be calculated based on inverse Fourier analysis. Since the critical information is in the phase of the signal, using a signal with low phase noise is a key factor in obtaining a clear image. Moreover, as described in [1], the range of the frequency sweeping determines the resolution and maximum dimension of the image along the Z-axis.

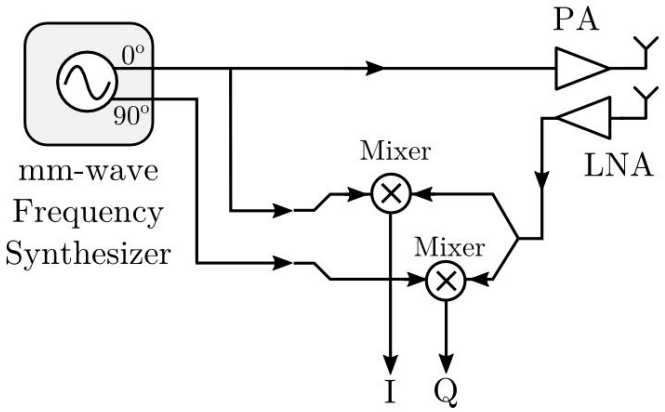


Figure 1.2: mm-wave transceiver for imaging

Fig. 1.2 shows the mm-wave transceiver architecture, used in many 3D imaging systems, composed of a quadrature frequency synthesizer that transmits a single-tone signal through a power amplifier. The received signal is applied to a low-noise amplifier and mixes with the quadrature components of the transmitted tone leading to in-phase (I) and quadrature (Q) components. It is these components that are used to calculate the complex value of s for each measurement.

As evident from Fig. 1.2 the frequency synthesizer plays a pivotal role in the accuracy of the I/Q output and eventually the quality of the image. For example, errors in quadrature phases and the phase noise of the synthesizer will lead to systematic and random error, respectively, in phase detection.

1.2 Frequency Synthesizer

Frequency synthesizers are widely used in both wireless and wireline telecommunication systems. In high-frequency integrated circuits a frequency synthesizer is implemented as a phase-locked loop (PLL), which consists of a negative feedback closed-loop system that controls the phase of the signal generated by an oscillator. Therefore, the output of a PLL

is a periodic waveform with relatively stable phase which is essential for many applications.

A PLL compares the phase and frequency of the output signal with an external reference signal. The reference signal is generally produced by a high quality factor resonance tank such as a crystal oscillator. For many applications the most common type of PLL is the integer PLL that allows the synthesis of a higher frequency signal using a lower frequency reference signal. Therefore, the output frequency is given by:

$$f_{out} = N f_{ref} \tag{1.2}$$

where N is the division factor. For many communication application N must be adjustable to allow the switching between the channels. For wireless communication systems, the PLL output is usually used as a carrier signal that up/down-converts the transmitted data. To serve this purpose PLLs have demanding performance specification that may include: wide tuning range, low phase noise, freedom from spurs, and I/Q phase matching.

Fig. 1.3 shows a simplified block diagram of a typical PLL. Its core is a voltage-controlled oscillator (VCO) whose output frequency is proportional to its input control voltage. The VCO output is fed back to a chain of frequency dividers whose output is compared with an external reference signal using a phase-frequency detector (PFD) whose output is a voltage proportional to the input phase difference. This signal is integrated by a charge pump and low-pass filter and then applied to the control input of the VCO.

Although a PLL improves the VCO phase noise and locks the frequency compared to a free-running oscillator, the VCO still often dominates the overall performance of the PLL. There are some fundamental trade-offs in designing frequency synthesizers subject to specifications such as frequency tuning range, phase noise, and power consumption that limit the performance.

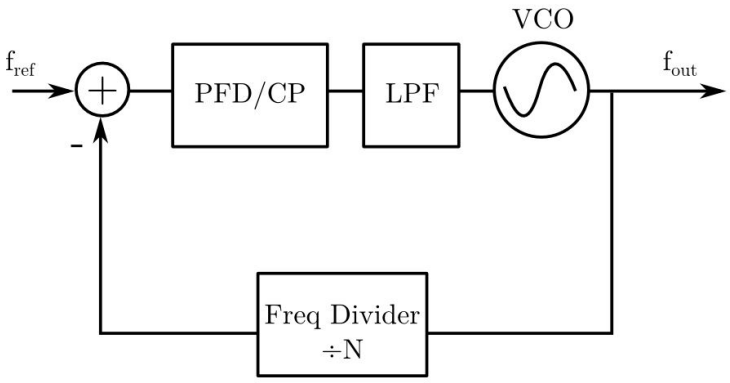


Figure 1.3: (a) Typical PLL configuration

1.2.1 Conventional mm-wave VCOs

The most popular method to design a mm-wave oscillator is to connect a cross-coupled pair transistor in parallel with to an LC resonance tank as shown in Fig. 1.4(a). The circuit is biased by a tail current source I_s. Multiple tuning mechanisms in the resonance tank are employed to sweep the output frequency such as capacitance and inductor switching for discrete tuning and using varactor for continuous tuning. The choices of tail current and impedance of the resonance tank play a key role in operation of VCOs. Fig. 1.4(b) shows the oscillation amplitude grows as the bias current increases (current limit region) until the current source either enters the triode region or the voltage swing reaches V_{DD} [5]. A commonly used figure of merit (FOM) applied to VCOs that is defined in literature [6] is given by:

$$FOM = \frac{(\frac{\omega_c}{\Delta\omega})^2}{\mathcal{L}(\Delta\omega)P_{DC}} \tag{1.3}$$

where the $\mathcal{L}(\Delta\omega)$ is the phase noise at the frequency offset of $\Delta\omega$, P_{DC} is the DC power dissipation in mW and ω_c the oscillation frequency. For an LC VCO this can be simplified

to [7]:

$$FOM = \frac{V_{osc}^2}{2R_p P_{DC}} \frac{2Q^2}{KTF} 10^{-3} \tag{1.4}$$

where V_{osc} is the voltage amplitude at the tank, Q is the quality factor of the tank, R_p is the equivalent parallel resistance of the tank, K is the Boltzman constant, T is the temperature, and F is the noise factor dictated by the VCO topology.

It is shown in Fig. 1.4(b) that the FOM increases with the tail current. At a certain value of I_s the amplitude reaches a maximum due to . Beyond this point increasing I_s increases consumption without increasing the voltage swing, which decreases the FOM. To maintain the voltage swing at a sufficiently high level either I_s or L must be kept high. The former leads to high dc power dissipation and therefore low efficiency; the latter results in small tank capacitor for a given oscillation frequency that limits the tuning range [8, 9]. To resolve these fundamental trade-offs, numerous works where novel design techniques are employed have been presented. One technique to boost the tuning range of a VCO with minimum impact on other performance parameters is to change the inductor along with capacitor of the tank, as explained in the following section.

The conventional way to change the VCO frequency is to employ a bank of switched capacitors for coarse switching and a varactor for fine and continuous tuning. For wide frequency tuning range, this technique leads to non-optimal operation of the oscillator. To achieve the maximum frequency tuning range, more capacitance must be included in the tank. Therefore, considering the fixed parasitic capacitor of FETs, in order to achieve a certain resonance frequency the tank inductor must be decreased, which leads to lower tank

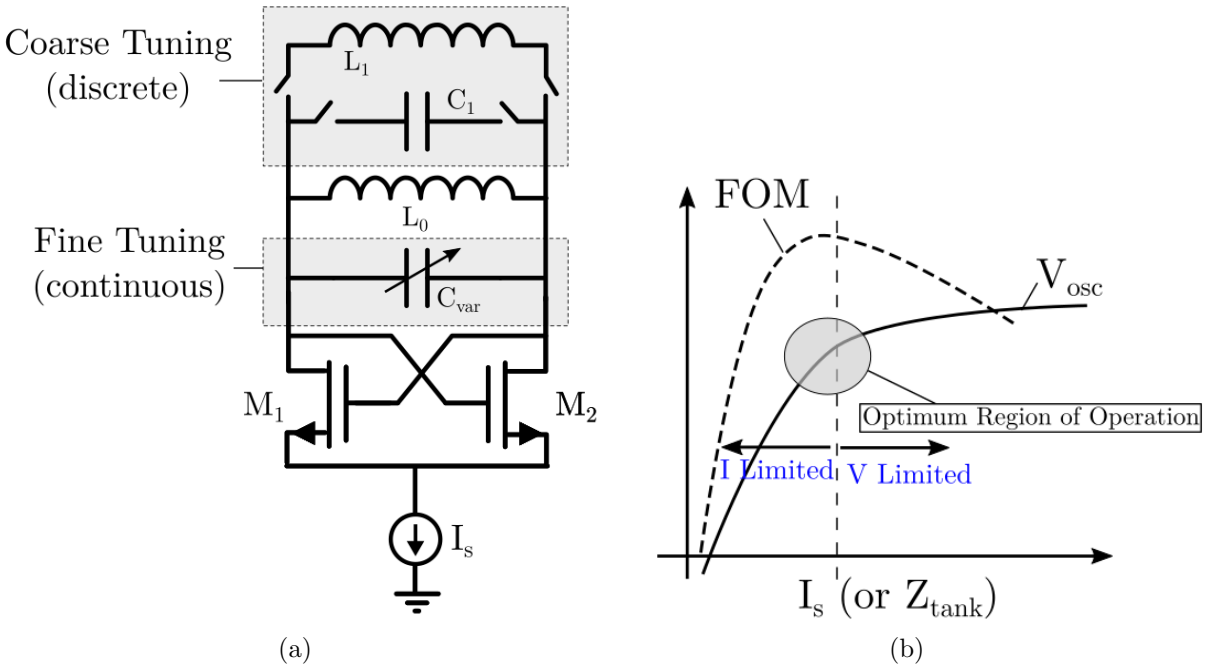


Figure 1.4: (a) Block diagram of a typical LC VCO with switchable capacitor and inductors, (b) Figure of Merit of a VCO versus tail current

impedance, $R_p = Q\omega L$. To achieve rail-to-rail voltage swing (optimized region of operation) for low impedance tank more current must be burned that results in less efficient oscillation.

Now let us assume that the tank inductor is not fixed and can be partially switched. In that case the inductor-to-capacitor ratio can be almost constant throughout the frequency range allowing for more optimum operation.

Moreover, achieving a wide contiguous frequency range is particularly difficult as the quality factor of varactors drops significantly at high frequencies.

1.3 Capacitive Versus Inductive Tuning

Although some distributed structures that realize high-Q resonances at mm-wave frequencies have been reported [10], most oscillators utilize a conventional LC tank to achieve resonance.

An LC tank can be realized as either a series or parallel connection of an inductor and capacitors. The quality factor of each of these elements, defined as the ratio of the imaginary part to the real part of its impedance, is the critical parameter that determines the phase noise of the VCO. Moreover conduction loss leading to finite quality factor, distributed implementation, and interconnect parasitics determines the element's self-resonance frequency (SRF).

An on-chip inductor can be implemented as either a planar winding or a transmission line using the thickest metal layer of the CMOS process to reduce the conduction loss. Fig. 1.5 (a) shows a typical square winding inductor with 8μm line width, 5μm spacing and sheet resistance of $R_s = 0.14\,\Omega/\square$; d_i and d_o represent inner and outer diameters respectively, and N is the number of turns. Fig. 1.5 (b) shows the contour plot of the quality factor values with respect to inductance and frequency calculated through full-wave EM simulations by HFSS. To obtain different inductor values, d_o is swept while the ratio d_o/d_i is kept between 0.4 and 0.7 for each number of turns (except for $N = 1$). It must be noted that the quality factor becomes negative at frequencies higher than the SLF; thus the white area corresponds to a region where the inductors are not usable. The value of the quality factor for each inductor has a peak at a frequency slightly lower than its SRF, which generally is the ideal band of operation. As the SRF moves to higher frequencies for single-turn inductors, the quality factor can attain a value higher than 20.

Capacitors in CMOS technologies can be realized as a metal-oxide-metal (MOM) structure, a metal-insulator-metal (MIM), or the gate-to-bulk capacitance of a MOSFET. MIM and MOM capacitors are not variable although their quality factors are generally quite high. On the other hand, a variable capacitor (varactor) can be realized by exploiting the fact that the gate-source and gate-drain capacitance with respect to gate bias voltage in a MOSFET biased in its accumulation region. Fig. 1.5 (c) shows the top view of a typical varactor with $N = 4$ fingers. To minimize the loss, particularly at high frequencies, using the maximum

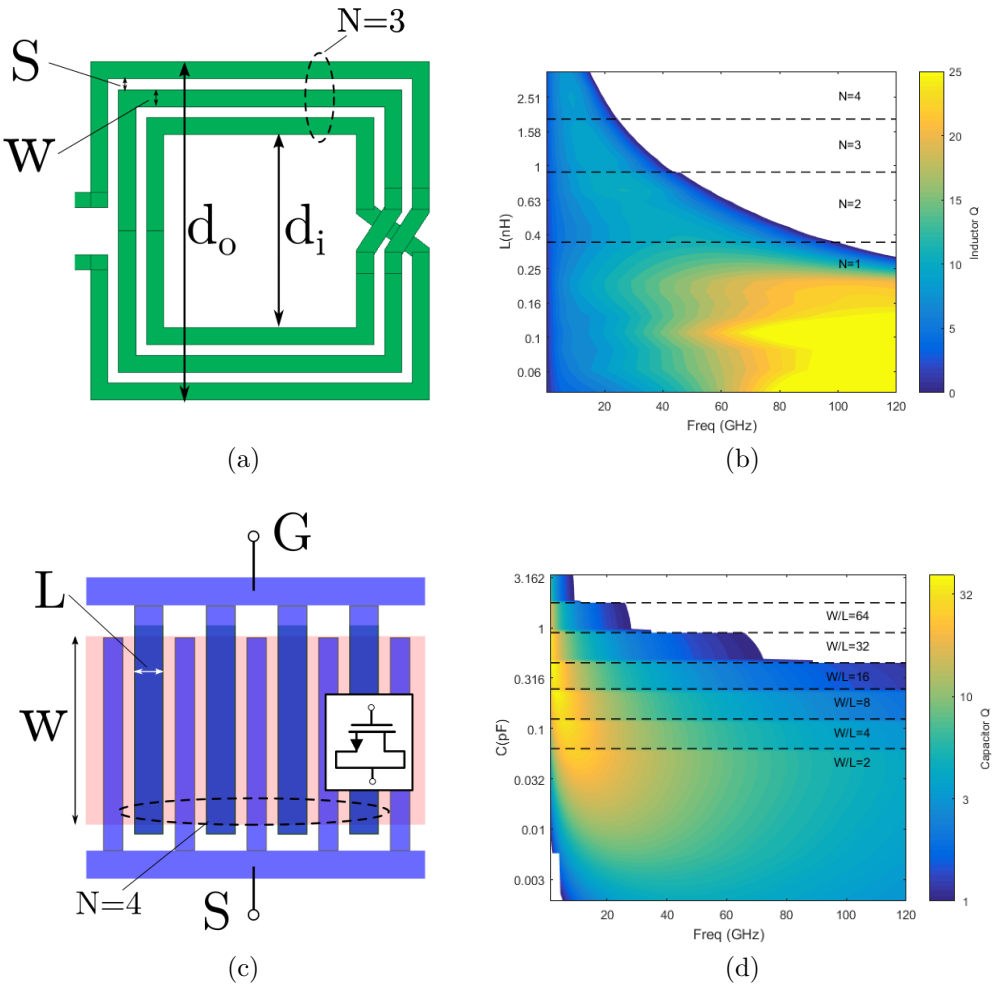


Figure 1.5: (a) top view of 3 turn inductor (N=3) with linewidth of W and spacing of S, (b) quality factor versus frequency and inductor values (log scale) (c) Top view of a typical 4-finger varactor with ratio of W/L (d) quality factor of varactor for $V_{GS} = 0$ versus frequency.

allowable number of fingers and the minimum allowable W/L ratio, determined by the PDK, is favorable. Moreover, minimum-length devices are usually chosen to decrease the channel resistance, although this may lead to a lower tuning range (C_{max}/C_{min}). The capacitance is a function of V_{GS} which can be biased between -V_{DD} and +V_{DD}. Fig. 1.5 (d) illustrates the quality factors for different capacitor values for $V_{GS} = 0$, with minimum length ($L = 200$ nm), and values of W/L ranging from 2 to 64. The number of fingers (N) is set to 64 except for very small capacitors in the $W/L = 2$ case. Similar to Fig. 1.5 (b) the blank area at the top right corner of the graph corresponds to frequencies above the SRF of the capacitor. The

maximum Q of a capacitor generally occurs at lower frequencies than that of an inductor, except for very small capacitors (below 60 fF), for which fewer number of fingers leads to more relative loss. Moreover, increasing the bias voltage from 0V degrades the quality factor, due to the large number of low-mobility charges in the channel.

The overall quality factor of a resonant tank is given by:

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_C}. \tag{1.5}$$

This is illustrated by contour plots in Fig. 1.6. Blank areas represent the values for which the quality factor becomes negative. These plots show that shows for a given desired resonant frequency, the values of L and C can be chosen in order to achieve a desired Q_T. For example, for an oscillator operating at 50 GHz the optimum L and C are 250 pH and 40 fF, respectively, providing a total quality factor of approximately 6. By referring to Fig. 1.5, the quality factors of the inductor and capacitor at 50 GHz are 17 and 10, respectively. It is true in general that for high-frequency tanks the Q_T is mostly dominated by varactor loss [11] and slight degradation of inductor quality factor will have an insignificant impact on the total quality factor. Therefore, the inductor quality factor can be used to trade off with either the tunability or the silicon area in such oscillators. For instance, the inductor used in a tank can be varied by MOSFET switches while imposing minimal Q degradation to the overall resonant tank.

Oscillation frequency tuning can be achieved by changing the capacitor or inductor value; i.e.,

$$\frac{\Delta\omega}{\omega} = -\frac{1}{2}(\frac{\Delta C}{C} + \frac{\Delta L}{L}) \tag{1.6}$$

In conventional VCOs, the inductor remains fixed and the capacitance is only changed by

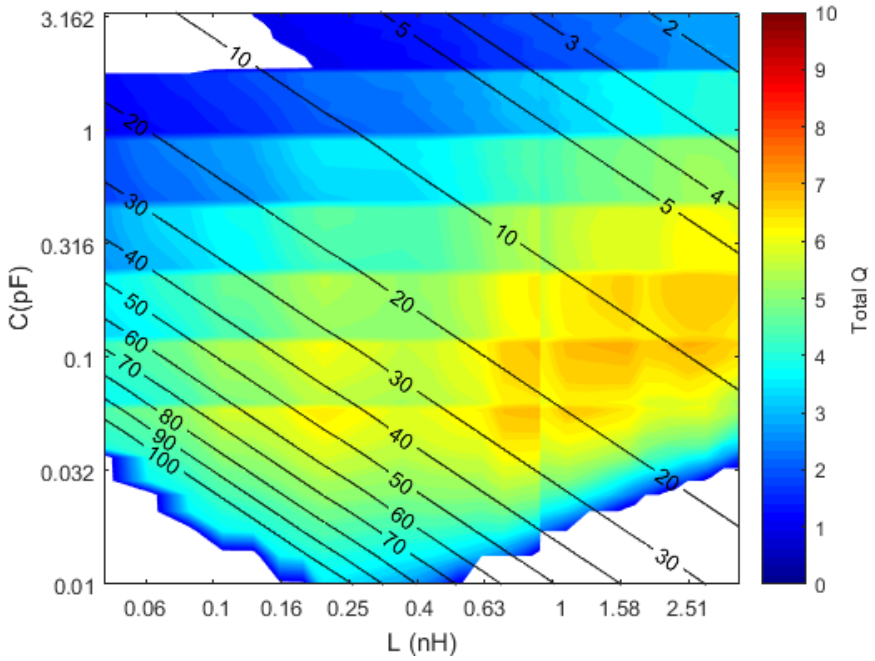


Figure 1.6: Resonant frequency (contour lines) in GHz and total quality factor of the LC tank at the resonance frequency with respect to inductor and capacitor in logarithmic scale. Blank area corresponds to regions that resonance frequency exceeds the self resonance frequency of inductor.

adjusting its bias voltage. There are some recent works that have reported the use of inductor switching along with capacitor sweeping for mm-wave range VCOs [12]. In the next chapter a VCO design is proposed where the effective inductance of the tank is switched, which leads to change in both the oscillation mode and frequency.

1.4 Summary

This thesis focuses on the improvement of the mm-wave oscillator designs by taking a multiport analysis approach that helps to alleviate some of these trade-offs. The next chapter is focused on the analysis and design, based on multiport oscillator theory, of resonance-coupled quadrature VCOs. In Chapter 3, the design of a PLL with wide tuning range that employs a multimode VCO based on inductor switching is described. In Chapter 4, an oscillator design

based on degenerate band edge (DBE) phenomenon is presented.

Chapter 2

Design and Analysis of QVCO Based on Multi-Port Oscillation Theory

2.1 Introduction

This paper presents a systematic approach to analyze and design multi-port oscillators. The proposed method is first used to analyze a conventional QVCO, which is based on two LC VCOs coupled together through 2 pairs of coupling transistors. It is shown that this mechanism results in a phase error depends on the mismatch of coupling transistors. Moreover, this method is employed to analyze a new class of QVCOs in which the coupling is realized by a passive resonant network. The possible passive and active networks that can be utilized in such QVCOs are presented, and the resonant frequency and oscillation condition for those QVCOs are derived. It is shown that the phase error for these QVCOs mainly depends on passive mismatch. A technique is presented to reduce the phase noise of the QVCOs based on an implicit common-mode resonance method. Furthermore, two designs based on magnetically and capacitively resonant-coupled QVCOs are studied and

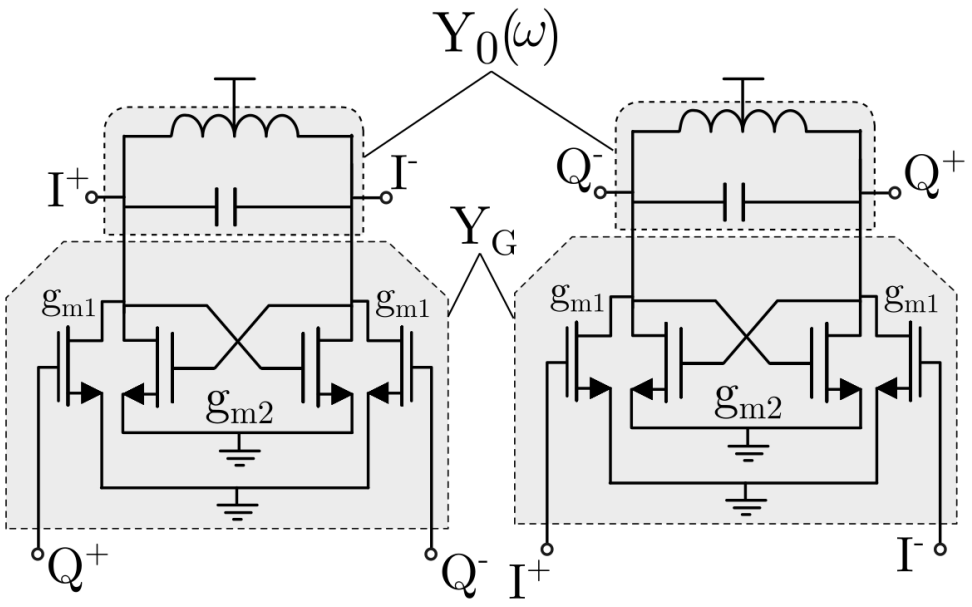
their performances are compared using this method.

2.2 Background

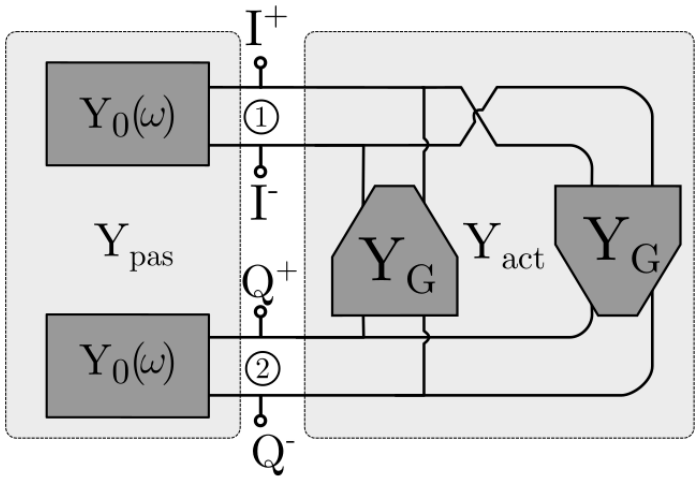
CMOS millimeter-wave transceivers have become a reliable solution to the growing demand for higher data rates and high-accuracy radar. The design of a signal synthesizer block, which is one of the critical parts of such systems, has been a topic of extensive research. In particular, generation of a quadratic signal enables direct conversion architectures with fewer complications and lower power consumption. In general, design of a quadrature VCO with low phase noise, wide tuning range, and minimum phase error is a major design challenge.

A popular method to implement quadratic voltage-controlled oscillators (QVCOs) is to simply couple two separate LC VCOs through an additional four transistors [13], shown in Fig. 2.1(a). This configuration can be generalized by the block diagram of Fig. 2.1(b), which consists of two pairs of active blocks, Y_G, corresponding to the transistors, and two pairs of passive blocks $Y_0(\omega)$, representing the LC tanks.

Convectional QVCOs, despite their widespread popularity, suffer from some drawbacks such as the high power consumption requirement to overcome phase noise and phase error trade-off, particularly at mm-wave frequencies [14]. To alleviate these drawbacks, resonant-coupled QVCOs can be used. As shown in Fig. 2.2(a), such structures are composed of two identical passive 2-port networks, $Y_0(\omega)$, and two identical 2-port active components, Y_G, forming a loop. Y_G is often implemented in one of three ways illustrated in Fig. 2.2(b) or any parallel combination of them. $Y_0(\omega)$ can also be implemented in many ways, such as a magnetically coupled resonance tank [15–18] or a capacitively coupled tank [19]. It should be noted that the wire-crossing incorporated in the loop plays a critical role in generation of quadrature oscillation. Furthermore, conventional QVCOs generally consume higher DC



(a)



(b)

Figure 2.1: (a) Schematics of a conventional QVCO, (b) block diagram of QVCOs where passive and active parts are separated

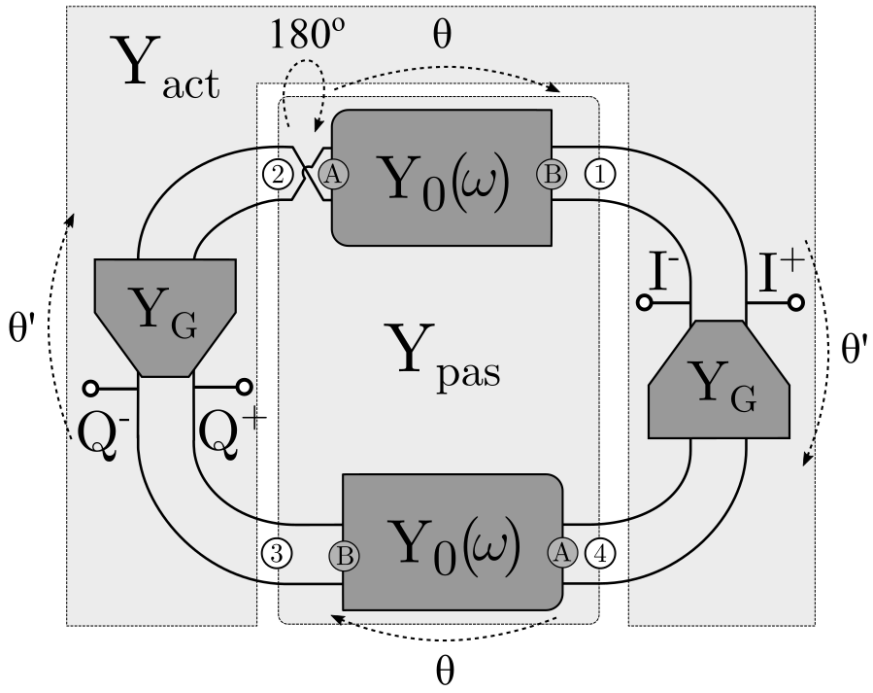


Figure 2.2: (a) Block diagram of resonant-coupled QVCOs in loop configuration with phase shifts due to passive 2-port networks, θ, and active components, θ'. In quadrature operation $\theta + \theta' = 2k\pi \pm 90°$. (b) active components (Y_G) can be realized in three ways in CMOS process: gm-cell, Cross-coupled and negative resistance.

power as they use a transistor pair for coupling whereas in resonant-coupled QVCOs, the coupling is realized by a passive network.

In this chapter the operation principle of various QVCOs is studied by taking a systematic approach based on the general theory of multi-port oscillators, explained in Section 2.3. Furthermore, closed-form expressions for the oscillation frequency, oscillation start-up condition, and phase errors are derived in Section 2.4. The proposed analysis method leads to necessary and sufficient conditions for quadratic oscillation of any QVCO so that designers can leverage the existing degrees of freedom to optimize design specifications such as output power and phase noise. In Section 2.5 some techniques to improve phase noise of QVCOs are discussed. Section 2.6 presents application of this analysis method on different QVCO topologies along with a proposed QVCO design with enhanced performance. A QVCO with novel coupling network is proposed in Section 2.8. Conclusions are given in the final Section.

2.3 Analysis of Multi-Port Oscillators

In [20], [10], [21], an analysis method is described for oscillators with N identical one-port active components (negative resistance), connected to an N-port passive resonance network. This method can be generalized to oscillators using N identical M-port active components connected to an MN-port passive network. Fig. 2.3 shows a general block diagram of such an oscillator for which $M = 2$, and Y_{act} encompasses all of the active components. To find the conditions for which the circuit is marginally stable – i.e., for which the circuit is on the threshold of oscillation – we solve the following equation:

$$\det(\mathbf{Y}_{\mathrm{tot}}(\mathrm{j}\omega_{\mathrm{o}})) = \det(\mathbf{Y}_{\mathrm{pas}}(\mathrm{j}\omega_{\mathrm{o}}) + \mathbf{Y}_{\mathrm{act}}) = 0 \tag{2.1}$$

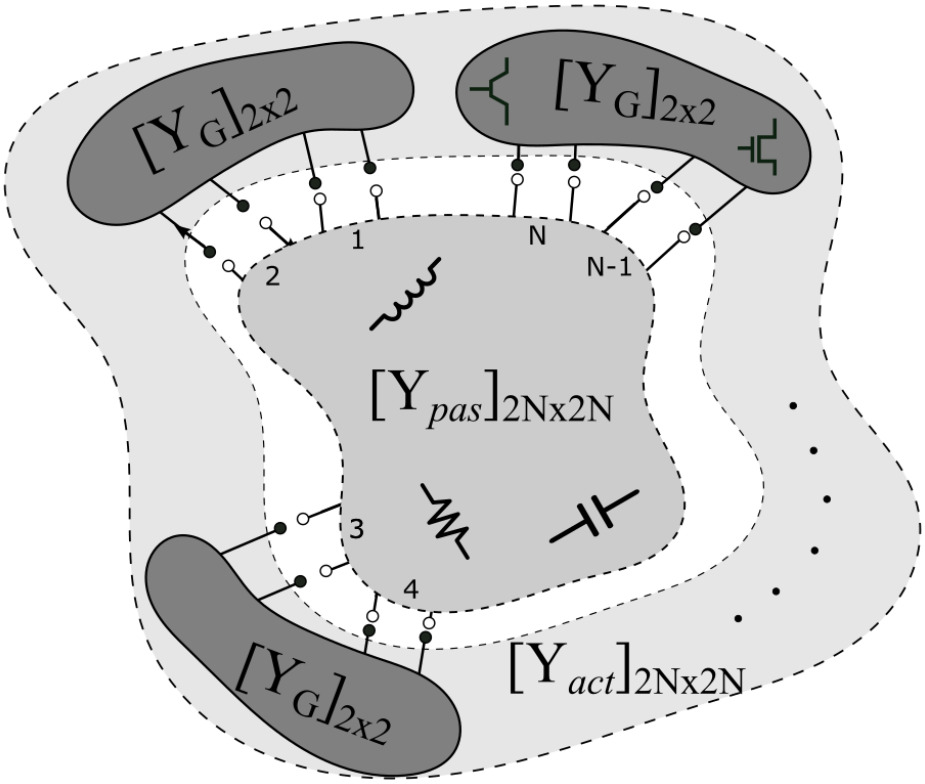


Figure 2.3: General N-port oscillator made of Y_{pas} and Y_{act} in parallel connection

where $\mathbf{Y}_{pas}$ and $\mathbf{Y}_{act}$ are the $MN \times MN$ admittance matrices of the passive and active networks, respectively. In previous works [10], the active network is assumed to consists of identical negative resistances; i.e. $\mathbf{Y}_{act} = -G\mathbf{I}$, where $\mathbf{I}$ is the unit matrix and G is the magnitude of negative conductance. Thus, the values of G that render the circuit marginally stable are the same as the eigenvalues of $\mathbf{Y}_{pas}$. In this work identical 2-port active components are used; thus $\mathbf{Y}_{act}$ is given by:

$$\mathbf{Y}_{\text{act}} = \begin{bmatrix} [\mathbf{Y}_G] & 0 & \dots \\ 0 & [\mathbf{Y}_G] & \dots \\ \vdots & \vdots & \ddots \end{bmatrix} \tag{2.2}$$

where $\mathbf{Y}_G$ is the 2×2 admittance matrix of the active components. For simplicity Y_{act} is assumed to be independent of frequency and all parasitics associated with the active devices

are partitioned in the passive network.

Each solution of (2.1) represents a possible oscillatory operation, called an *oscillation mode*, which corresponds to a different phase difference and amplitude ratio at the ports. Let us assume that a frequency $\omega_{o,i}$ satisfies (2.1) for a given Y_{pas} and Y_{act}. Zero determinant of Y_{tot} implies that its null-space is nonzero [22]. To have a single-mode oscillation this nullspace must be of dimension one, represented by a $1 \times 2N$ vector.

$$\mathbf{V}_i = \text{Nullspace}\{\mathbf{Y}_{pas}(j\omega_{o,i}) + \mathbf{Y}_{act}\} \tag{2.3}$$

$$\mathbf{V}_i = \text{Nullspace}\{\mathbf{Y}_{tot}(j\omega_{o,i})\} \tag{2.4}$$

where V_i is the vector of port voltages at the i-th mode, whose elements have complex values as

$$\mathbf{V}_i = A \times [1,\ a_{2i}e^{j\phi_{2i}},\ ...,\ a_{2Ni}e^{j\phi_{2Ni}}] \tag{2.5}$$

where A is the voltage amplitude at port 1 (usually normalized to 1) and $a_{ni}e^{j\phi_{ni}}$ is a complex number, representing the relative voltage at the n^{th} port normalized to A. The voltage at the n^{th} port oscillating at the i^{th} mode is given by:

$$v_{n,i}(t) = Aa_n cos(\omega_{o,i}t + \phi_{n,i}) \tag{2.6}$$

The number of $Y_{\text{act,i}}$ that satisfies (2.1) and has a one-dimensional nullspace indicates the number of possible oscillation modes. Higher dimensions of the nullspace lead to oscillation for which port voltages can take any arbitrary phases.

2.4 Analysis of QVCOs

The method explained in the previous section can be employed to analyze a wide range of QVCOs, including both conventional and resonant-coupled QVCOs.

2.4.1 Analysis of Conventional QVCO

Eq. (2.1) is directly applicable to the conventional QVCO shown in Fig. 2.1, where $N = 2$, and the passive part of the circuit is the two-port network composed of two parallel RLC circuits shunted to ground. The active component, Y_G, is the parallel connection of the cross-coupled pair, g_{m1}, which realizes the coupling, and negative resistance, g_{m2} – see Fig. 2.2(a). Considering the linearized equivalent circuit for FETs, this gives:

$$\mathbf{Y}_{act} = \begin{bmatrix} 0 & -g_{m1}/2 \\ g_{m1}/2 & 0 \end{bmatrix} + \begin{bmatrix} -g_{m2}/2 & 0 \\ 0 & -g_{m2}/2 \end{bmatrix} \tag{2.7}$$

As shown in Fig 2.2(b), each two-port active component is characterized by a simplified linear equivalent circuit whose parasitic capacitors are absorbed into the resonance tank. The admittance matrix of the tank $\mathbf{Y}_{pas}$ can be expressed as:

$$\mathbf{Y}_{pas}(\omega) = \begin{bmatrix} Y_{RLC}(\omega) & 0 \\ 0 & Y_{RLC}(\omega) \end{bmatrix} \tag{2.8}$$

where $Y_{RLC}(\omega)$ is the admittance of each parallel RLC resonance tank. Substituting (2.8) and (2.7) in (2.1) yields:

$$2Y_{RLC}(\omega) - g_{m2} \pm j g_{m1} = 0 \tag{2.9}$$

For a parallel RLC network this results in:

$$\omega C - \frac{1}{\omega L} \pm g_{m1}/2 = 0 \text{ and } g_{m2,min} = \frac{2\omega L}{Q} \tag{2.10}$$

where Q is the quality factor of the tank. The oscillation frequency is given by [14]:

$$\omega_o = -\frac{g_{m1}}{2C} + \sqrt{\frac{g_{m1}^2}{4C^2} + \frac{1}{LC}} \tag{2.11}$$

By substituting (2.9) in (2.3), the normalized voltage vector for the oscillation mode at ω_o can be obtained as:

$$\mathbf{V}_+ = [j, 1] \tag{2.12}$$

which verifies the quadrature signals in the differential circuit.

Although there is no limitation on the coupling transconductance, g_{m1}, on the oscillation start-up, this parameter plays a critical role in the accuracy of the quadrature phases. In other words, a small g_{m1} may lead to large deviation from quadrature phases in the presence of mismatch in active and passive components. Assuming a small mismatch between admittance's of the tanks given by $Y'_{RLC}(\omega_o) = Y_{RLC}(\omega_o)(1+\delta)$, where $\delta \ll 1$, leads to deviation in normalized voltage vector expressed as

$$\mathbf{V}_+ = [j + \frac{2Y_{RLC}}{g_{m1}}\delta, 1] \tag{2.13}$$

which implies that the error for a small mismatch may result in large phase error if g_{m1} is kept small. On the other hand, the phase noise degrades as the g_{m1}/g_{m2} ratio increases [14]. Therefore the only way to maintain low phase noise and phase error is to increase both g_{m1}

and g_{m2}, which leads to high DC power dissipation or limits the frequency tuning range [14]. This fundamental trade-off severely limits the performance of this topology particularly at high frequencies.

2.4.2 Analysis of Resonant-Coupled QVCOs

The method described in the previous section can be applied to resonant-coupled QVCOs where the passive network is a 4-port coupling/resonator tank as shown in Fig. 2.2(a). $Y_0(\omega)$ is a two-port network duplicated between ports (1, 2) and (3, 4) considering the port orders. The admittance of each 2-port network is given by:

$$\mathbf{Y}_0(\omega) = \begin{bmatrix} Y_1(\omega) & Y_3(\omega) \\ Y_3(\omega) & Y_2(\omega) \end{bmatrix} \tag{2.14}$$

which is a symmetric matrix due to reciprocity. Therefore, the admittance matrix of the entire 4-port network can be written as:

$$\mathbf{Y}_{\text{pas}(\omega)} = \begin{bmatrix} Y_1 & Y_3 & 0 & 0 \\ Y_3 & Y_2 & 0 & 0 \\ 0 & 0 & Y_1 & -Y_3 \\ 0 & 0 & -Y_3 & Y_2 \end{bmatrix} \tag{2.15}$$

where ω dependence is dropped for convenience. The negative signs are due to the crossing of differential lines. The 2-port active blocks, Y_G, can be realized in three ways using CMOS technology: a differential gm-cell, a cross-coupled pair, and a negative conductance

as shown in Fig. 2.2(b). As mentioned before the parasitic capacitances of transistors are associated with Y_G; therefore, g_m is assumed to be a real positive value. The differential pair is equivalent to a current source at the output controlled by input voltage, while the cross-coupled pair is equivalent to a negative resistance in parallel with a voltage-controlled current source. In the following subsections, resonant-coupled QVCOs using a gm-cell and a cross-coupled pair are analyzed.

QVCOs using Gm-cell

For the case when Y_G is a gm-cell, substituting (2.15) into (2.1) results in:

$$det(\mathbf{Y}_{pas}(\omega) + \begin{bmatrix} 0 & 0 & 0 & -g_m/2 \\ 0 & 0 & 0 & 0 \\ 0 & -g_m/2 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}) = 0 \tag{2.16}$$

whose solution gives the minimum g_m required for oscillation to occur:

$$g_m \pm j\frac{2}{Z_{12}(\omega_o)} = 0 \tag{2.17}$$

where $Z_{12} = (Y_1Y_2/Y_3 - Y_3)^{-1}$ is the transimpedance of the resonance network $Y_0(\omega)$.

Since g_m is assumed to be real-valued, oscillation occurs when Z_{12} becomes purely imaginary, i.e. $Re\{1/Z_{12}(\omega_o)\} = 0$. This condition in turn determines the oscillation frequency ω_o. Moreover, among the two possible solutions, the one that corresponds to $g_m > 0$ is acceptable;

this depends on the sign of $Im\{2/Z_{12}(\omega_o)\}$. All the solutions of Eq. (2.17) result in oscillation modes with quadratic phases at different frequencies; however, only the mode that requires the lowest g_m will be dominant eventually. For each mode, the minimum conductance for oscillation to occur is $g_m \geq g_{m,min} = |Im\{2/Z_{12}(\omega_o)\}|$.

These results can also be verified by observing Fig. 2.4(a). In general, a 2-port network can be replaced by an equivalent T-network whose shunt element is Z_{12}. Therefore, the threshold of oscillation corresponds to the loop gain being unity, i.e. $-(\frac{g_m}{2}Z_{12})^2 = 1$, which leads to (2.17).

It is reasonable to assume that $\mathbf{Y}_0(\omega)$ is realized using low-loss passive components, for which $Q \gg 1$. In general, this leads to a high-Q two-port network whose network parameters become purely imaginary as Q goes to infinity. Therefore, the first-order Taylor expansion of an arbitrary network parameter, $X(\omega)$, for such a network can be expressed as

$$X(\omega, Q) = jX_I(\omega) + \frac{1}{Q}X_R(\omega) + \mathcal{O}(\frac{1}{Q^2}) \tag{2.18}$$

where X represents an element of the $\mathbf{Z}$ or $\mathbf{Y}$ matrix, and X_I and X_R are real-valued functions. Applying this approximation to (2.17) leads to the fact that ω_o and $g_{m,min}$ are independent of Q for $Q \gg 1$. This is an important observation as for most oscillators such as LC VCOs and conventional QVCOs, $g_{m,min}$ for oscillation start-up is proportional to $1/Q$.

Both solutions of (2.17) lead to two 1-dimensional nullspaces whose voltage vectors can be expressed as:

$$\mathbf{V}_{\pm} = [\pm j\frac{Y_2(\omega_o)}{Y_3(\omega_o)},\ \mp j,\ \frac{Y_2(\omega_o)}{Y_3(\omega_o)},\ 1]. \tag{2.19}$$

Similarly the acceptable solution corresponds to $g_m > 0$, i.e., for $Im\{1/Z_{12}(\omega_o)\} < 0$ using

the upper signs in (2.19). If we express $Y_2(\omega_o)/Y_3(\omega_o)$ as $\rho e^{j\theta}$, then (2.17) can be written as:

$$\mathbf{V}_{\pm} = [\pm j\rho e^{j\theta},\ \mp j,\ \rho e^{j\theta},\ 1] \tag{2.20}$$

It can be observed that in both cases ($\mathbf{V}_{\pm}$), the phase difference between ports (1,3) and (2,4) are $\pm 90°$, independent of passive network parameters. Therefore, a pair of differential ports provides the quadratic phases of QVCO at these ports.

In summary, the quadrature oscillation occurs in this QVCO under the following conditions:

1. $Y_0(\omega)$ must have some non-zero coupling between its input and output ports, i.e., $|Y_3(\omega)| \neq 0$ to avoid division by zero. This essentially assures the closed-loop operation of QVCO at the oscillation frequency.

2. $Z_{12}(\omega)$ must be purely imaginary at the frequency of interest, which guarantees the $360°$ phase shift along the loop.

Numerous passive networks, including both magnetically and capacitively coupled tanks [15] [19], could be used to realize QVCOs. These are studied in the following sections.

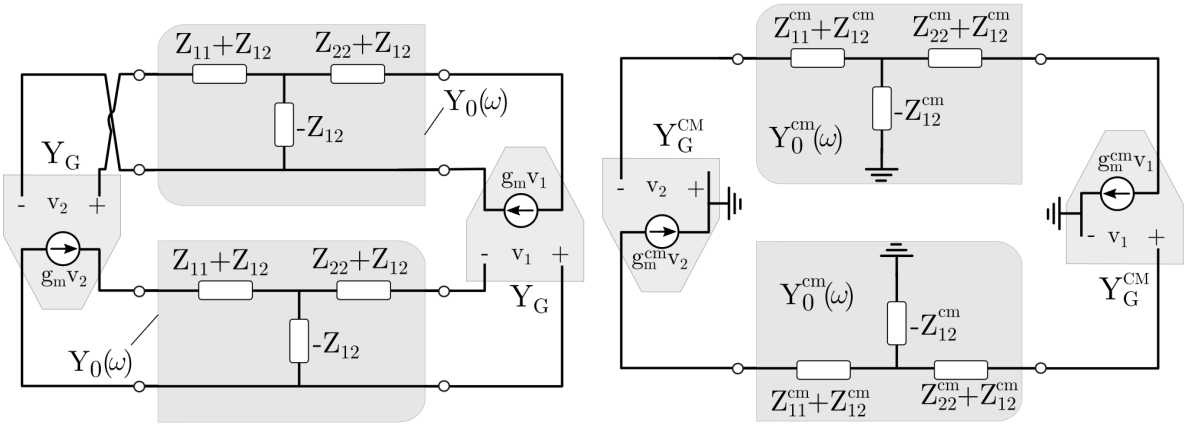


Figure 2.4: Resonant-coupled QVCO loop based on T-network equivalent circuit in (a) differential (b) common-mode operation.

QVCOs using Cross Coupled Pairs

In this subsection a class of QVCOs is analyzed whose Y_G blocks are implemented as cross-coupled pairs as shown in Fig. 2.2(b). Substituting (2.15) into (2.1) results in:

$$\det(\mathbf{Y}_{pas}(\omega) + \frac{1}{2}\begin{bmatrix} g_m & 0 & 0 & g_m \\ 0 & -g_m & -g_m & 0 \\ 0 & g_m & g_m & 0 \\ -g_m & 0 & 0 & -g_m \end{bmatrix}) = 0 \tag{2.21}$$

whose solution gives the minimum value of g_m for which oscillation occurs:

$$g_m - \frac{2}{\pm 2jZ_{12}(\omega_o) + Z_{11}(\omega_o) - Z_{22}(\omega_o)} = 0 \tag{2.22}$$

Similar to the previous QVCO type, the g_m is assumed to have a positive real value; therefore at the oscillation frequency, ω_o, the imaginary part of the second term equates to zero. The

number of acceptable solutions for g_m is determined by the sign of the real part of the second term. Furthermore, based on the approximation in (2.18) for low-loss networks ($Q \gg 1$), the real parts of the Z parameters are very small relative to the imaginary parts. Therefore, the real part of the second term in (2.18) is dominated by the jZ_{12} term. Thus, depending on the sign of jZ_{12} one solution is acceptable. The voltage vector of the oscillation is given by:

$$\mathbf{V}_{\pm} = [\pm\frac{Y_2 \mp jY_3}{-Y_2 + jY_1},\ \ \pm j,\ \frac{Y_2 + jY_3}{Y_2 + jY_1},\ 1]. \tag{2.23}$$

where the upper signs should be chosen when $Z_{12} > 0$. It can be seen that the phase difference between ports 2 and 4 is always 90° independent of circuit parameters. It is interesting to study the case of zero coupling between the ports of the passive network for which $Y_3 = 0$ leads to $Z_{12} = 0$. Thus, the two solutions for g_m will be identical, which leads to a 2-dimensional nullspace. This can be interpreted as an under-determined system in which the two uncoupled oscillators operate independently and thus the phase difference between them is not enforced by the design and depends only on the initial condition. However, these oscillators could be coupled through the second harmonic of the signal as explained in [23].

2.4.3 Phase Error in QVCOs

Sufficient conditions for quadrature oscillation were described in the previous subsection assuming perfect symmetry in the circuit. However, in the presence of mismatches in the passive and active devices, as well as in the parasitic elements, the phase difference between ports may deviate from 90°. Now let us consider the effect of two types of mismatches: First, we will assume a small relative mismatch, ϵ, between the transconductances of the

two active networks; i.e. $g'_m = g_m(1+\epsilon)$. Second, we will assume a relative mismatch δ between the coupling elements of the passive network; i.e. $Y'_3 = Y_3(1+\delta)$ where Y_3 and Y'_3 are the transadmittance of two passive networks and δ is a complex number representing the relative mismatch. For low-loss networks, Y'_3 and Y'_3 are purely imaginary, δ is purely real with magnitude much smaller than unity. This imposes both phase and amplitude imbalances in the voltage vector of (2.19) given by:

$$\mathbf{V}_{\pm} = [\pm j\rho e^{j\theta}\alpha,\ \ \mp j\alpha,\ \ \rho e^{j\theta}\delta,\ \ 1] \tag{2.24}$$

where

$$\alpha = 1 + j\delta\,\frac{Y_3^2 + Y_1Y_2}{Y_3^2 - Y_1Y_2} + \epsilon\frac{g_m Z_{12}}{4} \tag{2.25}$$

Let us focus on phase error as quadrature operation is crucial for QVCOs. From (2.24) it is evident that the phase deviates from quadrature by $\angle\alpha$. In high-Q passive networks all network parameters have very small real parts; thus the second term in (2.25) is nearly purely imaginary resulting in phase deviations. To reduce the phase error Y_3 should be high and Z_{12} should be low, which both means that the coupling between the two ports must be strong. The last term in (2.25) is purely imaginary and proportional to the loop gain, and thus, similar to the previous case, it primarily contributes to the phase error rather than the amplitude.

2.4.4 Common-Mode Analysis of QVCOs

The common-mode (CM) equivalent circuit of the Fig. 2.2 QVCO can be constructed by simply merging each differential line into a single common-mode node. Matrices Y_0^{CM} and Y_G^{CM} are defined as the common-mode admittance matrices of the 2-port passive and active

components, respectively. Fig. 2.4(b) shows the common-mode equivalent circuit of the QVCO loop based on T-networks. Assuming that Y_0 is a two-port network with *differential symmetry* (positive and negative ports are interchangeable), Y_0^{CM} can be expressed as:

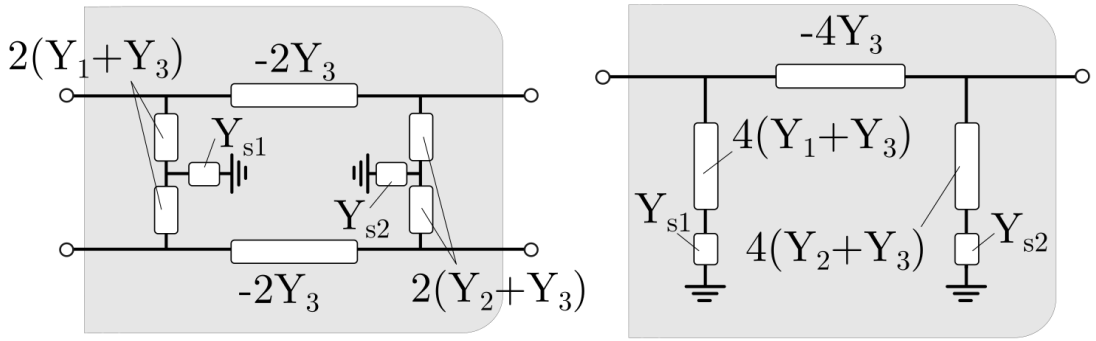
$$\mathbf{Y}_0^{cm} = \begin{bmatrix} Y_1^{cm} & Y_3^{cm} \\ Y_3^{cm} & Y_2^{cm} \end{bmatrix} \tag{2.26}$$

The condition for common-mode oscillation can also be derived using the multi-port oscillation theory. Generally, such oscillation is undesirable and must be suppressed through the design process. Similar to the previous section, since we are dealing with two types of active networks, the CM oscillation start-up condition must be studied for each case. For the cross-coupled network, there is no possibility of CM oscillation, as it is equivalent to a diode-connected transistor pair whose small-signal resistance is $(2g_m)^{-1}$. On the other hand, transistors of gm-cell act as two parallel transistors in CM; therefore, the CM transconductance matrix is similar to that of the differential one; i.e.,

$$\mathbf{Y}_{\mathrm{G},gcell}^{cm} = \begin{bmatrix} 0 & 0 \\ -g_m^{cm} & 0 \end{bmatrix} \tag{2.27}$$

Assuming that the current source of the gm-cell has a large output resistance of r_o, g_m^{cm} is significantly small due to source degeneration effect; i.e. $g_m^{cm} = g_m/(1 + g_m r_o)$. Thus, CM oscillation is very unlikely. On the other hand, for a pseudo-differential pair (without current source), $g_m^{cm} = g_m$, which leads to:

$$det(\begin{bmatrix} Y_1^{cm} & Y_3^{cm} & 0 & -g_m^{cm} \\ Y_3^{cm} & Y_2^{cm} & 0 & 0 \\ 0 & -g_m^{cm} & Y_1^{cm} & Y_3^{cm} \\ 0 & 0 & Y_3^{cm} & Y_2^{cm} \end{bmatrix}) = 0 \tag{2.28}$$



(a) (b)

Figure 2.5: (a) a general two port network with admittance parameter in Eq. (2.14), (b) equivalent CM representation when all nodes on virtual ground line are actually connected to ground.

Thus the oscillation start-up condition is given by:

$$g_m^{cm} - \frac{1}{Z_{12}^{cm}(\omega)} = 0 \tag{2.29}$$

where $Z_{12}^{cm}(\omega)$ is the CM transimpedance. Since g_m^{cm} is assumed to be real, the oscillation frequency is determined by $Im\{Z_{12}^{cm}(\omega_o)\} = 0$. Therefore a necessary condition to prevent CM oscillation is $g_m^{cm} < \mathrm{Re}\{1/Z_{12}^{cm}(\omega_o)\}$.

Differential passive networks are typically implemented with differential symmetry as the equivalent circuit is shown in Fig. 2.5(a). The CM π-network can be derived as shown in Fig. 2.5(b). It should be noted that shunt elements without middle ground connections do not appear in the equivalent CM circuit. These middle points of the shunt elements are connection to ground through series elements with admittances of Y_{s1} and Y_{s2}. As discussed in following sections, these elements can be chosen to lower the Z_{12} to suppress the CM oscillation.

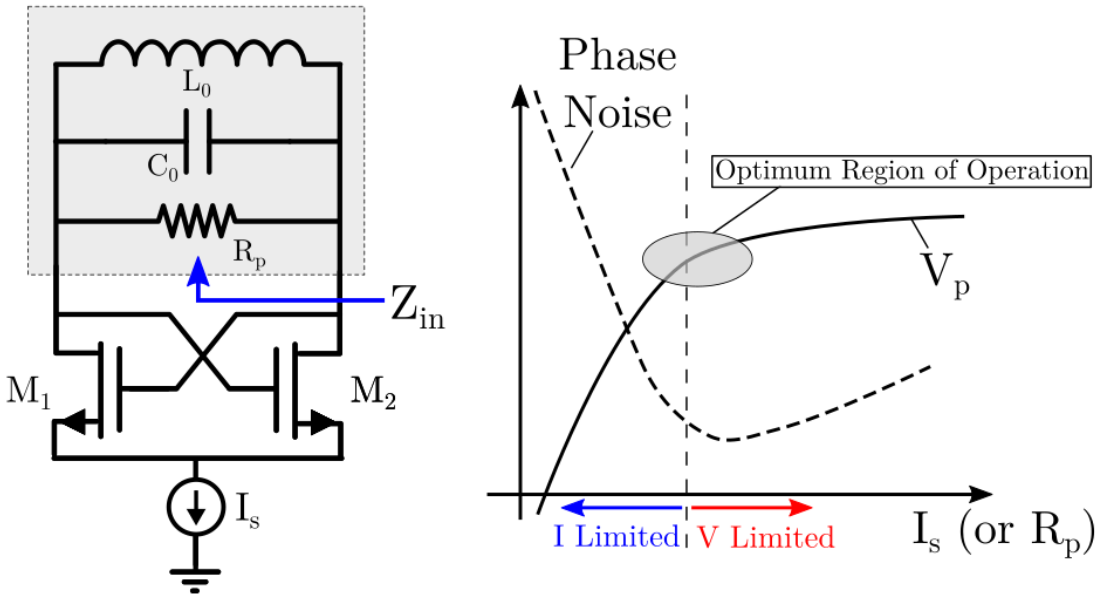


Figure 2.6: Phase noise and oscillation amplitude for a cross coupled oscillator with respect to tail bias current.

2.5 Phase Noise Optimization of QVCOs

As explained in the previous section, if certain criteria for Y_0 and Y_G to start up oscillation are met, then quadrature operation will be achieved. The freedom of choice for $Y_0(\omega)$ can be exploited to achieve low phase noise.

The phase noise of an oscillator, based on Leeson's Equation, is given by [8]:

$$\mathcal{L}(\Delta\omega) = 10\,\log_{10}\left[\frac{FK_BT}{Q^2}\,\frac{R_p}{V_p^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2\right] \tag{2.30}$$

where the noise factor F is an empirical value that models the noise contributions of the active devices, $\Delta\omega$ is the offset frequency, ω_0 is the carrier frequency, Q is the quality factor of the tank, V_p is the voltage swing, and R_p is the equivalent parallel resistance of the tank.

As shown in Fig. 2.6, for constant R_p, the amplitude of oscillation grows with the bias current I_s (current-limited-region) up to a point where the current source transistor enters

the triode region, at which point the voltage swing remains constant, nearly independent of I_s (voltage-limited-region). In the current-limited region, the increase in the the voltage swing is accompanied by a decrease in the phase noise until the edge of the current-limited-region is reached. Any further increase in the bias current will cause an increase in the transistor noise factors, thereby degrading the phase noise [9]. Therefore, the optimum region of operation is the edge of the current-limited-region that sets the bias current. It should be noted that the voltage swing can be changed by R_p as well as I_s, then the x-axis can represent R_p if I_s is fixed.

The main phase noise contributors for the oscillator in Fig. 2.6 are the tank loss (R_p), the differential pair, and the bias current source. To investigate the effect of the latter ones, let us consider different topologies of the active circuitry used in the VCOs. In Fig. 2.7(a) a pseudo-differential pair is connected to the resonance tank without a tail current source. Depending on the phase difference ϕ between the drain and gate each NMOS spends some portion of the oscillation period in the triode region. During this time, the NMOS acts as a resistor that loads the tank and reduces the quality factor [24]. By adding the tail current source, as shown in Fig. 2.7(b), the differential transistors are degenerated and do not load the tank in when they are in triode. Essentially the current source provides a high impedance in common node, which reduces the contribution of the differential pairs to the phase noise. However, as evident from noise factor equation in 2.7(b), the tail current source itself adds to the tank noise since its low-frequency (flicker noise) and $2\omega_o$-noise is down-converted by the differential pair acting as a single-balanced mixer [24]. However, the noise of the tail current source can be shorted to ground by a large capacitor connected to the source-coupled node as shown in Fig. 2.7(c). It is shown that this node must have high impedance only at second harmonics of ω_o to reduce the differential pair contribution. One way to achieve this is adding a parallel LC with resonance of $2\omega_o$ to the common node. Moreover, Murphy et al. [25] recently showed that coupled inductors can also provide high impedance at $2\omega_o$; these inductors could replace the current source.

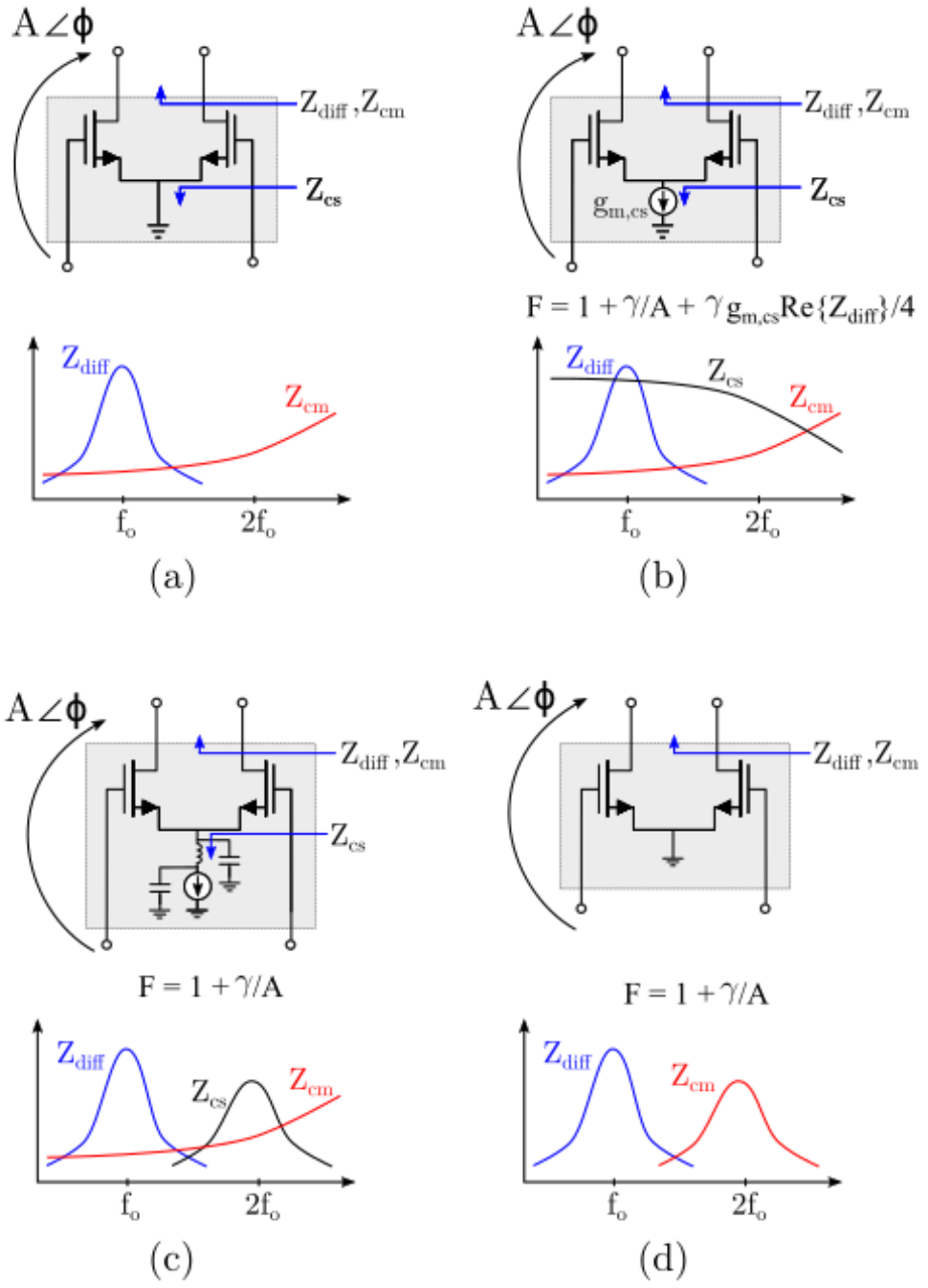


Figure 2.7: Noise factor, F, of gm-cell (a) without current source (b) with a current source (c) with current source and tail resonance (c) without current source with high CM impedance in tank.

Table 2.1: Quadrature VCO

	Y_{act}	Y_{pass}	N-port
[19]	gm-cell	Capacitive	4 port
[15]	CC pair	Magnetic	4 port
[16]	gm-cell	Magnetic	4 port
[13]	gm+CC	LC	2 port
[17]	gm+CC	Magnetic	4 port

These conclusions can be confirmed by calculating the impulse sensitivity function (ISF) of the noise contributors [26]. The phase noise of an oscillator is offset frequency $\Delta\omega$ is related to the ISF, $\Gamma(x)$, of the noise sources as follows:

$$\mathcal{L}(\Delta\omega) = 10\ \log_{10}\Big[\frac{1}{4q_{max}^2}\ (\frac{\bar{i_n^2}}{\Delta f})\Big(\frac{\Gamma_{rms}^2}{\Delta\omega^2} + \frac{\Gamma_{DC}^2}{2\Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\Big)\Big] \tag{2.31}$$

where q_{max} is the charge injected into an oscillator node by the noise source, which is equal to the maximum charge stored on the tank capacitor during oscillation, and $\omega_{1/f}$ is the flicker noise corner frequency. Γ_{rms} and Γ_{DC} are the rms and DC values of $\Gamma(x)$, respectively.

2.6 Design/Analysis Examples

Table 2.1 summarizes different design examples that are explained in this section.

2.6.1 Capacitively Coupled QVCOs

A pair of capacitively coupled two-port circuits can be used as the passive network, along with the gm-cell for the active network [19]. Fig. 2.8 shows the schematic of capacitively coupled QVCO (CCQVO). Each passive network is composed of two LC tanks coupled with

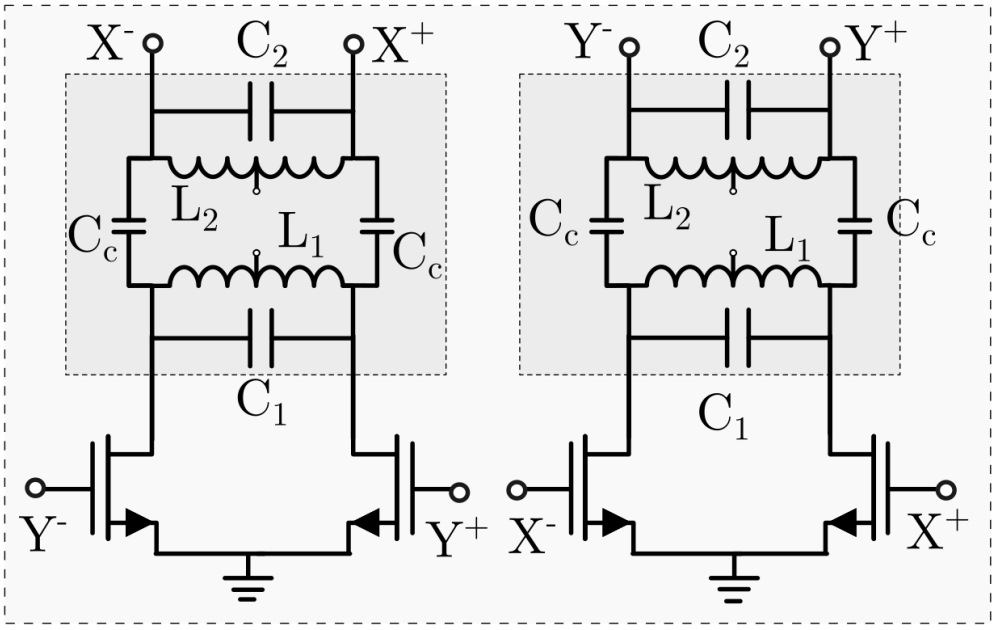


Figure 2.8: Schematics of QVCO with capacitively coupled, C_c, resonance tanks

a series capacitors, C_c.

For such a network elements of the admittance matrix, $\mathbf{Y}_0$, are given by:

$$Y_i = \frac{1}{j\omega L_i}(1 + \frac{j}{Q_L}) + j\omega(C_i + C_c),\ i = 1, 2 \tag{2.32}$$

$$Y_3 = -j\omega C_c \tag{2.33}$$

where $i = 1, 2$, $R_{s,i} = \omega L_i / Q_L$ is the series resistance of inductor L_i and Q_L is the quality factor of the inductors. In this work it is assumed that the quality factor of the passive network is dominated by inductors since in most CMOS processes the quality factor of the fixed capacitors, Q_c, is generally much higher than Q_L ($Q_c \sim 50$ versus $Q_L \sim 15$). However, the quality factor of varactors that are used for frequency tuning can be relatively low. Based on (2.17), the oscillation frequency obtained by solving $Re\{Z_{12}\} = 0$, and assuming

that $Q_L \gg 1$, yields:

$$\omega_o = \sqrt{\frac{2}{C_c(L_1+L_2)+C_1L_1+C_2L_2}}, \tag{2.34}$$

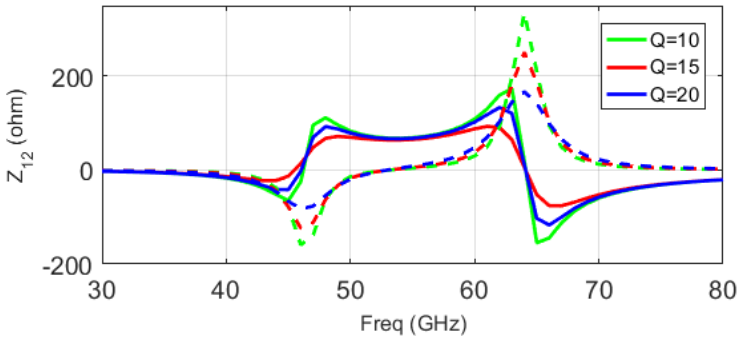
and the oscillation start-up condition is given by:

$$g_{m,min} = \Big[\frac{2L_1L_2C_c}{(C_cL_1-C_cL_2+C_1L_1-C_2L_2)^2+4L_1L_2C_c^2}\Big]^{-1} \tag{2.35}$$

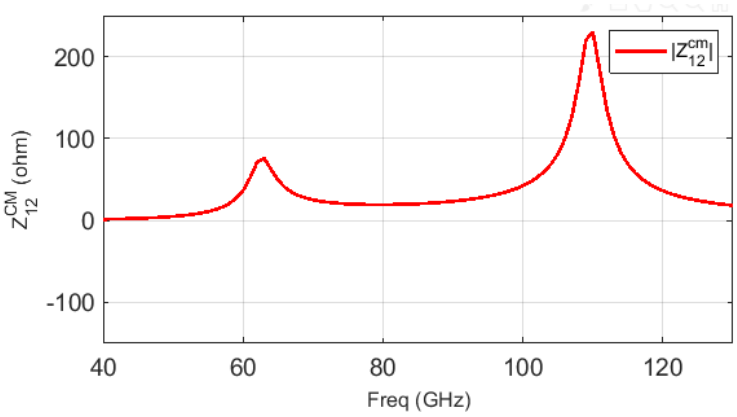
It is interesting to note that if $Q_L \gg 1$, then neither the oscillation frequency nor the start-up condition depends on Q_L. The real and imaginary parts of Z_{12} in differential mode are plotted in Fig. 2.9(a), indicating that the zero crossing (ω_o) occurs around 54 GHz nearly independent of Q_L. Moreover, $\mathrm{Im}\{Z_{12}(\omega_o)\}$ indicates that the $g_{m,min}$ slightly varies with Q (about 10% as Q increases by a factor of 2). This is fundamentally different from a conventional QVCO in which the oscillation start-up only depends on the tank Q and quadrature phase is guaranteed by a separate mechanism. On the other hand, in CCQVCO the start-up of oscillation and quadrature phase relations are guaranteed by (2.35).

Fig. 2.9(b) shows the common-mode transimpedance of the passive network. For simplicity let us assume $L_1 = L_2 = L$ and $C_1 = C_2 = C$, which results in the following resonant frequency and minimum transconductance:

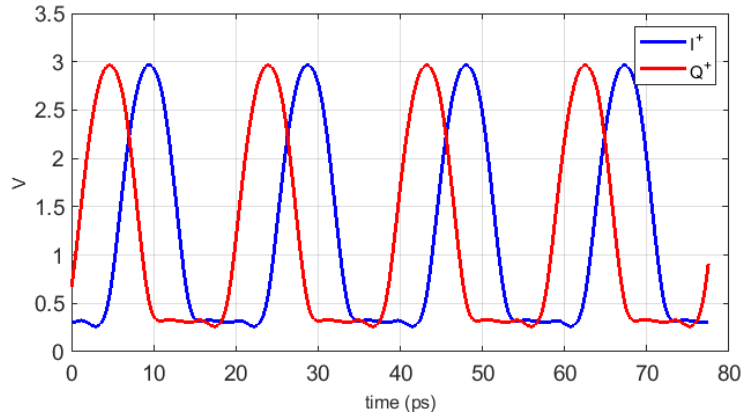
$$\omega_o = \sqrt{\frac{1}{L(C_c+C)}}, \quad g_{m,min} = 2\omega_o C_c \tag{2.36}$$



(a)



(b)



(c)

Figure 2.9: (a) Real (dashed line) and Imaginary (solid line) part of Z_{12} in differential mode for $Q = 10$, 15, 20 (b) $|Z_{12}|$ in common-mode for $Q = 10$, (c) quadrature voltage in time domain when $L_1 = L_2 = 110pH$, $C_1 = 88fF$, $C_2 = 45fF$, $C_c = 10fF$ and $W/L = 38\mu m/60nm$

Therefore, assuming that ω_o is fixed decreasing the C_c helps the oscillation start-up condition. However it should be noted that this is equivalent to reducing the coupling, Y_3, which in turn will worsen the phase error issue due to active and passive mismatch discussed in Section 2.4.3. Therefore there is a fundamental trade off between phase error and minimum g_m for oscillation in this QVCO.

The voltage vector parameters, ρ and θ, (Eq. 2.20) can be calculated as:

$$\rho e^{j\theta} = \frac{1}{C_c L_2}\Big(\frac{1}{\omega'^2} + \frac{j}{Q\omega_o^2}\Big) \tag{2.37}$$

where $\omega'^2 \equiv 2/(L_1(C_1 + C_c) - L_2(C_2 + C_c))$.

2.6.2 Magnetically Coupled QVCOs

Fig. 2.10 shows two types of magnetically coupled QVCOs (MCQVCO) using identical passive networks, but different active networks including (a) gm-cell and (b) cross-coupled pair. The passive network is composed of two pairs of mutually coupled inductors with coupling coefficient of k and two shunt capacitors at the inputs and outputs.

The elements of the Y-parameter matrix corresponding to the resonance tank are given by:

$$Y_i = j\omega C_i + \frac{1}{j\omega L_i(1-k^2)}\Big[1 + \frac{j}{Q}\frac{1+k^2}{1-k^2}\Big],\ i = 1, 2 \tag{2.38}$$

$$Y_3 = \frac{k}{j\omega\sqrt{L_1 L_2}(1-k^2)}\Big[1 + \frac{j}{Q}\frac{1}{1-k^2}\Big] \tag{2.39}$$

in which the series resistance of inductors is substituted by, $R_{s,i} = \omega L_i/Q_L$, and the inductor quality factor Q_L is assumed to be much larger than unity. Fig. 2.11 shows the real and imaginary parts of Z_{12} of a magnetically coupled tank.

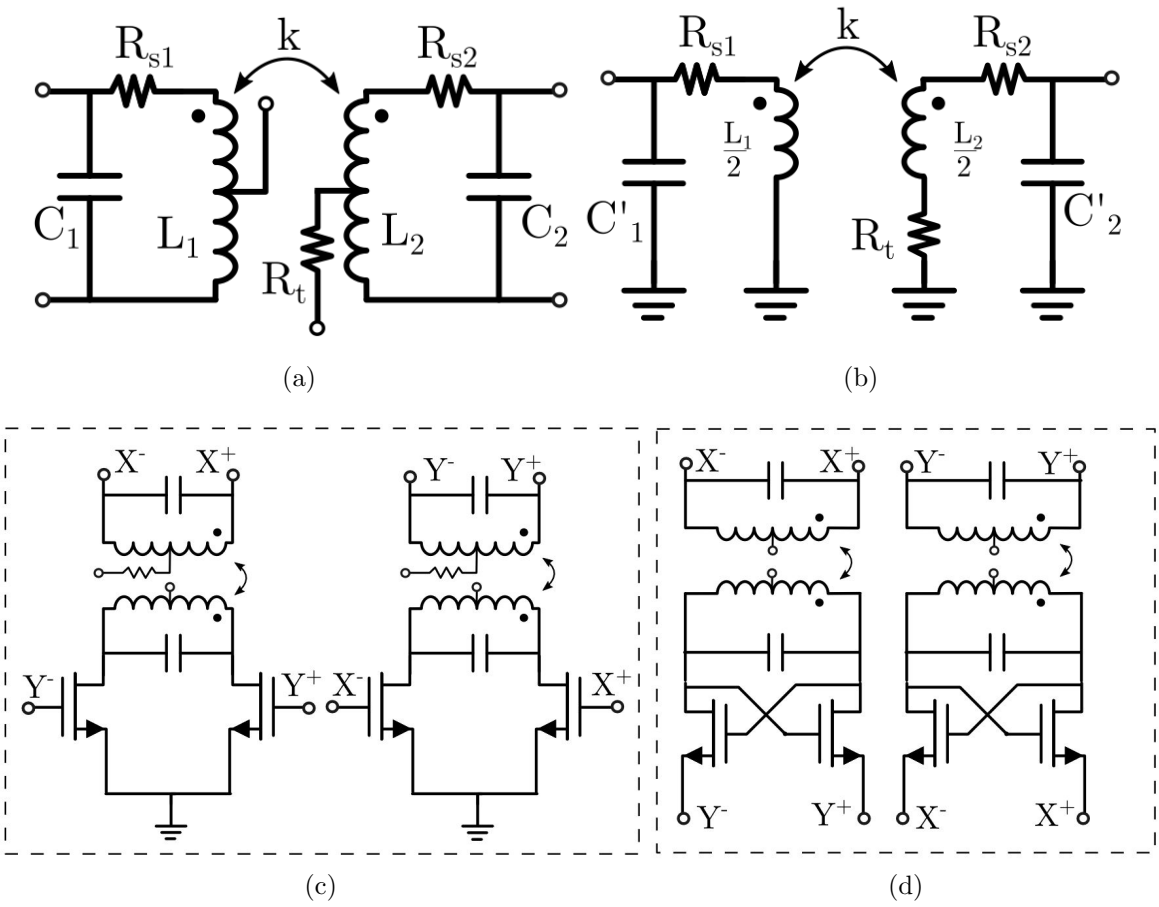


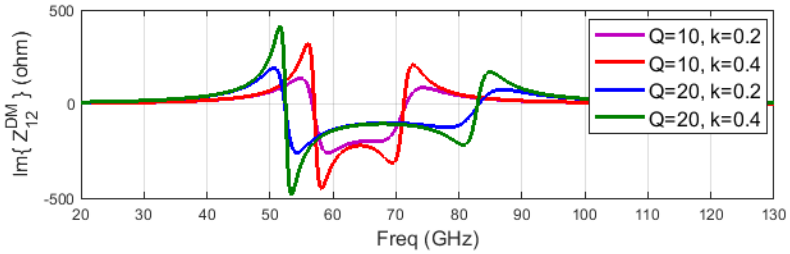
Figure 2.10: (a) Schematic of magnetically coupled tank in differential mode, (b) in common mode (c) MCQCVO based on gm-cell (d) MCQVCO based on cross-coupled pairs.

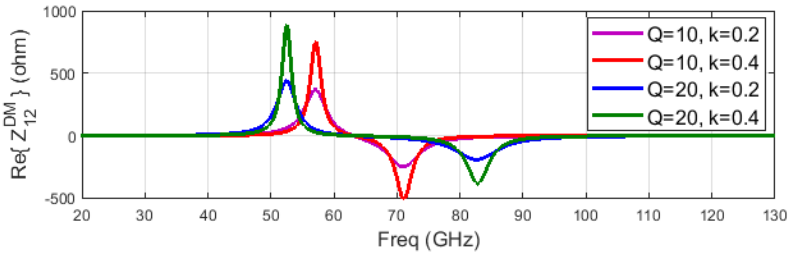
Gm-cell based MCQVCO

The oscillation frequency is obtained by $\mathrm{Re}\{1/Z_{12}\} = 0$, which gives:

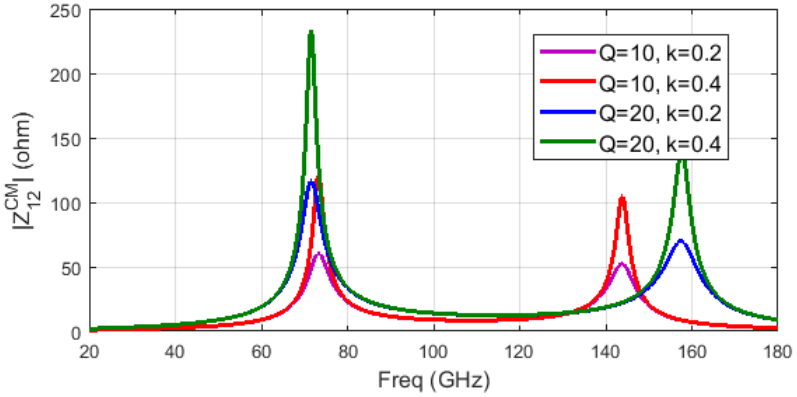
$$\omega_0 = \sqrt{\frac{1}{2}\left(\frac{1}{L_1 C_1} + \frac{1}{L_2 C_2}\right)} \tag{2.40}$$

This result is not in agreement with [16], and the discrepancy originates from the two possible ways of modeling the inductors' loss. In [16] the tank loss is modeled by a constant equivalent resistance in parallel with a capacitor that erroneously leads to a k-dependent frequency. Whereas modeling a series resistance, shown in Fig. 2.10(a), results in the oscil-





(a)



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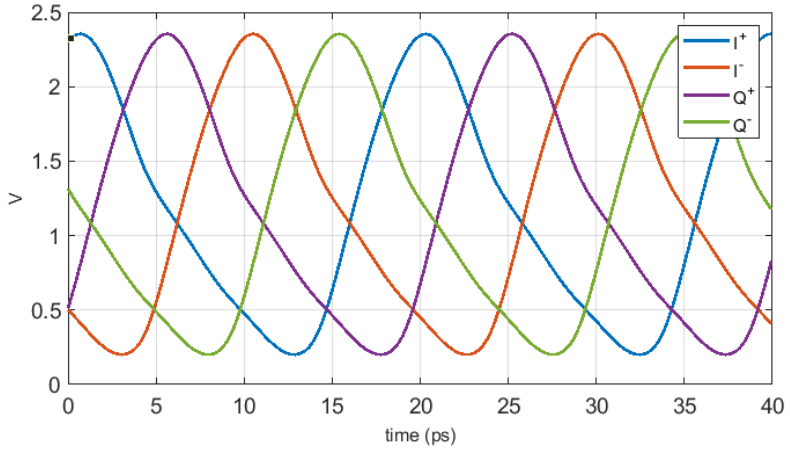


(c)

Figure 2.11: (a) Imaginary and real part of Z_{12} in common-mode in differential mode, (b) magnitude of Z_{12} in common-mode of the resonance tank for various Q and k values, $L_1 = L_2 = 110pH$, $C_1 = 50fF$, $C_2 = 50fF$, (c) voltages at the QVCO output versus time.

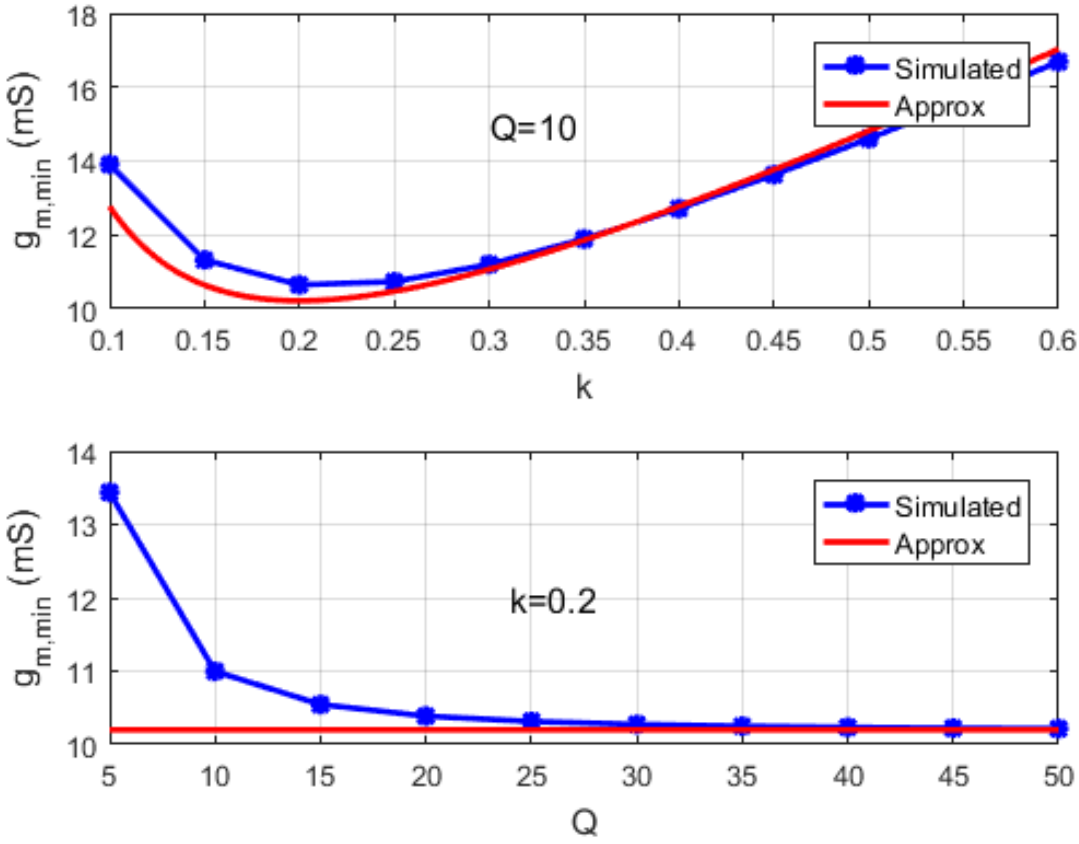


Figure 2.12: Simulated and approximated (Eq. 2.41) $g_{m,min}$ versus coupling coefficient and quality factor.

lation frequency independent of k as in (2.40). Fig. 2.11 shows that for $Q \gg 1$ the oscillation frequency depends on neither k nor Q. The minimum transconductance is given by:

$$g_{m,min} = 2\frac{(L_1C_1 + L_2C_2)\omega^2 - \omega_o^4 L_1L_2C_1C_2(1-k^2) - 1}{k\omega_o\sqrt{L_1L_2}} \tag{2.41}$$

Fig. 2.12 shows that $g_{m,min}$ obtained from (2.41) agrees well with simulation results for $Q \gg 1$. Moreover, it verifies that for $Q \gg 1$, $g_{m,min}$ is almost constant. For simplicity, if

we assume $C = C_1 = C_2$ and $L = L_1 = L_2$, (2.41) and (2.40) lead to:

$$\omega_0 = \frac{1}{\sqrt{LC}},\ g_{m,min} = 2\frac{k}{L\omega_o} \tag{2.42}$$

It is apparent that in order to minimize $g_{m,min}$, the coupling factor k must be sufficiently small, which leads to higher phase error ($Y_3 \to 0$), similar to the capacitively coupled case.

As explained in Section 2.4.4, the common-mode oscillation can be suppressed by decreasing the real part of the common-mode transimpedance, Z_{12}^{cm}. This can be achieved by adding a series resistor to the center tap of the inductors, as shown in Fig. 2.10(a). The equivalent common-mode circuit of the network is illustrated in Fig. 2.10(b). Including the center tap resistor, R_t, the common-mode transimpedance can be expressed as:

$$Z_{12}^{cm}(\omega) = \frac{2\omega k\sqrt{L_1 L_2}}{2R_t C_1'\omega(2 - L_2 C_2'\omega^2) + jA} \tag{2.43}$$

$$A \equiv \omega^2(L_1 C_1' + L_2 C_2') - \omega^4 C_1' C_2' L_1 L_2(1 - k^2) - 2 \tag{2.44}$$

where the inductor resistance is assumed to be small relative to R_t. Eq. (2.44) indicates that by increasing R_t, the real part of Z_{12}^{cm} can be decreased to prevent common-mode oscillation as per the condition in (2.29). It should be noted that R_t is connected to the center tap that provides the gate voltages, while the other center tap that draws bias current of transistors is directly connected to VDD.

The voltage vector parameters, ρ and θ, in (2.20) can be calculated as:

$$\rho e^{j\theta} = \frac{C_1 L_1(1 + k^2) - C_2 L_2(1 - k^2)}{2C_1 k\sqrt{L_1 L_2}} + \frac{jC_2 L_2}{2QkC_1\sqrt{L_1 L_2}} \tag{2.45}$$

Table 2.2: RMS and AVE values for ISF functions from node 1 and 4 for MCQVCO and CCQVCO shown in Fig. 2.13

	RMS	AVE
Γ_1^C	0.95	0.02
Γ_1^k	1.6	0.06
Γ_4^C	0.73	0.04
Γ_4^k	0.83	0.03

Therefore, for $Q \gg 1$ second term vanishes and $\theta \approx 0$; thus for such a QVCO the phase difference between the input and output of an active network is always zero.

The phase noise performance of this QVCO can be compared with the capacitively coupled QVCO (introduced in previous section) as the latter has a second-harmonic common-mode resonance that reduces the noise contribution of the differential pairs as discussed in Section 2.5. Fig. 2.13 shows the ISF of the MCQVCO and CCQVCO for one oscillation period when the current is injected into nodes 1 and 4 in Fig. 2.2. The passive network of the CCQVCO shows a resonance in Z_{12}^{cm} at the second-harmonic that is not observed in the MCQVCO, whereas the active networks for the two QVCOs are identical. The contribution of transistor noise to the phase noise is mainly due to the equivalent noise current that is injected into node 1. From (2.31), it is evident that the average and RMS values of the ISF determine the phase noise contribution of certain current source. As reported in Table 2.2, the rms values of the ISF for the MCQVCO is 1.6 , as compared to 0.95 for the CCQVCO. Therefore as explained in Section 2.5 considerable suppression of phase noise can be achieved by realization of a second-harmonic resonance of Z_{12}^{cm}.

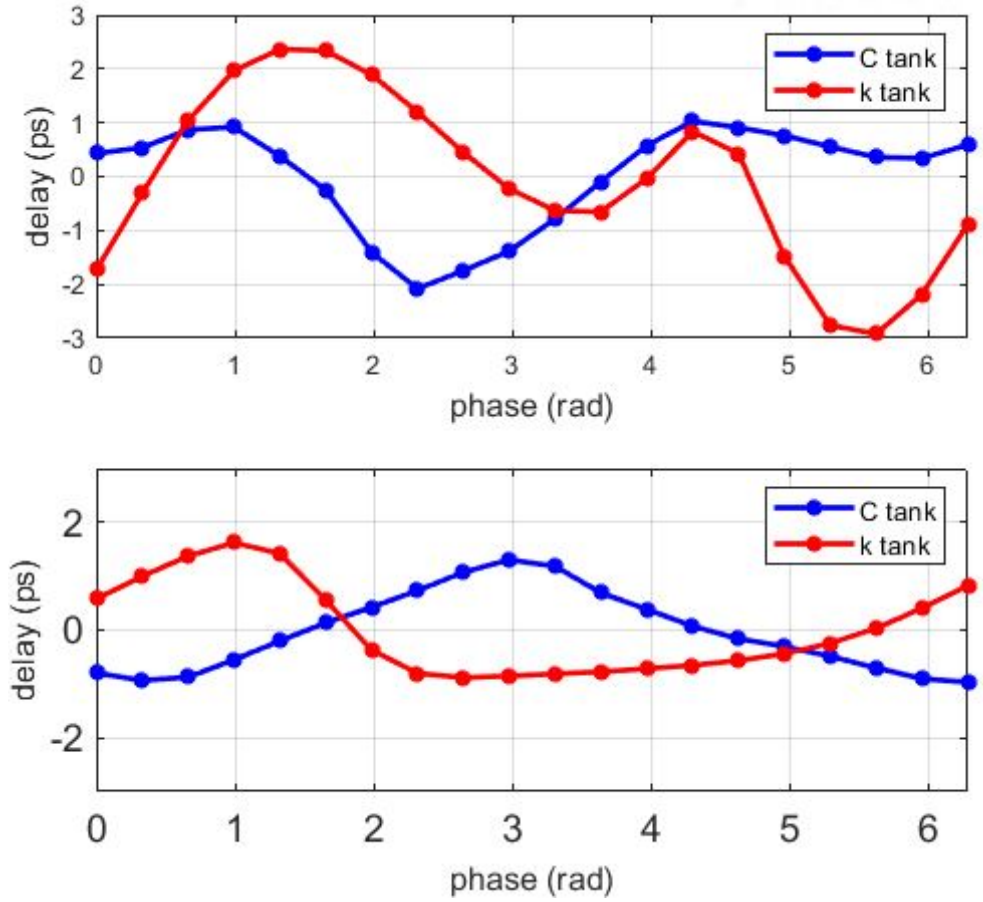


Figure 2.13: ISF for two QVCO for current injected from nodes 1 (top) and 4 (bottom) defined in Fig. 2.2

Cross-coupled pair based MCQVCO

The schematic of an MCQVCO based on a cross-coupled pair is shown in Fig. 2.10(d). For $Q_L \gg 1$, the oscillation frequency is obtained by solving (2.22) which leads to:

$$\omega_o = \sqrt{\frac{L_1 + L_2}{L_1 L_2 (C_1 + C_2)(1 - k^2)}} \tag{2.46}$$

For simplicity let us assume $L_1 = L_2$ and $C_1 = C_2$. The minimum g_m to start oscillation is given by:

$$g_{m,min} = 4\sqrt{\frac{L_1}{C_1}\frac{1 - k^2}{k}} \tag{2.47}$$

It can be seen that for small values of k the oscillation start-up requires very large conductance. This QVCO does not oscillate in common-mode due to lack of gain since the cross-coupled pair behaves as a diode-connected transistor.

2.7 Conclusion

Multi-port oscillation theory was briefly explained and used to systematically analyze different types of QVCOs. First, the conventional QVCO was studied and the oscillation frequency and start-up condition was calculated by this approach. Then, a general method to design and analyze resonant-coupled QVCOs was introduced. Quadrature phase accuracy of such QVCOs was investigated and a design method to enhance the phase noise was proposed. As

an example, two types of RCQVCOs are studied in details and the different performances specifications was compared.

2.8 Proposed QVCO Design

As mentioned earlier in this chapter, there are numerous choices for design of a passive coupling network in resonance coupled QVCOs. In this section a novel two-port network is proposed that satisfies the second harmonic resonance leading to low phase noise. Moreover, the proposed QVCO, unlike the capacitively coupled QVCO, does not exhibits a trade off between phase accuracy and power dissipation.

The passive network of the QVCO is shown in Fig. 2.14(a). This resonant tank consists of a transformer with coupling factor k and primary and secondary inductances of L_{1A} and L_{1B}, respectively. The DC biases are connected through the center taps of both windings, where they are shorted to ground by a large capacitors. Furthermore, there are two shunt inductor at the input and output whose center tap is connected to ground by capacitors C_{3A} and C_{3A}, respectively. There are also variable capacitors at the input and output ports, C_{1A} and C_{1B}, respectively, whose center connection points are grounded as shown in 2.14(a). Finally, fixed capacitors C_{2A} and C_{2B} are added to adjust the resonance frequency.

The network shown in Fig. 2.14(a), can be studied in differential- and common-mode operation. Fig. 2.14(b) shows the differential-mode equivalent circuit of the tank, in which C_{3A} and C_{3B} are eliminated as the center taps of L_{2A} and L_{2B} are grounded in differential mode.

The common-mode equivalent circuit of the tank is shown in Fig. 2.14(c). The coupling factor remains constant whereas the inductor values are divided by 4 due to their parallel connection in common-mode. It should be noted that C_{2A} and C_{2B} do not affect the common-mode as no common-mode current can flow through them. On the other hand, the center tap capacitors, C_{3A} and C_{3B}, connect the uncoupled inductors to ground, forming series LC tanks.

Having different equivalent circuits for differential- and common-mode operations facilitates

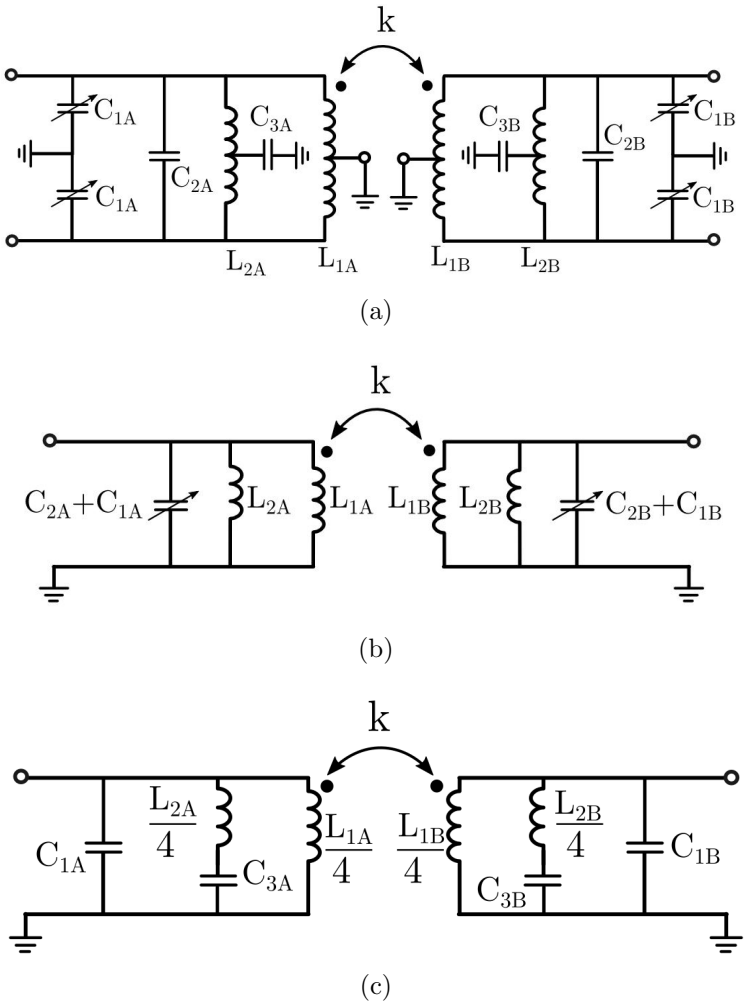


Figure 2.14: (a) schematic of the passive coupling network, (b) same network in differential mode and (c) common-mode

independent design of the impedance seen for each operation mode. As mentioned earlier, the transimpedance of the resonance tank, Z_{12}, plays a key role in operation of the QVCOs. Assuming $L_{1A} = L_{1B} = L_1$, $L_{2A} = L_{2B} = L_2$, $C_{1A} = C_{1B} = C_1$ and $C_{2A} = C_{2B} = C_2$, the resonance frequency of tank in differential mode is given by:

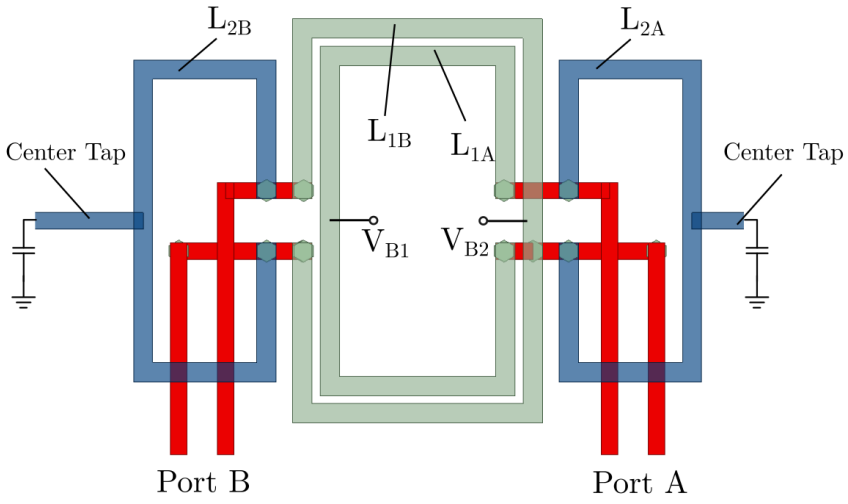
$$\omega_o = \sqrt{\frac{1}{C_1}\frac{L_2 + L_1(1-k)}{L_2 L_1(1-k)}} \tag{2.48}$$

which indicates that equivalent tank inductance is parallel connection of L_2 and $L_1(1-k)$.

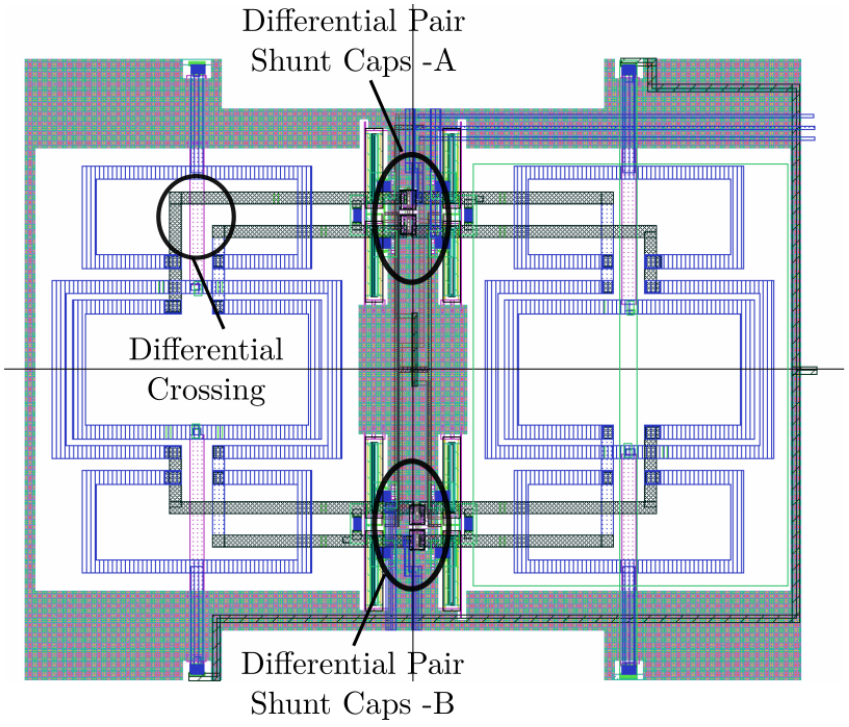
2.9 Resonant Tank Realization

Fig. 2.15(a) shows the top view of the inductors of the tank, which are realized in the top metal layer of the CMOS process. The network parameters are calculated at point A and B to consider the effect of extra transmission added to inductors terminals. The overlap between L_{1A} and L_{1B} leads to coupling factor $k = 0.55$ (see Fig. 3.16(a)) at 40 GHz, whereas since L_{2B} and L_{2A} do not overlap as their coupling is desired to be zero. It should be noted that since the inductance plotted in Fig. 3.16 is calculated from port A and B (with extra transmission line) the inductor parameters slightly vary over frequency.

This structure is modeled in HFSS with the scattering parameters exported to calculate the trans-impedance of the tank after adding the shunt capacitors. Fig. 2.21 shows the transimpedance of the tank (Fig. 2.15) with full-wave simulation of inductor in differential- and common-mode operation. In the imaginary part of the differential transimpedance crosses zero near 40 GHz, which indicates the oscillation frequency of QVCO; its real part at that frequency represents the minimum g_m for oscillation start-up. On the other hand, common-

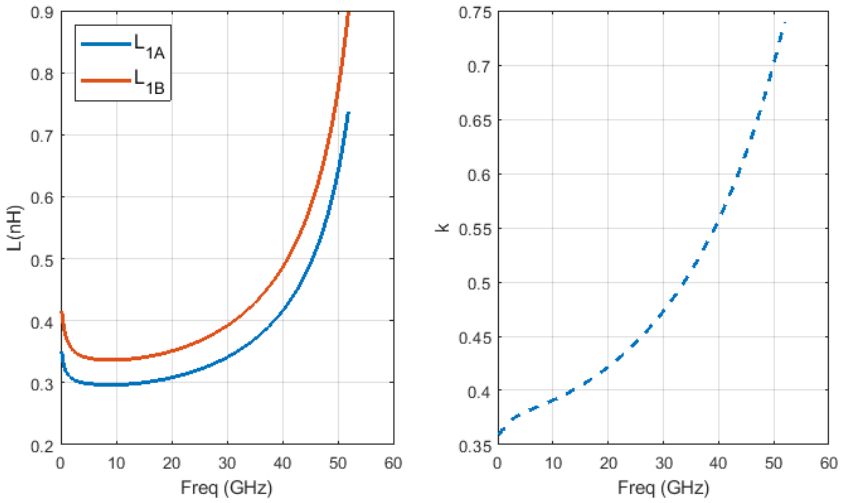


(a)

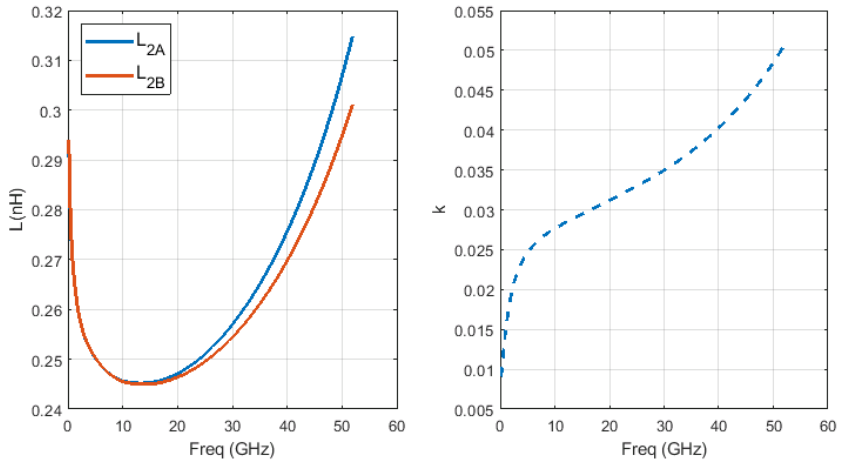


(b)

Figure 2.15: (a) Top view of physical implementation of the inductor, (b) lay out of the QVCO including resonant tanks and differential pairs.



(a)



(b)

Figure 2.16: Inductor and coupling coefficient of tank inductors: (a) L_{1A} and L_{1B}, (b) L_{2A} and L_{2B}

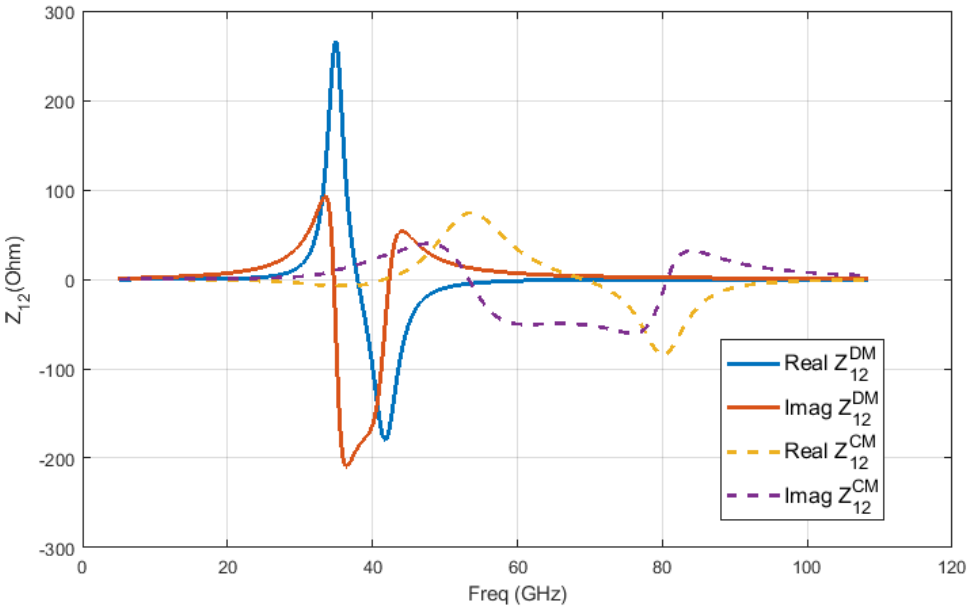


Figure 2.17: Transimpedance of the resonant tank in differential and common-mode

mode transimpedance has a peak at the second harmonic of the oscillation frequency, near 80 GHz.

The time-domain simulation results of the QVCO using EM simulation models are illustrated in Fig. 2.19. Some deviation from perfect quadrature is observed, which can be associated to asymmetry of the layout of two passive network seen in Fig. 2.15(b). By applying a DFT on the signals the phase of fundamental tones can be obtained as $(0°, 94°, 185°, 272°)$ for four output signals.

The waveforms of the signals show a compression at the low voltages which is due to the common-mode resonance at the second harmonics of output frequency [25]. This flat region of the waveform causes phase noise improvement since it corresponds to low values in ISF function. This is due to the fact that applying an current impulse during this period has less impact on the waveform crossing which is the definition of ISF.

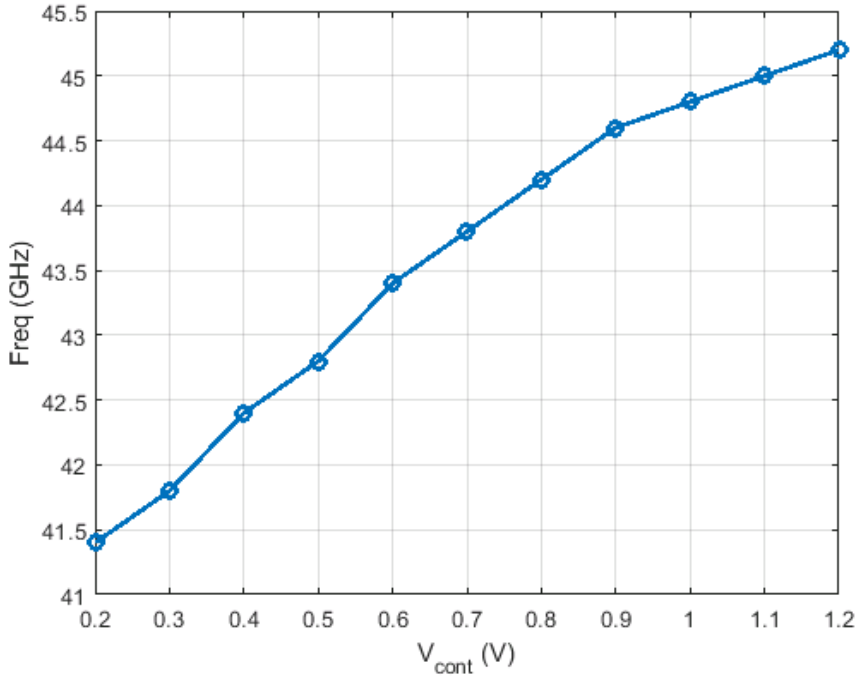


Figure 2.18: QVCO oscillation frequency with respect to control voltage

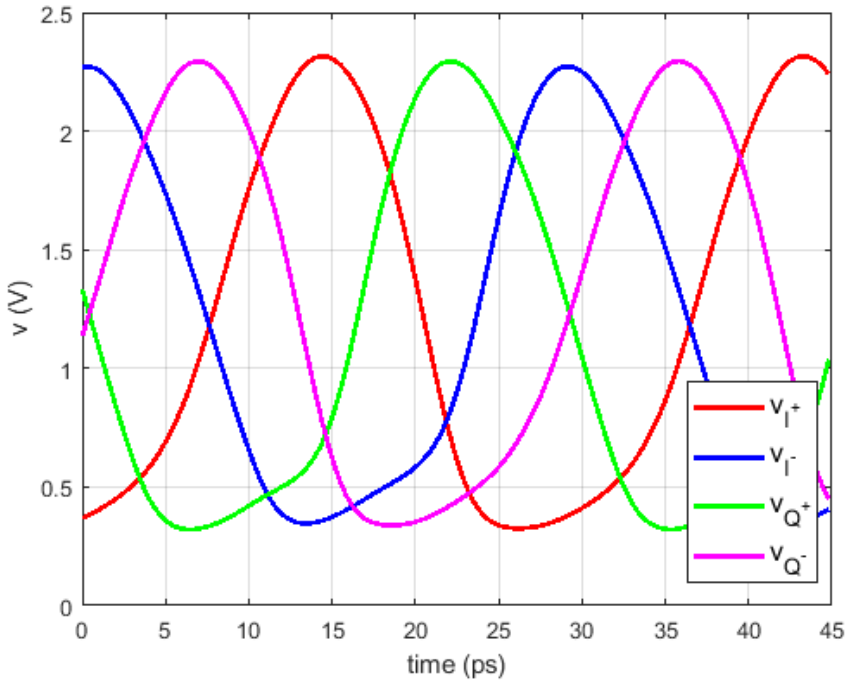


Figure 2.19: QVCO oscillation frequency with respect to control voltage

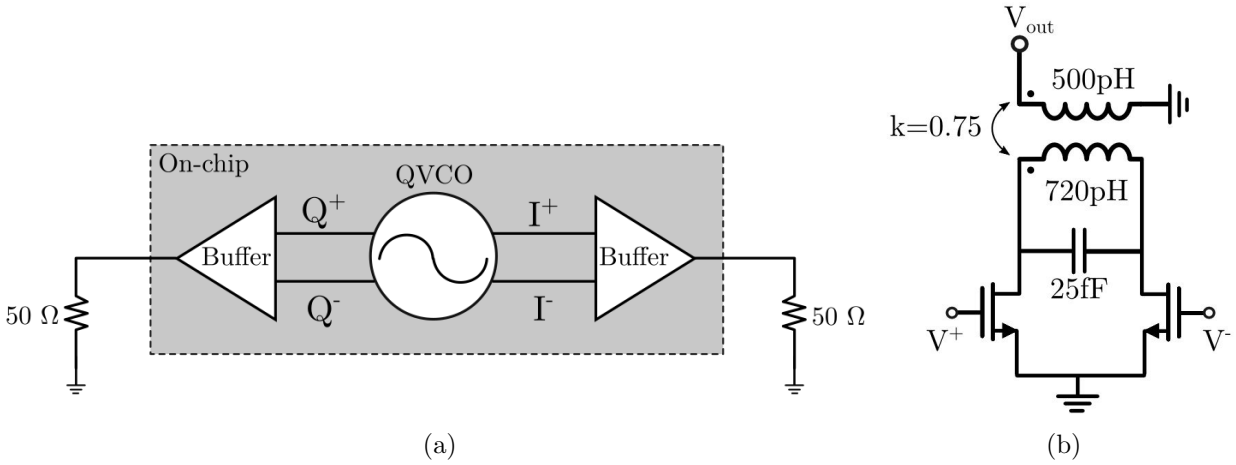


Figure 2.20: (a) Block diagram of QVCO with buffer stages to drive 50Ω load, (b) schematics of buffer stage

2.10 Buffer

In order to measure the quadrature output of the QVCO in the presence of an external 50Ω load terminal, a buffer stage is designed, as shown in Fig. 2.20(a). The buffer is composed of a common-source amplifier whose output is tuned to 40 GHz which is provided by a transformer and capacitor illustrated in Fig. 2.20(b). The transformer also converts the differential output of the QVCO into a single-ended signal that is connected to a GSG pad. Fig. 2.22 shows the QVCO die photograph including the QVCO , two buffers connected to output pads.

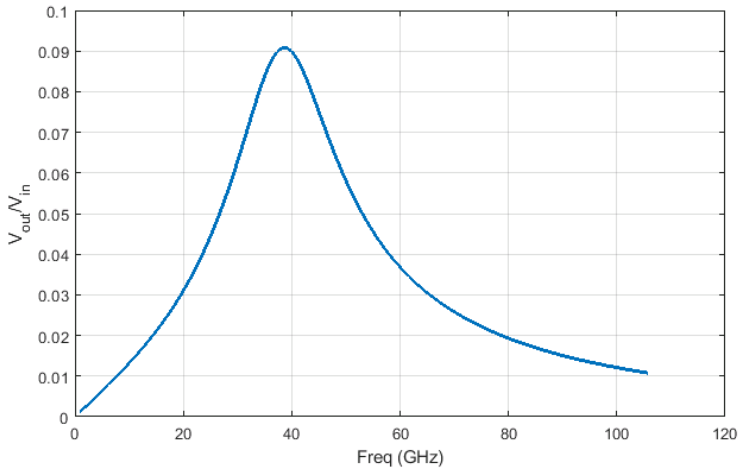


Figure 2.21: Voltage gain (V_{out}/V_{in}) of the buffer stage assuming 50Ω load at the output

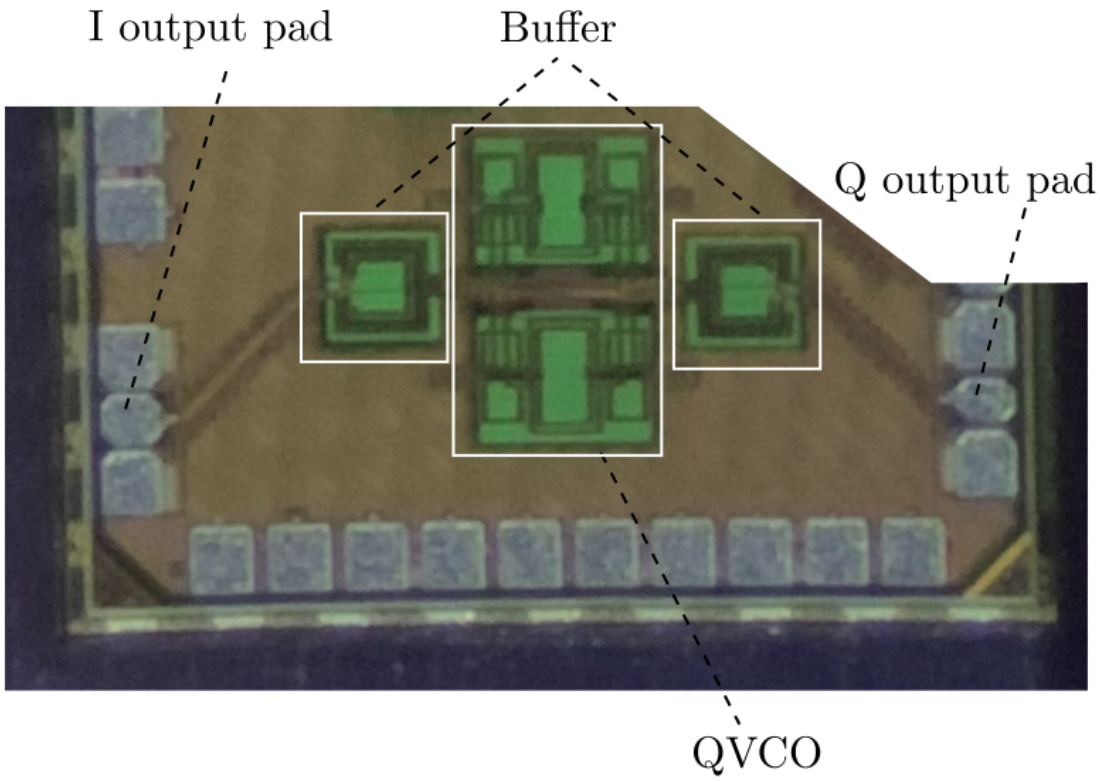


Figure 2.22: Die photograph of QVCO

Chapter 3

Wide Tuning range PLL Based on Multi-Port VCO

3.1 PLL Overview

The are numerous works in literature that describe high-performance mm-wave-range PLLs [27–33]. As mentioned before, a PLL is a negative feedback system that forces the divided VCO output phase to synchronize with the reference signal phase. In this chapter, we describe a PLL shown in Fig. 3.1. The VCO generates a signal with an output frequency that depends on the control voltage. It is assumed that this dependency is linear, i.e. the output frequency can be expressed as:

$$\omega_o = \omega_0 + K_{VCO} v_c \tag{3.1}$$

where v_c is the control voltage, ω_0 is the output frequency at $v_c = 0$, and K_{VCO} is a constant [34]. In addition to the control voltage, the proposed VCO has two switches to coarsely tune

the output frequency as described in next section.

The purpose of the buffer is to reduce the loading of the stages following the VCO output by providing an input impedance with a very large real part in order to maintain robust operation of the VCO. The buffer output is applied to two outputs that are impedance matched to the frequency divider and output pad.

The feedback path is composed of a cascade of frequency divider stages that realize a division ratio of 256. Therefore, the output of the divider can be expressed as:

$$\omega_{div} = \frac{1}{256}\,\omega_o \tag{3.2}$$

The first stage of the frequency divider chain, implemented as an injection-locked frequency divider (ILFD), includes a switch that controls the locking range in order to cover the full frequency band. The phase-frequency detector (PFD) and the charge pump are the blocks responsible to generate an output current that is proportional to the phase difference between the two PFD inputs. The output current of the charge pump can be expressed as:

$$i_{cp} = K_{PFD,CP}\,\Delta\phi \tag{3.3}$$

where $K_{PFD,CP}$ is a constant and $\Delta\phi$ is the phase difference between the reference signal and output of the frequency divider chain. The output current of the charge pump is applied to a low-pass filter (LPF) that eliminates the high-frequency components so that a relatively slowly varying control signal is delivered to the VCO. The output voltage of the LPF is given by:

$$v_c = i_{cp} Z_{LPF} \tag{3.4}$$

where Z_{LPF} is the impedance of the LPF.

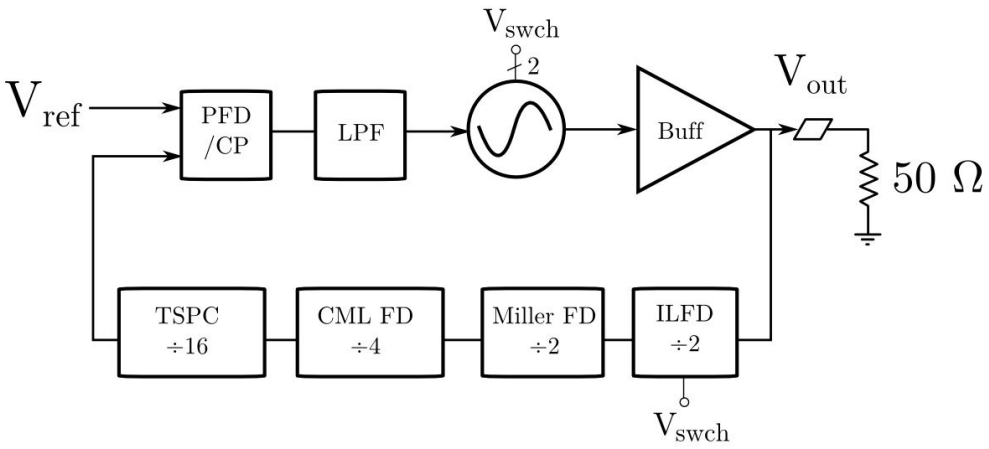


Figure 3.1: Block diagram of proposed PLL

As explained in Chapter 1, the VCO frequency can be fine-tuned by using a varactor and coarse-tuned by switching capacitor or inductor of the tank. Although simultaneous switching of the tank inductor and capacitor is advantageous, adding a series switch to an inductor has two important drawbacks: It directly affects the tank quality factor, and the parasitic capacitance of the switches is added to the tank capacitance, which limits the tuning range [35]. In particular, decreasing the switch resistance requires an increased transistor gate width, which further limits the frequency range. An alternative method to change the effective inductance is to insert the switch in series with a second loop that is mutually coupled to the tank inductor. The inductance of this loop can be used to resonate out the parasitic capacitances of the switches, so the switch size can be increased to reduce the loss.

Switching the tank inductor is completely feasible for a single loop, which leads to two states (ON/OFF). To achieve more tuning states, the number of loops must be increased, which leads to design complexity because of the mutual inductance between them. In this work, a novel VCO topology is employed to tune the frequency by changing the oscillation mode.

3.2 VCO Design

Fig. 3.2 shows the proposed VCO composed of a pair of cross-coupled transistors and a differential transistor pair connected to a resonant tank that includes a transformer with shunt capacitors connected to both windings. The admittance of each part is shown in the figure. The negative resistance part can be represented as a matrix with negative conductance $g_{m1}/2$ at one port and zero conductance at the other port. The coupling factor k between the primary and secondary windings of the transformer can take either positive or negative value depending on the geometry. However, in the next section a technique to change the value of k for a fixed geometry is explained.

To study the oscillation modes, multi-port oscillation theory is used. The admittance matrices of the tank, cross-coupled pair, and differential pair are presented in Fig. 3.2. The elements of the tank admittance matrix are given by:

$$Y_i = j\omega C_i + \frac{1}{j\omega L_i(1-k^2)}\Big[1 + \frac{j}{Q}\frac{1+k^2}{1-k^2}\Big],\ i = 1, 2 \tag{3.5}$$

$$Y_3 = \frac{k}{j\omega\sqrt{L_1 L_2}(1-k^2)}\Big[1 + \frac{j}{Q}\frac{1}{1-k^2}\Big] \tag{3.6}$$

The total admittance matrix of the VCO can be expressed as:

$$Y_{tot} = \begin{bmatrix} Y_1 - g_{m1}/2 & Y_3 + g_{m3}/2 \\ Y_3 & Y_2 \end{bmatrix} \tag{3.7}$$

The oscillation condition is given by:

$$\det(Y_{tot}) = (Y_1 - g_{m1}/2)Y_2 - (Y_3 + g_{m3}/2)Y_3 = 0 \tag{3.8}$$

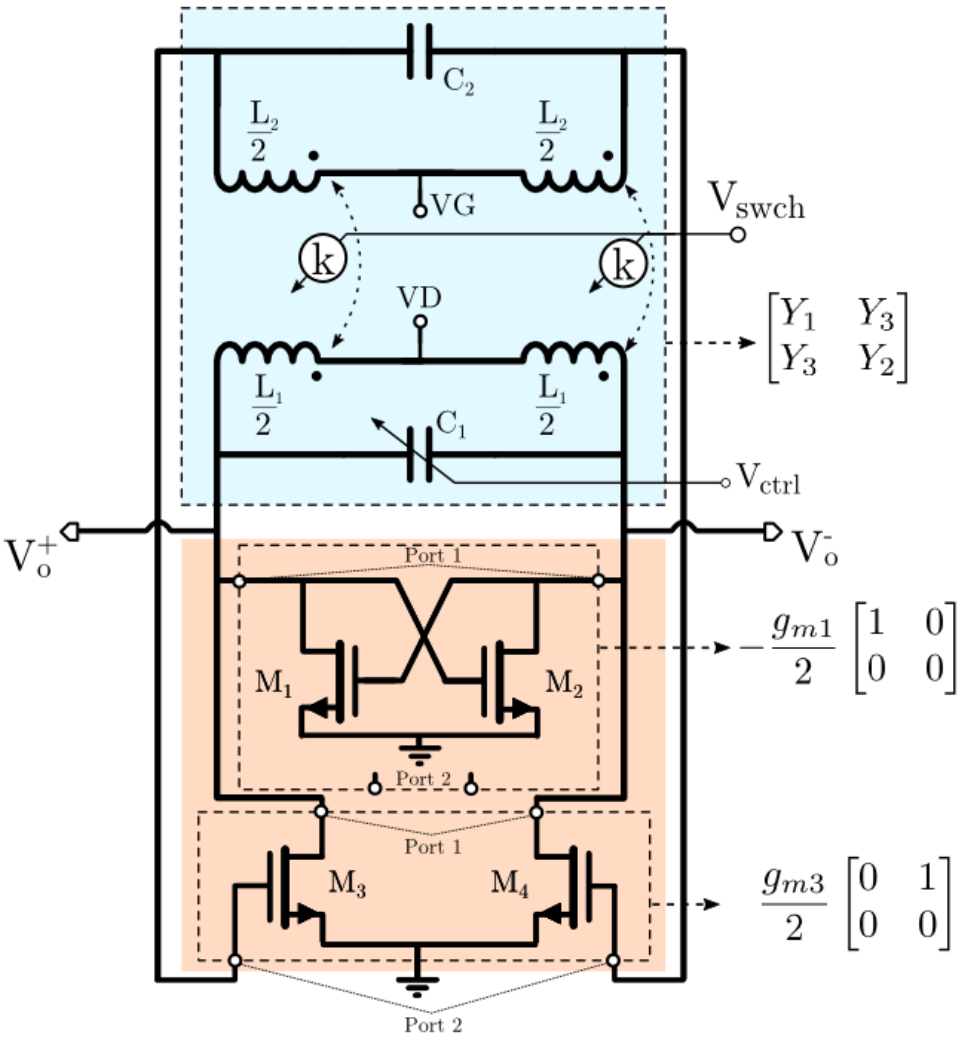


Figure 3.2: Block diagram of the proposed QVCO

Solving (3.8) for g_{m1} leads to:

$$\frac{g_{m1}}{2} = \frac{Y_1 Y_2 - Y_3(Y_3 + g_{m3}/2)}{Y_2} \equiv \frac{1}{Z'_{11}} \tag{3.9}$$

Since g_{m1} is assumed to be a real positive number, the oscillation frequency, ω_o, is determined by setting the imaginary part of the right-hand side of (3.9) to zero. At this frequency, the real part of g_{m1} indicates the minimum transconductance required for oscillation. The contour plots in Fig. 3.3 show minimum g_{m1} required for oscillation as a function of g_{m3} and k. The blank region represents the ranges of k and g_{m3} for which oscillation occurs even without the cross-coupled transistors. On the other hand, for $k = 0$ a relatively large g_{m1} is needed independent of g_{m3}. Under this condition the oscillator behaves more like a regular LC VCO as k goes to zero. As k increases a smaller value of g_{m1} is needed for oscillation for a given g_{m3} value. As mentioned earlier, each point on Fig. 3.3 corresponds to a different oscillation frequency; thus by varying k the oscillation frequency can be adjusted. In the following, the oscillation behavior two cases – $k = 0$ and $k \neq 0$ – is analyzed..

For $k = 0$, the coupling between ports 1 and 2 vanishes, making $Y_3 = 0$, which leads to a simple LC tank with $g_{m1} = 2Y_1$. Therefore $\omega_o = 1/\sqrt{L_1 C_1}$, and the minimum transconductance is $g_{m1,min} = 2(\omega_O L_1 Q)^{-1}$.

For $k \neq 0$, the oscillation frequency is obtained by equating the imaginary part of (3.9), which gives:

$$\omega_o = \sqrt{\frac{C_1 L_1 + C_2 L_2 \pm \sigma}{2 L_1 L_2 C_1 C_2 (1 - k^2)}} \tag{3.10}$$

where the Q of the inductors is assumed to be high and σ is given by:

$$\sigma = \sqrt{(C_1 L_1 - C_2 L_2)^2 + 4 C_1 C_2 L_1 L_2 k^2} \tag{3.11}$$

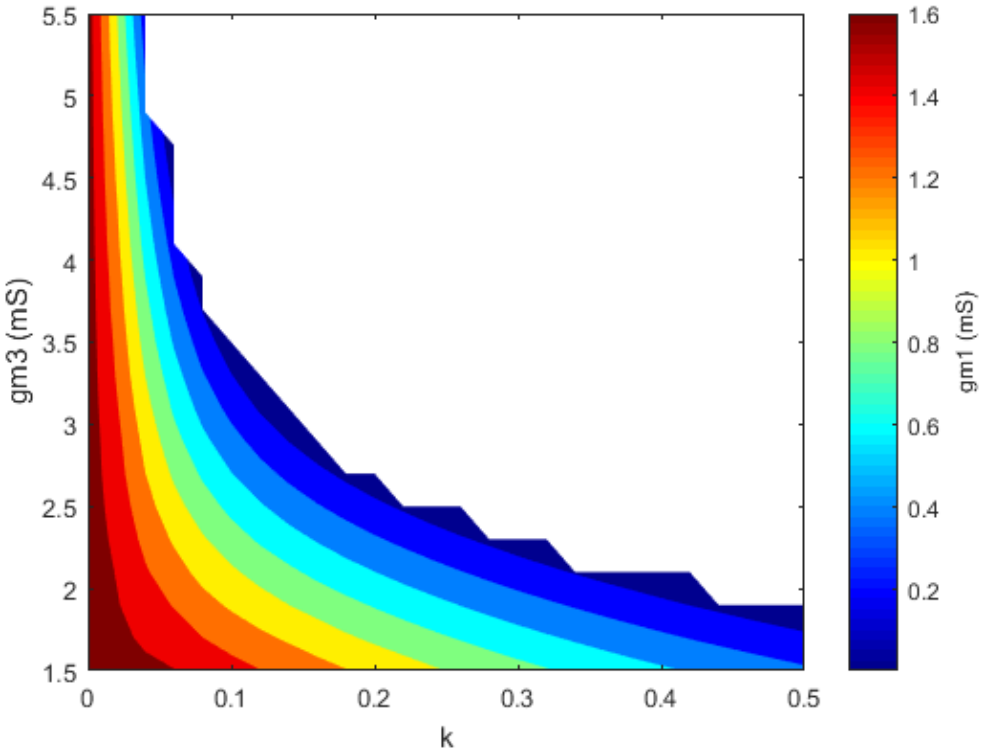


Figure 3.3: Contour plot of g_{m1} needed for oscillation versus g_{m1} and k.

If we set $L_1C_1 = L_2C_2 = LC$ then (3.10) simplifies to:

$$\omega_o = \frac{1}{\sqrt{LC(1 \pm k)}} \tag{3.12}$$

As per (3.9), Fig. 3.4 shows the real and imaginary parts of Z'_{11} for different values of k. It can be seen that the zero-crossing of imaginary part, representing oscillation frequency, changes as k varies. Moreover, the magnitude of the real part decreases with k. For $k = -0.2$ the imaginary part of Z'_{11} exhibits multiple zero crossings so that the oscillation eventually occurs at the resonant frequency for which the real part has the largest peak.

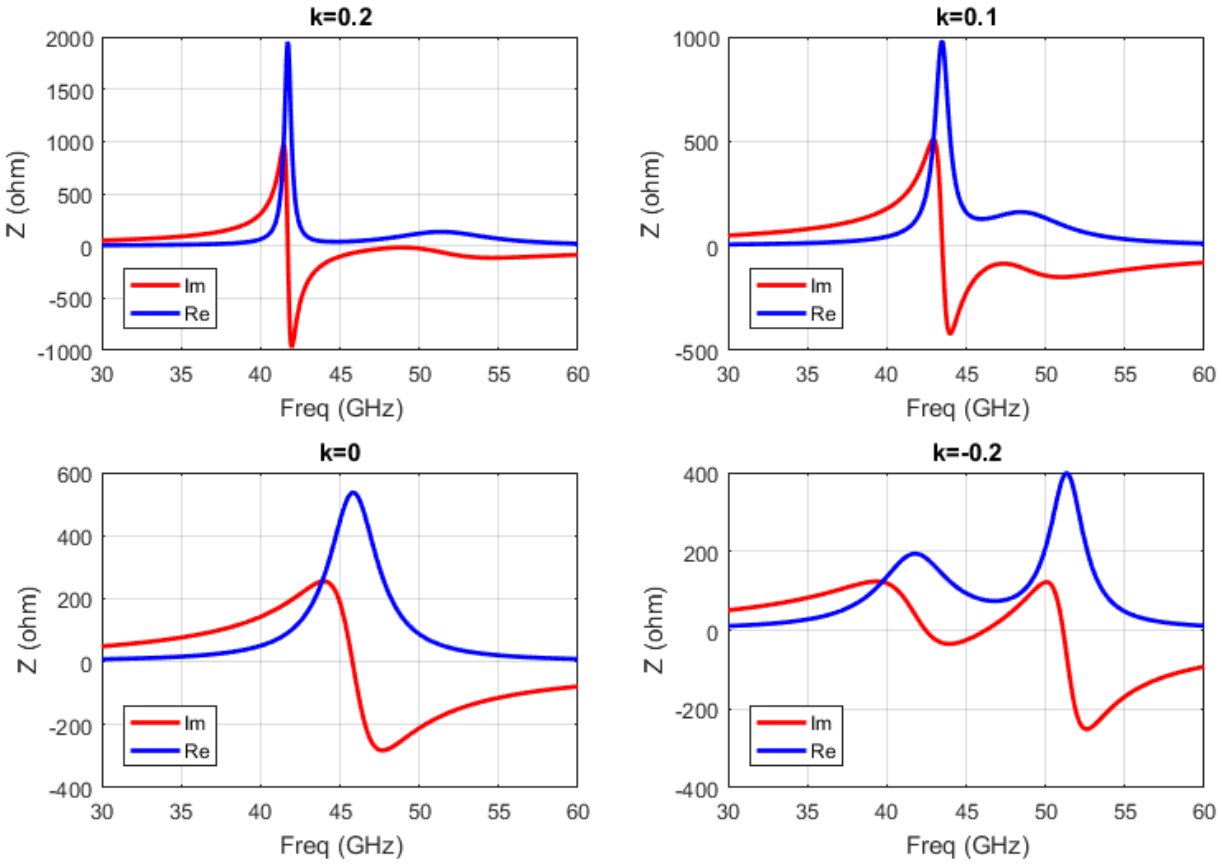


Figure 3.4: Imaginary and real part of Z'_{11} for different k, $L_1 = L_2 = 150pH$, $C_1 = C_2 = 80fF$, $Q = 10$ and $g_{m1} = 2.5mS$.

3.2.1 Variable-Coupling Transformer Design

The coupling coefficient k of two inductors is proportional to the mutual magnetic flux that is generated by the primary loop and passes through a the secondary loop; the sign of k depends on the relative orientation of the windings. Therefore, k can be adjusted by changing the mutual magnetic flux of inductors. This can be done by adding an overlapping loop that shorts the induced current and reduces the effective mutual magnetic flux, which leads to the reduction of the coupling coefficient of inductors [16, 18, 36, 37].

Fig. 3.5(a) shows a 3D view of a transformer that consists of a primary loop, a bow-tie shaped secondary loop, and two floating rings. Ports 1 and 2 are defined differentially at the primary and secondary terminals, respectively. The primary and secondary loops are implemented in metal (M9) to minimize the loss whereas the floating rings are implemented in metal (M7), with two FET switches added to open or short them. As shown, due to the direction of the currents, the mutual flux passing through two halves of inductors have opposite signs. Therefore, the net flux passing through the primary generated by the magnetic field of the secondary is zero, leading to zero coupling. By closing the FET switches the floating rings form a loop that provides a conducting path for the induced current. This induced current neutralizes the portion of magnetic flux passing through the loop, resulting in a non-zero net flux in the transformer, as shown in Fig. 3.5(c). It should be noted that the direction of the remaining magnetic field in the two cases have opposite directions which leads to different signs for k.

The equivalent circuit of the transformer is illustrated in Fig. 3.6(a). It consists of primary and secondary connected to the output ports with inductances L_i and L_o, respectively. Moreover, there are two non-overlapping floating loops with inductances of L_A and L_B connected to two NMOS switches. Every possible coupling coefficient between all four of these inductors is shown. It is expected that the value of k' is relatively small as loops A

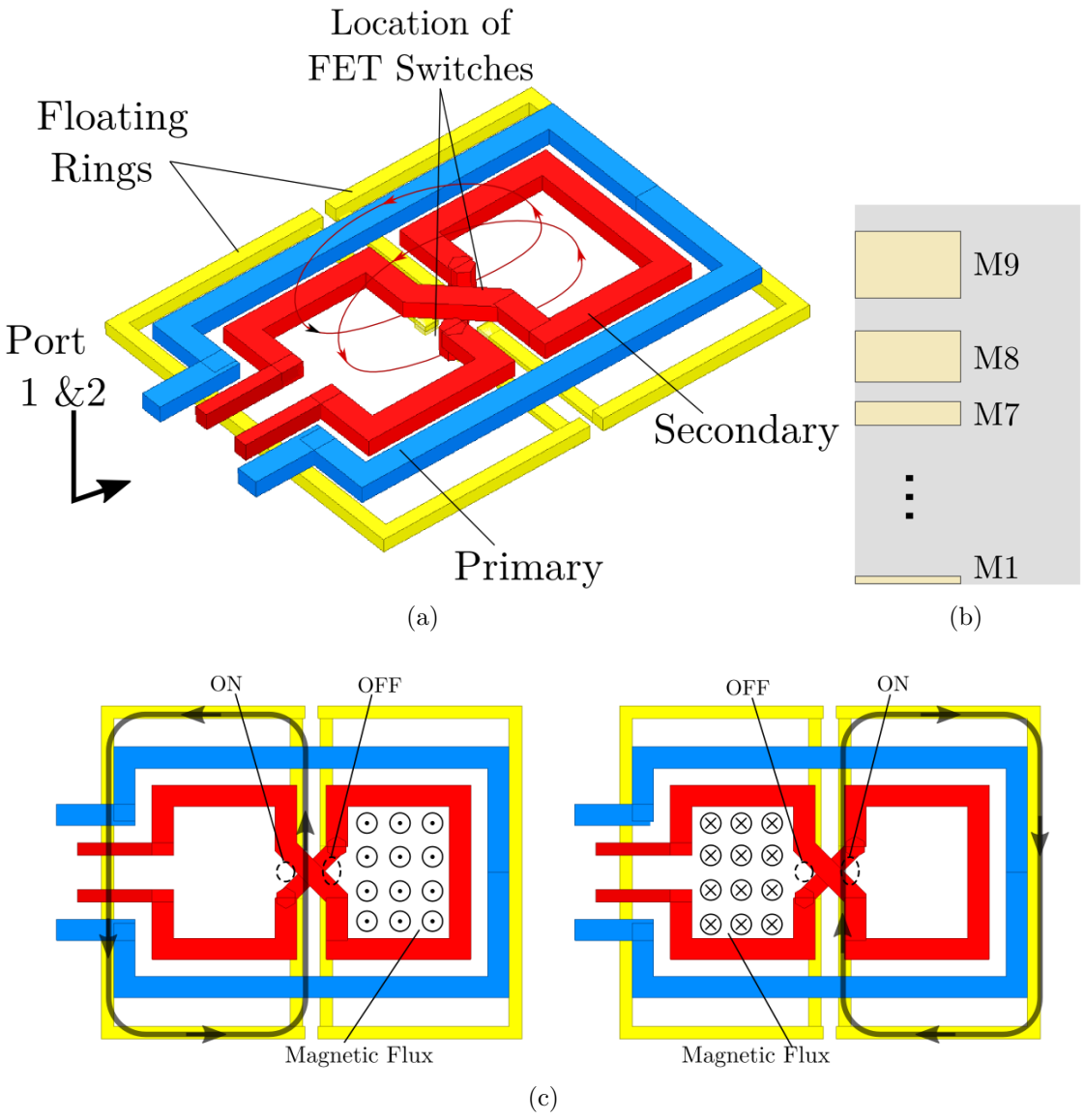


Figure 3.5: (a) 3D model of the transformer with floating ring and the magnetic flux direction, (b) stack-up of the CMOS technology, (c) magnetic flux and current direction in the floating rings for two states of switches

and B are not overlapping. Moreover, k_{12}, as the net mutual magnetic flux between primary and secondary loops, is assumed to be negligible. The transformer geometry is designed to have equal coupling between the main loops and the floating loops k_p, as shown in Fig. 3.6. Moreover, the floating rings are the same size so $L_A = L_B = L_p$. The impedance matrix of the 4-port inductor network is given by:

$$\mathbf{Z} = j\omega \left[\begin{array}{cc|cc} L_i & 0 & k_p L_{ip} & -k_p L_{ip} \\ 0 & L_o & k_p L_{op} & k_p L_{op} \\ \hline k_p L_{ip} & k_p L_{op} & L_p & k' L_p \\ -k_p L_{ip} & k_p L_{op} & k' L_p & L_p \end{array}\right] = \begin{bmatrix} \mathbf{Z_{11}} & \mathbf{Z_{12}} \\ \mathbf{Z_{21}} & \mathbf{Z_{22}} \end{bmatrix} \tag{3.13}$$

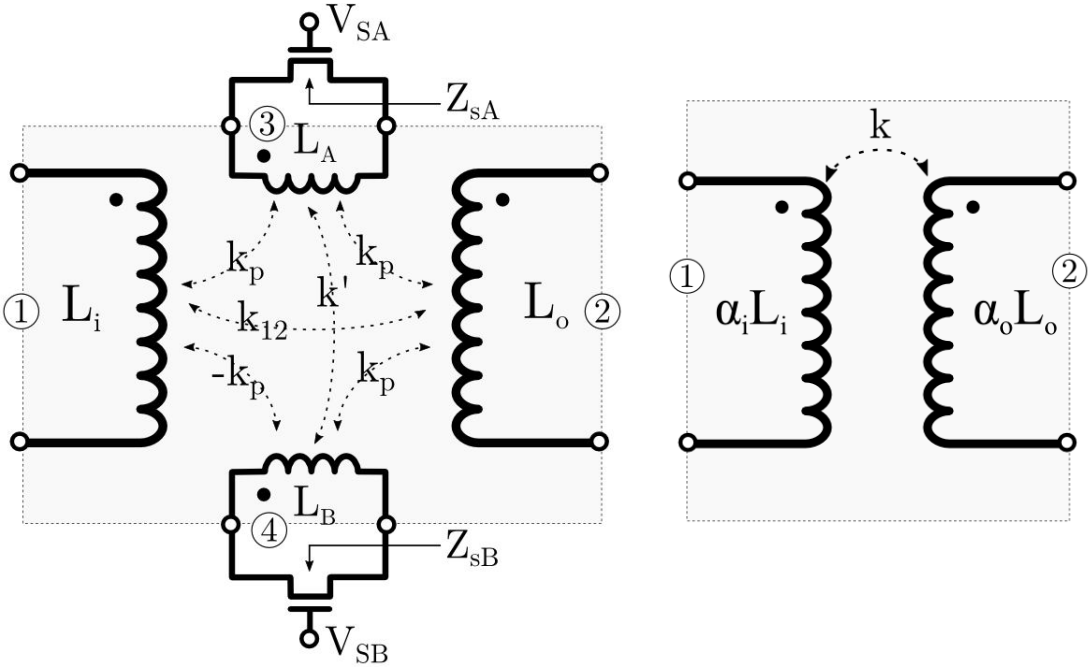
where $L_{op} = \sqrt{L_o L_p}$ and $L_{ip} = \sqrt{L_i L_p}$; and $\mathbf{Z_{11}}$, $\mathbf{Z_{12}}$, $\mathbf{Z_{21}}$ and $\mathbf{Z_{22}}$ are the impedance submatrices. Moreover, it is assumed that $k_{12} = 0$.

Fig. 3.7 shows the simulated parameters of the transformer network as a function of frequency. The coupling between both floating rings and primary and secondary are assumed to be k_p. Quality factor of primary and secondary are above 15 whereas the Q of the ring is around 12. It will be shown that if FET switches assumed to be ideal, i.e. $R_{ON} = 0$ and $R_{OFF} = \infty$, the network can be modelled by a transformer as shown in Fig. 3.6(b).

The impedance matrix of the equivalent circuit can be expressed as:

$$\mathbf{Z}_{io} = \mathbf{Z}_{11} + \mathbf{Z}_{12}(\mathbf{Z}_L + \mathbf{Z}_{22})^{-1}\mathbf{Z}_{21} \tag{3.14}$$

where $\mathbf{Z_L} = \mathrm{diag}(Z_{sA}, Z_{sB})$, and Z_{sA} and Z_{sB} are impedances of the switches connected to loops A and B, respectively. For ideal switches, Z_L can be calculated for the four switch states. If one of switch is ON and the other is OFF, the impedance matrix can be expressed



(a) (b)

Figure 3.6: (a) Transformer equivalent circuit with floating rings and CMOS switches controlled by V_{SB} and V_{SA}, (b) Equivalent circuit of transformer where values of α_i, α_o and k are all presented in table 3.1 for 4 combinations of switch status.

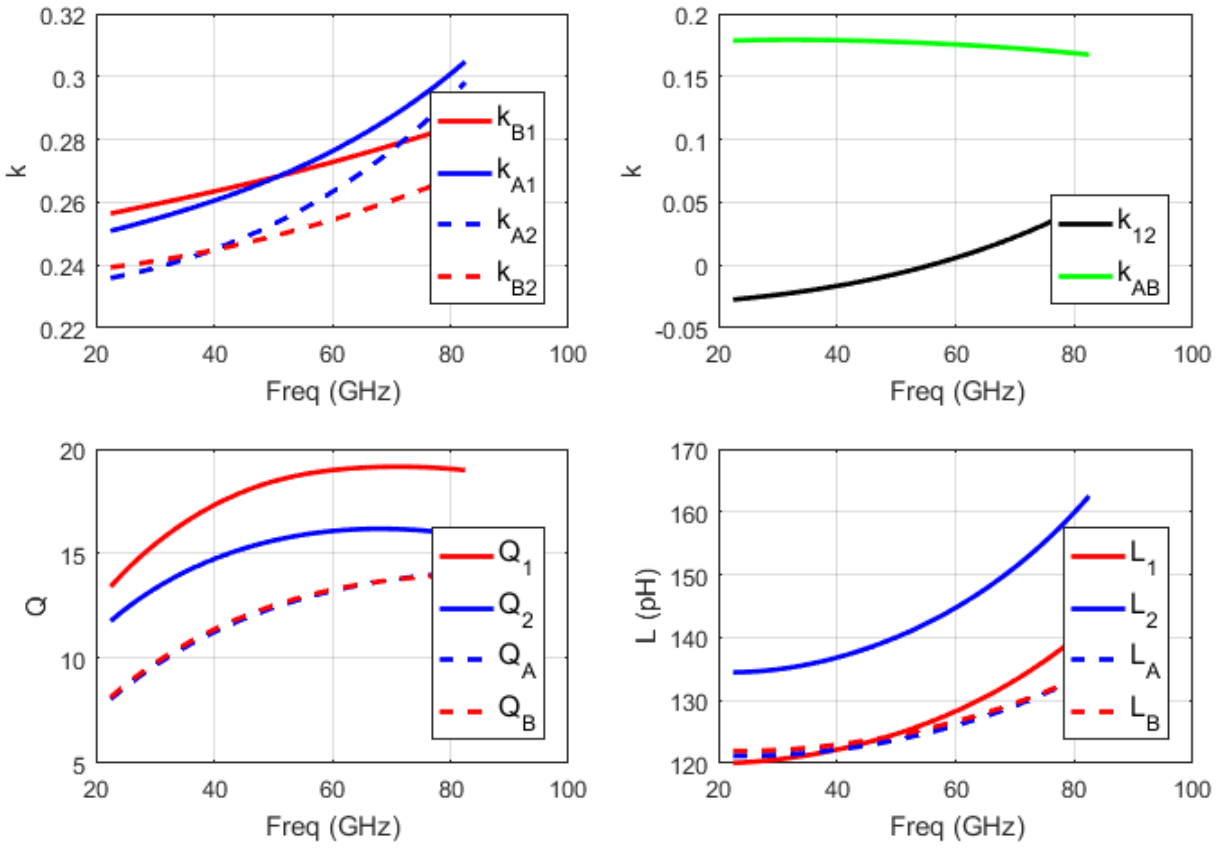


Figure 3.7: Transformer parameters including (a) coupling coefficient between main and floating loops, (b) coupling coefficient between loop main loops k_{12} and between floating rings K_{AB}, (c) Quality factor of the main loops and floating rings, (d) inductance of the main loops and floating rings calculated from full-wave EM simulation

Table 3.1: Equivalent inductor parameters for different switch states

	OFF/OFF	OFF/ON	ON/OFF	ON/ON
α_i	1	$1+k_p^2$	$1+k_p^2$	$1+\frac{2k'^2}{1-k'}$
α_o	1	$1+k_p^2$	$1+k_p^2$	$1+\frac{2k'^2}{1+k'}$
k	0	$-\frac{k_p^2}{1+k_p^2}$	$+\frac{k_p^2}{1+k_p^2}$	0
ω_{osc}	$\frac{1}{\sqrt{L_iC_1}}$	(3.10)	(3.10)	$\frac{1}{\sqrt{L_iC_1\alpha_i}}$

as:

$$\mathbf{Z}_{io} = j\omega \begin{bmatrix} L_i(1+k_p^2) & \pm\sqrt{L_iL_o}k_p^2 \\ \pm\sqrt{L_iL_o}k_p^2 & L_o(1+k_p^2) \end{bmatrix} \tag{3.15}$$

in which the sign determined by choice of switches to be ON. This leads to a transformer with inductor primary and secondary inductor multiplied by $\alpha_i = \alpha_o = 1+k_p^2$. The effective coupling coefficient is also $k = \pm k_p^2/(1+k_p^2)$. When both switches are OFF, the transformer is obviously equivalent to two uncoupled inductors, i.e.,

$$\mathbf{Z}_{io} = j\omega \begin{bmatrix} L_i & 0 \\ 0 & L_o \end{bmatrix} \tag{3.16}$$

Finally, when both switches are ON , we have:

$$\mathbf{Z}_{io} = j\omega \begin{bmatrix} L_i(1+\frac{2k'^2}{1-k'}) & 0 \\ 0 & L_o(1+\frac{2k'^2}{1+k'}) \end{bmatrix} \tag{3.17}$$

Table 3.1 summarizes the parameters of the equivalent circuit of switched transformer for the four switch states. For non-ideal switches the Z_{sA} and Z_{sB} must be replaced by the actual switch impedances in (3.14), which leads to degradation of the overall Q of the transformer.

The switches are realized by NMOS transistors with deep n-well in which the body is floated

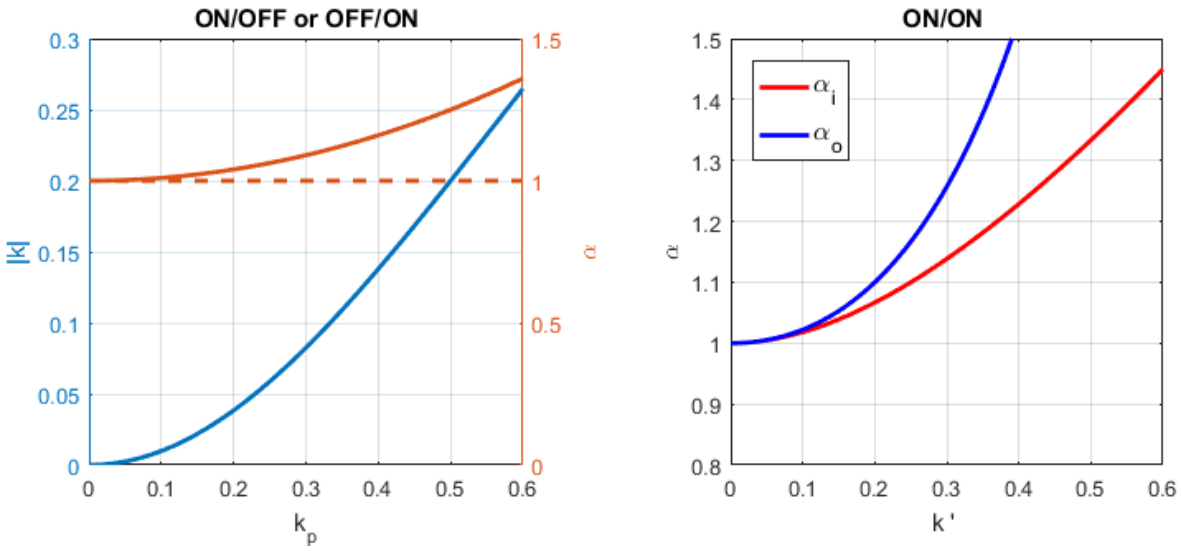


Figure 3.8: Parameters of equivalent transformer defined in Table 3.1

to reduce leakage and capacitance to the substrate. Switches are sized to minimize their ON resistance, R_{ON}, and their parasitic capacitances resonate out with the floating ring inductance when they are OFF. Therefore, the maximum size of the switches are limited by the inductance of the ring and oscillation frequency.

3.2.2 Frequency Sweeping

In the proposed VCO the fine frequency tuning is realized by the varactor C_1 , shown in Fig. 3.2, while coarse tuning is performed by varying the coupling coefficient of the transformer. As explained, each of the four switch states results in a different oscillation frequency as presented in Table 3.1.

There are two capacitors at the input C_1 and output C_2 of the transformer tank. C_2 is realized as a constant finger capacitor, while C_1 is implemented by a varactor because it impacts the oscillation frequency for all 4 modes.

By varying the varactor's control voltage from 0 to VDD a range of oscillation frequencies

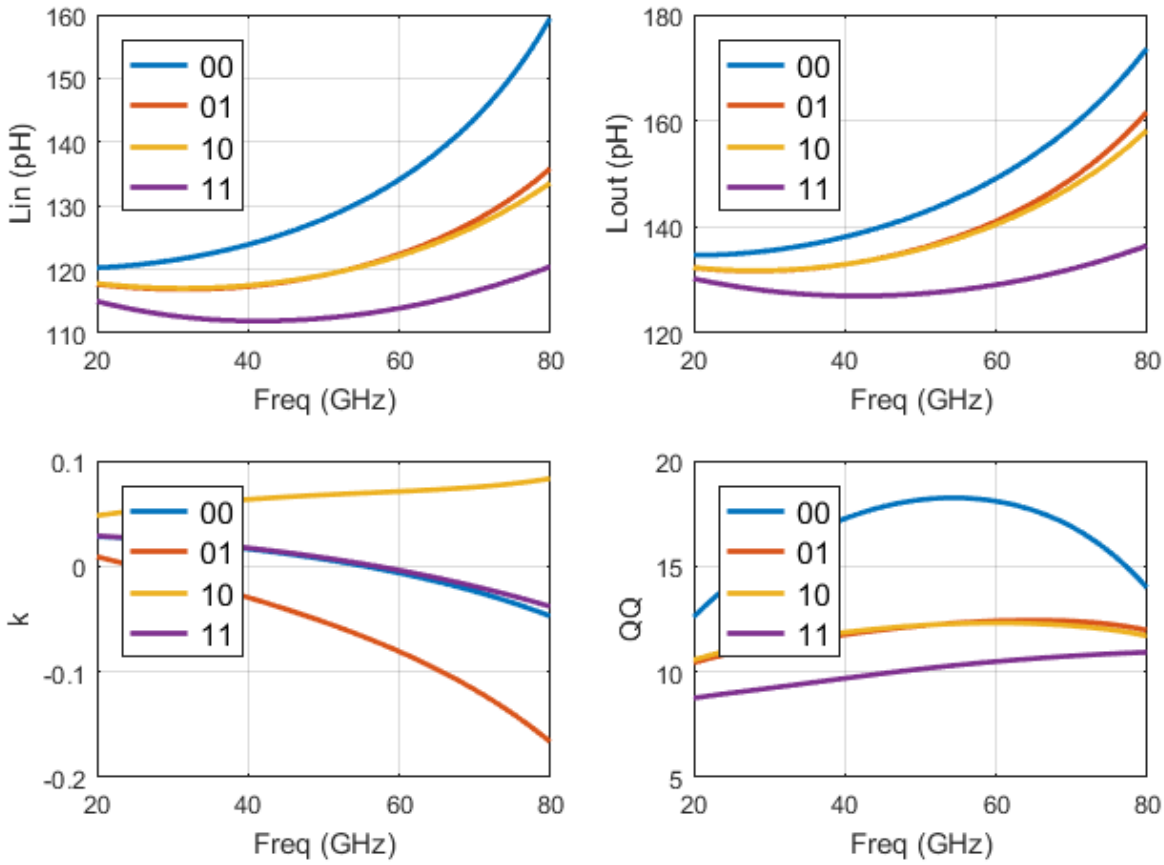


Figure 3.9: Effective parameters of the equivalent transformer

Table 3.2: VCO design parameters

L_1	150pH	$(W/L)_1$	14μm/60nm
L_2	150pH	$(W/L)_2$	14μm/60nm
C_1	80fF	$(W/L)_3$	14μm/60nm
C_2	80fF	$(W/L)_4$	14μm/60nm
k	0.15		

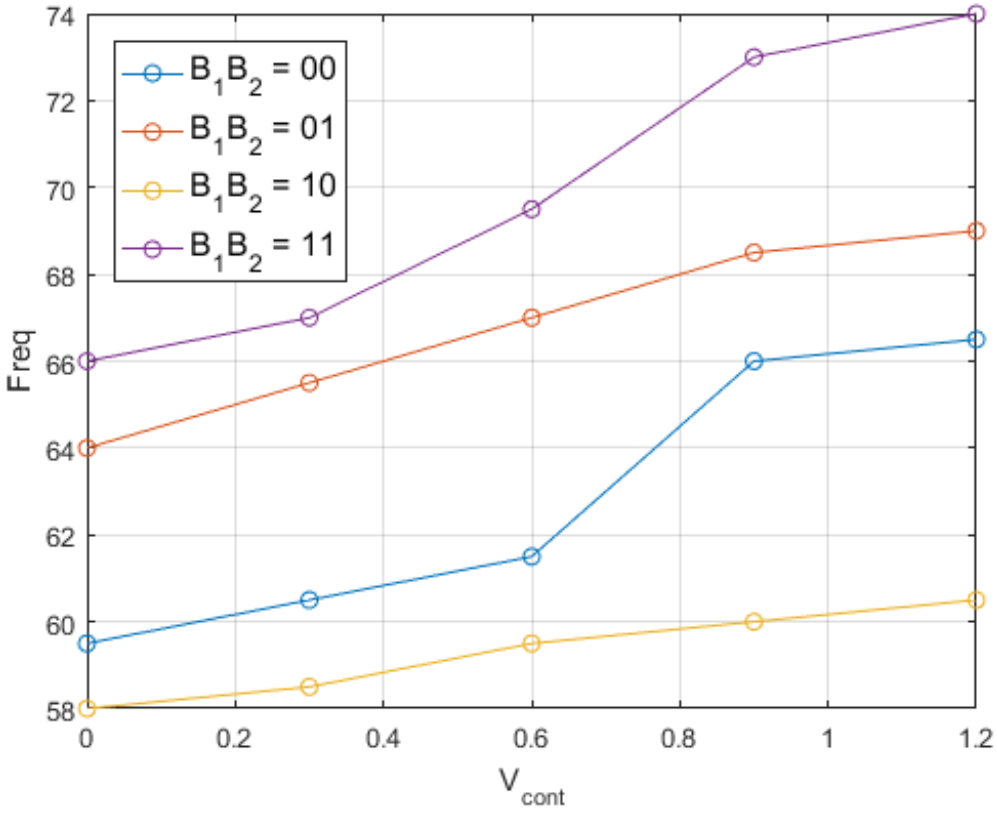


Figure 3.10: Transformer equivalent circuit

is realized, which depends on the switch states, as shown Fig. 3.10. The design parameters are chosen carefully so that these bands cover frequencies from 58 GHz to 74 GHz.

3.3 Buffer Design

Fig. 3.11 shows the schematic of the buffer that is realized as a cascode stage followed by a common drain. The input and output matching is provided by transformers.

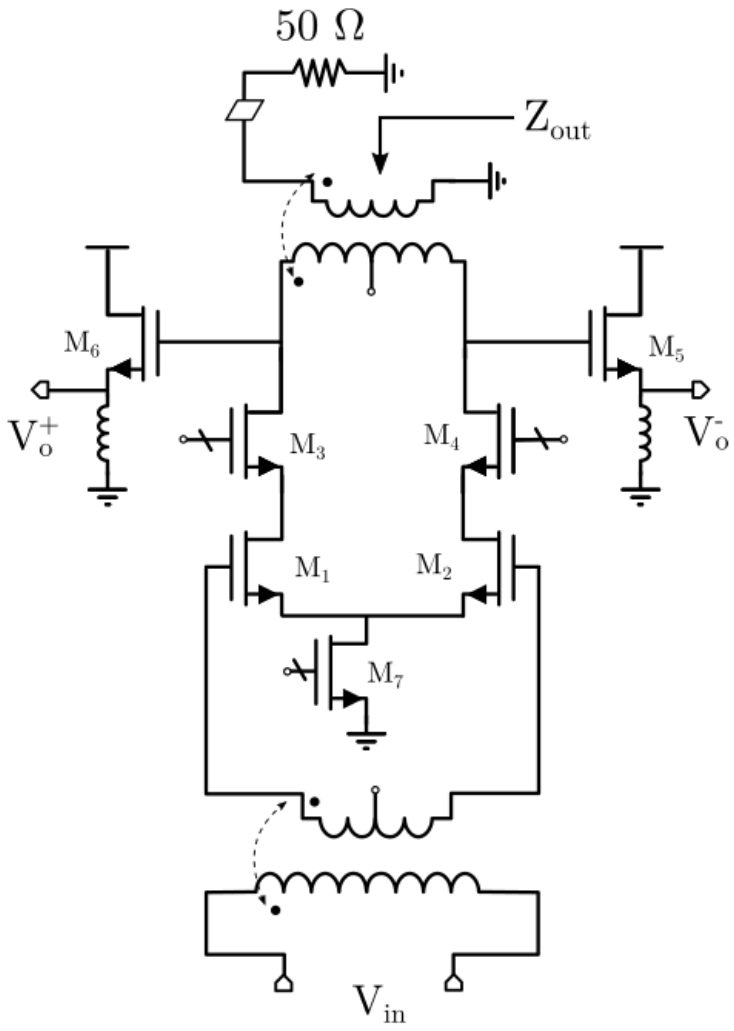
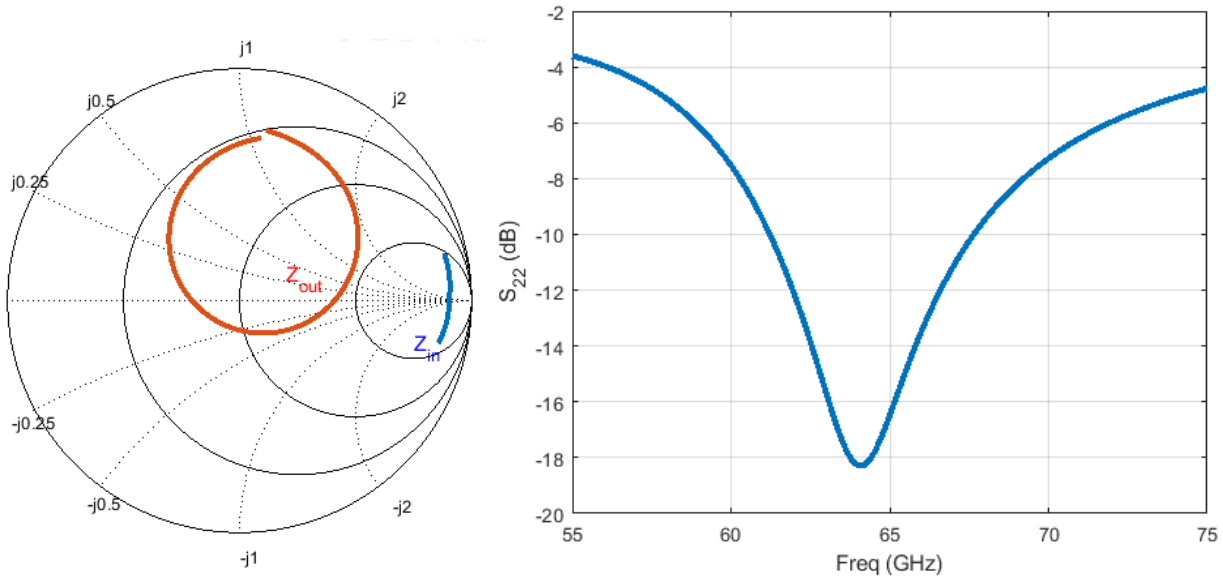


Figure 3.11: buffer schematic



(a) (b)

Figure 3.12: (a) Impedance seen from input and output ports, (b) S-parameter of output port

The input transformer is used to provide a high input impedance to minimize the loading on the VCO as well as the biasing of the second stage. Ideally this impedance should be purely resistive over the frequency band to avoid the impacting the resonance frequency of the tank. A cascode topology is chosen, which helps to achieve better broadband matching since the impedance at the drains of M1 and M2 is resistive and small. The input capacitance seen at the gates of M1 and M2 is $C_{gs} = 38fF$. The input transformer is designed in such a way that the input impedance to the buffer Z_{in} is near $1K\Omega$, as shown in 3.12(a).

The buffer has two outputs: the first one feeds external load $R_L = 50\Omega$, and the second one is connected to a frequency divider. The output of the cascode is connected to the load through a transformer that provides the matching to 50Ω. The center tap of the primary winding provides the bias of the drain. The other output of the buffer, which drives the divider, includes a source-follower stage with inductor at the source. It should be noted that two inductors shown in Fig. 3.11 are laid out as a differential inductor with center tap connected to ground.

3.4 Frequency Dividers

The divider chain is composed of 8 cascaded stages of divide-by-2 frequency dividers. The design of the first two divider stages to meet the wide locking range at high frequency is challenging. The first stage a direct injection-locked frequency divider [38] with differential input and outputs shown in Fig. (3.15), is essentially a cross-coupled LC oscillator tuned near half the frequency of main oscillator. The differential inputs are connected to the gates of NMOS and PMOS pairs, which directly injects the current to the output nodes. The inputs are DC decoupled with large capacitors to ensure that transistors M4 and M5 are biased in saturation, with $V_{bn} = 0.8V$ and $V_{bn} = 0.4V$. This configuration generally provides wider locking range compared to the classical injection-locked frequency divider [39], which the input signal is applied to the tail current. To cover the full tuning range of the main oscillator a capacitor switch (M_6) is added to tune the resonant frequency of the divider tank controlled by V_{s1}. Fig. 3.14 shows the simulation results of the divider output amplitude as a function of input frequency for different input voltage amplitudes under two switch states.

The second frequency divider stage is implemented as a Miller frequency divider in order to provide a wide frequency range [40].

The last 4 four frequency divider stages are implemented as True Single Phase Clock (TSPC) circuit [41, 42] as shown in Fig. 3.17.

3.5 PFD, Charge Pump and LPF

The most common form of phase detector is the phase-frequency detector, shown in Fig. 3.18, which has two inputs and two outputs [43], [44]. It is composed of two SR latches set by the inputs and their reset is fed back from the outputs. In order to adjust the delay

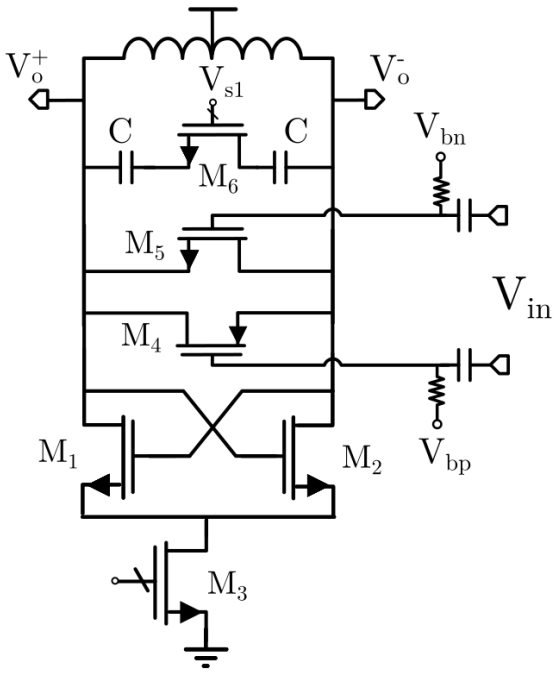


Figure 3.13: First frequency divider stage realized as a direct injection locked frequency divider

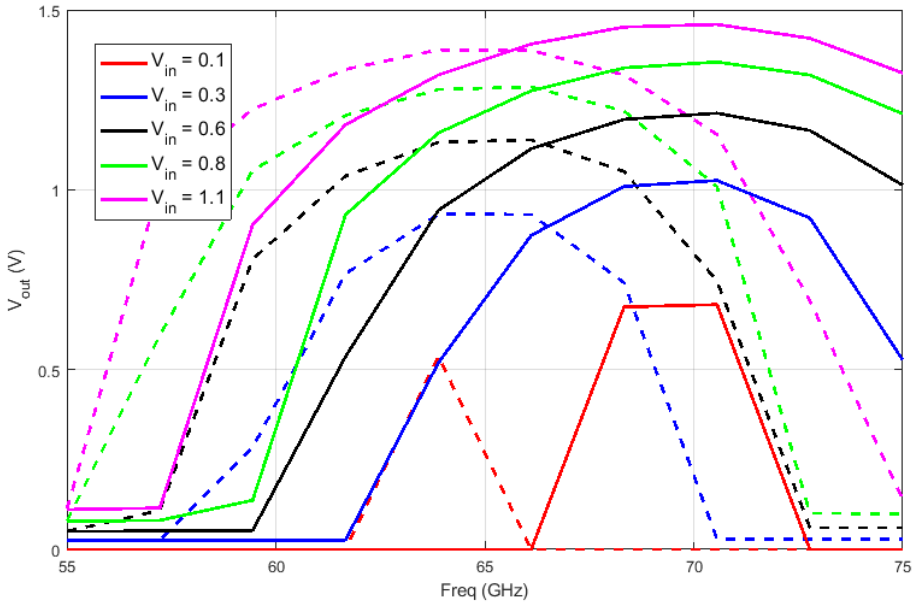


Figure 3.14: Output of first stage frequency divider over the frequency range for different input amplitude. Solid line is for $V_{s1} = 0$ and dashed line is for $V_{s1} = 1$.

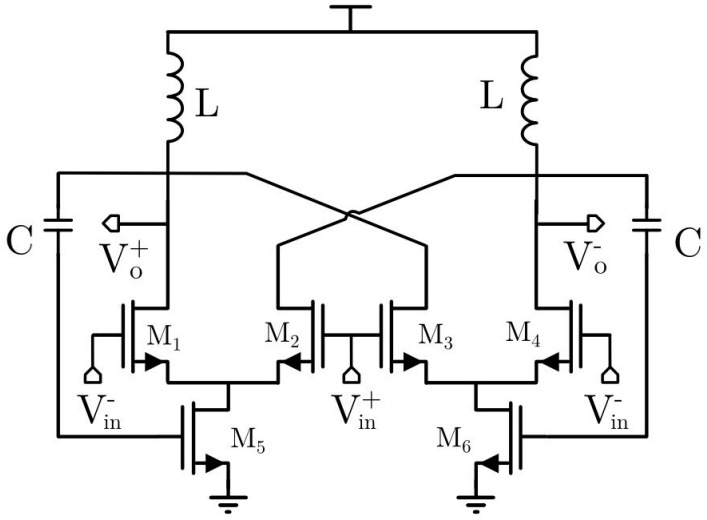


Figure 3.15: Second frequency divider stage realized as Miller frequency divider

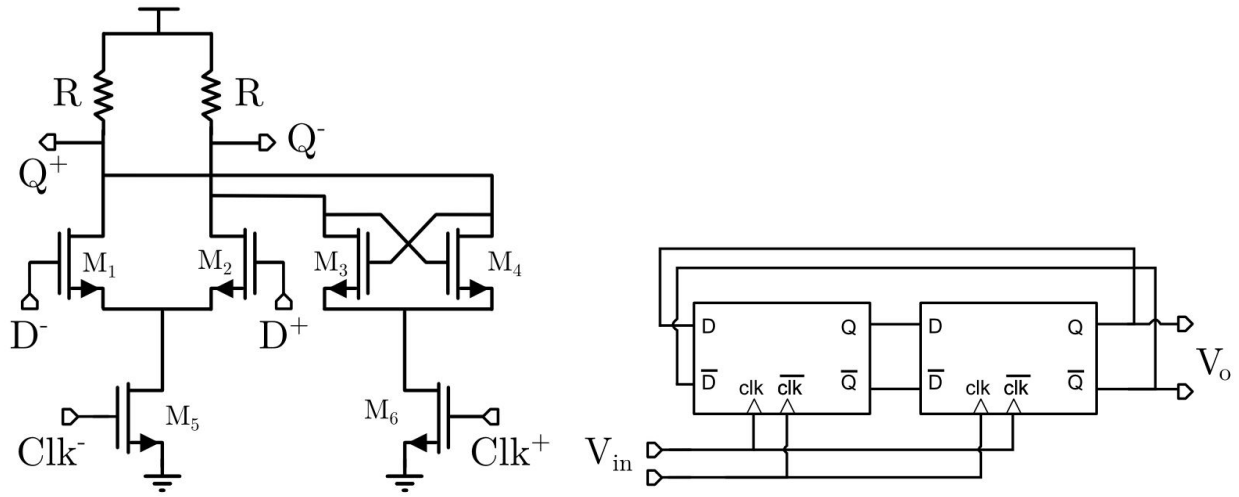


Figure 3.16: (a) CML latch, (b) flip-flop implemented by two CML latches configured as a frequency divider

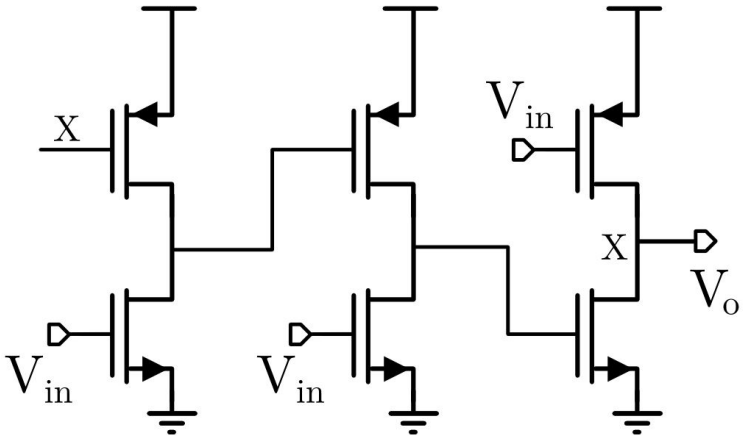


Figure 3.17: Static logic frequency divider

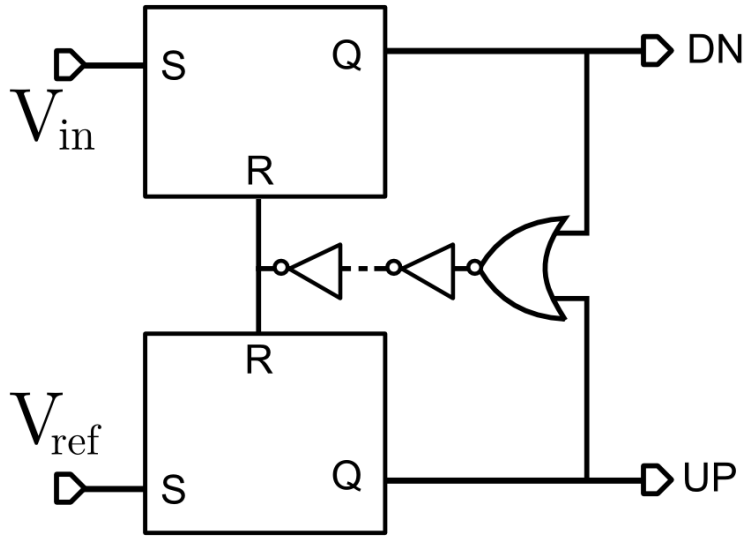


Figure 3.18: Phase frequency detector

caused by latches a delay stage should be added in series with NOR gate that prevents the glitches at the outputs. The operation of this PFD is explained in [34].

The PFD is followed by the charge pump circuit shown in Fig. 3.19 (a). This circuit is composed of two current sources that are switched ON and OFF by outputs of the PFD [45], [46]. Therefore the output current of charge pump is proportional to the delay between reference signal and divider output [47], [48]. The phase-to-current coefficient of the charge

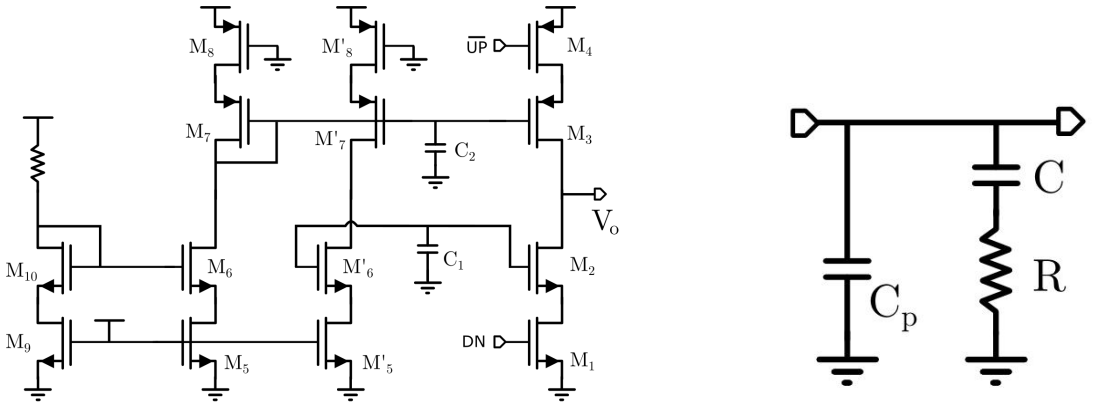


Figure 3.19: (a) Charge pump, (b) second order low pass filter

pump is given by:

$$K_{PFD,CP} = \frac{I}{2\pi} \tag{3.18}$$

where in this case current is set to $I = 770uA$. The output current of the charge pump is applied to a low-pass filter (LPF) that integrates the current and converts it to a voltage [45], which is applied to the control voltage of the VCO. A common type of filter used in PLLs is shown in Fig. 3.19(b). It includes a shunt capacitor, C_p, in parallel with a series RC. This filter integrates the current injected from charge pump where as RC is used to add a zero in order to increase phase margin. The admittance of the LPF in Fig. 3.19(b) can be expressed as:

$$Y = sC_p + \frac{1}{R + \frac{1}{sC}} = \frac{sC_p(sCR + 1) + sC}{sCR + 1} \tag{3.19}$$

Therefore, the control voltage of the VCO is given by:

$$v_c = \frac{I}{2\pi}\frac{1}{Y}\Delta\phi = \frac{I}{2\pi}\frac{sCR+1}{s(C+C_p)(1+sC_tR)}\Delta\phi \tag{3.20}$$

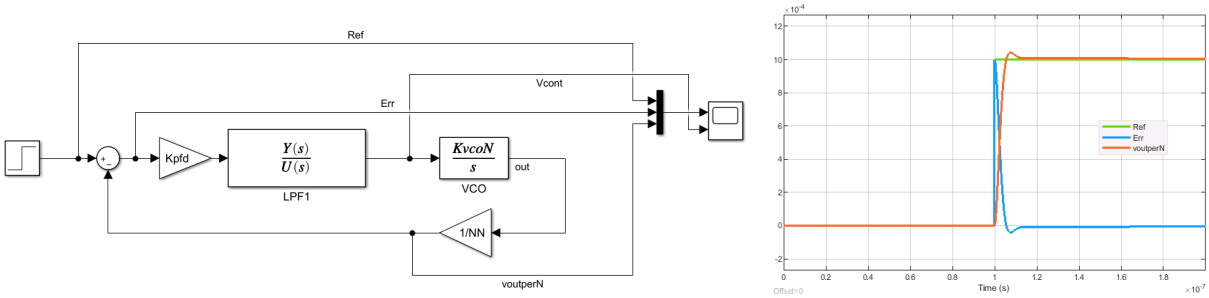
where $C_t = CC_p/(C+C_p)$. The values that are used in this design are $C_p = 1\,pF$ $C = 130\,pF$ and $R = 2.2\,k\Omega$.

3.6 Closed-Loop Analysis of PLL

A very popular PLL method to verify the time-domain behavior of a PLL is to examine the phase locking after disturbing it with a pulse input. The behavioral model of the PLL is implemented in MATLAB-Simulink, illustrated in Fig. 3.20(a). The closed loop transfer function can be expressed as:

$$\frac{\phi_o}{\phi_i} = \frac{k(1+RCs)}{RC_p(C+Cp)s^3 + (C+C_p)s^2 + kRC/Ns + k/N} \tag{3.21}$$

where $k = K_{PFD}k_{VCO}$. To study the locking mechanism a step function is applied to the input reference and the output response of the PLL is observed. Fig. 3.20(b) shows the applied input and the output signal after division which shows slight overshoot. Moreover the phase error at the input of PFD shows a sharp rising edge but the feedback loop limits the error to close to zero.



(a) (b)

Figure 3.20: (a) Charge pump, (b) second order low pass filter

3.7 Measurements

To measure the PLL a test board is designed and fabricated. The board is responsible for providing DC bias voltages and guiding the input/output signals to the connector to be connected to measurement equipment. The pads on the chip are wirebonded to the board. The chip is placed inside a cavity with a depth of 12 mil to minimize the wirebond inductance.

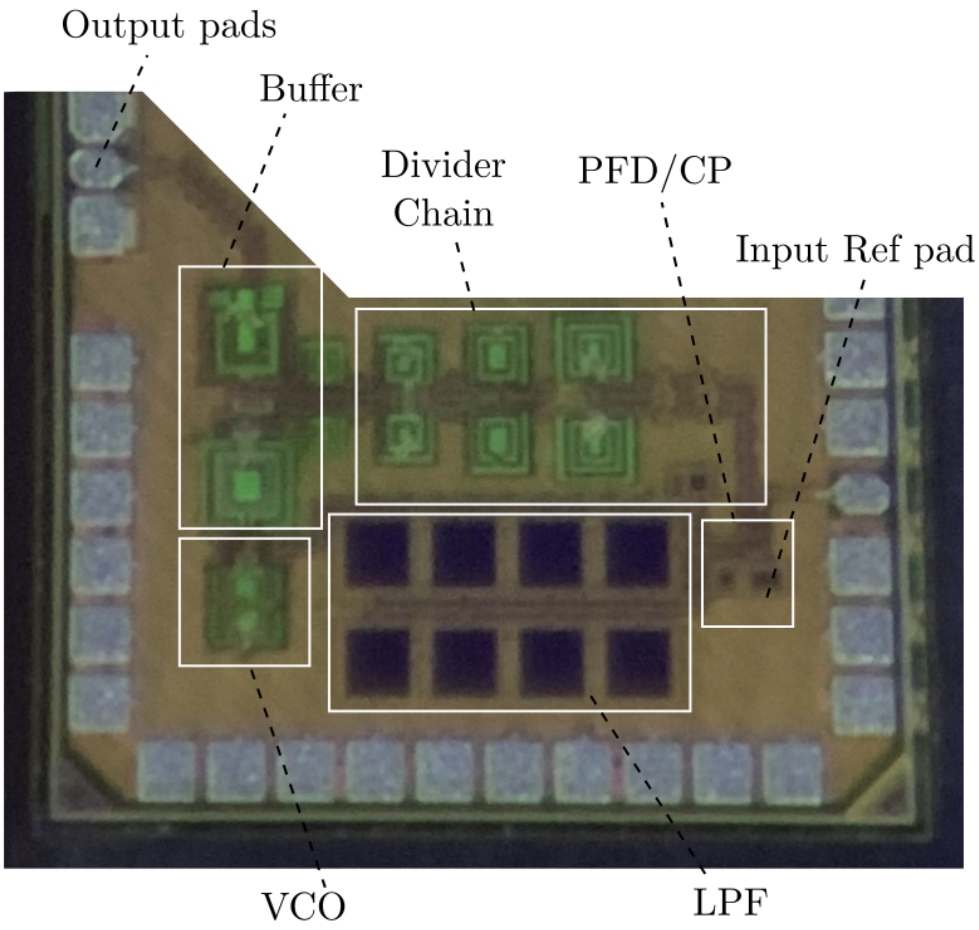


Figure 3.21: PLL die photograph

Chapter 4

Degenerate Band Edge Oscillator Design

4.1 Introduction

Many oscillators consist of a passive tank that is responsible for resonance, an active part that converts the DC power to the oscillation output and the load that is driven by the oscillator. Each of these parts has been studied extensively to improve the overall performance of oscillators. The passive network is realized as an LC tank in conventional VCOs, which is directly connected to the active parts and drives the load from the same point. In that case, the load directly impacts the quality factor of the LC tank, which may prevent the oscillation start up. To avoid the loading effect on the VCO a buffer stage can be inserted between oscillator and the load, which requires additional power consumption. Recently a new approach to oscillator design has been proposed where the LC tank is replaced by a set of distributed passive components [10, 49, 50]. In those structures the load and active components are connected to different ports of the passive network.

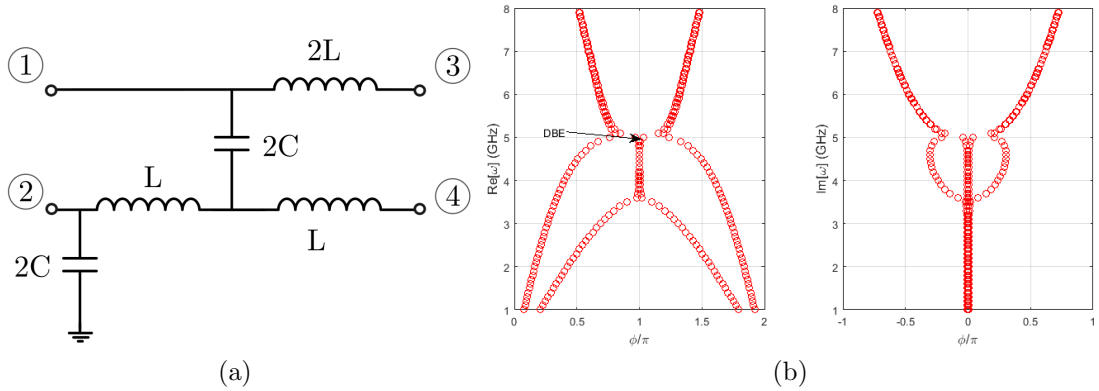
The use of degenerate band edge (DBE) structures have been shown to be a promising method to be used in oscillators to provide resonance with minimal loading effect. A DBE is a phenomenon that can be observed in the dispersion diagram of some structures such as double-ladder circuits. In that condition, the dispersion curve shows a degenerate behavior at the edge of the pass band. One of the interesting features of such behavior is that if the system oscillates at a nearby frequency it will be relatively insensitive to the external loading. While in theory a DBE can only be produced in a network with infinite number of unit cells, it can be approximated for a finite number of unit cells. The deviation from the ideal case for different numbers of unit cells is studied in [49].

4.2 DBE in double-ladder Structures

A ladder is a set of passive components arranged in an L-shape configuration; for example the shunt and series elements can a capacitor and inductor, respectively, that results in a lumped model of a transmission line. As explained in [49–51], single ladder cannot produce a degenerate band edge in the dispersion diagram. Alternatively, by having a pair of single ladders that are coupled together with either a capacitor or an inductor, a double-ladder structure can be realized. Double-ladders can easily lead to a degenerate band edge by selecting appropriate component values.

4.2.1 Lumped Structure

Double-ladder structures can be realized by lumped components. A ladder composed of series inductors and shunt capacitances can be used to form a double-ladder as shown in Fig. 4.1(a). The dispersion diagram for such a network, plotted in Fig. 4.1(b), consists of the real and imaginary parts of the frequency versus the phase shift between input and



(a) (b)

Figure 4.1: (a) A double-ladder structure, (b) corresponding dispersion diagram showing DBE at around 5 GHz. $C = 1\,pF$ and $L = 1nH$

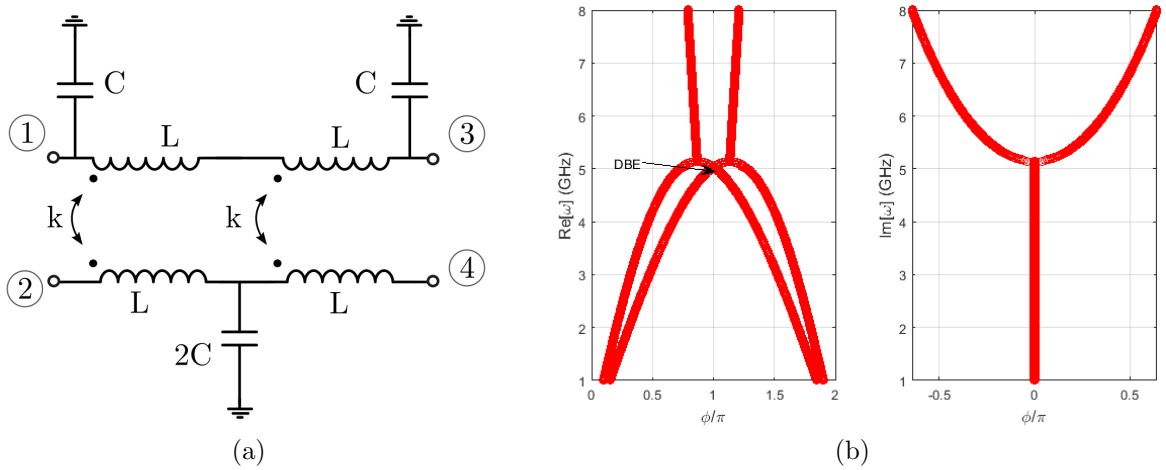
output ports.

A band gap occurs when the frequency becomes purely imaginary which means that the wave decays exponentially as it propagates. If the derivative of the dispersion diagram at the edge of the band gap is zero, then a degenerate band edge (DBE) is observed. As shown in Fig. 4.1(b) the DBE occurs at 5 GHz.

A DBE can also be observed in magnetically coupled right-handed ladders as shown in Fig. 4.2(a). In this double-ladder magnetic coupling is realized between series inductors within each ladder represented by coupling coefficient of k. For this structure the band gap starts around 5.7 GHz. Although the derivative is not exactly zero, it becomes very small.

For a lumped element implementation, this ladder is advantageous as the inductors can be overlapped to save the area, whereas in the previous case (Fig. 4.1(a)) there must be enough distance between all of the inductors to eliminate the magnetic coupling. Moreover, this structure is convenient to implement differentially due to its symmetric structure.

Fig. 4.3(a) shows another double-ladder structure that can realize a DBE. This structure includes both magnetic and capacitive coupling, which allows for placing the inductors closer to each other as compared to the Fig. 4.1(a) circuit. The dispersion diagram of this ladder



(a) (b)

Figure 4.2: (a) double-ladder with magnetic coupling, (b) corresponding dispersion diagram. $C = 1\,pF$, $L = 1nH$ and $k = 0.1$

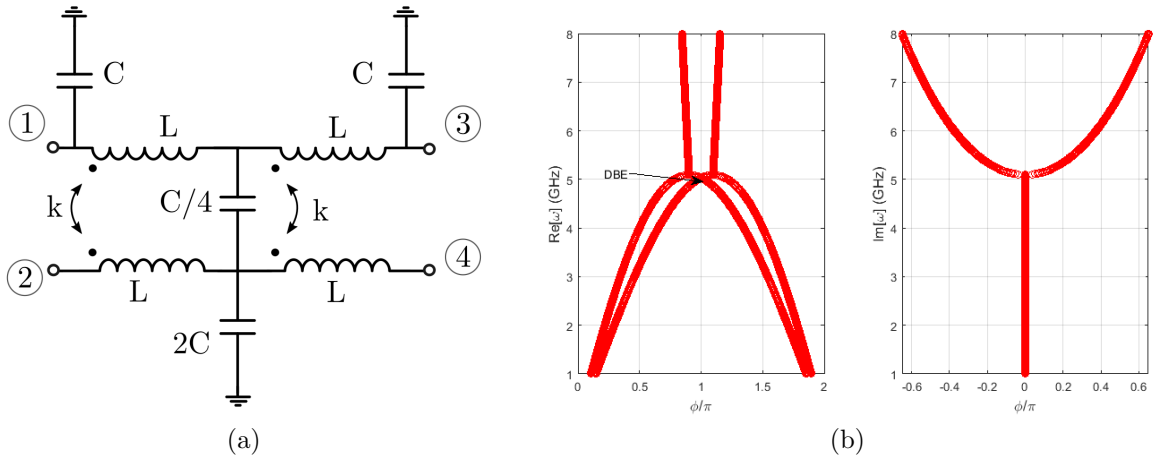
cell is shown in Fig. 4.3(b).

4.2.2 Distributed Structure

A DBE can be generated in a distributed structure as shown in 4.4(a), which is composed of a pair of transmission lines with a capacitor connected between the two centers. Unlike a lumped network, a distributed network can have an infinite number of resonances and band gaps. However, only the low frequency ones are important since The high-frequency resonances exhibit high losses and are therefore less likely to be excited.

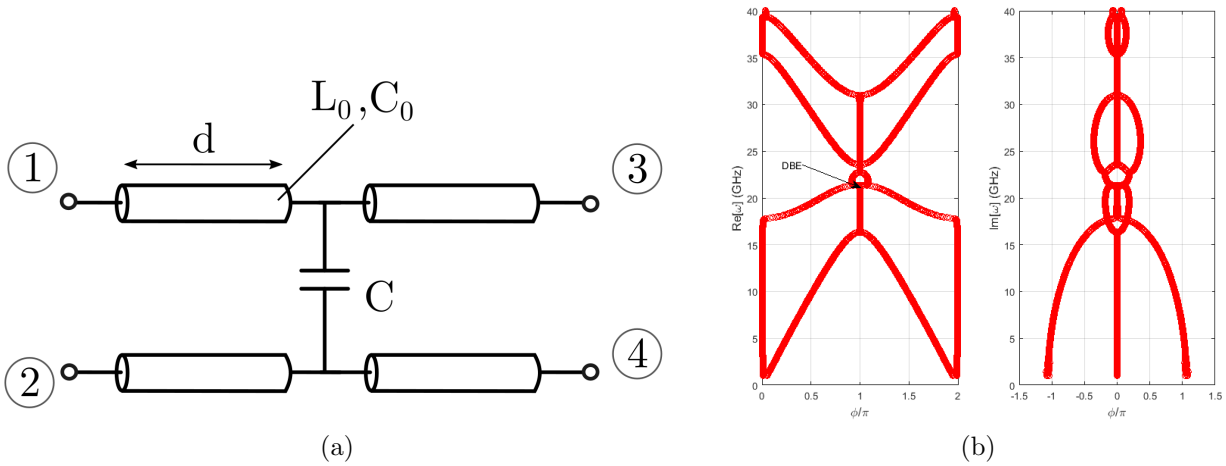
For accurate results distributed structures must be modeled in full-wave electromagnetic solvers such as HFSS. Fig. 4.5(a) shows the 3D model of a unit cell used in a double-ladder implemented as microstrip lines over a dielectric substrate. The dielectric is made of ROGERS-3003 material ($\epsilon_r = 3$) with 20 mil height.

The S-parameters obtained from the HFSS simulation are used to calculate the dispersion diagram illustrated in Fig. 4.6.



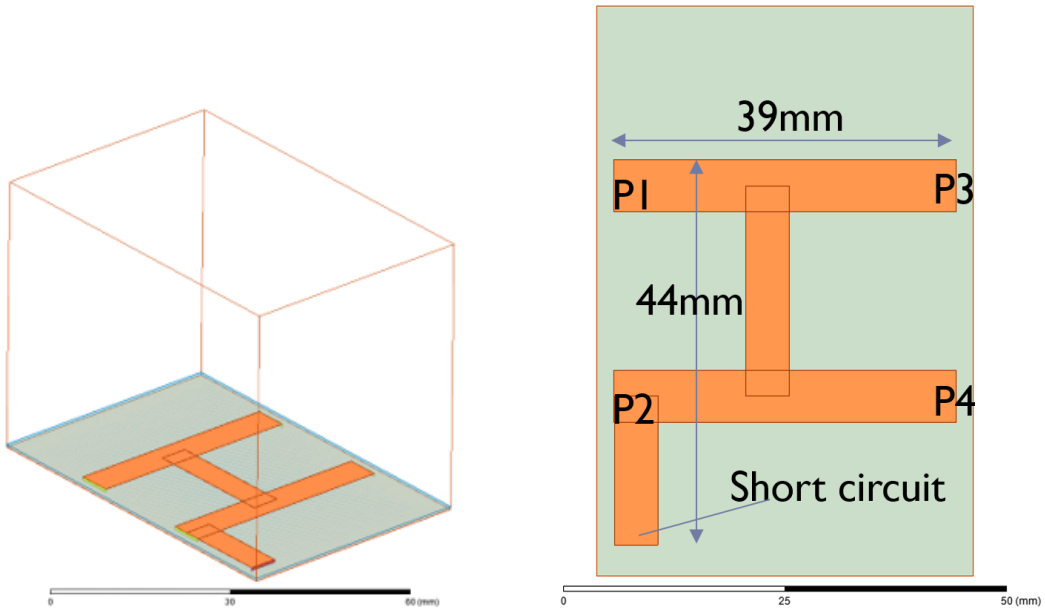
(a) (b)

Figure 4.3: (a) double-ladder with magnetic and capacitive coupling, (b) corresponding dispersion diagram. $C = 1\,pF$, $L = 1nH$ and $k = 0.1$



(a) (b)

Figure 4.4: (a) Distributed double-ladder realized by two transmission line and a series capacitor, (b) corresponding dispersion diagram.



(a) (b)

Figure 4.5: A unit cell of a distributed double-ladder realized by two transmission line and a short stub modeled in HFSS (a) 3D view (b) top view

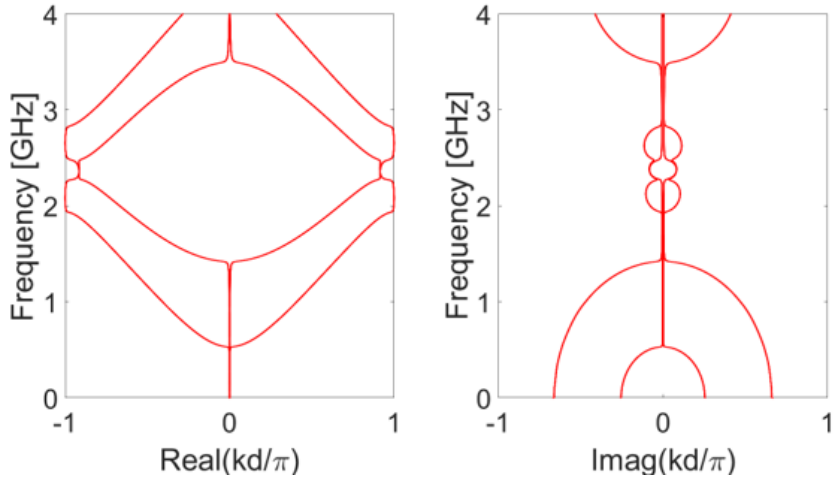


Figure 4.6: Dispersion diagram for a double-ladder microstrip line simulated in HFSS

4.3 Active Components for DBE Oscillators

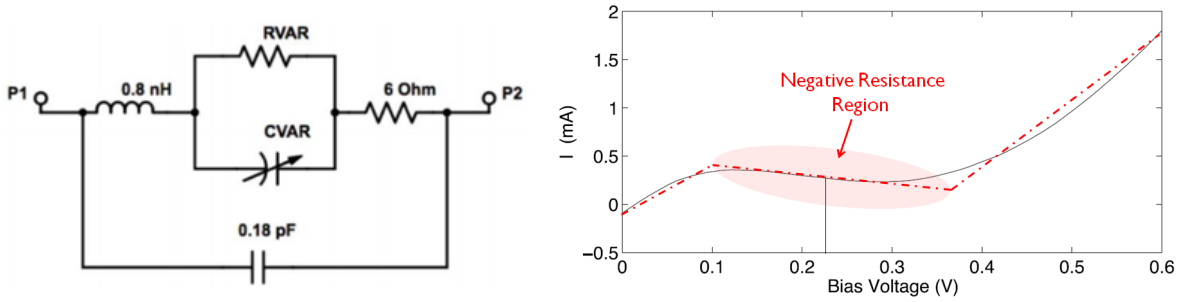
While the passive part is responsible for providing the resonance in an oscillator, the active part provides the gain to start and sustain the oscillation. A negative resistances can be modeled as a variable resistor whose resistance is negative for small voltage swings but becomes positive at higher swings. The IV characteristic of such model can be expressed as a 3rd-order polynomial given by:

$$i = -g_m v + \alpha v^3 \tag{4.1}$$

where g_m is the magnitude of the negative conductance and α is a constant. This equation can be implemented in circuit simulators, such as Cadence, as a polynomial voltage-controlled-current-source. Active components can be realized either as a single-ended or differentially. The most common single-ended realizations are based on two-terminal diodes such as the Gunn diode, IMPATT diode, and tunnel diode. Such elements are mainly implemented in a compound semiconductor (III-V semiconductor) and used in high power oscillators. On the other hand, a negative resistance can easily be realized in CMOS technology as a cross-coupled transistor pair.

4.3.1 Tunnel diode

A tunnel diode is a semiconductor that is biased in a region that shows negative resistance, This behavior is based on the tunnel effect of carriers through a highly-doped narrow p-n junction [52]. Such an element can be modeled by an equivalent circuit that includes a variable resistor that represents the nonlinear behavior, as well as junction and packaging parasitics as illustrated in Fig. 4.7 [53](a). The variable resistance has an IV-characteristic shown in Fig. 4.7(b), which can be approximated as a piece-wise linear function to be imple-



(a) (b)

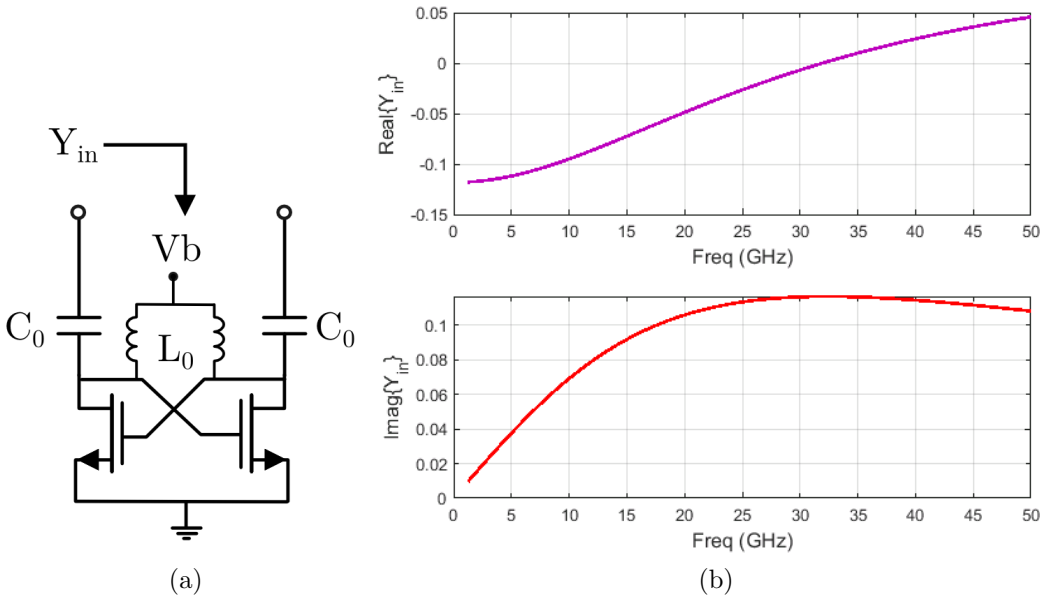
Figure 4.7: (a) Equivalent circuit for a tunnel diode, (b) IV-characteristic of RVAR in the tunnel diode model showing negative resistance over a voltage range from 0.1V to 0.35V.

mented in Cadence simulator. As evident from the IV-characteristic the negative resistance is only available from 0.1 V to 0.3 V with average current of 0.2 mA, which results in a low oscillation amplitude.

4.3.2 Cross-coupled Pair

A cross-coupled transistor pair is the most common realization of negative resistance as it can be implemented in CMOS process. As illustrated in Fig. 4.8(a), cross-coupled transistor pair is connected to decoupling capacitors C_0 and large inductor L_0 to bias the transistors. This circuit can provide conductance of $-g_m/2$ at the differential output port as well as parasitic capacitors at the drain and gate of the transistors. The real and imaginary parts of the admittance seen from the output port is plotted in Fig. 4.8(b).

The cross-coupled pair is essentially a differential component so it should be used in differential mode or one port must carefully terminated to a load in a way that does not disturb negative resistance behavior significantly. This can be done by simply connecting one of the differential terminals to a resistor around 40Ω. It should be noted that the negative resistance and input capacitance will be changed by this termination.



(a) (b)

Figure 4.8: (a) Cross-coupled pair to realize negative resistance with bias circuit, (b) real and imaginary parts of input admittance of cross-coupled pair in single-ended mode

4.4 DBE Based Oscillators

A DBE structures can be used as the passive part in a high-frequency oscillator. To make this realization feasible, first, the number of unit cells must be limited to a reasonable number. Then, the location of the load and the active device must be determined to be less sensitive to the load magnitude and provide maximum power to the load.

Fig. 4.9(a) shows 8 unit cells of a double-ladder network, whose unit cell is shown in Fig. 4.4. In this structure the ports are connected to ground except for port 1, which is excited by an AC source. Fig. 4.9(b) shows the voltage amplitudes at each of the nine nodes $(V_1, V_2, .., V_9)$ versus frequency. Although 7 resonances can be identified in the voltage response, only the resonance at 21.26 GHz is associated with a DBE (see Fig. 4.4(b)). Fig. 4.9(c) presents the voltage amplitude at the resonant frequencies versus the node number. Evidently voltages at nodes 1 and 9 are forced to be 1 V and 0 V, respectively. For each resonant frequency the distribution of voltage over the nodes has a relatively periodic behavior. For example,

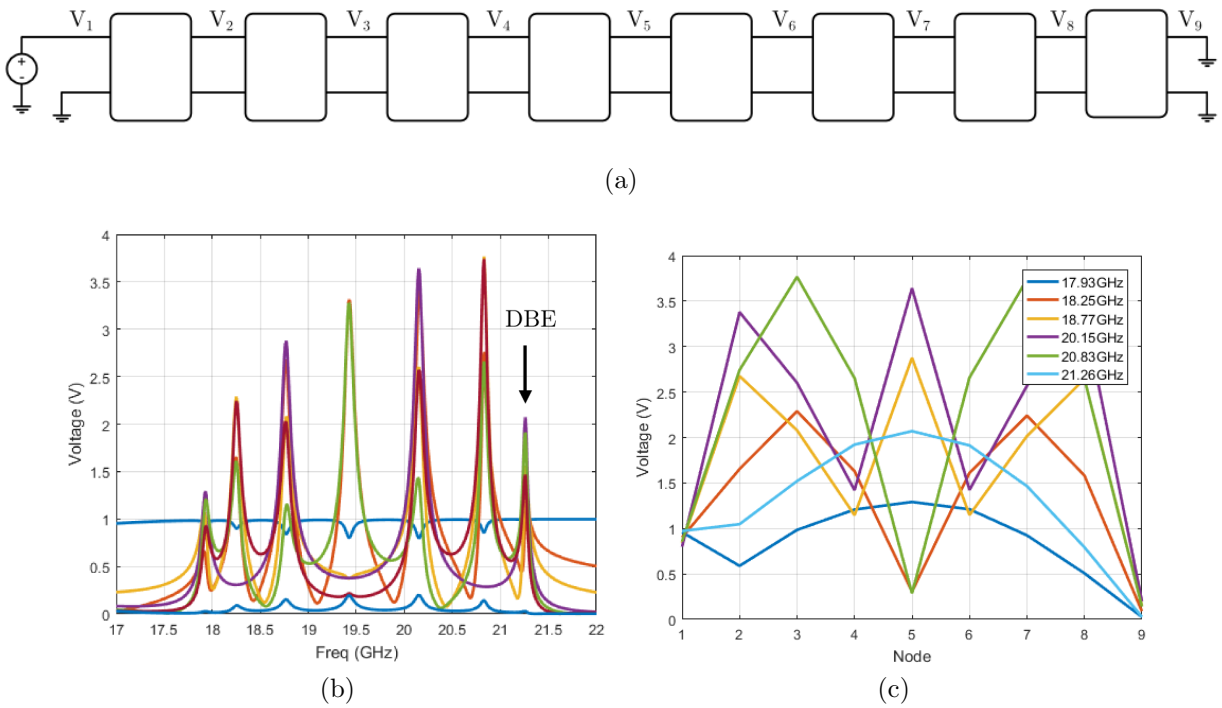
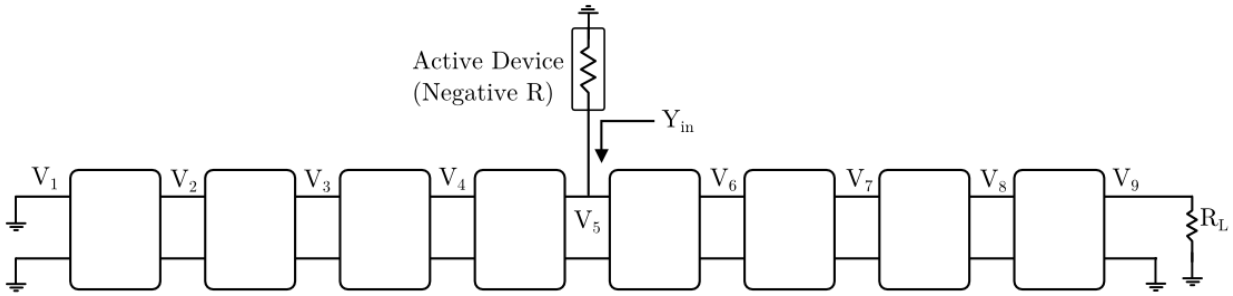


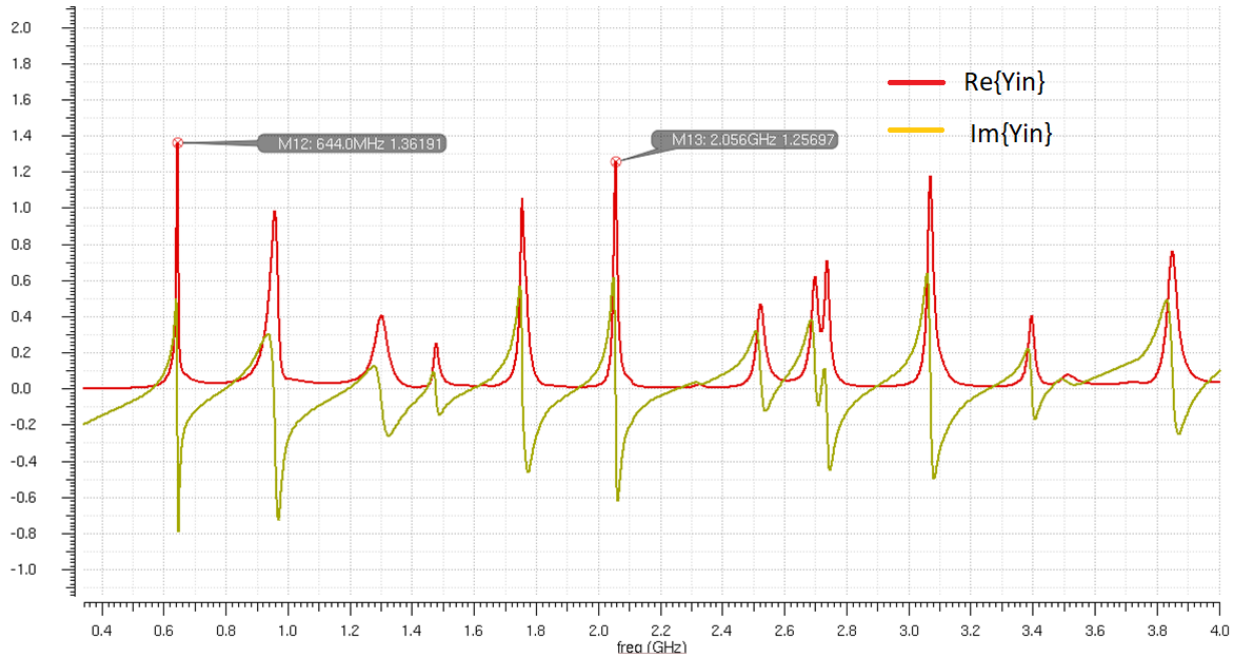
Figure 4.9: (a) Truncated DBE structure with eight unit cells, (b) voltage distribution at different nodes over the frequency, (c) voltage at different nodes at 6 resonance frequencies.

$f = 21.26$ and $f = 20.15$ GHz have one and three maxima, respectively. To excite the DBE resonance that occurs at $f = 21.26$ GHz the negative resistance must be located at the node with highest voltage swing, i.e. node 5.

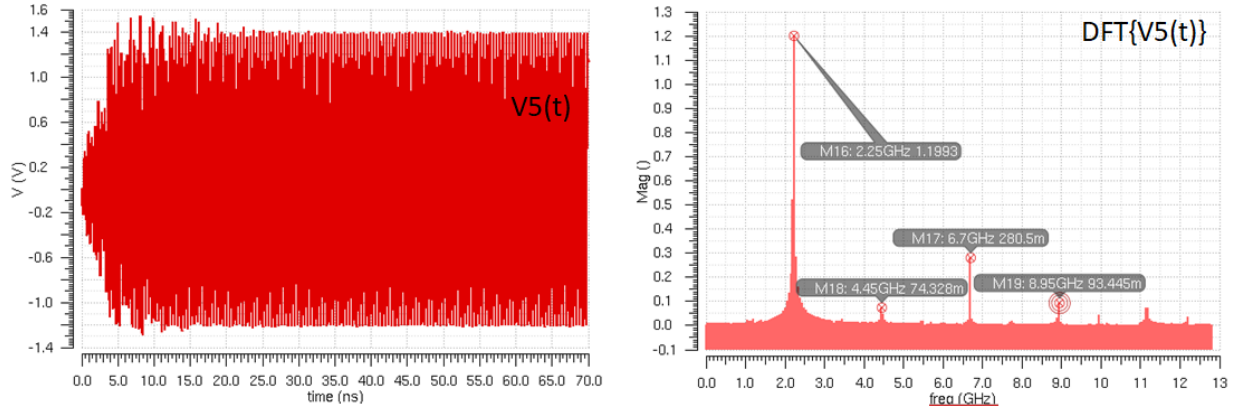
After choosing the location of negative resistance in the ladder structure, the impedance seen into that location determines the exact frequency of oscillation and minimum conductance for oscillation start-up. The active device can be connected to the ladder structure at the middle node, as shown in Fig. 4.10(a), which results in admittance illustrated in Fig. 4.10(b). Based on this configuration, the time domain simulation results can be conducted as presented in Fig. 4.10(c) that shows an oscillation at 2.25 GHz with voltage amplitude of 2.7 V peak-to-peak at node 5.



(a)



(b)



(c)

Figure 4.10: (a) Truncated DBE structure with eight unit cells with a negative resistance element connected to node 5, (b) input admittance seen at the node 5, (c) time domain simulation of the oscillator output at node 5 and its DFT.

Chapter 5

Conclusion

This dissertation presents a systematic method to analyze and design of VCOs for mm-wave imaging systems.

In Chapter 1, a typical mm-wave imaging system and its operation principles are presented. It is concluded that such a system requires high-performance frequency synthesizers and oscillators. A general configuration for a PLL is presented implying that the VCO is the most critical building block of a PLL. Moreover, a typical LC VCO design for such systems is demonstrated and its limitations are discussed. The trade-offs between inductor and capacitor switching for an LC VCO are investigated. The design approach taken in this dissertation is based on the multi-port oscillation theory which is rediscovered, generalized and applied to two different VCO designs discussed in the following chapters.

In Chapter 2, multi-port oscillation theory is applied to analyze a conventional QVCO in a systematic way. Then, this theory is employed to study another class of QVCOs, called resonant-coupled QVCOs, that are based on a ring oscillator with both active and passive components. Different design aspects of such oscillators are investigated and a design methodology is introduced to improve their performance such as phase noise and quadrature

phase error. Finally, a novel RC-QVCO operating at 40 GHz with common-mode resonance to improve phase noise is proposed and implemented in 65nm CMOS.

In Chapter 3, a 65 GHz PLL is designed and implemented in 65nm CMOS with a novel multimode VCO. The proposed VCO has 4 oscillation modes that can be changed by a proposed inductor switching structure. This structure is based on four coupled windings: primary, secondary, and two floating loops that are terminated to CMOS switches. Changing the states of switches leads to adjustment of the coupling factor between the primary and secondary windings that is exploited for coarse frequency tuning of the VCO.

In Chapter 4, design of VCOs based on degenerate band edge structures is studied. Due to the DBE's unique characteristics, such VCOs show low sensitivity to the value of the load. A few structures, including both lumped and distributed networks, that support DBE behavior are presented in this chapter. Moreover, active components that can be used in DBE-based VCOs are investigated such as tunnel diode and cross-coupled transistor pairs. Eventually, a VCO design is reported showing oscillation frequency of 2.25 GHz in a transient simulation.

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