UNIVERSITY OF CALIFORNIA

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Achieving Continuous-Wave Lasing for Violet *m*-plane GaN-Based Vertical-Cavity Surface-Emitting Lasers

A dissertation submitted in partial satisfaction of the requirements for the degree

Doctor of Philosophy
in
Materials

by

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December 2018

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Achieving Continuous-Wave Lasing for Violet *m*-plane GaN-Based Vertical-Cavity Surface-Emitting Lasers

by

Charles Alexander Forman

This dissertation is dedicated to my wife

Yimeng Sun

my parents

Peter and Marilyn Forman

and my brother

James Forman

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I am grateful to so many people for their tremendous support in both my life and career. First, I would like to thank my adviser, Prof. Shuji Nakamura, and the rest of my committee, Prof. Steve DenBaars, Prof. Jim Speck, and Prof. Jon Schuller, for giving me an opportunity to pursue this research. I am particularly grateful to Dr. Dan Cohen for all of his help throughout my time here. I would especially like to thank my wife, Yimeng Sun, for giving me continuous support throughout graduate school, even during the most difficult years when there were significant roadblocks in my research. My brother, James Forman, has also been very supportive, and I am lucky to have extremely supportive parents, Marilyn & Peter Forman. Thank you for always being there for me.

I would like to thank my high school physics teacher, Chris Blazey, for getting me excited about the world of science, and your excellent recommendation helped me get my first internship at Jefferson Lab. This led to several influential research experiences at Jefferson Lab and ultimately made me realize that I want to pursue a career in science and engineering. I am particularly grateful to my mentors at Jefferson Lab, including John Musson and Dr. Michael Kelley, as well as Jan Tyler and Olga Trofimova. I would also like to thank all of my great professors from Virginia Tech, including Prof. David Clark, Prof. Christopher Williams, Prof. Thomas Staley, Prof. Gary Pickrell, Prof. Abby Whittington, and Prof. Alex Aning.

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Work Experience

University of California, Santa Barbara (UCSB)
Graduate Student Researcher — Fall 2013 – Summer 2018
- Demonstrated the world's first continuous-wave (CW) nonpolar GaN VCSELs
- Increased UCSB GaN VCSEL output power from 0.5 mW to over 1 mW

Committee: Shuji Nakamura, James S. Speck, Steven P. DenBaars, Jon Schuller

University of California, Santa Barbara (UCSB)
Graduate Teaching Assistant — Winter 2017
200C: Structure Evolution in Materials
Supervisor: Anton Van der Ven

The College of William & Mary / Jefferson Lab — Summer 2012
Undergraduate Researcher
- Surface replication and characterization of electrodes for photoelectron guns

Advisor: Michael Kelley

Virginia Tech
Undergraduate Teaching Assistant — Spring 2012
MSE 3094: Materials and Manufacturing for Aerospace & Ocean Engineers
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Thomas Jefferson National Accelerator Facility
Science Undergraduate Laboratory Internship (SULI) — Summer 2010 and 2011
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Thomas Jefferson National Accelerator Facility
Undergraduate Internship — Summer 2009
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Publications

- **C. A. Forman**, S. Lee, E. C. Young, J. A. Kearns, D. A. Cohen, J. T. Leonard, T. Margalith, S. P. DenBaars, S. Nakamura, "Continuous-Wave Operation of *m*-Plane GaN-based Vertical-Cavity Surface-Emitting Lasers with a Tunnel Junction Intracavity Contact," *Appl. Phys. Lett.*, vol. 112, no. 11, p. 111106, March 2018.
- **C. A. Forman**, "The world's first CW non-polar GaN VCSEL," *Compound Semiconductor Magazine*, March 2018.
- **C. A. Forman**, S. Lee, E. C. Young, J. A. Kearns, D. A. Cohen, J. T. Leonard, T. Margalith, S. P. DenBaars, S. Nakamura, "Continuous-wave operation of nonpolar GaN-based vertical-cavity surface-emitting lasers," *Proc. SPIE Gallium Nitride Materials and Devices XIII*, 105321C, February 2018.
- S. Lee, **C. A. Forman**, C. Lee, J. Kearns, E. C. Young, J. T. Leonard, D. A. Cohen, J. S. Speck, S. Nakamura, S. P. DenBaars, "GaN-based vertical-cavity surface-emitting lasers with MOCVD-grown tunnel junction contacts,"*Appl. Phys. Express, under review*, 2018.
- **C. A. Forman**, S. Lee, E. C. Young, J. T. Leonard, D. A. Cohen, B. P. Yonkee, T. Margalith, R. M. Farrell, S. P. DenBaars, J. S. Speck, S. Nakamura , "Nonpolar GaN-based vertical-cavity surface-emitting lasers," *2017 IEEE Photonics Conference (IPC)*, Orlando, FL, pp. 233-234, 2017.
- **C. Forman**, J. Leonard, B. Yonkee, C. Pynn, T. Mates, D. Cohen, R. Farrell, T. Margalith, S. DenBaars, J. Speck, S. Nakamura, "Semipolar ($20\bar{2}1$) III-Nitride P-Down LEDs with in situ anneal to reduce the Mg memory effect," *Journal of Crystal Growth*, vol. 464, pp. 197-200, April 2017.
- **C. A. Forman**, J. T. Leonard, E. C. Young, S. Lee, D. A. Cohen, B. P. Yonkee, R. M. Farrell, T. Margalith, S. P. DenBaars, J. S. Speck, S. Nakamura, "Nonpolar GaN-based vertical-cavity surface-emitting lasers," *2016 International Semiconductor Laser Conference (ISLC)*, Kobe, Japan, pp. 1–2. IEEE, 2016.
- C. Lee, C. Zhang, D. L. Becerra, S. Lee, **C. A. Forman**, S. H. Oh, R. M. Farrell, J. S. Speck, S. Nakamura, J. E. Bowers, S. P. DenBaars, "Dynamic characteristics of 410 nm semipolar ($20\bar{2}\bar{1}$) III-nitride laser diodes with a modulation bandwidth of over 5 GHz," *Appl. Phys. Lett.*, vol. 109, no. 10, p. 101104, Sep. 2016.
- D. Snelling, H. Blount, **C. Forman**, K. Ramsburg, A. Wentzel, C. Williams, and A. Druschitz, "The effects of 3D printed molds on metal castings,." *International solid freeform fabrication symposium*, 2013.

Patents

- **C. Forman**, S. Lee, E. Young, J. Kearns, D. Cohen, S. DenBaars, J. Speck, S. Nakamura, "III-Nitride Surface-Emitting Laser and Method of Fabrication," Docket 30794.662-US-P1, Prepared by Gates & Cooper LLP, Oct. 2017 (provisional patent).
- **C. Forman**, S. Lee, J. Kearns, S. DenBaars, S. Nakamura, "MOCVD Tunnel Junction with As-Grown Activated Buried p-GaN," Docket 30794.672-US-P1, Prepared by Gates & Cooper LLP, Oct. 2017 (provisional patent).
- **C. Forman**, J. Kearns, S. Nakamura, "Polarization-locked Communication using III-Nitride *m*-Plane Vertical Cavity Surface Emitting Lasers (VCSELs)," Docket 30794.666-US-P1, Prepared by Gates & Cooper LLP, Oct. 2017 (provisional patent).
- **C. Forman**, J. Kearns, S. Nakamura, "III-Nitride Vertical Cavity Surface Emitting Laser (VCSEL) White Light Illumination System," Docket 30794.665-US-P1, Prepared by Gates & Cooper LLP, Oct. 2017 (provisional patent).
- **C. Forman**, J. Kearns, D. Cohen, K. Kosik, S. Nakamura, "III-Nitride Surface-Emitting Laser Fluorescent Sensor" Docket 30794.664-US-P1, Prepared by Gates & Cooper LLP, Oct. 2017 (provisional patent).
- **C. Forman**, J. Leonard, S. Lee, E. Young, D. Cohen, R. Farrell, S. DenBaars, J. Speck, S. Nakamura, "Buried Tunnel Junction Aperture for III-Nitride Surface Emitting Lasers," Docket 30794.629-US-P1, Prepared by Gates & Cooper LLP, Sept. 2016 (provisional patent).

Conference Presentations

- **C. A. Forman**, S. Lee, E. C. Young, J. A. Kearns, D. A. Cohen, J. T. Leonard, T. Margalith, S. P. DenBaars, S. Nakamura, "Continuous-wave operation of nonpolar GaN-based vertical-cavity surface-emitting lasers," *SPIE Photonics West 2018 (SPIE OPTO)*, San Francisco, CA, February 2018.
- **C. A. Forman**, S. Lee, E. C. Young, J. T. Leonard, D. A. Cohen, B. P. Yonkee, T. Margalith, R. M. Farrell, S. P. DenBaars, J. S. Speck, S. Nakamura, "Nonpolar GaN-Based Vertical-Cavity Surface-Emitting Lasers," *2017 IEEE Photonics Conference (IPC)*, Orlando, FL, Oct. 2017.
- **C. A. Forman**, J. T. Leonard, E. C. Young, S. Lee, D. A. Cohen, B. P. Yonkee, R. M. Farrell, T. Margalith, S. P. DenBaars, J. S. Speck, S. Nakamura, "Nonpolar GaN-based vertical-cavity surface-emitting lasers," *2016 International Semiconductor Laser Conference (ISLC)*, Kobe, Japan, Sept. 2016.
- **C. A. Forman**, J. T. Leonard, E. C. Young, D. A. Cohen, T. Margalith, S. P. DenBaars, J. S. Speck, S. Nakamura, "Nonpolar III-nitride Vertical-Cavity Surface-Emitting Lasers," *International Workshop on Nitride Semiconductors (IWN 2016)*, Orlando, FL, October 2016.
- **C. Forman**, J. Leonard, B. Yonkee, C. Pynn, T. Mates, D. Cohen, R. Farrell, T. Margalith, S. DenBaars, J. Speck, S. Nakamura, "Semipolar ($20\bar{2}1$) III-Nitride P-Down LEDs with in situ anneal to reduce the Mg memory effect," *18th International Conference on Metal Organic Vapor Phase Epitaxy*, San Diego, CA, July 2016.

Awards

- **SSLEEC Outstanding Researcher Award** 2017
- **NSF GRFP Honorable Mention** 2013
- **National ACerS Speaking Contest 3rd Place at MS&T in Columbus, Ohio** 2011
- **Virginia Tech ACerS Speaking Contest 1st Place** 2011
- **Selected for publication in the DOE Journal of Undergraduate Research XI** 2011
  Superconducting RF Accelerator Cavity: Examination of the Interior Surface
- **AAAS Student Poster Session 2nd Place in Math, Technology, and Engineering** 2011
  Acknowledged in *Science* Magazine (Volume 332, 22 April 2011)
- **National Semi-Finals in the ACerS Speaking Contest at MS&T in Houston, Texas** 2010
- **Virginia Tech ACerS Speaking Contest 1st Place** 2010

Materials Fabrication and Characterization Experience

Metal-organic chemical-vapor deposition (MOCVD), ion beam deposition (IBD), sputtering, thermal evaporation, e-beam evaporation, photolithography, photoelectrochemical (PEC) etching, plasma-enhanced chemical vapor deposition (PECVD), reactive-ion etching (RIE), dicing saw, chemical-mechanical polishing, flip-chip bonding, photoluminescence, SEM, AFM, FIB, XRD, cathodoluminescence, profilometry, UV-Vis spectroscopy, LIV characterization, ellipsometry, laser scanning confocal microscopy.

Software & Modeling Skills

Mathematica, COMSOL thermal modeling, Vertical waveguide optics modeling, Microsoft Office, Autodesk Inventor, CompleteEASE ellipsometry, and some experience with LabVIEW, Matlab, Lumerical Interconnect, SiLENSe, and FIMMWAVE.

Abstract

Achieving Continuous-Wave Lasing for Violet *m*-plane GaN-Based Vertical-Cavity Surface-Emitting Lasers

by

Charles Alexander Forman[1]

Vertical-cavity surface-emitting lasers (VCSELs) are a special class of laser diode that use top-side and bottom-side parallel mirrors to emit a laser beam vertically from the top surface, as compared to conventional edge-emitting lasers that emit light from the sides of the devices. Compared to edge-emitting lasers, VCSELs have many unique attributes, such as a low threshold current that leads to low power consumption, high-speed direct modulation, superior beam quality, and they can be easily arranged into two-dimensional VCSEL arrays for scalable power. This leads to several exciting applications; for example, VCSELs are the key component in the Apple iPhone X that enables Face ID, which allows users to securely unlock their devices simply by looking at their phones. However, the VCSEL market is currently limited to red-emitting and infrared-emitting VCSELs that use GaAs-based and InP-based systems. If shorter wavelength emitting VCSELs could be created, it would open up a whole new world of untapped and exciting applications. For example, blue and green VCSELs could be paired with red VCSELs to create next-generation display and projector technology. The low power consumption and high beam quality of VCSEL-based displays would be

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particularly promising for virtual and augmented reality systems. Shorter wavelength VCSELs can be created using GaN-based materials, but these devices have been very challenging to create. The first GaN-based VCSEL was demonstrated in 2008, and only eight research groups have demonstrated these devices over the following decade. With the first report in 2012, the University of California, Santa Barbara (UCSB) has been the only group in the United States to create GaN-based VCSELs. Compared to the *c*-plane GaN VCSELs from all of the other groups, VCSELs from UCSB have used *m*-plane GaN, which uniquely provides 100% polarized emission for both individual VCSELs and VCSEL arrays. The main problem with GaN VCSELs from UCSB has been their inability to lase under continuous-wave (CW) operation. They could only lase under pulsed operation, which means that these VCSELs would fail if turned *on* for longer than a fraction of a millisecond. This has been a severe limitation that has prevented most practical applications of these devices. Therefore, the ultimate goal of the research described in this thesis has been to achieve CW lasing. This has been a tremendously difficult goal, and the initial VCSEL designs failed to lase, even under pulsed operation. Despite these initial discouraging results, this experiment was important because it led to an extensive failure analysis that revealed several key problems with the VCSEL design. Surface roughness prior to the DBR mirror deposition turned out to be a major problem that inhibited lasing due to scattering loss and reduced mirror reflectance. After performing experiments to improve the surface morphology, the surface roughness on the p-side was reduced by utilizing an indium flux during MBE tunnel junction regrowth, and the roughness on the n-side was reduced by removing an oxide residue that formed after the photoelectrochemical (PEC) undercut etch to remove the *m*-plane GaN growth substrate. Another significant problem was VCSEL yield in which only a small percentage of devices

successfully transferred onto the flip-chip substrate, and most of those devices were cracked. A series of flip-chip bonding experiments were conducted to optimize the Au-Au thermocompression bond, but the yield only marginally improved at first. The flip-chip bond was also responsible for a severe thermal issue that prevented CW operation in previous devices. Based on thermal modeling in COMSOL, heat generated in the active region could not flow directly downward due to the thermally-insulating bottom DBR, so there was a bottleneck in heat transport through a relatively thin gold contact along the sidewall of the bottom DBR toward the flip-chip substrate. Focused ion beam (FIB) cross-sectioning revealed cracks in that thin metal contact, which were found to significantly impair the VCSEL thermal performance based on COMSOL simulations. Both the VCSEL yield and thermal performance were improved by implementing a new flip-chip bonding design. Instead of Au-Au thermocompression bonding, Au-In solid liquid interdiffusion (SLID) bonding was performed at a much lower temperature and pressure, which greatly improved the VCSEL yield. Furthermore, Au-In SLID bonding significantly improved the VCSEL thermal performance by incorporated a liquid phase during bonding so that the entire bottom DBR was embedded within metal. This led to the world's first demonstration of CW operation for *m*-plane GaN VCSELs, and they were able to lase under CW operation for over 20 minutes of continuous testing.

Table of Contents

1. Introduction

Vertical-cavity surface-emitting lasers (VCSELs) are a special type of semiconductor laser diode that emits a laser beam vertically from its top surface, which differs from conventional edge-emitting lasers that emit light from the sides of the devices. VCSELs have a unique combination of advantages, including scalable power through two-dimensional (2D) VCSEL arrays, low threshold current, high-speed direct modulation, circular mode profile with low divergence, and on-wafer testing which significantly reduces production costs.[1] The global VCSEL market is rising rapidly due to their long list of unique attributes that range from high-efficiency to superior beam quality. For example, in December 2017, Apple Inc. awarded Finisar Corp. $390 million for research and development of VCSEL technology,[2] and VCSELs are the key components in the iPhone X that enable popular features such as Face ID so that users can securely unlock their devices simply by looking at them.

However, the current VCSEL market is limited to infrared-emitting (invisible) and red-emitting VCSELs. If shorter-wavelength blue and green VCSELs were developed, it would enable a whole world of untapped applications in display, illumination, data communication, and sensing technology. Gallium nitride (GaN) bridges the spectral gap to shorter wavelengths, including ultraviolet (UV), violet, blue, green, yellow, and red.

While other research groups have created polar *c*-plane GaN VCSELs, the University of California, Santa Barbara (UCSB) is the only group that has created nonpolar *m*-plane GaN VCSELs, which have several advantages such as inherent 100% polarized emission.[3,4] However, these devices have had a severe limitation: they have only been able to lase under pulsed operation (i.e., repetitively turning them on/off very quickly), which prevents most

practical applications for these devices as they would fail in less than a millisecond of continuous-wave (CW) operation.

This dissertation focuses on solving this critical problem with the ultimate goal of achieving CW operation for *m*-plane GaN VCSELs. Although it has been a significantly challenging project with many failed VCSEL devices over the years, it eventually led to the first demonstration of CW operation for *m*-plane GaN VCSELs, as described in Section 4. Before delving into those experiments and results, Section 1 gives an overview of GaN optoelectronics and later goes into the details of GaN-based VCSEL design. In order to better understand the UCSB VCSEL design, Section 2 describes the growth and fabrication procedure to create *m*-plane GaN VCSELs. Section 3 outlines the numerous VCSEL design improvements that have been made over the years, and Section 4 discusses the main experiments and developments that led to achieving CW lasing for *m*-plane GaN VCSELs.

1.1. Overview of GaN Optoelectronics

GaN-based optoelectronics have made a tremendous impact on the world. For example, the 2014 Nobel Prize in Physics was awarded to Isamu Akasaki, Hiroshi Amano, and Shuji Nakamura for inventing the efficient GaN-based blue LED, which revolutionized illumination technology. Efficient white light can be created by coating a blue LED with a yellow phosphor, and white LED lightbulbs have begun to replace incandescent and fluorescent lamps. While incandescent lightbulbs have a low efficiency of ~16 lumens per watt (~4% efficiency), white LEDs achieve over 300 lumens per watt with a wall-plug efficiency over 50%.[5] This makes a significant world-wide impact as it is estimated that up to 261 TWh of electrical energy will be saved by year 2030 through the widespread use of

efficient LED lighting.[6] Section 1.1.1 gives a brief overview of the III-nitride materials system that enables GaN optoelectronics, and GaN-based LEDs are further discussed in Section 1.1.2.

While the device structure is similar to LEDs, GaN-based laser diodes require additional fabrication steps to create an optical cavity (i.e., formed by two parallel mirrors) to create the optical gain required for lasing. Compared to LEDs, GaN-based laser diodes have several advantages, such as higher power per chip area and higher efficiency at higher current densities.[7] This makes GaN-based edge-emitting lasers attractive for high-power and directional applications, such as in automobile headlights,[8] as white light can be produced by exciting a yellow phosphor with a violet or blue laser. More details about the design and applications for GaN-based edge-emitting lasers are described in Section 1.1.3

Despite a long list of advantages (e.g., low threshold, high beam quality, etc.), GaN-based VCSELs are not yet commercially available and have been relatively difficult to fabricate. Compared to edge-emitting lasers, VCSELs are much smaller and require horizontally oriented mirrors with a significantly higher reflectivity (> 99%) to reach the threshold for lasing. While GaN-based edge-emitting lasers were demonstrated back in 1996,[9] it took over a decade longer to solve the numerous growth and fabrication challenges to create the first GaN-based VCSEL. As further described in Section 1.1.4, there have been eight research groups that have successfully demonstrated these devices, and many performance improvements have been achieved over the past ten years.

1.1.1. III-Nitride Materials System

The group III-nitride materials system consists of wide-bandgap semiconductors with emission wavelengths that range from the ultraviolet (UV) to the entire visible spectrum from

violet to red. The band gap energy versus lattice constant for III-nitride semiconductors is shown in Figure 1.

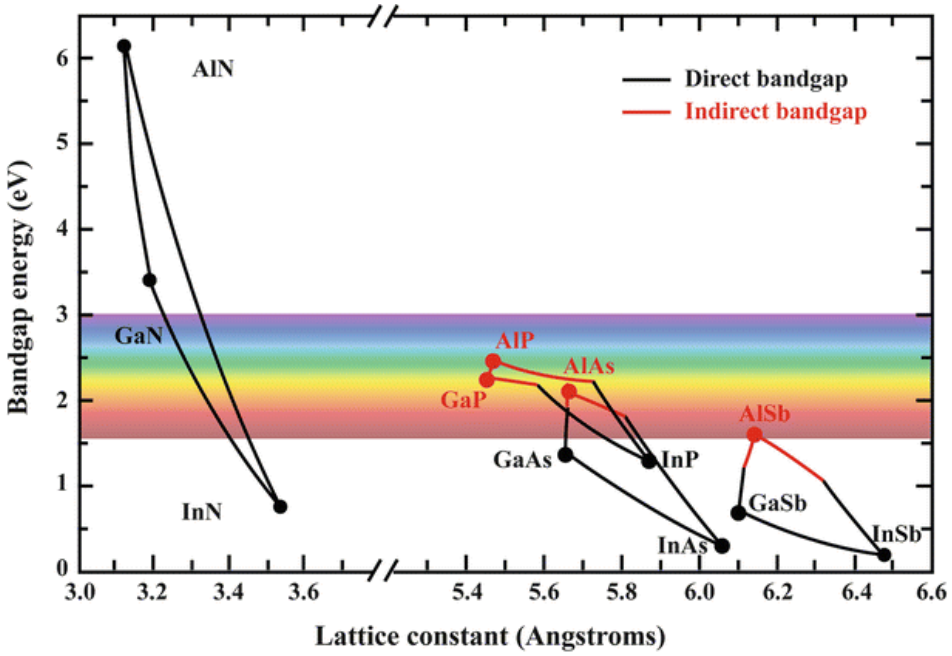


Figure 1. Band gap energy versus lattice constant at 300 K of III-V compound semiconductors.[10] Reprinted from [Zhu D., Humphreys C.J. (2016) Solid-State Lighting Based on Light Emitting Diode Technology. In: Al-Amri M., El-Gomati M., Zubairy M. (eds) Optics in Our Time. Springer, Cham] under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

There are a wide range of direct band gap energies for binary nitrides with values of 0.7 eV, 3.4 eV, and 6.0 eV for InN, GaN, and AlN, respectively. The emission wavelength in nanometers can be easily calculated by dividing 1240 by the band gap energy, as described by

$$E = \frac{h\,c}{\lambda} \approx \frac{(1240\ \text{eV} \cdot \text{nm})}{\lambda} \qquad (1)$$

where E is the band gap energy in electron volts, h is Planck's constant, c is the speed of light, and λ is the wavelength in nanometers. These band gap energies correspond to emission wavelengths of approximately 1771 nm for InN, 365 nm for GaN, and 207 nm for AlN. Emission wavelengths in between these values can be obtained by varying the compositions of AlGaN and InGaN ternary alloys, as shown in Figure 1. For example, while GaN emits UV

light, longer-wavelength emission from violet to red can be obtained by increasing the composition of indium in InGaN ternary alloys. However, while InGaN has the same crystal structure as GaN, indium atoms are larger than gallium atoms which leads to compressive and tensile stresses. The relatively large mismatch in the lattice constant between AlN, GaN, and InN causes highly strained heterostructures with InGaN and AlGaN ternary alloys and can lead to material defect formation and polarization-related electric fields. This makes it difficult to create efficient devices with longer wavelength emission from green to red because of the high lattice misfit strain that accompanies higher indium compositions in InGaN quantum wells (QWs). Furthermore, high indium composition InGaN QWs require relatively low MOCVD growth temperatures compared to GaN which can lead to increased impurity incorporation and growth defects such as nonradiative centers.[11]

Group III-nitride devices are conventionally grown on the basal *c*-plane (0001) along the polar *c*-axis of the hexagonal wurtzite crystal structure. Most devices are produced by heteroepitaxial growth in the *c*-direction using non-lattice matched substrates, such as sapphire or silicon carbide (SiC) substrates. While most companies use sapphire substrates, Cree, Inc. is known for using SiC substrates. However, heteroepitaxy on non-lattice matched substrates can lead to residual stress and high dislocation densities. As freestanding bulk GaN substrates have become more available due to improvements in bulk GaN growth, homoepitaxial growth has become a promising solution to significantly reduce defects such as threading dislocations.

While *c*-plane GaN devices are most common, extensive research has been conducted at UCSB for homoepitaxy on other growth orientations, and several unique properties have

been identified for semipolar planes and nonpolar *m*-plane GaN. Various crystallographic planes for the III-nitride wurtzite crystal structure are illustrated in Figure 2.

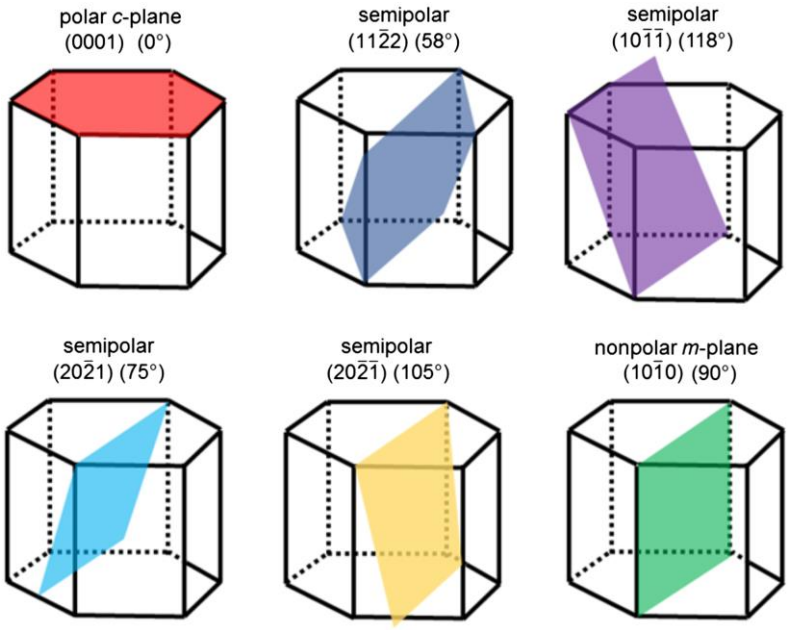


Figure 2. Illustrations of the III-nitride wurtzite crystal structure for polar *c*-plane (0001), [semipolar (11$\bar{2}$2), (10$\bar{1}\bar{1}$), (20$\bar{2}$1), and (20$\bar{2}\bar{1}$)], and nonpolar *m*-plane (10$\bar{1}$0). The inclination angles are shown with respect to *c*-plane.[10] Reprinted from [Zhu D., Humphreys C.J. (2016) Solid-State Lighting Based on Light Emitting Diode Technology. In: Al-Amri M., El-Gomati M., Zubairy M. (eds) Optics in Our Time. Springer, Cham] under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

Compared to conventional *c*-plane GaN devices, epitaxy on nonpolar and semipolar orientations can help reduce the quantum confined Stark effect (QCSE) that reduces electron-hole wave function overlap due to spontaneous and piezoelectric polarization fields parallel to the *c*-direction in InGaN QWs. Due to the polar nature of the Ga-N bond (represented by the difference in electronegativities) and the lack of inversion symmetry in wurtzite crystal structures, spontaneous and piezoelectric polarizations occur parallel to the *c*-axis. These create polarization-related electric fields in an InGaN QW, consisting of spontaneous and piezoelectric polarizations. The spontaneous polarization points toward the nitrogen face and results from the electronegativity of the nitrogen atom that creates a dipole in the III-nitride bond[12,13] as well as the unequal bonding lengths between Ga and N along the *c*- and *a*-

directions.[14,15] While spontaneous polarization is an intrinsic material property, piezoelectric polarization only exists in psuedomorphically grown strained layers, such as InGaN grown on GaN. For an InGaN QW grown on GaN, piezoelectric fields are generated by the compressive strain that causes further deviation of the *c/a* ratio compared to the ideal wurtzite crystal structure.[14,15] While spontaneous and piezoelectric polarizations both contribute to an electric field within an InGaN QW, the piezoelectric polarization dominates because the spontaneous polarization is nearly identical for InGaN and GaN.[15,16] As shown in the simulated energy band diagrams in Figure 3, the piezoelectric polarization causes an electric field, E_{pz}, that results in band bending and can greatly affect electron and hole wavefunction overlap.

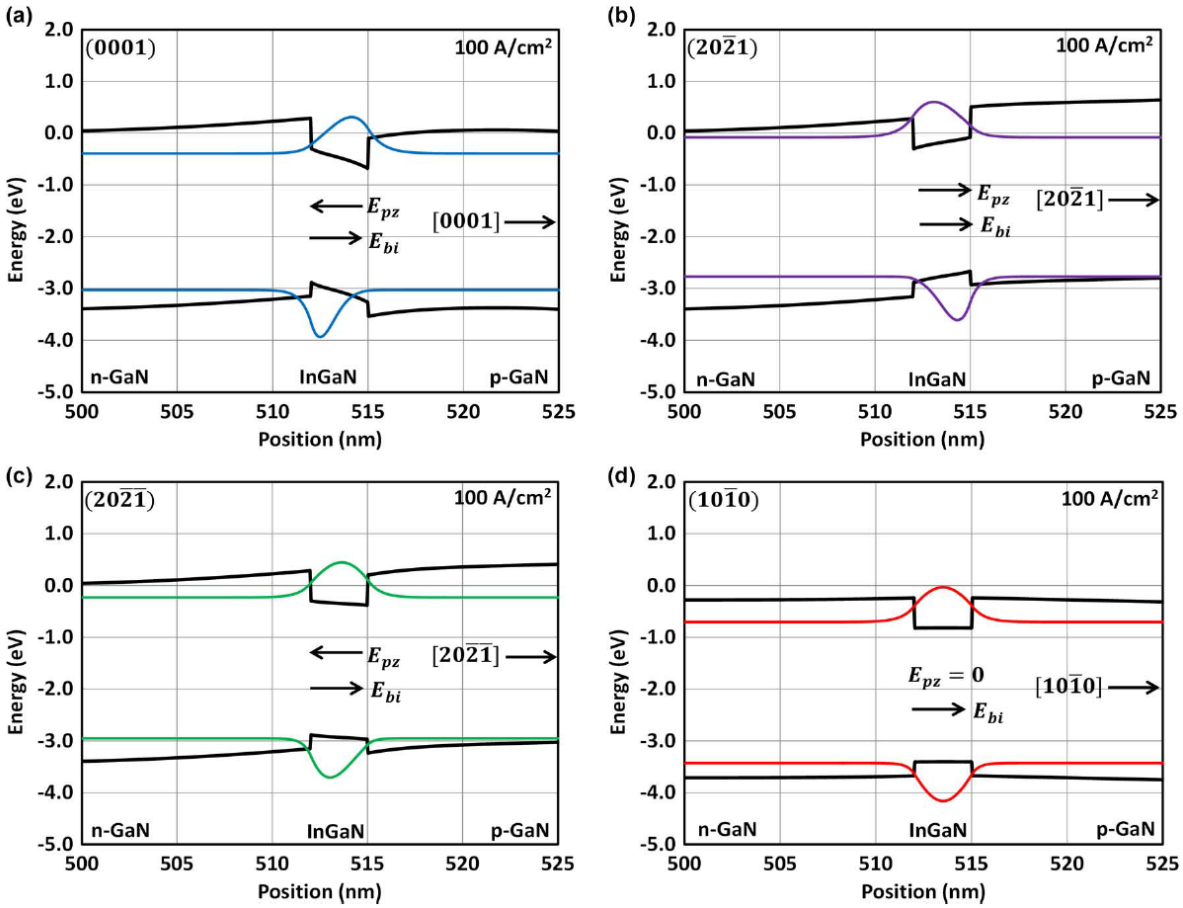


Figure 3. Simulated energy band diagrams for 3 nm InGaN single QWs with GaN barriers at an injected current density of 100 A/cm^2 for (a) polar *c*-plane, (b) semipolar (20$\bar{2}$1), (c) semipolar (20$\bar{2}\bar{1}$), and (d) nonpolar *m*-

plane ($10\bar{1}0$). The ground-state electron and hole wave functions are shown and the directions of the piezoelectric field and p-n junction built-in field are shown.[16] © 2013 IEEE

The relatively strong piezoelectric field in *c*-plane InGaN QWs causes band bending and spatially separates electron and hole wavefunctions, as shown in Figure 3(a). In contrast, the piezoelectric field is reduced for semipolar orientations and completely absent for nonpolar *m*-plane GaN, which results in a relatively flat band structure and greater electron and hole wavefunction overlap (leading to higher radiative efficiency).

The classic argument for utilizing semipolar and nonpolar orientations is to benefit from higher radiative efficiency due to increased electron hole wavefunction overlap, as the bimolecular recombination coefficient, *B*, is proportional to the square of wavefunction overlap.[17] Increasing *B* increases the internal quantum efficiency for LEDs, as described in terms of a rate equation model by

$$\eta_{IQE} = \eta_i \frac{BN^2}{AN + BN^2 + CN^3} \tag{2}$$

where η_{IQE} is the internal quantum efficiency, η_i is the injection efficiency (i.e., the fraction of terminal current that generates carriers in the active region), *N* is the carrier density, *A* is the Shockley-Read-Hall (SRH) recombination coefficient, *B* is the bimolecular (radiative) recombination coefficient, and *C* is the Auger recombination coefficient. However, experimental and theoretical reports suggest that *A* and *C* are also proportional to the square of wave function overlap.[18,19] This suggests that increased wave function overlap does not increase the internal quantum efficiency for a given carrier density.

One notable advantage for semipolar and nonpolar orientations is due to the relationship between carrier density and current density, as described by

$$J = qd \cdot (AN + BN^2 + CN^3) \tag{3}$$

where J is the current density, d is the active region thickness, and q is the electron charge.[16] The higher wavefunction overlap for semipolar and nonpolar orientations increases A, B, and C, so the current density is larger for a given carrier density. This means that for a given current density, the carrier density is lower on semipolar and nonpolar orientations which helps mitigate efficiency droop. Efficiency droop is a significant problem with LEDs at high current densities in which the internal quantum efficiency decreases as the CN^3 term dominates. Because semipolar and nonpolar devices can operate at a relatively low carrier density, they suffer less from efficiency droop and have higher efficiency at high current densities. Furthermore, semipolar and nonpolar orientations enable thicker InGaN QW designs without reduced radiative efficiency and reduced leakage current.[13,16,20]

Here, we mainly focus on homoepitaxy on freestanding nonpolar *m*-plane GaN substrates, which offer several advantages compared to conventional *c*-plane devices. For example, higher peak material gain is predicted for orientations with increasing inclination angle towards *m*-plane.[21–27] This is a consequence of the broken in-plane symmetry for orientations deviating from the *c*-axis that results in an anisotropic strain tensor that also leads to anisotropy in the band structure.[26] Furthermore, the energy separation between the *A1* and *B1* valence subbands increases at the Γ-point for non *c*-plane orientations, as shown in Figure 4 for the valence band structure of 3.5 nm $In_{0.15}Ga_{0.85}N$/GaN QWs on *c*-plane and *m*-plane .

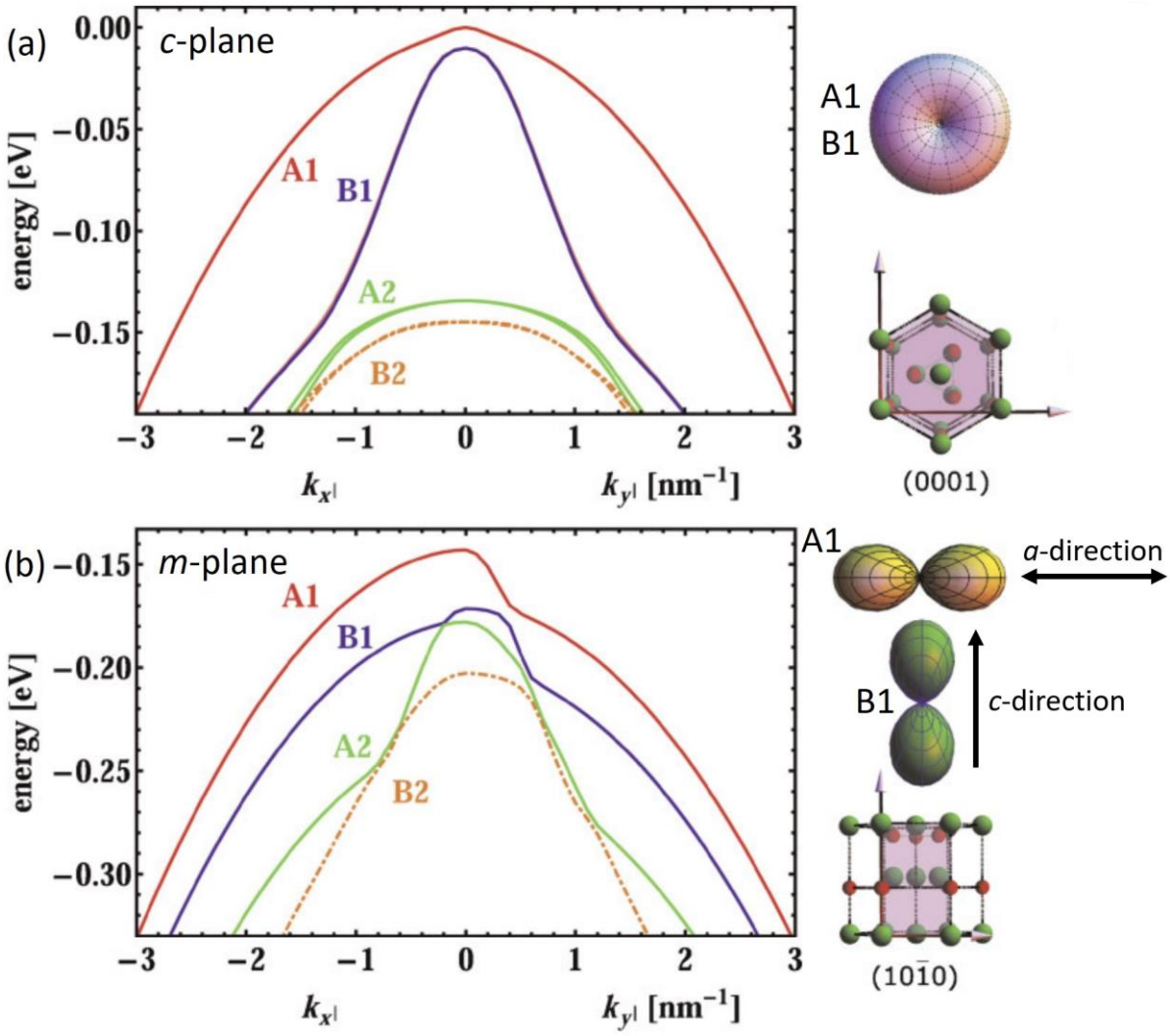


Figure 4. Valence band structure in *k*-space for 3.5 nm $In_{0.15}Ga_{0.85}N$/GaN QWs on (a) *c*-plane and (b) *m*-plane orientations. For non-*c*-plane orientations of the QW, the symmetry for k_x and k_y is lost and the separation in energy between the uppermost *A1* and *B1* valence subbands increases with increasing inclination angle towards *m*-plane. The right side of each graph shows the top-down view of the crystallographic plane and the spherical representations of the *A1* and *B1* valence subbands at the *Γ*-point. These represent the transition strength dependence with angle between the electron *k*-vector and an incident electric field. For *c*-plane, the *A1* and *B1* valence subbands have the same shape due to isotropic strain, which leads to unpolarized emission. For *m*-plane, the anisotropic strain leads to anisotropic shapes: the *A1* subband interacts most intensely with an electric field that is parallel to the *a*-direction, resulting in emission polarized in the *a*-direction, and the *B1* subband has strongest transitions when parallel to the *c*-direction which leads to emission polarized in the *c*-direction.[26] Adapted from [Schade, L., Schwarz, U. T., Wernicke, T., Weyers, M., & Kneissl, M. (2011). Impact of band structure and transition matrix elements on polarization properties of the photoluminescence of semipolar and nonpolar InGaN quantum wells. Physica Status Solidi (B) Basic Research, 248(3), 638–646. https://doi.org/10.1002/pssb.201046350] © 2011 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

The isotropic strain on *c*-plane leads to symmetric valence bands about the *Γ*-point while the anisotropic strain on *m*-plane leads to an asymmetric valence band structure. The right side of

Figure 4 shows the top-down view of the crystallographic planes for *c*-plane and *m*-plane as well as their spherical representations of the *A1* and *B1* valence subbands. The spherical representations of the valence bands represent the transition strength dependence on angle that a carrier interacts with an electric field. For *c*-plane, both the *A1* and *B1* valence subbands have circularly symmetric interaction strengths, which leads to unpolarized emission as the conduction band also has spherical symmetry. However, on *m*-plane, the lattice constants are different in the *c*-direction and *a*-direction, which leads to anisotropic strain.[28] This causes an angular dependence on interaction strength so that the *A1* subband interacts most strongly with an electric field that is parallel to the *a*-direction, which leads to a 100% polarization ratio in the *a*-direction for transitions from the *A1* subband on *m*-plane. Similarly, the *B1* valence subband for *m*-plane aligns in the perpendicular direction, which leads to polarized emission parallel to the *c*-direction for *B1* subband transitions. While the *A2* band contributes to the density of states, transitions from the conduction band to the *A2* band are forbidden by symmetry in the nonpolar QW,[28] so the uppermost *A1* and *B1* valence subbands contribute the most toward radiative carrier recombination. The polarization-dependent emission from *m*-plane QWs is shown in the photoluminescence spectra in Figure 5 that was collected at various linear polarizer angles.

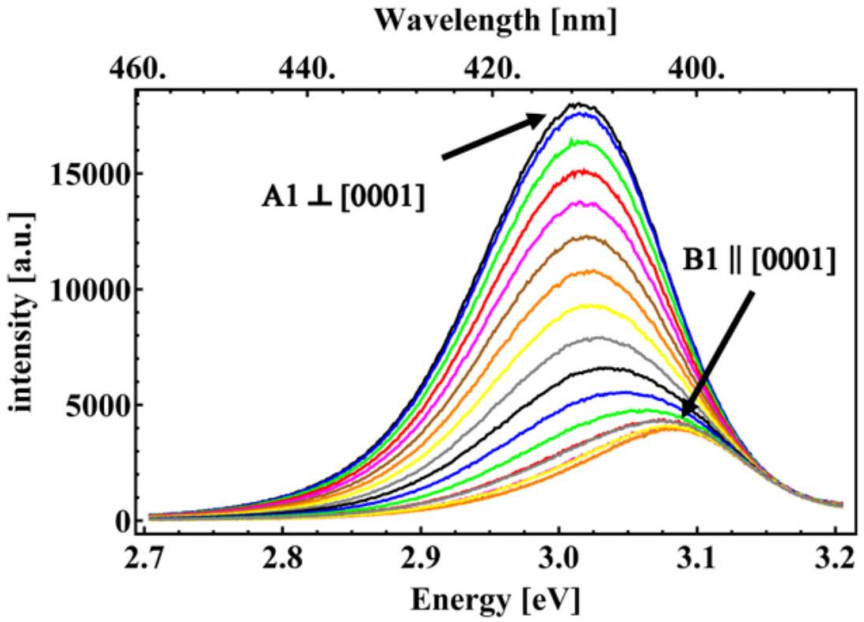


Figure 5. Photoluminescence spectra of a nonpolar *m*-plane QW measured with a linear polarizer that was rotated by 5° between each spectrum. The emission that was polarized in the *a*-direction corresponds to transitions with the *A1* valence subband and the emission polarized toward the *c*-direction corresponded to *B1* transitions. Compared to *A1* transitions, the larger transition energy between the conduction band and the *B1* valence subband resulted in higher energy emission that was blueshifted by 78 meV.[28] Reprinted by permission from [Kneissl, M., Rass, J., Schade, L., & Schwarz, U. T. (2013). Growth and Optical Properties of GaN-Based Non- and Semipolar LEDs BT - III-Nitride Based Light Emitting Diodes and Applications. In T.-Y. Seong, J. Han, H. Amano, & H. Morkoc (Eds.) (pp. 83–119). Dordrecht: Springer Netherlands. https://doi.org/10.1007/978-94-007-5863-6_5]. © Springer Science+Business Media Dordrecht 2013

A linear polarizer was rotated by 5° between each spectrum measurement. The emission was strongly polarized in the direction perpendicular to the *c*-axis (i.e., the *a*-direction), which corresponds to transitions from the conduction band to the *A1* valence band. Transitions to the *B1* valence band were measured by rotating the polarizer by 90° to collect light polarized toward the *c*-direction. Compared to *A1* transitions, the emission was relatively weaker and blueshifted by 78 meV due to the larger transition energy between the conduction band and the *B1* band. The large energetic spacing between *A1* and *B1* valence subbands leads to *m*-plane emission that is predominantly polarized in the *a*-direction with a polarization ratio of 68%.[28] The polarization ratio (i.e., the effective polarization or degree of polarization) is defined as

$$P = \frac{L_{max} - L_{min}}{L_{max} + L_{min}} \quad (4)$$

where L_{max} is the maximum light intensity and L_{min} is the minimum light intensity for emission measured at various polarizer angles.[4] For the emission of QWs on *m*-plane, L_{max} corresponds to light polarized in the *a*-direction and L_{min} corresponds to light polarized along the (0001) *c*-direction. As discussed in later sections, *m*-plane GaN VCSELs uniquely have a polarization ratio of 100% with emission polarized along the *a*-direction.[29,30]

1.1.2. GaN-Based LEDs

While epitaxial GaN films were first grown on sapphire by hydride vapor-phase epitaxy (HVPE) in 1969,[31] it took many years to improve GaN crystal quality, create p-type GaN, grow high-quality InGaN films, and eventually create high-efficiency LEDs. In 1983, S. Yoshida et al. reported improved GaN crystal quality by using MBE to grow AlN buffer layers on sapphire prior to GaN growth,[32] and Amano et al. demonstrated crack-free GaN grown using MOCVD in 1986 using low-temperature AlN buffer layers on sapphire prior to GaN growth.[32] As an alternative to AlN buffer layers, in 1991, S. Nakamura demonstrated high-quality MOCVD-grown GaN by growing a low-temperature GaN buffer layer on sapphire.[33,34] GaN-based LEDs require a p-n junction, but it was very challenging to create p-type GaN. During MOCVD growth, ammonia (NH_3) dissociates and introduces atomic hydrogen into the GaN crystal to form magnesium-hydrogen complexes (Mg-H), which prevent Mg from acting as an acceptor.[35] In 1989, H. Amano et al. created p-type Mg-doped GaN using the low-energy electron beam irradiation (LEEBI) method,[36] and in 1991, S. Nakamura et al. demonstrated a p-n homojunction LED by combining the low-temperature MOCVD GaN buffer layer technique with the LEEBI method for creating p-GaN.[37] However,

the LEEBI method had several restrictions as it required an electron beam, and the highly-doped p-type GaN was limited to a very thin region on the surface. This was solved in 1992 when S. Nakamura et al. demonstrated a post-thermal annealing treatment to create highly doped p-GaN.[38] Unlike the LEEBI method, p-GaN activation by thermal annealing can be performed quickly and simultaneously on multiple samples of any size and has since become the industrial standard process for p-type activation of GaN. After S. Nakamura and T. Mukai reported a breakthrough in MOCVD-grown InGaN films in 1992,[39] S. Nakamura et al. demonstrated the first p-GaN/InGaN/n-GaN double-heterostructure blue LEDs in 1993 that reached a peak output power of 125 μW.[40] Since then, tremendous research has been conducted to improve GaN-based LED performance, such as using p-AlGaN as an electron blocking layer (EBL) to reduce electron overflow past the MQW,[41] improving epitaxial growth of InGaN to produce high-brightness blue, green, and yellow InGaN-based LEDs,[42] and using an indium tin oxide (ITO) current spreading layer to enhance light extraction efficiency.[43]

Breakthroughs in GaN-based LED efficiency have made a significant impact on a global scale, and this was recognized by the 2014 Nobel Prize in Physics that was awarded to Isamu Akasaki, Hiroshi Amano, and Shuji Nakamura "for the invention of efficient blue light-emitting diodes leading to bright and energy-saving white light sources."[44] White light can be obtained by coating a blue LED with a yellow-emitting phosphor. These phosphor-converted blue LEDs have had tremendous improvements over the past decade in terms of efficiency, affordability, high brightness emission, and long device lifetime. While the incandescent lightbulb has a low efficiency of ~16 lumens per watt (~4% efficiency), white LEDs achieve over 300 lumens per watt with a wall-plug efficiency over 50%.[5] With the widespread use of

high-efficiency white LED lightbulbs, it is estimated that by 2030, approximately 261 TWh of electrical energy will be saved.[6] This is an electrical savings of approximately 40% and eliminates the need of more than 30 gigawatt power plants and avoids generating 185 million tons of carbon dioxide.[5] In addition to LED lightbulbs, GaN-based LEDs currently dominate the market for back-illuminated liquid crystal displays (LCDs) in televisions, computer monitors, laptops, mobile phones, and tablets. Future research is being conducted on AlGaN/GaN UV-emitting LEDs that have great potential for water purification because UV light can be used to kill bacteria and other harmful microorganisms.

1.1.3. GaN-Based Edge-Emitting Lasers

Shortly after the breakthroughs in GaN-based LEDs in the early 1990s, S. Nakamura et al. demonstrated the first InGaN-based laser diode in 1996 under pulsed operation,[9] and continuous wave (CW) operation was achieved in 1997.[45] GaN-based laser diodes are very similar to LEDs as they both consist of InGaN MQW active regions located in between a p-n junction. While LEDs emit light due to spontaneous emission, a laser's output is dominated by stimulated emission in which a photon causes an excited electron (i.e., in the conduction band) to drop to a lower energy level (i.e., the valence band) and emit a new photon with an identical phase, frequency, polarization, and direction of travel compared to the original photon. During a population inversion (i.e., empty valence band and filled conduction band states), photons cause stimulated emission in an avalanche effect to produce coherent, monochromatic light. Laser diodes are essentially LEDs that also have an optical cavity with two parallel mirrors that amplify light to create the optical gain necessary for lasing emission. While silver-coated mirrors offer a high reflectance for visible wavelengths, metallic mirrors are usually not suitable for laser diodes because metals inevitably absorb incident light and

produce heat. This would result in a significant amount of loss as light is absorbed during an infinite number of reflections within the cavity. It is important to minimize loss (i.e., internal loss, mirror loss, and scattering loss) because the optical gain needs to overcome the loss in order to reach the threshold for lasing. Therefore, instead of lossy metallic mirrors, GaN-based laser diodes can simply use a smooth GaN/air interface as mirrors because GaN has a relatively high refractive index (n_{GaN} ~ 2.56 at 405 nm) compared to air (n_{air} = 1). These mirrors (also known as laser facets) can be formed by performing a dry etch, such as reactive ion etching (RIE),[9] or they can be formed by cleaving along crystallographic planes to form smooth facets.[46] In addition to the epitaxial layers in LEDs, laser diodes require optical confinement, which can be achieved using epitaxial InGaN and/or AlGaN waveguiding cladding layers for edge-emitting lasers. These waveguiding layers cause a refractive index contrast to confine the optical mode over the gain-producing QW active region.

There have been significant performance improvements in the past two decades, and laser diodes offer several promising advantages compared to LEDs. One problem with LEDs has been efficiency droop in which the efficiency decreases at higher injection levels, and practical operation has generally been limited to low current densities (~ 20-35 A/cm^2).[47] In contrast, GaN-based laser diodes do not suffer from efficiency droop above threshold and have higher power per chip area.[7] This makes GaN-based edge-emitting laser diodes attractive for high-power and directional lighting applications, such as in automobile headlights,[8] and efficacies of 76 lm/W have been obtained.[48] Similar to white LEDs, laser-based white lighting can be produced by using a blue laser that excites a yellow phosphor, as illustrated in Figure 6.

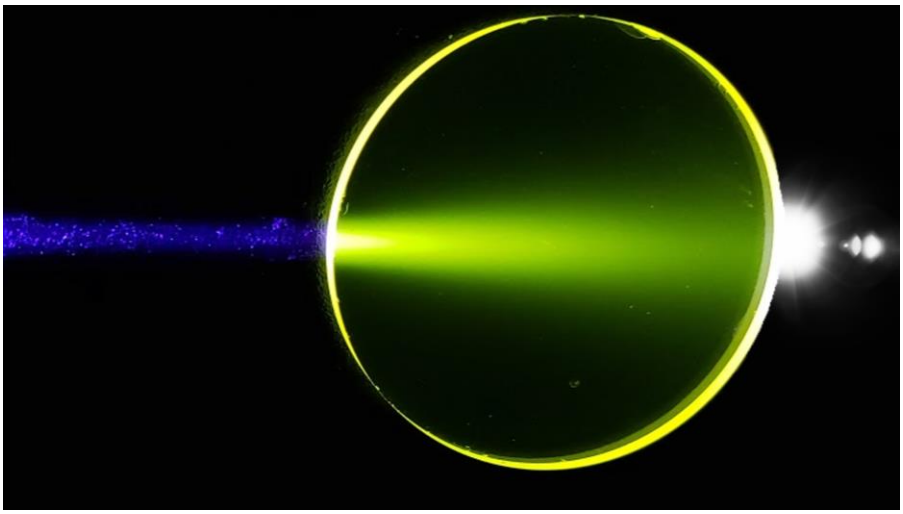


Figure 6. Illustration of how white light can be produced by exciting a yellow phosphor with a blue laser.

Another promising application for GaN-based lasers is high-speed visible light communication (VLC) and light fidelity (Li-Fi) technology. Li-Fi networks use modulated light to send and receive data at rates that are over 100 times faster than Wi-Fi.[49] Laser-based light bulbs are particularly promising because they can provide both illumination and Li-Fi wireless communication because they can be modulated at rates that are imperceptible to the human eye.[50] By utilizing the ubiquitous nature of white light illumination sources, extensive Li-Fi networks can be created with multiple wireless access points. While LEDs typically only have approximately 10 ~ 100 MHz of modulation bandwidth, laser diodes can be modulated at least 100 times faster.[48] For example, a modulation bandwidth of 1.2 GHz from unfiltered white light has been demonstrated by directly modulating a blue GaN edge-emitting laser diode that excited YAG:Ce phosphors,[48] and up to 5 GHz of bandwidth has been attained for a violet GaN edge-emitting laser diode.[51] As further explained later, GaN-based VCSELs are especially promising for this application because they can be modulated at even higher bandwidths.

1.1.4. GaN-Based VCSELs

Compared to LEDs and edge-emitting lasers, GaN-based VCSELs have been relatively difficult to create but offer several unique advantages. While the first blue laser was demonstrated in 1996,[9] it took over a decade longer before the first electrically-injected GaN VCSEL was demonstrated in 2008 by T.-C. Lu et al. at National Chiao Tung University (NCTU).[52] Due to several growth and fabrication challenges, only eight research groups in the world have successfully demonstrated these devices.[3,4,29,30,52–80] One of the many challenges for GaN-based VCSELs has been the formation of high-reflectivity distributed Bragg reflector (DBR) mirrors. DBRs are necessary because VCSELs require mirrors with significantly higher reflectance than edge-emitting lasers. For an edge-emitting laser, the gain path length is relatively long because the active region extends laterally throughout the entire optical cavity, so the threshold for lasing can be achieved with relatively low-reflectivity mirrors. For example, the mirrors for an edge-emitter can simply consist of a GaN/air interface (e.g., etched facet or cleaved facet lasers), which has a reflectance of ~18% due to the index contrast. On the other hand, the active region of a VCSEL only comprises a small layer within the vertical cavity. Consequently, due to the short gain path length in VCSELs, the pair of parallel mirrors need to be significantly more reflective (> 99%) in order to reach the threshold for lasing. This can be achieved using DBR mirrors that consist of multiple periods of alternating quarter-wavelength-thick layers with low and high refractive index. This is relatively easy for GaAs-based VCSELs that can use alternating lattice-matched layers of doped, quarter-wavelength-thick GaAs and AlGaAs to create reflective and electrically conductive epitaxial DBRs. However, epitaxially-grown DBRs have been much more difficult to create for GaN-based VCSELs due to the lattice mismatch of AlGaN/GaN that leads to

cracking. While full epitaxial DBR designs have not been possible, GaN-based VCSELs have either employed two sets of dielectric DBRs or a hybrid design that has a bottom epitaxial DBR. In the hybrid DBR design, researchers at Meijo University have demonstrated a promising epitaxial DBR design that uses lattice-matched and n-type conducting AlInN/GaN, but this design requires relatively long growth times, many mirror periods (~46) due to the low index contrast, and precise thickness control to match the peak reflectance with the lasing wavelength. The more widely-used approach has been to use two sets of dielectric DBR mirrors (i.e., SiO_2/Ta_2O_5) that are relatively easy to deposit using electron beam deposition or sputtering. With a higher index contrast, dielectric DBRs have a much wider high-reflectivity stopband that is easier to align with the lasing wavelength. One difficulty of the dual-dielectric DBR design is being able to deposit DBRs on both sides of the device within a few microns of the active region. This requires more complicated fabrication processes such as flip-chip bonding and growth substrate removal. After highlighting the advantages and applications for VCSELs in Section 1.2, more details about GaN-based VCSEL design are discussed in Section 1.3. Each of the *c*-plane GaN VCSEL designs that have been reported in the literature are summarized in Section 1.3.3, and previously-reported *m*-plane GaN VCSEL designs are outlined in Section 1.3.4.

1.2. VCSEL Advantages and Applications

VCSELs have many useful applications due to their unique combination of sensing and illumination characteristics. Figure 7 shows schematic illustrations and emission profiles for LEDs, edge-emitting lasers, and VCSELs, and several advantages of VCSELs are summarized below.

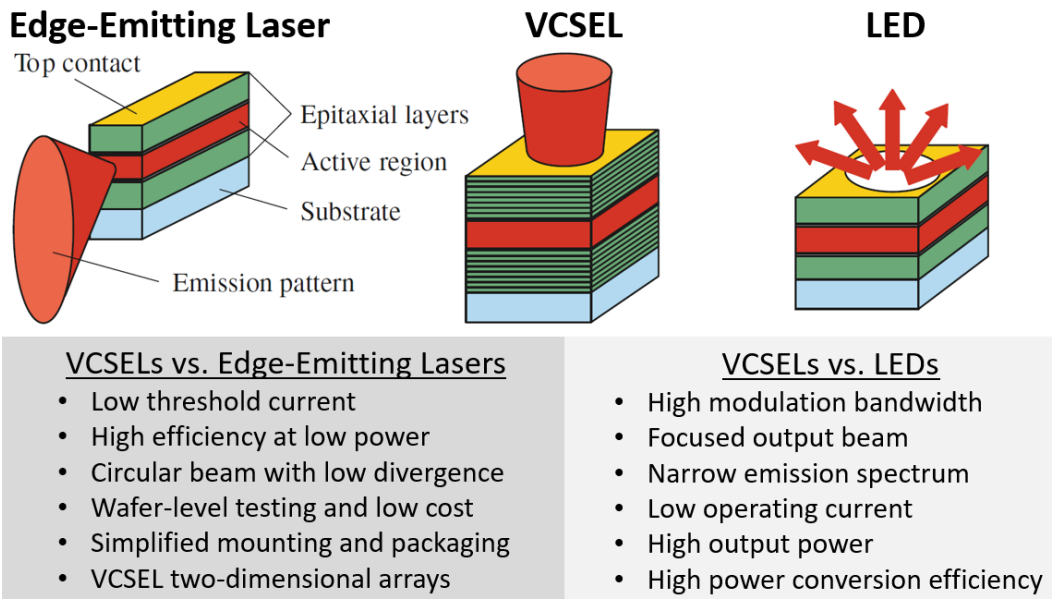


Figure 7. Schematic illustrations of an edge-emitting laser (*left*), VCSEL (*center*), and LED (*right*). Key advantages of VCSELs are summarized compared to edge-emitting lasers (*bottom-left*) and compared to LEDs (*bottom-right*).[1] Reprinted by permission from [Michalzik, R. (2013). *VCSELs: Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers* (1st ed.). Heidelberg: Springer. https://doi.org/10.1007/978-3-642-24986-0]. © Springer-Verlag Berlin Heidelberg 2013

Compared to conventional edge-emitting lasers, VCSELs emit a beam normal to the substrate and are much smaller, which translates into higher modulation speeds that can be used for data communication and a low threshold current that leads to lower power consumption that is ideal for battery-powered devices. The combination of emission normal to the substrate and small device footprint allows VCSELs to be easily arranged into densely-packed 2D VCSEL arrays. While a single VCSEL has a relatively low output power, 2D VCSEL arrays can be easily created and scaled to reach high output powers. Unlike edge-emitting lasers, VCSELs have a circular beam profile with a low beam divergence angle that simplifies the design of beam-shaping optics. VCSELs also have a relatively wide ambient temperature range that enables stable operation even in automobiles. VCSELs can also be tested on the wafer-level, which results in a significant cost reduction compared to edge-emitting lasers. Emission normal to the substrate gives VCSELs another advantage because

well-known LED mounting and packaging technology can be applied to VCSELs. VCSEL emission has very high spectral purity with a narrow spectral width, and VCSELs have the ability for single-mode emission. These unique advantages lead to several applications in illumination, display, communication, and sensing technology.

1.2.1. Red and Infrared VCSEL Applications

Compared to GaN-based VCSELs, GaAs-based infrared-emitting VCSELs have been much more well-developed, with the first CW operating devices reported in the late 1980s[81,82] and commercialized products offered in 1996 by Honeywell.[1] One of the largest markets for VCSELs has been their use as transceivers for data communication through optical fibers. Compared to edge-emitting lasers, VCSELs are ideal for data communication because they can be modulated at much higher speeds and are stable over a larger range of temperatures. Furthermore, VCSELs have lower manufacturing costs because they can be manufactured and tested at the wafer-level while edge-emitting lasers must be cleaved before initial optical testing. VCSELs have a circularly symmetric emission beam with a relatively narrow beam divergence, which simplifies system integration and enables efficient coupling to a multimode optical fiber. These advantages led to low-cost optical interconnects for data communication, and over 18 million 850 nm VCSEL-based transceivers were sold in 2009 with a revenue approaching $500 million.[1] VCSELs have achieved impressive speeds with data rates ranging from 30 Gb/s to 40 Gb/s for VCSELs emitting at 850 nm,[83,84] 980 nm,[85] and 1,100 nm.[86]

Another main application for VCSELs has been in optical video links. Large-screen digital video displays have become increasingly popular in today's world filled with liquid crystal display (LCD) computer monitors, ultra-high-definition televisions, and large venue

projectors. One standard interface for transmitting audio and video data is High-Definition Multimedia Interface (HDMI), but it is difficult to transmit high-resolution video over large distances using traditional copper HDMI cables. For transmitting high-speed and large bandwidths of data, impedance causes signal loss for copper HDMI cables longer than ~15 feet, resulting in digital artifacts and pixelation.[87] As copper interconnect loss is frequency and distance dependent, transmitting modulated laser light using optical fiber is a solution to maintain high data rates over longer distances with significantly lower attenuation. Another interconnect technology is called Thunderbolt, which can transmit data at rates up to 40 Gb/s for Thunderbolt 3. An active copper Thunderbolt cable can transmit data at 40 Gb/s (using dual 20 Gb/s links), but it is limited to a link distance of less than two meters. Using VCSEL technology, an active optical Thunderbolt cable can support a much longer link distance of up to 60 meters.[88] Today, 4K video resolution (i.e., 4096 × 2160 for the movie projection industry and 3840 × 2160 for consumer televisions) is quickly becoming mainstream. The demand for VCSEL optical video links will likely increase as significant interconnect throughput will be required for future 8K (7680 × 4320) video and virtual reality high-resolution displays.

Other than data communication, one of the largest VCSEL markets has been in optical mice. Compared to LED-based optical mice, VCSEL-based products have improved reliability for tracking, simplified optics, and are more efficient which leads to longer battery lifetimes. In general, red LEDs are used in cheaper mice while infrared VCSELs are used in higher-end optical mice. VCSELs are well-suited for tracking displacement and velocity of moving objects (e.g., movements of a computer mouse) because VCSELs can be used as Doppler interferometers that can measure precise displacements via self-mixing interference. As laser light scatters off a moving object, back-scattered light couples into the VCSEL cavity

and creates light intensity modulations that are proportional to the speed of the object.[89] By applying this concept into optical mice, precise tracking can be achieved by placing a photodetector underneath the VCSEL to measure the self-mixing interference.[1,89–91] Compared to edge-emitting lasers, VCSELs are ideal for this application because they can provide single longitudinal and lateral mode emission, which avoids signal distortions from mode beatings.[1,89] Doppler interferometry systems also enable several other applications, such as motion tracking of finger movements for menu navigation,[1,89] onboard velocity measurements for automotive applications,[92] measuring blood and liquid flow rates in human tissue,[93] and in proximity sensors for detecting range.[94]

Unlike edge-emitting lasers, VCSELs can be easily arranged into densely-packed 2D arrays, which has led to improved image quality and higher speed for laser printers. After eight years of research on VCSEL arrays, Fuji Xerox Co. launched the first VCSEL array-based laser printer (DocuColor 1256 GA) in 2003, which is the highest reported resolution in the printing industry with 2400 dots per inch (dpi) resolution.[95] While this model printed at a speed of 50 pages per minute,[95] as of 2016, VCSEL-based laser printers from Fuji Xerox have reached speeds up to 137 pages per minute while maintaining 2400 dpi resolution.[96] These printers use a 780 nm single-mode 8×4 VCSEL array to emit modulated light that contains the image information toward a rotating polygon mirror, which scans the beam through a lens that focuses the light across the photoconductor to create an electrostatic latent image.[95] The final image is printed as charged toners electrostatically attach to the photoconductor and then thermally or mechanically transfer to the paper.[96] Some of the main goals for printing technology are to improve the printed image quality and speed. One way to increase the resolution and printing speed is to increase the rotational frequency of the polygon mirror, but

this has practical limits. For example, a high resolution of 2400 dpi at a printing speed of 500 mm/s would not be possible with a single laser beam because polygon mirrors are not capable of rotating at speeds near 230,000 rpm.[1] Other than increasing the polygon mirror rotational frequency, another way to increase resolution and printing speed is to use multiple laser beams.[95] While edge-emitting lasers can be used for this application, VCSELs are more suitable because it is relatively easy to create a larger number of laser beams using 2D VCSEL arrays.[96] A VCSEL emission wavelength of 780 nm was chosen based on the high sensitivity at that wavelength for the phthalocyanine pigment organic photoconductor, and a Gaussian-like beam profile with a single transverse mode is desired because multimode beam profiles are difficult to focus, which directly affects the image profile.[95]

Recently, there has been rising demand for VCSEL technology as Apple has included VCSELs in the iPhone X for three-dimensional (3D) depth sensing. As a replacement for the fingerprint-based TouchID system, the TrueDepth system creates a 3D depth map to check for a facial identity match to securely unlock the device. Based on an imaging report by S. Hallereau, the TrueDepth system uses an infrared VCSEL, folded optic, and an active diffractive optical element to shine 30,000 dots of light onto the user's face.[97] An infrared camera captures the image of the dots and based on the density of the dots, a 3D depth map is created.[98] The system works quickly so users can track their faces in real-time and map their expressions onto virtual avatars. 3D sensing has many other applications; for example, the Microsoft Kinect uses 3D sensing, so users can interact with the game console without the need for a game controller. VCSEL-based 3D sensing is promising as it can apply this concept to extend the capabilities of future electronics. With Apple Inc. awarding Finisar Corp. $390 million in December 2017 for research and development of VCSELs,[2] future devices will

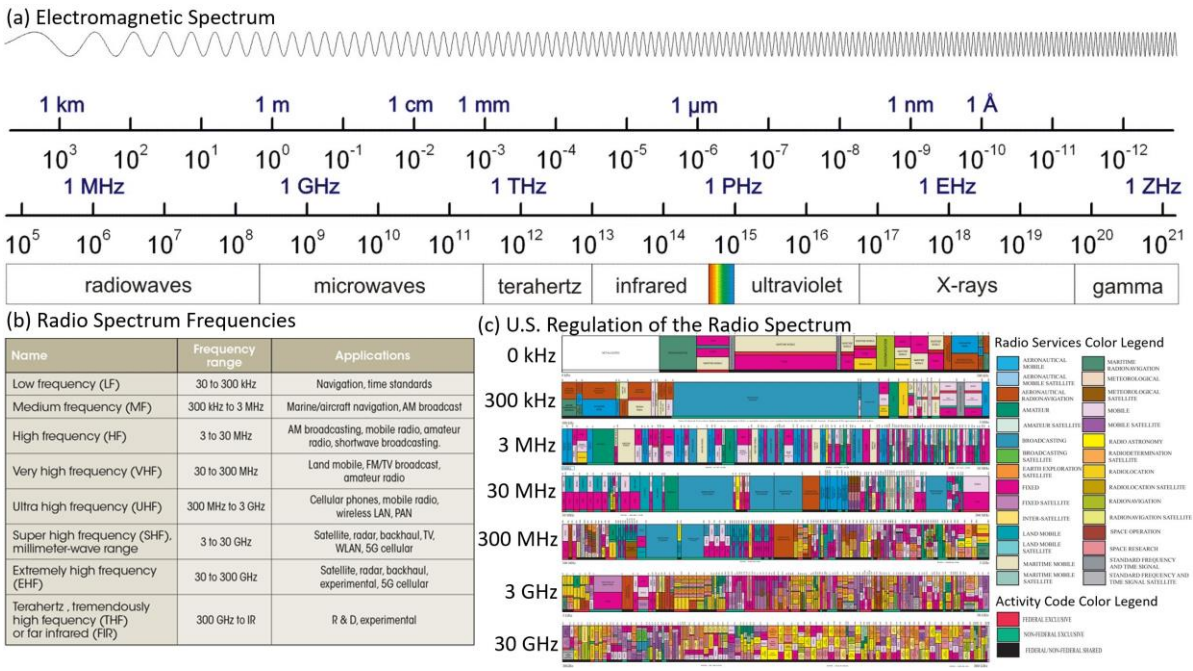
likely employ VCSEL-based technology and enable a whole new range of applications and ways to interact with devices.

1.2.2. GaN-Based VCSEL Applications

While the VCSEL market is currently limited to red and infrared emission, GaN-based VCSELs enable shorter wavelength emission from violet to green, which enables novel applications in display, data communication, illumination, and sensing technology. Projector and display technology are particularly promising applications for GaN-based VCSELs due to several features, such as their high beam quality with circular emission profile and low divergence angle. Full-color light sources for displays could be created by pairing blue and green GaN-based VCSELs with red AlGaInP-based VCSELs. With relatively low threshold currents, VCSELs have a low power consumption, which is especially important for battery-powered devices. This makes GaN-based VCSELs promising for portable devices such as laser pico-projectors and in augmented reality headsets that could have a similar form factor as Google Glass. Because VCSELs emit a coherent, highly directional, and circular beam profile with low divergence, they are also excellent candidates for displays and projectors that use diffractive optics technology,[99] which is promising for augmented reality headsets and heads-up displays.

Laser-based white lighting using a GaN-based blue laser to illuminate a phosphor is a promising alternative to LEDs in order to avoid efficiency droop and to obtain higher power per chip area.[7] While edge-emitting lasers are suitable for this application, GaN-based VCSELs offer several advantages as illumination sources. Similar to LEDs, VCSELs emit light normal to the substrate, making it easier to integrate VCSELs with existing LED infrastructure. While a single VCSEL has a relatively low output power, multiple VCSELs

can be easily arranged into densely-packed 2D VCSEL arrays that can produce much higher output powers. This gives the advantage of scalability, in which a desired output power can be obtained by adjusting the number of VCSELs within the array. Furthermore, VCSELs can be screened and tested on-wafer, which leads to lower production costs.[1] GaN-based VCSELs are also promising for high-speed VLC and Li-Fi technology. While 5 GHz of bandwidth has been achieved for a violet GaN edge-emitting laser diode,[51] GaN-based VCSELs have the potential for even higher modulation bandwidths due to their smaller active region volume.[100] In addition to higher data transfer speeds, VLC is attractive because it is not regulated by the Federal Communications Commission (FCC) and does not require a spectrum license. Conventional communication using radio frequencies requires a spectrum license for broadcasting at most business radio frequencies. The frequency and wavelength ranges for the electromagnetic spectrum are shown in Figure 8(a), and Figure 8(b) shows definitions and applications for various ranges of radio frequencies.



Name	Frequency range	Applications
Low frequency (LF)	30 to 300 kHz	Navigation, time standards
Medium frequency (MF)	300 kHz to 3 MHz	Marine/aircraft navigation, AM broadcast
High frequency (HF)	3 to 30 MHz	AM broadcasting, mobile radio, amateur radio, shortwave broadcasting.
Very high frequency (VHF)	30 to 300 MHz	Land mobile, FM/TV broadcast, amateur radio
Ultra high frequency (UHF)	300 MHz to 3 GHz	Cellular phones, mobile radio, wireless LAN, PAN
Super high frequency (SHF), millimeter-wave range	3 to 30 GHz	Satellite, radar, backhaul, TV, WLAN, 5G cellular
Extremely high frequency (EHF)	30 to 300 GHz	Satellite, radar, backhaul, experimental, 5G cellular
Terahertz , tremendously high fequency (THF) or far infrared (FIR)	300 GHz to IR	R & D, experimental

Figure 8. (a) Wavelength and frequency for the electromagnetic spectrum from radio waves to gamma rays,[101] (b) radio spectrum frequencies and applications,[102] and (c) United States regulation chart of the radio spectrum.[103]

As shown in Figure 8(c), the FCC regulates a large range of frequencies that are reserved for military purposes or auctioned for private or commercial use. There are certain frequencies that are unlicensed, such as frequencies used for Wi-Fi, but existing bands are becoming highly congested as there has been a large increase in the Internet of Things (IoT) devices (i.e., devices connected to the internet), and it has been predicted that there will be up to 50 billion connected devices by 2020.[104] VLC opens the door to a larger range of unregulated visible frequencies for high-speed data communication and also offers enhanced security. For example, relatively long-wavelength Wi-Fi signals can transmit through walls, which gives hackers an opportunity to enter the network even if they are outside the building. On the other hand, VLC requires a direct line of sight between the emitter and detector, giving the network an extra layer of security. VCSELs also have several applications that use their unique ability to act as sensors, such as in 3D depth sensing using the time of flight method,[105] self-mixing interferometry,[106] and in VCSEL-based biosensing applications.[107] GaN-based VCSEL performance has rapidly improved over the past decade, and they will soon be commercially viable, enabling new and innovative future technologies.

1.3. GaN-Based VCSEL Design

This section describes the main factors and objectives during the design of GaN-based VCSELs. The fundamentals of laser diode design are described in Section 1.3.1 and VCSEL design goals are discussed in Section 1.3.2. Section 1.3.3 outlines the *c*-plane GaN-based VCSEL designs that have been reported from companies and research institutions, and Section 1.3.4 describes *m*-plane GaN-based VCSEL designs that were created at UCSB.

1.3.1. Fundamental Laser Design

This section summarizes the fundamentals of laser design, which applies to both edge-emitting laser diodes and VCSELs. Specific design goals for VCSELs are discussed in Section 1.3.2. Lasers consist of an optical gain medium (i.e., active region for light amplification) within a resonant optical cavity (e.g., two parallel mirrors). The optical gain medium is similar to the light-emitting active region of an LED (e.g., InGaN/GaN MQW) that absorbs light over a certain wavelength range but can also be *pumped* with electrical or optical energy to emit light via electroluminescence and photoluminescence, respectively. Light traveling within an unpumped optical cavity is absorbed within the active region, but with sufficient electrical or optical pumping, light can be amplified to produce optical gain through stimulated emission. Once the optical gain sufficiently overcomes the optical losses in the cavity, the threshold for lasing is reached and relatively coherent light will be emitted. The threshold current can be identified based on the *kink* (i.e., sharp increase in slope) in the light output power versus current (*L*-*I*) characteristic, as shown in Figure 9.

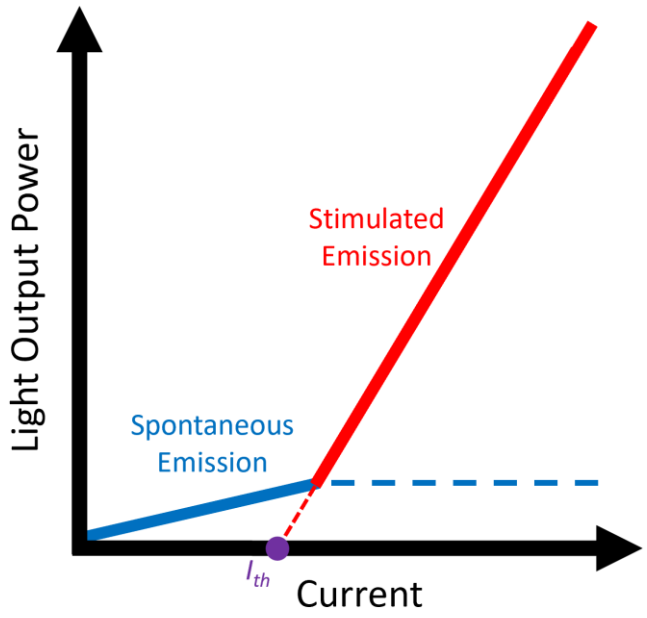


Figure 9. Illustration of light output power versus current for a diode laser. Below the threshold current, I_{th}, spontaneous emission dominates. Above threshold, the light output power from stimulated emission increases while the spontaneous emission is clamped at the threshold value.

Below threshold, the light output power is dominated by spontaneous emission as the gain has not yet overcome the total loss of the cavity. Above threshold, the carrier density clamps (i.e., remains constant) at its threshold value, which causes the gain and spontaneous emission to clamp as well. Every additional injected carrier into the active region above threshold produces a photon in the lasing mode and the slope of the *L-I* curve increases abruptly as stimulated emission begins to dominate.

Minimizing the threshold current is a key goal for laser design and can be accomplished by reducing the total amount of optical loss within the cavity. The main sources of optical loss for a laser diode consist of internal loss, scattering loss, and mirror loss. Internal loss is due to optical absorption within the various materials within the cavity, such as free carrier absorption,[108] and the absorption coefficient of a material can be calculated, as described by

$$\alpha = \frac{4\pi k}{\lambda} \tag{5}$$

where α is the absorption coefficient, k is the extinction coefficient (i.e., the imaginary part of the complex refractive index), and λ is the wavelength. Scattering loss accounts for the light that is radiated out of the mode due to scattering at interfaces or due to surface roughness. Scattering loss is proportional to surface roughness and inversely proportional to wavelength, as described by

$$\beta = 1 - e^{-\left(\frac{4\,\pi\,\sigma\cos(\theta_i)}{\lambda}\right)} \tag{6}$$

where β is the percentage of scattering loss, σ is the root-mean-square (RMS) roughness of the surface, θ_i is the angle of incidence, and λ is the optical wavelength.[109–111] The mirror loss depends on the cavity length and mirror reflectance, as described by

$$\alpha_m = \frac{1}{L_{eff}} \ln\left(\frac{1}{\sqrt{R_1 R_2}}\right) \tag{7}$$

where α_m is the mirror loss, L_{eff} is the effective cavity length, R_1 is the reflectance of the first mirror, and R_2 is the reflectance of the second mirror. The threshold material gain, g_{th}, is the total gain of the active region (e.g., InGaN MQW) that is required to reach threshold. For lasers with poor quality active regions, low optical confinement, or large total amounts of loss, the threshold material gain may be unobtainable, which would result in the laser failing to lase. If the optical gain equals the total loss of the cavity, the threshold for lasing occurs. This condition is described by the threshold modal gain, Γg_{th}, which is defined as

$$\Gamma g_{th} = \alpha_i + \alpha_m + \alpha_s \tag{8}$$

where Γ is the confinement factor, g_{th} is the threshold material gain, α_i is the internal loss, α_m is the mirror loss, and α_s is the scattering loss. The threshold for lasing can be reduced by maximizing the confinement factor and minimizing the total loss of the cavity (i.e., α_i, α_m, and α_s). The confinement factor describes the degree of overlap between the active region volume and the cavity volume occupied by photons. This is important because photons are necessary to stimulate electron-hole pairs to recombine and produce optical gain, but the volume of the active region occupied by electrons is much smaller than the cavity volume occupied by photons, which decreases the photon generation rate based on the confinement factor (i.e., active region volume divided by cavity volume occupied by photons). In an edge-emitting laser, optical confinement in the axial direction (i.e., along the length of the laser bar)

is accomplished by reflections at the mirror facets. It is also important for the laser to have optical confinement in the remaining two perpendicular directions (i.e., laterally and transversely). This can be accomplished in a similar fashion as optical confinement in an optical fiber that consists of a core material with a high refractive index surrounded by lower-index cladding material, so light travels along the core of the fiber and can have total internal reflection within the core for incident light at or below the critical angle. Without sufficient index contrast between the core and cladding, the critical angle decreases and incident light greater than that angle can escape the optical fiber through the cladding. Therefore, sufficient index contrast is important for fiber optic waveguides and similarly applies to lasers for optical confinement. In an edge-emitting laser, lateral optical confinement (i.e., along the width of the laser bar) is commonly achieved by etching the device into a rectangular-shaped laser bar to form a ridge waveguide, which provides a large index contrast at the semiconductor/air interface. Transverse confinement (i.e., along the direction of epitaxial growth) can be achieved by sandwiching the high-index active region (e.g., InGaN/GaN MQW) in between epitaxially-grown layers of lower refractive index (e.g., lower composition InGaN) to form a separate confinement heterostructure (SCH), which is surrounded by cladding layers (e.g., GaN and/or AlGaN). It is helpful to note that refractive index, n, is inversely proportional to band gap, E_g, so $n_{InGaN} > n_{GaN} > n_{AlGaN}$ and $E_{g,InGaN} < E_{g,GaN} < E_{g,AlGaN}$. Achieving effective optical confinement is necessary for any type of laser, and the threshold can be reduced by increasing the confinement factor. As discussed later in Section 1.3.2, optical confinement for VCSELs is particularly important and can even offer higher confinement factors compared to edge-emitting lasers.

In addition to reducing the threshold current, another common goal in laser design is to increase the differential quantum efficiency which enables higher output powers at a given current. Differential efficiency is defined as the number of photons emitted from the device per injected electron and is proportional to the slope of the measured light output power versus current (*L*-*I*) characteristic above threshold, as described by

$$\eta_d = \left[\frac{q}{h\nu}\right]\frac{dP}{dI} \approx \frac{\lambda}{1240}\frac{dP}{dI} \tag{9}$$

where η_d is the differential efficiency, q is the charge of an electron, h is Planck's constant, ν is the frequency of light, dP/dI is the derivative of the *P*-*I* characteristic (note that the light output power can be denoted as either *L* or *P*), and λ is the wavelength in nanometers.[17] While it is important to minimize internal loss and scattering loss, the optimal amount of mirror loss varies based on the intended properties of the laser because mirror loss also accounts for the useful light that escapes through the mirrors. Therefore, it is sometimes advantageous to use lower reflectivity mirrors to increase the mirror loss and increase the fraction of light that couples out of the mirror, as described by

$$F_1 = \frac{1 - R_1}{(1 - R_1) + \frac{R_1}{R_2}(1 - R_2)} \tag{10}$$

where F_1 is the fraction of light that couples out of one mirror, R_1 is the reflectance of the first mirror, and R_2 is the reflectance of the second mirror. Reducing the mirror reflectance increases α_m and F_1, which leads to higher differential efficiency, as described by

$$\eta_{d1} = F_1\eta_i\frac{\alpha_m}{\Gamma g_{th}} \tag{11}$$

where $\eta_{d1}$is the differential efficiency from one mirror, F_1 is the fraction of light that couples out of one mirror, η_i is the injection efficiency (i.e., the fraction of terminal current that

generates carriers in the active region), α_m is the mirror loss, Γ is the confinement factor, and g_{th} is the threshold material gain.

With the goals of minimizing threshold current and maximizing differential efficiency, there is a trade-off in terms of the optimal mirror loss, as illustrated in Figure 10.

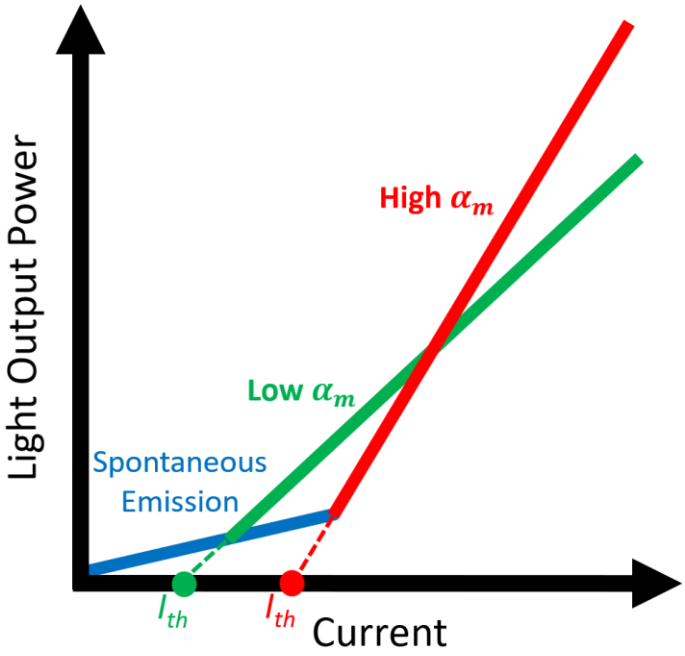


Figure 10. Schematic illustration of light output power versus current for lasers with different values of mirror loss (α_m) due to varying values of mirror reflectivity. As shown for the green curve, a laser with relatively low α_m (e.g., mirrors with relatively high reflectance) leads to a lower threshold current (I_{th}), but the slope of the *L*-*I* curve is lower due to lower differential efficiency (η_d) and leads to a lower peak output power. The red curve illustrates a laser with a relatively high α_m (e.g., mirrors with relatively low reflectance) that leads to a higher I_{th}, higher η_d, and higher peak output power. Note that although not shown, the spontaneous emission for the green curve should clamp at threshold.

While using lower reflectivity mirrors to increase the mirror loss can improve the differential efficiency, it has the disadvantage of increasing the threshold for lasing, as illustrated by the red curve in Figure 10. The optimal mirror loss depends on the intended application for the laser. For example, if a low threshold is more important than higher output power, this could be achieved using high-reflectivity mirrors to decrease the mirror loss and reduce the threshold, as illustrated by the green curve in Figure 10. For edge-emitting lasers, one solution to this trade-off is to use a high-reflection (HR) coating for one mirror and an anti-reflection

(AR) coating on the other facet. This is useful for applications that only need a beam emitted from one direction as the HR coating helps reduce the threshold while the beam emits most strongly through the facet with the AR coating with a high differential efficiency. Although VCSELs require HR coatings for both mirrors, a similar concept can be applied by slightly reducing the reflectivity of the mirror on the intended side of beam emission.

1.3.2. Overview of VCSEL Design

VCSELs share many of the common design goals as edge-emitting lasers, such as minimizing the threshold and maximizing output power, but there are several additional design considerations that greatly affect performance. These are mainly a result of the significant differences in the geometry of the two designs. Compared to edge-emitting lasers, VCSELs emit laser beams vertically from the uppermost surface and are much smaller with a shorter cavity length. Figure 11 shows a schematic illustration of a VCSEL.

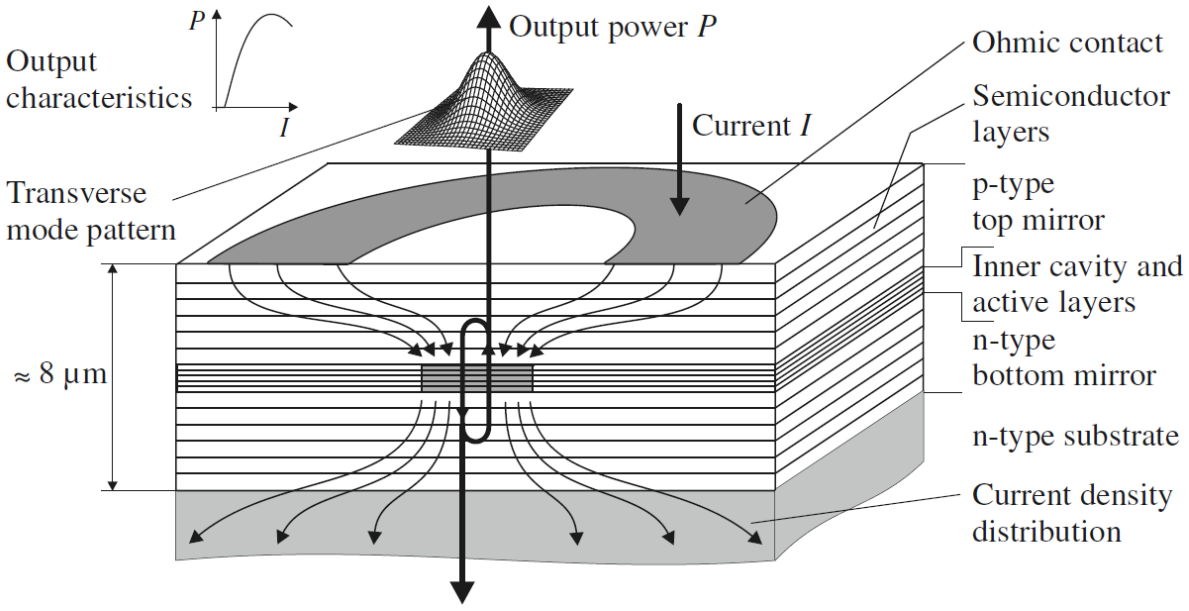


Figure 11. Schematic illustration and operating principle of a VCSEL.[1] Reprinted by permission from [Michalzik, R. (2013). *VCSELs: Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers* (1st ed.). Heidelberg: Springer. https://doi.org/10.1007/978-3-642-24986-0]. © Springer-Verlag Berlin Heidelberg 2013

While edge-emitting lasers have cavity lengths on the order of ~1 mm, VCSELs have cavity lengths on the order of ~1 μm. Another important difference is the geometry of the active region within the cavity. The InGaN/GaN MQW active region can span along the entire length of the cavity for an edge-emitting laser, but the active region only occupies a very small fraction of the total cavity length for a VCSEL. These geometrical differences cause several challenges during VCSEL design but also lead to unique advantages.

1.3.2.1. DBR Mirror Design

In order to emit a laser beam vertically, VCSELs require bottom and top mirrors that are parallel to the substrate. While edge-emitting lasers can use a relatively simple GaN/air interface for the mirrors, VCSELs require mirrors with much higher reflectance values over 99% because of the relatively short gain path length within the cavity. This complicates the VCSEL fabrication process, but it can be accomplished using distributed Bragg reflectors (DBRs) that consist of several periods of quarter-wavelength-thick alternating layers of high and low refractive index. There are three main types of DBR designs: epitaxial DBRs, dielectric DBRs, and air-gap DBRs. While air-gap DBRs have been demonstrated for InP-based VCSELs[112] and III-nitride air-gap DBRs have been fabricated,[113–115] only dielectric and epitaxial DBRs have been used for GaN-based VCSELs. Reported GaN-based VCSELs have used dielectric DBRs for the top mirror (e.g., SiO_2/Ta_2O_5), and the bottom mirror has either consisted of a dielectric DBR or an epitaxially grown DBR (e.g., AlGaN/GaN).

GaN-based VCSELs with a hybrid DBR design (i.e., epitaxial DBR on the bottom side and dielectric DBR on the top side) are significantly easier to fabricate because flip-chip bonding and substrate removal are not required. However, it is very difficult to grow high-

quality epitaxial DBRs with the necessary high reflectance. One challenge is that there is very low index contrast between AlGaN and GaN, so many mirror periods are necessary to reach the target reflectance. Furthermore, AlGaN and GaN have different lattice constants, so an increasing amount of strain builds up with each added AlGaN/GaN mirror period in the DBR and typically leads to cracking and defects. Despite these challenges, GaN-based VCSELs with epitaxially grown AlGaN/GaN DBRs have been reported,[52] and crack-free AlN/GaN DBRs have been created by incorporating strain-relieving AlN/GaN superlattices into the DBR.[52] Lastly, another challenge is that the DBRs need to be precisely spaced apart at the designed cavity length, as described in Section 1.3.2.2.

1.3.2.2. Optical Cavity Design

Precise control of layer thicknesses and cavity length is very important for VCSELs because it affects the resonant modes, gain enhancement factor, and electric field standing wave within the cavity. A VCSEL consists of an optical cavity formed by two parallel mirrors, also known as a Fabry-Perot etalon, and constructive interference occurs at certain wavelengths of light. The longitudinal mode spacing (i.e., the spacing between resonance wavelengths) is inversely proportional to the cavity length, as described by

$$\Delta\lambda = \frac{\lambda^2}{2\, L_{eff}\, \bar{n}_g} \tag{12}$$

where $\Delta\lambda$ is the Fabry-Perot longitudinal mode spacing, λ is the lasing wavelength, L_{eff} is the effective cavity length, and $\bar{n}_g$ is the effective group index.[1] The effective cavity length of a VCSEL is actually longer than the distance between the mirrors because the mode penetrates into the DBRs, which can be defined as an effective penetration length. The refractive index, *n*, is an important material parameter that describes several optical phenomena, such as

reflection, refraction, and diffraction at optical interfaces. For instance, the wavelength of light in a material is *n*-times smaller than the wavelength in a vacuum. Similarly, dividing the speed of light by *n* gives the speed of light within the material (e.g., $n = 1$ for a vacuum, and $n \sim 2.6$ for GaN at a 405 nm wavelength). Because the refractive index varies based on the wavelength of light, this only gives the phase velocity at one particular wavelength. This wavelength-dependence of refractive index manifests as chromatic dispersion wherein different colors of light travel at different velocities within a material, and a familiar example of this is rain separating white light into a rainbow of colors. While refractive index only gives the phase velocity at a single wavelength, the group velocity accounts for index dispersion and applies to a packet of waves that cover a certain range of wavelengths. The group velocity describes the speed of the envelope of a propagating wave and has a corresponding group index, as defined as

$$n_g = n - \lambda \frac{\partial n}{\partial \lambda} \tag{13}$$

where n_g is the group index and n is the refractive index at a particular wavelength, λ. In the normal dispersion regime for semiconductors, the refractive index decreases with increasing wavelength (i.e. $\partial n/\partial \lambda < 0$), so the group index is typically approximately 20-30% larger than the refractive index and depends on the wavelength relative to the band edge.[17] Because n_g only applies to a single material, it is useful to define an effective group index, $\bar{n}_g$, as used in Equation (12). This is helpful to describe VCSELs as they consist of various materials of varying refractive indices and index dispersion profiles. An experimentally measured group index dispersion profile for an $In_{0.15}Ga_{0.85}N$ edge-emitting laser diode emitting at a wavelength of 403.5 nm is shown in Figure 12.

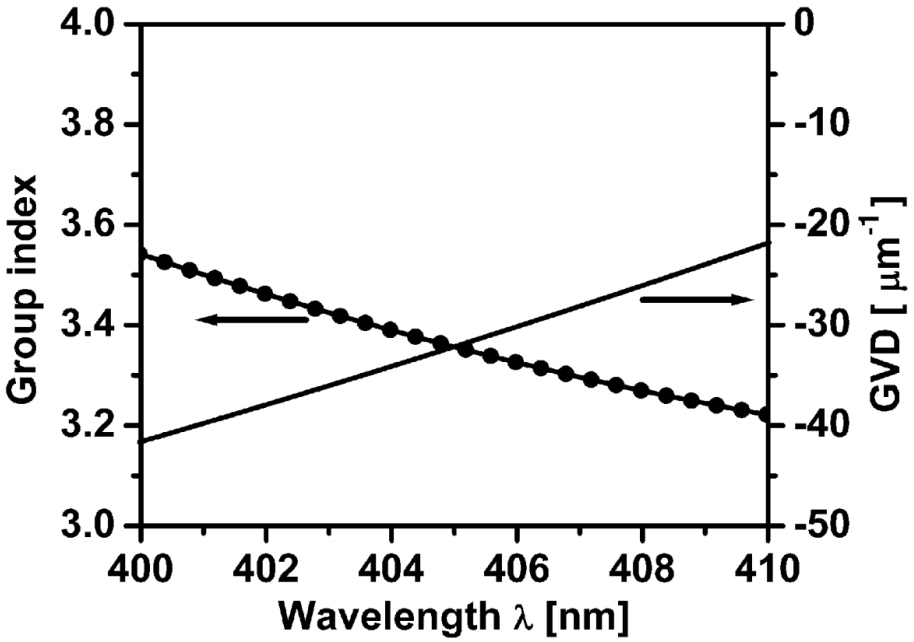


Figure 12. Measured group index and group velocity dispersion (GVD) ($\partial n_g/\partial\lambda$) for an InGaN MQW edge-emitting laser diode biased at a current of 30 mA.[116] Reprinted with permission from [Gan, K. G., & Bowers, J. E. (2004). Measurement of gain, group index, group velocity dispersion, and linewidth enhancement factor of an InGaN multiple quantum-well laser diode. *IEEE Photonics Technology Letters*, *16*(5), 1256–1258. https://doi.org/10.1109/LPT.2004.826003]. © IEEE 2004

By using this data to approximate the group index dispersion for violet-emitting GaN-based VCSELs ($n_g \sim 3.35$ at a wavelength of 405 nm), the longitudinal mode spacing is ~20.4 μm for an effective cavity length of 1.2 μm, as calculated by Equation (12). This corresponds to an optical cavity length of ~ 7λ based on a calculated effective index of 2.35 within the VCSEL cavity. GaN-based VCSELs with effective cavity lengths of ~7λ or less have been mostly reported from academic groups, such as UCSB (6.95λ – 7.5λ),[3,4,29,30,58,65] National Chiao Tung University (5λ – 7λ),[52,78] École polytechnique fédérale de Lausanne (7λ),[80] and Meijo University (4λ – 4.5λ).[60,66] Cavity lengths of ~23λ and longer (mode spacing ~6 nm and lower) have been reported mainly by industry groups, such as Nichia (~23λ),[77,79] Panasonic (~35λ),[53,54] and Sony (~23λ).[57,61–63] Short cavity lengths can be used to obtain single longitudinal mode emission due to the large mode spacing, but there can be issues with poor thermal performance and alignment of a resonance mode with the gain spectrum.

In a laser, the peak gain wavelength (determined by the active MQW) needs to align with a resonance mode within the cavity. This is trivial for an edge-emitting laser because the long cavity length results in a very small resonance mode spacing, so the peak gain always aligns with a resonance mode and provides multi-longitudinal mode operation. However, it becomes a problem for VCSELs due to the short cavity length that leads to a much larger resonance mode spacing. Misalignment of the peak gain wavelength with a resonance mode could prevent lasing, so precise cavity length control is very important for VCSELs. Optical simulations can be performed during VCSEL design of the cavity length to tune the resonance mode to a desired wavelength that aligns with the peak gain wavelength. Alignment is further complicated because the peak gain wavelength is not always constant. For example, at higher injection levels, the peak gain spectrum can redshift due to heating. If a resonance mode is aligned to the peak gain at low junction temperatures, a low threshold can be obtained, but the maximum peak output power would be reduced as the peak gain redshifts away from the lasing wavelength at higher injection levels. Although the threshold will increase, a higher output power can be achieved by intentionally designing the VCSEL with a longer-wavelength resonance mode, so perfect alignment occurs at higher injection levels. Therefore, the optimal alignment (also described by the gain offset factor) depends on the desired operating conditions of the device. The resonance wavelengths within the cavity can be found by using the transmission matrix method (TMM) to simulate the reflectance of the VCSEL structure. The resonance modes correspond to the reflectance null wavelengths of the simulated reflectance spectrum. While a single DBR has a high-reflectivity stopband (e.g., range of wavelengths with a high reflectivity), a VCSEL contains two DBRs separated by a cavity length, which causes sharp dips in the measured reflectance at the resonant frequencies

within the cavity. Note that while it is easy to view the resonance wavelengths using reflectance simulations, experimental measurement is much more difficult. The dips in the reflectance at the resonance wavelengths have a very narrow line-width for VCSELs, so it would require an extremely high-resolution spectrometer with a small spot size that could be accurately aligned within the VCSEL aperture.

Another key design goal for VCSELs is to maximize the gain enhancement factor, which uniquely enables VCSELs to have a confinement factor up to two times greater than edge emitting lasers. The gain enhancement factor plays a large role in the confinement factor, Γ, for a VCSEL, as described by

$$\Gamma = \Gamma_{fill}\Gamma_{xy}\Gamma_{enh} \tag{14}$$

where Γ_{fill} is the fill factor, Γ_{xy} is the lateral confinement factor, and Γ_{enh} is the enhancement factor. The gain enhancement factor depends on the overlap of the active region with the optical standing wave within the cavity. The enhancement factor can be maximized by aligning the active region with the peak of the optical standing wave, and it approaches a value of two for an infinitesimally-small QW aligned at the antinode of the standing wave.[17] Gain enhancement factor is not applicable to edge-emitting lasers because the active region extends throughout a relatively long cavity length and overlaps many peaks and nulls of the optical standing wave, so the enhancement factor approaches a value of one. Gain enhancement factor gives VCSELs a unique advantage, but it also makes fabrication challenging because it requires precise layer thickness control. In the worst-case scenario, the enhancement factor approaches a value of zero if the active region is aligned to the null of the optical standing wave. During VCSEL design, it is important to simulate the optical mode profile (e.g., using TMM simulations) within the cavity and adjust cavity layer thicknesses to maximize the

enhancement factor. Furthermore, the optical mode profile within the cavity determines the amount of optical absorption and internal loss from each layer. In order to minimize optical absorption, cavity layers with large absorption coefficients (e.g., ITO or highly-doped $p^{++}GaN/n^{++}GaN$) can be strategically placed at the null of the optical mode. In addition to adjusting epitaxial n-GaN and p-GaN layer thicknesses, the relative position of the optical mode can be adjusted by depositing optical spacer layers, such as Ta_2O_5. Another component in the confinement factor is the fill factor, Γ_{fill}, which depends on the gain medium thickness in relation to the cavity length, as described by

$$\Gamma_{fill} = \frac{N_{qw}\, d_{qw}}{L_{eff}} \tag{15}$$

where N_{qw} is the number of QWs, and d_{qw} is the thickness for a single QW in the active region, and L_{eff} is the effective cavity length. This shows that there can be poor optical confinement for VCSEL designs with thin active regions or relatively long cavity lengths. The final component in the VCSEL confinement factor is the lateral confinement factor, Γ_{xy}, which depends on the index contrast radially from the center of the aperture.

1.3.2.3. Current Aperture Design

In addition to optical confinement, lateral current confinement is a key aspect of VCSEL design to ensure that high current densities are obtained in close proximity to the active region. Without effective current confinement, current can flow outside the aperture (i.e., current leakage) and the VCSEL may fail to lase. Current that flows outside the aperture is essentially wasted because even if there is radiative recombination, it does not contribute to useful gain for the lasing mode that is located within the aperture. Reaching the threshold for lasing requires sufficient pumping to create a population inversion. While higher energy levels

are normally less populated under thermal equilibrium, a population inversion can be created at high current injection levels so there are a large number of occupied states (i.e., electrons) in the conduction band and unoccupied states (i.e., holes) in the valence band. This requires reaching high carrier and current densities, which can be achieved by confining current to a small aperture (e.g., aperture diameter ~20 μm or less). The aperture size can greatly affect performance; for example, for devices with the same threshold current density, a VCSEL with a smaller aperture has a lower threshold current than a larger aperture device. However, there can be reduced optical confinement for very small apertures, while larger apertures can suffer from poor current spreading. The most commonly reported current aperture design for GaN-based VCSELs has consisted of dielectrics (e.g., SiO_2 or SiN_x) deposited outside the aperture. Because current cannot flow through the dielectric material, current is forced to flow through the circular aperture of the device. Other current aperture designs reported for GaN-based VCSELs have consisted of passivated p-GaN apertures formed by reactive ion etching,[80] photoelectrochemically etched air-gap apertures,[65] and ion implanted apertures.[3,30,58,61–63,72,73,117] Current aperture design is further discussed in Section 3.4 in the context of *m*-plane GaN VCSELs.

1.3.2.4. Intracavity Contact Design

Due to the relatively high resistance of p-type GaN, additional current spreading layers have been necessary on the p-side of GaN-based VCSELs. Current spreading is a problem because vertical current injection into the aperture is not possible through dielectric DBRs. Instead, metal contacts are used to inject current laterally toward the edge of the circular aperture, so adequate current spreading is necessary for current to occupy the center of the aperture. While this is not a problem on the n-side of the device, p-GaN has a high spreading

resistance and there would be significant current crowding at the edges of the aperture if a current spreading layer was not implemented. The most commonly employed intracavity contact and current spreading layer for GaN-based VCSELs has been indium tin oxide (ITO), which is a transparent conductive oxide (TCO) that is also commonly used in liquid crystal displays, plasma displays, and smartphone touchscreen displays. For example, patterned grids of ITO are key components for tracking finger movements in capacitive touchscreens, wherein a user's finger increases the capacitance of nearby ITO electrodes to compute the location on the screen. ITO is a great material for this application because it is both electrically conductive and optically transparent. While a grid of metal wires could also work for tracking, metal would block light from the display. Similarly, for VCSELs, the current spreading layer needs to be conductive and optically transparent at the wavelength of operation. However, ITO is not perfectly transparent at blue and violet wavelengths, which leads to internal loss due to optical absorption. If ITO is located between the p-GaN and p-side DBR, there can be significant internal loss because an antinode of the optical mode is located at the interface between ITO and the first low-index material of the p-side DBR. One method to minimize internal loss is to deposit a high-index spacer material (e.g., Ta_2O_5) before the p-side DBR so that ITO is placed at the null of the optical standing wave. There is also a trade-off in terms of ITO thickness, as thinner ITO minimizes internal loss while thicker ITO has improved current spreading.

Even when placing ITO at the null of the optical standing wave, there is still significant internal loss, and an alternative to ITO is to grow highly-doped n-type GaN (n^{++}GaN) above p^{++}GaN to form a n^{++}GaN/p^{++}GaN tunnel junction (TJ) intracavity contact. This design is advantageous because additional n-GaN can be easily grown above the n^{++}GaN to improve

current spreading while internal loss is minimized as n-GaN has a much lower optical absorption coefficient compared to ITO. Highly-doped layers have higher levels of optical absorption, so internal loss can be further minimized by placing the n^{++}GaN/p^{++}GaN TJ at the null of the optical standing wave. The optimal placement of the null is likely closer to p^{++}GaN, assuming it has a higher absorption coefficient than n^{++}GaN. J. Leonard et al. at UCSB reported the first GaN-based VCSEL with a TJ intracavity contact wherein molecular-beam epitaxy (MBE) was used to grow n^{++}GaN on the p-side of the device.[58] Due to the reduced internal loss compared to ITO VCSELs, the threshold current was lower and the peak output power was significantly higher for the TJ VCSEL compared to a similar VCSEL design that used ITO. The TJ was grown using MBE because of its ability to produce relatively high doping concentrations and because buried p-GaN can remain activated even after MBE growth of n-GaN. MOCVD growth of n-GaN on the p-side of the device typically passivates the p-GaN with hydrogen to form electrically-inactive Mg-H complexes. In this case, standard p-GaN thermal activation is not possible due to the n-GaN cap (i.e., n-GaN grown above p-GaN), but sidewall activation is an alternative solution to this problem that is effective for adequately small-area devices.[118] Despite the well-known claim that MOCVD growth of n-GaN passivates the underlying p-GaN, in a collaboration with S. Lee, we have demonstrated MOCVD-grown TJs with as-grown activated p-GaN without the need for sidewall activation. As further discussed in Section 3.5.2, this led to the first demonstration of a GaN-based VCSEL with a TJ intracavity contact grown using MOCVD.[117]

1.3.3. *c*-plane GaN-Based VCSELs

The first electrically-injected GaN-based VCSEL was demonstrated in 2008,[52] and there have been eight research groups that have demonstrated these devices over the following

ten years. All of the reports have been for *c*-plane GaN-based VCSELs except for UCSB which has focused on nonpolar *m*-plane GaN. Section 1.3.3 summarizes reports in the literature for *c*-plane GaN-based VCSELs from groups at National Chiao Tung University (NCTU), Nichia, Panasonic, EPFL, Xiamen University, Meijo University, and Sony. Reports of nonpolar *m*-plane GaN-based VCSELs from UCSB are summarized later in Section 1.3.4.

1.3.3.1. National Chiao Tung University (NCTU)

T.C. Lu et al. at National Chiao Tung University (NCTU) demonstrated the first electrically pumped GaN-based VCSEL in 2008.[52] A schematic of the VCSEL design, emission spectrum, and SEM cross-section are shown in Figure 13.

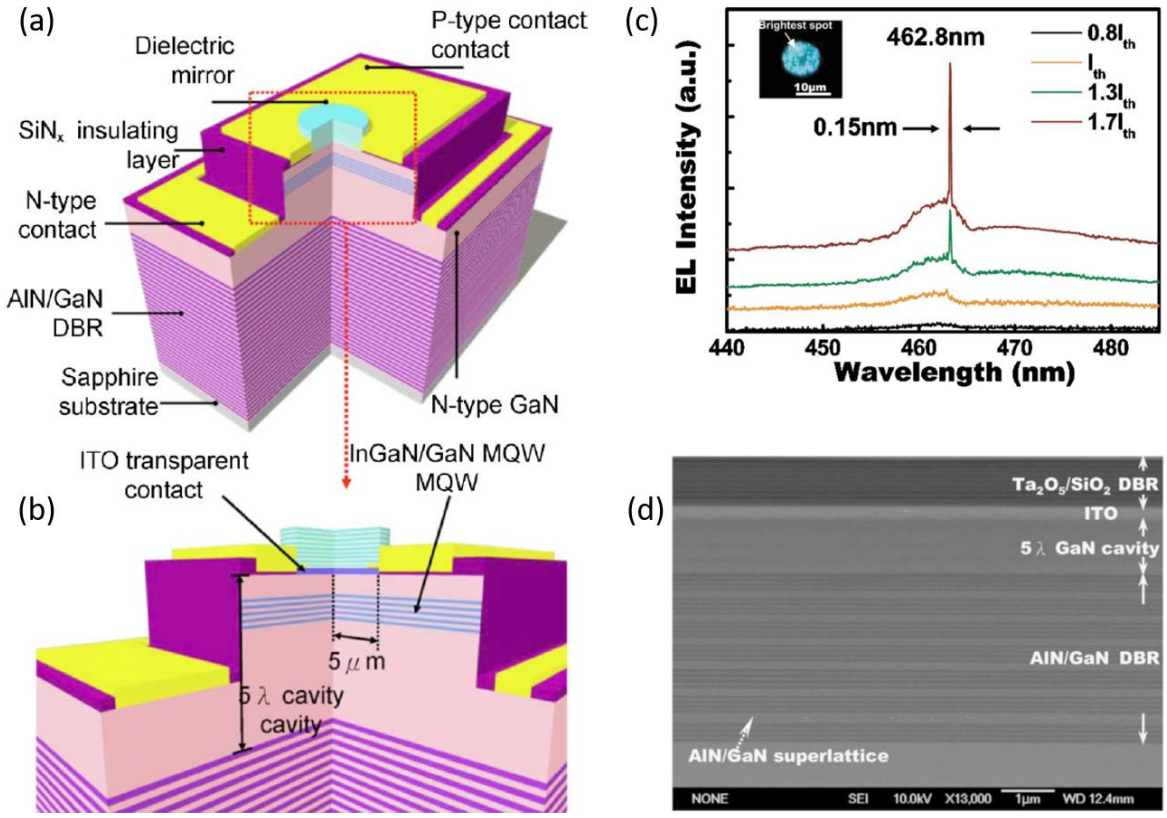


Figure 13. (a) Schematic diagram of the first demonstration of an electrically-injected GaN-based VCSEL. (b) Magnified view showing the 5λ optical cavity length, 5 μm aperture radius, and InGaN/GaN MQW. (c) VCSEL emission spectrum measured at 77 K and the inset shows a charge-coupled device (CCD) image of emission

from the aperture. (d) Cross-section SEM image of the VCSEL cavity with a hybrid DBR design. Reprinted from [Lu, T.-C. C., Kao, T.-T. T., Chen, S.-W. S. W., Kao, C.-C. C., Kuo, H.-C. C., & Wang, S.-C. C. (2008). CW lasing of current injection blue GaN-based vertical cavity surface emitting lasers. In 2008 Conference on Lasers and Electro-Optics and 2008 Conference on Quantum Electronics and Laser Science (Vol. 141102, pp. 1–2). https://doi.org/10.1109/CLEO.2008.4551202] with the permission of AIP Publishing.[52]

The *c*-plane GaN-based VCSEL on sapphire lased under pulsed operation at room temperature but could only lase under CW operation when it was cooled to 77 K. With an optical cavity length of 5λ, a hybrid DBR design was employed with an MOCVD-grown 29-period AlN/GaN DBR on the n-side and an 8-period Ta_2O_5/SiO_2 dielectric DBR on the p-side. The current aperture was formed using SiN_x with an aperture diameter of 10 μm, and a 240-nm-thick layer of ITO was used as a transparent contact layer (i.e., current spreading layer on the p-side). The threshold current was 1.4 mA (1.8 kA/cm^2) with a lasing wavelength of 462.8 nm. The divergence angle was ~11.7° and emission had a polarization ratio of 80%. A crack-free epitaxial AlN/GaN DBR was grown by inserting AlN/GaN superlattices into the DBR to reduce the biaxial tensile strain. The superlattices were inserted between every four pairs of DBR mirror periods and consisted of 5.5 pairs of AlN/GaN with a half-wavelength optical thickness. The epitaxial bottom DBR had a peak reflectivity of 99.4% and a spectral bandwidth of ~25 nm.[52]

In 2010, T.C. Lu et al. at NCTU achieved CW operation at room temperature using an improved design that consisted of an epitaxially grown 29-pair AlN/GaN DBR, 7λ optical thickness, 10-period InGaN/GaN MQW, AlGaN electron blocking layer (EBL), and a top-side 10-period Ta_2O_5/SiO_2 DBR. A schematic diagram of the VCSEL and electrical characteristics are shown in Figure 14.

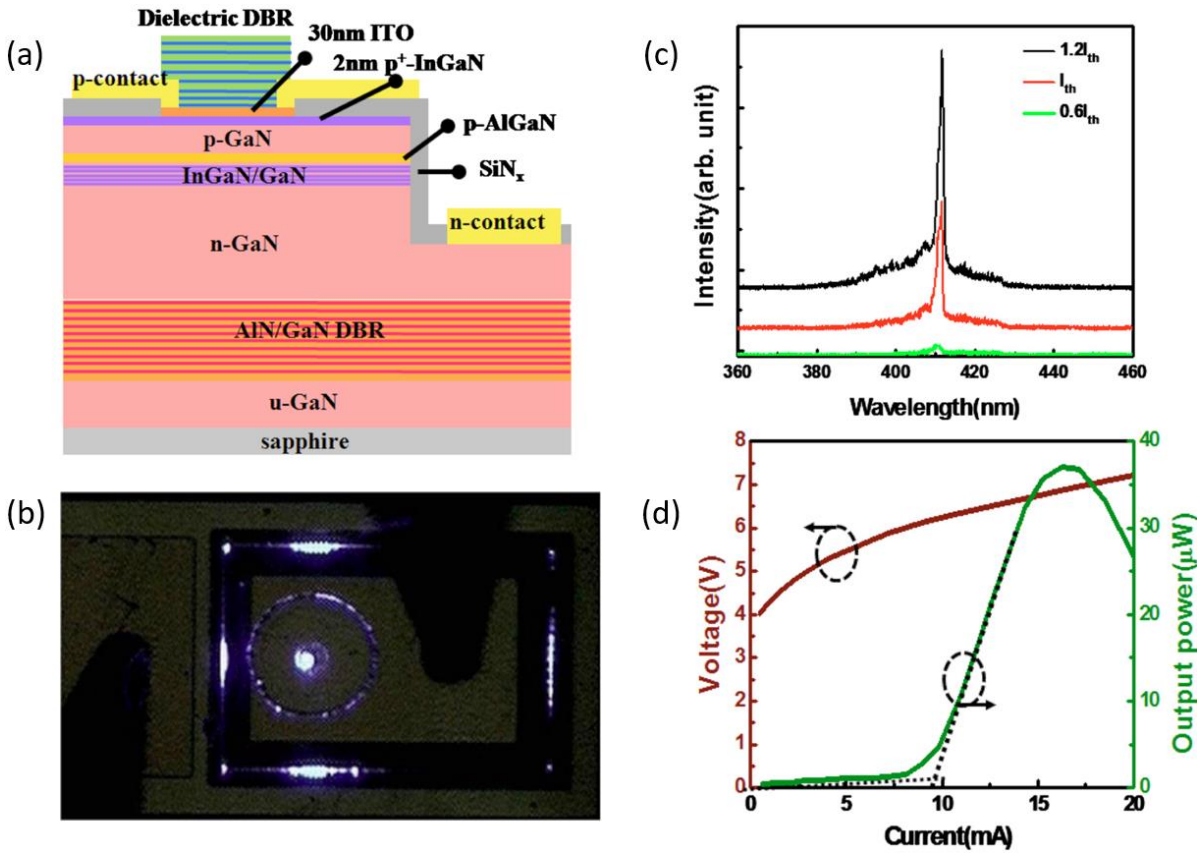


Figure 14. (a) Schematic diagram of the hybrid DBR design from NCTU that achieved CW operation at room temperature. (b) CCD image of emission from the aperture, (c) VCSEL emission spectrum, and (d) Light output power and current versus voltage (*L-I-V*) measured at room temperature. Reprinted from [Lu, T.-C. C., Chen, S.-W. W., Wu, T.-T. T., Tu, P.-M. M., Chen, C.-H. C.-K. C. H. C. K. C.-H., Chen, C.-H. C.-K. C. H. C. K. C.-H., Wang, S.-C. C. (2010). Continuous wave operation of current injected GaN vertical cavity surface emitting lasers at room temperature. Applied Physics Letters, 97(7), 71114. https://doi.org/10.1063/1.3483133] with the permission of AIP Publishing.[78]

Compared to the previous design with an ITO thickness of 240 nm,[52] the ITO thickness was reduced to 30 nm. Another improvement was the addition of an AlGaN electron blocking layer (EBL) to inhibit carrier overflow. A 2 nm p^+InGaN layer above the p-GaN helped reduced the series resistance between the p-GaN and ITO, but the drawback of this design is an increase in optical absorption. As shown in Figure 14(c)-(d), the lasing wavelength was 412 nm, and threshold current was ~9.7 mA (12.4 kA/cm^2) with a peak output power of ~38 μW.[78]

In 2015, D.H. Hsieh et al. at NCTU reported a significantly higher peak output power of 0.9 mW by replacing the AlGaN EBL with an AlGaN/GaN multiple quantum barrier (MQB).[56] Compared to a conventional bulk AlGaN EBL, the MQB-EBL reduced the threshold current from 9.5 mA (12 kA/cm^2) to 8.5 mW (10.6 kA/cm^2). The VCSEL design was similar to previous reports,[52,78] but the EBL was replaced with a 5-period AlGaN/GaN (2 nm/2 nm) MQB. Theoretical calculations suggest that the improved performance of the MQB EBL VCSEL design is due to higher injection efficiency due to improved electron blocking ability, which was attributed to reduced strain in a MQB structure that created a higher virtual potential barrier for electrons due to the quantum interference effect.[56]

In 2016, P.S. Yeh et al. at NCTU demonstrated a GaN-based VCSEL with a novel current aperture design that used a silicon-diffusion-defined current blocking layer for lateral confinement.[68] The aperture was created by selectively diffusing silicon (Si) to convert p-GaN into n-GaN to achieve a current-blocking effect. Figure 15 shows a schematic of the VCSEL design, CCD images of emission, and the emission spectrum for a 3 μm diameter aperture VCSEL.

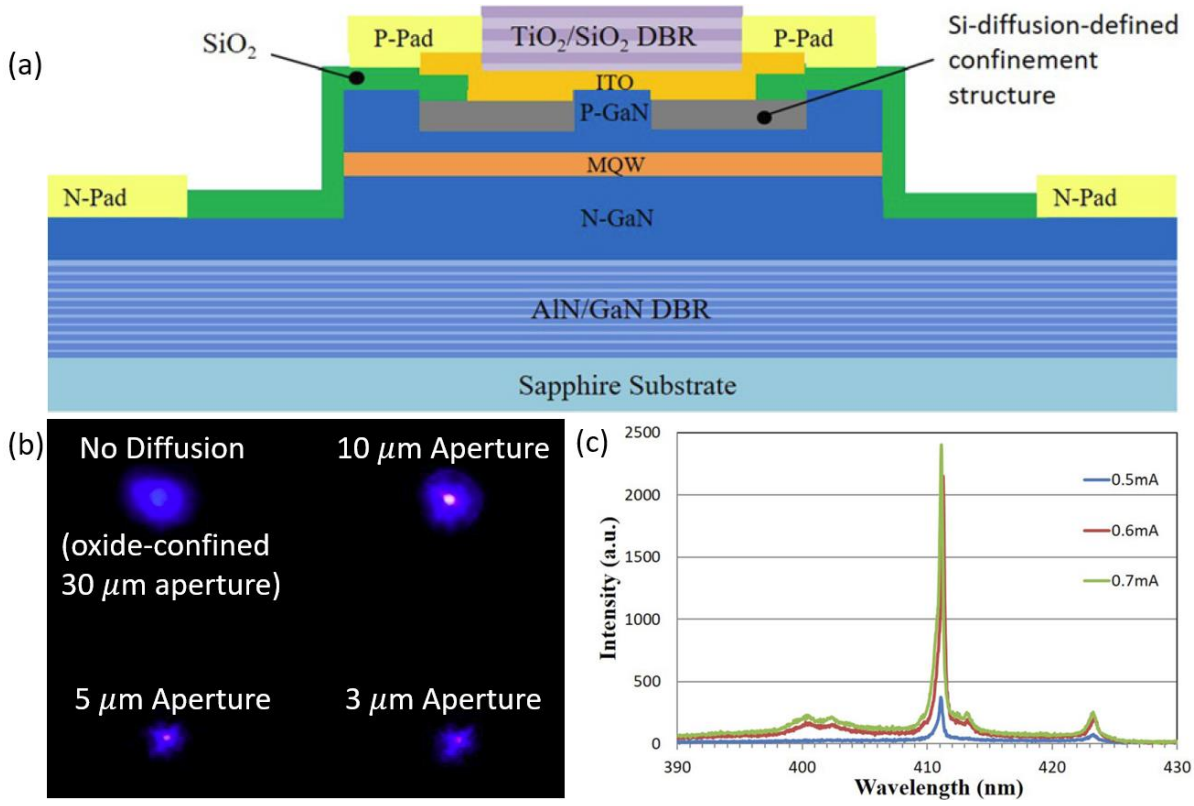


Figure 15. (a) Schematic diagram of the hybrid DBR design from NCTU using a Si-diffusion-defined current aperture. (b) CCD images of emission for VCSELs without a Si-diffusion-defined aperture (top-left) and Si-diffusion-defined apertures with diameters of 10 μm (top-right), 5 μm (bottom-left), and 3 μm (bottom-right). (c) VCSEL emission spectrum for a device with an aperture diameter of 3 μm, showing a sub-milliamp threshold current. Reprinted from [Yeh, P. S., Chang, C.-C., Chen, Y.-T., Lin, D.-W., Liou, J.-S., Wu, C. C., … Kuo, H.-C. (2016). GaN-based vertical-cavity surface emitting lasers with sub-milliamp threshold and small divergence angle. Applied Physics Letters, 109(24), 241103. https://doi.org/10.1063/1.4972182] with the permission of AIP Publishing.[68]

A hybrid DBR VCSEL design was employed with a 25-period AlN/GaN epitaxial bottom DBR, 880 nm n-GaN, 10-period InGaN/GaN MQW, 25 nm p-AlGaN EBL, 100 nm p-GaN, 4 nm p-InGaN, 30 nm ITO intracavity contact, and an 8-period TiO_2/SiO_2 dielectric top DBR. The silicon-diffusion-defined current aperture was fabricated by using reactive ion etching (RIE) to etch a donut-shaped region past the p-InGaN into the p-GaN (15 nm etch depth), depositing a thin film of Si into that region using electron-beam evaporation, and annealing at 800 °C in a N_2 ambient for 20 minutes in order for Si to diffuse throughout the donut-shaped region. The top-left CCD image of Figure 15(b) shows emission for a device without the Si-

diffusion process, resulting in a 30 μm current aperture confined by SiO_2. The other images in Figure 15(b) show Si-diffusion-defined current apertures of various aperture diameters, which showed relatively bright emission that was confined to the Si-diffusion-defined aperture. As shown in Figure 15(c) for a 3 μm aperture device, the threshold current was 0.5 mA (7.1 kA/cm^2) with a peak emission wavelength of 411.2 nm and mode spacing of 12.1 nm. Near-single lateral mode operation was achieved using a relatively small current aperture, and the a divergence angle of ~ 5° was measured.[68]

While previous designs from NCTU used a hybrid DBR design,[52,56,68,78] a dual-dielectric DBR design was reported in 2017 by T.C. Chang et al. that could operate at temperatures up to 350 K.[69] Compared to the previous design that used a sapphire substrate (with a low thermal conductivity),[68] improved thermal performance was achieved by flip-chip bonding to a silicon substrate, which has a relatively high thermal conductivity. Although dielectric DBRs have a low thermal conductivity and inhibit thermal transport toward the flip-chip substrate, heat could flow through a 20-μm-wide metal pathway toward the Si submount. The lasing wavelength was measured to redshift as a function of temperature at a rate of 0.012 nm/K while the temperature-dependent gain peak redshifted at a rate of 0.034 nm/K. The thermal resistance was predicted to be ~708 K/W based on the lasing wavelength redshift at higher input powers, which agreed with thermal simulation results.[69]

1.3.3.2. Nichia Corporation

Shortly after the first electrically-injected GaN-based VCSEL created at NCTU in 2008, Y. Higuchi et al. at Nichia Corporation reported the first demonstration of CW lasing at room temperature for a *c*-plane GaN-based VCSEL.[76] These devices had a 7λ optical cavity length, SiO_2 dielectric current aperture, ITO intracavity contact, and a dual-dielectric DBR

design. MOCVD growth was performed on a sapphire substrate, and the active region consisted of a 2-period InGaN/GaN (9 nm/13 nm) MQW. After depositing the p-side 11.5-period SiO_2/Nb_2O_5 DBR, the sample was bonded to a Si substrate and the sapphire substrate was removed using a laser-induced lift-off process. This was followed by polishing, thinning, and chemical mechanical polishing (CMP) of n-GaN to form a cavity length of ~1.1 μm (~7λ). The n-side mirror consisted of a 7-period SiO_2/Nb_2O_5 DBR. With an 8 μm diameter aperture, the threshold current was 7 mA at a lasing wavelength of 414 nm.[76]

In 2009, K. Omae et al. at Nichia Corporation reported an improved peak output power of 0.62 mW by using a GaN substrate instead of a sapphire substrate during MOCVD growth.[77] The device structure and fabrication steps were very similar to the previous report.[76] While laser liftoff is effective to remove the sapphire growth substrate after flip-chip bonding, it cannot be used to remove a GaN substrate. Instead, the GaN substrate was removed by mechanical polishing and CMP, which resulted in more cavity length variation compared to devices grown on sapphire. While devices on GaN were expected to have a lower threshold current due to the lower dislocation density compared to sapphire substrates, the threshold current was similar between the devices, with values of 8.0 mA and 7.0 mA, respectively. During lifetime tests, the devices grown on sapphire could lase up to 2 minutes while devices grown on GaN lased over 10 minutes. The main performance improvement for growing on GaN substrates instead of sapphire was a ~ 4.5 higher peak output power of 0.62 mW, which was attributed to the relatively large lasing spot size.[77]

While previous GaN-based VCSELs emitted at violet wavelengths,[52,76–78] in 2011, D. Kasahara et al. at Nichia Corporation reported the first demonstration of blue-emitting and green-emitting GaN-based VCSELs.[79] These devices had very similar designs as before, using

a GaN substrate for MOCVD and a dual-dielectric DBR design. The blue VCSEL could lase under CW operation while the green VCSEL only lased under pulsed operation. The blue VCSEL had a threshold current of 1.5 mA and peak output power of 0.7 mW. The green VCSEL had a threshold current of 22 mA, but the output power could not be accurately determined by the pulsed current measurements. The reduced threshold current for the blue VCSEL was attributed to the optimization of the epitaxial structure.[79]

1.3.3.3. Panasonic Corporation

In 2012, T. Onishi et al. at Panasonic Corporation demonstrated a dual-dielectric GaN-based VCSEL with the longest reported cavity length, which lased under CW operation at room temperature with a threshold current below 2 mA and peak output power of 3 μW.[53] Compared to other reports of GaN-based VCSELs, this design had a relatively long cavity length of 6 μm (~35λ). A schematic illustration of the design is shown in Figure 16(a).

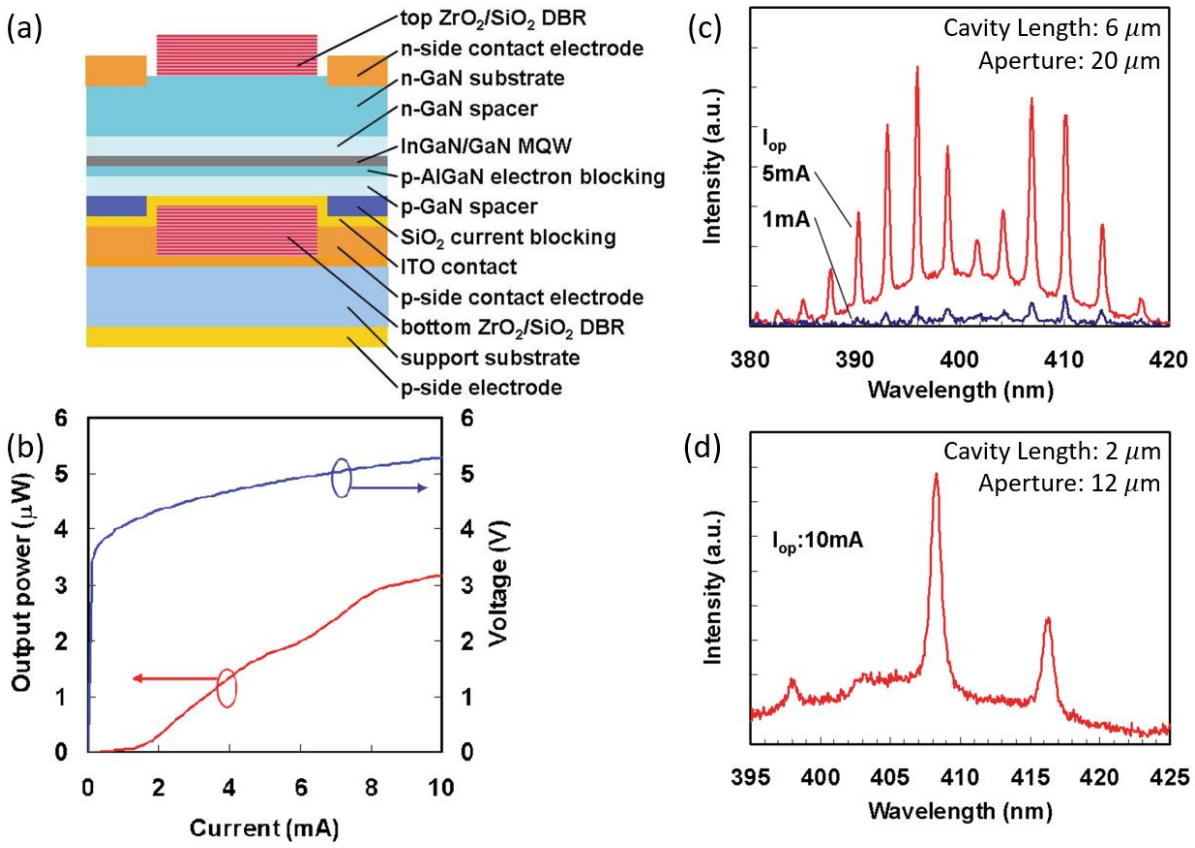


Figure 16. (a) Schematic diagram of the dual-dielectric DBR GaN-based VCSEL design from Panasonic. (b) *L-I-V* characteristic for a 6 μm cavity length and 20 μm aperture diameter. (c) VCSEL emission spectrum for a device with an aperture diameter of 20 μm and cavity length of 6 μm. (d) Emission spectrum of a VCSEL with a 12 μm aperture diameter and a 2 μm cavity length. Figures compiled from [Onishi, T., Imafuji, O., Nagamatsu, K., Kawaguchi, M., Yamanaka, K., & Takigawa, S. (2012). Continuous Wave Operation of GaN Vertical Cavity Surface Emitting Lasers at Room Temperature. Quantum Electronics, IEEE Journal Of, 48(9), 1107–1112. https://doi.org/10.1109/jqe.2012.2203586].[53] © 2012 IEEE

MOCVD growth was conducted on a *c*-plane GaN substrate with an epitaxial structure consisting of n-GaN, an InGaN/GaN MQW, p-AlGaN EBL, and p-GaN. The current aperture consisted of SiO_2, ITO was used as an intracavity contact, and the DBRs consisted of 13 pairs of ZrO_2/SiO_2. After flip-chip bonding to a support substrate, the GaN growth substrate was thinned to several micrometers by CMP to define the cavity length. With aperture diameters ranging from 12 μm to 20 μm, VCSELs were fabricated with cavity lengths of 2 μm, 6 μm, and 10 μm. The *L-I-V* characteristic for a device with an aperture diameter of 20 μm and cavity length of 6 μm is shown in Figure 16(b). The threshold current was less than 2 mA and the

peak output power was 3 μW. As shown in the emission spectrum in Figure 16(c) for a 20 μm aperture diameter VCSEL, the relatively long 6 μm cavity length supported many longitudinal lasing modes with a mode spacing of ~ 3 nm. Figure 16(d) shows the emission spectrum for a shorter 2 μm cavity length that has a larger mode spacing of ~ 7 nm. Lastly, a 5 × 5 GaN-VCSEL array was demonstrated under CW operation at room temperature.[53,54]

1.3.3.4. École Polytechnique Fédérale de Lausanne (EPFL)

In 2012, G. Cosendey et al. at École polytechnique fédérale de Lausanne (EPFL) demonstrated a violet GaN-based VCSEL with an RIE passivated p-GaN current aperture under pulsed operation.[80] A hybrid epitaxial/dielectric DBR design was employed using epitaxial AlInN/GaN DBRs grown on *c*-plane GaN free-standing substrates and a TiO_2/SiO_2 DBR on top. While AlGaN/GaN DBRs have a large lattice parameter mismatch that can lead to defects, the design from EPFL used a lattice-matched, defect-free 41.5-period $Al_{0.8}In_{0.2}N$/GaN DBR grown using MOCVD. A schematic illustration of the design is shown in Figure 17(a).

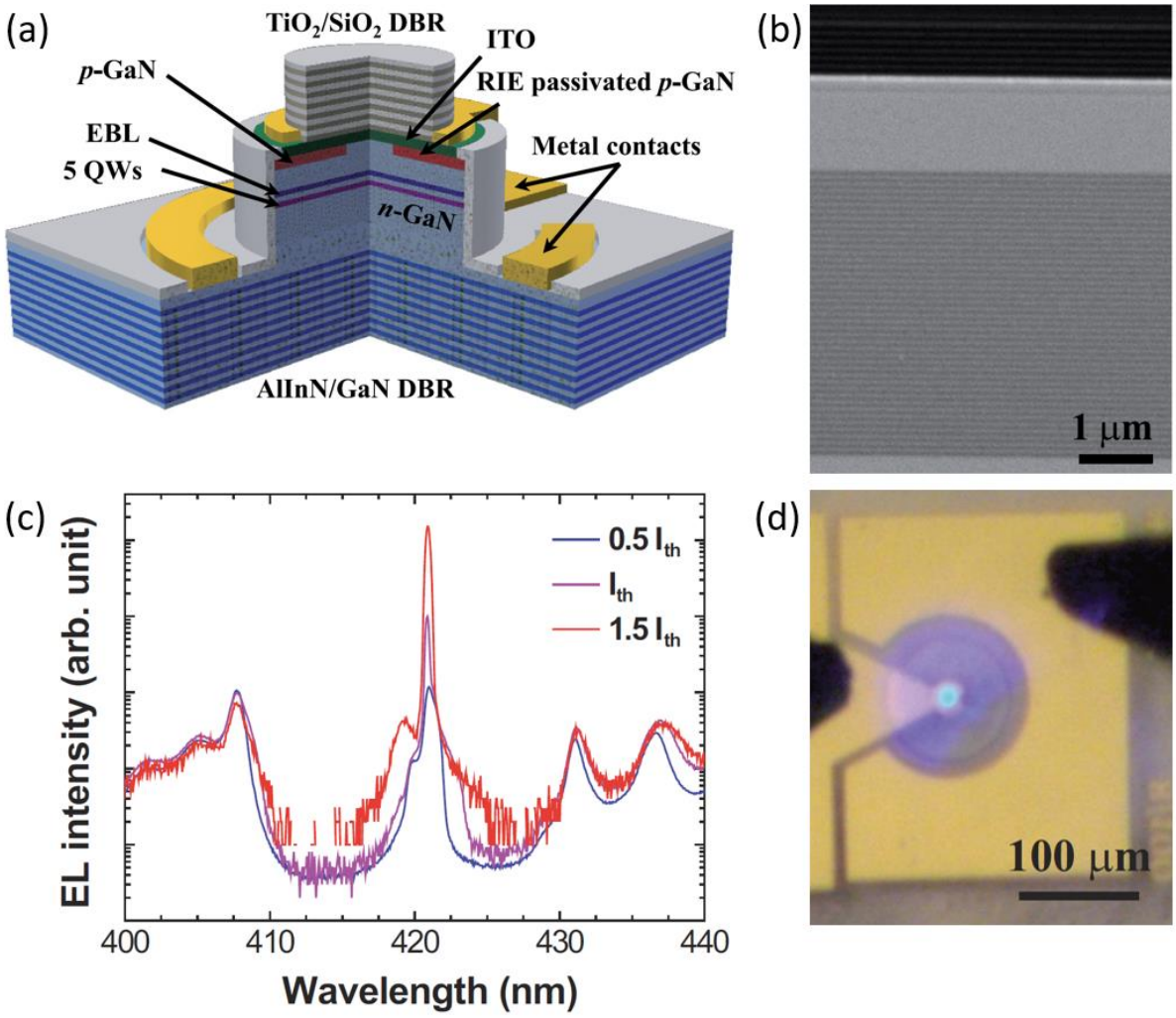


Figure 17. (a) Schematic diagram of the GaN-based VCSEL design from EPFL that used a hybrid DBR design (MOCVD-grown 41.5-period AlInN/GaN n-DBR and 7-period TiO_2/SiO_2 p-DBR) and a current aperture defined by RIE passivated p-GaN. (b) Emission spectrum under pulsed operation from the bottom-side of a device with an aperture diameter of 8 μm. (c) Focused ion beam (FIB) cross-section SEM image of the VCSEL microcavity. (d) Optical micrograph of a device under low CW electrical injection. Reprinted from [Cosendey, G., Castiglia, A., Rossbach, G., Carlin, J.-F., & Grandjean, N. (2012). Blue monolithic AlInN-based vertical cavity surface emitting laser diode on free-standing GaN substrate. Applied Physics Letters, 101(15), 151113. https://doi.org/10.1063/1.4757873] with the permission of AIP Publishing.[80]

The VCSELs had a 7λ cavity length, 940 nm n-GaN, MQW consisting of five periods of InGaN/GaN (5 nm/5 nm), 20 nm p-AlGaN EBL, and 120 nm p-GaN. A focused ion beam (FIB) cross-section SEM image of the VCSEL cavity is shown in Figure 17(b). These VCSELs employed a novel current aperture design that was formed by performing a CHF_3/Ar RIE plasma treatment to passivate the p-GaN surface while the aperture was protected by

photoresist. This aperture design is advantageous compared to conventional dielectric apertures because the device surface remains flat, which improves the quality of the top DBR and conformal deposition of ITO is no longer necessary. ITO was sputtered with a quarter-wavelength thickness to act as the first half-pair layer in the topside 7-period TiO_2/SiO_2 dielectric DBR. Under pulsed operation for an 8 μm aperture diameter device, the threshold current was ~ 70 mA (~140 kA/cm^2) and the peak output power of ~330 μW. As shown in the bottom-side emission spectra in Figure 17(c), the lasing wavelength was at 421 nm, which was similar to the spectrum measured from the top-side of the device. Figure 17(d) shows an optical micrograph of a VCSEL under low CW electrical injection. The effectiveness of the RIE passivated p-GaN current aperture was tested by fabricating similar devices that replaced the aperture with a conventional SiO_2 dielectric aperture. Both types of apertures had equivalent *I-V* characteristics, which shows that the RIE passivated p-GaN aperture was effective. Furthermore, light emission was limited to the current aperture diameter and the threshold current density did not depend on aperture diameter. The relatively high threshold current was attributed to absorption loss in the ITO and insufficiently high reflectivity of the top DBR.[80]

1.3.3.5. Xiamen University

W.J. Liu et al. at Xiamen University reported a GaN-based VCSEL in 2014 with a threshold current density of 1.2 kA/cm^2 and peak output power of ~ 0.5 μW under CW operation at room temperature.[55] A schematic diagram of the design is shown in Figure 18(a).

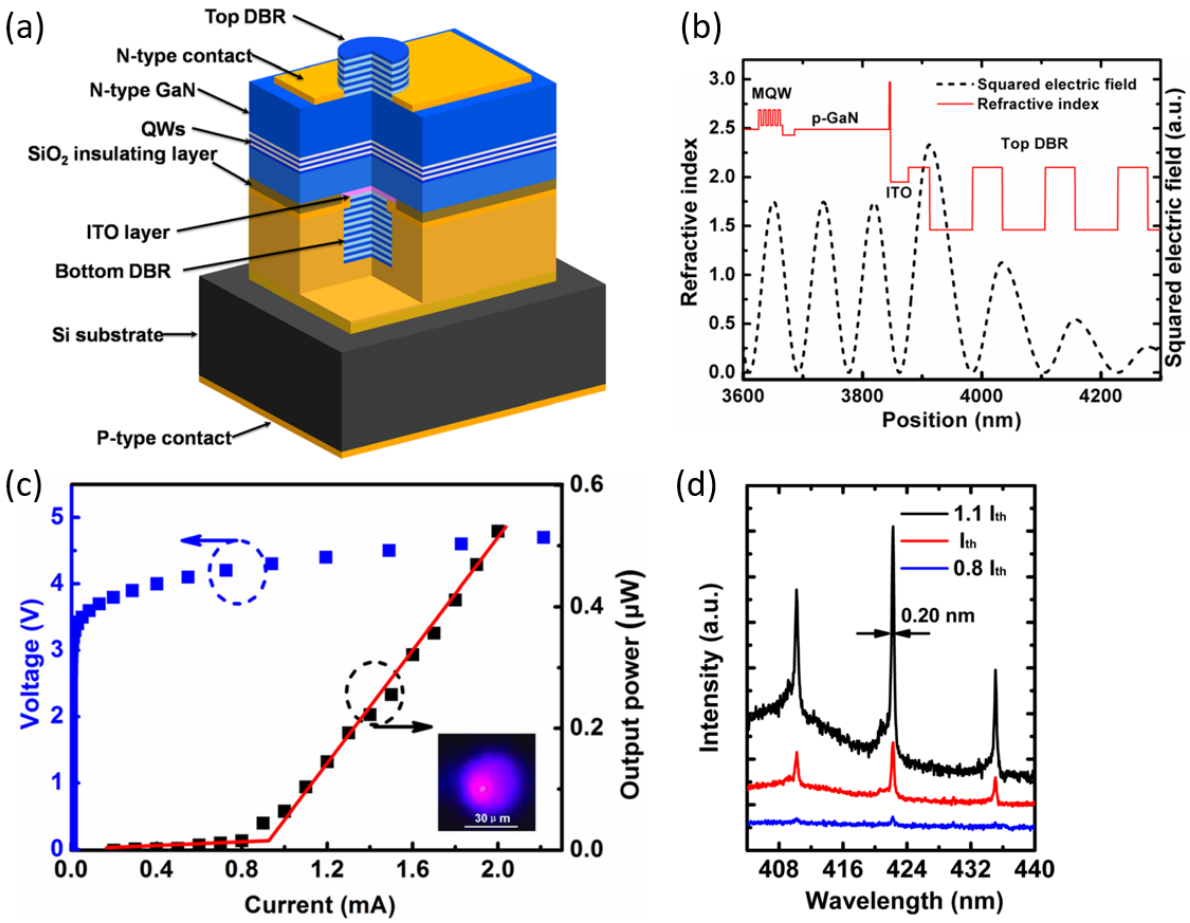


Figure 18. (a) Schematic diagram of the dual-dielectric DBR GaN-based VCSEL design with a SiO_2 current aperture from Xiamen University. (b) Emission spectrum under pulsed operation from the bottom-side of a device with an aperture diameter of 8 μm. (c) *L-I-V* characteristic of a 10 μm diameter aperture device with the lasing spot shown in the inset . (d) VCSEL emission spectra at different injection currents. Reprinted from [Liu, W.-J., Hu, X.-L., Ying, L.-Y., Zhang, J.-Y., & Zhang, B.-P. (2014). Room temperature continuous wave lasing of electrically injected GaN-based vertical cavity surface emitting lasers. Applied Physics Letters, 104(25), 251116. https://doi.org/10.1063/1.4885384] with the permission of AIP Publishing.[55]

MOCVD growth was performed on a sapphire substrate to grow a 30 nm GaN nucleation layer, 3 μm GaN layer, 2.5 μm n-GaN, 5 × InGaN/GaN MQW with 4 nm InGaN QWs and 4 nm GaN barriers, 20 nm p-AlGaN EBL, 159 nm p-GaN, and 2 nm n-InGaN which was used to improve the contact between the 30-nm-thick ITO and p-GaN layers. The bottom and top dielectric ZrO_2/SiO_2 DBRs consisted of 17.5-periods and 12-periods, respectively. The current aperture was defined using SiO_2 and the sample was flip-chip bonded to a Si substrate. The sapphire growth substrate was removed via laser lift-off and the cavity length was defined

by inductively coupled plasma (ICP) etching and CMP. The refractive index and simulated optical standing wave distribution within the cavity are shown in Figure 18(b). To reduce optical absorption loss, the 2 nm InGaN and ITO layer were positioned at the null of the electric field by inserting a 36.6 nm ZrO_2 layer between the ITO and the top DBR. The *L-I-V* characteristic for a 10 μm diameter aperture device is shown in Figure 18(c), which also shows the lasing spot in the inset. The threshold current was ~ 0.93 mA (1.2 kA/cm^2) and the peak output power was ~ 0.5 μW. Figure 18(d) shows the emission spectra at various currents and based on a mode spacing of ~ 12.5 nm, the cavity length was calculated to be ~ 2.18 μm.[55]

In 2016, G. Weng et al. at Xiamen University demonstrated the first yellow-green-emitting GaN-based VCSEL by using an InGaN quantum dot active region, achieving a low threshold current of 0.61 mA (0.78 kA/cm^2) and emission wavelength of 560.4 nm.[67] Green and longer-wavelength emission has been difficult to achieve because higher compositions of indium in InGaN QWs results in low internal quantum efficiency, due to defects and the strain-induced piezoelectric field that produces the QCSE. An alternative to the conventional InGaN QW is to use quasi-zero-dimensional InGaN quantum dots, which have advantages such as smaller effective active volume, higher temperature stability, stronger carrier localization, fewer structural defects than QWs, and suppressed QCSE. MOCVD was performed on a sapphire substrate and the active region consisted of two layers of InGaN/GaN quantum dots. InGaN quantum dots can be grown directly in the Stranski-Krastanov growth mode, which consists of layer-by-layer wetting layer growth followed by island formation and coalescence.[119] InGaN quantum dots (indium composition ~ 27%) were grown at 670 °C and were subsequently capped by 2-nm-thick GaN grown at the same temperature (to protect the quantum dots during the following temperature ramp), followed by an 8-nm-thick GaN barrier

grown at 850 °C. The quantum dots had a dot density of ~ 1.5×10^{10} cm^{-2} and a diameter ranging between 20 nm and 60 nm. The VCSEL structure had a dual-dielectric DBR design (12.5-period TiO_2/SiO_2 bottom DBR and 11.5-period TiO_2/SiO_2 top DBR), 10 μm SiO_2 current aperture, and a 30 nm ITO intracavity contact. Using a copper flip-chip substrate, the sapphire growth substrate was removed by laser lift-off, and the cavity length was defined by ICP etching and CMP. The threshold current was 0.61 mA (0.78 kA/cm^2) with a peak output power of ~ 6 μW under CW operation.[67]

In 2017, R. Xu et al. at Xiamen University reported the first GaN-based VCSEL with simultaneous blue and green lasing by using an active region consisting of quantum dots placed within two QWs.[71] Instead of using a 2-nm-thick GaN capping layer for the quantum dots (as used in the previous design),[67] the $In_{0.27}Ga_{0.73}N$ quantum dots were embedded within 2-nm-thick $In_{0.1}Ga_{0.9}N$ QWs, which were capped by an 8-nm-thick GaN layer. The VCSEL structure was similar to the previous design and consisted of a dual-dielectric DBR design (13.5-period Ti_3O_5/SiO_2 bottom DBR and 11.5-period Ti_3O_5/SiO_2 top DBR), 10 μm SiO_2 current aperture, 30 nm ITO intracavity contact, copper flip-chip substrate, and the cavity length was defined by laser liftoff of the sapphire growth substrate, ICP etching, and CMP. Under CW operation, a green lasing peak appeared at a wavelength of 545 nm and threshold current of 30 μA. This was due to the $In_{0.27}Ga_{0.73}N$ quantum dots while the $In_{0.1}Ga_{0.9}N$ QWs produced a blue lasing peak at a higher threshold current of ~ 5 mA at a wavelength of 430 nm. The blue and green lasing peaks had nearly identical intensities at a current of 10 mA, and the blue peak became dominant at higher injection levels. Based on a longitudinal mode spacing of ~ 13 nm, the cavity length was ~ 3.8 μm. It is predicted that the lasing wavelength

can be easily tuned by adjusting the growth conditions to vary the size of the quantum dots or the indium content.[71]

1.3.3.6. Sony Corporation

In 2015, S. Izumi et al. at Sony Corporation demonstrated a novel dual-dielectric DBR GaN-based VCSEL design using epitaxial lateral overgrowth (ELO) to embed a dielectric DBR within MOCVD-grown n-GaN, achieving CW operation with a peak output power of 0.9 mW at a blue lasing wavelength of 446 nm.[57] This was the first reported dual-dielectric DBR design that does not require flip-chip bonding and substrate removal, which greatly simplifies the VCSEL fabrication process. Furthermore, ELO allows precise cavity length control, unlike conventional thinning and polishing for most dual-dielectric DBR designs. After depositing and patterning a 14.5-period SiO_2/SiN_x dielectric DBR onto an n-GaN substrate, MOCVD growth was performed to embed the DBR within n-GaN using ELO. The epitaxial structure consisted of 4 μm n-GaN, an active region with two pairs of InGaN/GaN (6 nm/10 nm), and p-GaN. The current aperture was formed by SiO_2 with an 8 μm diameter and ITO was used as the p-type ohmic contact. The top mirror consisted of a 12-period Ta_2O_5/SiO_2 dielectric DBR. The n-GaN substrate was lapped to a thickness of ~ 80 μm and n-contact was formed on the backside of the wafer. Under CW operation, the threshold current was 8 mA (~16 kA/cm^2) with a peak output power of 0.9 mW. Based on a longitudinal mode spacing of 6.7 nm and group refractive index of 3.3, the optical cavity length was estimated to be 4.5 μm.[57]

In 2016, T. Hamaguchi et al. at Sony Corporation demonstrated the first GaN-based VCSEL with a peak output power over 1 mW.[61,62] Similar to the previous dual-dielectric DBR design,[57] these devices featured a bottom dielectric DBR that was embedded within n-GaN

using ELO during MOCVD growth. A schematic illustration of the design is shown in Figure 19(a).

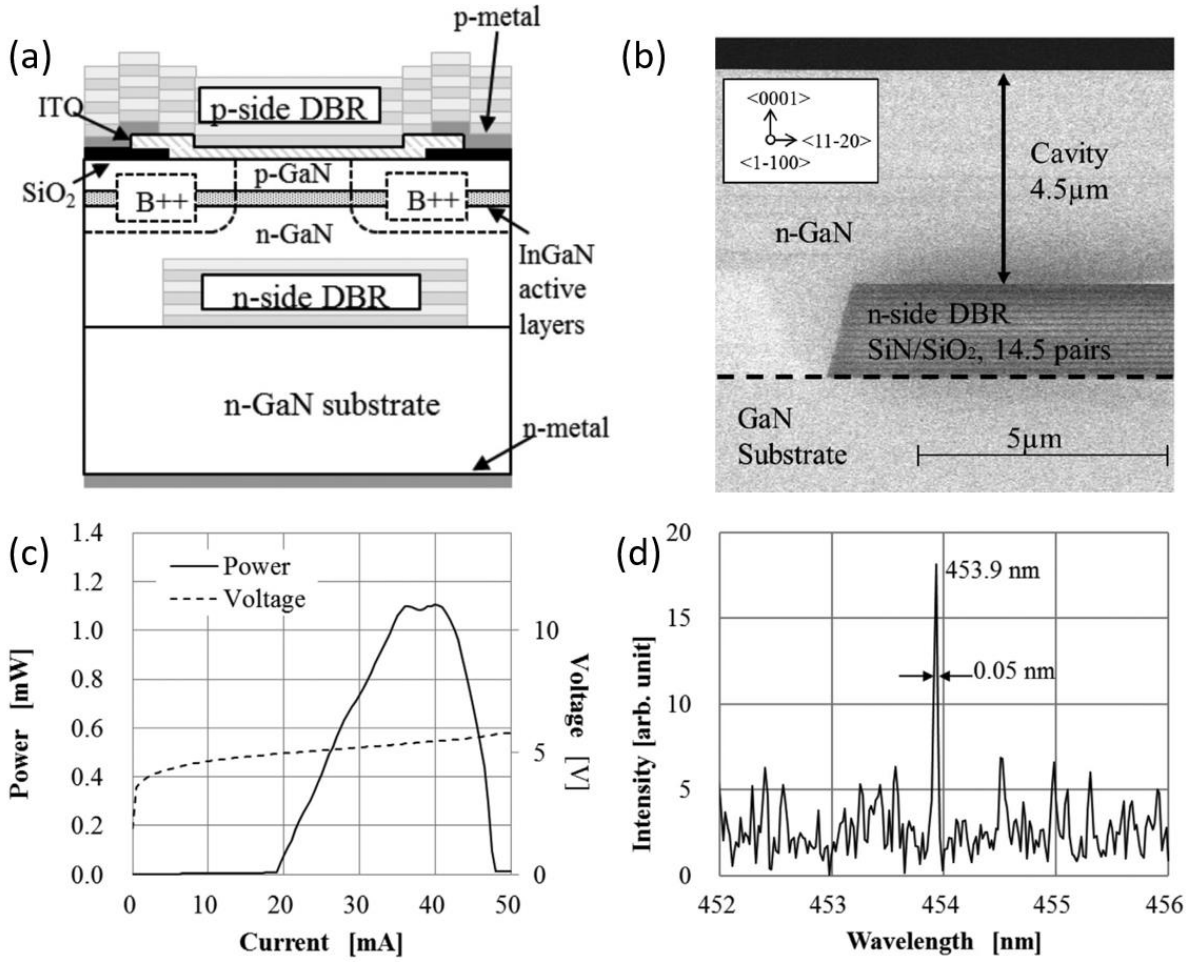


Figure 19. (a) Schematic diagram of the dual-dielectric DBR GaN-based VCSEL design from Sony Corporation that was fabricated using ELO and used a boron ion (B++) implanted current aperture. (b) Cross-section SEM image of the VCSEL structure with a dielectric DBR embedded within n-GaN that was grown by ELO. (c) *L-I-V* characteristic of an 8 μm diameter VCSEL. (d) VCSEL emission spectrum showing a lasing wavelength of 453.9 nm.[62] Figures adapted from [Hamaguchi, T., Fuutagawa, N., Izumi, S., Murayama, M., & Narui, H. (2016). Milliwatt-class GaN-based blue vertical-cavity surface-emitting lasers fabricated by epitaxial lateral overgrowth. Physica Status Solidi (A) Applications and Materials Science, 213(5), 1170–1176. https://doi.org/10.1002/pssa.201532759] with the permission of AIP Publishing. © 2016 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

A 14.5-period SiN/SiO_2 DBR was deposited and patterned on a GaN substrate, and ELO growth was performed to grow seed crystals of n-GaN in the window regions between DBR islands until the n-GaN engulfed the DBR to form a planar surface. A cross-section SEM image of the VCSEL cavity is shown in Figure 19(b), which demonstrates that the bottom

DBR was completely embedded with n-type GaN by the ELO technique without cracks or voids. A 30-nm-thick ITO intracavity contact was employed on the p-side and the top mirror consisted of an 11.5-period Ta_2O_5/SiO_2 DBR. Although this design was very similar to the previous report,[57] the number of InGaN QWs was increased from two to four, and boron implantation on the p-GaN surface was used to define the current aperture (diameter of 8 μm) instead of SiO_2. As shown in the *L-I-V* curve in Figure 19(c), the threshold current was 18 mA (35.8 kA/cm^2) and the peak output power was 1.1 mW under CW operation at room temperature. The longitudinal mode spacing below threshold was 6.7 nm, which agreed with the ~ 4.5 μm cavity length measured by SEM. As shown in the emission spectrum in Figure 19(d), the lasing wavelength was 453.9 nm with a full width at half maximum (FWHM) of 0.05 nm (spectrometer limited). The increase in output power compared to previous devices was attributed to the greater number of QWs and enhanced multilateral mode operation after switching from the SiO_2 aperture to boron implantation.[62]

Later in 2016, T. Hamaguchi et al. at Sony Corporation reported further analysis of boron ion implantation for lateral carrier confinement in GaN-based VCSELs.[63] Circular transmission line model (CTLM) measurements of ITO-coated LEDs with boron-implanted p-GaN showed less than 1 μA of current flow at an applied voltage of 1 V, which indicates that boron implantation sufficiently blocks current injection and can be used to effectively define a current aperture. This was further supported by another test that showed light successfully confined to the 8-μm-diameter ion implanted current aperture for an LED sample. Based on ellipsometry measurements, boron ion implantation was found to increase the refractive index of GaN from 2.45 to 2.51 at a wavelength of 453 nm. Although higher refractive index extends the cavity length and could result in internal loss due to an anti-

guiding waveguide, it was determined to be an insignificant effect based on the small increase in cavity length of 2.2 nm compared to the relatively long cavity length of 4.5 μm. Boron implantation also increased the absorption coefficient of GaN to a value of 800 cm^{-1} at a wavelength of 453 nm. If a photon traveled within the boron ion implanted region in a VCSEL, calculations suggest that boron implantation would cause an absorption of 0.42% per round trip in the cavity. The measured far field beam profile showed a Gaussian distribution with an emission angle ($1/e^2$) of 2.19°. The Fourier transformation of this angle indicated a Gaussian optical profile with a standard deviation of 3.74 μm. For an 8 μm diameter current aperture, the lateral overlap between the lasing mode and the boron implanted area was calculated to be 10.1%, which corresponds to a negligible amount of absorption (~0.04% per round trip) due to boron implantation. Lastly, boron implantation was found to cause non-radiative recombination in the implanted region but did not degrade the QWs within the aperture.[63]

1.3.3.7. Meijo University

In 2016, K. Matsui et al. at Meijo University demonstrated a GaN-based VCSEL with two MQW active regions, which had a threshold current density of 16.5 kA/cm^2 under CW operation.[60] These used periodic gain structures that consisted of two 5×MQW InGaN/GaN active regions (3-nm-thick InGaN QWs and 6-nm-thick GaN barriers) separated by a 45-nm-thick p-GaN intermediate layer. A hybrid DBR design was employed with an epitaxial 40-period AlInN/GaN DBR on the bottom and an 8-period SiO_2/Nb_2O_5 DBR on top. The optical cavity thickness was 4.5 λ and the operation wavelength was 409.9 nm.[66]

Shortly after, T. Faruta et al. at Meijo University demonstrated room temperature CW operation of a GaN-based VCSEL using relatively thick 6 nm InGaN QWs, which produced a threshold current density of 7.5 kA/cm^2.[60] Using MOCVD on a GaN substrate, the VCSEL

design consisted of a 40-period epitaxial AlInN/GaN DBR, 300 nm n-GaN, 5-period InGaN/GaN MQW with 6-nm-thick InGaN QWs, 15 nm p-AlGaN EBL, 60 nm p-GaN, 10 nm p^{++}GaN contact layer, 20 nm ITO p-contact, 30 nm Nb_2O_5 spacer, 8-period SiO_2/Nb_2O_5 DBR, 4 λ optical cavity thickness, and 413.5 nm peak wavelength. While a 2.0% optical confinement factor was calculated for a 5×MQW with 3-nm-thick QWs (as used in the previous design[66]), a 3.5% confinement factor was estimated for an active region with 6-nm-thick QWs. The lower threshold current density of 7.5 kA/cm^2 (compared to 16.5 kA/cm^2 in the previous design[66]) was attributed to the increased confinement factor for the thicker InGaN MQW design.[60]

Later in 2016, K. Ikeyama et al. at Meijo University demonstrated room temperature CW operation of a GaN-based VCSEL with bottom-side n-type conducting epitaxial AlInN/GaN DBRs.[64] Performing MOCVD on an n-GaN substrate with a carrier concentration of 1×10^{18} cm^{-3}, the epitaxial DBR consisted of a 46-period Si-doped $Al_{0.82}In_{0.18}N$/GaN DBR with the following thicknesses and Si doping concentrations for a single mirror period: 35 nm $Al_{0.82}In_{0.18}N$ ([Si]: 1.5×10^{19} cm^{-3}), 10 nm $Al_{0.82}In_{0.18}N$ ([Si]: 6×10^{19} cm^{-3}), 5 nm n-GaN ([Si]: 6×10^{19} cm^{-3}), and 35 nm n-GaN ([Si]: 1×10^{18} cm^{-3}). This modulation scheme with high Si concentrations at the top of AlInN interfaces with GaN was implemented to neutralize the high negative polarization charge concentration at AlInN/GaN interfaces and obtain a low vertical electrical resistance through the interfaces. The VCSEL structure above the bottom DBR consisted of 50 nm n-GaN, 5-period InGaN/GaN MQW with 3 nm InGaN QWs and 6 nm GaN barriers, 20 nm p-$Al_{0.2}Ga_{0.8}N$ EBL, 60 nm p-GaN, 10 nm p^{++}GaN, 20 nm SiO_2 current aperture (8 μm aperture diameter), 20 nm ITO p-electrode, 32 nm Nb_2O_5 spacer, 8-period SiO_2/Nb_2O_5 top DBR, and a 1.5 λ optical cavity thickness. The n-type AlInN/GaN bottom

DBR showed ohmic behavior and a high reflectivity ~99.9%.While the previous VCSEL design with an electrically-insulating AlInN/GaN bottom DBR had a threshold current density of 7.5 kA/cm^2,[60] the n-type epitaxial bottom DBR VCSEL had a lower threshold current density of 5.2 kA/cm^2 at a lasing wavelength of 405.1 nm.[64]

At the 2016 International Semiconductor Laser Conference, T. Furuta et al. at Meijo University reported the highest peak output power for a GaN-based VCSEL, reaching a peak output power of 1.7 mW at a wavelength of 407 nm.[59] The VCSEL structure was equivalent to the thick InGaN QW design reported earlier,[60] consisting of a 4 λ cavity, hybrid DBR design, and a 5×MQW active region consisting of 6 nm InGaN QWs and 6 nm GaN barriers. The 7× increase in output power Compared to the peak output power of 0.32 mW for the previous design,[60] a higher peak output power of 1.7 mW was achieved with a differential quantum efficiency of 11.5% and threshold current of 4.5 mA. The higher peak output power was attributed to growth optimization and improvements in layer thickness.[59]

In 2018, N. Hayashi et al. at Meijo University demonstrated a GaN-based VCSEL with a convex structure for optical guiding, which reached a peak output power of 0.88 mW and threshold current of 2 mA.[75] Figure 20(a) shows a schematic illustration of the hybrid DBR VCSEL design.

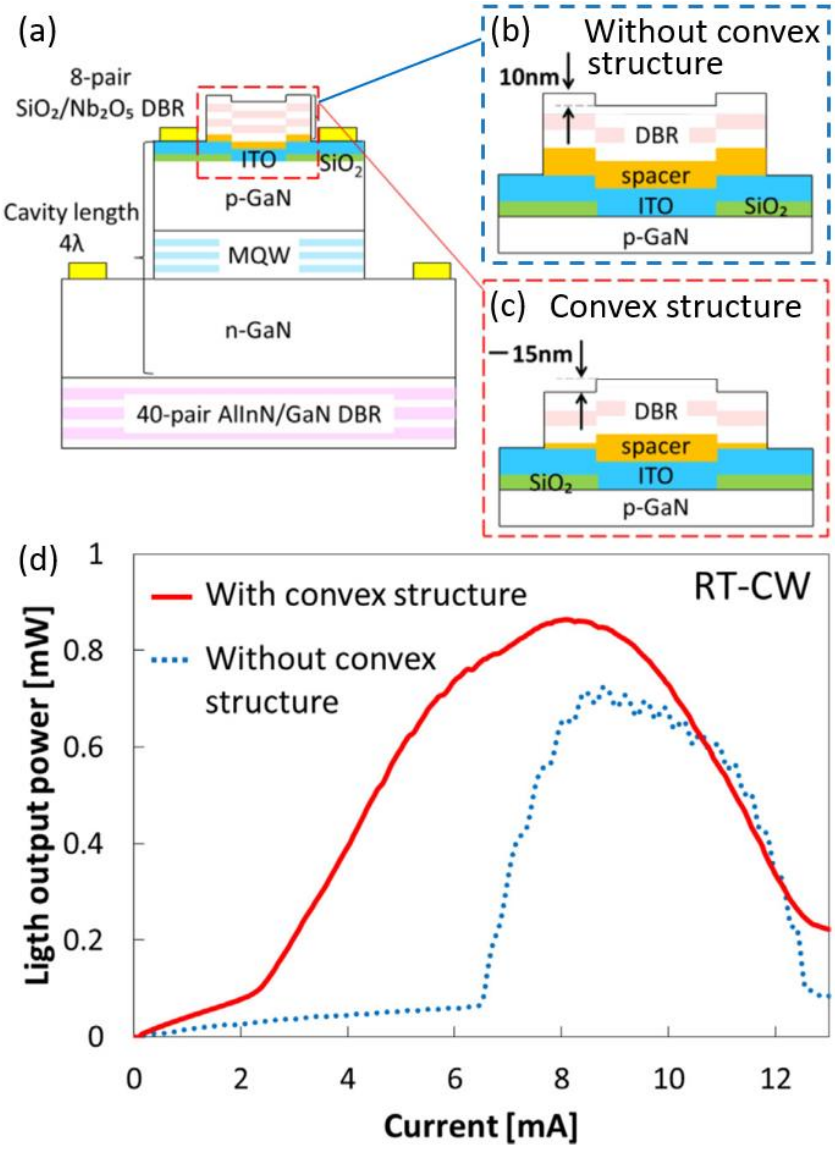


Figure 20. (a) Schematic diagram of the hybrid DBR GaN-based VCSEL design from Meijo University showing (b) the standard VCSEL design without the convex structure for optical guiding and (c) with the convex structure for optical guiding. (d) *L-I-V* characteristic for VCSELs with and without the convex structure for optical guiding.[75] Figures adapted from [Natsumi, H., Junichiro, O., Kenjo, M., Takashi, F., Takanobu, A., Sho, I., Isamu, A. (2018). A GaN-Based VCSEL with a Convex Structure for Optical Guiding. Physica Status Solidi (A), 0(0), 1700648. https://doi.org/10.1002/pssa.201700648] with the permission of AIP Publishing. © 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

The VCSEL design consisted of a 40-period lattice-matched AlInN/GaN bottom DBR, 1.5 λ optical cavity thickness, 5-period InGaN/GaN MQW with 3 nm InGaN QWs and 6 nm GaN barriers, p-AlGaN EBL, p-GaN, 250-nm-thick SiO_2 current aperture, 20 nm ITO p-electrode, Nb_2O_5 spacer, and 8-period SiO_2/Nb_2O_5 top DBR. Two different VCSEL designs

were fabricated simultaneously on the same wafer: a standard VCSEL design without a convex structure and a VCSEL design with a convex structure for optical guiding. As shown in Figure 20(b) for the standard VCSEL design (without a convex structure), the Nb_2O_5 spacer layer was deposited with the same thickness inside and outside the aperture, leading to a concave shape and anti-guiding. Figure 20(c) illustrates the VCSEL design with a convex structure for optical guiding, which was fabricated by depositing a thinner 7-nm-thick Nb_2O_5 spacer outside the aperture, and a convex structure was created as the spacer was 15 nm thicker within the aperture compared to outside. After depositing the top DBR, the backside of the GaN growth substrate was polished to measure the light output power from the backside. The convex structure had a lower threshold current (~ 2 mA) compared to the VCSEL without a convex structure, as shown in the *L-I* characteristic in Figure 20(d) that was measured from the bottom DBR. The higher peak output power of 0.88 mW was further attributed to the higher optical confinement of the convex structure. However, as seen by the slope of the *L-I* curve, the differential efficiency appeared greater for the VCSEL without a convex structure, which may be due to a thermal lensing effect that appears at higher injection levels. Figure 21(a) shows calculated effective refractive index values for possible linearly polarized (LP) modes as a function of the relative refractive index difference, Δn/n, as described by

$$\frac{\Delta n}{n} = \frac{\lambda_c - \lambda_p}{\lambda} \tag{16}$$

where λ_c is resonance wavelength inside the aperture, λ_p is the resonance wavelength outside the aperture, and λ is the wavelength of light.

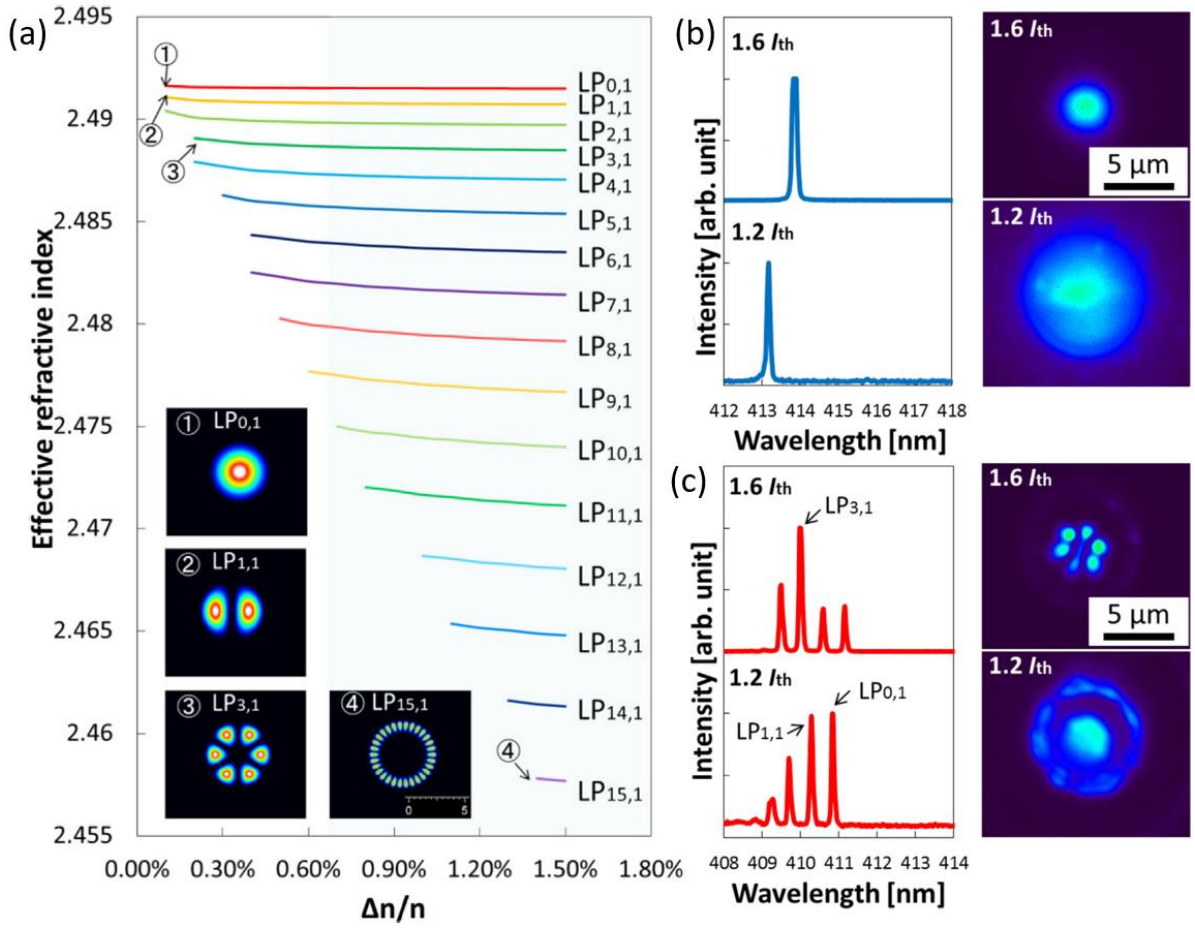


Figure 21. (a) Calculated effective refractive indices of possible LP modes in a 6 μm diameter core as a function of *Δn/n* and the inset shows selected corresponding simulated near field patterns. The measured emission spectra and near field patterns are shown for a VCSEL (b) without the convex structure for optical guiding and (c) with the convex structure for optical guiding.[75] Figures adapted from [Natsumi, H., Junichiro, O., Kenjo, M., Takashi, F., Takanobu, A., Sho, I., Isamu, A. (2018). A GaN-Based VCSEL with a Convex Structure for Optical Guiding. Physica Status Solidi (A), 0(0), 1700648. https://doi.org/10.1002/pssa.201700648] with the permission of AIP Publishing. © 2018 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim

As for the VCSEL with a convex structure, optical guiding can be obtained when $\lambda_c - \lambda_p$ is positive, and the VCSEL had a calculated Δn/n value of 1.5%. As shown in Figure 21(a) increasing the optical confinement can result in higher order lateral LP modes, which are illustrated in the inset for four different near field patterns. The emission spectra and near field patterns are shown in Figure 21(b) for the VCSEL without the convex structure, which exhibited the fundamental lateral mode ($LP_{0,1}$) because there was no strong optical confinement. On the other hand, the relatively strong optical confinement for the VCSEL with

the convex structure resulted in higher order mode emission, as shown in Figure 21(c). In summary, the convex structure VCSEL increased the optical confinement, lowered the threshold, increased the peak output power, and resulted in multi-mode operation.[75]

Later in 2018, M. Kuramoto et al. at Meijo University reported the highest output power of a GaN-based VCSEL, reaching 6 mW at a lasing wavelength of 441 nm.[74] This consisted of a hybrid DBR VCSEL design using a SiO_2-buried lateral optical confinement structure and current aperture, as illustrated in Figure 22(a).

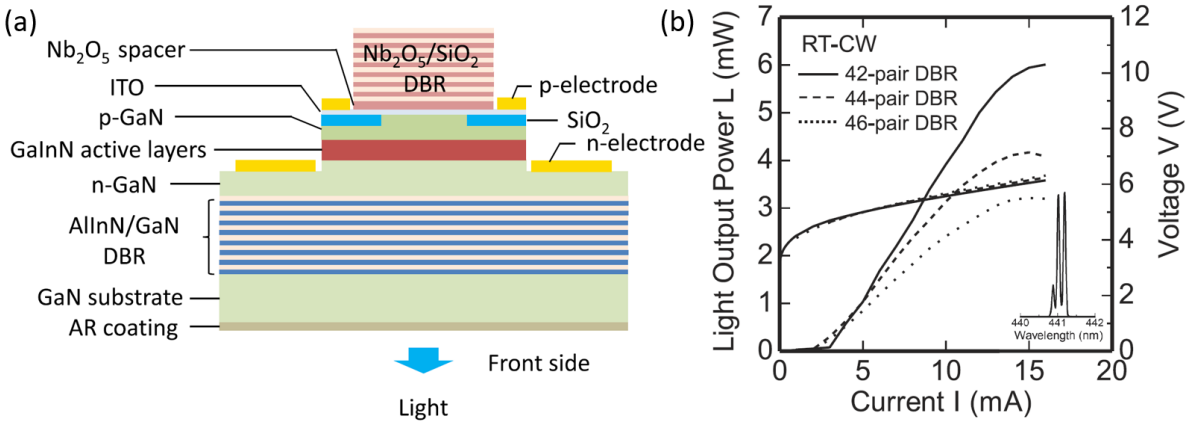


Figure 22. (a) Schematic diagram of the hybrid DBR GaN-based VCSEL design from Meijo University. (b) *L-I-V* characteristic for VCSELs with different numbers of mirror periods for the bottom epitaxial DBR. The inset shows the emission spectrum. Reprinted from [Kuramoto, M., Kobayashi, S., Akagi, T., Tazawa, K., Tanaka, K., Saito, T., & Takeuchi, T. (2018). Enhancement of slope efficiency and output power in GaN-based vertical-cavity surface-emitting lasers with a SiO2-buried lateral index guide. Applied Physics Letters, 112(11), 111104. https://doi.org/10.1063/1.5020229] with the permission of AIP Publishing.[74]

Using MOCVD on a GaN substrate, the VCSEL design consisted of a lattice-matched AlInN/GaN bottom DBR, 570 nm n-GaN, 5-period InGaN/GaN MQW with 3 nm InGaN QWs and 4 nm GaN barriers, 20 nm p-$Al_{0.15}Ga_{0.85}N$ EBL, 75 nm p-GaN, 20-nm-thick buried SiO_2 current aperture (8 μm diameter), 20 nm ITO p-electrode, 38 nm Nb_2O_5 spacer, 10.5-period SiO_2/Nb_2O_5 top DBR, and a 4.5 λ optical cavity thickness. The buried SiO_2 structure was fabricated by using RIE to etch 20 nm into the p-GaN prior to depositing 20 nm of SiO_2.

After depositing n- and p-electrodes, the backside of the GaN substrate was polished and coated with a 4-period SiO_2/Nb_2O_5 anti-reflection coating. After flip-chip bonding to a copper heat sink, the light output power versus current was measured under CW operation, as shown in Figure 22(b). The VCSEL with a 42-pair epitaxial AlInN/GaN DBR reached the highest peak output power of 6 mW with a threshold current of 3 mA (6.0 kA/cm^2). The multiple kinks in the *L-I* curve were attributed to multimode lasing, and the multimode spectra at a lasing wavelength of 441 nm is shown in the inset of Figure 22(b). The slope efficiency was 0.64 W/A (0.87 W/A under pulsed operation) and the differential efficiency was 23% (32% under pulsed operation). These improvements and higher peak output power were attributed to the reduction of internal loss by introducing the SiO_2 buried lateral optical confinement structure.[74]

1.3.4. *m*-plane GaN-Based VCSELs

While the majority of the reported GaN-based VCSELs have used the polar *c*-plane orientation of GaN, nonpolar *m*-plane GaN offers several unique advantages. The absence of the quantum confined Stark effect (QCSE) in nonpolar InGaN/GaN QWs leads to several advantages, such as increasing the electron-hole wave function overlap.[16] While *c*-plane devices are constrained to relatively thin QWs to minimize the QCSE, *m*-plane devices have more flexibility in the design space as thicker InGaN QW active region designs are possible without suffering from reduced radiative efficiency.[20] Furthermore, nonpolar *m*-plane devices have anisotropic gain that leads to a 100% polarization ratio for *m*-plane GaN-based VCSELs.[3,4] While individual *c*-plane GaN VCSELs have been reported to have up polarization ratios up to ~96%,[69] they have random directions of linear polarization from device to device, which means that a *c*-plane VCSEL array effectively has a polarization ratio

that approaches 0%. In contrast, *m*-plane GaN VCSELs are consistently polarized along the *a*-direction,[29] which enables inherently polarization-locked VCSEL arrays.[29] Linearly polarized emission is desirable for several applications; for example, the optics in virtual and augmented head mounted displays can be sensitive to polarization. While an unpolarized light source can be used with a linear polarizer, ~50% of the light is lost. Therefore, for several polarization-sensitive applications, inherently polarized light sources are ideal because they are more efficient and do not require additional polarizer optical filters.

There have been several reports of nonpolar *m*-plane GaN VCSEL designs from UCSB that implement a dual-dielectric DBR flip-chip design. These devices have had various current aperture and intracavity contact designs, including dielectric apertures,[4,29] ion implanted apertures,[3,58] air-gap apertures,[65] ITO intracavity contacts,[3,4,29] and GaN-based tunnel junction intracavity contacts with current spreading layers grown by molecular beam epitaxy (MBE).[58] The following sections delve into the details of these different designs and their corresponding impact on performance. While there have been significant VCSEL performance improvements over the years, the most significant challenge has been that none of these devices could lase under CW operation. Having a clear understanding of the results from these previous *m*-plane GaN VCSEL designs has been very useful when pursuing the primary goal in this thesis of achieving CW operation, as discussed in Section 4.

1.3.4.1. ITO VCSEL with Dielectric Aperture

In 2012, C. Holder and colleagues at UCSB reported the first nonpolar *m*-plane GaN-based VCSEL that had a threshold current of 70 mA, peak output power of 19.5 μW, and lasing wavelength of 411.9 nm under pulsed operation.[29] These devices had a dual-dielectric DBR design and used a unique flip-chip process involving PEC etching to selectively remove

the GaN growth substrate with precise cavity length control. Similar to other reported devices, the *m*-plane GaN VCSEL had an ITO intracavity contact and a dielectric current aperture consisting of SiN_x. Figure 23(a) shows an illustration of the dual-dielectric DBR and flip-chip VCSEL design.

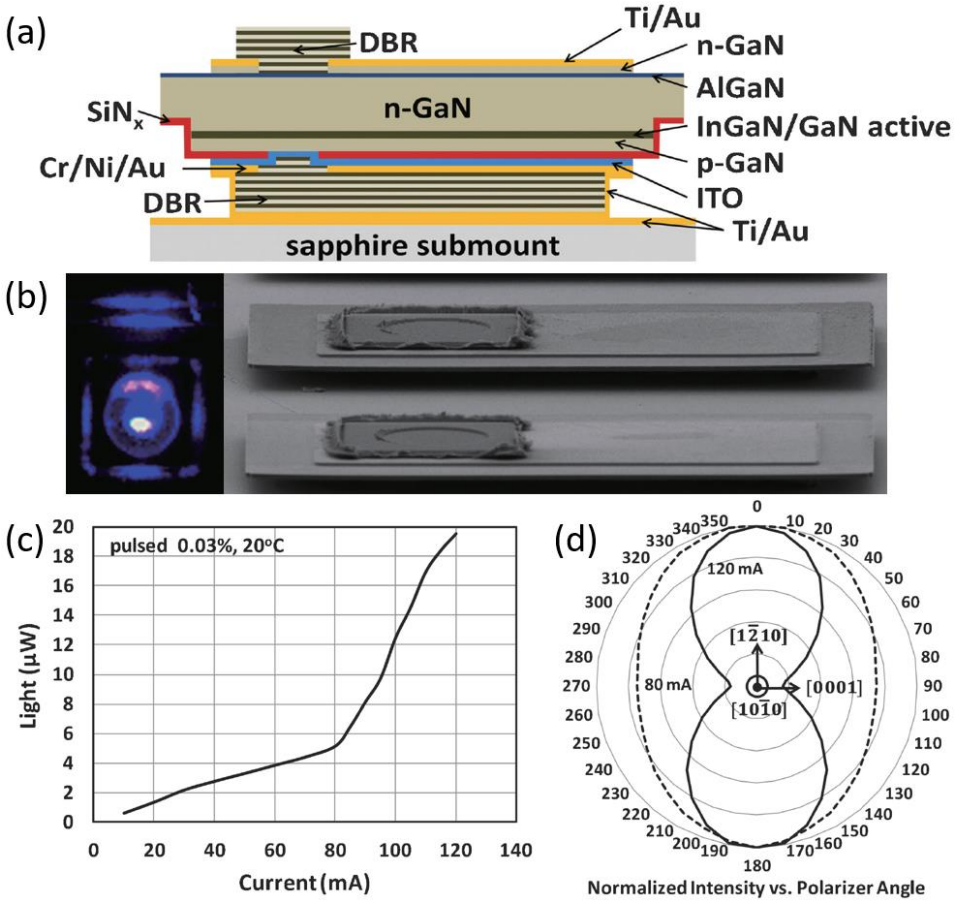


Figure 23. (a) Schematic diagram of the dual-dielectric DBR flip-chip VCSEL design from UCSB with a SiN_x current aperture and ITO intracavity contact. (b) Optical micrograph of a device lasing under pulsed operation (left) and a SEM image of multiple completed devices (right). (c) *L-I-V* characteristic under pulsed operation with a duty cycle of 0.03%. (d) Plot of normalized intensity versus polarizer angle at different current injection levels, showing polarized emission along the *a*-direction of the wurtzite crystal structure. Reprinted from [Holder, C., Speck, J. S., DenBaars, S. P., Nakamura, S., & Feezell, D. (2012). Demonstration of nonpolar GaN-based vertical-cavity surface-emitting lasers. In K. D. Choquette & J. K. Guenter (Eds.), Applied Physics Express (Vol. 5, p. 863906). IOP Publishing. https://doi.org/10.1143/APEX.5.092104] with the permission of AIP Publishing.[29]

The VCSEL growth and fabrication process is described as follows. MOCVD was performed on a free-standing *m*-plane GaN substrate with an intentional 1° miscut in the negative *c*-direction and the epitaxial structure consisted of a sacrificial 3-period $In_{0.12}Ga_{0.88}N$/GaN (7

nm/5 nm) MQW, 50 nm n-GaN for metal contact, 15 nm $Al_{0.30}Ga_{0.70}N$ hole blocking layer, thicker n-GaN for the cavity, active region 5×MQW with 7 nm $In_{0.10}Ga_{0.90}N$ QWs and 5 nm GaN barriers, 15 nm p-$Al_{0.20}Ga_{0.80}N$ EBL, and p-GaN. After performing a dry etch past the active region but not past the sacrificial region, SiN_x was deposited to define the current aperture and to coat the sidewall of the active region to protect it from etching during a PEC etching step later on. Electron cyclotron resonance sputtering was used to deposit 50 nm of ITO (λ/4-wave) to serve as the p-type ohmic intracavity contact and current spreading layer. After depositing a metal ring around the aperture, a λ/8-wave Ta_2O_5 interlayer was deposited to align the high-absorption ITO layer with the node of the optical standing wave, and the p-side 13-period SiO_2/Ta_2O_5 DBR was deposited. A deeper dry etch was performed to expose the sidewall of the sacrificial MQW, and metal was patterned to form the bonding pad and p-contact. After flip-chip gold-gold (Au-Au) thermocompression bonding to a gold-coated sapphire submount, the GaN growth substrate was removed by performing a selective PEC lateral etch of the sacrificial MQW. PEC undercut etching was performed using aqueous potassium hydroxide (KOH) and a 405 nm laser. This is a bandgap-selective etch as the 405 nm laser light only creates photogenerated holes in the sacrificial MQW, which causes oxidation and the oxide subsequently dissolves in the KOH solution as the etch progresses. To prevent the active MQW from etching, SiN_x was deposited on the sidewall, as described previously. Because the sacrificial layer was grown by MOCVD, this PEC etching method achieves precise cavity length control, in contrast with other flip-chip VCSEL designs that removed the growth substrate using thinning and polishing. Furthermore, after depositing ohmic ring n-contacts, another PEC etch was performed to etch n-GaN down to the $Al_{0.30}Ga_{0.70}N$ etch-stop layer, which was used to define the 7.5 λ cavity length. Lastly, a 10-

period SiO_2/Ta_2O_5 top DBR was deposited. Figure 23(b) shows an optical micrograph of a device lasing under pulsed operation (left image) and a SEM image of completed devices (right image). As shown in the *L-I-V* measurement in Figure 23(c), the peak output power was 19.5 μW with a threshold current of ~ 70 mA under pulsed operation. Unlike *c*-plane devices, these *m*-plane GaN VCSELs were found to be consistently polarized along the $[1\bar{2}10]$ *a*-direction of the wurtzite crystal structure, as shown in Figure 23(d).[29]

In 2014, C. Holder et al. at UCSB demonstrated *m*-plane GaN-based VCSELs with emission polarized along the *a*-direction with a polarization ratio of 100%.[4] The VCSEL had a similar structure to the previous design,[29] and further details about the fabrication process were described. The epitaxial structure consisted of a ~2 μm n-GaN template, sacrificial 3-period $In_{0.12}Ga_{0.88}N$/GaN (7 nm/5 nm) MQW emitting at 415 nm, 50 nm n-GaN contact region, 15 nm $Al_{0.30}Ga_{0.70}N$ hole blocking layer and etch-stop, ~902 nm n-GaN, active region 5×MQW with 7 nm $In_{0.10}Ga_{0.90}N$ QWs and 5 nm GaN barriers, 15 nm p-$Al_{0.2}Ga_{0.8}N$ EBL, 113 nm p-GaN, 14 nm p^{++}GaN contact layer, and designed cavity length of 7.5 λ. As described in the previous report,[29] the VCSEL had a dual-dielectric DBR and flip-chip design that used a PEC undercut etch to selectively etch the sacrificial MQW to remove the GaN growth substrate. The PEC undercut etch was performed using a solution of 0.1 M KOH and a 405 nm CW laser to electrons and holes in the sacrificial MQW. Photogenerated holes diffused to the sidewall of the sacrificial MQW, assisting the oxidation of gallium atoms, and the resulting oxide was subsequently dissolved in the KOH solution as the etch progressed. Photogenerated electrons were eliminated by a reduction reaction at a Ti/Au cathode on the *m*-plane GaN substrate, as shown in Figure 24(a), which shows a schematic illustration of the structure after flip-chip bonding and before the PEC undercut etch.

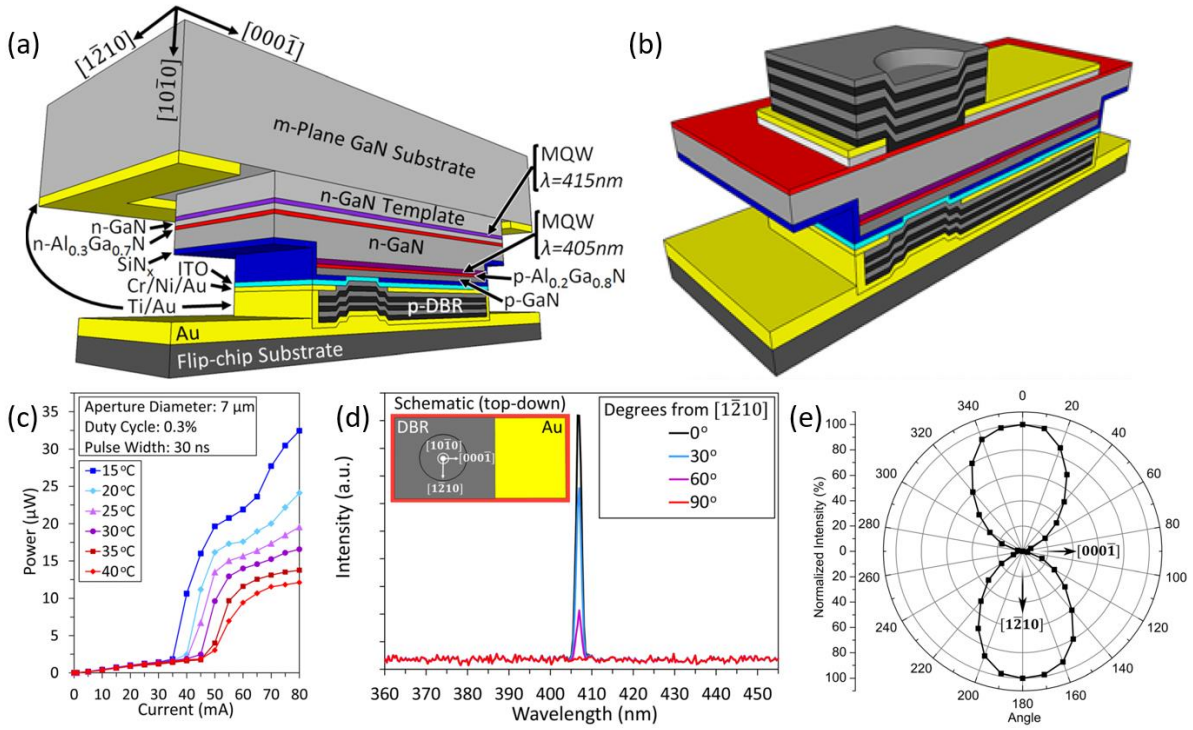


Figure 24. (a) Schematic illustration of the VCSEL structure after flip-chip bonding but prior to PEC undercut etching of the sacrificial MQW. (b) Schematic illustration of the completed VCSEL. (c) *L-I-V* characteristic under pulsed operation at various stage temperatures. (d) Emission spectra at various polarizer angles. (e) Normalized emission intensity versus polarizer angle showing 100% polarized emission along the *a*-direction of the wurtzite crystal structure. Reprinted from [Holder, C. O., Leonard, J. T., Farrell, R. M., Cohen, D. A., Yonkee, B., Speck, J. S., Feezell, D. F. (2014). Nonpolar III-nitride vertical-cavity surface emitting lasers with a polarization ratio of 100% fabricated using photoelectrochemical etching. Applied Physics Letters, 105(3), 31111. https://doi.org/10.1063/1.4890864] with the permission of AIP Publishing.[4]

After depositing an n-contact metal ring, the PEC top-down etch was performed in 0.01 M KOH solution with illumination by a Hg-Xe arc lamp with a 320 nm long-pass filter. Illumination at wavelengths below 365 nm was necessary to etch the 50 nm of n-GaN within the aperture, but the 320 nm long-pass filter prevented the n-AlGaN ($\lambda \sim 310$ nm) from etching. Additionally, the n-AlGaN layer served as a hole blocking layer to prevent holes generated in the cavity region from participating in the etch. Therefore, the n-AlGaN layer enabled precise cavity length control for this design. The etch selectivity was measured and showed an etch rate of 30.7 nm/min for n-GaN while n-AlGaN etched at a much slower rate of 0.12 nm/min.

Atomic force microscope (AFM) scans showed a smooth morphology with a root mean square (RMS) roughness of 0.53 nm, which is comparable to MOCVD-grown layers. Lastly, the top 10-period SiO_2/Ta_2O_5 DBR was deposited, as shown in the schematic in Figure 24(b). Figure 24(c) shows pulsed *L-I-V* measurements at various stage temperatures, showing the threshold current varying from 34 mA at 15 °C to 48 mA at 40 °C. The peak lasing wavelength was 407 nm at 20 °C and was found to vary with temperature at a rate of 0.015 nm/K. Figure 24(d) shows spectra at various polarization angles, which shows no emission polarized in the *c*-direction and a maximum intensity emission polarized in the *a*-direction. The normalized intensity versus polarizer angle is shown in Figure 24(e), which demonstrates a polarization ratio of 100% for *m*-plane GaN-based VCSELs.[4]

1.3.4.2. Ion Implanted Aperture

In 2015, J. Leonard et al. at UCSB demonstrated the first GaN-based VCSEL that used aluminum ion implantation to define the current aperture, reaching a peak output power of 12 μW with a threshold current density of 16 kA/cm^2.[3] A schematic of the nonpolar *m*-plane GaN-based dual-dielectric DBR design is shown in Figure 25(a).

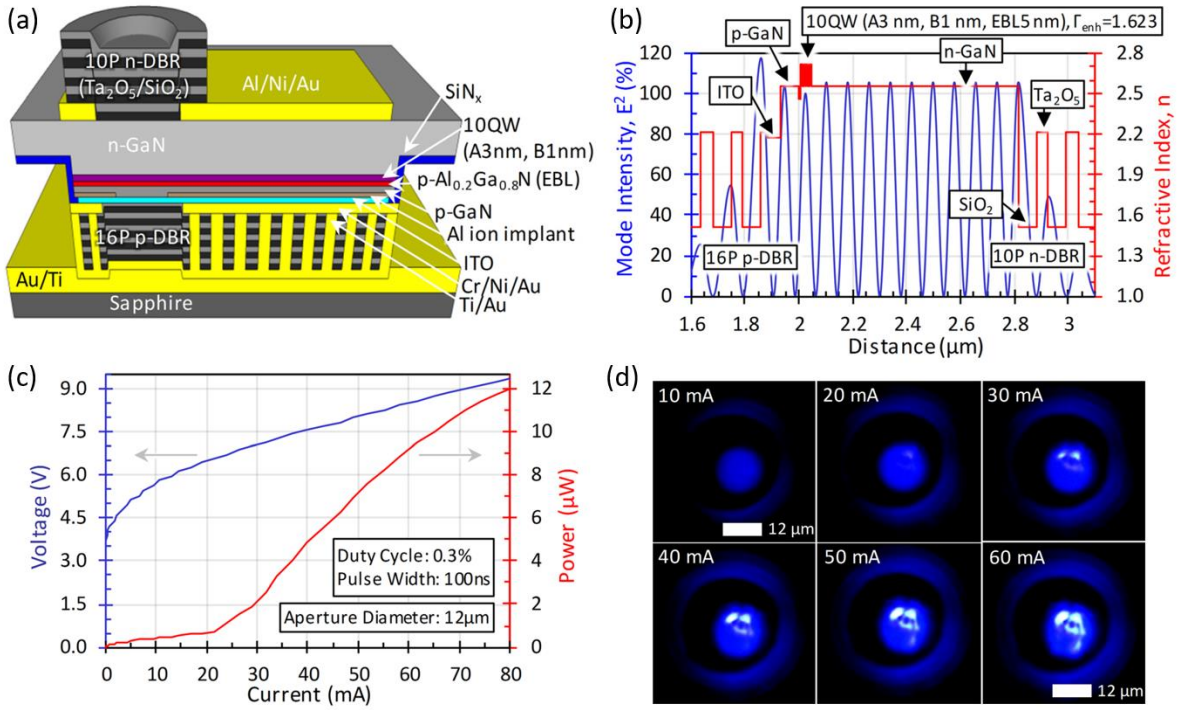


Figure 25. (a) Schematic diagram of the dual-dielectric DBR flip-chip VCSEL design incorporating an aluminum ion implanted current aperture (b) Optical mode and index profile within the cavity. (c) *L-I-V* characteristic for a 12 μm aperture diameter VCSEL under pulsed operation, (d) Optical micrographs within the aperture at various current injection levels. Reprinted from [Leonard, J. T., Cohen, D. A., Yonkee, B. P., Farrell, R. M., Margalith, T., Lee, S., Nakamura, S. (2015). Nonpolar III-nitride vertical-cavity surface-emitting lasers incorporating an ion implanted aperture. Applied Physics Letters, 107(1), 11102. https://doi.org/10.1063/1.4926365] with the permission of AIP Publishing.[3]

The epitaxial structure consisted of a ~1.2 μm n-GaN template, sacrificial 3-period InGaN/GaN (7 nm/5 nm) MQW emitting at 415 nm, 50 nm n^{++}GaN, ~770 nm n-GaN, active region 5×MQW with 3 nm InGaN QWs and 1 nm GaN barriers, 5 nm p-$Al_{0.2}Ga_{0.8}N$ EBL, 56 nm p-GaN, 14 nm p^{++}GaN contact layer, and optical cavity length of ~6.95 λ. After depositing a Ti/Au hardmask atop the p^{++}GaN to protect the aperture, aluminum ion implantation was carried out by Leonard Kroko, Inc. to form the current aperture. After implantation, aqua regia was used to remove the metal hardmask and the remaining fabrication process was similar to the previous design, consisting of ~47 nm ITO intracavity contact deposition by electron beam evaporation, SiN_x deposition to protect the sidewall of the active region, 16-period p-side Ta_2O_5/SiO_2 DBR deposition incorporating a λ/8-wave Ta_2O_5 spacer next to ITO, Ti/Au PEC

cathode and p-pad deposition, flip-chip bonding to a sapphire submount coated with Ti/Au (i.e., 200 °C for 2 hours using a graphite compression fixture), PEC undercut etching for substrate removal, Al/Ni/Au n-contact deposition, and deposition of a 10-period Ta_2O_5/SiO_2 DBR. Note that a PEC top-down etch was not performed and this design did not incorporate an n-AlGaN etch-stop layer. Figure 25(b) shows the optical mode intensity and index profile for the design, and Figure 25(c) shows the *L-I-V* characteristics measured under pulsed operation. For a lasing wavelength at 406 nm, the peak output power was 12 μW with a threshold current of 18 mA (16 kA/cm^2) for a 12 μm aperture diameter VCSEL. Unlike the previous design with a SiN_x current aperture,[4,29] Al ion implantation was found to decrease the refractive index by ~2% and enables a planar ITO design (i.e., no height change in the ITO and DBR layers at the edge of the aperture) because implantation does not affect the height of the p-GaN surface. Simulations by E. Hashemi et al. suggest that having a low index layer outside the aperture and a planar ITO design can significantly reduce internal loss in III-nitride VCSELs.[120,121] Therefore, the ~5× decrease in the threshold current density compared to the previous design with a SiN_x aperture was attributed to the ion implanted current aperture with a planar ITO design. Optical micrographs of the VCSEL aperture at various currents are shown in Figure 25(d), which show non-uniform lasing. This has been described as filamentary lasing, which has an unknown origin but may be caused by inhomogeneity in material composition, surface morphology, current spreading, or lateral index fluctuations.[3]

1.3.4.3. PEC Air-Gap Aperture

In 2016, J. Leonard et al. at UCSB demonstrated an *m*-plane GaN-based VCSEL with a PEC etched air-gap aperture that had a threshold current of 25 mA (22 kA/cm^2) and a peak output power of 180 μW.[65] Similar to previous *m*-plane GaN VCSELs,[3,4,29,30,58] the VCSEL employed a dual-dielectric DBR and flip-chip design using PEC undercut etching to remove the growth substrate. The air-gap aperture was fabricated using a similar procedure as the PEC undercut etch of a sacrificial MQW for growth substrate removal. After MOCVD growth and p-GaN activation, a dry etch was performed to define a mesa and expose the active MQW sidewall. A Ti/Au mask was deposited within the aperture of the device to serve as the PEC cathode and to protect the active MQW within the aperture. To form an air-gap aperture, the MQW outside the aperture area was laterally etched by PEC etching using a 405 nm LED array and 0.1 M KOH solution. The opaque metal mask prevented PEC etching within the aperture area because photogenerated holes created by above-band-gap illumination are required for PEC etching. A schematic illustration of the VCSEL structure after forming the PEC air-gap aperture is shown in Figure 26(a).

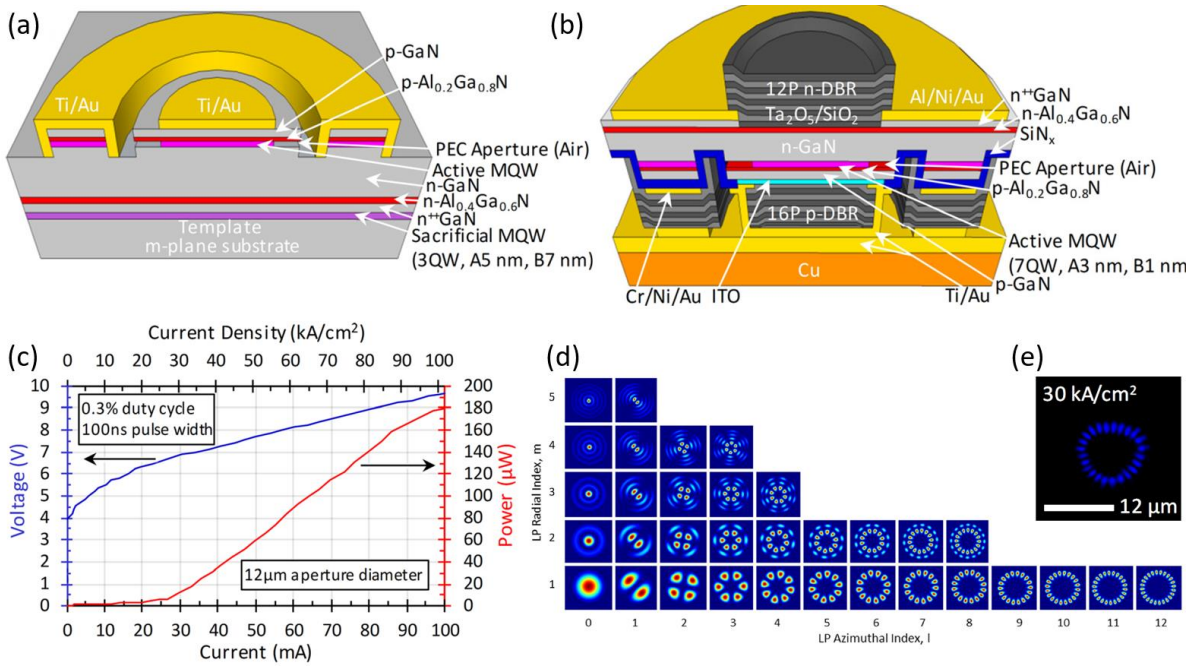


Figure 26. (a) Schematic diagram of a partially processed VCSEL after the PEC air-gap aperture was defined (b) Schematic illustration of the dual-dielectric DBR flip-chip VCSEL design with PEC air-gap aperture (c) *L-I-V* characteristic for a 12 μm aperture diameter VCSEL under pulsed operation. (d) Simulated linearly polarized ($LP_{l,m}$) mode profiles as a function of the radial mode index, *m*, and azimuthal modal index, *l*. (e) Optical micrograph within the aperture at a current density of 30 kA/cm^2, showing a high-order lateral optical mode ($LP_{12,1}$). Reprinted from [Leonard, J. T., Yonkee, B. P., Cohen, D. A., Megalini, L., Lee, S., Speck, J. S., … Nakamura, S. (2016). Nonpolar III-nitride vertical-cavity surface-emitting laser with a photoelectrochemically etched air-gap aperture. Applied Physics Letters, 108(3), 031111. https://doi.org/10.1063/1.4940380] with the permission of AIP Publishing.[65]

After the air-gap aperture was formed, aqua regia was used to remove the metal hardmask and the VCSEL was fabricated using the methods described in previous reports.[3,4,29,58] Figure 26(b) shows a schematic of the completed dual-dielectric DBR VCSEL structure with an air-gap aperture and ITO intracavity contact. The active region consisted of a 7×MQW with 3 nm InGaN QWs and 1 nm GaN barriers, and the cavity length was 6.95 λ. FIB cross-section SEM images confirmed the presence of an air-gap thickness of ~30 nm, which is similar to the active MQW thickness. As shown in the *L-I-V* characteristic under pulsed operation in Figure 26(c), the threshold current was ~25 mA (22 kA/cm^2) and the peak output power was 180 μW. While the spontaneous emission was centered at ~405 nm, the peak lasing wavelength was ~417 nm, which was due to an unintentional Ta_2O_5 spacer deposited prior to the n-DBR. This

gain offset factor could potentially explain the higher threshold compared to the ion implant aperture VCSEL. The top-side differential efficiency was ~0.07% and the differential resistance was ~42.82 Ω. While previous *m*-plane VCSELs exhibited filamentary lasing within the aperture without clear linear polarized (LP) lateral optical modes, the air-gap aperture VCSEL exhibited a high order lateral optical lasing mode. Figure 26(d) shows COMSOL simulations of several LP mode profiles, which are organized by the radial modal index, l, and azimuthal index, m ($LP_{l,m}$). The PEC air-gap aperture VCSEL showed $LP_{12,1}$ lasing, as demonstrated by the near field pattern shown in the optical micrograph in Figure 26(e). Lower order modes likely did not lase due to the large spreading resistance on the p- and n-sides, which could result in more injected current near the edges of the aperture compared to the center. High order mode emission is further supported by the relatively large core-cladding index contrast for the air-gap aperture that increases the normalized frequency. The absence of higher order modes above $LP_{12,1}$ was attributed to higher levels of scattering loss for those modes. Compared to a similar ion implanted aperture VCSEL reported earlier, the air-gap aperture VCSEL had a higher threshold current density (22.1 kA/cm^2 compared to 8 kA/cm^2) and a higher peak output power (180 μW compared to 80 μW), but further experimentation would be required to give a direct comparison between aperture designs.[65]

1.3.4.4. Tunnel Junction Intracavity Contact

This section describes the highest performing GaN-based VCSEL design from UCSB that was reported prior to the advancements described in this thesis. In 2015, J. Leonard et al. at UCSB demonstrated an *m*-plane GaN VCSEL with an ion implanted current aperture and III-nitride tunnel junction (TJ) intracavity contact grown by molecular-beam epitaxy (MBE).[58] The general structure of the VCSEL design was similar to the earlier ion implanted VCSEL

design with ITO intracavity contact reported earlier,[3] but there were a few notable changes. The most significant change was that the highly-absorbing ITO intracavity contact was replaced by an n^{++}GaN TJ and current spreading layer grown by MBE. Ammonia MBE was chosen for regrowth of n-GaN layers because the low hydrogen levels do not result in hydrogen passivation of MOCVD-grown p-GaN layers. The MBE regrowth consisted of n^{++}GaN/n^{+}GaN/n^{++}GaN/n-GaN (39.6 nm/39.6 nm/39.6 nm/22.1 nm) with a silicon concentration of 1.1×10^{20} cm^{-3} for n^{++}GaN and 1×10^{19} cm^{-3} for n^{+}GaN. There were also some changes in the VCSEL design regarding the n-GaN and p-GaN thicknesses to account for a 7×MQW active region instead of a 10×MQW, and an n-$Al_{0.4}Ga_{0.6}N$ etch-stop layer was employed to define the cavity length via a top-down etch. Lastly, the devices were flip-chip bonded to a Ti/Au copper submount instead of sapphire. Figure 27(a) summarizes the layer thicknesses, refractive indices, and absorption coefficients of the various materials in the VCSEL design.

(a)

Layer			Thickness (nm)	Index, n	Abs. Coeff., α (cm^{-1})
Air ($\lambda/4$)			101.25	1	0
12P n-DBR ($SiO_2 + Ta_2O_5$)			66.8 + 45.6	2.22 + 1.52	0
n-$Al_{0.4}Ga_{0.6}N$			15	2.414	10
n-GaN			762.65	2.557	10
7× MQW $\lambda = 405$		GaN	1	2.557	5
		InGaN	3	2.72	$-g_{th}$
		GaN	1	2.557	5
p-$Al_{0.25}Ga_{0.75}N$ (EBL)			5	2.456	40
p-GaN			62.2	2.557	40
P^{++}GaN			14		150
Intracavity contact		**ITO ($\lambda/4$)**	**46.7**	**2.17**	**2000**
	TJ	**n^{++}GaN**	**39.6**		**100**
		n-GaN	**39.6**	**2.557**	**15**
		n^{++}GaN	**39.6**		**100**
		n-GaN	**22.1**		**15**
Ta_2O_5 ($\lambda/8$) (ITO VCSEL only)			**22.802**	**2.220**	**0**
16P p-DBR ($SiO_2 + Ta_2O_5$)			66.8 + 45.6	2.22+1.52	0
SiO_2 ($\lambda/5.2$)			51.37	1.516	0
Ti			10	2.046	893 740
Au ($\lambda/4$)			61.37	1.65	607 141

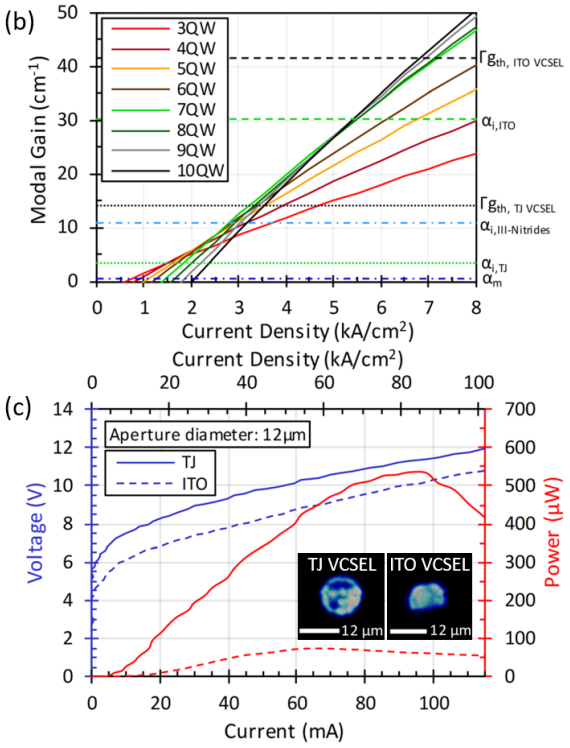


Figure 27. (a) Simulated modal gain versus current density for 405 nm VCSELs (6.95 λ cavity length) with various numbers of QWs, showing a breakdown of the sources of loss in the cavity. (b) Summary of the VCSEL parameters used in the TMM simulation of the 405 nm cavity mode. (c) *L-I-V* characteristic for a 12 μm aperture diameter VCSEL under pulsed operation with optical micrographs during lasing operation shown in the inset. Reprinted from [Leonard, J. T., Young, E. C., Yonkee, B. P., Cohen, D. A., Margalith, T., DenBaars, S. P., … Nakamura, S. (2015). Demonstration of a III-nitride vertical-cavity surface-emitting laser with a III-nitride tunnel junction intracavity contact. Applied Physics Letters, 107(9), 091105. https://doi.org/10.1063/1.4929944] with the permission of AIP Publishing.[58]

These values were used in a transmission matrix method (TMM) simulation to give a general idea of the internal loss of the structures. Using the confinement factor from TMM simulations and gain versus current density data for a 405 nm m-plane edge-emitting laser reported by R. Farrell et al.,[122] the modal gain versus current density for 405 nm VCSELs (7λ cavity length) was calculated for various numbers of QWs, as shown in Figure 27(b). The modal gain was plotted using the three-parameter fit model, as described by

$$\Gamma g(J) \approx N_{qw} \Gamma_1 g_0 \ln\left(\frac{J + J_s}{N_w J_{tr_1} + J_s}\right) \tag{17}$$

where N_w is the number of QWs, Γ_1 is the average confinement factor per well, Γ is the total confinement factor, g_0 is the empirical gain coefficient,[122] J_{tr_1} is the transparency current density per well,[122] and J_s is a linearity parameter.[122] VCSELs designs with more QWs have a higher transparency current density (i.e., current density at a modal gain of 0 cm^{-1}) but the slope of the modal gain curve is also greater. Figure 27(b) shows a breakdown of sources of loss in VCSEL designs and shows that the TJ VCSEL has a much lower total loss, Γg_{th}, than the ITO VCSEL, which is notably due to the lower internal loss, α_i, of the TJ compared to ITO. With the goal of minimizing the threshold current density, Figure 27(b) shows that a 7×MQW is ideal for the TJ VCSEL (i.e., the 7QW green curve intersects Γg_{th} at the lowest current density) and a 10×MQW is ideal for the ITO VCSEL (i.e., the 10QW black curve intersects Γg_{th} at the lowest current density). To experimentally compare the two designs, ITO and TJ VCSELs were fabricated, each with a 7×MQW active region. The pulsed *L-I-V*

characteristics of the 12 μm aperture diameter ITO and TJ VCSELs are shown in Figure 27(c). Compared to the ITO VCSEL with a threshold current of 9 mA (8 kA/cm^2), the TJ VCSEL had a lower threshold current of 4 mA (3.5 kA/cm^2). The ITO VCSEL had a differential efficiency of 0.062% and reached a peak output power of 80 μW while the TJ VCSEL had a differential efficiency of 0.262% and achieved 550 μW. The lower threshold, higher differential efficiency, and higher peak output power of the TJ VCSEL was attributed to the significantly lower internal loss. As shown in the inset of Figure 27(c), filamentary lasing was observed in both ITO and TJ VCSELs, which may be related to variations in contact resistance or non-uniform current spreading.[58]

Nonpolar *m*-plane VCSEL designs have improved significantly over the years at UCSB, but none of the designs were able to lase under CW operation, which severely limits their use in practical applications. The primary goal of the work described in this thesis has been to improve the VCSEL design to achieve stable CW operation of *m*-plane GaN VCSELs. The VCSEL growth and fabrication process is outlined in Section 2 and optimization of various aspects in the VCSEL design are described in Section 3. Lastly, the key experiments and design improvements leading to CW operation are discussed in Section 4.

2. Fabrication of *m*-plane GaN VCSELs

This section outlines the growth and fabrication methods to create *m*-plane GaN-based dual-dielectric VCSELs. Each of the photographs shown in this section were taken during the fabrication of the VCSELs that are described in Section 4. Before going into the details for each of the processing steps, a general overview of the fabrication process is first described.

Unlike VCSEL designs that use an epitaxial DBR on the bottom side, the dual-dielectric DBR design has a relatively complicated fabrication process because DBRs need to be deposited on the top and bottom of the device with a precise cavity length in between. In the design described here, this is accomplished by depositing the p-side DBR, flip-chip bonding to a submount, and removing the growth substrate to deposit the n-side DBR. There are several other processing steps to define the current aperture, intracavity contact for current spreading on the p-side, metallization, and many others. Figure 28 shows images of the samples during various phases of the VCSEL fabrication process.

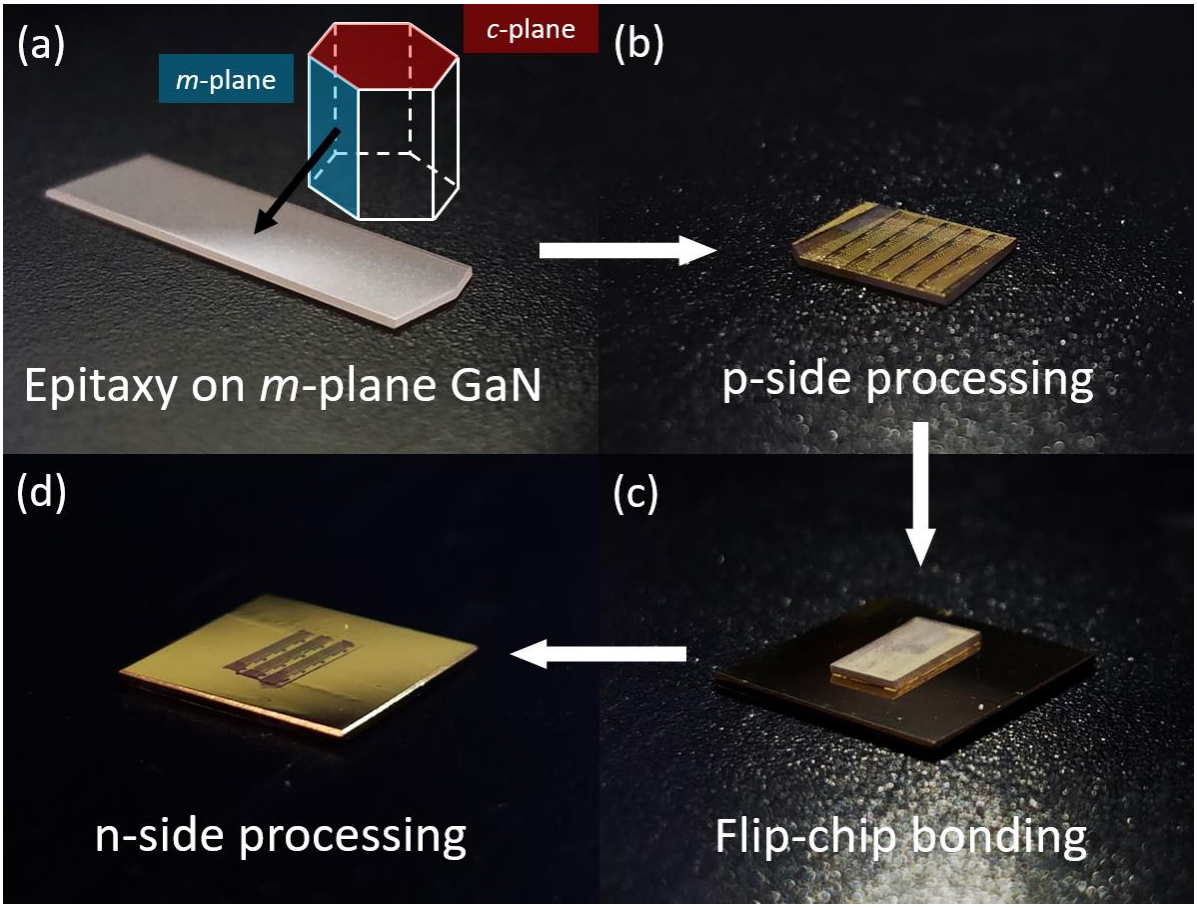


Figure 28. Photographs of the sample during various stages of the fabrication process for *m*-plane GaN dual-dielectric DBR flip-chip VCSELs. (a) MOCVD growth on freestanding *m*-plane GaN substrates with a 1° intentional miscut in the negative *c*-direction. (b) p-side processing including steps such as dry etching, ion implantation, MBE TJ regrowth, SiN_x deposition, p-DBR deposition, and metal deposition. (c) Flip-chip bonding to a metal-coated submount, such as copper or sapphire. (d) After PEC undercut etching to remove the GaN growth substrate, n-side processing includes steps such as metal deposition and n-DBR deposition.

As shown in Figure 28(a), the first step is MOCVD growth on freestanding *m*-plane GaN substrates to grow layers such as the sacrificial MQW, n-GaN, the active MQW, and p-GaN. Then, there are a series of processing steps on the p-side (e.g., dry etching, ion implantation, MBE regrowth, p-DBR deposition, metallization, etc.), as shown in Figure 28(b). With the p-side metal as the top surface, the sample is then flip-chip bonded face-down onto a metal-coated submount, as shown in Figure 28(c). To access the n-side of the device, the GaN growth substrate is removed by using PEC undercut etching to selectively etch a sacrificial MQW. Lastly, Figure 28(d) shows the final n-side processing steps, such as n-contact deposition and

n-DBR deposition. There have been several different current aperture designs (e.g., dielectric, PEC air-gap, and ion implantation apertures) and intracavity contact designs for current spreading on the p-side (e.g., ITO or TJ MBE regrowth) reported for *m*-plane GaN VCSELs. Here, we describe the fabrication process for the design that uses ion implantation for current confinement and a TJ intracavity contact grown by MBE.

For each of the stages shown in Figure 28, Figure 29 shows the corresponding schematic illustration of the structure.

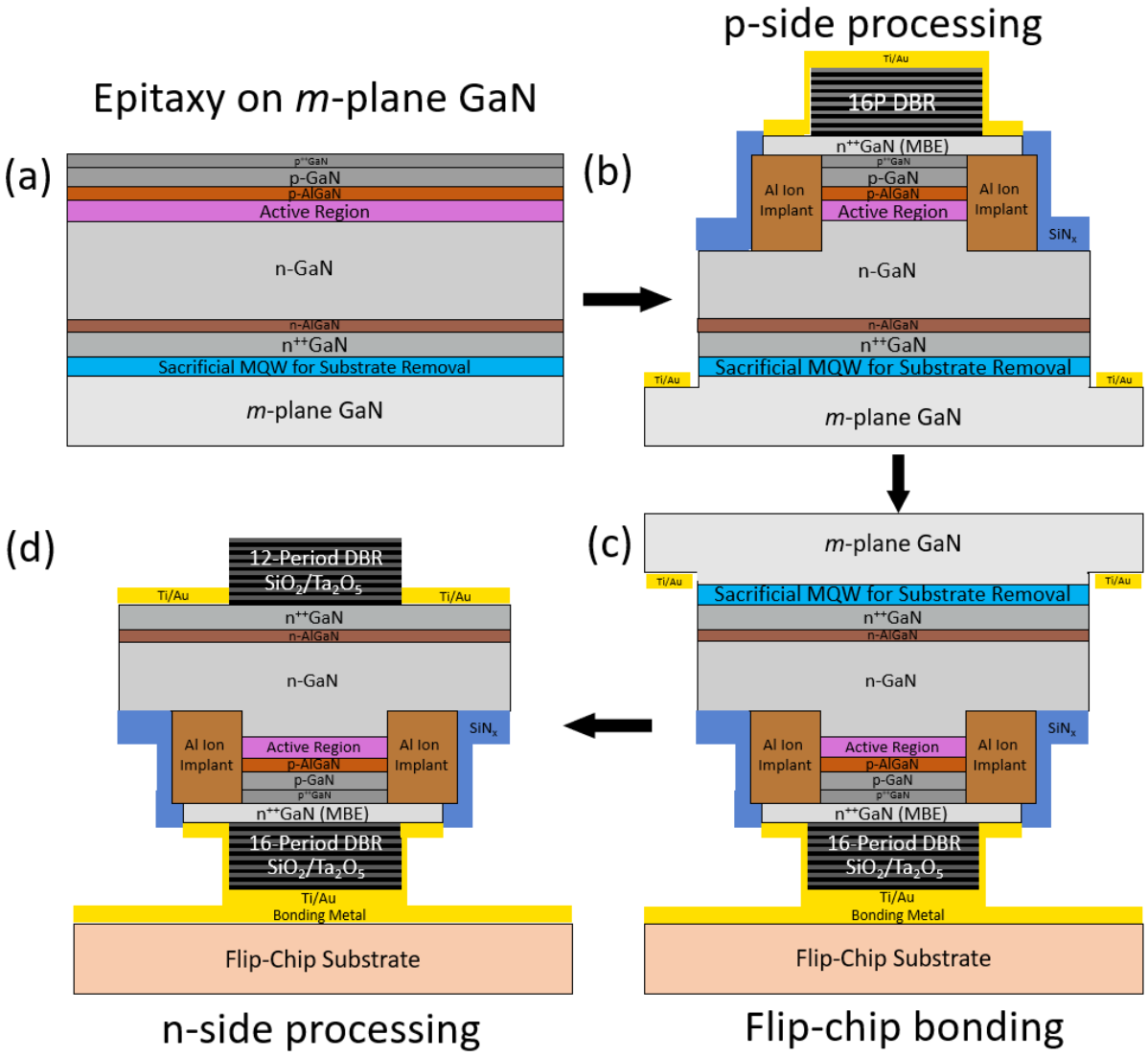


Figure 29. Schematic illustrations during various stages of the fabrication process for *m*-plane GaN dual-dielectric DBR flip-chip VCSELs. (a) MOCVD growth on freestanding *m*-plane GaN substrates with a 1°

intentional miscut in the negative *c*-direction. (b) p-side processing including steps such as dry etching, ion implantation, MBE TJ regrowth, SiN_x deposition, p-DBR deposition, and metal deposition. (c) Flip-chip bonding to a metal-coated submount, such as copper or sapphire. (d) After PEC undercut etching to remove the GaN growth substrate, n-side processing includes steps such as metal deposition and n-DBR deposition.

Before growing the epitaxial structure shown in Figure 29(a), a series of MOCVD growths are performed for each of those layers to measure the growth rate using X-ray diffraction (XRD). For example, the growth rate for n-GaN can be found by performing MOCVD on an *m*-plane GaN substrate to grow an n-GaN template, 15 nm AlGaN, and a 100 nm n-GaN layer. Using XRD to perform a 2-theta/omega scan, it shows interference fringes with a spacing that is inversely proportional to the layer thickness. Using the layer thickness from XRD and deposition time, the MOCVD growth rate can be obtained. The 15 nm AlGaN layer is used to create interference fringes (due to the phase difference between x-rays reflected from different materials) and is similarly used for XRD calibrations of n^{++}GaN, p-GaN, and p^{++}GaN layers. While the n-AlGaN and p-AlGaN layers are relatively thin in the VCSEL structure (15 nm and 5 nm, respectively), the layers are grown with a thickness ~70 nm in order to have a stronger XRD signal to measure the growth rate. Lastly, the growth rate for the active region is determined by growing a 12×MQW using the QW and barrier thicknesses used in the VCSEL design. Although the actual design typically has fewer QWs, increasing the number of periods increases the XRD signal and makes it easier to determine the thickness and growth rates. The final calibration step is to grow the epitaxial structure shown in Figure 29(a), activate the p-GaN (600 °C for 15 minutes), and perform electroluminescence (EL) measurements to check the quality of the growth and to make sure the emission wavelength is near the target wavelength ~405 nm. This is typically performed using the "quick-test" method in which indium is pressed through a shadow mask to create circular p-contacts on the top surface and n-contact is formed by soldering indium on the backside of the GaN

substrate. The emission wavelength is inversely proportional to the temperature during MOCVD growth of the active region (i.e., higher growth temperatures result in lower indium content in the MQW and shorter wavelength emission), so the growth recipe can be modified to obtain the target emission wavelength.

After calibrating the growth rates and MQW emission wavelength, MOCVD is performed for the actual VCSEL samples. As opposed to growing on half-wafer or quarter-wafers, it is helpful to perform MOCVD growth on full-size *m*-plane GaN substrates (5 mm × 15 mm) because low yield has been a longstanding problem during the VCSEL process, as further discussed in Section 4.4.6. After MOCVD growth, the samples are placed into a furnace for p-GaN activation at 600 °C for 15 minutes. To check the quality of the MOCVD growth, indium contacts are soldered to measure the EL characteristics. At a current of 20 mA and wavelength ~405 nm, the voltage should be ~5 V and the output power should be ~ 3 mW. If the voltage is much higher or power is much lower, MOCVD growth is reperformed to create new samples. While the FWHM of the emission spectrum is typically ~14 nm for samples with a single MQW, the FWHM can seem larger for the VCSEL epitaxial growth because the sacrificial MQW is designed to emit at a longer wavelength (~420 nm) compared to the active MQW (~405 nm). Then, the samples are submerged in boiling aqua regia (3:1 HCl:HNO_3) for a total of 30 minutes to remove the soldered indium contacts. At this stage, the samples are ready for a series of photolithography processing steps in the clean room to create the structure shown in Figure 29(b).

The 1st photolithography step is to create a mesa using reactive ion etching (RIE) to etch past the active MQW but not past the sacrificial MQW, as shown in Figure 30(a).

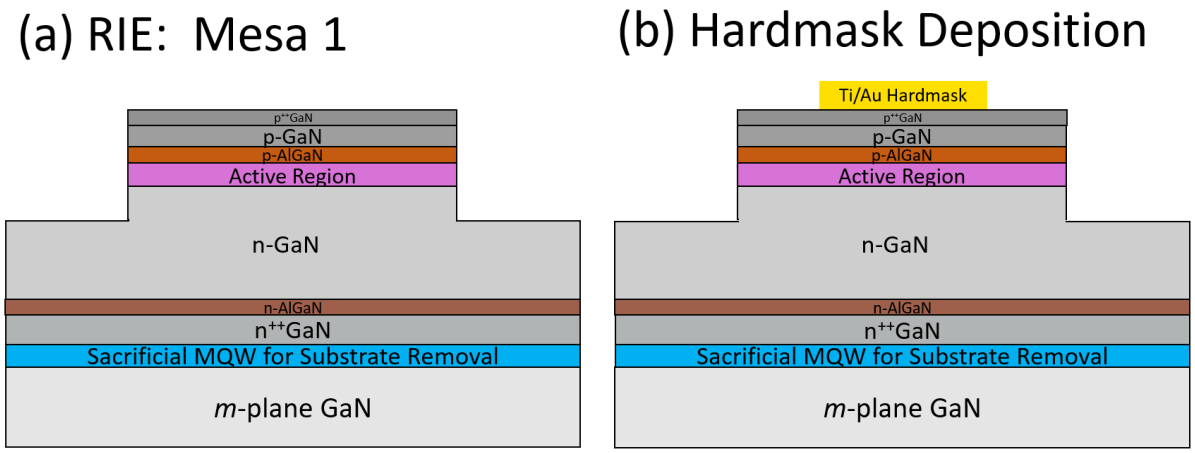


Figure 30. Schematic illustrations of the structure during VCSEL fabrication process. (a) RIE was used to etch past the active MQW by not past the sacrificial MQW. (b) A Ti/Au hardmask was deposited using electron beam evaporation in order to protect the aperture during ion implantation.

The mesas are protected with a positive photoresist during the RIE Cl_2 etch. The purpose of this etch is to expose the sidewall of the active MQW so that it can be protected with a layer of SiN_x in a later step, which protects the active MQW during PEC etching of the sacrificial MQW during growth substrate removal. If the dry etch shown in Figure 30(a) etched past the sacrificial MQW, the sacrificial MQW sidewall would later become protected with SiN_x, which could prevent growth substrate removal. Using an RIE etch rate of ~120 nm/min, the target etch depth is typically chosen so the etch terminates at the midpoint between the active MQW and sacrificial MQW, which falls within the n-GaN layer. As discussed later in this section, there could be a problem for deep dry etches that terminate near the sacrificial MQW because ion implantation could passivate the sacrificial MQW and prevent etching. This could be solved by removing this dry etch step and the SiN_x deposition step from the VCSEL process (i.e., relying on ion implantation to protect the active MQW during PEC etching instead of SiN_x).

In order to protect the p-side material within the circular aperture during ion implantation, the 2nd photolithography step is to deposit circular Ti/Au (20 nm/200 nm)

hardmasks using electron beam evaporation, as shown in Figure 30(b). The samples are then shipped to Leonard Kroko, Inc. to perform Al ion implantation at a normal incidence angle using a dose of 10^{15} ions/cm^2 and energy of 20 keV, as illustrated in Figure 31(a).

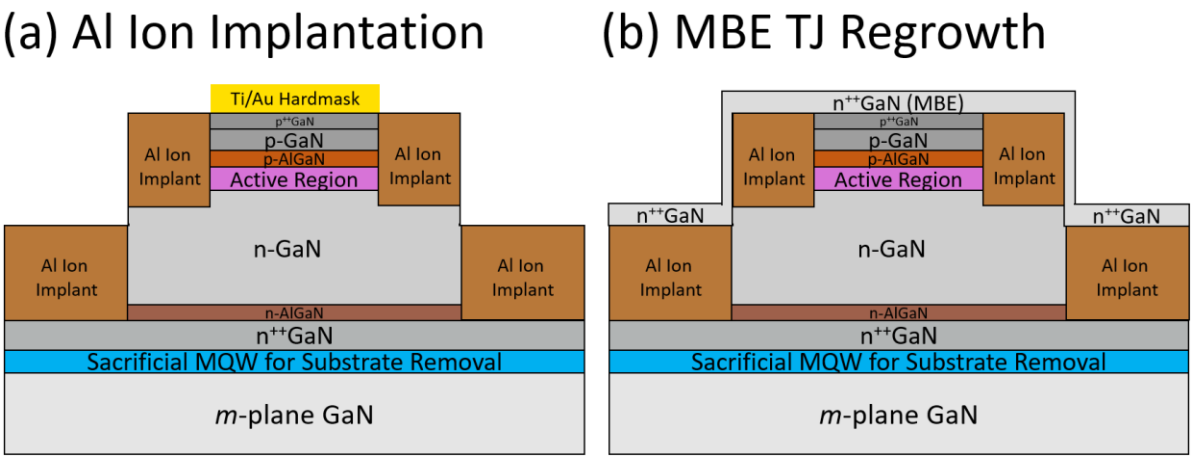


Figure 31. Schematic illustrations of the structure during VCSEL fabrication process. (a) Al ion implantation creates the circular current aperture as the circular Ti/Au hardmask protects the aperture during implantation. (b) MBE is used to grow the TJ intracavity contact and current spreading layer on the p-side of the device.

This creates the VCSEL current aperture as Al ion implantation electrically passivates the p-side material everywhere except for the circular apertures that were protected by the Ti/Au hardmasks. Recently, it was discovered that ion implantation also passivates the active MQW outside the aperture, which protects the active region during PEC etching for growth substrate removal. Ion implantation was actually found to be more effective at protecting the active region during PEC etching compared to SiN_x. This is useful, but it could pose a problem if the sacrificial MQW becomes passivated by ion implantation which would prevent PEC etching. Therefore, the initial mesa etch should not be too deep and the ion implantation energy should not be too high so ion implantation does not penetrate through the sacrificial MQW. Although this has not been a problem for 7λ, 13λ, and 23λ VCSELs, it could become an issue for shorter cavity designs that have thinner n-GaN layers. Note that Figure 31(a) is not drawn to scale, so

ion implantation in the dry-etched region (i.e., between mesas) should terminate well within the n-GaN layer. The next step is to grow the TJ intracavity contact and current spreading layer by MBE, as illustrated in Figure 31(b). In a collaboration with S. Lee, we have demonstrated that MOCVD can also be used to create TJ VCSELs.[117] As discussed in Section 4.5, the *m*-plane GaN VCSELs that achieved CW operation used MBE for the TJ regrowth, which consisted of n^{++}GaN/n-GaN/n^{++}GaN (39.6/61.7/39.6 nm) with respective Si concentrations of 1.1×10^{20}, 2.5×10^{18}, and 1×10^{19} cm^{-3}. As discussed in Section 4.4.3, surface roughness can be a critical issue for VCSELs, so it is important to measure the roughness using AFM after TJ regrowth.

The 3rd photolithography step consists of a dry etch and a self-aligned SiN_x deposition, as shown in Figure 32.

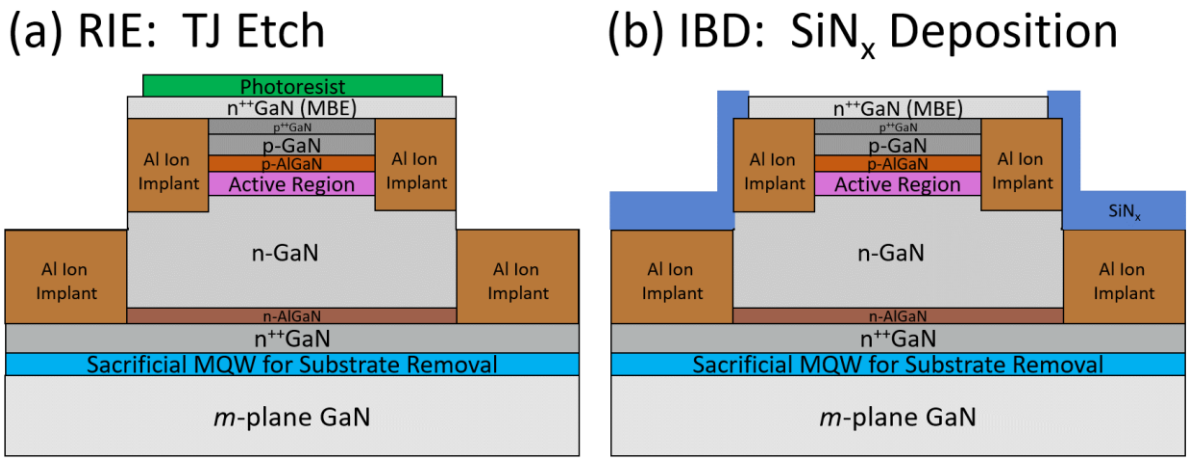


Figure 32. Schematic illustration of the structure after the 3th photolithography step of the VCSEL fabrication process. (a) RIE was used to etch the regrown material on the mesa sidewall and in the field between mesas. (b) Using the same photoresist that was used for the previous etch, SiN_x was deposited with the goal of protecting the active MQW sidewall during PEC etching in a later step. Note that this step is no longer necessary in the VCSEL process if ion implantation successfully protects the active MQW.

As illustrated in Figure 31(a), a current leakage path could be created if there is n^{++}GaN growth along the sidewall of the mesa, so a dry etch is performed to remove that material, as shown in Figure 32(a). The dry etch is typically performed to etch through the MBE regrown

thickness and through the 14-nm p^{++}GaN layer. Using the same photoresist shown in Figure 32(a) that was used during the TJ etch, IBD is used to deposit a ~250 nm layer of SiN_x, as shown in Figure 32(b), with the goal of protecting the sidewall of the active MQW so that it does not etch during PEC etching at a later stage. However, based on results from VCSELs fabricated in Section 4.3, the SiN_x layer has not successfully protected the active region, and the active MQW has etched laterally during PEC etching for VCSELs that did not have ion implanted apertures. This also showed that ion implantation was very effective at protecting the active MQW during PEC etching. Therefore, the SiN_x deposition step can be eliminated from the fabrication process in future VCSEL designs that use ion implantation, and this has already been demonstrated in the MOCVD TJ VCSEL design.[117]

The 4th photolithography step is to deposit the p-side 16-period SiO_2/Ta_2O_5 dielectric DBR using IBD, as shown in Figure 33(a).

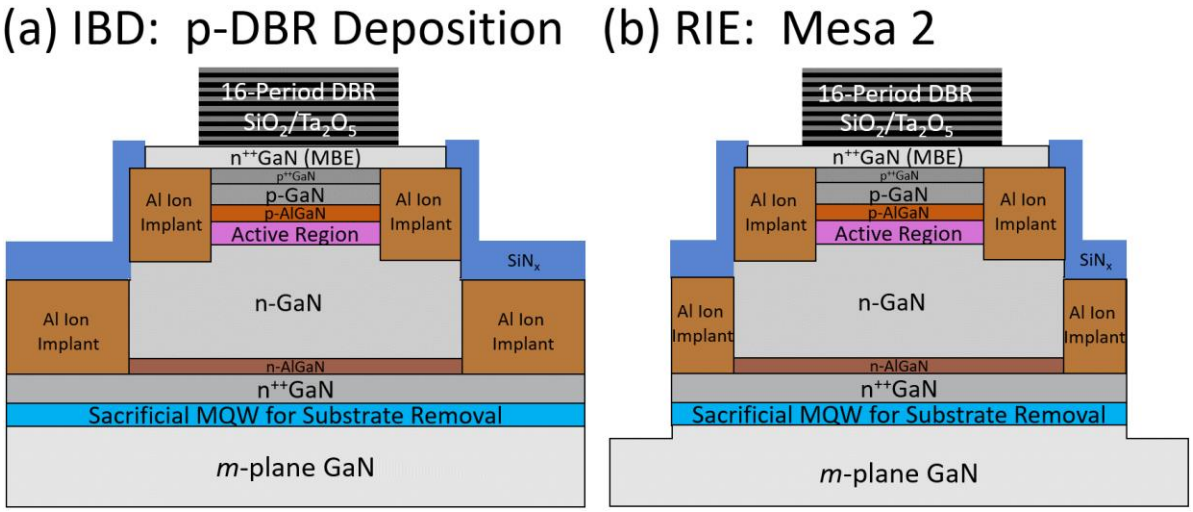


Figure 33. Schematic illustrations of the structure after the 4th and 5th photolithography steps of the VCSEL fabrication process. (a) IBD was used to deposit the 16-period Ta_2O_5/SiO_2 p-side DBR. (b) RIE was used to etch a relatively deep mesa to expose the sidewall of the sacrificial MQW so that it can be etched via PEC etching during growth substrate removal at a later stage of the VCSEL process.

The p-side 16-period DBR consists of quarter-wavelength-thick alternating layers of SiO_2 and Ta_2O_5, with respective thicknesses of ~67.1 nm and ~45.6 nm (assuming n_{SiO_2}~1.51 and

$n_{Ta_2O_5}$~2.22 at $\lambda = 405$ nm). Prior to DBR deposition, single layers of SiO_2 and Ta_2O_5 are deposited onto Si wafers to measure their thicknesses (to calculate the IBD deposition rates) and their refractive indices, which are used to calculate the quarter-wavelength thickness, as described by Equation (22). Then, a series of SiO_2/Ta_2O_5-based Fabry-Perot cavities are deposited on silicon and/or a sapphire wafers, and the Cary 500 spectrophotometer is used to measure the reflectance spectrum. The Fabry-Perot cavities have a half-wavelength-thick cavity length to produce destructive interference at the target wavelength, so the minimum point of the reflectance spectrum curve gives information about the optical thickness of the SiO_2/Ta_2O_5 layers. This is used to further calibrate the IBD prior to DBR deposition, and more details about this calibration process are described in Section 4.4.2.

The 5th photolithography step is to use RIE to etch a relatively deep mesa to expose the sidewall of the sacrificial MQW, as shown in Figure 33(b). Exposing the sidewall of the sacrificial MQW is necessary so that it can etch via PEC etching during growth substrate removal in a later stage of the VCSEL process. Note that SiN_x etches at a much slower rate than GaN, so there is a risk of underestimating the RIE etch time to etch past the sacrificial MQW. This has happened during VCSEL processing for some samples, but it was found that VCSEL fabrication is still possible, as discussed later in this section. This problem was prevented during the fabrication of recent VCSELs by calculating the *Mesa 2* RIE etch time using the following equation

$$t_{M2\ Etch} = \frac{T_{MOCVD} + T_{MBE}}{R_{GaN}} - t_{M1\ Etch} - t_{TJ\ Etch} + \frac{T_{SiN_x}}{R_{SiN_x}} + t_{extra} \tag{18}$$

where $t_{M2\ Etch}$ is the RIE etch time in minutes for the *Mesa 2* etch, T_{MOCVD} is the thickness of the MOCVD-grown layers (not counting the initial n-GaN template), T_{MBE} is the thickness of the MBE-grown layers, R_{GaN} is the RIE etch rate for GaN (~120 nm/min), $t_{M1\ Etch}$ is the RIE

etch time used for the *Mesa 1* etch, $t_{TJ\ Etch}$ is the RIE etch time used for the TJ etch, T_{SiN_x} is the thickness of the deposited SiN_x (~250 nm), R_{SiN_x} is the RIE etch rate for SiN_x (estimated to be ~25 nm/min), and t_{extra} is an additional time buffer (~5 minutes) that is added to help ensure that the etch is deep enough to etch past the sacrificial MQW. As long as the photoresist (~7 μm thick) protecting the mesa does not completely etch, there would probably not be an issue for choosing even longer RIE etch times to make sure the etch is deep enough. Though the RIE etch rate for GaN is typically ~120 nm/min, confocal microscope measurements showed etch rates ranging from 111 nm/min to 120 nm/min. A direct measurement of the SiN_x RIE etch rate has not been measured here, but based on the measured step height after the *Mesa 2* etch and assuming a GaN etch rate of 117 nm/min, the SiN_x etch rate is estimated to be ~25 nm/min. Note that the positive photoresist used for this step (SPR 220-7.0) is relatively viscous and often leads to thick edge bead (i.e., thicker photoresist near the edge of the wafer). This effect can be minimized by placing the long edges of the GaN sample in between the edges of two sapphire wafers during spin coating of the photoresist. It helps to fully cover the GaN sample with photoresist as well as the edges of the sapphire corrals prior to spinning.

The 6th photolithography step is to deposit the intracavity contact metal (p-electrode) and to deposit metal in the field between devices to serve as a PEC cathode, as shown in Figure 34(a).

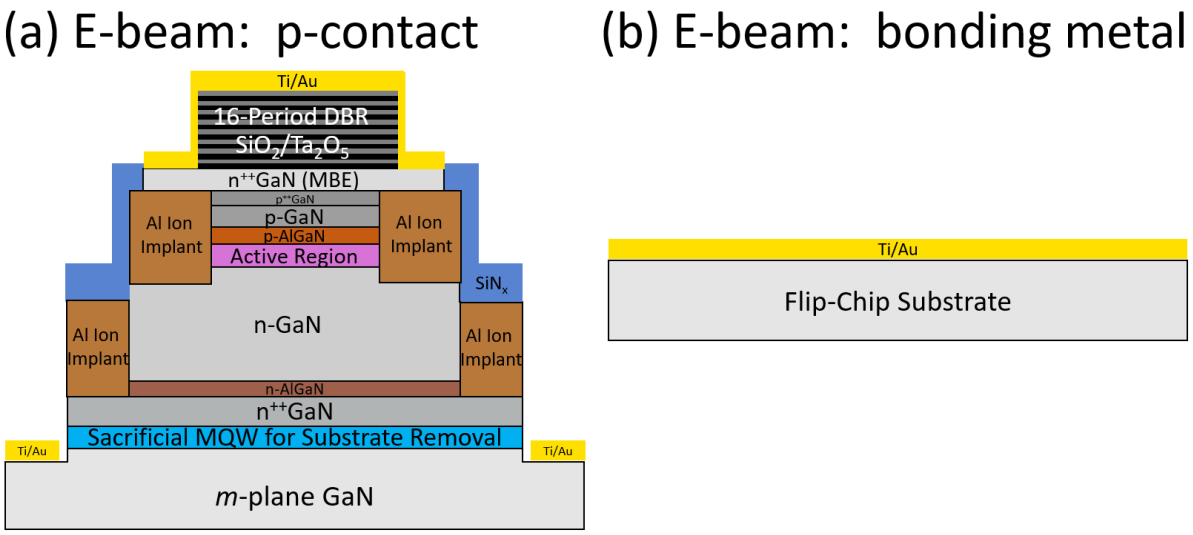


Figure 34. Schematic illustration of the devices after the 6th photolithography step of the VCSEL fabrication process. (a) Electron beam evaporation (or magnetron sputtering) is used to deposit Ti/Au (20/1000 nm) to conformally coat the sidewall of the p-side DBR to serve as p-contact. Metal is also deposited in the field between devices to serve as the PEC cathode during PEC etching. (b) Electron beam evaporation is used to deposit Ti/Au or another metal stack onto a flip-chip substrate. While Ti/Au has been used to coat the flip-chip substrate for previous VCSELs that used Au-Au thermocompression bonding, a major improvement in recent VCSELs has been to deposit Ti/Ni/Au/In/Au (20/100/100/2100/350 nm) to perform Au-In solid-liquid interdiffusion bonding.

Ti/Au is deposited on the MBE regrown n^{++}GaN contact layer for p-side contact and the metal on top of the DBR is the contact metal during flip-chip bonding. An angled rotating electron evaporation fixture is used for deposition because metal needs to conformally coat the sidewalls of the DBR so that current can be injected into the VCSEL by probing the metal on the flip-chip substrate. As discussed further in Section 4.4, this Ti/Au layer on the sidewall of the p-DBR is the main metal pathway for heat transport during VCSEL operation. Increasing the thickness of this metal layer would improve the thermal performance, but the thickness has usually been limited by the maximum deposition thickness of ~1 μm for the electron beam evaporation tool. As discussed in Section 4.5, one of the most significant thermal improvements that led to CW lasing was creating a thicker pathway for heat transport using Au-In solid-liquid interdiffusion (SLID) bonding to embed the p-DBR within metal. This section describes the original flip-chip design using Au-Au thermocompression bonding, and more details about the recent VCSEL design using Au-In SLID bonding are discussed in

Section 4.4.6.2. In the original Au-Au flip-chip bonding design, the next step is to deposit Ti/Au (10/500 nm) onto flip-chip substrates (e.g., sapphire, copper, SiC, etc.), as illustrated in Figure 34(b). For copper substrates, it can be useful to deposit Ti/Ni/Au (~10/100/500 nm) because the nickel (Ni) layer can serve as a diffusion barrier during thermocompression bonding to avoid interdiffusion between Cu and Au. As further described in Section 4.4.6.1, it is important during thermocompression bonding for the flip-chip substrate to be completely flat, so polished copper substrates are preferred compared to unpolished copper blocks.

The next step in the original flip-chip design is to place the GaN sample face-down onto the metal-coated flip-chip substrate within a graphite compression mount, as shown in Figure 35(a).

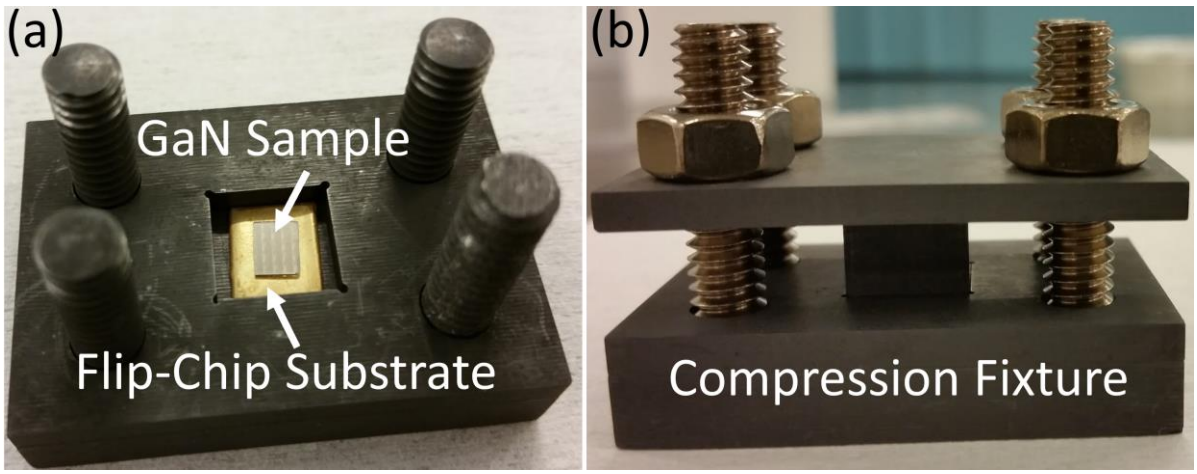


Figure 35. (a) GaN sample placed face-down onto the metal-coated flip-chip substrate placed within the bottom half of a graphite compression fixture. (b) Fully-assembled graphite compression fixture used for Au-Au thermocompression bonding in a furnace at 200 °C for 2 hours.

Figure 35(b) shows the fully-assembled graphite compression fixture to perform Au-Au thermocompression bonding in a furnace at 200 °C for two hours. This Au-Au bonding process has been used for previous *m*-plane GaN VCSELs, but it has resulted in low VCSEL yield, as described in Section 4.4.6.1. This has been improved for recent VCSELs by using the Finetech flip-chip bonder to perform thermocompression bonding. Based on Au-Au

bonding experiments described in Section 4.4.6.1, the optimum bonding conditions were at a temperature of 310 °C, bonding time of 280 seconds, and applied force of 300 N; however, the VCSEL yield was still very low even using those optimized bonding conditions. The most significant improvement in VCSEL yield was accomplished by replacing Au-Au thermocompression bonding with Au-In SLID bonding, as discussed in Section 4.4.6.2. Figure 36(a) shows a schematic illustration of the structure after flip-chip bonding.

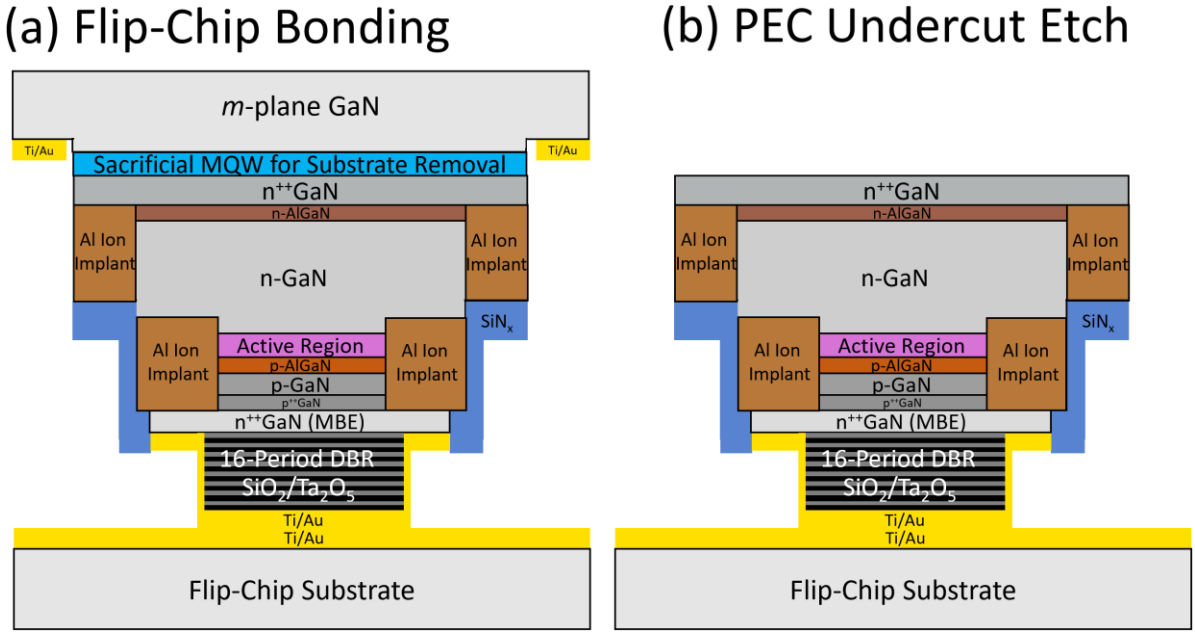


Figure 36. Schematic illustrations of the structure during the VCSEL fabrication process. (a) Au-Au thermocompression bonding to a flip-chip substrate. (b) PEC undercut etching of the sacrificial MQW to remove the *m*-plane GaN substrate.

After flip-chip bonding, the samples are ready for PEC undercut etching of the sacrificial MQW to remove the *m*-plane GaN growth substrate, as shown in Figure 36(b). The standard process has been to perform PEC etching in a solution of 1 M KOH solution using a 405 nm LED array illumination source to create electron-hole pairs within the sacrificial MQW ($\lambda \sim 420$ nm). Photogenerated holes diffuse toward the sidewall of the sacrificial MQW where they assist in the oxidation of Ga atoms,[123,124] and the undercut etch progresses as the resulting oxide dissolves in the KOH solution. Photogenerated electrons are eliminated by a

reduction reaction at the Ti/Au cathode on the *m*-plane GaN substrate. There are also photogenerated carriers within the active MQW, so the sidewall of the active region is protected with SiN_x to prevent it from etching. However, recent results showed that the active MQW can still etch during PEC etching even if the sidewall of the active MQW is coated with ~250 nm SiN_x deposited using IBD. Instead of SiN_x, the most effective method to protect the active MQW during PEC etching has been to use Al ion implantation. In addition to forming the current aperture, Al ion implantation passivates the active MQW outside the aperture and protects it during PEC etching.

If the *Mesa 2 Etch* was not deep enough (i.e., the sidewall of the sacrificial MQW is not exposed for each device), *m*-plane GaN substrate removal is still possible by PEC undercut etching through the entire sacrificial MQW layer. However, the PEC undercut etch takes much longer and it results in a thin GaN sheet that connects each device on the flip-chip substrate. The thin GaN sheet can be a problem during VCSEL testing because it provides a current path between devices, but the GaN sheet is typically very fragile and breaks during n-side VCSEL processing.

As discussed in Section 4.4.3, recent results showed that a rough oxide residue forms after PEC undercut etching. Removing the residue is important because it could contribute to scattering loss and reduced DBR mirror reflectivity. Most of the residue can be removed by submerging the samples in 11.7 M KOH for ~20 minutes, but the most effective method of residue removal has been to use a foam swab to gently wipe the samples in Tergitol detergent, which resulted in sub-nanometer RMS roughness. Although swabbing in Tergitol has been the best method to remove the residue, the downside is that it can reduce VCSEL yield as swabbing can damage devices. Devices with pre-existing cracks from flip-chip bonding are

especially prone to damage after swabbing. This has become less of a problem for recent VCSELs because switching from Au-Au thermocompression bonding to Au-In SLID bonding has significantly increased the number of crack-free devices after bonding, so swabbing in Tergitol has become less destructive.

The 7th photolithography step is to deposit the n-contact metal, as shown in Figure 37(a).

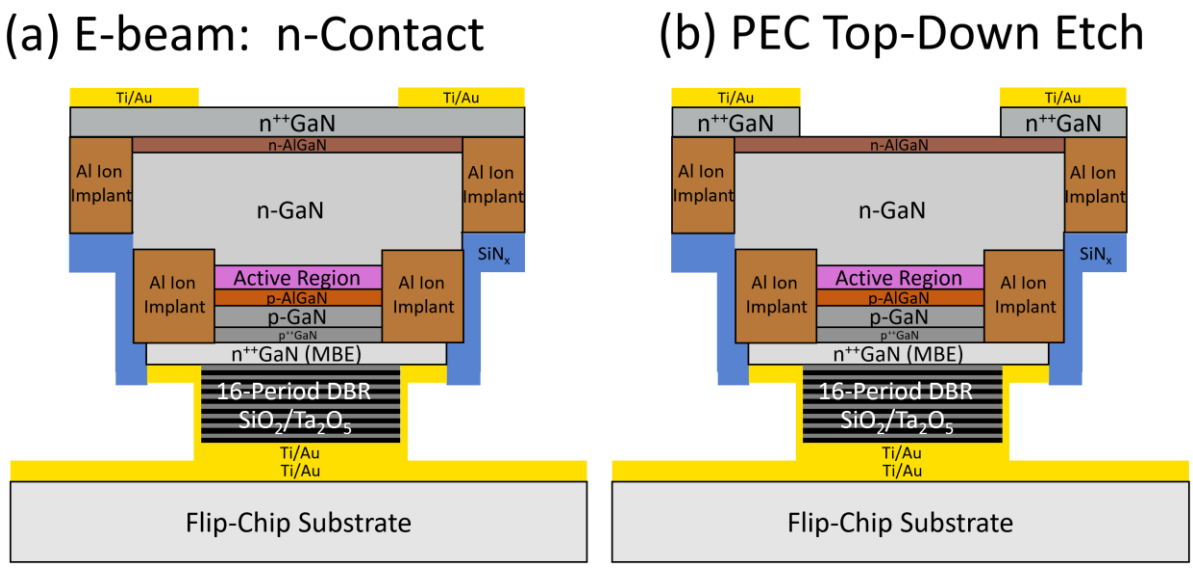


Figure 37. Schematic illustration of the structure after the 7th photolithography step of the VCSEL fabrication process. (a) Ti/Au n-contact deposition using electron beam evaporation or sputtering. (b) Optional step in the VCSEL process consisting of a PEC top-down etch (0.001M KOH solution and a Hg-Xe arc lamp with a 345 nm long-pass filter) to etch n^{++}GaN within the aperture down to the n-AlGaN stop-etch layer.

This step has been problematic during fabrication of recent VCSELs as the Ti/Au has been difficult to liftoff (i.e., despite having underlying photoresist for liftoff, Ti/Au frequently remains in the field between devices). While the standard process is to use a single negative photoresist (nLOF2020), this problem could probably be solved by using a liftoff layer (e.g., LOL 2000) prior to spinning the negative photoresist.

The next step in the VCSEL fabrication process is optional and consists of top-down PEC etching of the n^{++}GaN within the aperture down to the n-AlGaN stop-etch layer, as illustrated in Figure 37(b). This etch has typically been performed for 3 minutes in a solution of 0.001

M KOH using a Hg-Xe arc lamp illumination source with a 345 nm long-pass filter to prevent n-AlGaN from etching. However, there have been problems with the PEC top-down etch for recently fabricated VCSELs. The n^{++}GaN was unable to etch for those devices because the Si doping was too high. It was found that n^{++}GaN with Si doping concentrations of $> 1 \times 10^{19}$ cm^{-3} were unable to etch during PEC top-down etching due to the short photoexcited carrier lifetime and shallow band bending at the surface.[125] Despite this problem, the PEC top-down etch is not necessary in the VCSEL process. The purpose of the PEC top-down etch has been to remove n^{++}GaN in the aperture down to the n-AlGaN stop-etch layer in order to provide precise cavity length control, but epitaxially-defined cavity length control is already provided by the PEC undercut etch of the sacrificial MQW. Another purpose of the PEC top-down etch has been to create a smooth n-side surface, but recent results showed that a smooth surface can be achieved directly after PEC undercut etching by removing the oxide residue. Therefore, recent VCSELs have been fabricated without the PEC top-down etch, and the n^{++}GaN thickness has been reduced from 50 nm to ~26 nm to reduce optical absorption. The PEC top-down etch could be useful in future VCSEL designs because removing n^{++}GaN in the aperture can reduce optical absorption, but this could also be accomplished by depositing a Ta_2O_5 spacer layer prior to the n-DBR so that the null of the optical standing mode is aligned with the n^{++}GaN layer.

Before depositing the top-side DBR, the electroluminescence (EL) spectrum is collected to view the resonance wavelengths within the cavity. Even without the top n-DBR, an optical cavity is formed between the bottom-side p-DBR and the GaN/air interface on the top, but lasing will not occur because the topside reflectance is much lower than the required reflectance of ~99.9%. Instead, there are peaks and nulls in the spontaneous emission

spectrum due to resonance wavelength(s) within the optical cavity, and this provides an estimate of the optical cavity thickness as it is inversely proportional to the resonance wavelength spacing. It is important that the resonance wavelength(s) aligns with the peak gain wavelength and falls within the DBR reflectance stopband. If the resonance wavelength is misaligned, a Ta_2O_5 spacer can be deposited prior to the n-DBR to adjust the resonance wavelength for better alignment. More details about this process are described in Section 4.3.2.

The 8th and final photolithography step is to deposit the n-side 12-period SiO_2/Ta_2O_5 dielectric DBR using IBD, as illustrated in Figure 38.

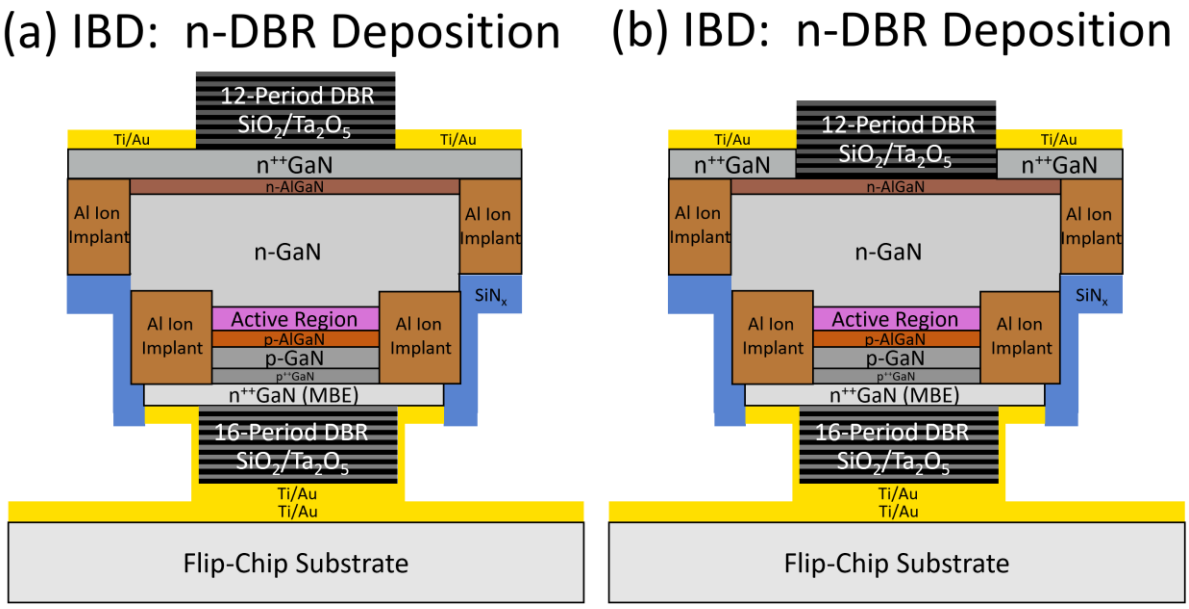


Figure 38. Schematic illustration of the completed VCSEL structure for a device that (a) was fabricated without the PEC top-down etch and (b) was fabricated with the PEC top-down etch to remove $n^{++}GaN$ within the aperture.

Figure 38(a) shows a VCSEL that was fabricated without the PEC top-down etch, and Figure 38(b) shows a device that included the PEC top-down etch. Similar to the previously deposited p-DBR, depositing the n-DBR requires precisely calibrating the IBD to deposit the correct

optical thicknesses. After DBR deposition and liftoff, the VCSELs are ready for electrooptical characterization.

3. Optimizing *m*-plane GaN VCSEL Design

This section delves into the details of *m*-plane GaN-based VCSEL design and outlines the improvements that have been made over the years. For more details about past improvements, see C. Holder's thesis in Ref. 126 and J. Leonard's thesis in Ref. 127. Section 3.1 discusses epitaxial growth on nonpolar *m*-plane GaN and outlines the epitaxial design improvements that have been made over the years for *m*-plane GaN-based VCSELs. In addition to epitaxial improvements, there have also been several processing and structural improvements. Section 3.2 describes progress in flip-chip Au-Au thermocompression bonding and Section 3.3 discusses developments in PEC etching. Current aperture and intracavity contact design are discussed in Section 3.4 and Section 3.5, respectively. Lastly, Section 3.6 describes the main challenge in which previous *m*-plane GaN-based VCSELs have not been able to lase under CW operation. Solving this problem has been the main goal of the research described in this thesis, and Section 4 discusses the experiments and developments that led to the first demonstration of CW operation for *m*-plane GaN-based VCSELs.

3.1. Epitaxy on *m*-plane GaN

There have been many challenges with epitaxial growth on *m*-plane GaN. VCSELs require very smooth surfaces with subnanometer RMS roughness, but epitaxy on *m*-plane GaN tends to form irregular growth morphologies that depend on the miscut angle and indium content. For on-axis *m*-plane GaN substrates (i.e., no miscut angle), MOCVD growth produces undesirable morphological features that are generally referred to as pyramidal

hillocks.[128] Pyramidal hillocks were found to be caused by spiral dislocation propagation near a screw component threading dislocation.[129] These features can be suppressed by performing MOCVD growth on *m*-plane GaN substrates that have an intentional miscut angle. While several miscut angles have been investigated,[128–133] a 1° miscut in the negative *c*-direction $[000\bar{1}]$ (i.e., a -1° miscut) has produced some of the best growth morphologies for violet-emitting devices with RMS roughness typically < 1 nm.

These substrates have been used in each of the violet-emitting *m*-plane GaN VCSEL designs from UCSB; however, there are some problems with this miscut. While *m*-plane GaN substrates with a -1° *c*-miscut are ideal for MOCVD-grown violet-emitting devices, this orientation is less suitable for longer wavelength blue- or green-emitting devices due to problems such as low indium uptake (requiring lower growth temperatures that leads to poor crystal quality and defects) and spectral broadening at higher indium compositions.[128] An alternative orientation is *m*-plane with a double miscut (i.e., miscut along both the *a*- and *c*-direction), which has shown higher indium uptake and narrower spectral emission in the blue spectrum.[133] Another problem with -1° *c*-miscut *m*-plane GaN is that while it is ideal for MOCVD growth, MBE growth on this orientation can lead to a rough morphology. As further discussed in Section 4.4.3 and 4.4.4, this was an important factor that prevented VCSELs from lasing due to the rough surfaces from MBE TJ regrowth.

3.1.1. Epitaxial Structure and Doping

The general epitaxial structure for *m*-plane GaN 7λ VCSELs with TJ intracavity contacts is illustrated in Figure 39.

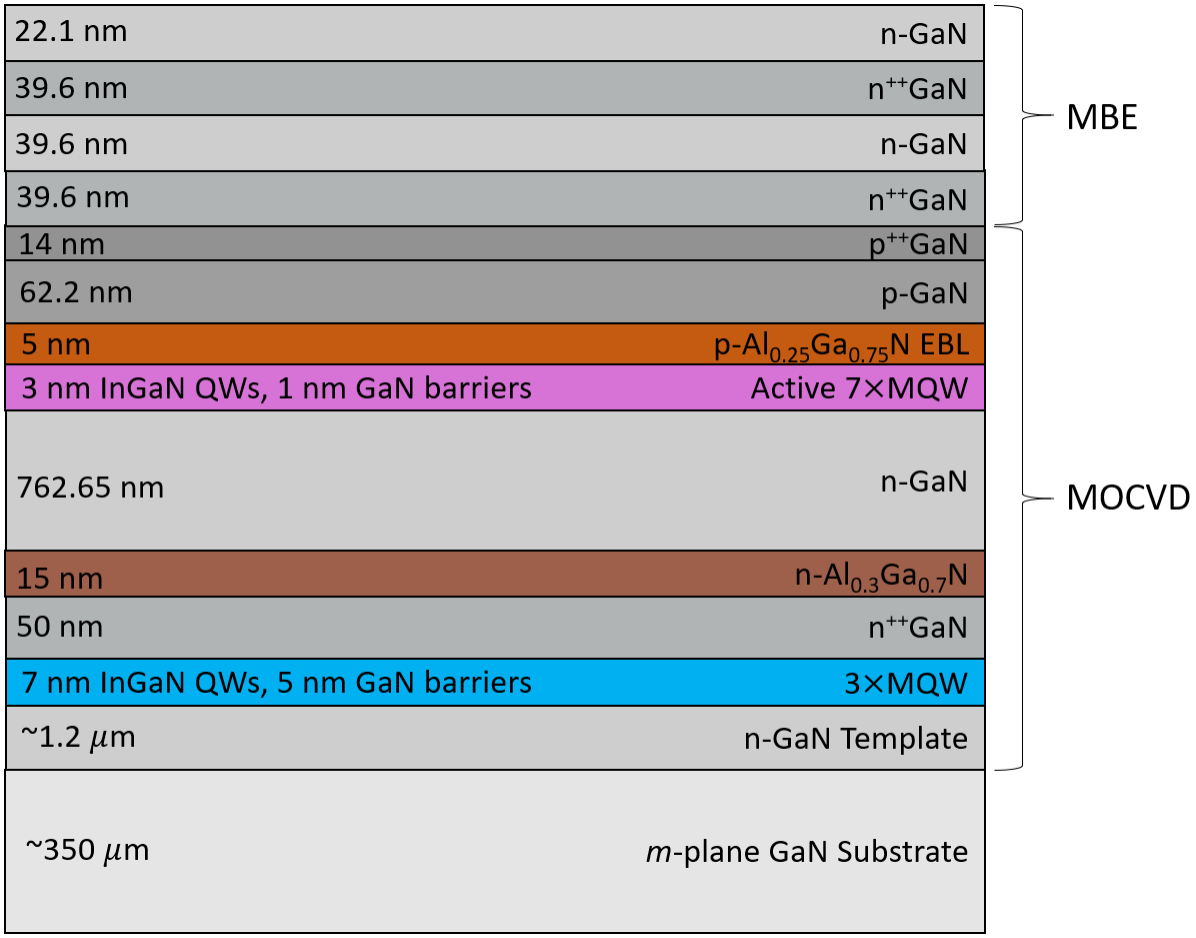


Figure 39. Illustration of the epitaxial structure for an *m*-plane GaN 7λ VCSEL with a TJ intracavity contact. The MOCVD- and MBE-grown layer thicknesses correspond to the initial nonpolar GaN TJ VCSEL design.[58,127]

The -1° *c*-miscut *m*-plane GaN substrates are from Mitsubishi Chemical Corporation (MCC) and are n-type with a Si concentration of ~2×10^{17} cm^{-3}. Using a modified two-flow reactor, MOCVD growth was performed at atmospheric pressure with typical V/III ratios (i.e., >3000) and growth temperatures ranging between 800 °C and 1200 °C. During growth, nitrogen was used as the precursor for ammonia (NH_3) and trimethylgallium (TMG) was used as the Ga precursor for thick n-GaN layers due to its relatively high growth rate ~50 nm/min. With a slower growth rate of ~5 nm/min, triethylgallium (TEG) was used as the Ga precursor for the InGaN/GaN MQW due to its lower impurity incorporation, and TEG was also used for highly-doped layers (i.e., n^{++}GaN and p^{++}GaN) because higher doping concentrations could

be achieved compared to using TMG. Bis(cyclopentadienyl)magnesium (Cp_2Mg) and silane (SiH_4) were used as the Mg (p-type) and Si (n-type) dopant precursors, respectively. Grown using TEG as the Ga precursor, trimethylindium (TMI) was used as the In precursor for InGaN layers, and trimethylaluminum (TMA) was used as the Al precursor for AlGaN layers. Hydrogen (H_2) carrier gas was used for p-GaN growth while all other layers were grown with nitrogen (N_2) carrier gas.

As shown in Figure 39, the general MOCVD-grown structure consists of a ~1.2 μm n-GaN template, sacrificial 3×MQW (7 nm QWs and 5 nm barriers), 50 nm n^{++}GaN, 15 nm n-AlGaN, 762.65 nm n-GaN, active region 7×MQW (3 nm QWs and 1 nm barriers), 5 nm p-AlGaN EBL, 62.2 nm p-GaN, and 14 nm p^{++}GaN. These layer thicknesses correspond to the 7λ TJ VCSEL structure reported in Ref. 58, and the MBE TJ regrowth consisted of 39.6 nm n^{++}GaN, 39.6 n-GaN, 39.6 n^{++}GaN and 22.1 nm n-GaN. As described further in Ref. 127, SIMS was performed on previous VCSELs to measure the doping concentration for each layer.

Starting from the bottom, the ~1.2 μm n-GaN template consisted of a lower doped and higher doped region with Si concentrations of approximately 1×10^{18} cm^{-3} and 2×10^{18} cm^{-3}, respectively. This template has been transferred from older MOCVD growth recipes, but it could likely be simplified to a single doping concentration or reduced thickness to reduce the total growth time without affecting device performance as long as the growth morphology is smooth (i.e., < 1 nm RMS roughness). Since the initial demonstration of the nonpolar GaN VCSEL,[29] the sacrificial MQW structure has not been changed because it has worked effectively during PEC etching to remove the growth substrate. However, as discussed in Section 4.4, a rough residue can form after PEC etching which can cause significant scattering

loss for VCSELs. As discussed in the PEC etching experiments in Section 4.4.5, one way to prevent the residue from forming was to use a single QW instead of a MQW as the sacrificial layer for PEC etching, but the downside was significantly slower PEC etch rates.

The next layer was the 50 nm n^{++}GaN contact layer, which had a Si concentration of ~1.7 to 2.5 × 10^{19} cm^{-3}. Further detail about this layer are discussed in Section 3.1.4. The 15 nm n-AlGaN layer was used as the stop-etch during PEC top-down etching of n^{++}GaN within the aperture, but this layer is not required. With a Si concentration of ~2.7 × 10^{19} cm^{-3}, n-AlGaN was designed with a higher doping than the n-GaN layers to prevent n-AlGaN from acting as an EBL. While an EBL is useful on the p-side to reduce carrier leakage, an n-side EBL would prevent electrons from entering the active region. The n-AlGaN layer had an Al composition of ~40% and it was found that lower compositions could be obtained using higher growth temperatures.[127]

Above the n-AlGaN layer is the relatively thick ~763 nm n-GaN layer that comprises the majority of the 7λ VCSEL cavity. For the recent *m*-plane GaN 23λ VCSELs that achieved CW operation, the n-GaN thickness was increased to ~3217 nm, as described in Section 4. The Si concentration for this n-GaN layer was ~2.3 × 10^{18} cm^{-3} for each of the nonpolar VCSEL designs. There is a tradeoff between the doping in terms of operating voltage and internal loss. While the voltage could be reduced by increasing the doping, it leads to higher levels of optical absorption and internal loss. Previously, optimizing the doping levels has not been a critical concern during the development of nonpolar ITO VCSELs because the total internal loss of the III-nitride layers is estimated to be relatively low compared to the loss due to an ITO intracavity contact.[58] By replacing ITO with a III-nitride TJ to significantly reduce the internal loss, optimizing the doping levels could play a stronger role on VCSEL

performance. By reducing the doping concentration, the lower internal loss would decrease the threshold current, but one problem could be an increased operating voltage. Although not experimentally tested, one potential solution to minimize both internal loss and voltage could be to use a modulated doping profile with lower-doped layers aligned with the peaks of the optical standing wave and higher-doped layers aligned with the nulls.

Above n-GaN is the 7×MQW active region with 3 nm InGaN QWs and 1 nm GaN barriers, as reported in the initial TJ VCSEL design.[58] As discussed in Section 4.5, a relatively thick active region (2×MQW with 14 nm QWs and 1 nm barriers) was used in the VCSEL design that achieved CW operation. Further active region design considerations are discussed in Section 3.1.2. The next layer is the 5 nm p-AlGaN EBL, which had a Mg concentration of ~6×10^{19} cm^{-3} and further details about this layer are described in Section 3.1.3. Lastly, the 62.2 nm p-GaN layer had a Mg concentration of ~2×10^{20} cm^{-3} and the 14 nm p^{++}GaN layer had a Mg concentration of ~2×10^{21} cm^{-3}.[127]

The MBE TJ regrowth for the original TJ VCSEL design consisted of 39.6 nm n^{++}GaN, 39.6 n-GaN, 39.6 n^{++}GaN and 22.1 nm n-GaN with Si concentrations of 1.1×10^{20} cm^{-3} for n^{++}GaN and 1×10^{19} cm^{-3} for n^{+}GaN.[58] While a modulated doping profile was originally used to minimize internal loss by aligning the highly doped regions with the null of the optical mode, a simplified doping scheme was employed for more recent TJ VCSELs, consisting of a thick n-GaN region sandwiched between thin n^{++}GaN regions for contact. More details about the TJ intracavity contact are described in Section 3.5.

3.1.2. Active Region Design

GaN-based VCSELs have active regions consisting of multiple periods of InGaN QWs and GaN barriers. One of the primary goals during VCSEL active region design is to minimize

the threshold current for lasing. The QW thickness, GaN barrier thickness, and number of QWs can each strongly affect VCSEL performance as they affect the gain enhancement factor, carrier injection efficiency, and gain versus current characteristics. Unlike LEDs and edge-emitting lasers, it is important for VCSELs to maximize the overlap of the active region with the peak of the optical standing wave to increase the gain enhancement factor, which increases the confinement factor and reduces the threshold. For a QW placed at the antinode of the optical standing wave, the enhancement factor approaches a peak value of 2 as the QW thickness decreases. For active region designs with a large number of QWs, the enhancement factor can be maximized by decreasing the total thickness of the MQW to increase the overlap between the peak intensity of the mode and each layer of the QWs. This motivated the use of thin GaN barriers (1-nm-thick) and relatively thin InGaN QWs (3-nm-thick) for the 7×MQW active region in previous reports of *m*-plane GaN VCSELs.[58] However, note that there can be a reduction in radiative recombination efficiency and gain per well if the GaN barriers are too thin to efficiently confine carriers.

Another important consideration during active region design is the threshold modal gain (i.e., the total loss in the laser) and the gain versus current characteristics for a particular QW design. The internal parameters and gain versus current characteristics can be experimentally extracted by length-dependent analysis of edge-emitting lasers.[17,122,134,135] Instead of VCSELs, edge-emitting lasers are used for this type of analysis because it is much easier to vary the cavity length among devices on the same wafer. Based on the confinement factor from TMM simulations and length-dependent analysis of violet-emitting *m*-plane GaN edge-emitting lasers carried out by Farrell et al.,[122,134] J. Leonard et al. calculated the modal gain versus current density for violet-emitting 7λ VCSELs with various numbers of QWs, as

shown in Figure 27(b).[58] Active regions with more QWs have a higher transparency current density but also have higher differential gain (i.e., the slope of the gain vs. current density curve). This means that for a cavity with a significant amount of optical loss (e.g., absorption from an ITO layer), a greater number of QWs leads to a lower threshold. For example, a 10×MQW is predicted to produce the lowest threshold for an ITO VCSEL while a VCSEL with a III-nitride TJ intracavity contact (with lower optical absorption than ITO) is predicted to have the lowest threshold using a 7×MQW active region design.[58] As further described in Ref [127], this analysis motivated changing from the 5×MQW design used in the original *m*-plane GaN VCSELs,[4,29,136] to the 10×MQW active region,[3] and later to the 7×MQW design.[30,58,65] However, as described in Section 4.4.1, there have been problems with the 7×MQW design, and a 2×MQW with 14 nm QWs and 1 nm barriers was used in the *m*-plane GaN VCSELs that achieved CW operation, as described in Section 4.5.

Another important consideration during active region design is the carrier injection efficiency and uniformity for a given number of QWs. For designs with a large number of GaN barriers, carriers may not be able to uniformly populate all of the QWs, and some of the QWs can act as absorbing layers that increase the internal loss within the cavity. This can be avoided by decreasing the number of QWs or by reducing the GaN barrier thickness. However, reducing the GaN barrier thickness further would probably not be beneficial because the barriers are already quite thin at 1 nm in the latest *m*-plane GaN VCSEL design, and the QW quality can decrease if the GaN barrier is too thin.[137] Based on recent EL quick-test measurements of LED samples, VCSEL performance could likely be improved by increasing the GaN barrier thickness. However, it is also important to keep in mind the tradeoff that thicker barriers can reduce the gain enhancement factor.

Despite the various active region designs that have been employed for *m*-plane GaN VCSELs, there has not been a direct comparison between active region designs for fully-processed VCSELs. One of the goals of the work described in Section 4.3 was to directly compare VCSEL active region designs, but none of those VCSELs were able to lase. During the fabrication of the VCSELs that achieved CW operation described in Section 4.5, VCSELs were fabricated with 7×MQW (3 nm QWs and 1 nm barriers) and 2×MQW (14 nm QWs and 1 nm barriers) active regions. Although some comparisons were made, it would be useful to continue comparing active region designs in fully-processed VCSELs for future work. Note that the gain offset factor (i.e., alignment of the Fabry-Perot cavity resonance wavelength(s) with the peak gain) can strongly affect VCSEL performance, which could make it difficult to compare active region designs. This is particularly a factor for short cavity length VCSEL designs (~7λ) because the large mode spacing only allows one resonance wavelength to align with the peak gain. This effect is less of a problem for longer cavity length VCSELs (~23λ) because they have a shorter resonance mode spacing, so there are multiple resonance wavelengths that fall within the peak gain. Furthermore, longer cavity length VCSELs have improved thermal performance. As further discussed in Section 4.5, the peak gain redshifts at higher temperatures, higher duty cycles, and higher current injection levels, which can also affect VCSEL performance (e.g., the threshold current) and make it difficult to compare active region designs. Therefore, with improved thermal performance and better mode alignment, longer cavity length VCSELs would likely provide more consistent results among samples and be more suitable to directly compare active region designs for fully-processed VCSELs.

3.1.3. Electron Blocking Layer (EBL)

Although a direct study on the effect of the p-AlGaN EBL for *m*-plane GaN VCSELs has not been carried out, SiLENSe simulations have suggested that the injection uniformity can be improved for active region designs with more than five QWs by switching from the 15 nm EBL, as was used in early demonstrations,[4,29] to a 5 nm EBL.[127] These simulations motivated the use of a 5 nm EBL in later reports,[3,30,58,65] but it would be useful to carry out future experiments on full *m*-plane GaN VCSEL structures to find the optimal thickness and composition of the EBL. It is important to mention that the EBL design can also depend on the VCSEL emission wavelength. For example, higher indium content InGaN QWs (e.g., green-emitting InGaN QWs) have relatively deep QWs due to the reduced band gap for InGaN, which leads to better carrier confinement and an EBL may not be necessary in this case. As described in Ref. 127, one problem with the p-AlGaN EBL was Mg diffusion into the MQW which can reduce the radiative efficiency of the active region. Based on quick-test EL measurements, the light output power was tripled by reducing the Cp_2Mg flow from 30 SCCM to 12.5 SCCM during p-AlGaN EBL growth.[127] This supported the notion that Mg diffusion into the MQW was degrading the performance. A sample without an EBL had relatively lower output power, which suggested that the EBL is an important part of the design to enhance the active region performance.[127] As discussed in Section 4.4.1, the p-AlGaN EBL may have been causing a problem for recent MOCVD growths. Growing the standard VCSEL epitaxial structure frequently resulted in low (< 1 mW) EL output power based on quick-test measurements. As discussed in Section 4.4.1, this problem was solved by removing the EBL, so the problem could have been due to Mg diffusing into the MQW. This could possibly be

improved by increasing the p-AlGaN growth temperature to reduce the Al composition (which also reduces the Mg concentration) or by decreasing the Cp_2Mg flow during growth.

3.1.4. n^{++}GaN and p^{++}GaN Contacts

Reducing the contact resistance is important because it can lower the VCSEL operating voltage which leads to reduced internal heating during CW operation. Contact optimization has not been a priority as previous devices have had a fairly low turn-on voltage and differential resistance, so the contact has not significantly limited device performance. The n^{++}GaN contact layer has had a relatively high doping of ~2.5×10^{19} cm^{-3}, but there has not been much previous work to optimize this layer or determine whether the doping level is sufficient to yield Ohmic contacts. Based on recent CTLM measurements from J. Kearns, the doping level and surface treatment prior to metallization affected the n^{++}GaN contact for test samples. The standard Ti/Au (10/500 nm) contact on the n^{++}GaN layer showed Ohmic behavior with a specific contact resistivity of ~5.7×10^{-5} Ω cm^2 while another sample with a 15-minute 11.7 M KOH dip prior to Ti/Al/Ni/Au (20/100/100/100nm) deposition had a value of ~5.9×10^{-5} Ω cm^2. However, a 15-minute HCl dip prior to metallization showed non-Ohmic behavior for each metal contact structure. Similar samples were fabricated using a higher Si concentration by doubling the SiH_4 flow to 5 SCCM during n^{++}GaN MOCVD growth. Using Ti/Au contacts, a sample with no surface treatment had a contact resistivity of ~9.3×10^{-5} Ω cm^2 and a sample with a 15-minute KOH dip prior to metallization had a value of ~8.2×10^{-5} Ω cm^2. Similar to the previous samples, HCl treatments prior to metallization showed non-Ohmic behavior. While relatively simple Ti/Au (10/500 nm) n-contacts have been used, the contact resistance could likely be improved by using more optimal metal contact structures. Although increasing the doping of the n^{++}GaN layer could improve the contact, it could cause

higher optical absorption and internal loss within the VCSEL structure. This could be avoided by using the PEC top-down etch to remove n^{++}GaN within the aperture; however, highly-doped n^{++}GaN can be difficult to PEC etch. As discussed in Section 4.4.5, the standard n^{++}GaN layer that was used in previous devices was unable to etch during PEC top-down etching. It has been found for our process that PEC top-down etching is not successful for n^{++}GaN with doping concentrations greater than 1×10^{19} cm^{-3} due to its short photoexcited lifetime.[125] Due to this, as discussed in Section 4.5, the *m*-plane GaN VCSELs that achieved CW operation were fabricated without the PEC top-down etch and the n^{++}GaN layer was reduced from 50 nm to ~26 nm to reduce optical absorption.

One significant factor that has contributed to a high operating voltage has been due to the p^{++}GaN/n^{++}GaN TJ contact as TJ VCSELs showed a ~1.5 V increase in forward voltage compared to ITO VCSELs.[58] While the cause of this is not well understood, there have been recent improvements in the voltage, as discussed in Section 4.5 for recent VCSELs that achieved CW operation. This improvement may be due to improvements in MBE TJ regrowth or possibly due to the removal of the PEC oxide residue prior to n-contact deposition.

Most of the p^{++}GaN contact optimizations were conducted during the initial development stages of nonpolar GaN VCSELs, as described in Ref. 126. There were also some processing-related issues that increased the voltage, as described in Ref. 127, including problems such as p-GaN plasma damage from IBD deposition as well as a voltage increase after flip-chip bonding at 300 °C.[127] Even with 50-nm-thick ITO above p^{++}GaN, IBD deposition of the p-DBR was found to increase the voltage. While there was always some degree of ion damage, this problem could be minimized by reducing the IBD beam power. Although it has not been verified experimentally, IBD damage may not be a problem for

VCSELs with n-GaN TJ intracavity contacts because they are thicker (> 100 nm) than ITO contacts (~50 nm) and because plasma damage creates n-type nitrogen vacancies.[127]

3.2. Flip-Chip Bonding

Low yield has been an ongoing problem for nonpolar GaN VCSELs and has been largely due to flip-chip bonding. For the initial nonpolar GaN VCSELs,[4,29] the flip-chip bond consisted of a Au-Au thermocompression bond at 300 °C for 2 hours, and the flip-chip substrate comprised of sapphire that was coated with Ti/Au. By measuring the *I-V* before and after bonding, it was found that the voltage significantly increased due to the 300 °C anneal. It was found that bonding at 300 °C increased the voltage but it did not matter whether the bonding time was 30 minutes or 2 hours, and the same effect was observed for bonding in an air ambient compared to a nitrogen ambient. One way to mitigate the *I-V* damage was to decrease the bonding temperature to 200 °C and bond for 2 hours, and this process was used in slightly more recent reports of nonpolar VCSELs.[4,29]

Other than flip-chip bonding conditions, another important design consideration is the type of flip-chip substrate. There are several factors to consider when choosing a flip-chip substrate, such as the thermal conductivity, thermal expansion coefficient, surface roughness, surface planarity, chemical stability in KOH, and cost. Previously, sapphire substrates were used as the flip-chip substrates due to their low cost, availability, and stability in KOH. However, sapphire's low thermal conductivity (~0.25 W/Kcm) leads to poor thermal performance and makes it more difficult to achieve CW operation. As described in Section 4.5, note that sapphire flip-chip substrates were used in the *m*-plane GaN VCSELs that achieved CW operation, and despite the poor thermal conductivity of sapphire, other

significant thermal improvements were made to enable CW lasing. Several flip-chip substrates have been tested during C. Holder's and J. Leonard's development of nonpolar GaN VCSELs, including sapphire, GaN, silicon, silicon carbide, aluminum, and copper. GaN is an excellent submount due to its high thermal conductivity and equivalent thermal expansion coefficient to the GaN cavity, but bulk GaN substrates are relatively expensive. Although silicon submounts can be used, note that it reacts with KOH to produce hydrogen gas. Aluminum could be a good choice, but it is highly susceptible to etching and bubbling in KOH. One of the most significant problems has been cracking after flip-chip bonding, which is caused by the high temperature and bonding force. Strain could also play a role in cracking as VCSEL devices consist of several materials with various coefficients of thermal expansion. Copper has seemed to have the best results previously; however, as discussed in Section 4.4.6, the unpolished copper blocks did not have a completely planar surface, which led to problems with cracking and low device transfer percentage. While Au-Au thermocompression bonding was used previously, the recent VCSEL design that achieved CW operation used Au-In solid-liquid interdiffusion (SLID) bonding, as discussed in Section 4.4.6.2. Due to the lower temperature and force required for Au-In SLID bonding (as well as the liquid phase present that softens the bond), cracking was significantly reduced. While several submounts were previously abandoned due to cracking (e.g., silicon and silicon carbide), these materials are now possible using the improved flip-chip bonding method. Using Au-In SLID bonding, the main considerations when selecting a flip-chip substrate are KOH compatibility, surface planarity, and thermal conductivity. Further details about recent flip-chip bonding experiments are discussed in Section 4.4.6.

3.3. PEC Etching

One unique advantage of *m*-plane GaN VCSELs is that it allows for growth substrate removal using band-gap-selective PEC undercut etching of a sacrificial layer. This allows precise cavity length control which is important when aligning the cavity resonance wavelength with the peak gain wavelength of the VCSEL. In comparison, growth substrate removal for flip-chip *c*-plane GaN VCSELs has conventionally consisted of thinning and polishing, which makes cavity thickness control difficult. Precise cavity length control can be achieved using PEC etching because the sacrificial layer can be defined during epitaxial growth, and MOCVD growth rates can be precisely calibrated using XRD. PEC etching is also a very low-damage etching technique as opposed to other substrate removal techniques, such as laser lift-off which can cause crystal damage. PEC etching is possible on *c*-plane, but it can result in significant roughness due to roughening in KOH, which is not ideal for VCSELs. The original *m*-plane GaN VCSELs from UCSB used PEC etching of a sacrificial 3×MQW (7 nm InGaN QWs, 5 nm GaN barriers, and $\lambda \sim 415$ nm) using a 0.1 M KOH solution with illumination with a 405 nm CW laser with an output power of ~200 mW.[127] Photogenerated electrons were eliminated by a reduction reaction at the Ti/Au cathode on the *m*-plane GaN substrate and photogenerated holes diffused to the sidewall of the sacrificial MQW where they assisted in oxidation of Ga atoms.[123,124] The etch progressed as the resulting oxide dissolved in the KOH solution. There are also photogenerated carriers within the active MQW, so the sidewall of the active region was protected with SiN_x to prevent it from etching, though note ion implantation was recently found to be more effective. Several PEC etching experiments have been performed by C. Holder and J. Leonard during earlier optimization of

nonpolar GaN VCSELs. For example, RMS roughness of the n-side surface was found to be inversely proportional to KOH concentration, but lower concentrations etch at a much slower rate.[127] For more details about previous PEC etching experiments, see Ref. 127 and Ref. 126. While PEC undercut etching has been effective at removing the growth substrate, recent results showed that a rough oxide forms after PEC etching, which can contribute to scattering loss. Section 4.4.5 describes recent PEC etching experiments that have been conducted to smoothen the surface morphology.

3.4. Current Aperture Design

There have been several current aperture designs used for nonpolar GaN VCSELs, including dielectric SiN_x apertures,[4,29] Al ion implanted apertures,[3,30,58] and PEC air-gap apertures.[65] These aperture designs have each had significant impacts on VCSEL performance. The most common current aperture design for GaN-based VCSELs has been a dielectric aperture, such as SiO_2 or SiN_x deposited on the p-side of the device outside the circular aperture. In C. Holder's initial demonstrations of nonpolar GaN VCSELs at UCSB, the current aperture design consisted of SiN_x deposited using plasma-enhanced chemical vapor deposition (PECVD). This design can effectively confine current to the aperture of the device, but simulations have suggested that there can be poor lateral optical confinement for dielectric apertures with ITO intracavity contacts, which can result in an anti-guiding structure.[120,121,138] The main problem comes from the step-height created by the dielectric aperture before ITO is deposited. This can be solved by creating a planar ITO design (e.g., etching the p-GaN prior to deposition of the dielectric aperture to create a flat surface prior to ITO deposition); however, etching p-GaN can potentially cause plasma damage that extends

within the aperture. Another type of planar ITO design was demonstrated by G. Cosendey et al. at EPFL which used RIE to passivate p-GaN outside the aperture.[80] This was attempted at UCSB, but the aperture showed current leakage, especially after the flip-chip bonding process which appeared to heal the p-GaN damage.[127] This led to J. Leonard's development of using Al ion implantation to define the current aperture, which could also create a planar ITO design as the height of the semiconductor does not change after implantation. Using a dose of 10^{15} cm^{-2}, Al ion implantation was performed at normal incidence at 10, 20, and 30 keV implantation energies to create test samples to compare with the SiN_x aperture that was previously used at UCSB. The SiN_x aperture showed a ~1 V increase in voltage compared to ion implanted samples, which was attributed to the plasma damage induced from the PECVD process.[80,139–142] Al ion implantation at 20 keV also caused a ~2% reduction in the p-GaN refractive index, which slightly improves the lateral confinement factor with predicted values of 98% for a 12 μm aperture diameter and below 90% for diameters less than 6 μm.[127] Although the initial demonstration of an *m*-plane GaN VCSEL with an ion implanted current aperture only had a peak output power of 12 μW, it had a ~5× lower threshold current density of ~16 kA/cm^2 compared to previous devices with a SiN_x aperture. The ion implanted aperture was also employed in the first demonstration of a GaN VCSEL with a TJ intracavity contact, which reached a peak output power of 550 μW and had a threshold current density of 3.5 kA/cm^2.[58]

Ion implantation has many advantages, such as providing effective current confinement, a small degree of lateral optical confinement due to the slight reduction in refractive index for the implanted region, a planar intracavity contact design as the height is unchanged after implantation, no risk of p-GaN plasma damage within the aperture (unlike

PECVD-deposited SiN_x), and it is a robust process with high yield. As previously discussed in Section 2, Al ion implantation is also useful because it passivates the MQW outside the aperture to protect the active region during PEC etching. Therefore, Al ion implantation was employed in the work described in this thesis and was included in the first demonstration of CW lasing for *m*-plane GaN VCSELs, as described in Section 4.5. However, there are some potential problems with Al ion implantation, such as increased optical absorption that can lead to internal loss. For example, boron implantation was reported to increase the GaN absorption coefficient to 800 cm^{-1} at 453 nm, which would cause a round-trip absorption of 0.42% in the cavity for a photon traveling within the implanted region.[63] Another issue is lateral optical confinement. Although Al ion implantation decreases the refractive index slightly, there are other current aperture designs that can provide better lateral optical confinement.

An air-gap aperture is one example of a design that can provide both effective current confinement and lateral optical confinement. In 2016, J. Leonard et al. demonstrated an *m*-plane GaN-based VCSEL with a PEC etched air-gap aperture and ITO intracavity contact that had a threshold current of 25 mA (22 kA/cm^2) and a peak output power of 180 μW.[65] This was created by using PEC etching to laterally etch the active MQW (~28 nm thick) outside the aperture to create a small air gap, and a schematic of the PEC air-gap aperture VCSEL is illustrated in Figure 26. With a high index contrast between GaN (n~2.557 at 405 nm) in the aperture and air (n = 1) outside the aperture, the air-gap aperture design has a much higher lateral confinement factor. The core-cladding effective index step was predicted to be 0.049 (2.344-2.295) for the PEC air-gap aperture design while an ion implanted aperture VCSEL was predicted to have a value of ~0.001.[65] The increased lateral optical confinement helps reduce the threshold but also increases the normalized frequency, which promotes higher

lateral optical modes within the VCSEL. Reducing the aperture diameter can help promote single transverse-mode emission if it is required for a certain application, but in general, higher-order and multi-mode operation is not a problem. For example, most oxide-aperture GaAs-based commercial VCSELs have multimode emission.[143,144] Despite the increased lateral optical confinement of the air-gap aperture, the high index contrast can also cause scattering loss which can increase the threshold. As discussed in Section 4.4.3, recent results showed a rough oxide residue can form after PEC etching which could further cause scattering loss. Another problem with the PEC air-gap aperture was very low yield due to the fragility of the air-gap design. As discussed in Section 4.4.6, low yield after flip-chip bonding has been a significant problem even for designs without fragile air-gap apertures. Therefore, due to its structural integrity among other advantages, Al ion implantation was used to define the current aperture for recent VCSELs, as discussed in Section 4.

Although it has not yet been fully demonstrated for GaN-based VCSELs, another promising aperture design is the buried tunnel junction (BTJ) aperture. Effective electrical confinement has been reported using a BTJ in III-nitride micro-LEDs,[145,146] and utilizing a BTJ aperture in GaN-based VCSELs is a promising solution for providing both electrical and optical confinement. During recent processing of nonpolar GaN VCSELs, BTJ aperture devices were fabricated in addition to devices with ion implanted apertures, as described in Section 4.5.1. After MOCVD growth of the VCSEL epitaxial structure up to the p^{++}GaN and etching a mesa, the main steps to fabricate the BTJ aperture are to grow n^{++}GaN using MBE to form the TJ, etch the n^{++}GaN and p^{++}GaN outside the aperture using RIE, and perform another MBE regrowth to grow an n^{+}GaN current spreading layer followed by an n^{++}GaN contact layer that buries the TJ. The subsequent fabrication steps are equivalent to the ion

implanted aperture design. Further growth and fabrication details of BTJ aperture VCSELs are described in Section 4.3, and a schematic illustration is shown in Figure 44. The BTJ design confines current to the highly-doped n^{++}GaN/p^{++}GaN TJ in the aperture as there is a much larger barrier for current to flow outside the aperture through the lower-doped n^{+}GaN/p-GaN region. Moreover, RIE passivates the p-GaN outside the aperture to further prevent current leakage. Recently-fabricated BTJ aperture devices were found to successfully confine current to the aperture. Note that one potential problem of replacing the ion implant aperture with the BTJ aperture is that ion implantation no longer protects the active MQW during PEC etching. Despite using IBD to deposit SiN_x on the sidewall of the active MQW, the active MQW partially etched during PEC etching. Further details about BTJ aperture VCSELs are described in Section 4.3 and Section 4.5. Despite these challenges, the BTJ design is particularly promising because it avoids some of the problems of ion implantation, such as implant-induced optical absorption and poor lateral optical confinement. The BTJ aperture can provide lateral optical confinement in future designs by incorporating AlGaN in the second MBE regrowth to provide core-cladding index contrast. After recently demonstrating *m*-plane GaN VCSELs with MOCVD-grown TJ intracavity contacts in a collaboration with S. Lee,[117] MOCVD is a promising alternative to MBE to create BTJ aperture VCSELs.

3.5. Intracavity Contact Design

The intracavity contact has been found to have a significant impact on VCSEL performance and can affect the optimal number of QWs to lower the threshold based on the amount of internal loss. Without electrically conductive DBRs, vertical current injection on the p-side is not possible for GaN-based VCSELs. Instead, current is injected laterally from

the edges of the aperture. Due to the high spreading resistance of p-GaN, GaN VCSELs have required an intracavity contact for current spreading. Section 3.5.1 discusses ITO intracavity contacts, which have been the most common design for GaN-based VCSELs. However, ITO can cause significant absorption loss which can be reduced by replacing ITO with III-nitride TJ intracavity contacts, as described in Section 3.5.2.

3.5.1. Indium Tin Oxide (ITO)

The most common intracavity contact for GaN VCSELs has been ITO because it is electrically conductive and optically transparent, though it is not as optically transparent as III-nitride TJ intracavity contacts, as described in Section 3.5.2. Due to the VCSEL performance improvement of switching from ITO to TJ intracavity contacts,[58] the work described in this thesis focused solely on TJ VCSELs, as described in Section 4. Nonetheless, ITO intracavity contacts have been widely used and were present in GaN VCSEL designs that have achieved over 1 mW of output power.[62,74] This section summarizes the developments of ITO intracavity contacts for GaN VCSELs created at UCSB, and further information is found in Ref. 127.

In the earliest *m*-plane GaN VCSEL design, electron-cyclotron resonance (ECR) sputtering was used to deposit very smooth, conductive, and transparent ITO intracavity contacts with a thickness ~50 nm. [4,29,126,136] However, that ECR sputtering system was not purchased so another ITO deposition technique was developed. The main goal is for the ITO layers to be transparent to minimize absorption loss, electrically conductive to provide uniform current spreading on the p-side throughout the VCSEL aperture, and smooth because roughness can lead to scattering loss. Another requirement is that the ITO deposition technique needs to avoid damaging the p-GaN, which is quite sensitive to plasma damage.

This requires deposition techniques such as remote-plasma ECR sputtering or low-damage physical vapor deposition (e.g., electron beam evaporation). Electron beam evaporation of ITO was chosen for its simplicity and reduced cost compared to ECR sputtering. As reported in Ref. 127, several ITO deposition optimizations were performed with the goal of depositing ITO with < 1 nm RMS roughness, high transparency, and high conductivity. Based on an ITO deposition temperature series, increasing the temperature was found to decrease the resistivity and increase the transparency up to a saturated value of 90% at 405 nm. However, the RMS roughness increased to 5 nm at 200 °C, so despite the ideal transparency and conductivity, the rough morphology was not suitable for VCSELs. The next experiment was to investigate the effect of oxygen (O_2) flow and pressure on the ITO films, which showed that low O_2 flows produced very rough, fairly conductive (~3.5×10^{-3} Ω-cm), and transparent (~95% at 405 nm) ITO films. While these conditions could be useful for LEDs that could benefit from roughness for light extraction, the O_2 flow and pressure could not be varied to produce < 1 nm RMS roughness for VCSELs while depositing at a high temperature to yield transparent and conductive films. The next experiment was aimed at producing high quality ITO films by growing an initial layer at a low temperature (room temperature ~25 ^{o}C to 100 °C), followed by a thicker layer grown at a higher temperature (≥ 250 ^{o}C) to promote the growth of large ITO grains with < 1 nm RMS roughness, while maintaining the conductivity and transparency. Results showed that the ITO grain size increased due to the reduced number of nucleation sites for the low-temperature ITO layer which produced a smoother morphology (~0.3 nm RMS roughness) while maintaining the high transparency and conductivity of the high-temperature ITO deposition. The optimal ITO deposition conditions consisted of the following. The low-temperature 4.4-nm-thick ITO layer was deposited at room temperature

and the high-temperature ~40-nm-thick ITO layer was deposited at 400 °C at an O_2 flow rate of 30 SCCM, pressure of 0.27 mTorr, and deposition rate of 0.2 Å/s. The ITO films had a transmission of 86% at 405 nm with a large absorption coefficient ~2000 cm^{-1}, which implied that the internal loss in ITO VCSELs is dominated by the relatively large optical loss in ITO.[127]

3.5.2. III-Nitride Tunnel Junctions (TJs)

Nonpolar GaN VCSEL performance was increased significantly by replacing the ITO intracavity contact with a III-nitride TJ grown by MBE.[58] The main advantage of the TJ is that it has much lower levels of optical absorption compared to ITO, especially at violet wavelengths. MBE was used for TJ regrowth because MOCVD-grown III-nitride TJs have had highly resistive contacts,[147–151] which is caused by hydrogen repassivation of p-GaN during MOCVD growth of n^{++}GaN. MOCVD-grown p^{++}InGaN/n^{++}GaN III-nitride TJs have been demonstrated for micro-LEDs, but the p-GaN needed to be activated via sidewall activation because the MOCVD-grown n-GaN prevented thermal activation of buried p-GaN.[118] On the other hand, MBE regrowth can be performed after p-GaN activation and enables growth of n-GaN layers without repassivating the p-GaN. While a lower band gap material (e.g., an InGaN contact layer) can be used to reduce the TJ voltage, it could lead to significant optical absorption and internal loss if incorporated in a GaN VCSEL, especially for violet-emitting devices. Absorption could be minimized by aligning the null of the optical mode with the InGaN layer, similar to the ITO VCSEL design, but using a p^{++}GaN/n^{++}GaN TJ would be ideal for minimizing optical absorption. Note that violet-emitting or UV-emitting (< 390 nm) devices would have particularly high absorption losses from ITO, so a III-nitride TJ would significantly reduce optical loss; however there is less absorption in ITO for blue-

emitting (405 nm) or green-emitting (525 nm) devices, so switching to a TJ contact in those devices would have a less significant impact on performance.

In the TJ VCSEL design, the p^{++}GaN layer is grown via MOCVD and the n^{++}GaN layer is grown via ammonia MBE with solid source effusion cells for Ga and Si and thermally cracked NH_3 as the nitrogen precursor for GaN growth. While MOCVD growth is performed at atmospheric pressure with high levels of hydrogen present, MBE growth is performed at vacuum with much lower hydrogen levels at a pressure ~10^{-6} so p-GaN does not become repassivated by hydrogen. Several steps are performed prior to MBE TJ regrowth during VCSEL fabrication. After MOCVD growth and p-GaN activation (600 °C for 15 minutes), a mesa is etched using RIE. In the ion implanted aperture VCSEL design, the next step is to deposit a Ti/Au hardmask and then the sample is sent to Leonard Kroko, Inc. to perform Al ion implantation to define the current aperture. After removing the Ti/Au hardmask in aqua regia, the samples are prepared for MBE TJ regrowth. After an acetone and isopropanol solvent clean, the samples are loaded into the MBE chamber and baked at 400 °C for one hour. Each of the MBE TJ regrowths for nonpolar GaN VCSELs have been performed by E. Young, who is an expert in MBE growth. The MBE TJ regrowth reported in Ref. 58 was performed at 750 °C (measured by pyrometry) with a Ga flux of ~10^{-7} Torr and NH_3 flow rate of 200 sccm. The streaky reflection high-energy electron diffraction (RHEED) pattern during growth indicated a smooth MBE growth morphology. The total MBE regrowth was ~141 nm thick, consisting of n^{++}GaN/n-GaN/n^{++}GaN/n-GaN (39.6 nm/39.6 nm/39.6 nm/22.1 nm). The Si concentration was 1.1×10^{20} cm^{-3} for n^{++}GaN and 1×10^{19} cm^{-3} for n-GaN while the MOCVD-grown 14-nm-thick p^{++}GaN had a Mg concentration of ~2.5×10^{20} cm^{-3}. The step-function doping was used to reduce internal loss by aligning the highly-doped layers with the

nulls of the optical mode, but more recent TJ designs have consisted of n^{++}GaN/n-GaN/n^{++}GaN with a relatively lower doping for the thick n-GaN layer in the middle. Based on Hall method measurements on test samples, the resistivity was ~4×10^{-4} Ω-cm for n^{++}GaN and ~4.4×10^{-3} Ω-cm for n-GaN.

In a reverse-biased TJ, charge transport occurs across the junction as electrons in the valence band of the p-type material tunnel across the depletion region to empty states in the conduction band of the n-type material. This leaves a hole behind in the p-type material, which results in hole injection on the p-side for the VCSEL device. In order to reduce the voltage required for tunneling, the depletion width can be minimized by heavily doping the p-type and n-type materials (p^{++}GaN/n^{++}GaN). The simulated performance of the TJ was predicted using energy band structure simulations in SiLENSe, as shown in Figure 40.

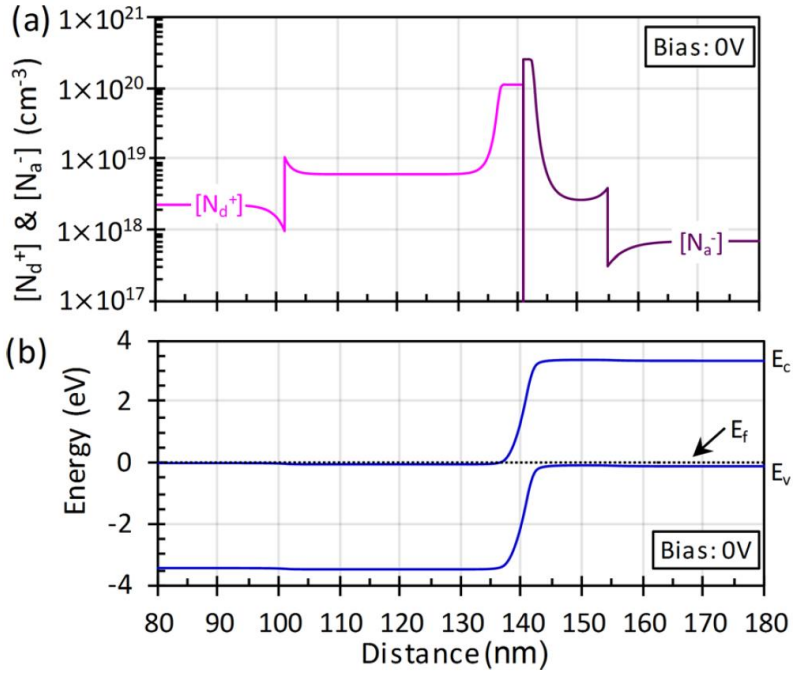


Figure 40. SiLENSe simulations of the III-nitride TJ reported in Ref. 58. (a) Ionized donor and acceptor concentrations, assuming a donor ionization energy of 5 meV and acceptor ionization energy of 165 meV. (b) Energy band diagram of the TJ, showing a total depletion width of ~7.95 nm with 6.25 nm of depletion on the n-side. Reprinted from [Leonard, J. T., Young, E. C., Yonkee, B. P., Cohen, D. A., Margalith, T., DenBaars, S. P., Nakamura, S. (2015). Demonstration of a III-nitride vertical-cavity surface-emitting laser with a III-nitride

tunnel junction intracavity contact. *Applied Physics Letters*, *107*(9), 091105. https://doi.org/10.1063/1.4929944] with the permission of AIP Publishing.[58]

There was a relatively large depletion width of ~7.95 nm with 6.25 nm of depletion on the n-side which suggested that tunneling would not be possible, but TJ VCSELs only showed a ~1.5 V increase and a similar differential resistance compared to an ITO VCSEL.[58] Tunneling may have been assisted by regrowth interface or defect states that assisted carrier transport across the junction,[152–154] or perhaps tunneling occurred as SiLENSe simulations predicted a high electric field at the junction that is 2× larger than the breakdown field for GaN (5 MV/cm).[155] Based on TMM simulations, replacing ITO with a TJ intracavity contact significantly reduced the internal loss, which reduced the threshold modal gain from ~41.6 cm^{-1} to ~14.1 cm^{-1}.[127]

As discussed in Section 4.3, longer cavity length 13λ and 23λ VCSELs were fabricated with the goal of achieving CW operation, and relatively thick MBE regrowths were employed to improve current spreading on the p-side. The MBE regrowths consisted of n^{++}GaN/n-GaN/n^{++}GaN (39.6/695.3/39.6 nm for 13λ VCSELs and 39.6/1562.4/39.6 nm for 23λ VCSELs) with respective Si concentrations of 1.1×10^{20}, 2.5×10^{18}, and 1×10^{19} cm^{-3}. However, as discussed in Section 4.4, the relatively thick MBE regrowth led to significant roughness on the p-side, which prevented each of the devices from lasing due to scattering loss and reduced mirror reflectivity. Section 4.4.4 describes recent MBE regrowth experiments that showed improved the growth morphology using a thinner MBE regrowth and by using a non-incorporating indium surfactant during growth. As discussed in Section 4.5, the *m*-plane GaN VCSELs that lased under CW operation had an MBE regrowth consisted of n^{++}GaN/n-GaN/n^{++}GaN (39.6/61.7/39.6 nm) with respective Si concentrations of 1.1×10^{20}, 2.5×10^{18}, and 1×10^{19} cm^{-3}.

In a collaboration with S. Lee, we have also demonstrated nonpolar GaN VCSELs with TJ intracavity contacts grown completely using MOCVD.[117] While MOCVD-grown TJs typically passivate p-GaN with hydrogen and require a small device size to permit sidewall activation of p-GaN,[118] the p-GaN in our devices remained activated after MOCVD regrowth of the TJ, so sidewall activation was not necessary. These VCSELs were fabricated by first performing MOCVD to grow the epitaxial structure up to the p^{++}GaN. Then, the samples were treated in BHF for 5 minutes to remove a Mg-rich film on the surface to reduce the Mg diffusion into the regrown n^{++}GaN. During MOCVD regrowth of the TJ, the temperature was maintained at 750 °C for 5 minutes to activate the p-GaN and then growth commenced at 900 °C to grow 40 nm n^{++}GaN, 100 nm n-GaN, and 5 nm n^{+}GaN with Si concentrations of ~1×10^{20}, ~1.8×10^{18}, and ~1×10^{19} cm^{-3}. For TJ LED test samples, the voltage was 3.4 V at 20 A/cm^2 and 4.5 V at 1 kA/cm^2. This is reasonably close to a diode with MOCVD-MBE hybrid TJ contacts reported by E. Young et al. that had a voltage of 3.05 V at 20 A/cm^2.[156]

3.6. Main Challenge: Achieving Continuous-Wave (CW) Operation

Despite noteworthy performance improvements since 2012, the most significant challenge with UCSB *m*-plane GaN VCSELs has been their inability to lase under CW operation. This has been due to their poor thermal performance, and previous devices have only been able to lase under pulsed operation. This is a major problem because it prevents most practical applications of these devices. Many applications require a constant output power with time (i.e., CW operation), such as using VCSELs for data communication by direct modulation. However, previous *m*-plane GaN VCSELs could only lase under pulsed operation

wherein a pulse generator produces a time-varying voltage to essentially turn the VCSEL repeatedly *on* and *off* very quickly, which can be used to minimize the effects of heating. The pulse width and pulse repetition rate (frequency) can be controlled so that the device is only turned *on* for a fraction of the time, as described by the duty cycle, D, which is defined as:

$$D = PW \times f \tag{19}$$

where PW is the pulse width and f is the frequency. For example, a duty cycle of 1% means that the device is turned *on* 1% of the time while it is *off* 99% of the time. *L-I-V* and emission spectra measurements were previously collected under pulsed operation with a duty cycle of 0.3% (pulse width of 100 ns and frequency of 30 kHz).[58] Previous *m*-plane GaN TJ VCSELs were able to lase for pulse widths up to 10's of μs (duty cycle ~ 30%), but lasing was not possible at higher duty cycles.[30] The ultimate goal of this project has been to achieve stable lasing under CW operation (i.e., 100% duty cycle). However, this has been a challenging prospect due to a series of complications, and the next chapter describes the experiments that eventually led to the first demonstration of CW operation for *m*-plane GaN VCSELs.

4. Achieving Continuous-Wave (CW) Operation for *m*-plane GaN VCSELs

The main goal of this project has been to achieve lasing under continuous-wave (CW) operation for *m*-plane GaN VCSELs, which have previously only been able to lase up to ~ 30% duty cycle.[30] Lasing at higher duty cycles or under CW operation has not been possible due to the poor thermal performance of the devices. As described in Section 4.1, there are several temperature-dependent effects that can increase the threshold or even prevent lasing. Therefore, it is important to have a good understanding of heat flow during VCSEL operation, and Section 4.2 describes the thermal simulations that helped motivate design changes to improve the thermal performance. Section 4.3 describes the initial experimental plan to achieve CW lasing; however, none of the VCSELs were able to lase – even under pulsed operation. The next steps were to identify the main the problems with the VCSEL design that prevented lasing, implement solutions to those problems, and ultimately make thermal design improvements to work toward the goal of achieving CW lasing. Section 4.4 describes the key problems that were identified during VCSEL failure analysis and the experiments that were conducted to improve the VCSEL design. These design improvements were eventually successful and led to the first demonstration of CW operation for *m*-plane GaN VCSELs, as described in Section 4.5.

4.1. Temperature Effects

VCSEL performance typically degrades at higher operating temperatures and makes it difficult to achieve CW operation due to several factors. Operating VCSELs at high current

densities increases the junction temperature and redshifts the peak gain to longer wavelengths while decreasing the maximum gain due to Fermi spreading (i.e., thermal redistribution) of carriers.[157,158] Furthermore, the increased temperature causes higher non-radiative carrier losses due to carrier leakage and Auger recombination.[159–162] Therefore, higher temperatures tend to increase the threshold current for lasing,[17] which can be observed by measuring the *L*-*I* curve at various stage temperatures or by comparing the threshold under pulsed operation (low temperature) versus CW operation (high temperature). In contrast with edge-emitting lasers, higher operating temperatures can further prevent VCSELs from lasing by causing a misalignment of the cavity Fabry-Perot resonance wavelengths with the peak gain wavelength. The Fabry-Perot resonance wavelengths redshift to longer wavelengths as higher temperatures increase the effective index of the VCSEL cavity.[163] The redshift in Fabry-Perot resonance wavelength with temperature has been reported to be ~0.015 nm/°C for *m*-plane GaN VCSELs.[4] In comparison, the peak gain wavelength generally redshifts at a faster rate with temperature,[4] which can cause a misalignment with the Fabry-Perot resonance wavelength(s) and inhibit lasing. While this can be a problem when the peak gain redshifts farther away from a resonance wavelength, this phenomenon can be taken into account during VCSEL design to cause some interesting effects. While edge-emitting lasers have a higher threshold current at higher temperatures, it is possible for VCSELs to have a lower threshold at higher temperatures. This can be accomplished by designing the VCSEL to have a shorter peak gain wavelength than the Fabry-Perot resonance wavelength, so at higher temperatures, the redshifted peak gain provides better mode alignment and reduces the threshold for lasing. By tuning this gain offset parameter (i.e., the alignment of the peak gain and resonance mode wavelengths), perfect mode alignment can be achieved at a designed current injection level.

However, there can be a trade-off between achieving a low threshold and high output power; for example, output power can be maximized if there is perfect mode alignment at high current densities, but the downside would be an increased threshold due to reduced mode alignment at low injection levels. By improving the design to reduce the thermal impedance of the device, there is less heating during operation which makes it easier to achieve mode alignment at a larger range of current densities.

These temperature-dependent effects are important to consider when designing a VCSEL capable of lasing under CW operation. The next sections outline the modeling, experiments, failure analysis, and design changes that ultimately led to the first demonstration of CW lasing for *m*-plane GaN VCSELs.

4.2. VCSEL Thermal Performance and Thermal Modeling

With the goal of achieving CW operation, it has been helpful to gain a better understanding of the VCSEL thermal performance by carrying out thermal simulations in COMSOL. By building on the work of J. Leonard,[127] VCSEL thermal models were created using the COMSOL 2D axis-symmetric module with the "Heat transfer in solids" physics package. Figure 41 shows a simplified schematic of the VCSEL structure, and the color scheme corresponds to the thermal conductivity of each layer.

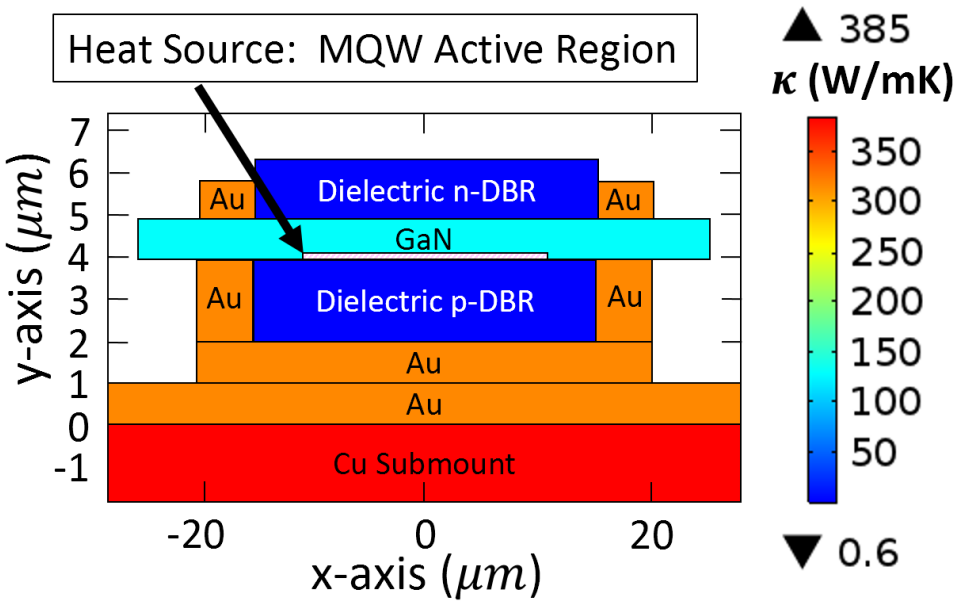


Figure 41. Simplified schematic for thermal modeling of a dual dielectric DBR VCSEL with a flip-chip design. The color scheme corresponds to the thermal conductivity of each layer. As heat generates in the MQW active region during VCSEL operation, the largest barrier to heat flow is due to the thermally-insulating bottom dielectric DBR.

Several simplifications were made in the thermal model with respect to the thermal conductivity of each layer: Ti/Au metal contacts were simplified to Au contacts, the thermal conductivity of GaN was assumed for the entire epitaxial structure, and the SiO_2/Ta_2O_5 dielectric DBRs were simplified to a uniform dielectric layer. The vertical thermal conductivity, $k_{eff,V}$, and lateral thermal conductivity, $k_{eff,L}$, of the DBRs can be defined by:

$$k_{eff,V} = \frac{d_1 + d_2}{d_1/k_1 + d_2/k_2} \tag{20}$$

$$k_{eff,L} = \frac{d_1 k_1 + d_2 k_2}{d_1 + d_2} \tag{21}$$

where d_1 and d_2 are the thicknesses of layer 1 (SiO_2) and layer 2 (Ta_2O_5), and k_1 and k_2 are the thermal conductivities of each respective layer.[164] For a DBR with quarter-wavelength-thick layers to produce a reflectance stopband centered at 405 nm (SiO_2: ~66.79 nm and Ta_2O_5: ~45.61 nm), the effective vertical and thermal conductivities are ~0.6 W/mK and ~0.57

W/mK, respectively. These values are quite similar, so the thermal model was simplified by assuming an isotropic thermal conductivity of 0.6 W/mK for the dielectric DBRs. In the thermal simulation, the temperature of each layer was initially set at room temperature (23 °C) and the active region MQW was set as the heat source with an input power of 0.25 W. Boundary conditions were defined with a constant temperature of 23 °C for the bottom and edges of the Cu flip-chip substrate, and surfaces exposed to air followed the COMSOL-defined surface-to-ambient radiation equations. Thermal simulations were run until reaching steady-state, and the thermal performance was visualized by graphing the temperature profile and thermal flux profile. Figure 42(a) shows a COMSOL thermal model of a 7λ VCSEL with a 6 μm aperture diameter.

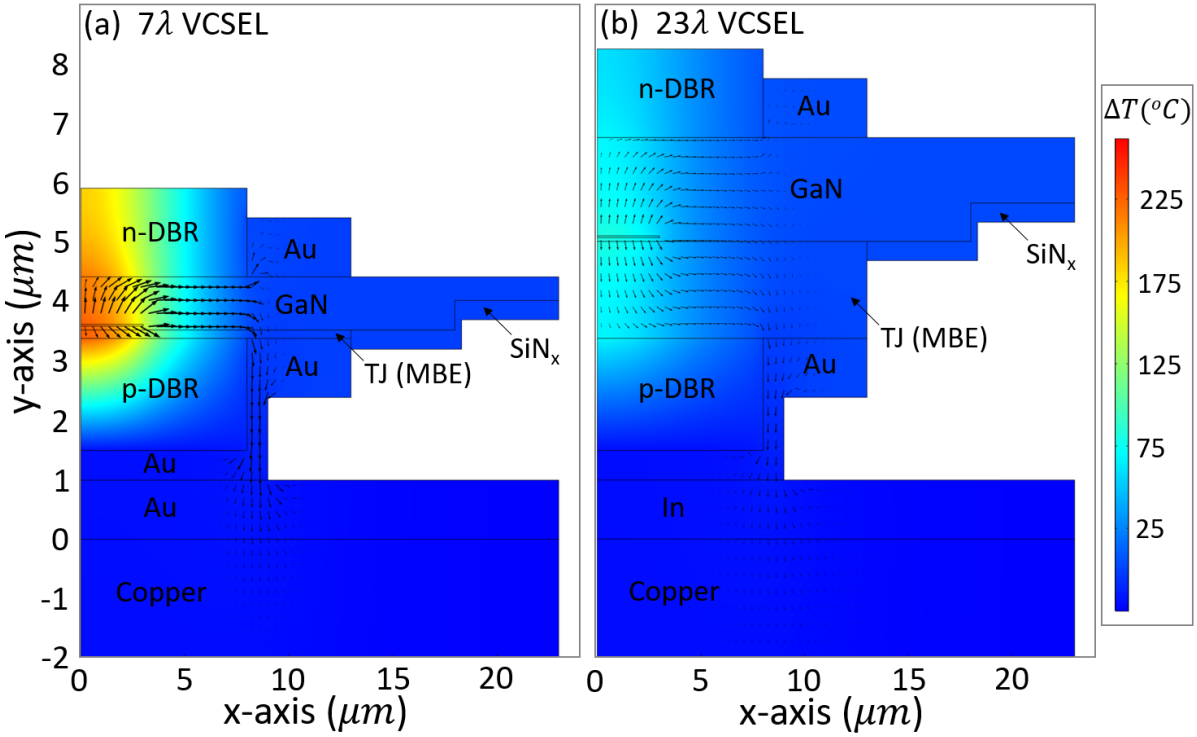


Figure 42. COMSOL thermal model of a 6 μm aperture diameter VCSEL with optical cavity lengths of (a) 7λ and (b) 23λ. The increase in temperature is shown by the color scheme and the thermal flux is shown by the overlain arrows. Increasing the cavity length from 7λ to 23λ decreases the predicted thermal impedance from 1970 °C/W to 847°C/W, respectively. Due to the thermally-insulating bottom dielectric DBR, the main pathway for heat transport is through a thin Au contact (~1 μm thick) on the sidewall of the bottom DBR toward the flip-chip substrate.

The color scheme corresponds to the temperature increase, ΔT, and the size of the overlain thermal flux arrows indicates the relative strength of the flux on a logarithmic scale. These thermal simulations revealed a bottleneck in heat flow due to the thermally-insulating bottom dielectric DBR. Based on the thermal flux arrows, heat generated in the active region cannot flow directly downward through the insulating bottom DBR, but instead, heat must first flow laterally until it reaches the gold metal contact that surrounds the bottom DBR, and then heat can flow downward through the gold contact toward the flip-chip substrate. This created a bottleneck in heat flow because the main pathway for heat transport was limited to a relatively thin (~1 μm) gold contact that coated the bottom DBR. A thicker metal pathway for heat transport would improve the thermal performance, as described later in Section 4.4.6, but the Au contact is deposited using an angled rotating fixture in an electron beam evaporator that cannot deposit layers much thicker than 1 μm. Another way to improve the thermal performance is to increase the GaN cavity length, as illustrated in the COMSOL thermal model of a 23λ VCSEL shown in Figure 42(b). By switching from a 7λ cavity length to a longer 23λ cavity length, the predicted thermal impedance improved from 1970 °C/W to 847 °C/W. Longer cavity length VCSELs are predicted to have better thermal performance because GaN has a relatively high thermal conductivity of ~ 130 W/mK, so more heat can be extracted away from the active region as it spreads throughout the GaN cavity before flowing downward through the gold contact toward the flip-chip substrate.

These thermal simulations indicated that increasing the cavity length can improve the thermal performance, which is necessary to achieving the goal of CW operation. This motivated an experiment to increase the VCSEL cavity length from 7λ to 13λ and 23λ, as described in Section 4.3.

4.3. 13λ and 23λ VCSELs with thick MBE regrowth

Based on the COMSOL thermal simulations described in Section 4.2, VCSELs with longer cavity lengths have improved thermal performance. This motivated the following experiment to modify the VCSEL design with the hope of achieving CW operation. While previous *m*-plane GaN VCSELs had a 7λ cavity length,[3,4,29,30,58,65] the cavity length was increased to 13λ and 23λ, as described in the next section. Section 4.3.1 describes the design of experiment and Section 4.3.2 delves into the fabrication details and results. Unfortunately, there were unforeseen factors caused by the design changes, and none of the devices were able to lase. Despite the unfruitful results, this experiment gave tremendous insight into some of the key problems of VCSEL design. Solving those problems led to performance improvements and eventually led to achieving CW lasing for *m*-plane GaN VCSELs, as described in Section 4.5.

4.3.1. VCSEL Design and Experimental Methods

This experiment was initially started in collaboration with J. Leonard before he graduated from UCSB. The main goal was to achieve CW operation by using longer cavity lengths (13λ and 23λ compared to previous 7λ VCSELs) to improve the thermal performance.

The design of experiment involved parallel processing of multiple samples to analyze the effects of cavity length (13λ and 23λ), active region designs with different numbers of QWs

(5, 7, and 10), number of mirror periods on the top-side n-DBR (10 and 12 period), and aperture design (ion implanted aperture (IIA) and buried tunnel junction (BTJ) aperture). While the previous highest-performing *m*-plane GaN VCSELs used a 7-period MQW because TMM simulations and modal gain calculations predicted the lowest threshold current density for a 7×MQW TJ VCSEL,[58] this experiment was the first to experimentally vary the number of QWs in full VCSEL structures. With significantly lower internal loss for TJ VCSELs compared to ITO VCSELs,[58] it may be possible to reach threshold with fewer mirror periods, which would increase the differential efficiency and peak output power. This motivated the plan to compare a 12-period n-DBR (as used in the previous 7λ VCSELs) versus a 10-period n-DBR. Figure 43 shows a schematic illustration of a VCSEL with an aperture formed by ion implantation and a VCSEL with a BTJ aperture.

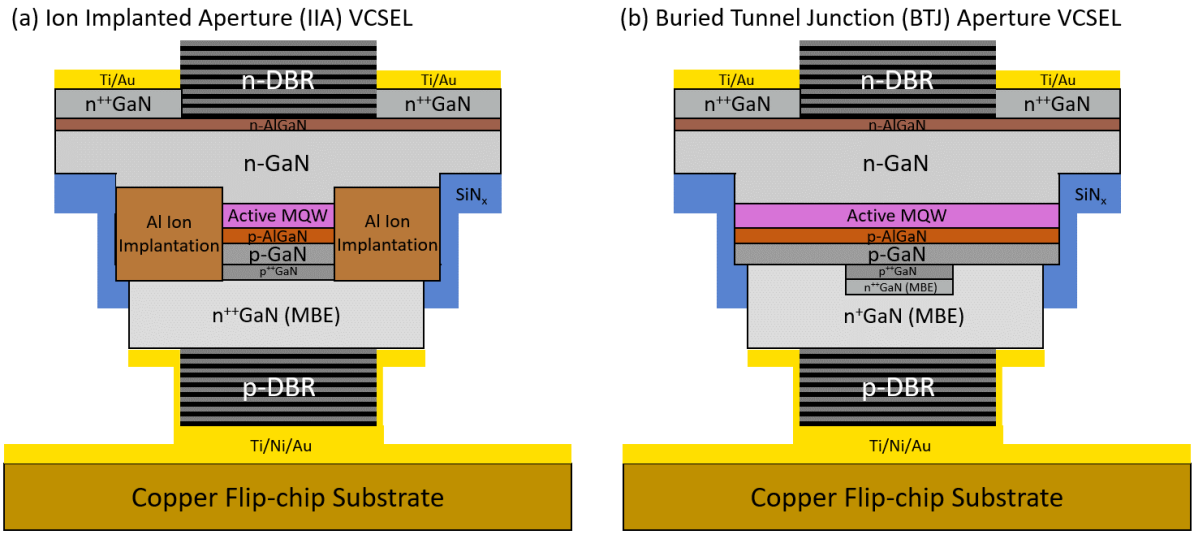


Figure 43. Schematic illustration of the (a) IIA VCSEL and (b) BTJ aperture VCSEL.

In order to increase the cavity length from 7λ (previous *m*-plane GaN VCSEL cavity length) to 13λ and 23λ, the MOCVD-grown n-GaN thickness was increased from ~763 nm to ~1005 nm and ~1733 nm, respectively. Additionally, the n^{++}GaN MBE regrowth for the TJ and current spreading layer on the p-side was increased from a total thickness of ~141 nm

(previous 7λ VCSEL) to ~775 nm for 13λ VCSELs and ~1642 nm for 23λ VCSELs. There were two reasons for increasing the MBE regrowth thickness. In addition to improved thermal performance, a thicker MBE regrowth was employed to also improve current spreading on the p-side of the devices. In these dual dielectric DBR VCSELs, current cannot be injected vertically through the electrically-insulating dielectric DBRs. Instead, current is injected laterally from the edges of the circular aperture. This can become a problem on the p-side of the device due to the high spreading resistance of p-GaN, which is why GaN VCSELs have used either an ITO or MBE-grown TJ and n-GaN current spreading layer on the p-side. Poor current spreading could explain some of the lasing behaviors of previous *m*-plane GaN VCSELs. For example, the near-field images of lasing in the PEC air-gap aperture VCSEL showed a higher order lateral optical mode with lasing near the edges of the aperture,[65] which could indicate a current spreading problem that prevented lasing at the center of the aperture. Poor current spreading could also explain why *m*-plane GaN ITO and TJ VCSELs exhibited filamentary lasing within the aperture, with a stochastic spatial distribution of lasing instead of well-defined LP modes.[58] Therefore, thicker MBE regrowths were chosen to help improve current spreading. However, as described in 4.4, there were some roughness problems due to the thicker MBE regrowth.

While effective electrical confinement has been reported using a BTJ in III-nitride micro-LEDs,[145,146] a BTJ has not yet been reported for III-nitride VCSELs. The BTJ aperture is a promising alternative to the ion implanted aperture because it can minimize optical absorption and has the potential to provide higher lateral confinement. This experiment was the first attempt to create a BTJ aperture GaN VCSEL, and Figure 44 shows a schematic representation of the fabrication steps involved in creating a BTJ aperture.

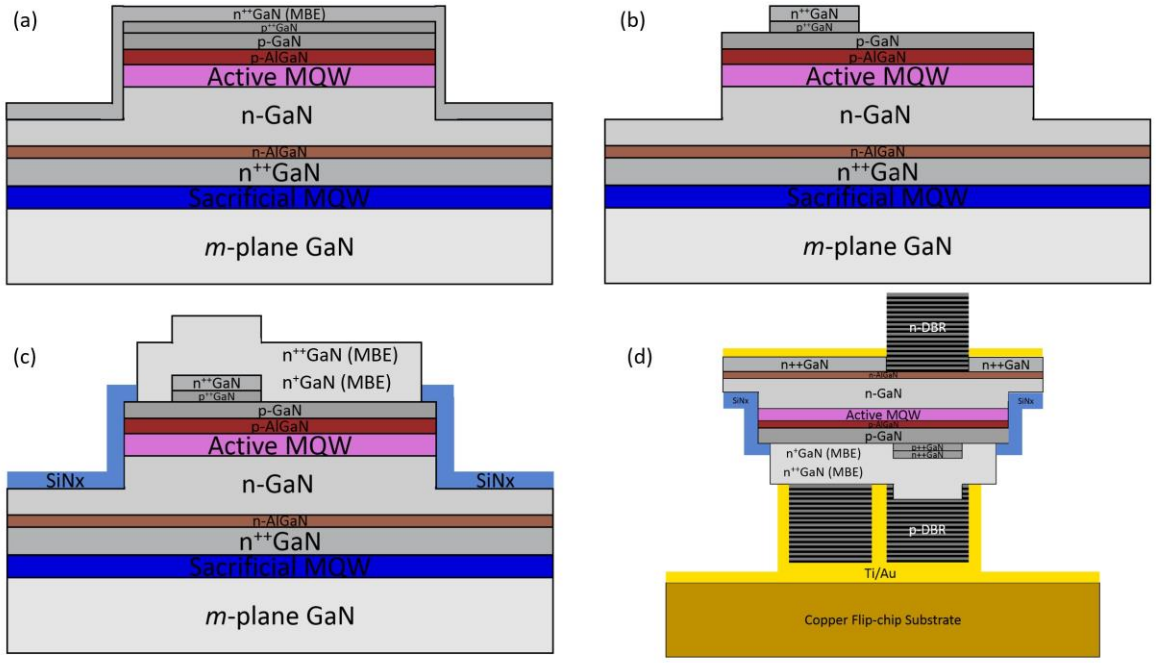


Figure 44. Schematic illustration of the growth and fabrication of a VCSEL with a BTJ aperture. (a) MOCVD growth is performed until the p^{++}GaN layer, a mesa is etched using RIE, and then MBE is used to grow n^{++}GaN to form the TJ. (b) RIE is used to etch the n^{++}GaN and p^{++}GaN everywhere outside the aperture. (c) MBE is used to grow an n^{+}GaN current spreading layer and an n^{++}GaN contact layer, RIE is used to etch regrown material off the sidewalls, and then SiN_x is deposited on the sidewall to protect the active MQW during a later step to remove the GaN substrate using PEC etching. (d) The remaining processing steps are equivalent to the previous IIA design, and this is the final BTJ aperture VCSEL structure.

The first steps to create BTJ aperture VCSELs are similar to previous IIA VCSELs: MOCVD is performed to grow the epitaxial structure up to a p^{++}GaN layer, and after the p-GaN activation anneal (600 °C for 15 minutes), a mesa is etched using RIE to expose the sidewall of the active MQW. IIA VCSELs would undergo ion implantation to form the current aperture at this stage, but the BTJ VCSEL process differs. Instead, MBE is used to grow an n^{++}GaN layer to form the TJ, as shown in Figure 44(a). Then, RIE is used to etch the n^{++}GaN and p^{++}GaN everywhere outside the aperture, as shown in Figure 44(b). At this stage, another MBE regrowth is performed to grow an n^{+}GaN current spreading layer followed by an n^{++}GaN contact layer, and then RIE is used to etch the regrown layers off the sidewalls of the mesa

before depositing SiN_x to protect the active MQW during a later PEC etching step to remove the GaN substrate, as shown in Figure 44(c). The next step is to deposit the p-side DBR and the remaining fabrication steps are equivalent to the IIA VCSEL process. A schematic of the final BTJ aperture VCSEL structure is shown in Figure 44(d).

The BTJ design is able to confine current to the aperture of the device due to a few reasons. One factor is due to p-GaN passivation during the RIE etch, as shown in Figure 44(b). During VCSEL processing, it is important to avoid exposing p-GaN surfaces to plasmas (e.g., RIE dry etching, sputtering, plasma ashing, etc.) because it can passivate the p-GaN. As-grown MOCVD-grown p-GaN is passivated with hydrogen but becomes p-type after an activation anneal. However, p-GaN is particularly sensitive to passivation via plasma damage. This effect has even been utilized as a current aperture scheme for GaN-based VCSELs, which used a CHF_3/Ar RIE plasma treatment for p-GaN surface passivation outside the aperture.[80] In the BTJ design, the RIE etch is performed into the p-GaN outside the aperture, which would cause p-GaN surface passivation and help confine current to the aperture. Furthermore, even without this p-GaN surface passivation effect, the BTJ design should still confine current to the aperture. This is because the RIE etch removes the p^{++}GaN and n^{++}GaN material outside the aperture, which confines current to the highly-doped p^{++}GaN/n^{++}GaN TJ. It is important to heavily dope the p^{++}GaN and n^{++}GaN TJ layers to decrease the depletion width and lower the barrier for current flow via tunneling. Outside the aperture, however, there is a much larger barrier to current flow because it consists of lower-doped p-GaN/n-GaN, which is essentially a lower-performing TJ that requires a much higher voltage for current to flow. Combining this effect with the RIE p-GaN surface passivation effect, current should be confined to the aperture in the BTJ VCSEL design.

While ion implantation and the BTJ design can both confine current to the aperture, the BTJ aperture offers several advantages. One problem with ion implantation is that it increases the absorption coefficient of GaN, which leads to higher internal loss due to optical absorption. For example, a GaN VCSEL created at Sony used boron ion implantation to form the current aperture, and ellipsometry revealed an absorption coefficient of 800 cm^{-1} at 453 nm for ion implanted GaN.[63] This would correspond to an absorption of 0.42% per round trip in the cavity if a photon traveled through the boron-implanted area.[63] While lasing mostly occurs within the aperture, there is some degree of lateral overlap with the implanted area which can contribute to internal loss. In comparison, the BTJ design avoids ion implantation altogether, which decreases the internal loss caused by optical absorption. Another advantage of the BTJ design is the ability to provide enhanced lateral optical confinement, which increases the confinement factor and reduces the threshold for lasing. Lateral optical confinement is obtained by increasing the refractive index in the center of the aperture compared to the outside, similar to an optical fiber with a higher-index core and lower-index cladding. Aluminum ion implantation only provides a small degree of lateral optical confinement because it reduces the index of refraction outside the aperture by ~2%.[3] The BTJ design can provide lateral optical confinement by utilizing n-AlGaN in the 2nd MBE regrowth for the n-GaN current spreading layer, as shown in Figure 44(c). The lower refractive index of AlGaN outside the GaN aperture would provide increased lateral optical confinement without the absorption loss of ion implantation.

Here, the BTJ aperture VCSELs used n-GaN in the 2nd MBE regrowth current spreading layer (without n-AlGaN) to serve as a proof-of-concept, and future devices could investigate the effect of AlGaN current spreading layers to improve VCSEL performance with

increased lateral optical confinement. Section 4.3.2 describes the details of VCSEL fabrication and results from this design of experiment.

4.3.2. VCSEL Fabrication and Results

MOCVD growth was performed on eight full *m*-plane GaN substrates. Six samples were designated to have ion implanted apertures and the remaining two were designated to have the new BTJ aperture design. For a total of six IIA VCSEL samples, there were two cavity length designs (13λ and 23λ) and three different types of active regions for each (5, 7, 10 QWs with 3 nm InGaN QWs and 1 nm GaN barriers). The BTJ samples consisted of two cavity length designs (13λ and 23λ) with 7 QWs. Table 1 summarizes the design for each sample, including cavity length, number of QWs, and the thicknesses of the epitaxial layers.

Table 1. Summary of the VCSEL design for each *m*-plane GaN sample, including the optical cavity length, number of QWs, and the thicknesses of the epitaxial layers (in nanometers). "SacMQW" refers to the sacrificial 3×MQW (5 nm QWs and 7 nm GaN barriers) that was selectively etched using PEC etching to remove the *m*-plane GaN substrate.

Label	a	b	c	d	e	f	g	h
Cavity Length	13λ	13λ	13λ	23λ	23λ	23λ	13λ	23λ
# of QWs	5	7	10	5	7	10	7	7
n++GaN	39.5971	39.5971	39.5971	39.5971	39.5971	39.5971	39.597	39.5971
n+GaN	695.304	695.304	695.304	1562.38	1562.38	1562.38	695.304	1562.38
n++GaN	39.5971	39.5971	39.5971	39.5971	39.5971	39.5971	39.597	39.5971
p++GaN	14	14	14	14	14	14	14	14
p-GaN	66	62.2	55.4	70	62.2	59.6	62.2	62.2
p-AlGaN	5	5	5	5	5	5	5	5
GaN Barrier	1	1	1	1	1	1	1	1
InGaN QW	3	3	3	3	3	3	3	3
GaN Barrier	1	1	1	1	1	1	1	1
n-GaN	1005.08	1005.08	994.272	1717.89	1717.03	1627.69	1005.08	1717.03
n-AlGaN	15	15	15	15	15	15	15	15
n++GaN	50	50	50	50	50	50	50	50
SacMQW	36	36	36	36	36	36	36	36

The etching time for the RIE *Mesa 1 Etch* (i.e., the etch to expose the sidewall of the active MQW so it could be coated it with SiN_x to protect during PEC etching) was 5 minutes and 25 seconds, which corresponds to an etch depth of ~650 nm (based on a RIE etch rate of 120 nm/min). The RIE *Intracavity Contact Etch* (i.e., the etch to remove the MBE-grown material from the sidewalls of the mesas) was performed for 6 minutes and 45 seconds (~810 nm etch depth) for samples a-c, 14 minutes (~1680 nm etch depth) for samples d-f, 6 minutes and 8 seconds (~736 nm etch depth) for sample g, and 13 minutes and 21 seconds (~1602 nm etch depth) for sample h. IBD was used to deposit ~250 nm of SiN_x to protect the active MQW sidewall, and the RIE *Mesa 2 Etch* (i.e., the etch to expose the sidewall of the sacrificial MQW for PEC etching) was conducted for 32 minutes for an estimated etch depth of ~3840 nm. The *Mesa 2* etch depth was likely less than this because SiN_x has an etch rate ~5× slower than GaN. Figure 45 shows the reflectance of the 16-period Ta_2O_5/SiO_2 p-DBR for a double-side polished (DSP) sapphire monitor that was coloaded during the IBD deposition of the p-DBR.

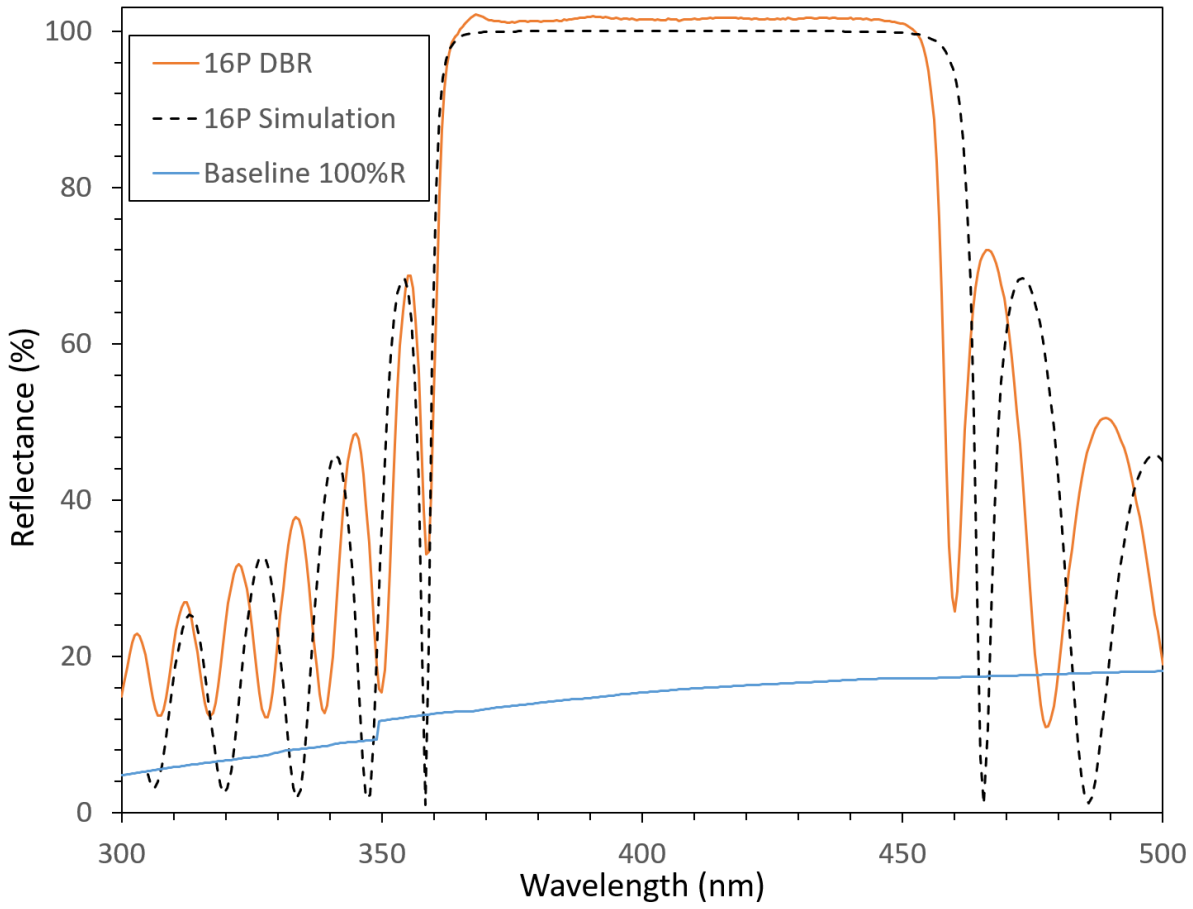


Figure 45. Reflectance of the 16-period Ta_2O_5/SiO_2 DBR on a DSP sapphire monitor that was coloaded during the IBD deposition of the p-DBR.

The peak of the DBR reflectance stopband was targeted for a wavelength of 405 nm. The dashed-black curve is a TMM simulation of a 16-period DBR and the orange curve is the measured reflectance of the 16-period DBR using a Cary 500 spectrophotometer. The blue curve is the reflectance measurement of a baseline mirror, which is assumed to have a reflectance of 100%. The vertical shift in reflectance of the baseline mirror at 350 nm is an artifact of the measurement that always occurs when the Cary 500 shifts from visible spectrum measurements to UV measurements below 350 nm. The measured reflectance of over 100% for the 16-period DBR is not physically true, but it means that it had a higher reflectance than the baseline mirror. Without a perfectly reflective baseline mirror, it is not possible to obtain

the true absolute reflectance value of these DBRs. However, these reflectance measurements are useful to make sure that the peak of the reflectance stopband is centered at the desired wavelength.

Yield became a significant issue after flip-chip bonding and removal of the *m*-plane GaN substrate by PEC etching of the sacrificial MQW. There were two problems that contributed to a low yield. First, only a few devices would transfer to the flip-chip substrate. Secondly, devices that transferred to the flip-chip substrate were covered with cracks, as shown in Figure 46(a).

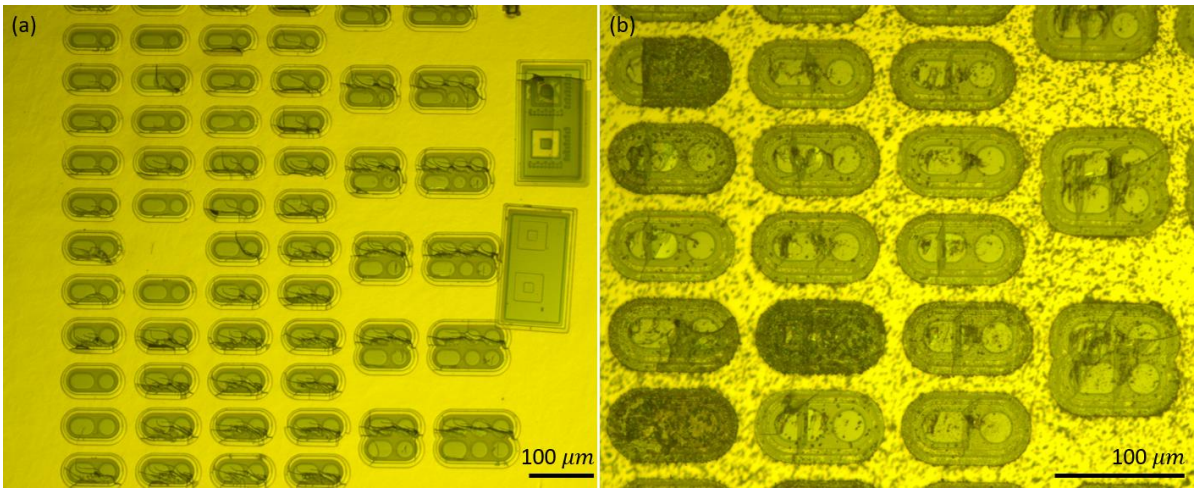


Figure 46. Optical microscope image after flip-chip bonding and PEC undercut etching to remove the *m*-plane GaN substrate.

Another problem was increased roughness on the n-side of the devices at this stage in the VCSEL process, as shown in Figure 46(b). More details about these issues with yield and roughness are described in Section 4.4.

After the PEC undercut etch, Ti/Au (10/500 nm) was sputtered to form the n-contact and a PEC top-down etch was performed using a Hg-Xe Arc Lamp with a 345 nm long-pass filter and 0.001 M KOH for three minutes. The surface morphology appeared very similar before and after the PEC top-down etch based on optical micrographs and AFM scans. The

surface was quite rough, as described further in Section 4.4. Before depositing the final n-DBR, the *L-I-V* and spectrum were measured under pulsed operation to measure the cavity resonance. A schematic of the VCSEL structure at this stage (prior to n-DBR deposition) is shown in Figure 47.

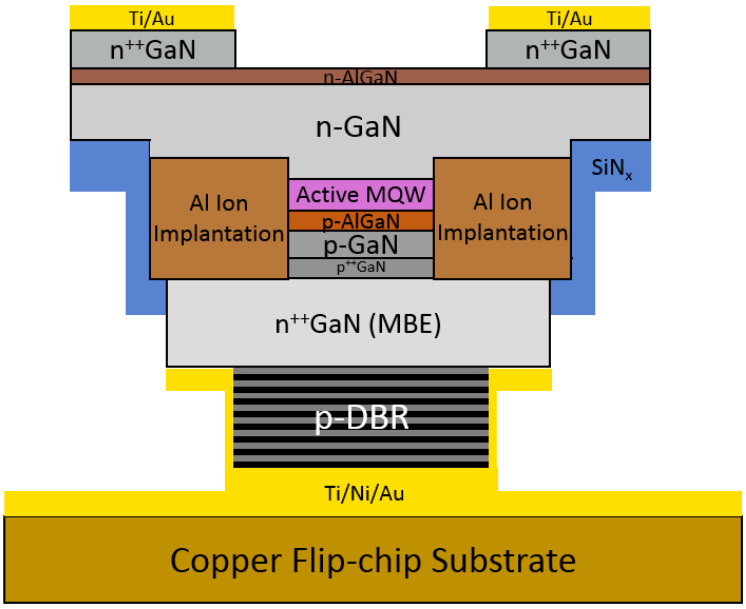


Figure 47. Schematic illustration of VCSELs prior to the n-DBR deposition. The *L-I-V* and spectrum were measured under pulsed operation to measure the cavity resonance. Although the top DBR is not present, there is still an optical cavity formed between the p-DBR on the bottom and GaN/air interface at the top. While lasing is not possible at this stage, the spectrum shows resonance wavelengths that have a spacing that is dependent on the optical thickness of the cavity. Measuring the spectra prior to the final DBR is important because it can reveal if the resonance wavelength(s) aligns with the peak gain wavelength and peak DBR reflectance wavelength. If the resonance wavelength(s) is not aligned, a Ta_2O_5 spacer can be deposited prior to the n-DBR to produce the desired resonance wavelength.

Even without the top n-DBR, there is an optical cavity formed between the p-DBR on the bottom and the GaN/air interface on the top. However, lasing will not occur because the reflectance of the GaN/air interface is much lower than the required reflectance of ~99.9%. Instead, there are peaks and nulls in the spontaneous emission spectrum due to resonance wavelength(s) within the optical cavity. Measuring the spectrum can provide an estimate of the optical cavity thickness because it is inversely proportional to the spacing between resonance wavelengths, as described by Equation (12). The most important reason for

measuring the spectral emission at this stage in the VCSEL process is to make sure that the resonance wavelength(s) aligns with the peak gain wavelength and falls within the DBR reflectance stopband. If the resonance wavelength is misaligned, a Ta_2O_5 spacer can be deposited prior to the n-DBR to adjust the resonance wavelength for better alignment. Ta_2O_5 is chosen as the spacer material instead of SiO_2 because the index of refraction for Ta_2O_5 (~2.22 at 405 nm) is the closer to GaN (~2.557 at 405 nm), so a Ta_2O_5 spacer effectively increases the optical cavity length and redshifts the longitudinal resonance wavelengths. The thickness of the Ta_2O_5 spacer can be determined by using Vertical (TMM simulation software) to simulate the reflectance of the structure and by varying the Ta_2O_5 spacer thickness until the desired resonance wavelength is obtained.

The spectrum under pulsed operation prior to the topside n-DBR is shown in Figure 48(a) for a VCSEL with a 13λ cavity length and Figure 48(b) for a VCSEL with a 23λ cavity length.

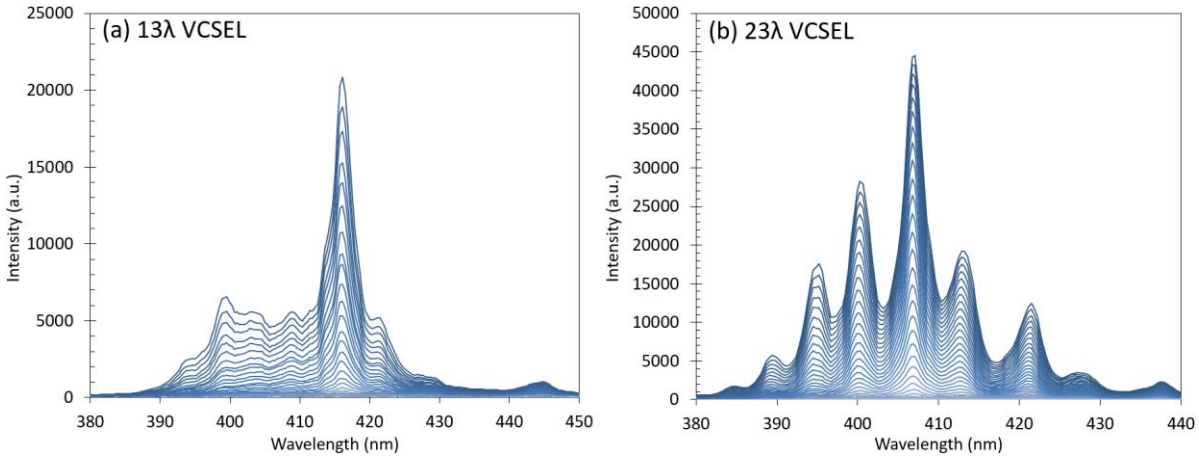


Figure 48. Spectrum under pulsed operation prior to the topside n-DBR for a VCSEL with an optical cavity length of (a) 13λ and (b) 23λ. Each colored curve corresponds to the spectrum measured at a different current injection level.

The 23λ VCSEL has a greater number of resonance peaks in the spectrum measurement because the longer cavity length reduces the spacing between longitudinal resonances, so

more resonance wavelengths overlap with the spontaneous emission spectrum. While the 23λ VCSEL had six resonance wavelengths at 389 nm, 395 nm, 401 nm, 408 nm, and 421 nm, the 13λ VCSEL had two resonance wavelengths at 399 nm and 416 nm. With many resonance wavelengths for the 23λ VCSEL, it is much easier to align the peak gain spectrum with a resonance wavelength, so a Ta_2O_5 spacer before the n-DBR is not necessary. On the contrary, the 13λ VCSEL had resonance wavelengths at 399 nm and 416 nm, which are offset from the peak spontaneous emission wavelength ~405 nm. By increasing the cavity length using a Ta_2O_5 spacer, the resonance wavelengths can be shifted so that a longitudinal lasing mode occurs at 405 nm. The *L-I-V* characteristics were also measured prior to the n-DBR deposition, and Figure 49 shows the *L-I-V* characteristics under pulsed operation for a 23λ VCSEL with a 10 μm aperture diameter.

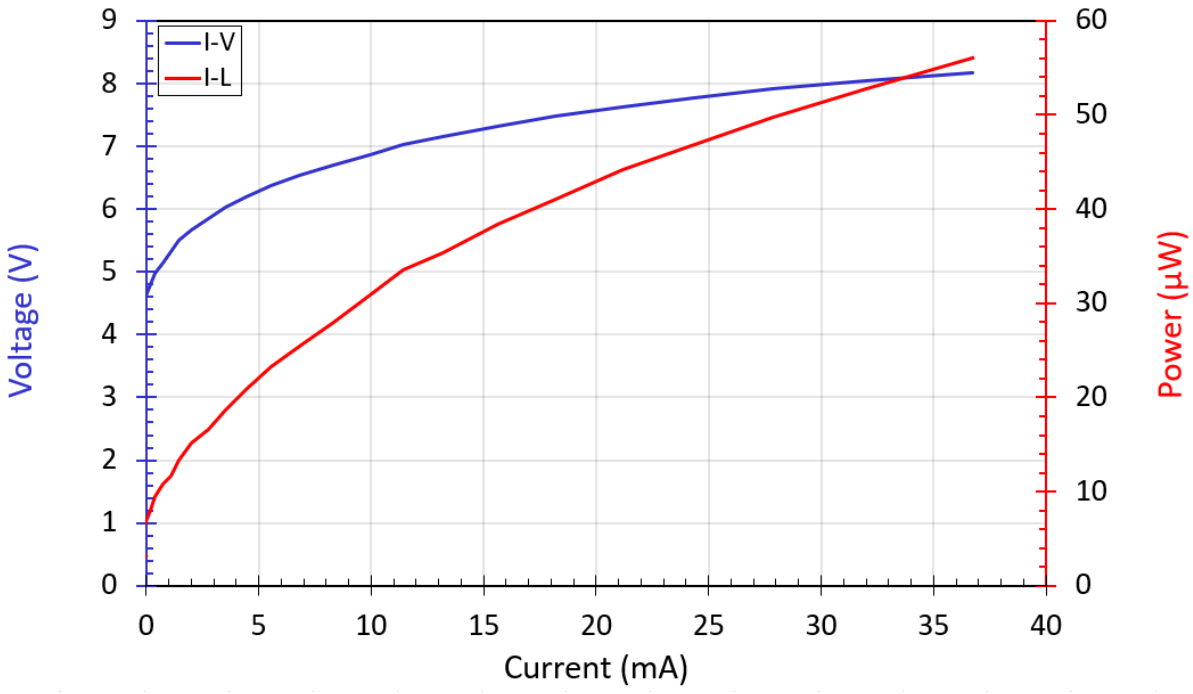


Figure 49. *L-I-V* characteristics under pulsed operation prior to the n-DBR deposition for a 23λ VCSEL with a 10 μm aperture diameter.

The *L-I-V* and spectrum measurements were both measured under pulsed operation with a duty cycle of 0.5% with a pulse width of 500 ns.

After electrooptical characterization, a 10-period Ta_2O_5/SiO_2 n-DBR was deposited using IBD. Figure 50 shows the reflectance of the 10-period n-DBR on a DSP sapphire substrate that was coloaded during IBD deposition.

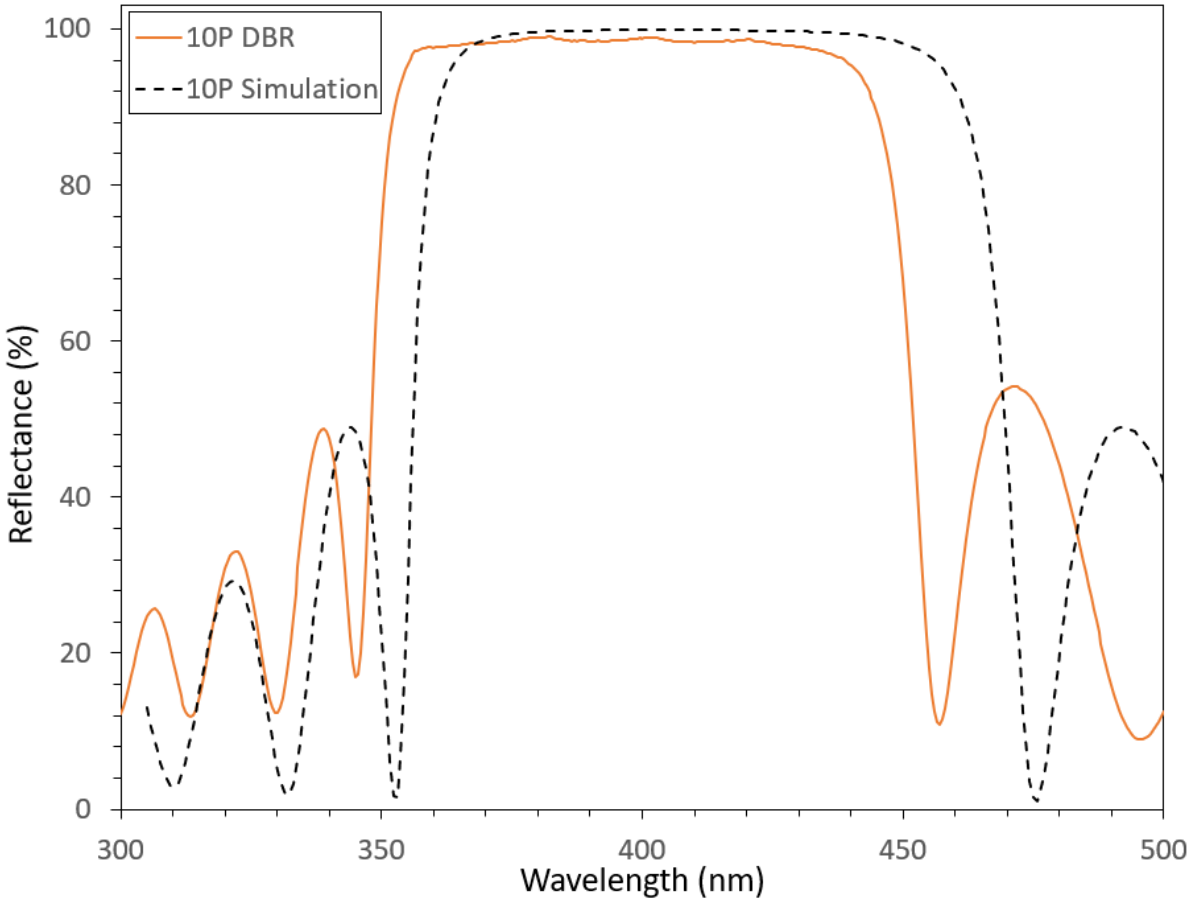


Figure 50. Reflectance of the 10-period Ta_2O_5/SiO_2 DBR on a DSP sapphire monitor that was coloaded during the IBD deposition of the n-DBR for 13λ and 23λ cavity length VCSELs.

Compared to the 16-period p-DBR, the 10-period n-DBR had a lower absolute reflectance (~98%) and did not match the reflectance simulation curve as well. It should be noted that the absolute reflectance values highly depend on the baseline mirror and even the exact location that was measured on the baseline mirror (i.e., the reflectance is not completely uniform across the baseline mirror). Due to the fewer mirror periods, the 10-period DBR had a lower

reflectance stopband width of 86 nm at 95% reflectance compared to the 16-period DBR that had a stopband width 93 nm. By comparing the center of the reflectance stopbands, the 10-period DBR reflectance stopband was blueshifted by approximately 13 nm compared to the simulation, which indicated that the Ta_2O_5 and SiO_2 layers were thinner than the targeted quarter-wave optical thickness for a wavelength of 405 nm. This was caused by problems with the IBD deposition rate calibration method and is further described in Section 4.4.2. Low DBR mirror reflectance can be a significant issue for VCSELs due to the relatively short gain path length that requires DBR mirror reflectance values over 99% to reach the threshold for lasing.

After depositing the final 10-period n-DBR, the VCSELs were tested under pulsed operation to measure the *L-I-V* and emission spectrum. Figure 51 shows the *L-I-V* characteristics for a 23λ VCSEL with a 10 μm aperture diameter.

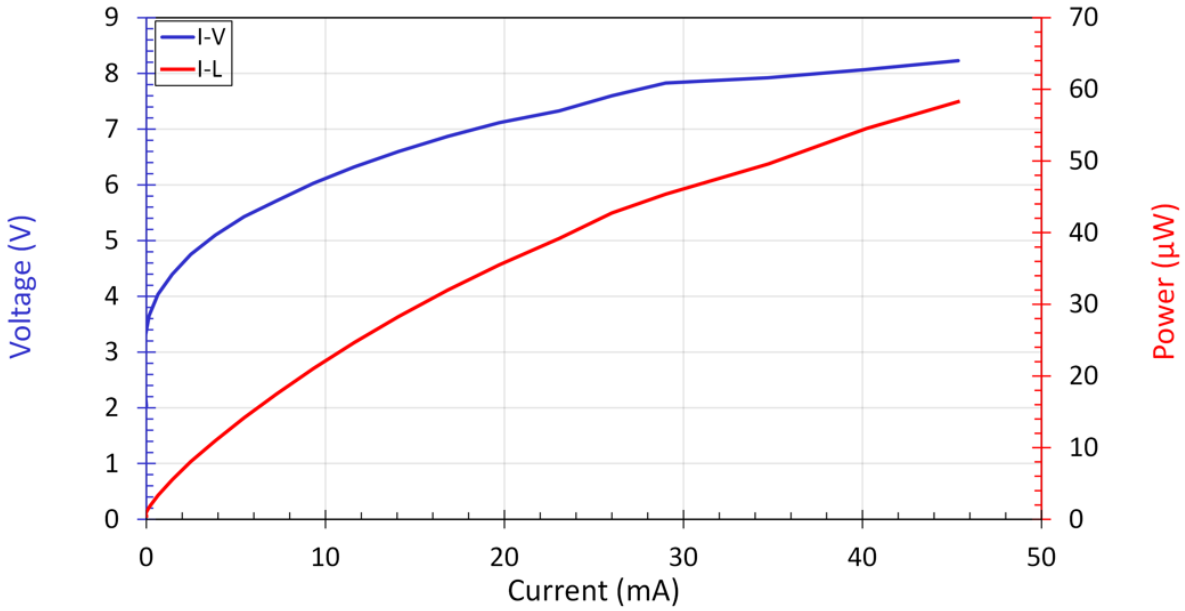


Figure 51. *L-I-V* characteristics under pulsed operation for a 23λ VCSEL with a 10 μm aperture diameter.

Lasing was not observed, and the *L-I-V* curves were very similar to the measurement prior to the n-DBR. The slope of the *I-L* curve gradually decreased at higher injection levels, which is not characteristic for a laser diode. Above the threshold current, a laser would have a

characteristic kink in the *I-L* curve where the slope significantly increases and becomes linear with respect to current. This kink in the *I-L* curve was not observed, which indicates that the threshold for lasing was not reached. Each of the samples have multiple VCSELs with aperture diameters varying from 4 μm to 20 μm, but none of the VCSELs were able to lase based on the *L-I-V* measurements. Another way to determine whether the VCSELs were able to lase is to measure the spectrum. Figure 52(a) shows the emission spectrum of a 23λ VCSEL with a 10 μm aperture diameter before the n-DBR deposition, and Figure 52(b) shows the spectrum for the completed VCSEL after deposition of the 10-period n-DBR.

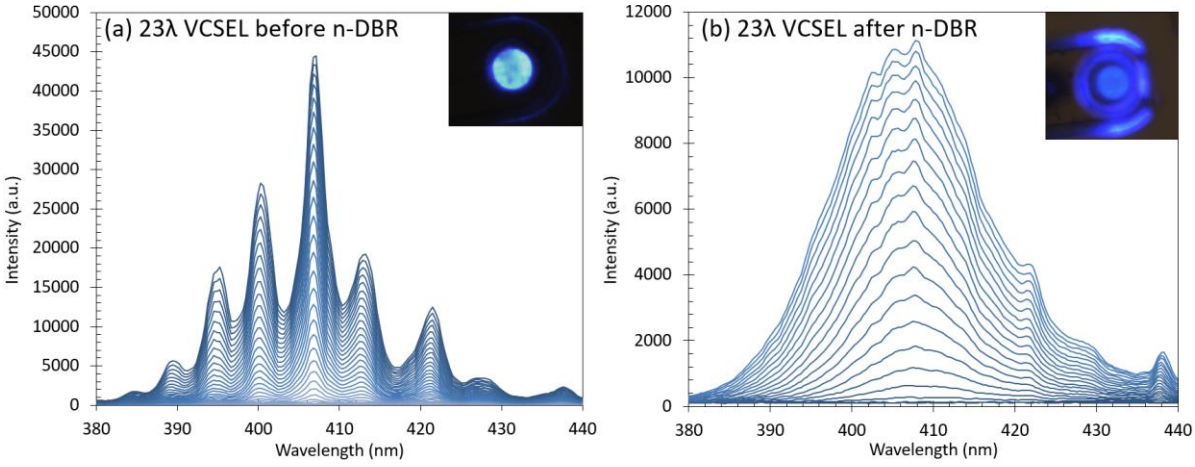


Figure 52. Emission spectrum under pulsed operation for a 23λ VCSEL with a 10 μm aperture diameter (a) prior to the n-DBR deposition and (b) the completed VCSEL after the 10-period n-DBR deposition. Lasing was not observed. The insets show near-field optical microscope images during operation.

Lasing was not observed based on the emission spectrum. Above the threshold for lasing, the spectral width of emission should significantly decrease to a FWHM less than 2 nm (the FWHM of a VCSEL would be even narrower, but the spectrometer resolution is limited to ~2 nm). However, the FWHM of the spectrum after the n-DBR was ~ 20 nm, so lasing was not observed. None of the samples exhibited lasing based on the emission spectrum. Another way to verify whether lasing is present is to observe the near-field emission profile during operation. The insets of Figure 52 show near-field optical microscope images during

electroluminescence. These images furthermore indicated that none of the VCSELs were able to lase. Above the threshold for lasing, a significantly brighter spot would appear within the aperture. However, there was no indication of lasing within the aperture, as shown in the Figure 52(b) inset.

This meant that the VCSELs were essentially micro-cavity LEDs, which have a spontaneous emission spectrum overlain with resonance wavelengths due to interference, as shown by the peaks in emission intensity in Figure 52(a). Interestingly, the resonance wavelengths are not observed in the spectrum after the n-DBR, as shown in Figure 52(b). This was initially unexpected because the top-side n-DBR mirror should have increased the quality factor of the optical cavity, which would have caused further spectral narrowing at resonance wavelengths (i.e., enhanced constructive and destructive interference effects due to the higher reflectance mirrors of the optical cavity compared to devices with only a single DBR). The absence of resonance wavelengths in the spectrum after the top-side DBR deposition can be explained by spontaneous emission that scatters from areas of the device outside the DBR. As shown in the Figure 52(b) inset, the brightest emission does not come from the circular VCSEL aperture. Instead, emission is brighter in areas outside the circular DBR near the edges of the device. This makes sense because only a small fraction of light can transmit through the high-reflectance n-DBR, so emission that scatters outside the DBR is relatively bright. When aligning the fiber optic for the spectrum measurement, it was aligned to the peak intensity. That means the spectrum was likely collected for light that escapes near the edges of the device instead of light within the optical cavity, which explains why resonance wavelength peaks were not observed in the spectrum. On the other hand, resonance wavelengths were observed for the devices without the top-side DBR because the brightest

emission comes from the circular aperture, as shown in the Figure 52(a) inset, so the spectrum measurement was for light that escaped from the optical cavity. This is because the GaN/air interface is significantly less reflective than the case with a top-side DBR, so more light escapes from the optical cavity compared to light that scatters from the edges of the device. The amount of scattered light that emits from the edges of the device should be similar with and without the n-DBR, but it appears brighter in the Figure 52(b) inset because the optical microscope camera exposure time was increased to account for the lower light intensity, as a result of the n-DBR. The resonance wavelengths could likely be observed in the spectrum for the VCSEL after the n-DBR if the fiber optic was aligned to collect light that passed through the n-DBR, but the integration time would need to be increased due to the relatively low light intensity.

Based on the *I-L* curves, emission spectra, and near-field optical images, none of the VCSELs were able to lase, even under pulsed operation. While this was initially a discouraging result, failure analysis of these devices revealed tremendous insight into key problems of these devices. This led to several experiments to solve these problems and improve the VCSEL design. Section 4.4 describes the failure analysis, experiments, and design improvements that eventually led to the first demonstration of CW lasing for *m*-plane GaN VCSELs.

4.4. VCSEL Failure Analysis and Design Improvements

While the goal of the previous experiment was to increase the VCSEL cavity length to 13λ and 23λ to improve the thermal performance and achieve CW lasing, all of the devices

failed. None of the VCSELs could lase, even under pulsed operation. These devices were essentially micro-cavity LEDs instead of VCSELs. Another major problem was extremely low yield during VCSEL fabrication: only a small percentage of devices would transfer onto the flip-chip substrate, and among the few devices that did transfer, nearly all of them were cracked. The next step was to perform failure analysis on these devices to figure out why the VCSELs did not lase under pulsed operation, how to improve VCSEL yield, and eventually figure out how to achieve the ultimate goal of CW lasing.

The following sections describe the failure analysis and experiments that led to several VCSEL design improvements and eventually to the first demonstration of CW lasing for *m*-plane GaN VCSELs. The first priority was to identify the main problem that prevented lasing. This was challenging because the VCSEL fabrication process involves hundreds of steps, so it can be difficult to pinpoint which ones caused problems. For comparison, the VCSEL process contains seven photolithography steps while LEDs typically have only three photolithography steps. One potential problem that could have prevented the devices from lasing was if there was an issue during MOCVD growth. As discussed in Section 4.4.1, this was not likely the case, but there were problems with the standard growth recipe that led to a series of MOCVD growth experiments. Next, the DBR mirrors were investigated because low mirror reflectance could have prevented the devices from lasing. Furthermore, fewer mirror periods were deposited for the n-DBR (10-period) compared to previous VCSELs (12-period), and the measured reflectance was lower than expected with a blueshifted stopband compared to the simulated reflectance. Section 4.4.2 describes the investigation into the DBRs, which led to an improved DBR deposition method. As discussed in 4.4.3, the most significant problem that prevented lasing turned out to be scattering loss due to rough surfaces on both

the n-side and p-side prior to DBR mirror deposition. Section 4.4.5 describes the PEC etching experiments that were conducted to reduce roughness on the n-side, and Section 4.4.4 describes MBE TJ regrowth experiments to improve the morphology on the p-side of the devices. To improve VCSEL yield, a series of Au-Au flip-chip bonding experiments were conducted, as described in Section 4.4.6. The most significant improvement in VCSEL yield and thermal performance was switching from Au-Au thermocompression bonding to Au-In solid liquid interdiffusion (SLID) bonding, as described in Section 4.4.6.2. This led to the first demonstration of CW operation for *m*-plane GaN VCSELs, which are described in Section 4.5.

4.4.1. MOCVD Growth Experiments

Based on the electroluminescence (EL) measurements after MOCVD growth, there was not likely an issue with MOCVD growth that prevented lasing for the 13λ and 23λ VCSELs. However, there were problems with the standard VCSEL growth recipe that led to a series of MOCVD experiments to improve the epitaxial design.

The previous highest-performing nonpolar GaN TJ VCSEL design used an active region consisting of a 7×MQW with 3 nm InGaN QWs and 1 nm GaN barriers;[58] however, MOCVD growth of that design often showed poor performance in terms of electroluminescence (EL) output power for LED test samples. These were measured using the quick-test method, which involves MOCVD growth, p-GaN activation at 600 °C for 15 minutes, pressing indium through a shadow mask to create circular p-contacts, soldering indium on the backside of the GaN substrate for n-contact, and performing EL measurements (i.e., measuring the *L-I-V* characteristics under CW operation). This method was used to check the quality of MOCVD-grown layers prior to proceeding with VCSEL fabrication. In

general, the EL measurements should show an output power of ~3 mW at 20 mA, voltage of ~4.5 V, wavelength of ~405 nm, and a full width at half maximum (FWHM) of ~15 nm. However, the standard MOCVD recipe with a 7×MQW active region was found to often produce samples with very low output powers, sometimes even below 0.1 mW at a current of 20 mA. VCSEL fabrication is a particularly lengthy process, so it is important to have high-quality MOCVD-grown material prior to starting fabrication. Therefore, this was a significant problem that needed to be solved in order to proceed with VCSEL fabrication and experiments.

This led to a series of MOCVD growth experiments to improve the EL characteristics. One possible explanation for the low EL output power was poor injection efficiency due to the large number of GaN barriers in the 7×MQW. If carriers only occupy some of the QWs, the unoccupied QWs would be optically absorbing and could decrease the output power. This could be solved using active regions with fewer QWs (and fewer GaN barriers). A large number of GaN barriers in the MQW can also be problematic for VCSELs because it can lead to a lower gain enhancement factor. Confinement factor is maximized by aligning the peak of the optical mode with the InGaN QWs, but the GaN barriers do not contribute to the enhancement factor. By replacing passive GaN barriers with active InGaN, the gain enhancement factor can be increased in certain designs (note that this is not always the case, particularly for GaN barriers located farther away from the center of the active region). This motivated carrying out a series of MOCVD growth experiments of active regions that have fewer GaN barriers and thicker QWs. Increasing the QW thickness was further motivated by reports that higher output powers were achieved using thicker QW active regions for m-plane GaN LEDs.[165] While *c*-plane devices are limited to QW thicknesses ~4 nm due to the QCSE,

m-plane GaN LEDs with ITO p-contacts had maximum output powers with QW widths of 8-10 nm and worked well for QW widths up to 20 nm.[165] Increasing the total active region thickness can also be beneficial for VCSELs because it increases the fill factor component of the confinement factor, as described by Equation (15). However, this benefit may be negated because the density of states is inversely proportional to the QW width.[17]

A series of MOCVD growth experiments were performed to investigate the EL characteristics for various active region designs on *m*-plane GaN. In addition to a sample grown using the standard VCSEL recipe with a 7×MQW (3 nm QWs and 1 nm barriers), samples were grown with active regions consisting of a 3×MQW (9 nm QWs and 1 nm barriers), a 2×MQW (14 nm QWs and 1 nm barriers), and a single 20 nm QW. The epitaxial structure was similar to the 7λ TJ VCSEL design reported earlier,[58] but the sacrificial MQW was not included in the recipe. After thermal annealing for p-GaN activation, indium contacts were used for EL measurements. The light output power versus wavelength at a current of 20 mA is shown in Figure 53.

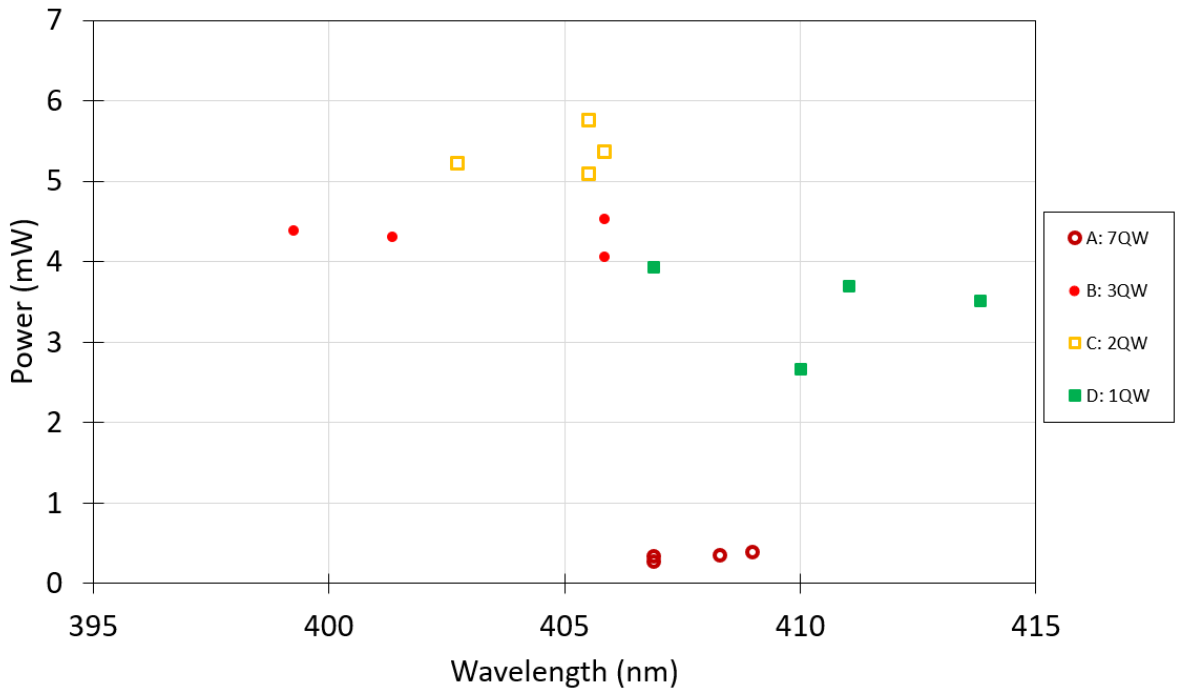


Figure 53. Light output power versus wavelength at a current of 20 mA for *m*-plane LED samples with various active regions consisting of a single QW, double QW, triple QW, and 7×MQW. Sample A had the standard VCSEL growth recipe with a 7×MQW (3 nm QWs and 1 nm barriers),[58] and Sample B had a 3×MQW (9 nm QWs and 1 nm barriers). Sample C had a 2×MQW (14 nm QWs and 1 nm barriers), and Sample D had a single 20 nm QW.

The standard VCSEL recipe with the 7×MQW had the lowest output power ~0.3 mW at 20 mA while each of the other samples reached peak powers of 4 mW and higher. The FWHM was ~16 nm for each of the samples except for the single QW sample, which had a FWHM of ~21 nm. The 2×MQW sample had the highest peak output power of ~5.8 mW. To see if these results were reproducible, this experiment was repeated for samples with 7×MQW and 2×MQW active regions. The output power versus wavelength for these samples is shown in Figure 54.

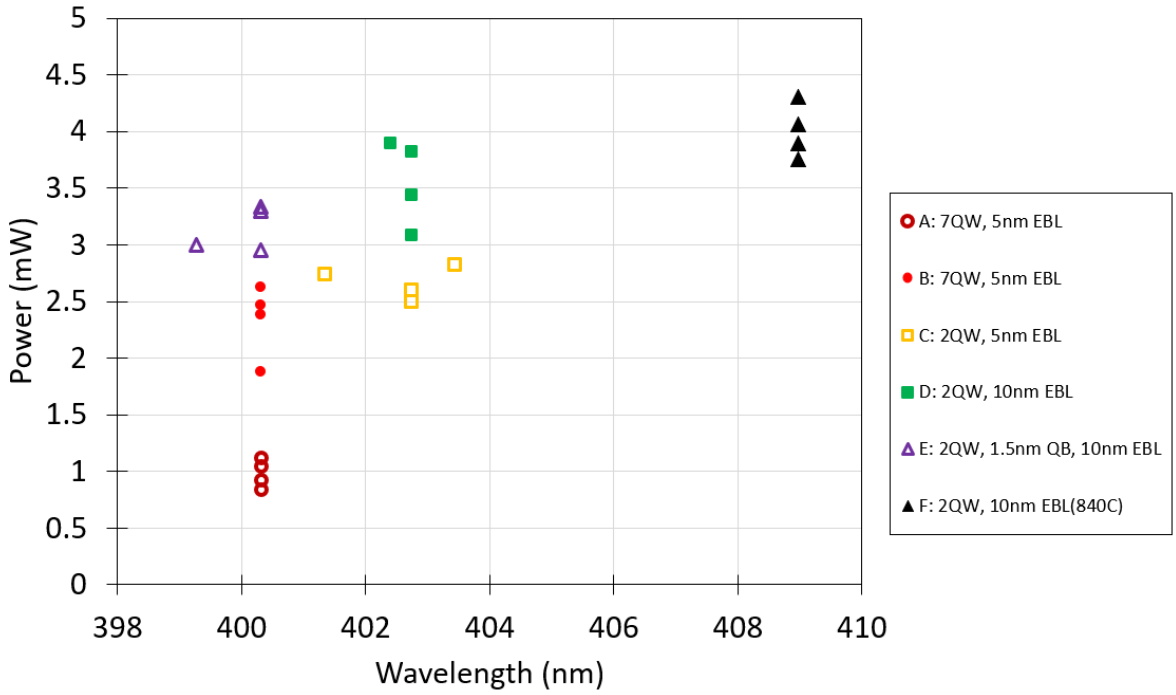


Figure 54. Light output power versus wavelength at a current of 20 mA for *m*-plane LED samples with various active regions showing relatively higher output powers for 2×MQW active regions compared to 7×MQW. Sample A and B had the standard VCSEL growth recipe with a 7×MQW (3 nm QWs and 1 nm barriers) and 5 nm EBL.[58] Samples C and D had a 2×MQW active region (14 nm QWs and 1 nm barriers) with a 5 nm and 10 nm EBL, respectively. Sample E had a 2×MQW active region (14 nm QWs and 1.5 nm barriers) with a 10 nm EBL. Sample F was identical to Sample D except the active region was grown at 840 °C instead of 850 °C like the other samples.

The results were similar to the previous experiment as the 7×MQW samples had the lowest output power (Samples A and B). There appeared to be variation in growth quality because Sample A and B were grown consecutively with identical growth recipes but had varying output powers of ~1 mW and ~2.5 mW, respectively. These samples also had the highest FWHM values of 14.2 and 15.6 nm, respectively. Each of the 2×MQW samples had peak output powers over 2.5 mW, and there was a marginal improvement for samples that had a 10 nm p-AlGaN EBL instead of the standard 5 nm thickness. A slight improvement in peak output power was also shown by increasing the GaN barrier thickness from 1 to 1.5 nm, as shown by Sample E. Similar to Sample D, Sample F had a 10 nm EBL, but its active region was grown at 840 °C instead of 850 °C, which resulted in a redshifted peak wavelength of ~

409 nm. The 2×MQW samples (Samples A-F) had approximate FWHM values of 13.8 nm, 13.2 nm, 11.5 nm, and 12.8 nm, respectively, which suggest that it is beneficial to increase the GaN barrier and EBL thicknesses.

Additional MOCVD experiments were conducted and the 2×MQW active region consistently had higher EL output power after performing over 40 growths. While ~50% 7×MQW samples had peak output powers below 1 mW, ~85% of the 2×MQW samples had powers over 3 mW. Although these tests do not necessarily indicate better VCSEL performance, using the 2×MQW active region significantly increased the probability that the quality of the MOCVD growth was sufficient (based on the EL characteristic) to move forward with VCSEL processing for the sample. As further discussed in Section 4.5.1, 7×MQW and 2×MQW active regions were grown to compare the performance of fully-processed VCSELs.

Although not employed in fully-processed VCSELs, additional MOCVD growths were performed to investigate the inconsistent EL performance of the 7×MQW active region. Other than injection efficiency, another possible explanation for low EL output power could be due to the high Mg concentration in the p-AlGaN EBL, which could result in Mg diffusion into the MQW and lower radiative efficiency because Mg acts as a source of nonradiative recombination. This was tested by growing samples with 7×MQW (3 nm QWs and 1 nm barriers) active regions with and without a p-AlGaN EBL. The output power versus wavelength for these samples is shown in Figure 55.

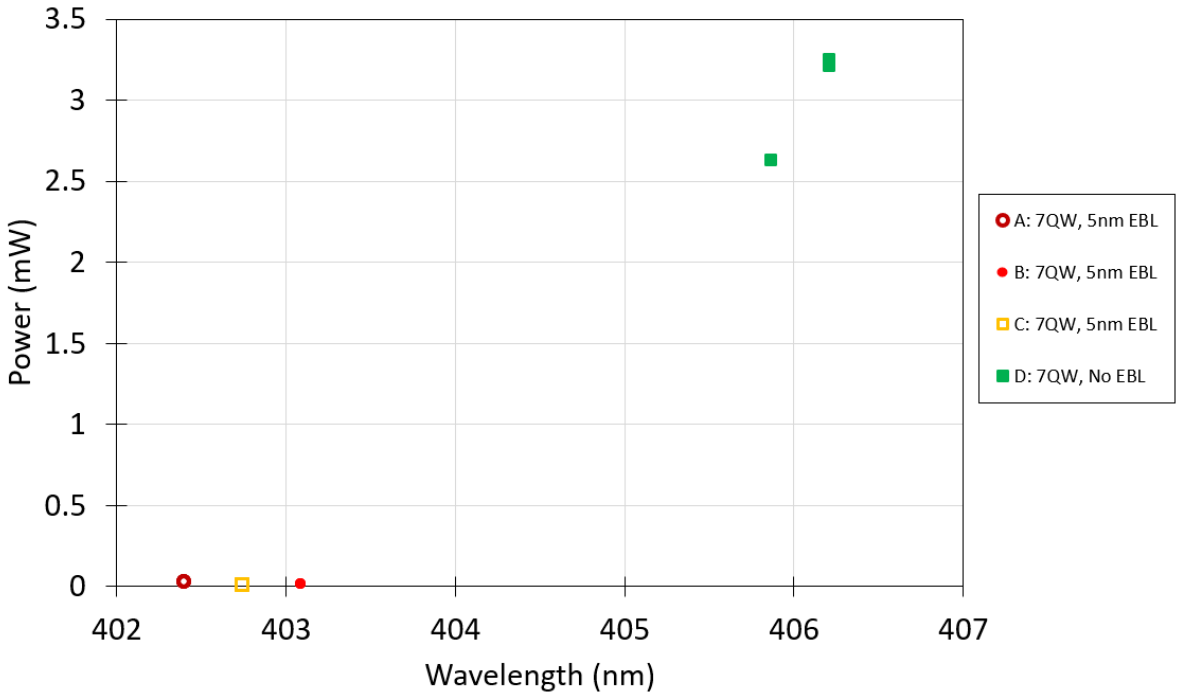


Figure 55. Light output power versus wavelength at a current of 20 mA for *m*-plane LED samples with and without a 5 nm p-AlGaN EBL. Sample A, B, and C each had the standard VCSEL growth recipe with a 7×MQW (3 nm QWs and 1 nm barriers) and 5 nm EBL.[58] Sample D had the same structure except the p-AlGaN EBL was removed from the growth recipe. Samples with an EBL (A, B, and C) each had a very low EL output power, but Sample D without an EBL reached a peak power over 3 mW at a current of 20 mA.

Samples A, B, and C were grown with the standard MOCVD recipe (7×MQW with 5 nm EBL) and they each had a very low output power ~0.01 mW. Although Sample A was grown the day before, Samples B, C, and D were grown directly after one another. Sample D had an identical growth recipe as the others except the EBL was removed, and it reached a peak output power over 3 mW. Therefore, the EBL may play a large role in the quality of the MOCVD growth, but further experimentation would be necessary to confirm. For example, secondary-ion mass spectrometry (SIMS) could be used to investigate whether the low EL output power was due to Mg diffusion into the MQW. This effect could potentially be reduced by decreasing the bis(cyclopentadienyl)magnesium (Cp_2Mg) flow during MOCVD growth to reduce the Mg doping or using higher MOCVD growth temperatures to lower the Al composition, which would also reduce the Mg doping. Another possible solution could be to

increase the GaN barrier thickness between the MQW and p-AlGaN EBL to reduce Mg diffusion into the active region.

4.4.2. DBR Mirror Improvements

After none of the VCSELs from the previous experiment could lase, the DBR mirrors were investigated as a possible reason because low mirror reflectance could have prevented the devices from lasing. Fewer mirror periods were deposited for the n-DBR with 10-periods of Ta_2O_5/SiO_2 compared to previous *m*-plane GaN VCSELs that had 12-periods, and the measured reflectance of the 10-period DBR was lower than expected with a blueshifted stopband compared to the simulated reflectance. Although the DBR reflectance stopband appears flat, there is actually curvature with a peak reflectance at the center. Therefore, it can be important to align the DBR reflectance stopband so that the peak reflectance is aligned to the lasing wavelength. The spectral position of the DBR reflectance stopband depends on the optical thicknesses of the Ta_2O_5 and SiO_2 layers, so this requires a series of calibrations to obtain the precise IBD deposition times for each layer. However, the unexpected reflectance spectra of the 10-period DBR indicated that there could be a problem with the IBD calibration method, which motivated an investigation to identify problems and try to improve the method.

The purpose of the IBD calibration procedure is to obtain precise IBD deposition times to accurately deposit quarter-wavelength layers of SiO_2 and Ta_2O_5 for the DBRs. This first involves depositing ~67 nm of SiO_2 onto a silicon wafer and ~46 nm of Ta_2O_5 onto a separate silicon wafer. Then, ellipsometry is used to measure the thickness and refractive index of each layer. The IBD deposition rate is obtained by dividing the measured layer thicknesses by their respective deposition times, and the measured refractive indices were used to calculate the correct thickness for a quarter-wavelength layer, $T^*_{\lambda/4}$, as described by

$$T^*_{\lambda/4} = \frac{\lambda}{4n} \tag{22}$$

where λ is the wavelength (405 nm in this case) and *n* is the refractive index for each material (at $\lambda = 405$ nm, n_{SiO_2}~1.51 and $n_{Ta_2O_5}$~2.22). This corresponds to SiO_2 and Ta_2O_5 quarter-wavelength layer thicknesses of $T^*_{\lambda/4,SiO_2}$~67.05 nm and $T^*_{\lambda/4,Ta_2O_5}$~45.61 nm, respectively. While the thickness and refractive index measurements from ellipsometry give the approximate deposition time to deposit quarter-wavelength layers, further calibration is required. The next step in the IBD calibration process involves depositing dielectric Fabry-Perot cavities onto silicon wafers, as illustrated in Figure 56.

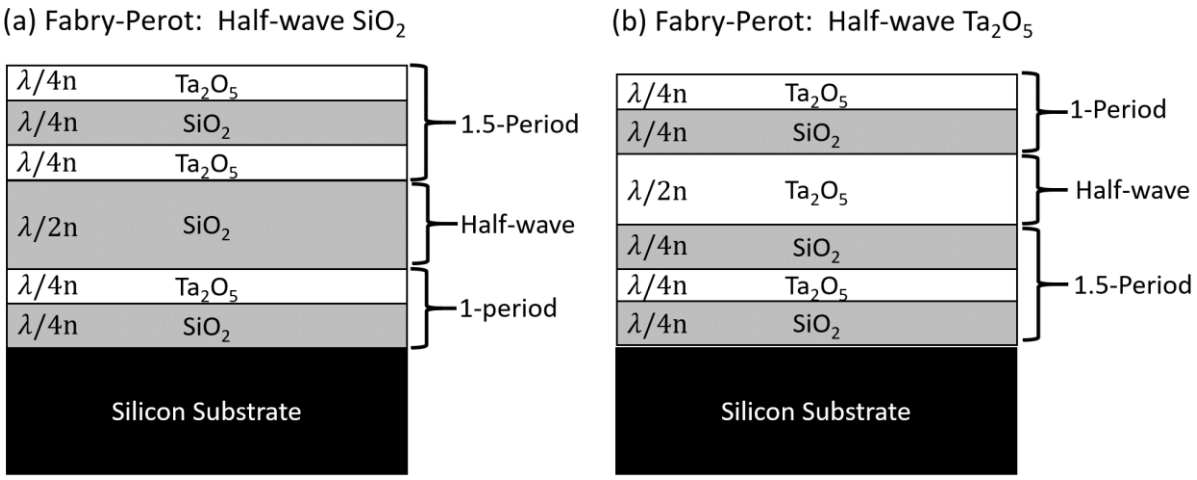


Figure 56. Schematic illustration of Fabry-Perot cavities that are deposited onto silicon wafers during the IBD calibration process for obtaining precise deposition times to deposit quarter-wavelength-thick SiO_2 and Ta_2O_5 for VCSEL DBRs. The Fabry-Perot cavities consist of two parallel reflectors with SiO_2/Ta_2O_5 quarter-wavelength-thick layers and a half-wavelength layer in between that is composed of (a) SiO_2 and (b) Ta_2O_5. If each of the layer thicknesses are correct, there should be a reflectance null at the targeted wavelength. In the IBD calibration method, the SiO_2 and Ta_2O_5 deposition times are adjusted based on the reflectance nulls of these Fabry-Perot cavities until each structure has a reflectance null at the targeted wavelength.

The Fabry-Perot cavities have two parallel reflectors that consist of 1-period (SiO_2/Ta_2O_5) and 1.5-period ($SiO_2/Ta_2O_5/SiO_2$ or $Ta_2O_5/SiO_2/Ta_2O_5$) quarter-wavelength-thick layers that surround a half-wavelength-thick layer of SiO_2 for the first structure, as shown in Figure 56(a), and a half-wavelength-thick layer of Ta_2O_5 for the second structure, as shown in Figure 56(b). If the optical thickness of each of the SiO_2/Ta_2O_5 layers is perfect, a spectrophotometer

measurement should show a reflectance null at the targeted wavelength of 405 nm. However, this is never the case initially, and the first deposited Fabry-Perot cavity with layer thicknesses based on ellipsometry calibrations typically have reflectance nulls ranging between 380 to 430 nm, which means that the deposition time needs to be adjusted. Note that in the following discussion, the layers of the Fabry-Perot cavities are referred to as *quarter-wave* and *half-wave* layers, but the actual optical thicknesses vary during the IBD calibration method with the goal of eventually obtaining the correct thicknesses.

In the original IBD calibration method, the first Fabry-Perot cavity is deposited with a SiO_2 half-wave layer, as depicted in Figure 56(a), and then its reflectance is measured using a Cary 500 spectrophotometer. If the reflectance null is offset from the desired wavelength of 405 nm, the deposition time for SiO_2 is adjusted, as described by

$$t_{IBD}' = \left(\frac{\lambda}{\lambda_{null}}\right) t_{IBD} \tag{23}$$

where t_{IBD}' is the adjusted IBD deposition time, λ is the targeted wavelength ($\lambda = 405$ nm in this case), λ_{null} is the measured wavelength of the reflectance null, and t_{IBD} is the original deposition time of the half-wavelength-thick layer (SiO_2 or Ta_2O_5) that was used during the deposition of the Fabry-Perot cavity. For example, if the SiO_2 half-wave Fabry-Perot cavity had a reflectance null at 410 nm (5 nm longer than the target wavelength of $\lambda = 405$ nm), this calibration method assumes that the SiO_2 half-wave layer was too thick and the deposition time for SiO_2 should be reduced by ~1.22% to produce a reflectance null at 405 nm. After adjusting the SiO_2 deposition time accordingly, the second type of Fabry-Perot cavity is deposited with a half-wave Ta_2O_5 layer, as illustrated in Figure 56(b), and its reflectance is measured. Again, it is assumed that the reflectance null depends solely on the thickness of the half-wave layer (Ta_2O_5 this time), and Equation (23) is used to adjust the Ta_2O_5 deposition

time based on the wavelength of the reflectance null. Using the new deposition times, a third Fabry-Perot cavity is deposited with a half-wave SiO_2 layer, and this calibration process repeats for a total of four to six Fabry-Perot cavities. If the calibration method is successful, the final SiO_2 and Ta_2O_5 half-wave Fabry-Perot cavity structures should both have a reflectance null at the targeted wavelength of 405 nm. Finally, those calibrated quarter-wavelength deposition times are then used to deposit the Ta_2O_5/SiO_2 DBR.

While this IBD calibration method of depositing Fabry-Perot cavities is better than simply relying on ellipsometry measurements, further investigation revealed that there were problems with this method. In the ideal situation, the reflectance null should converge to the targeted wavelength of 405 nm after adjusting the deposition time based on several Fabry-Perot cavity depositions. However, the reflectance null did not converge to the targeted wavelength during the calibration for the 10-period n-DBR in the previous devices, even after six Fabry-Perot cavity depositions. Figure 57 shows the reflectance of six Fabry-Perot cavities that were deposited using the previously-described IBD calibration method wherein the SiO_2 and Ta_2O_5 deposition times were adjusted based on the measured reflectance nulls.

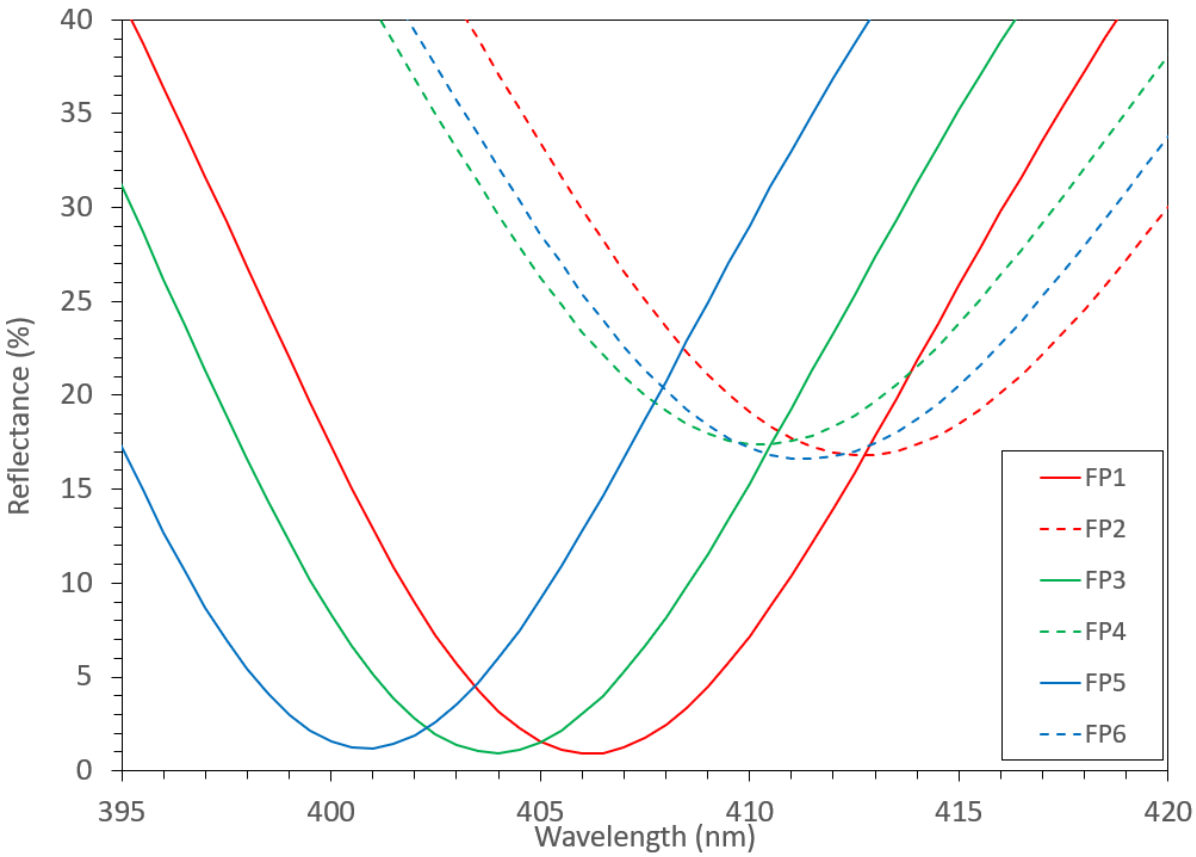


Figure 57. Reflectance of six Fabry-Perot (FP) cavities that were deposited during the IBD calibration for the 10-period Ta_2O_5/SiO_2 n-DBR that was deposited on the previous VCSELs that failed to lase. Solid curves represent a Fabry-Perot cavity with a SiO_2 half-wave layer (FP1, FP3, and FP5) and dashed curves are cavities with a Ta_2O_5 half-wave layer (FP2, FP4, and FP6).

The solid curves represent the reflectance for Fabry-Perot cavities with a SiO_2 half-wave layer (FP1, FP3, and FP5) and the dashed curves are for cavities that have Ta_2O_5 half-wave layers (FP2, FP4, and FP6). In the order of deposition, the six Fabry-Perot cavities had reflectance nulls at approximately 406 nm, 413 nm, 404 nm, 410 nm, 401 nm, and 411 nm. Even after adjusting the deposition time by calibrating using six Fabry-Perot cavities, the reflectance null wavelength did not converge to 405 nm. Instead, for the SiO_2 half-wave Fabry-Perot cavities, the reflectance nulls diverged from the target wavelength of 405 nm as it shifted from 406 nm (FP1) to 401 nm (FP5), as shown by the solid red and blue curves in Figure 57. The reflectance nulls for the Ta_2O_5 half-wave Fabry-Perot cavities only improved slightly as they shifted from

413 nm (FP2) to 411 nm (FP6), as shown by the dashed red and blue curves in Figure 57. Because the wavelength of the reflectance nulls did not converge to the target wavelength of 405 nm, it indicated that there could be a problem with the IBD calibration method, which could explain the unexpected reflectance spectrum of the 10-period DBR that was deposited on the VCSELs that failed to lase.

With the goal of identifying problems with the IBD calibration method, the half-wave SiO_2 and Ta_2O_5 Fabry-Perot cavities (as illustrated in Figure 56) were modeled using TMM simulations. As expected, the simulated reflectance for each structure had a reflectance null at the target wavelength of 405 nm when the SiO_2 and Ta_2O_5 layers had the correct optical thicknesses with quarter-wave thicknesses of 67.0494 nm and 46.5646, respectively, and half-wave thicknesses that were twice those values (assuming refractive indices $n_{SiO_2} = 1.51008$ and $n_{Ta_2O_5} = 2.1744$). The next step was to simulate Fabry-Perot cavities with incorrect layer thicknesses and apply the IBD calibration method to the simulation to see if the reflectance null converges to the target wavelength after six Fabry-Perot calibrations. The first simulated Fabry-Perot cavity (FP1) was chosen to have incorrect quarter-wave and half-wave layers so that the simulated reflectance null matched the experimental value of 406 nm. The simulated structure had SiO_2 layers that were ~2.3% thinner than the correct optical thickness and the Ta_2O_5 layers were ~5.2% thicker than the correct thickness, yielding a simulated reflectance null of 406 nm for FP1. According to the IBD calibration procedure, the reflectance null only depends on the thickness of the half-wave layer, so the SiO_2 thickness should be reduced slightly when simulating the next Fabry-Perot cavity (FP2). However, this revealed a flaw in the IBD calibration method because the simulated structure actually had an SiO_2 thickness that was thinner than the correct optical thickness. This meant that the IBD

calibration procedure incorrectly assumed that the half-wave layer was the only factor that affected the position of the reflectance null. By applying this flawed calibration method to the simulated structure, the reflectance null values were similar to the experimental results and did not converge to the target wavelength of 405 nm. Table 2 summarizes these results and compares the reflectance null wavelengths between the experimental and simulated data.

Table 2. Comparison of experimental and simulated reflectance null wavelengths for SiO_2 and Ta_2O_5 half-wave Fabry-Perot cavities that were deposited to calibrate the IBD for DBR deposition. The Fabry-Perot cavities consist of the structure illustrated in Figure 56, and the experimentally measured reflectance null wavelengths are from Figure 57. In the TMM simulations, the perfect quarter-wave thicknesses for SiO_2 and Ta_2O_5 were 67.0494 nm and 46.5646, respectively (assuming refractive indices $\boldsymbol{n_{SiO_2} = 1.51008}$ and $\boldsymbol{n_{Ta_2O_5} = 2.1744}$). These thicknesses were modified to 65.5 nm for SiO_2 and 49 nm for Ta_2O_5 to shift the simulated reflectance null to 406 nm to match the experimental data for the first structure (FP1). By applying the IBD calibration procedure to the simulation and modifying the SiO_2 and Ta_2O_5 layer thicknesses accordingly, the simulated reflectance nulls were similar to the experimental values and did not converge to the target wavelength of 405 nm.

Fabry-Perot Cavity	½-Wave Layer	Experimental Reflectance Null Wavelength (nm)	Simulated Reflectance Null Wavelength (nm)	Simulated ¼-Wave SiO_2 Thickness (nm)	Simulated ¼-Wave Ta_2O_5 Thickness (nm)
FP1	SiO2	406	406	65.50	49.00
FP2	Ta2O5	413	415	65.29	49.00
FP3	SiO2	404	402	65.29	47.86
FP4	Ta2O5	410	409	65.72	47.86
FP5	SiO2	401	402	65.72	47.35
FP6	Ta2O5	411	407	66.15	47.35

The experimental reflectance null wavelengths are from the Fabry-Perot cavity reflectance spectra that were shown in Figure 57, and the first simulated structure (FP1) had quarter-wave thicknesses of 65.5 nm for SiO_2 (~2.3% thinner than the correct quarter-wave thickness) and 49 nm for Ta_2O_5 (~5.2% thicker than the correct quarter-wave thickness). Although not shown in the table, the half-wave layer thicknesses were twice the thickness of the quarter-wave layer thickness. For example, FP1 had an SiO_2 half-wave layer thickness of 131 nm, and FP2 had a Ta_2O_5 half-wave layer thickness of 98 nm. By applying the flawed IBD calibration method to the simulation, a 406 nm reflectance null means that the SiO_2 thickness should be reduced (by a factor of ~405/406) to 65.29 nm for FP2. This resulted in a simulated reflectance null at 415

nm for FP2, which is similar to the experimental value of 413 nm. Note that the reflectance null values in Table 2 were rounded to the nearest integer for simplicity, but their exact values were used in the calculations. Assuming the simulated reflectance null at 415 nm meant that the Ta_2O_5 layer was too thick for FP2, the quarter-wave Ta_2O_5 layers were reduced (by a factor of ~405/415) to 47.86 nm when simulating FP3. This resulted in a simulated reflectance null of 402 nm for FP3, which is similar to the experimental value of 404 nm. This process was continued to simulate a total of six Fabry-Perot cavities, and the final simulated reflectance nulls were 402 nm and 407 nm for FP5 and FP6, respectively. Similar to the experimental results, the simulated reflectance nulls did not converge to the target wavelength of 405 nm.

TMM simulations revealed a flaw in the IBD calibration method in which there was an incorrect assumption that the reflectance null of the Fabry-Perot cavities only depended on the half-wave layer thickness. Instead, for example, the reflectance of the cavity with a half-wave SiO_2 layer not only depends on the half-wave SiO_2 thickness, but it also depends on the quarter-wave thicknesses of SiO_2 and Ta_2O_5. This means that there are an infinite number of combinations of SiO_2 and Ta_2O_5 thicknesses that could produce a given reflectance null. For example, a reflectance null at 410 nm for a half-wave SiO_2 Fabry-Perot cavity could be caused by several possibilities: 1) the SiO_2 layers could be too thick, 2) the Ta_2O_5 layers could be too thick, or 3) both layers could be too thick. As shown by the example in Table 2, the SiO_2 layers could even be too thin, but the relatively thick Ta_2O_5 layers pushed the simulated reflectance null to longer wavelengths than the target wavelength of 405 nm. Therefore, adjusting layer thicknesses based on the reflectance null of a single Fabry-Perot cavity could result in layer thicknesses that are even further away from the correct optical thicknesses.

The next objective was to create an improved IBD calibration method using TMM simulations. While the reflectance null of a single Fabry-Perot cavity could be caused by various combinations of SiO_2 and Ta_2O_5 layer thicknesses, it is possible to determine the actual layer thicknesses by comparing the reflectance nulls of two different Fabry-Perot cavities. This can be accomplished by using the same SiO_2/Ta_2O_5 IBD deposition rates to deposit an SiO_2 half-wave Fabry-Perot cavity and then a Ta_2O_5 half-wave structure (onto a separate silicon wafer). Based on the reflectance null wavelengths for each structure, TMM simulations indicate that there is only one possible combination of SiO_2/Ta_2O_5 deposition rates that could produce the unique pair of reflectance null wavelengths. For example, reflectance null wavelengths at 406 nm for the SiO_2 half-wave Fabry-Perot structure and 411 nm for the Ta_2O_5 structure can only be reproduced in the simulation if the SiO_2 quarter-wave layers are ~1 nm thinner than the targeted optical thickness and Ta_2O_5 quarter-wave layers are ~1.5 nm too thick (with half-wave layers ~2 nm too thin for SiO_2 and ~3 nm too thick for Ta_2O_5). Even though the SiO_2 layers were thinner than the intended optical thickness, the SiO_2 half-wave structure had a simulated reflectance null longer than the targeted wavelength of 405 nm because the Ta_2O_5 layers were too thick. It can be seen that the reflectance null depends more strongly on the thickness of the material used for the half-wave layer, but the thickness of the other quarter-wave layers can still significantly affect the wavelength.

By simulating several Fabry-Perot cavities with various layer thicknesses, a model was created to determine the SiO_2 and Ta_2O_5 layer thicknesses based on a unique pair of reflectance null wavelengths from a SiO_2 half-wave Fabry-Perot cavity and a Ta_2O_5 half-wave cavity. The simulated Fabry-Perot cavities still had the structure shown Figure 56, but the quarter-wave and half-wave layer thicknesses were varied from the perfect optical thickness

values to see the effect on the reflectance null wavelength. The layer thickness of each material was varied by a constant factor for each simulation, which would be similar to depositing these structures using incorrect IBD deposition rates. For example, in the case of simulating an underestimate of the SiO_2 deposition rate, one simulation consisted of a Fabry-Perot cavity with SiO_2 quarter-wave layers that were each 1 nm thicker than the correct optical thickness and a half-wave SiO_2 layer that was 2 nm thicker than the correct optical thicknesses. Several simulations were conducted for a variety of combinations of underestimates and overestimates of the SiO_2 and Ta_2O_5 deposition rates, as illustrated in Figure 58.

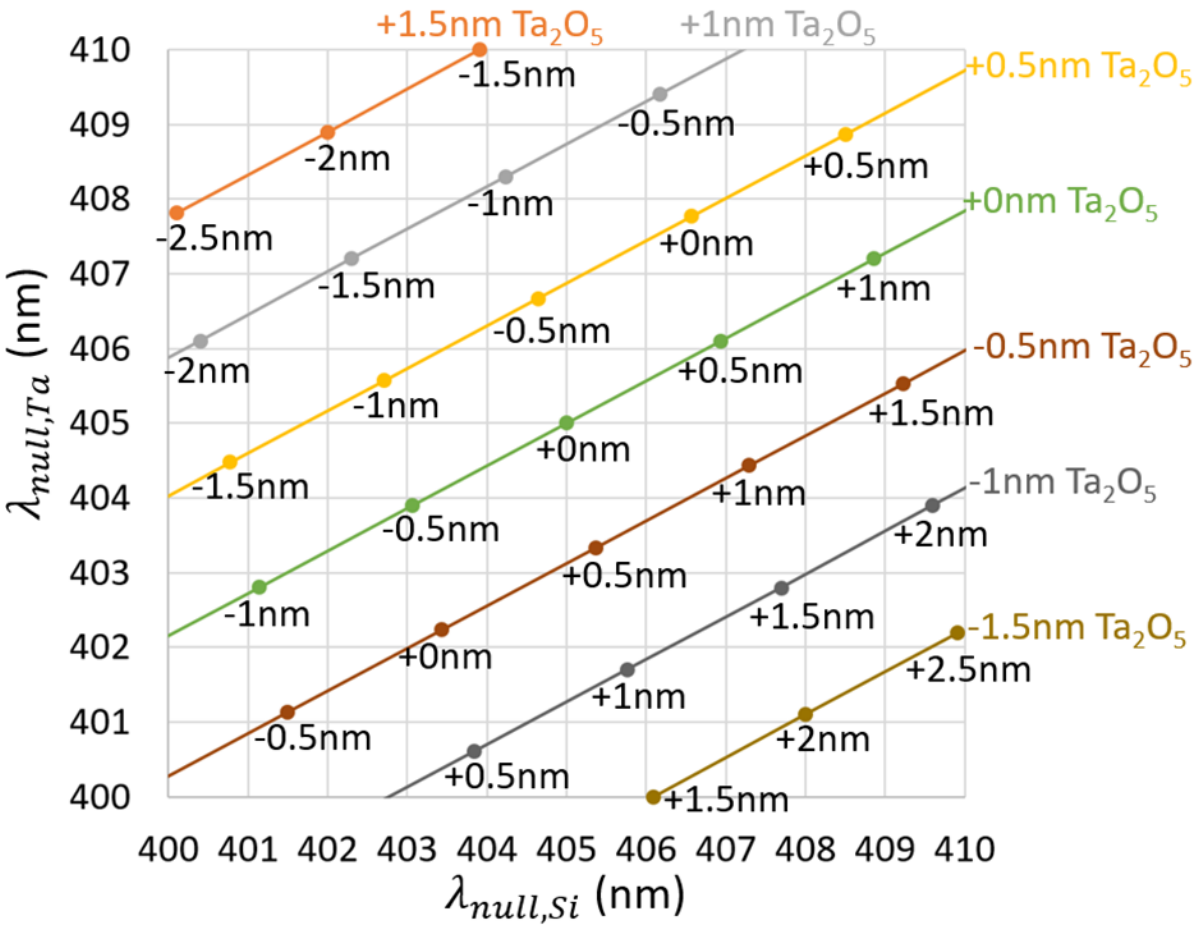


Figure 58. Simulated reflectance nulls for SiO_2 and Ta_2O_5 half-wave Fabry-Perot (FP) cavities with various layer thicknesses. Each colored line represents a specific Ta_2O_5 quarter-wave thickness; for example, data points on the yellow curve correspond to Ta_2O_5 quarter-wave layers that are 0.5 nm thicker than the perfect optical thickness. Similarly, the black text under each data point denotes the thickness of the SiO_2 quarter-wave layers compared to the perfect optical thickness.

The x-axis represents the reflectance null wavelengths for SiO_2 half-wave structures while the y-axis represents the reflectance null wavelengths Ta_2O_5 half-wave structures. For a given pair of reflectance null wavelengths for SiO_2 and Ta_2O_5 half-wave Fabry-Perot cavities, the curves in Figure 58 estimate the actual layer thicknesses in terms of the difference in the thickness of quarter-wave layers compared to the perfect quarter-wave thickness. Each colored line represents a specific Ta_2O_5 quarter-wave thickness; for example, data points on the yellow curve correspond to Ta_2O_5 quarter-wave layers that are 0.5 nm thicker than the perfect optical thickness. Similarly, the black text under each data point denotes the thickness of the SiO_2 quarter-wave layers compared to the perfect optical thickness. For example, reflectance nulls at 408 nm for the SiO_2 half-wave structure and 401 nm for the Ta_2O_5 half-wave structure predict that the quarter-wave layers were 2 nm thicker and 1.5 nm thinner than the perfect optical thicknesses for SiO_2 and Ta_2O_5, respectively.

The next objective was to generalize the results so that accurate SiO_2 and Ta_2O_5 layer thicknesses could be predicted for any given pair of reflectance null wavelengths. It was seen that for a given Ta_2O_5 quarter-wave thickness, the reflectance null wavelength linearly depended on the SiO_2 quarter-wave thickness. The converse was also true, and the reflectance null wavelength linearly depended on the Ta_2O_5 quarter-wave thickness for a given SiO_2 quarter-wave thickness. The solution space consisted of a series of parallel lines, and the actual layer thicknesses of any pair of Fabry-Perot cavities could be obtained by comparing the relative position of their reflectance null wavelengths to the targeted wavelength of 405 nm. The following equations describe trends from the simulated reflectance data which led to creating a model that can predict the SiO_2 and Ta_2O_5 layer thicknesses within the Fabry-Perot cavities based on any given pair of reflectance null wavelengths ($\lambda_{Null,Si}$ and $\lambda_{Null,Ta}$). To

simplify the problem by considering the case with perfect SiO_2 optical thicknesses, the Ta_2O_5 half-wave Fabry-Perot simulated reflectance null wavelength was found to shift by a linear factor that depended on the Ta_2O_5 layer thickness, as described by

$$\lambda_{Shift,Ta} = (\sim 3.746)(T_{\lambda/4,Ta} - T^*_{\lambda/4,Ta}) \quad (24)$$

where $\lambda_{Shift,Ta}$ is the shift in nanometers for the Ta_2O_5 half-wave Fabry-Perot reflectance null wavelength compared to the target wavelength (405 nm in this case), $T_{\lambda/4,Ta}$ is the actual thickness in nanometers for the Ta_2O_5 quarter-wave layers in the structure (usually shifted slightly from the perfect quarter-wave thickness), and $T^*_{\lambda/4,Ta}$ is the perfect thickness for a Ta_2O_5 quarter-wave layer. For example, if the Ta_2O_5 quarter-wave layers were 1 nm thicker than the correct quarter-wave thickness ($T_{\lambda/4,Ta} - T^*_{\lambda/4,Ta} = 1$ nm), the Ta_2O_5 half-wave Fabry-Perot reflectance null wavelength would shift by 3.746 nm (corresponding to a wavelength of 408.746 nm). Similarly, for the case with perfect Ta_2O_5 optical thicknesses, the SiO_2 half-wave Fabry-Perot reflectance null wavelength shifted by a linear factor according to the SiO_2 layer thickness, as described by

$$\lambda_{Shift,Si} = (\sim 3.857)(T_{\lambda/4,Si} - T^*_{\lambda/4,Si}) \quad (25)$$

where $\lambda_{Shift,Si}$ is the shift in nanometers for the SiO_2 half-wave Fabry-Perot reflectance null wavelength compared to the target wavelength, $T_{\lambda/4,Si}$ is the actual thickness for the SiO_2 quarter-wave layers in the structure, and $T^*_{\lambda/4,Si}$ is the perfect optical thickness for a SiO_2 quarter-wave layer. For a given Ta_2O_5 quarter-wave thickness, the simulated reflectance nulls formed a series of parallel lines, as described by

$$\lambda_{Null,Ta} = m_{Ta/Si}\,\lambda_{Null,Si} + \lambda^o_{Null,Ta} \quad (26)$$

where $\lambda_{Null,Ta}$ is the reflectance null wavelength of the Ta_2O_5 half-wave structure, $m_{Ta/Si}$ is the slope of the line with a value of ~0.571, $\lambda_{Null,Si}$ is the reflectance null wavelength for the

SiO_2 half-wave structure, and $\lambda^o_{Null,Ta}$ is the *y-intercept* value for the theoretical case when $\lambda_{Null,Si}$ is zero (note that this is not physically possible because it would require negative values of layer thicknesses). The green line in Figure 58 is described by Equation (26) for the special case when the Ta_2O_5 optical layer thickness is perfect (when $\lambda_{Null,Ta} = 405$ nm), and this line has a *y-intercept* value of ~173.571 which will be designated as $\lambda^{*o}_{Null,Ta}$. The next step was to calculate $\lambda^o_{Null,Ta}$ by inserting the reflectance null wavelengths ($\lambda_{Null,Si}$ and $\lambda_{Null,Ta}$) into Equation (26). As shown by the other colored lines in Figure 58, altering the Ta_2O_5 thickness simply offsets the lines vertically from the green line, so the difference in the *y-intercepts* ($\lambda^o_{Null,Ta} - \lambda^{*o}_{Null,Ta}$) can be used to determine the true Ta_2O_5 thickness. Therefore, the actual Ta_2O_5 quarter-wave thickness ($T_{\lambda/4,Ta}$) can be calculated, as described by

$$T_{\lambda/4,Ta} = T^*_{\lambda/4,Ta} + \frac{\lambda^o_{Null,Ta} - \lambda^{*o}_{Null,Ta}}{3.746} \tag{27}$$

where $T^*_{\lambda/4,Ta}$ is the perfect thickness for a Ta_2O_5 quarter-wave layer, $\lambda^o_{Null,Ta}$ is the *y-intercept* that can be calculated by inserting the pair of reflectance null wavelengths ($\lambda_{Null,Si}$ and $\lambda_{Null,Ta}$) into Equation (26), and $\lambda^{*o}_{Null,Ta}$ has a constant value of ~173.571 (this is the *y-intercept* for the structure with a perfect SiO_2 optical thickness for a designed wavelength of 405 nm). Noting that $\lambda_{Null,Si}$ redshifted by ~3.16 nm for every nanometer that $T_{\lambda/4,Ta}$ was thicker than the perfect optical thickness, the final step was to calculate the actual thickness of the SiO_2 quarter-wave layers, $T_{\lambda/4,Si}$, as described by

$$T_{\lambda/4,Si} = T^*_{\lambda/4,Si} + \frac{\lambda_{Shift,Si} - 3.16\left(T_{\lambda/4,Ta} - T^*_{\lambda/4,Ta}\right)}{3.857} \tag{28}$$

where $T^*_{\lambda/4,Si}$ is the perfect thickness for an SiO_2 quarter-wave layer, $\lambda_{Shift,Si}$ is the shift in the SiO_2 half-wave Fabry-Perot reflectance null wavelength compared to the target wavelength,

and $\left(T_{\lambda/4,Ta} - T^{*}_{\lambda/4,Ta}\right)$ is the difference in the actual thickness of the Ta_2O_5 quarter-wavelength layers compared to the perfect quarter-wave values. Note that Equation (28) is equivalent to Equation (25) for the case with perfect Ta_2O_5 optical thicknesses ($T_{\lambda/4,Ta} = T^{*}_{\lambda/4,Ta}$).

Therefore, the actual thicknesses of the Ta_2O_5/SiO_2 quarter-wave layers ($T_{\lambda/4,Ta}$ and $T_{\lambda/4,Si}$) can be calculated based on two reflectance null wavelengths ($\lambda_{Null,Si}$ and $\lambda_{Null,Ta}$). By generalizing Equation (27) and Equation (28) for any target wavelength and refractive index, the actual thicknesses of the Ta_2O_5/SiO_2 quarter-wave layers can be calculated, as described by

$$T_{\lambda/4,Ta} = \frac{\lambda}{4\, n_{Ta_2O_5}} + \frac{\lambda_{Null,Ta} - 0.571\, \lambda_{Null,Si} - 0.429\, \lambda}{3.746} \tag{29}$$

$$T_{\lambda/4,Si} = \frac{\lambda}{4\, n_{SiO_2}} + \frac{\lambda_{Null,Si} - \lambda - 3.16\left(T_{\lambda/4,Ta} - \frac{\lambda}{4\, n_{Ta_2O_5}}\right)}{3.857} \tag{30}$$

where $T_{\lambda/4,Ta}$ and $T_{\lambda/4,Si}$ are the actual thicknesses of the quarter-wave layers for Ta_2O_5 and SiO_2 in the Fabry-Perot half-wave cavities, λ is the target wavelength, $\lambda_{Null,Ta}$ is the reflectance null wavelength of the Ta_2O_5 half-wave structure, $\lambda_{Null,Si}$ is the reflectance null wavelength for the SiO_2 half-wave structure, $n_{Ta_2O_5}$ is the refractive index of Ta_2O_5, and n_{SiO_2} is the refractive index of SiO_2. Using refractive indices from ellipsometry measurements, Equation (29) and Equation (30) can predict the actual Ta_2O_5 and SiO_2 quarter-wave layer thicknesses based on the pair of measured reflectance null wavelengths for the two Fabry-Perot cavities. This information can then be used to obtain more accurate IBD deposition times that can be implemented to deposit higher-quality DBRs with correct quarter-

wavelength SiO_2/Ta_2O_5 optical thicknesses. Note that the constants in Equation (29) and Equation (30) were calculated based on reflectance simulations that used particular values for $n_{Ta_2O_5}$ and n_{SiO_2}, so it is possible that the values of the constants could vary as a function of refractive index. Additionally, the reflectance simulations did not consider the effect of index dispersion in which refractive index varies as a function of wavelength.

An improved IBD calibration method was developed using the results from the TMM reflectance simulations so that higher-quality DBRs could be deposited with more accurate quarter-wave layer thicknesses for SiO_2 and Ta_2O_5. Similar to the previous calibration method, the first step is to deposit single layers of SiO_2 and Ta_2O_5 on separate silicon wafers. Ellipsometry is used to measure their refractive indices and thicknesses, which are used to obtain IBD deposition times to deposit quarter-wave layers, as described by Equation (22). In contrast with the previous IBD calibration method, the next step is to deposit an SiO_2 half-wave Fabry-Perot cavity and a Ta_2O_5 half-wave structure on separate silicon or sapphire wafers using the same IBD deposition rates for each layer. For further clarification, each of the SiO_2 quarter-wave layers have the same deposition time for both cavities, and each of the Ta_2O_5 quarter-wave layers have the same deposition time for both cavities. The half-wave SiO_2 and Ta_2O_5 layers have a deposition time that is doubled compared to their respective quarter-wave layers, and the half-wave Fabry-Perot cavities consist of the structures illustrated in Figure 56(a) and Figure 56(b). The next step is to measure the reflectance spectra of each Fabry-Perot cavity using a Cary 500 spectrophotometer to obtain the reflectance null wavelengths for each structure ($\lambda_{Null,Si}$ and $\lambda_{Null,Ta}$), which are likely shifted from the target wavelength. These reflectance null values are then inputted into Equation (29) and Equation (30) to predict the actual quarter-wave layer thicknesses of Ta_2O_5 and SiO_2 in the Fabry-Perot

cavities based on the model that was developed using TMM reflectance simulations. These thicknesses are used to modify the IBD deposition time to deposit quarter-wave layers that are closer to the correct optical thicknesses, and the IBD deposition times for SiO_2 and Ta_2O_5 are adjusted as described by

$$t'_{\lambda/4} = \frac{T^*_{\lambda/4}}{T_{\lambda/4}}\, t_{\lambda/4} \tag{31}$$

where $t'_{\lambda/4}$ is the adjusted IBD deposition time to deposit a quarter-wave layer of SiO_2 or Ta_2O_5, $t_{\lambda/4}$ is the original IBD deposition time that was used for the quarter-wave layers in the two Fabry-Perot cavities, $T^*_{\lambda/4}$ is the correct thickness for a quarter-wave layer of SiO_2 or Ta_2O_5, and $T_{\lambda/4}$ is the actual thickness of the quarter-wave layer ($T_{\lambda/4,Si}$ or $T_{\lambda/4,Ta}$) that was calculated using Equation (29) or Equation (30). After calculating the adjusted IBD deposition times to deposit quarter-wave (and half-wave) layers of SiO_2 and Ta_2O_5, the next step is to deposit another pair of SiO_2 and Ta_2O_5 half-wave Fabry-Perot cavities on separate silicon or sapphire wafers using the modified IBD deposition rates for each layer. Following the same process as before, the two reflectance null wavelengths are measured, Equation (29) and Equation (30) are used to calculate the actual SiO_2/Ta_2O_5 quarter-wave layer thicknesses, and Equation (31) is used to adjust the IBD deposition time for both layers. If the reflectance null wavelengths are both within ~$\pm$2 nm of the target wavelength, the final step is to deposit the DBR on the VCSEL samples using the adjusted IBD deposition times. If not, another pair of SiO_2 and Ta_2O_5 half-wave Fabry-Perot cavities are deposited on separate silicon wafers, and this process is repeated until the reflectance null wavelengths are both within ~$\pm$2 nm of the target wavelength.

During experimental testing of the improved IBD calibration method, additional factors were found to have an effect on the SiO_2 and Ta_2O_5 layer thicknesses and reflectance spectra of Fabry-Perot cavities and DBRs. First, the native oxide on the silicon wafers was found to affect the ellipsometry and reflectance spectra measurements. For silicon wafers with surfaces freshly exposed to air in ambient conditions, a native oxide will grow to a self-limiting thickness of ~2.1 nm within a few hours.[166] During the initial steps of the IBD calibration method to deposit single layers of SiO_2 and Ta_2O_5 on separate silicon wafers, the native oxide on the silicon wafers was found to slightly increase the ellipsometry thickness measurements, which resulted in overestimates of the IBD deposition rates for each layer. This caused underestimates of the deposition times for each layer, so the reflectance nulls of the first two deposited Fabry-Perot cavities were at shorter wavelengths than the targeted wavelength. One way to account for this effect is to subtract the ellipsometry thickness measurements by a certain factor to account for the native oxide. In practice, the ellipsometry thickness measurements have been reduced by 8 nm for SiO_2 and 4 nm for Ta_2O_5 to account for the native oxide. While this produced more accurate deposition rates in some cases, there have been other cases in which the first pair of Fabry-Perot cavities had reflectance nulls at wavelengths ~15 nm longer than the target wavelength. Practically, this is not a problem because accurate IBD deposition rates can be obtained based on the reflectance null wavelengths of the Fabry-Perot cavities. However, the native oxide could have a slight effect on the reflectance null wavelengths of the Fabry-Perot cavities. By including a 2-nm-thick SiO_2 layer in the TMM reflectance simulations to act as the native oxide, the simulated reflectance null of the Fabry-Perot cavities redshifted by 1.2 nm for the SiO_2 half-wave structure (FP1) and it redshifted by 0.8 nm for the Ta_2O_5 half-wave structure (FP2). This was

studied experimentally by depositing the same Fabry-Perot cavity on a silicon wafer with a native oxide, a silicon wafer without a native oxide, and a sapphire wafer. The native oxide on a silicon wafer can be removed by submerging the sample in buffered hydrofluoric (BHF) acid until the surface becomes hydrophobic (SiO_2 is hydrophilic so water spreads out on the wafer while bare silicon is hydrophobic wherein water droplets remain spherical on the surface with a large contact angle). To study the effect of the native oxide on the reflectance null wavelength, three samples were coloaded during IBD deposition of SiO_2 and Ta_2O_5 half-wave Fabry-Perot cavities: a silicon wafer with a native oxide, a silicon wafer that had its native oxide removed with BHF, and a sapphire wafer. Figure 59 shows the reflectance spectra of these Fabry-Perot cavities for each of the three substrates.

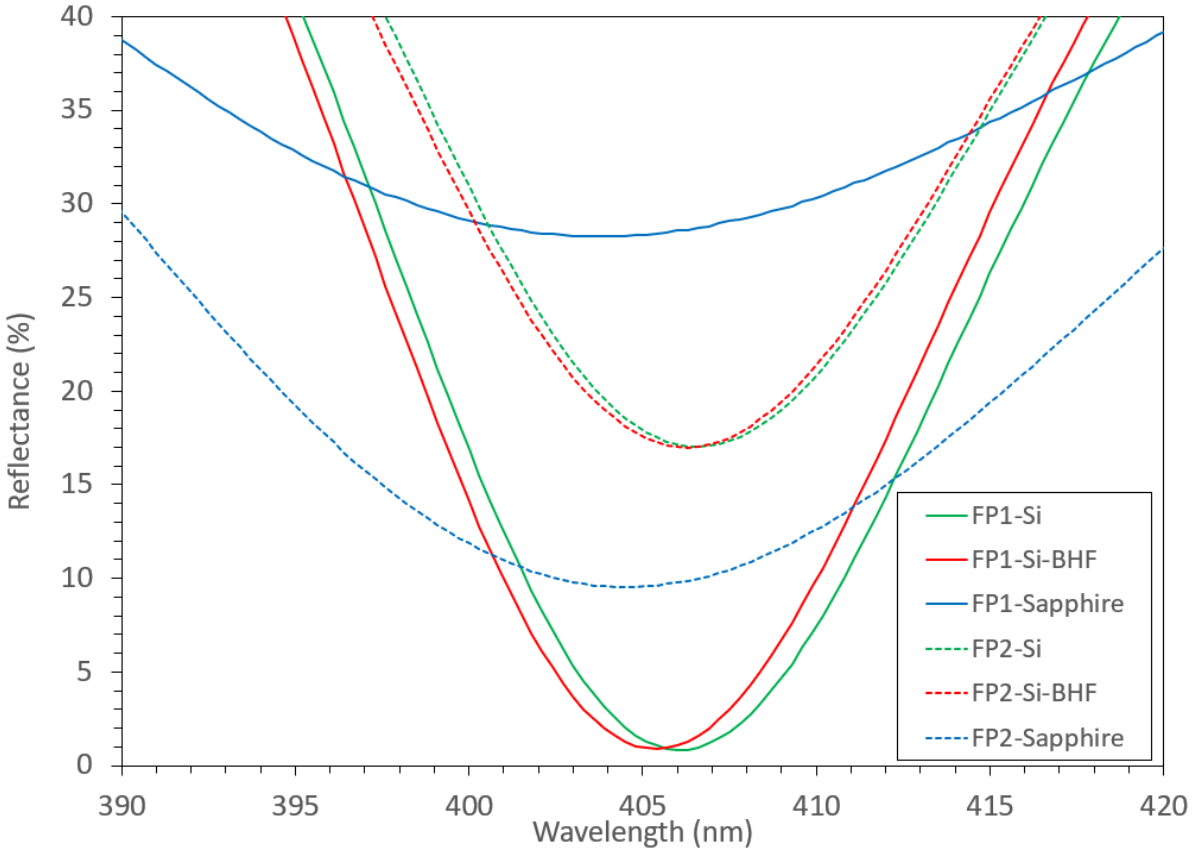


Figure 59. Reflectance spectra of SiO_2 and Ta_2O_5 half-wave Fabry-Perot (FP) cavities deposited on three different substrates that were coloaded during IBD deposition: a silicon with a native oxide (*FP1-Si* and *FP2-*

Si), a silicon wafer with its native oxide removed with BHF (*FP1-Si-BHF* and *FP2-Si-BHF*), and sapphire (*FP1-Sapphire* and *FP2-Sapphire*). Removing the silicon wafer native oxide with BHF prior to IBD deposition caused the reflectance null to shift slightly toward shorter wavelengths, and the Fabry-Perot cavities deposited on sapphire had the shortest wavelength reflectance nulls.

The IBD calibration procedure heavily depends on the reflectance spectra of Fabry-Perot cavities, so the primary goal of this experiment was to determine whether the native oxide on silicon shifts the reflectance null wavelengths and whether it significantly affects the IBD calibration. The samples labelled *FP1* have the SiO_2 half-wave Fabry-Perot cavity structure illustrated in Figure 56(a) and *FP2* have the Ta_2O_5 half-wave structure illustrated in Figure 56(b). As shown by the solid curves in Figure 59 for the SiO_2 half-wave structures, the reflectance null wavelength was at 406 nm for the untreated silicon wafer with a native oxide (*FP1-Si*), 405.4 nm for the silicon wafer treated with BHF to remove the native oxide (*FP1-Si-BHF*), and 403.8 nm for the sapphire wafer (*FP1-Sapphire*). This shows that a native oxide on the silicon wafer that is present prior to the Fabry-Perot cavity deposition can redshift the reflectance null wavelength, which can affect the IBD calibration process. The silicon wafer that was treated with BHF to remove the native oxide had a reflectance null wavelength that was only blueshifted by 0.6 nm compared to the untreated silicon wafer, which is a smaller shift than the expected shift of 1.2 nm based on TMM simulations for a 2-nm-thick native oxide. Even though the BHF treatment was performed directly prior to IBD deposition, this suggests that a native oxide was present on the wafer beneath the deposited layers. The native oxide was likely ~1 nm thinner on the BHF-treated silicon wafer compared to the untreated silicon wafer based on TMM reflectance simulations that show a shift of 0.6 nm in the reflectance null wavelength by adjusting the native oxide thickness by 1 nm. The sapphire wafer had the shortest reflectance null wavelength and was blueshifted by 2.2 nm compared to the untreated silicon wafer, which further suggested that the BHF-treated silicon wafer

formed a native oxide (otherwise the reflectance null wavelengths should match). Based on TMM simulations to produce a 2.2 nm shift, this suggested that the untreated silicon wafer had a native oxide thickness of 3.7 nm. This is somewhat thicker than expected because the native oxide on silicon usually does not become thicker than ~2.1 nm in ambient conditions,[166] but it is possible for thicker oxides to grow in moisture-rich and higher temperature environments. This topic could be further explored by measuring the silicon native oxide thickness and refractive index using ellipsometry and repeating this experiment to see if the reflectance null wavelength shift matches the simulation. Note that the TMM simulations assumed a refractive index of ~1.51 for SiO_2 for the native oxide and other SiO_2 layers. In the preceding discussion about estimating the native oxide thickness based on the reflectance null wavelength shift, it was also assumed that the IBD deposition rate was equivalent for each sample. Even though the wafers were coloaded, the IBD deposition rate can vary based on the radial position of the wafer on the sample holder, which would shift the reflectance null wavelength if samples were in different radial locations. However, this effect was accounted for and each sample was positioned in the same approximate radial position during deposition. These experiments were repeated several times and showed the same trends each time in terms of blueshifted reflectance null wavelengths for BHF-treated silicon wafers and sapphire wafers, which showed that the IBD deposition rate was consistent enough between samples that the effect of the native oxide on the reflectance null wavelength could be observed.

As shown by the dashed curves in Figure 59 for the next IBD deposition of the Ta_2O_5 half-wave structures, the reflectance null wavelength was at 406.6 nm for the untreated silicon wafer with a native oxide (*FP2-Si*), 406.3 nm for the silicon wafer treated with BHF to remove the native oxide (*FP2-Si-BHF*), and 404.8 nm for the sapphire wafer (*FP2-Sapphire*). This

shows the same trend as observed for *FP1* in which the reflectance null wavelength blueshifts for the BHF-treated silicon wafer and blueshifts further for the sapphire wafer. The BHF-treated silicon wafer had a blueshift of 0.3 nm compared to the untreated silicon wafer, which is a smaller shift than observed for *FP1*. There are two factors that could explain this smaller blueshift compared to the previous case. First, TMM simulations predict that a native oxide on the silicon wafer produces a slightly smaller shift in the reflectance null wavelength for a Ta_2O_5 half-wave cavity compared to a SiO_2 half-wave cavity. Secondly, the BHF-treated silicon wafer that was used for *FP2* likely had a thicker native oxide than the silicon wafer used for *FP1* because the BHF treatment was performed prior to the first IBD deposition for *FP1*, which was over four hours earlier. While four hours is normally enough time to grow a ~2 nm native oxide in ambient conditions, during that time, the oxide growth was inhibited by storing the BHF-treated silicon wafers in vacuum-sealed containers (99% vacuum, 1% nitrogen). However, vacuum-sealing does not completely prevent the native oxide growth based on ellipsometry measurements of BHF-treated silicon wafers that resided in vacuum-sealed containers for several days. Based on TMM simulations for a 0.3 nm blueshift compared to the untreated silicon wafer for *FP2*, the native oxide thickness was reduced by 0.8 nm for the BHF-treated sample that was stored in a vacuum-sealed container for ~4 hours prior to IBD deposition. In comparison, the reflectance null wavelength was blueshifted by 1.8 nm for the sapphire sample compared to the untreated silicon sample, which suggested that the untreated silicon sample had a native oxide of ~4.5 nm based on TMM simulations. As mentioned before, this experiment could be improved in the future by measuring the native oxide thickness and refractive index with ellipsometry prior to IBD deposition to verify that it matches the TMM reflectance simulation of the reflectance null wavelength shift.

These experiments were repeated, and the same trends were observed for each set of Fabry-Perot cavity depositions, which showed that the native oxide on silicon can redshift the reflectance null wavelength and affect the IBD calibration procedure. While the BHF treatment seemed to remove some of the native oxide, the reflectance null was always redshifted compared to sapphire samples. Furthermore, a BHF treatment was not an ideal solution because it would need to be performed immediately prior to every IBD deposition of the Fabry-Perot cavities during calibration. Therefore, the best solution to avoid the effects of the native oxide was to deposit Fabry-Perot cavities on sapphire instead of silicon wafers during IBD calibration. As shown by the blue curves in Figure 59, one potential disadvantage of using sapphire was that it is somewhat more difficult to determine the reflectance null wavelength because the dip in in the reflectance spectra was more broadened compared to Fabry-Perot cavities deposited on silicon wafers. In practice, this has not been a problem, especially if Fabry-Perot cavities were deposited on both silicon and sapphire wafers for comparison.

The previous 13λ and 23λ VCSELs failed to lase, which may have been due to the low reflectance of the 10-period n-DBR that was deposited using the old IBD calibration method. The next step was to apply the improved IBD calibration method to deposit higher-quality DBRs. The 10-period n-DBR was only deposited on half of the previous VCSEL samples, so there were several samples remaining to deposit the n-DBR using the improved IBD calibration method. At this point, the goal for these samples was to reach the threshold for lasing, so the number of mirror periods was increased to 12-periods in order to increase the peak reflectance. Following the improved IBD calibration method, SiO_2 half-wave and Ta_2O_5 halfwave cavities were deposited on separate sapphire wafers using the same IBD deposition

rates for each layer based on ellipsometry measurements, and the reflectance spectra was measured, as shown in Figure 60.

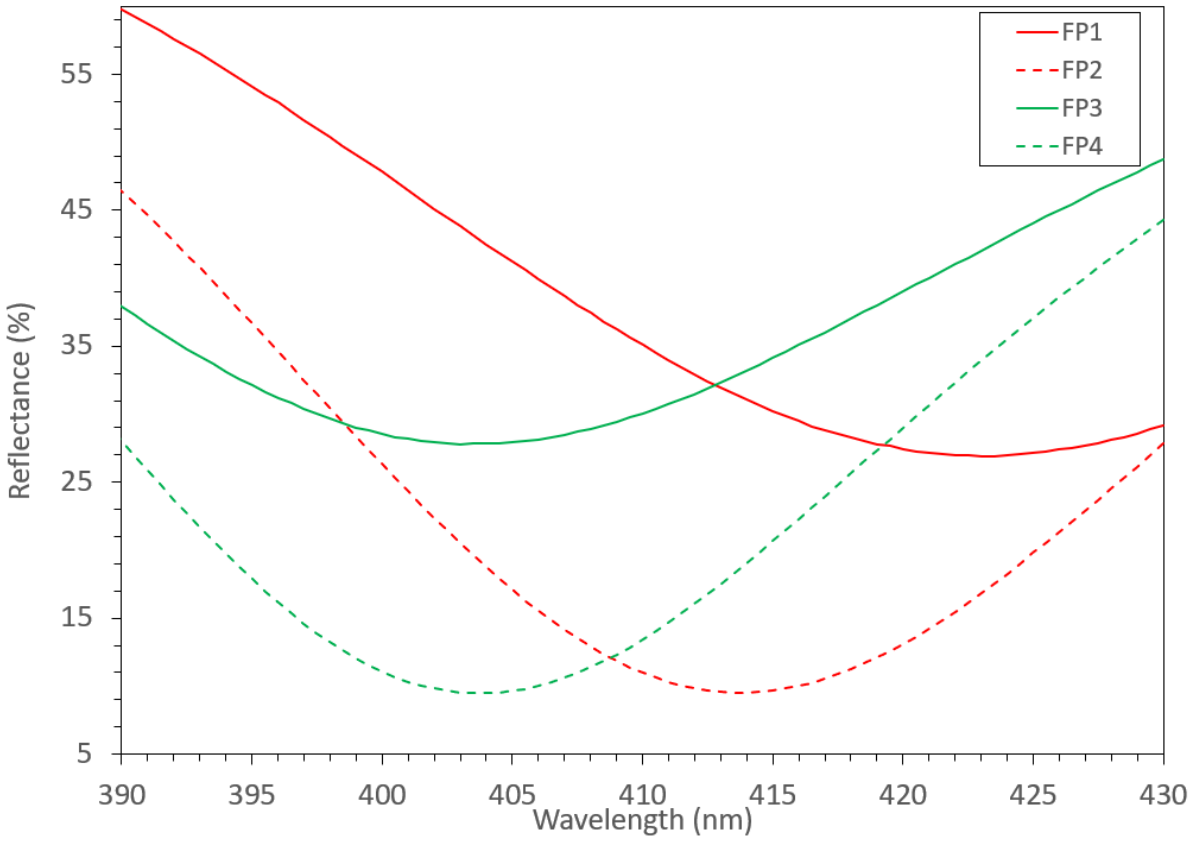


Figure 60. Reflectance spectra of SiO_2 and Ta_2O_5 half-wave Fabry-Perot (FP) cavities deposited sapphire using the improved IBD calibration method. The SiO_2 half-wave (*FP1*) and Ta_2O_5 halfwave (*FP2*) cavities were deposited on separate sapphire wafers using the same IBD deposition rates for each layer. The reflectance nulls of 423.2 nm (*FP1*) and 413.9 nm (*FP2*) were inserted into Equation (29) and (30) to calculate the actual layer thicknesses for SiO_2 and Ta_2O_5, and Equation (31) was used to calculate the adjusted IBD deposition time to obtain the correct optical thickness for each layer. The adjusted IBD deposition times for SiO_2 and Ta_2O_5 were used to deposit two more Fabry-Perot cavities (*FP3* and *FP4*), and their reflectance null wavelengths were at ~403.6 nm. This is close to the target wavelength of 403.8 nm, which means that the IBD calibration was successful and these deposition times can be used to deposit the DBR. Note that for a VCSEL target wavelength of 405 nm, the target wavelength is 403.8 nm during IBD calibration because the Cary 500 spectrophotometer measures the reflectance at an 8° incidence angle, which causes a blueshift of ~1.2 nm in the reflectance spectra based on TMM simulations.

The solid red curve represents the reflectance spectra for the first SiO_2 half-wave Fabry-Perot cavity (*FP1*) with a reflectance null wavelength of 423.2 nm, and the dashed red curve is for the Ta_2O_5 half-wave structure (*FP2*) with a reflectance null at 413.9 nm. By inserting these reflectance null wavelengths into Equation (29) and (30), it predicted that the quarter-wave

layers were ~5.2 nm too thick for SiO_2 and ~0.3 nm too thin for Ta_2O_5 compared to the perfect quarter-wave thicknesses. After using Equation (31) to adjust the IBD deposition time for each layer, another pair of SiO_2 half-wave (*FP3*) and Ta_2O_5 half-wave (*FP4*) Fabry-Perot cavities was deposited on separate sapphire wafers. As shown by the green curves in Figure 60, *FP3* and *FP4* both had reflectance null wavelengths at ~403.6 nm, which was close to the target wavelength of 403.8 nm and means that the optical layer thicknesses were accurate. Note that while the target VCSEL lasing wavelength is 405 nm, 403.8 nm was the target reflectance null wavelength for the Fabry-Perot cavities because the Cary 500 spectrophotometer measures the reflectance at an incidence angle of 8°, which causes a blueshift in the reflectance spectra by ~1.2 nm according to TMM simulations. Having achieved the target reflectance null wavelength for both Fabry-Perot cavities, it meant that the IBD calibration was complete and the next step was to deposit a 12-period DBR on the VCSEL samples. Figure 61 shows the reflectance spectra of a 12-period DBR that was deposited on a sapphire substrate that was coloaded with the VCSEL samples.

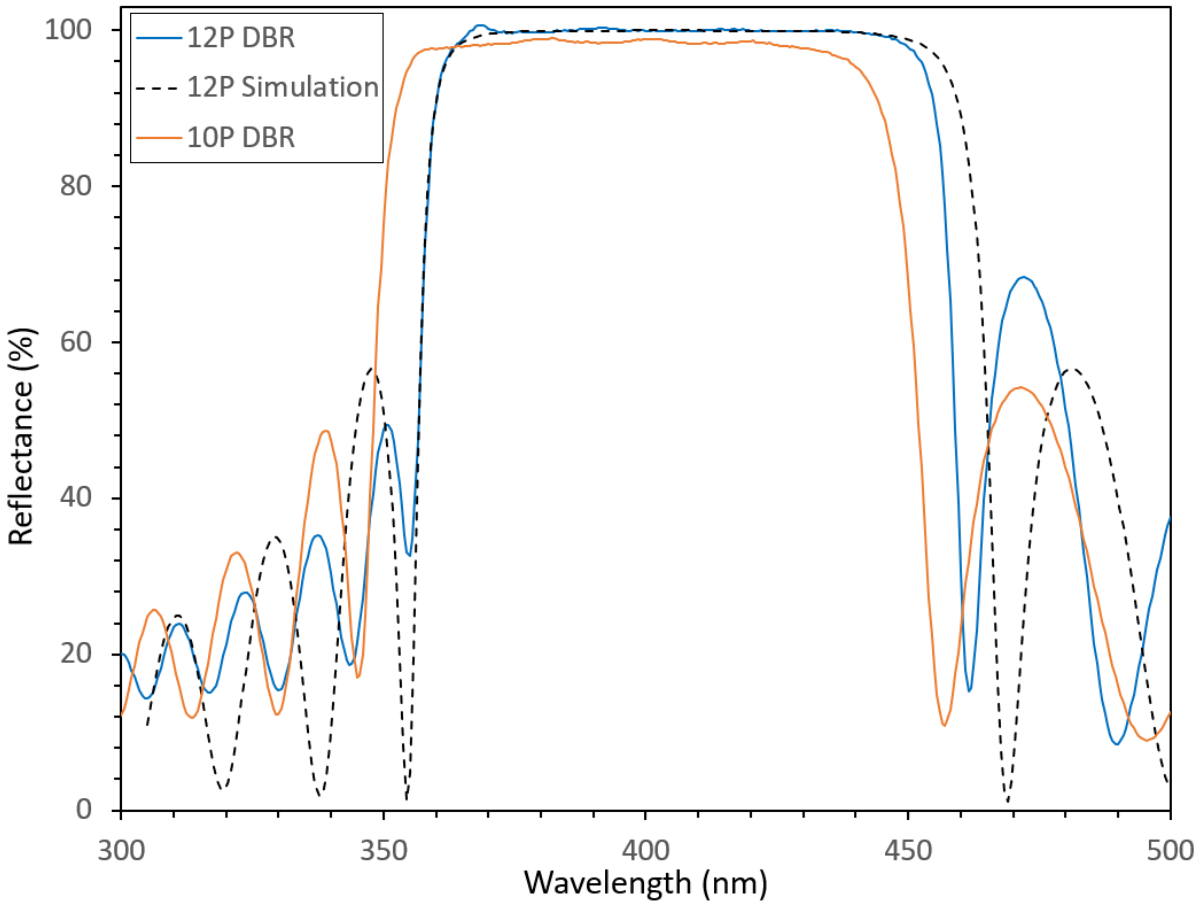


Figure 61. Reflectance spectra of a 12-period Ta_2O_5/SiO_2 DBR deposited using the improved IBD calibration method compared to the 10-period DBR that was deposited on the 13λ and 23λ VCSELs that failed to lase. The 12-period DBR had a higher peak reflectance and the reflectance stopband was centered at the target wavelength of 405 nm, which means that the improved IBD calibration method was successful.

The orange curve represents the reflectance spectra for the 10-period DBR that was deposited on the previous VCSELs that failed to lase, and the blue curve is the reflectance for the 12-period DBR that was deposited using the improved IBD calibration method. In comparison, the 12-period DBR had a higher peak reflectance and the reflectance stopband was centered at the target wavelength, which was closer to the simulation as shown by the dashed black curve. This showed that the improved IBD calibration method was successful. As mentioned earlier, the IBD deposition rate was found to vary based on the location of the sample during IBD deposition. This was accounted for during IBD deposition and samples were placed 5 mm away from the edge of the sample holder. The reflectance of the 12-period DBR was

measured at different locations on the wafer and the reflectance slightly varied based on the radial position of the wafer on the sample holder during IBD deposition. The peak reflectance was approximately 100%, 99.9%, 99.8%, and 99.6% for measured locations on the sample that were 5 mm, 7 mm, 9 mm, and 11 mm from the edge of the IBD sample holder, respectively. To verify that this was not caused by drift of the Cary 500 spectrophotometer, the original location (5 mm) was remeasured and again showed a reflectance of 100%.

The IBD deposition rate was also found to vary over time, which is why the IBD calibration method is necessary prior to DBR deposition. The drift in the IBD calibration rate was studied by depositing SiO_2 and Ta_2O_5 half-wave Fabry-Perot cavities on separate wafers using the same deposition times for each layer so that the pair of reflectance null wavelengths could be used to estimate the actual layer thicknesses. Then, another pair of SiO_2 and Ta_2O_5 half-wave Fabry-Perot cavities was deposited on separate sapphire wafers using the same deposition times as before, as shown in Figure 62.

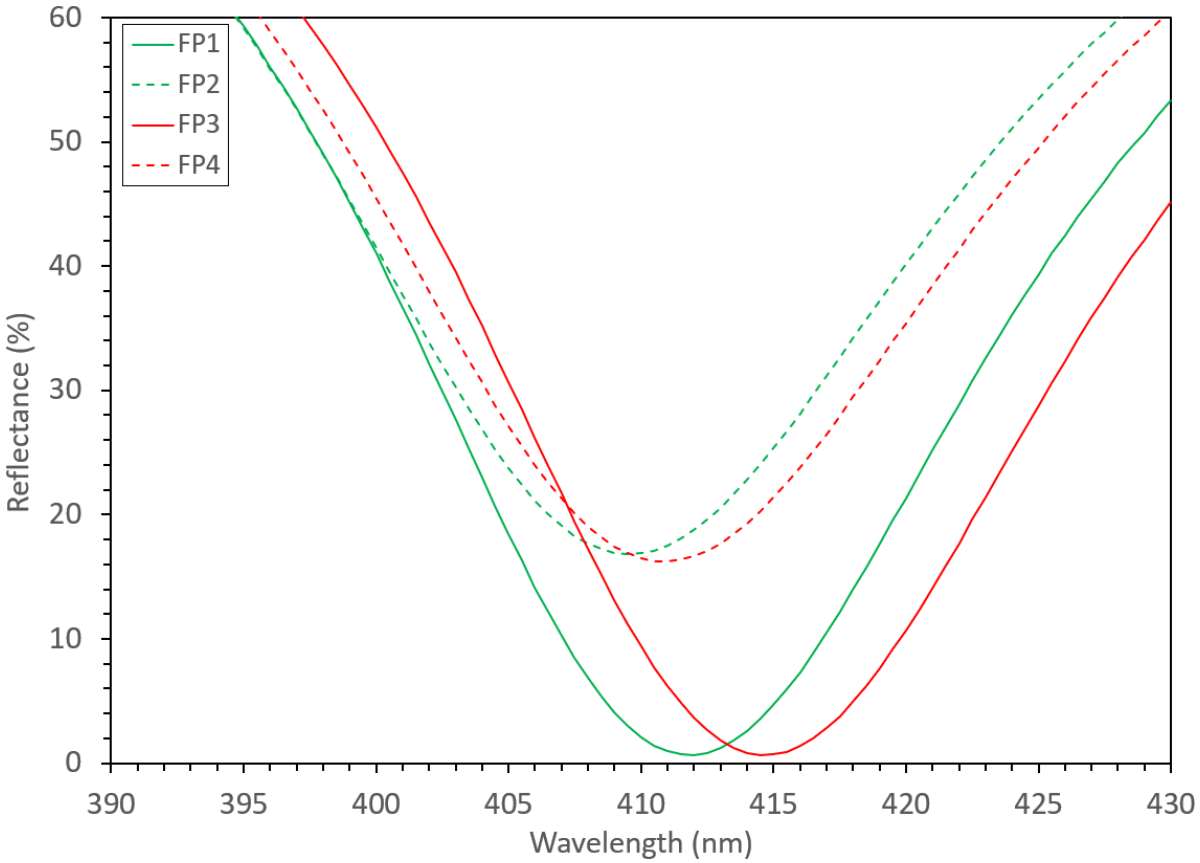


Figure 62. Reflectance spectra of SiO_2 and Ta_2O_5 half-wave Fabry-Perot (FP) cavities showing drift of the IBD deposition rate. The SiO_2 half-wave (*FP1*) and Ta_2O_5 halfwave (*FP2*) cavities were deposited on separate wafers, and then those exact recipes were used to deposit *FP3* and *FP4* to see if the IBD deposition rate changed. The IBD deposition rate appeared to increase over time as the reflectance null wavelengths redshifted for *FP3* and *FP4* compared to *FP1* and *FP2*.

The green curves show the initial pair of Fabry-Perot cavities that were deposited, which had reflectance null wavelengths of 412 nm for *FP1* and 409.5 nm for *FP2*. Using Equation (29) and (30), the IBD deposition rates were predicted to be 3.97 nm/min and 7.18 nm/min for SiO_2 and Ta_2O_5, respectively. The red curves show the 2nd pair of structures that were deposited using the same IBD recipe as *FP1* and *FP2*. The reflectance null wavelengths were 415 nm for *FP3* and 411 nm for *FP4*, which predict IBD deposition rates of 4.0 nm/min and 7.17 nm/min for SiO_2 and Ta_2O_5, respectively. This showed a slight drift of the IBD deposition rate after four 3-hour IBD depositions. Further experimentation would be necessary to

determine how the IBD deposition rate drifts over time, which may depend on other factors, such as the amount of remaining source material.

The pulsed *L-I-V* and emission spectrum were measured for the 13λ and 23λ VCSELs with the 12-period n-DBR. Despite the higher n-DBR reflectance using the improved IBD calibration method and more mirror periods (12-periods instead of 10-periods), none of the VCSELs were able to lase. This indicated that there was another source of loss in the VCSEL structures that prevented lasing. While the bottom-side p-DBR was deposited using the old IBD calibration method, it was not likely the issue because it had a high reflectance due to the higher number of mirror periods (16-periods). The most significant source of loss that prevented lasing turned out to be from surface roughness prior to the DBR deposition, as described in Section 4.4.3.

4.4.3. Surface Roughness Prior to DBRs

Surface roughness prior to the DBRs likely caused the most significant source of loss that prevented the 13λ and 23λ VCSELs from lasing. There was a high degree of roughness on the p-side of the devices due to the MBE TJ regrowth and there was also roughness on the n-side of the devices after the PEC undercut etch to remove the GaN growth substrate. Surface roughness is problematic for VCSELs because it leads to scattering loss and increases the threshold for lasing. Focused-ion beam (FIB) cross-section SEM images were taken of the failed VCSELs and revealed that the surface roughness can also affect the DBR mirror, as shown in Figure 63.

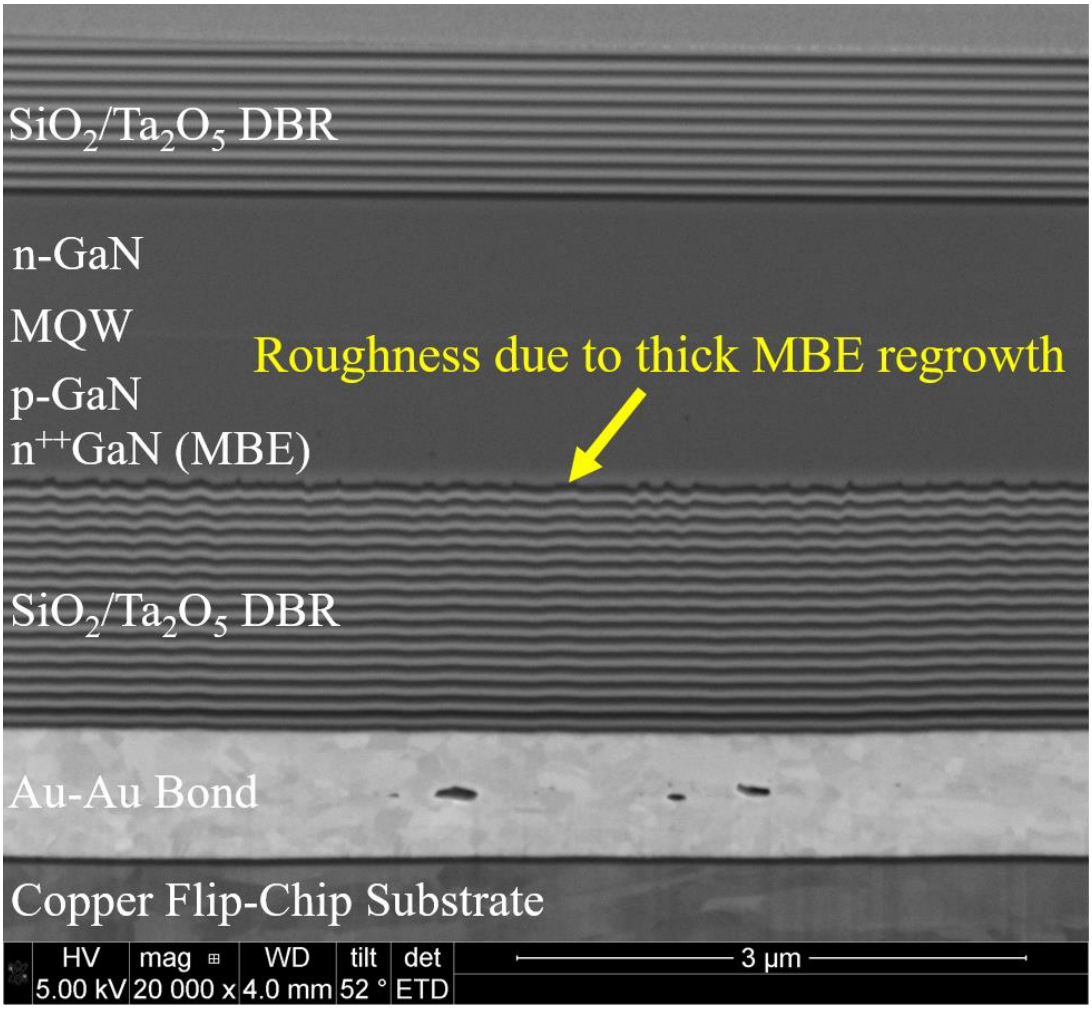


Figure 63. FIB cross-section SEM image of a 23λ VCSEL showing a rough morphology on the p-side due to the relatively thick 1642 nm MBE regrowth. This roughness prevented lasing due to scattering loss and reduced reflectivity of the bottom dielectric DBR as roughness propagated through the DBR layers.

Because IBD deposition of the DBR is conformal, the surface roughness propagated through several of the quarter-wavelength-thick SiO_2/Ta_2O_5 layers in the bottom p-side DBR. This causes further scattering loss and can also reduce the reflectivity of the DBR, which further inhibits lasing. The roughness shown in Figure 63 was due to the MBE TJ regrowth. The perspective of the image may seem confusing with roughness propagating downward through the bottom DBR, but this was because the FIB cross-section image was taken of the fully-processed VCSEL (i.e., after it was flipped upside down for flip-chip bonding). Prior to flip-

chip bonding, the p-side roughness was on the top surface and the p-DBR was deposited on top.

Ideally, the root mean square (RMS) surface roughness prior to DBR deposition should be less than 1 nm to minimize scattering loss for VCSELs;[167] however AFM scans revealed 6 nm RMS roughness on the p-side surface after the MBE TJ regrowth, as shown in Figure 64.

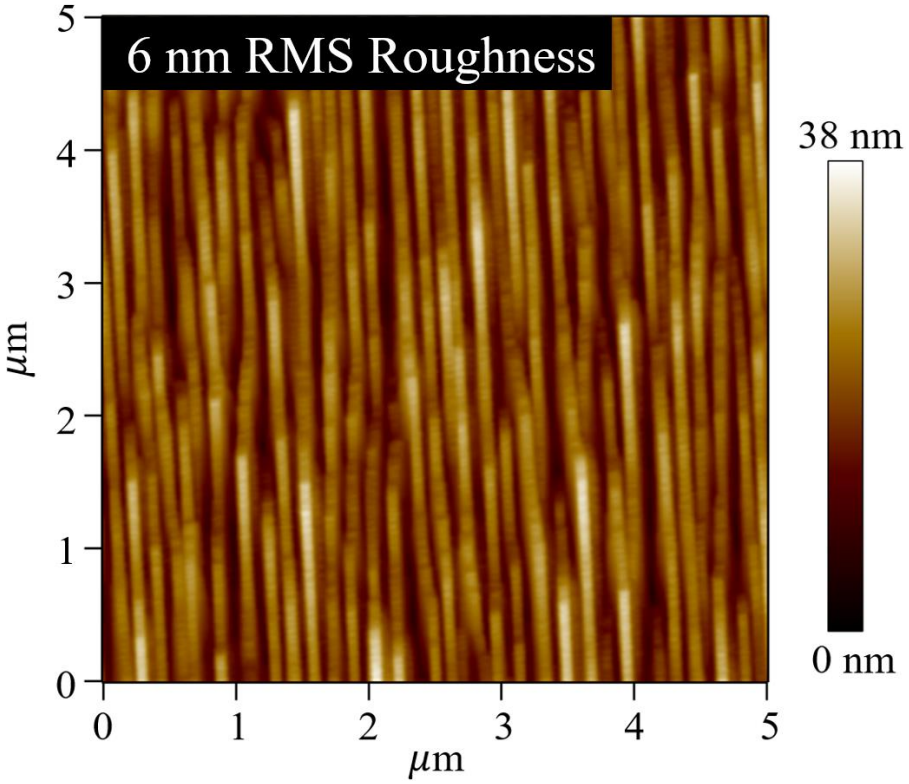


Figure 64. AFM scan after a relatively thick 1642 nm MBE TJ regrowth that led to a rough morphology with 6 nm RMS roughness prior to the p-DBR, which prevented the 23λ VCSEL from lasing due to scattering loss and reduced mirror reflectivity. The roughness consisted of striations oriented along the *c*-direction of the wurtzite crystal.

Based on scattering loss calculations for roughness prior to DBR deposition for VCSELs,[167] a scattering loss of over 90 cm^{-1} is predicted for 6 nm RMS roughness.[73] This is a significant amount of loss, considering the internal and mirror loss for a 7λ TJ VCSEL is estimated to be only ~14.1 cm^{-1}.[58] Furthermore, the scattering loss for 6 nm RMS roughness would be much

higher than 90 cm^{-1} if the correlation length of the roughness is not significantly smaller than the optical wavelength.[167] In addition to scattering loss, 6 nm RMS roughness is predicted to reduce the DBR mirror reflectance below 99% for short-range correlation lengths or below 98% for long-range correlation lengths.[167] Therefore, significant scattering loss and reduced mirror reflectivity due to surface roughness likely explains why these VCSELs were unable to reach the threshold for lasing. The surface morphology of the MBE regrowth was similar in different areas throughout the samples and consisted of striations oriented along the *c*-direction of the GaN wurtzite structure. Note that the MBE surface roughness is visible in the FIB cross-section image in Figure 63 because the cross-section was oriented along the *a*-direction of the device (i.e., perpendicular to the *c*-oriented striations in Figure 64). FIB cross-section images taken along the *c*-direction of devices did not show roughness on the p-sides of devices, as shown in Figure 65.

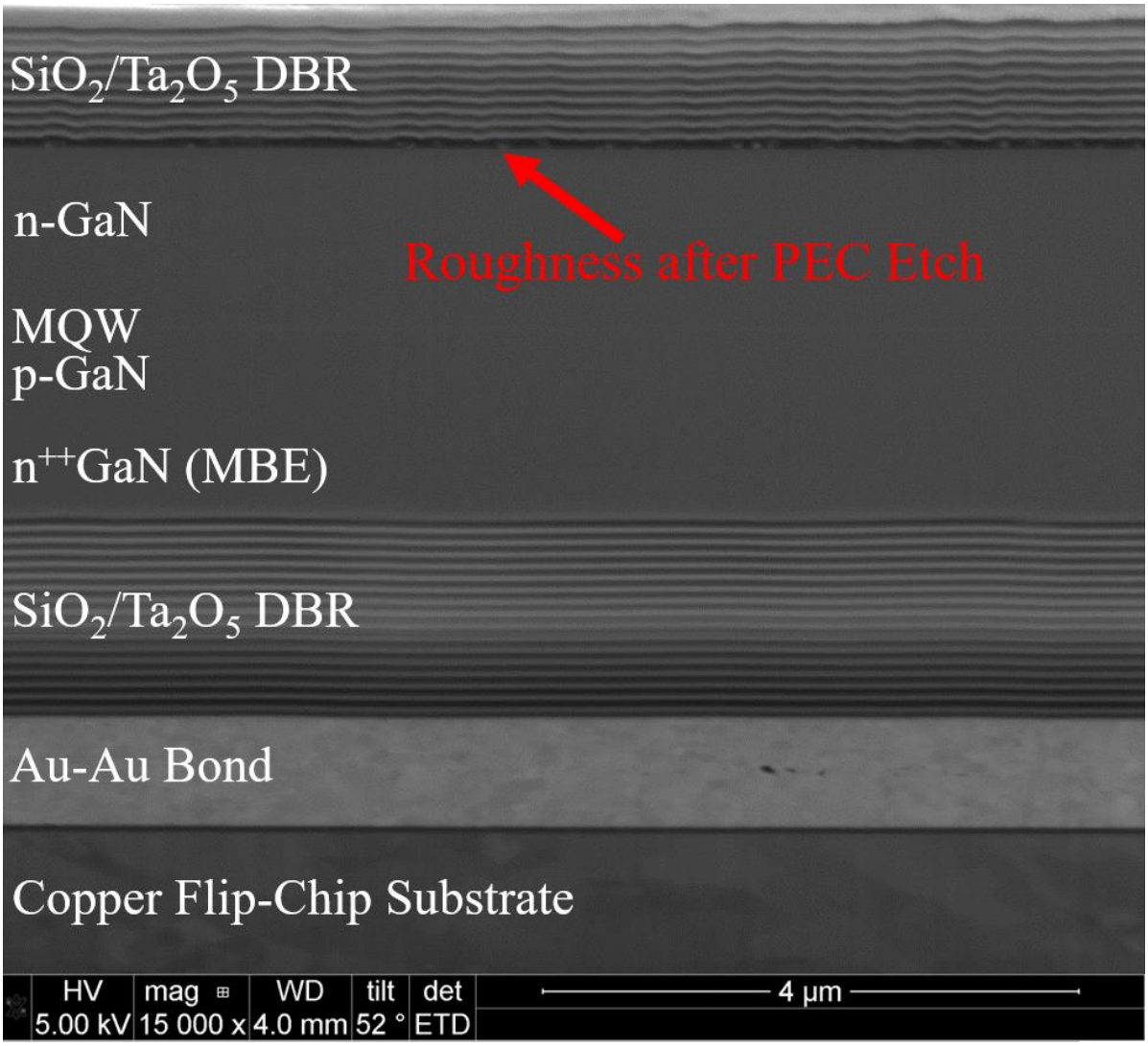


Figure 65. FIB cross-section SEM image of a 23λ VCSEL showing roughness on the n-side due to the PEC undercut etch to remove the growth substrate. The p-side roughness was not observable in this image because the FIB cross-section was taken parallel to the rough striations along the *c*-direction.

Although the p-side roughness is not visible, Figure 65 shows roughness on the n-side of the device which also propagated through the top DBR. This roughness appeared after the PEC undercut etch of the sacrificial MQW to remove the *m*-plane GaN growth substrate. Unlike the regular roughness from the MBE regrowth, the n-side surface roughness varied significantly across devices, as shown in Figure 66.

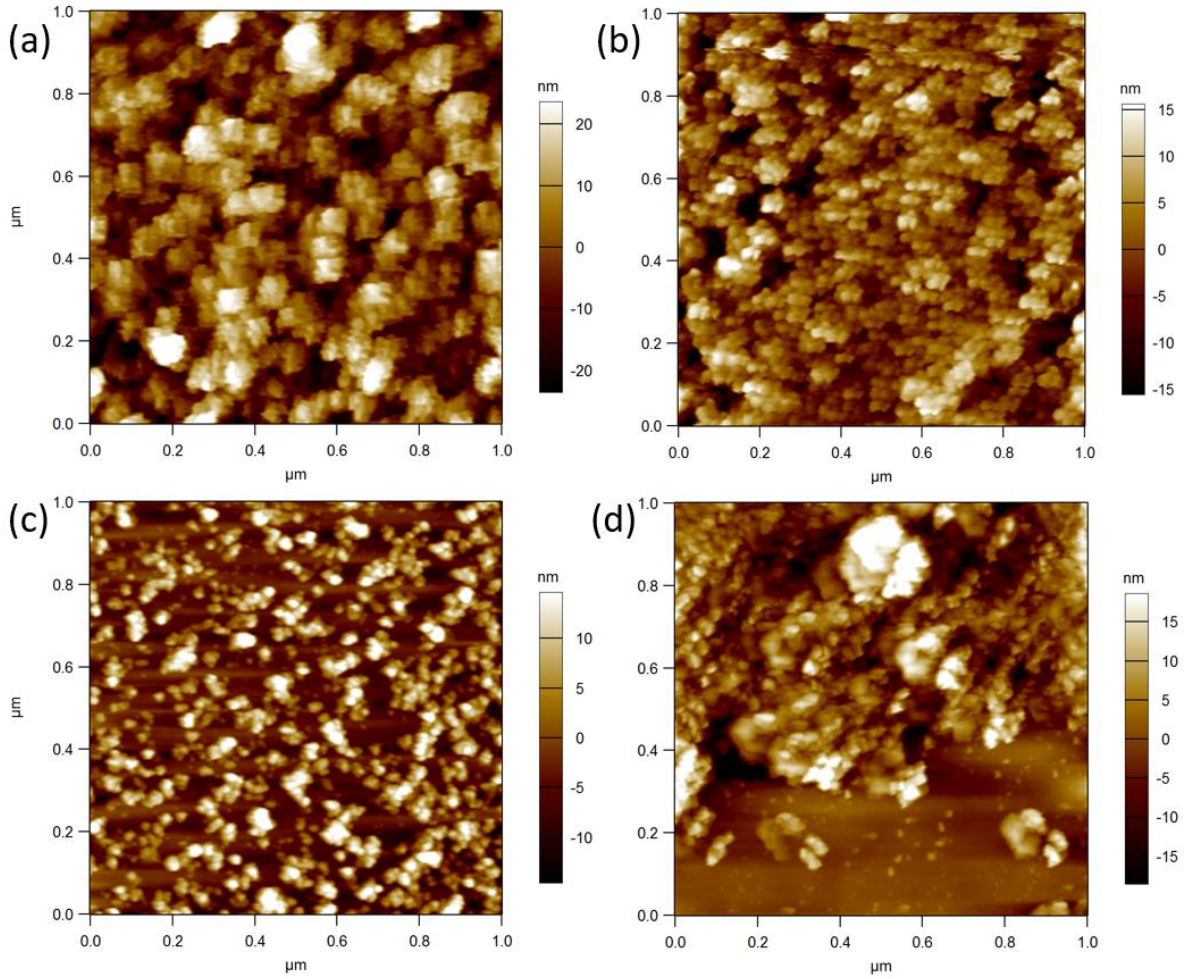


Figure 66. AFM images of the n-side roughness after the PEC undercut etch to remove the GaN growth substrate, showing RMS roughness values of (a) 10.8 nm, (b) 6.0 nm, (c) 6.3 nm, and (d) 7.4 nm. Unlike the roughness from the MBE regrowth, the morphology after PEC etching was non-uniform with varying degrees of roughness.

The RMS roughness on the n-side after PEC undercut etching ranged from 6 nm to 12 nm. As discussed earlier, this would cause significant scattering loss and reduced mirror reflectivity, which further explains why these VCSELs were unable to lase.

Knowing that surface roughness was a significant problem for previous VCSELs, the next step was to identify the cause of the roughness and develop methods to create a smoother surface morphology. Section 4.4.4 describes MBE TJ regrowth experiments that were conducted to smoothen the growth surface, and Section 4.4.5 discusses experiments to create a smoother morphology after PEC etching.

4.4.4. MBE TJ Growth Experiments

The most significant source of loss that prevented lasing for the 13λ and 23λ VCSELs was due to surface roughness prior to the DBRs that caused significant scattering loss and reduced DBR mirror reflectivity. There was 6 nm RMS roughness on the p-side of devices, which was due to the MBE TJ regrowth. The next step was to identify the cause of the rough surface and then develop methods to smoothen the morphology. Surface roughness did not seem to be a problem for previously reported TJ VCSELs,[58] but unfortunately, the degree of surface roughness on the p-side was not measured for those devices. The MBE regrowth conditions were very similar in both cases, but the main difference was that the failed 13λ and 23λ VCSELs had much thicker MBE regrowths (1642 nm compared to 141 nm). This led to a series of MBE regrowth experiments to see if smoother surfaces could be grown by decreasing the regrowth thickness or by varying other growth conditions.

In order to prepare samples for the MBE regrowth experiments, MOCVD growth was performed on *m*-plane GaN substrates with the same epitaxial structure as previously reported TJ VCSELs,[58] and then the samples were annealed at 600 °C for 15 minutes for p-GaN activation. Prior to MBE regrowth for n^{++}GaN, the top surface of the samples consisted of 14-nm-thick p^{++}GaN. One difference compared to the actual VCSEL samples was that Al ion implantation was not performed, which makes these samples similar to the growth morphology within the aperture of VCSEL devices (i.e., VCSEL apertures are protected with a metal hardmask during ion implantation). After performing an aqua regia treatment to remove indium contacts that were used for EL characterization, the samples were solvent cleaned and baked in the ammonia (NH_3) MBE chamber at 400 °C for one hour in vacuum (NH_3 pressure ~ 1×10^{-6} Torr) prior to MBE regrowth. With help from E. Young, a series of

MBE TJ regrowths were performed with the goal of smoothening the regrowth surface morphology, and four samples were grown with different MBE growth conditions. The 1st sample had a 40-nm-thick n^{++}GaN MBE regrowth performed at 710 °C with an approximate Si concentration of 1.1×10^{20} cm^{-3}, and a representative AFM image of the resulting roughness is shown in Figure 67.

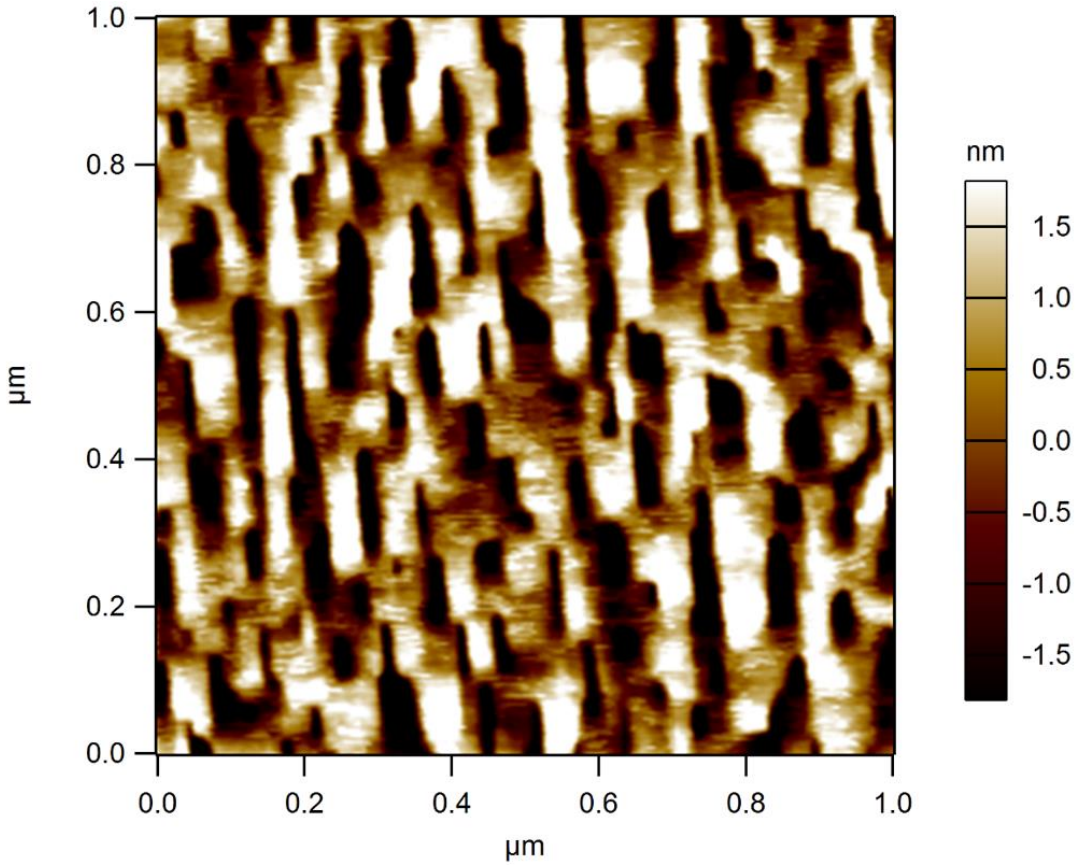


Figure 67. AFM image showing 1.8 nm RMS roughness for a sample that had a 40-nm-thick n^{++}GaN MBE regrowth performed at 710 °C.

The RMS roughness was ~1.8 nm for a 1 µm × 1 µm AFM scan and ~1.3 nm for a 5 µm × 5 µm AFM scan. This was much smoother than the 6 nm RMS roughness on the failed VCSEL devices, which was attributed to the thinner MBE regrowth (40 nm compared to 1642 nm). Although the surface was smoother, the morphology was very similar with striations oriented in the *c*-direction of the wurtzite crystal structure. These trenches had a depth of ~14 nm and

were spaced between 30 nm and 80 nm apart. The lower RMS roughness from the 5 μm × 5 μm AFM scan may have been a result of the AFM tip not being able to resolve the full depth of the trenches compared to the relatively slow 1 μm × 1 μm scan. The next step was to modify the growth conditions to see if smoother surfaces can be produced for the 2nd regrowth sample.

Smoother growth surfaces have been obtained by implementing higher MBE growth temperatures[168] and by utilizing an In surfactant during growth.[169] Based on those findings, the 2nd MBE regrowth sample was grown at a higher temperature of ~750 °C with a non-incorporating indium surfactant (indium flux ~ 4×10^{-8} Torr). All other conditions were identical to the 1st sample and the MBE regrowth thickness was ~40 nm. Figure 68 shows the surface morphology of the 2nd MBE regrowth sample.

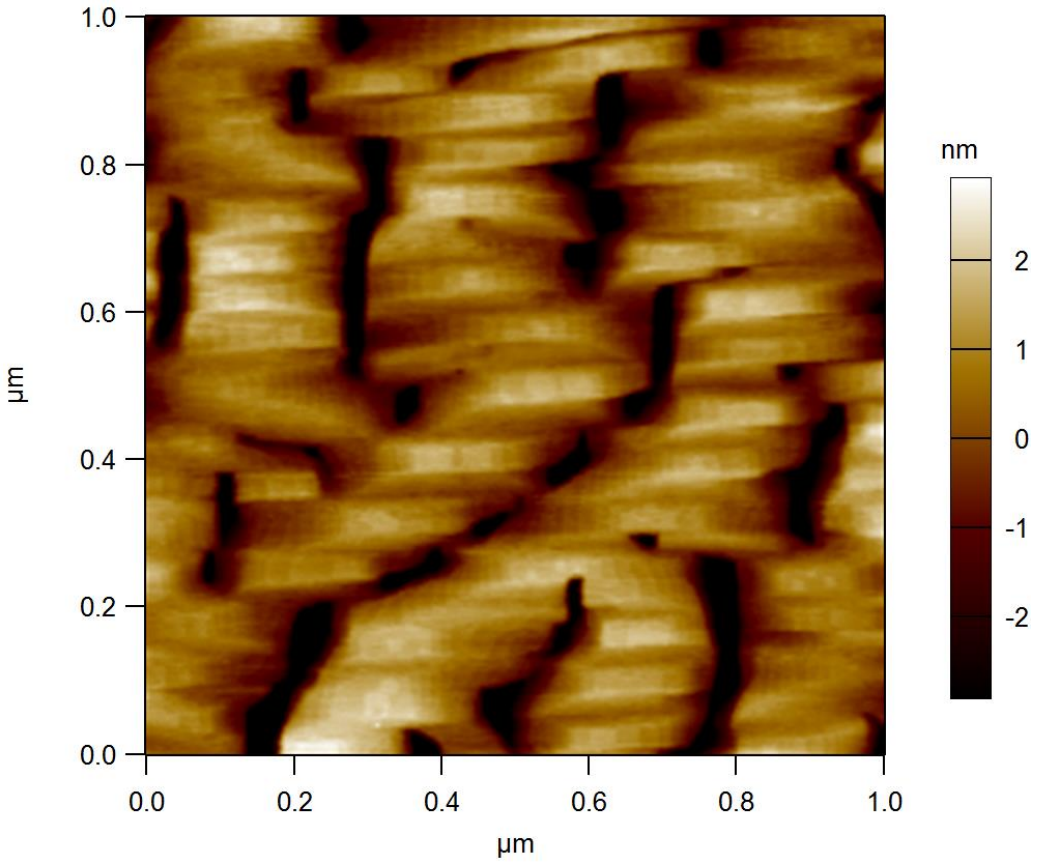


Figure 68. AFM image showing 1.4 nm RMS roughness for a sample that had a 40-nm-thick n^{++}GaN MBE regrowth performed at 750 °C with a non-incorporating indium surfactant.

The RMS roughness was ~1.4 nm for a 1 µm × 1 µm AFM scan and ~1.2 nm for a 5 µm × 5 µm AFM scan. Increasing the MBE growth temperature and utilizing an indium surfactant decreased the RMS roughness by ~22% and produced a ~10× larger the spacing between ~10-nm-deep trenches (~200-300 nm) compared to the 1st MBE regrowth sample. This was an expected change in surface morphology as the indium surfactant increases the adatom diffusion length, especially at these relatively low growth temperatures where indium has a longer surface residence time prior to desorption.

While the 1st and 2nd MBE regrowth samples had relatively thin regrowths of 40 nm, the next step was to apply the improved growth conditions to grow the full regrowth structure that would be used in a VCSEL. Using the same MBE growth conditions as the 2nd

sample (growth temperature of 750 °C and utilizing an indium surfactant), the 3rd sample had a 141-nm-thick MBE regrowth consisting of n^{++}GaN/n-GaN/n^{++}GaN (39.6/61.7/39.6 nm) with respective Si concentrations of 1.1×10^{20}, 2.5×10^{18}, and 1×10^{19} cm^{-3}. The MBE regrowth surface morphology is shown in Figure 69.

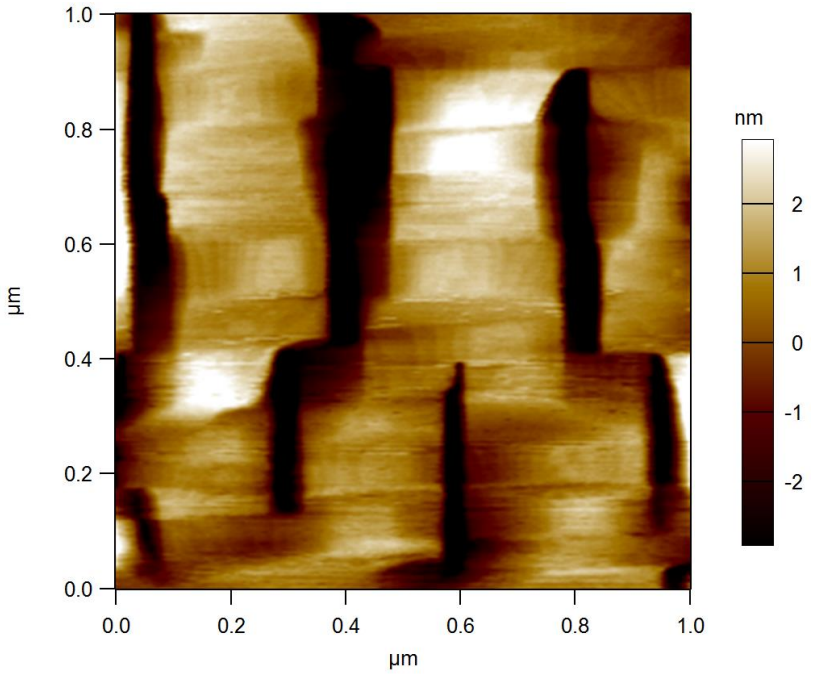


Figure 69. AFM image showing 2 nm RMS roughness for a sample that had a 141-nm-thick n^{++}GaN MBE regrowth performed at 750 °C with a non-incorporating indium surfactant.

The RMS roughness was ~2.0 nm for a 1 µm × 1 µm AFM scan and ~2.1 nm for a 5 µm × 5 µm AFM scan. As expected, the thicker 141-nm MBE regrowth had a slightly rougher morphology compared to the 40-nm thick regrowths. The trenches were somewhat deeper with a depth ~12 nm with a spacing ranging between 250-350 nm. The 4th MBE regrowth sample was also 141-nm-thick, but a slower growth rate was implemented with a lower Si doping to see if a smoother surface could be produced. However, the morphology was nearly identical to the 3rd sample in terms of RMS roughness, trench depth, and trench spacing. Obtaining smooth surfaces after MBE growth is particularly difficult due to this growth orientation. While *m*-plane with a -1° intentional miscut toward the *c*-direction is

ideal for MOCVD growth and can produce subnanometer RMS roughness, this is a suboptimal miscut for MBE growth. One solution to this problem could be to use growth planes that are optimal for MOCVD and MBE, such as semipolar orientations. Although < 1 nm RMS roughness would be ideal for VCSELs, 2 nm RMS is significantly improved compared to the 6 nm RMS roughness on the failed VCSEL samples. These improved MBE growth conditions (higher growth temperature with indium surfactant) were applied to the VCSELs described in Section 4.5.

4.4.5. PEC Etching Experiments

In addition to the MBE regrowth roughness on the p-side, the 13λ and 23λ VCSELs that failed to lase also had roughness on the n-side of the devices prior to the top DBR deposition. This roughness ranged from 3-12 nm RMS roughness and appeared on the uppermost n^{++}GaN surface after the PEC undercut etch of the sacrificial MQW to remove the growth substrate, as illustrated in Figure 70.

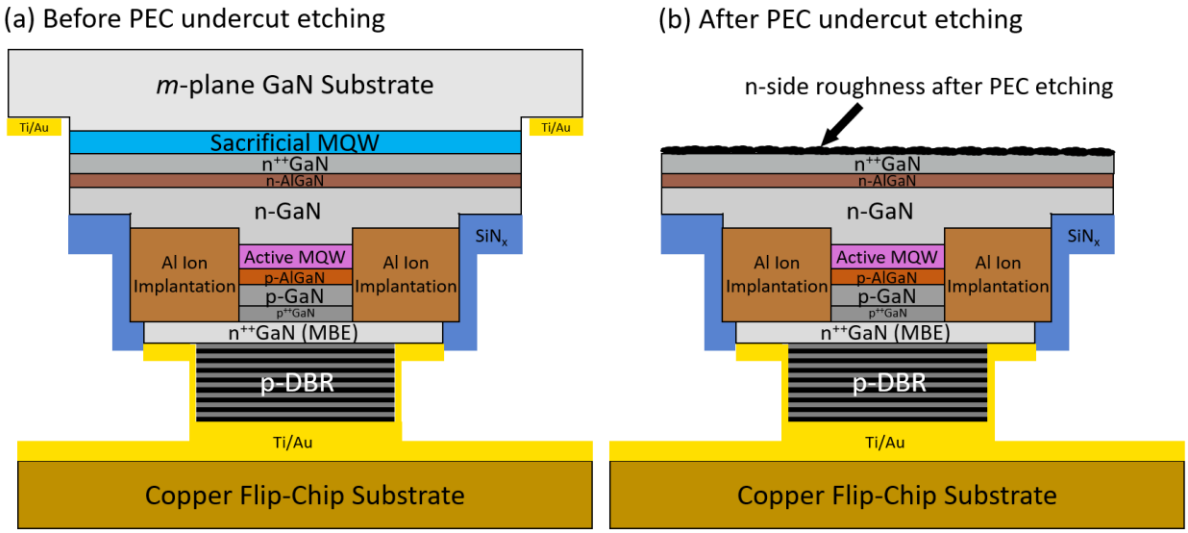


Figure 70. (a) Schematic of the partially-processed VCSEL structure after flip-chip bonding to a submount and prior to the PEC undercut etch of the sacrificial MQW to remove the GaN growth substrate. (b) Schematic structure after the GaN substrate was removed via PEC undercut etching, which produced a rough surface morphology on the n-side of the devices ranging from 3-12 nm RMS roughness.

Figure 70(a) shows a schematic of the partially-processed VCSEL structure after flip-chip bonding and before the PEC undercut etch. Figure 70(b) shows the structure after the GaN substrate was removed via PEC etching, which resulted in a rough morphology on the n-side of the devices ranging from 6-12 nm RMS roughness.

This led to several PEC etching experiments with the goal of achieving a smoother surface morphology. Motivated by previously reported experiments that produced smoother surfaces by lowering the KOH concentration during PEC etching,[127] a PEC etching experiment was conducted using various KOH concentrations to see its effect on the resultant surface roughness. The standard PEC etching procedure used a 405 nm LED array for above-bandgap illumination of the sacrificial MQW and a 1 M KOH solution. During this process, photogenerated holes in the sacrificial MQW assist in oxidation and the surface oxide subsequently dissolves in the KOH solution as the etch progresses laterally. The 405 nm illumination should only generate electron-hole pairs within the sacrificial MQW and the active MQW, but the active MQW is protected by SiN_x (or ion implantation) so only the sacrificial MQW should etch. However, it is possible for KOH to cause chemical-related roughening of GaN, particularly for the N-face of *c*-plane GaN. Although *m*-plane GaN is much more resistant to chemical-related roughening, this was a possible explanation for roughness on the n-side of the devices after PEC etching. If the roughness was due to chemical roughening in KOH, lowering the KOH concentration could reduce this effect to produce a smoother surface. However, as described in the following PEC experiments and roughness characterization, it was found that the n-side roughness was not due to chemical roughening in KOH. While the rough surface after PEC etching was initially presumed to be roughened n-GaN, further characterization revealed that this was not the case. The first PEC etching

experiment showed an unexpected result in which reducing the KOH concentration did not decrease the roughness after PEC undercut etching, as shown in Figure 71.

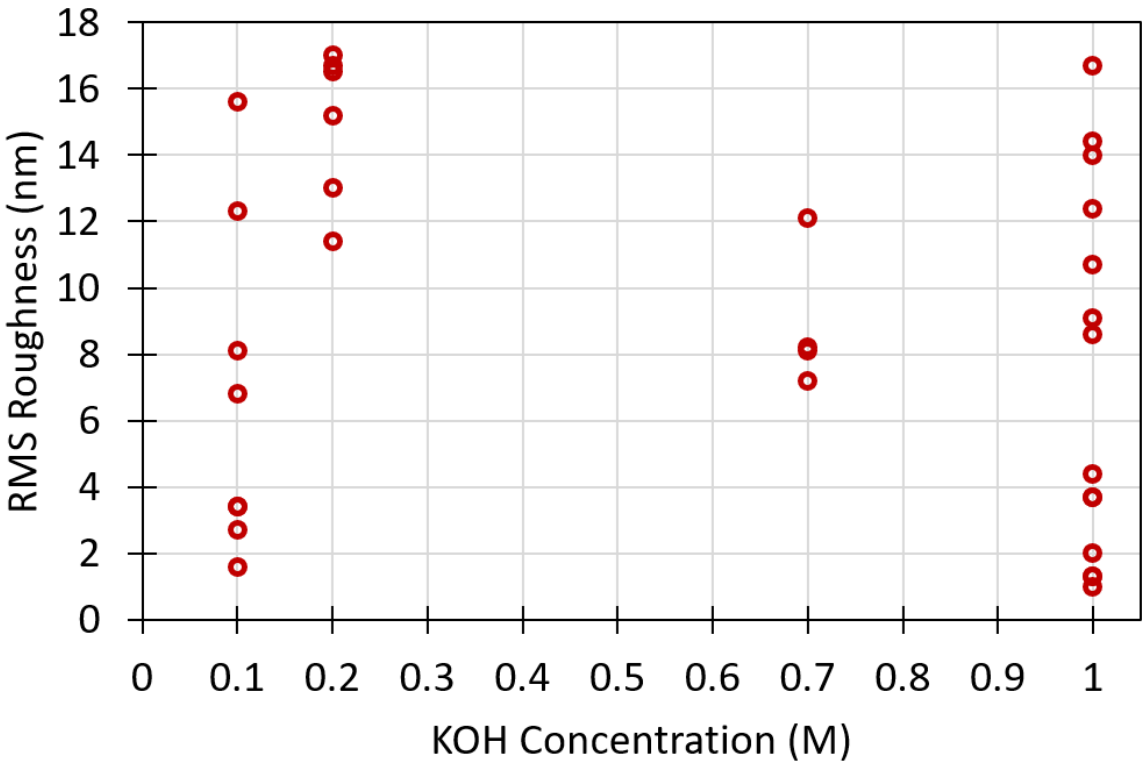


Figure 71. Plot of n-side RMS roughness versus KOH concentration used during PEC etching of a sacrificial MQW for *m*-plane GaN substrate removal. AFM was used to measure the RMS roughness of the n^{++}GaN surface directly after PEC etching.

Unlike the previously-reported results,[127] there was no apparent trend between KOH concentration and surface roughness after PEC etching. RMS roughness values varied between ~2-17 nm for samples that were PEC etched using 1 M KOH as well as for samples that used 0.1 M KOH. For a total of nine samples, each data point corresponds to the RMS roughness of an individual AFM scan. Four samples were etched in 1 M KOH, one sample in 0.7 M KOH, two samples in 0.2 M KOH, and two samples in 0.1 M KOH. If the roughness was due to chemical-related roughening of GaN in KOH, it would be expected for the roughness to decrease when using lower concentrations of KOH, but this trend was not

observed. There was also no clear trend between PEC etching time and RMS roughness, as shown in Figure 72(a).

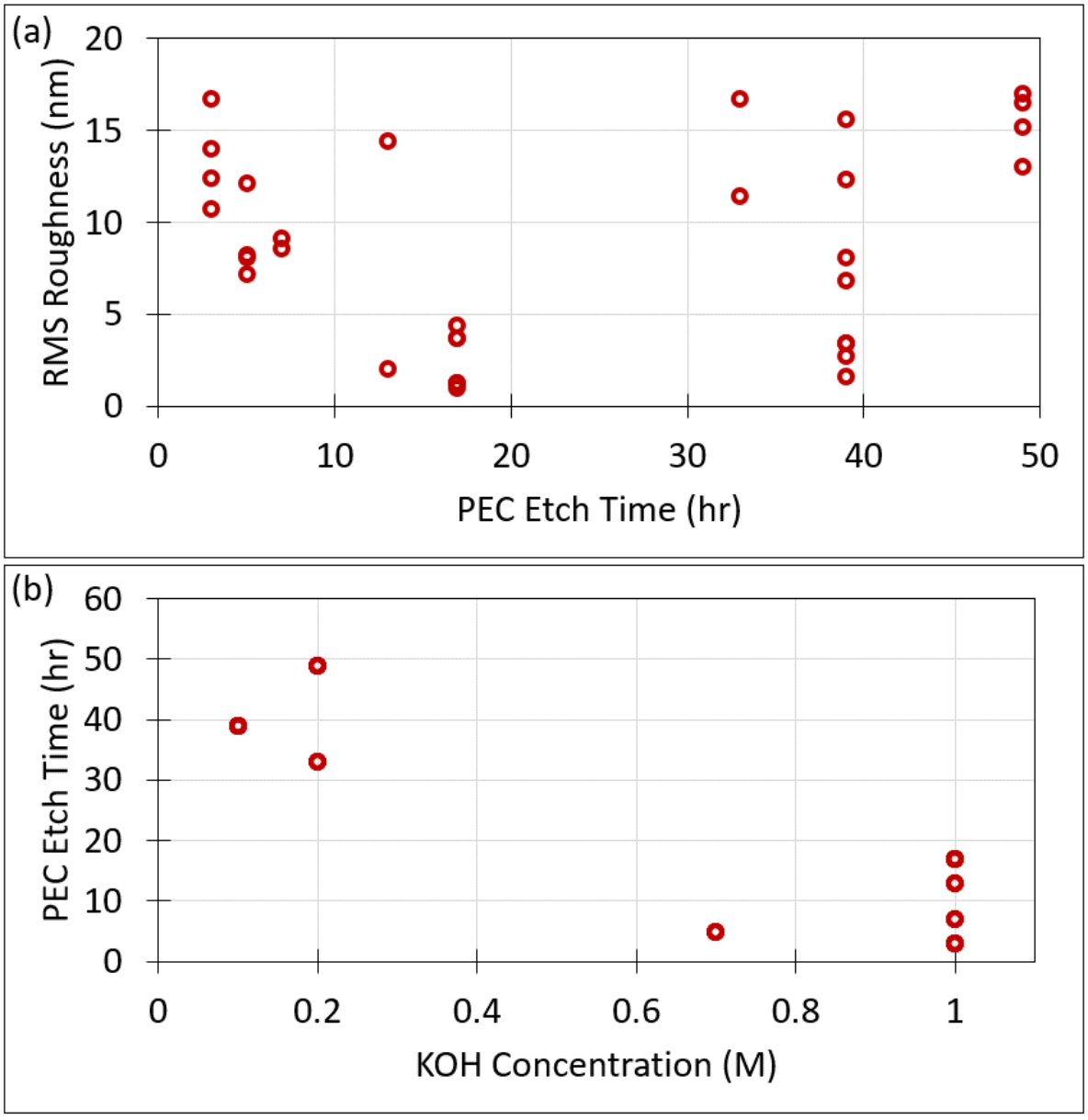


Figure 72. (a) RMS roughness after PEC undercut etching versus total PEC etching time in hours, showing no clear trend. (b) PEC etching time versus KOH concentration, showing that lower KOH concentrations typically take longer for the PEC undercut etch to complete.

Though, as expected, there did seem to be a trend showing that lower KOH concentrations generally required longer PEC etching times, as shown in Figure 72(b). The PEC etching time was defined as the number of hours elapsed until the sacrificial MQW was fully etched,

allowing the GaN growth substrate to be removed with very little force (e.g., using a water jet from a pipette). Under 405 nm LED array illumination, the sacrificial MQW emitted ~420 nm light, which could be observed using ultraviolet-blocking safety glasses during PEC etching to determine when the PEC etching was complete and the GaN growth substrate would no longer be attached to the device. Though, note that the GaN substrate would still be positioned face-down on the flip-chip substrate. Figure 73 shows a photograph of a partially-processed VCSEL sample during PEC undercut etching to remove the *m*-plane GaN growth substrate.

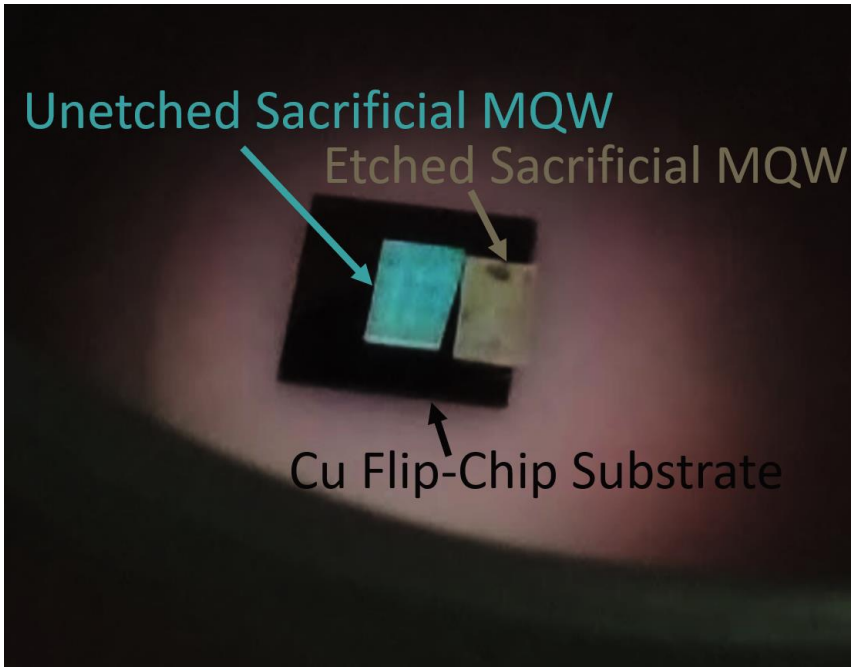


Figure 73. Photograph of a flip-chip bonded sample during growth substrate removal using PEC undercut etching in 1 M KOH and illumination from a 405 nm LED array. The dark-colored square is the copper flip-chip substrate and the GaN chip in its center is flip-chip bonded face-down. The sacrificial MQW emits greenish light due to photoluminescence from the 405 nm LED array. For comparison, a GaN sample that was previously lifted-off via PEC etching was placed to the right of the bonded sample, which shows no greenish emission because its sacrificial MQW was previously etched. Note that this photograph was taken through glasses that filter UV and violet light, which is why the image does not appear violet from the 405 nm LED array.

The dark-colored square is the copper flip-chip substrate and the rectangle in its center is the flip-chip bonded GaN chip that emits greenish light ($\lambda \sim 420$ nm) due to fluorescence of the sacrificial MQW. For comparison, a GaN sample that was previously PEC-etched is shown on the right side and shows that greenish light no longer emits once PEC etching is complete.

Once the greenish light was no longer visible (indicating the PEC etch was complete), a pipette was used to generate a gentle stream of KOH solution toward the sample, which would usually cause the GaN growth substrate to move away and reveal the n-side of the device, as shown in Figure 70(b). Note that the PEC etching time may not be exactly the same amount of time needed for the sacrificial MQW to be completely etched. The greenish light fluorescing from the sacrificial MQW was difficult to observe for some samples and occasionally the pipette was ineffective at removing the GaN substrate even when the sacrificial MQW appeared to be completely etched, which either required further PEC etching or using tweezers to gently remove the GaN substrate. In general, there was a clear trend that PEC etching could be completed within a single day using KOH concentrations of 0.7 M and 1 M, but lower KOH concentrations of 0.1 M and 0.2 M would require at least 30 hours. However, there was no trend in terms of PEC etching time and roughness and varying the KOH concentration was not able to solve the roughness problem on the n-side of the devices.

Further experimentation was necessary to solve the n-side roughness problem, but at this point, there were very few remaining samples that could be used for PEC etching experiments. Fabricating VCSEL samples that are ready for PEC etching is a particularly extensive process as it requires completing six out of the eight photolithography steps in the VCSEL process and involves several time-consuming steps (e.g., 8 MOCVD growth calibrations, shipping samples for ion implantation, MBE regrowth, DBR calibration and deposition, etc.). Therefore, it would have been impractical to create another set of nearly-complete VCSEL samples that would likely fail during the PEC etching experiments due to roughness on the n-side. This led to designing test structures that could be used for PEC etching experiments with the goal of solving the n-side roughness problem

The most important design goal for the PEC test structures was that they needed to closely resemble the VCSEL structure so that PEC etching would produce the same type of roughness on the n-side. Another goal was to simplify the fabrication process so that it would be easy to create an abundant supply of samples that could be used for PEC etching experiments. Based on these goals, the PEC test structures were created as follows. While the actual VCSEL samples are flip-chip bonded face-down to a submount prior to PEC etching, this would not be necessary for the PEC test structures, so the fabrication process could be simplified. The epitaxial structure was also simplified, and the order of the epitaxial layers near the sacrificial MQW were reversed because the flip-chip bonding step was omitted (i.e., to measure the roughness of the n^{++}GaN layer after PEC etching without flip-chip bonding, the n-AlGaN, n^{++}GaN, and sacrificial MQW regions were grown in the reverse order compared to the VCSEL epitaxy epitaxial structure). MOCVD growth for the PEC test samples was performed on *m*-plane GaN substrates with an epitaxial structure consisting of a 600 nm n-GaN template, 15 nm n-AlGaN, 50 nm n^{++}GaN, a sacrificial layer for PEC etching (InGaN/GaN MQW or single QW), and 200 nm n-GaN. The sacrificial layer structure was varied among four samples to study its effect on roughness after PEC etching. Three samples were grown with different sacrificial MQWs and one sample was grown with a sacrificial single QW. After MOCVD growth, the samples were characterized by photoluminescence (PL). Table 3 summarizes the sacrificial layer structure, MOCVD growth temperature, PL wavelength, and relative PL intensity for each of the samples.

Table 3. Sacrificial layer structure, MOCVD growth temperature, and photoluminescence (PL) wavelength and intensity for the test samples fabricated for PEC etching experiments.

Sample	QWs (#)	QW Thickness (nm)	Barrier Thickness (nm)	Growth Temperature (°C)	PL λ (nm)	PL Intensity (Counts)
A	3	9	4	820	411	41770
B	3	9	4	805	424	16548
C	3	13	2.5	820	412	49206
D	1	9	N/A	820	405	21577

In addition to these samples, a 5×MQW sample was grown to measure the MOCVD growth rates to determine the QW and barrier thicknesses. Sample A was grown using the standard sacrificial MQW growth recipe that was used for previous VCSELs. Note that while the sacrificial MQW has previously consisted of 7 nm QWs and 5 nm barriers,[127] the thicknesses were somewhat different for these samples because XRD calibration was not performed prior to growth. Also note that since C. Holder's initial *m*-plane GaN VCSEL design, XRD calibrations have not typically been performed for the sacrificial MQW because slight variations in QW or barrier thickness have not seemed to affect the PEC undercut etch (and because variations in sacrificial MQW thickness does not affect the VCSEL cavity length). While the growth temperature for the InGaN regions was 820 °C for most of the samples, an 805 °C growth temperature was chosen for Sample B to see if increased indium content of the MQW affected roughness after PEC etching. The thickness of the MQW was varied for Sample C, and Sample D consisted of a 9-nm-thick single QW instead of a MQW. While Sample A and C had similar PL emission wavelengths of 411 and 412 nm, the increased indium content in Sample B caused a redshift in emission wavelength to 424 nm. Likely due to the thinner active region with a single QW, Sample D had a shorter emission wavelength of 405 nm.

While the VCSEL fabrication process involves six photolithography steps prior to PEC etching, this was simplified to two photolithography steps for the PEC test samples. In the 1st photolithography step (SPR 220-3.0 using the *Mesa 2* mask during exposure), the

sidewall of the sacrificial MQW was exposed by dry etching a ~600-nm-deep mesa using RIE. The mesas had the same lateral geometry as the ones defined by the dry etch to expose the sacrificial MQW in the VCSEL design. The 2nd photolithography step (nLOF2020 using the *Intracavity Metal* mask during exposure) involved depositing Ti/Au (20/1000 nm) using electron beam evaporation to produce the same geometry as the flip-chip bonding metal and PEC cathode as the VCSEL design. After fabrication of the PEC test structures, small pieces were cleaved to use for PEC etch experiments, as shown in Figure 74.

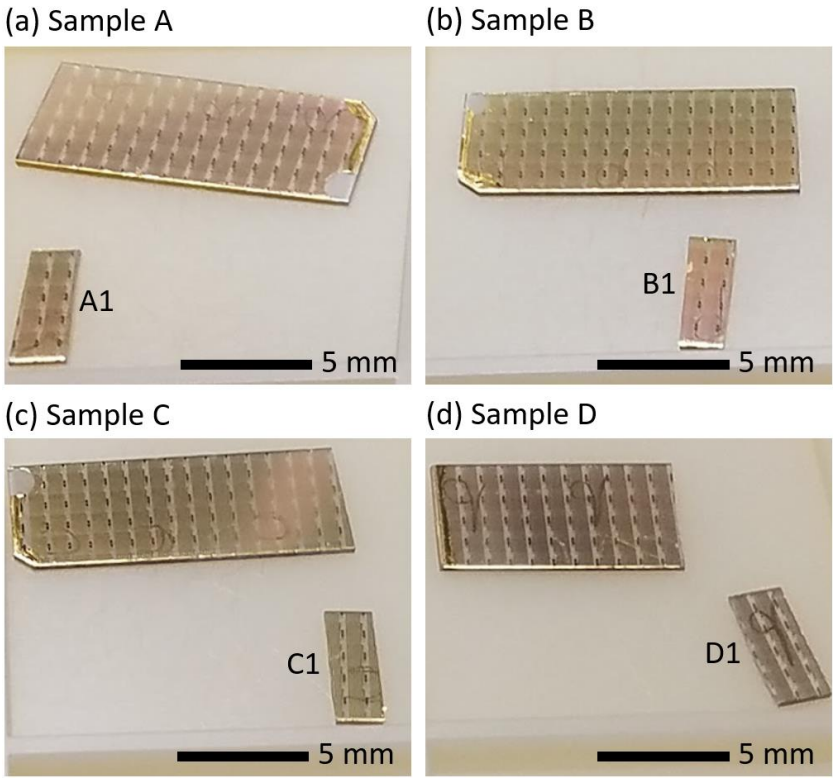


Figure 74. Photographs of the fabricated PEC test structures for (a) Sample A, (b) Sample B, (c) Sample C, and (d) Sample D. Small pieces were cleaved to use as samples for PEC etch (Samples A1, B1, C1, and D1).

A schematic illustration of the PEC test structure design is shown in Figure 75(a).

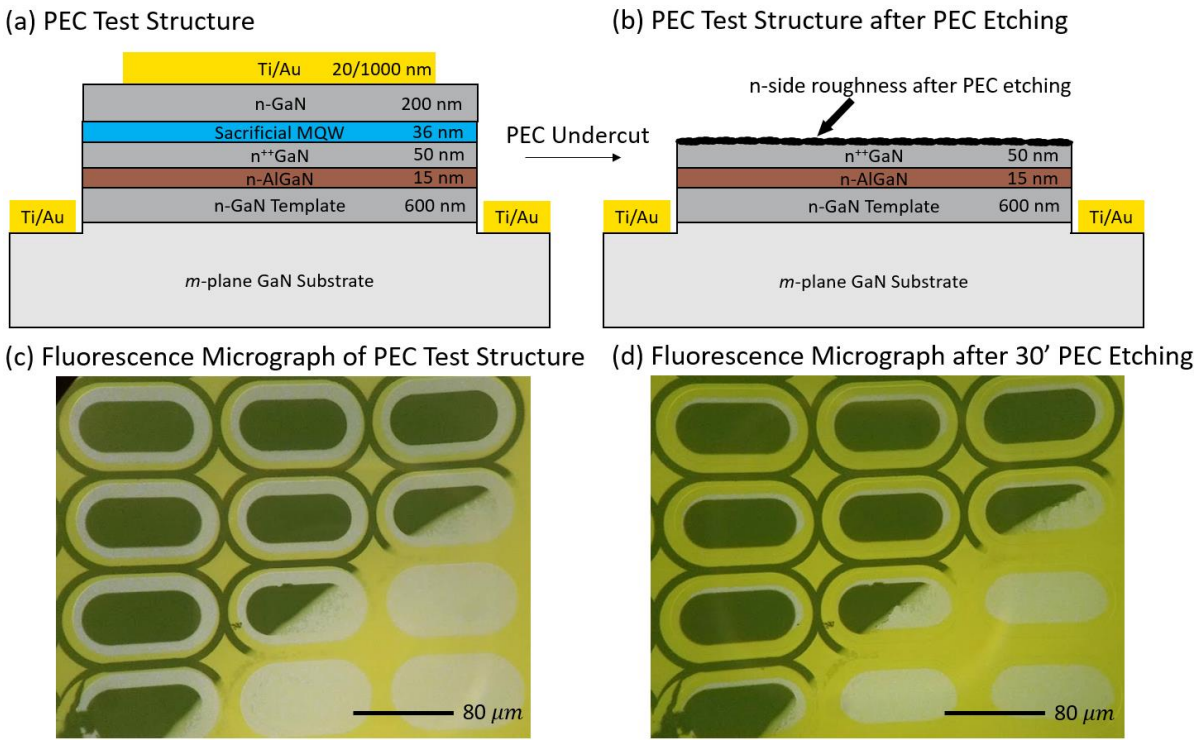


Figure 75. (a) Schematic illustration of the test structures created for PEC etching experiments to solve the roughness problem that occurs on the n-side of devices. (b) Schematic of the test structure after PEC etching of the sacrificial MQW to expose the n^{++}GaN surface to measure the n-side roughness. (c) Fluorescence microscope image showing PEC test structures after fabrication. The dark-colored regions are the Ti/Au metal, blueish regions are due to fluorescence of the sacrificial MQW, and the yellow-colored region is the dry-etched surface in the field between devices. Devices in the bottom-right corner of the image were uncovered with metal because that area was shadowed by a mounting clip during metal deposition. (d) Fluorescence micrograph after 30 minutes of PEC etching in 1 M KOH with a 405 nm LED array illumination source. The blueish regions decreased in size as the sacrificial MQW etched during PEC etching.

The samples were placed face-down in a solution of KOH during PEC etching of the sacrificial layer using a 405 nm LED array. This is a similar orientation as for VCSELs during the PEC etching process that have the GaN sample face-down, so the sacrificial MQW is illuminated by 405 nm light that shines through the backside of the *m*-plane GaN substrate. Similar to VCSELs after PEC etching, the n^{++}GaN surface is revealed after the sacrificial MQW etches completely, as illustrated in Figure 75(b), and the n-side roughness after PEC etching can be characterized. Figure 75(c) shows a fluorescence micrograph of a PEC test sample before PEC etching. The dark-colored regions are Ti/Au, the blueish regions are due to fluorescence of the sacrificial MQW, and the yellow-colored region is the dry-etched surface in the field

between mesas. Note that Ti/Au did not cover mesas in the bottom-right corner of the image because that area was shadowed by a mounting clip during electron beam evaporation. Figure 75(d) shows a fluorescence micrograph after 30 minutes of PEC etching, showing the blueish regions diminishing in size as the sacrificial MQW etched during PEC etching. The Ti/Au on top of the mesas was useful to determine when PEC etching was complete because they would fall off once the sacrificial MQW was completely etched. Figure 76 shows micrographs of the PEC test structures after PEC etching for 2 hours in 1 M KOH.

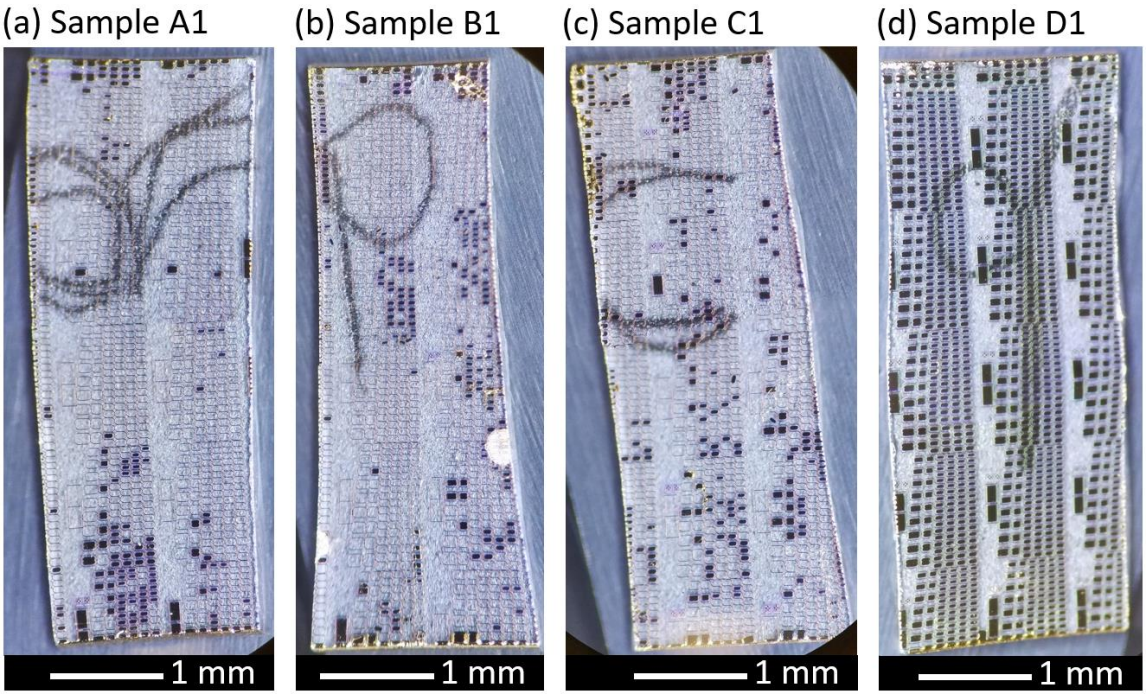


Figure 76. Optical Micrograph of the PEC test structures after PEC etching for 2 hours in 1 M KOH with a 405 nm LED array illumination source for (a) Sample A1, (b) Sample B1, (c) Sample C1, and (d) Sample D1.

After PEC etching, the samples were placed in DI water and a pipette was used to generate a stream of KOH solution toward the samples to determine whether the sacrificial layers were completely etched (i.e., the Ti/Au pads float away once the sacrificial layer is completely etched). As shown in Figure 76(a-c), most of the Ti/Au pads on the mesas were removed after 2 hours of PEC etching for Samples A1, B1, and C1, which indicated that PEC etching of the

sacrificial MQW was complete in those regions. This was further confirmed by fluorescence microscopy as the sacrificial MQW no longer fluoresces once it is PEC-etched. In contrast with the samples that had a sacrificial MQW (A1, B1, and C1), the PEC etch rate was much slower for the single-QW Sample D1, and none of the Ti/Au pads lifted off after 2 hours of PEC etching, as shown in Figure 76(d). After a total of 320 minutes of PEC etching, many of the Ti/Au pads lifted off. AFM was used to measure the RMS roughness of the n^{++}GaN surface for each sample after PEC etching with AFM scan sizes of 1 μm × 1 μm, 5 μm × 5 μm, and 10 μm × 10 μm, as shown in Figure 77.

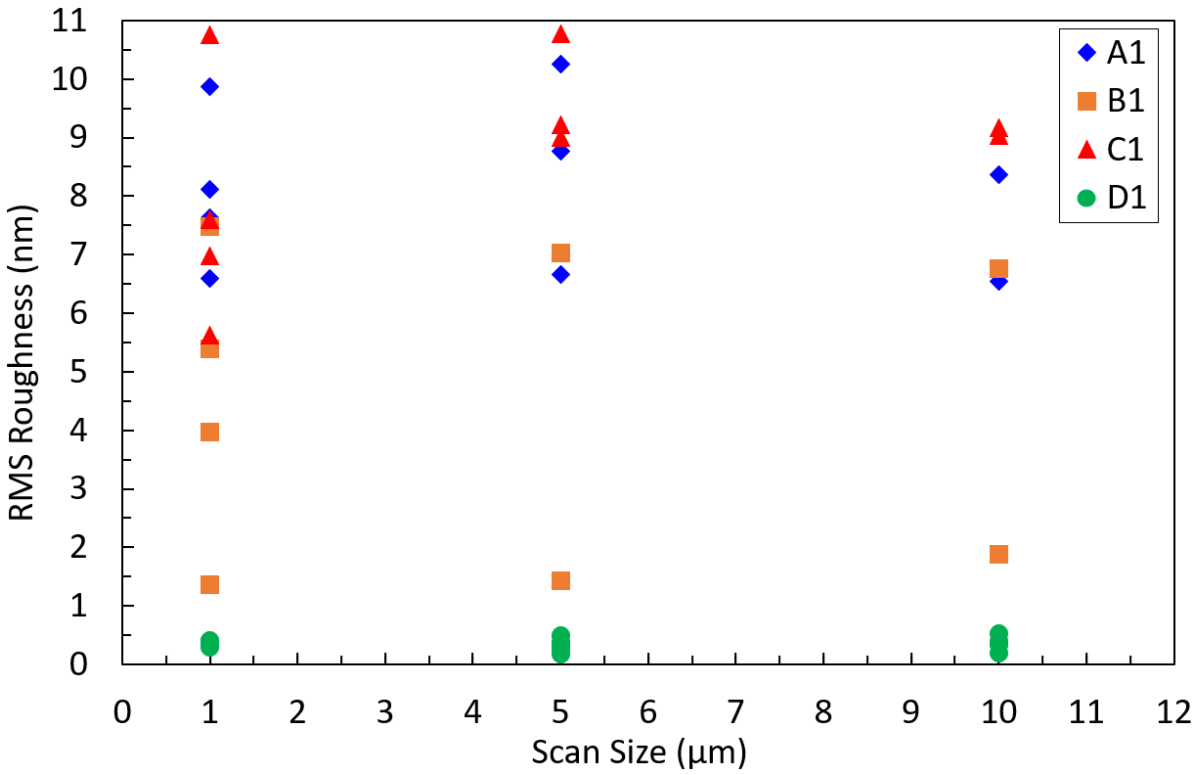


Figure 77. RMS roughness of the n^{++}GaN surface after PEC etching versus AFM scan size for the PEC test structures. Each of the samples that had a sacrificial MQW had very rough surfaces up to ~10 nm RMS roughness. With a sacrificial single QW, Sample D1 had a much smoother morphology below 1 nm RMS roughness after PEC etching. Note that the AFM scan size corresponds to a square area (e.g., a 5 μm scan size corresponds to a 5 μm × 5 μm AFM scan).

Each of the samples that had a sacrificial MQW (Sample A1, B1, and C1) had a rough morphology with an RMS roughness up to ~ 10 nm, which was similar to the n-side roughness measured for VCSELs. As shown by the green data points in Figure 77, the sample with a sacrificial single QW (Sample D1) had a much smoother surface after PEC etching with an RMS roughness below 1 nm. Characteristic AFM images after PEC etching for each of the samples are shown in Figure 78.

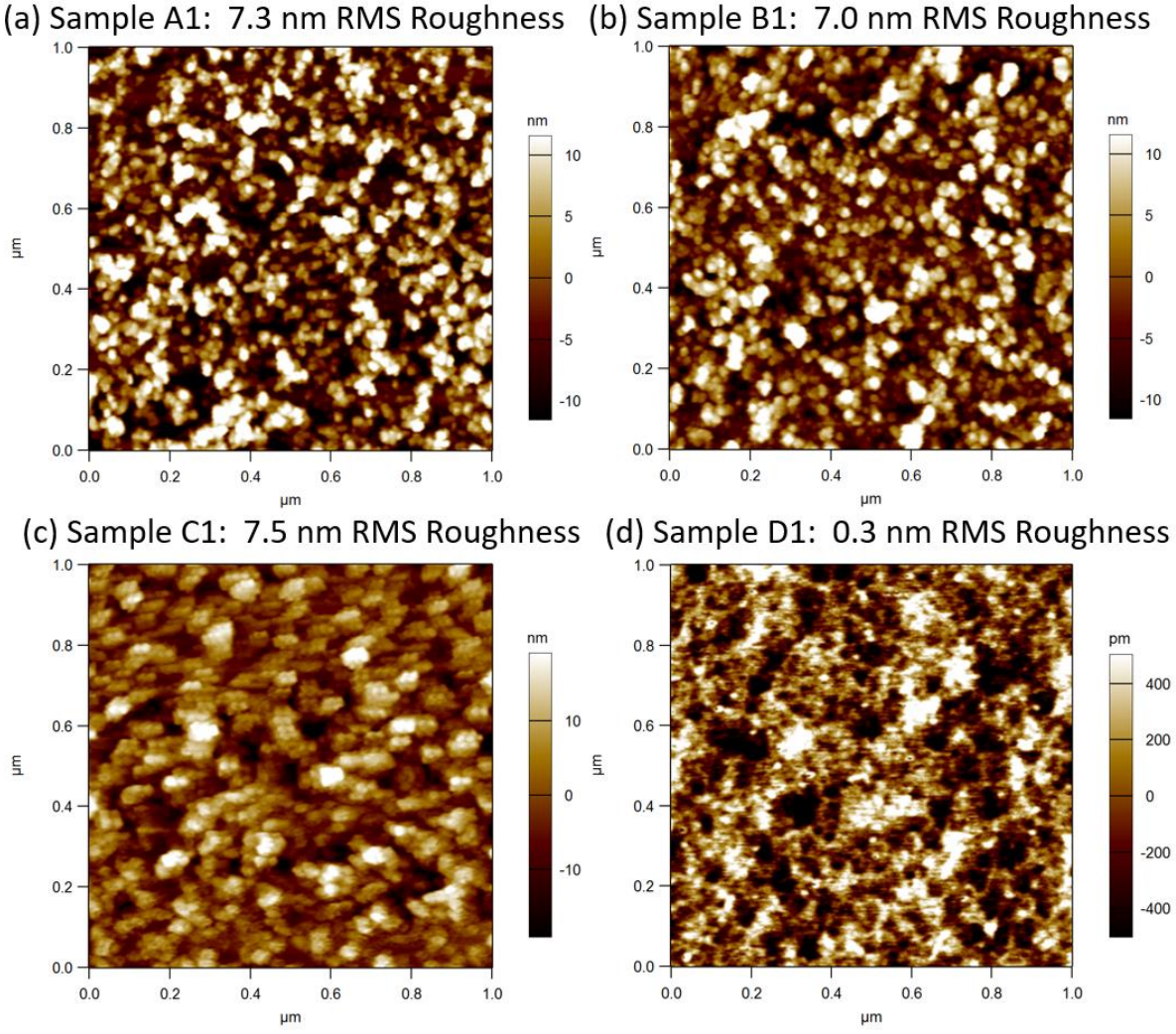


Figure 78. AFM images showing the roughness on the n^{++}GaN surface after PEC etching for PEC test samples (a) A1, (b) B1, (c) C1, and (d) D1. Samples with a sacrificial MQW (A1, B1, and C1) had a rough morphology while the single-QW sample (D1) had a smooth surface (< 1 nm RMS roughness) after PEC etching.

As shown in in Figure 78(a-c) for PEC test samples with a sacrificial MQW, the roughness on the n^{++}GaN surface after PEC etching was very similar to the n-side roughness shown in Figure 66 that was present on the 13λ and 23λ VCSELs that failed to lase. This qualitatively confirmed that the simplified PEC test structures were similar enough to the VCSEL structure to produce the same type of roughness, so these test samples could be used in place of actual VCSELs for PEC etching experiments. Unlike the sacrificial MQW samples, the sample with a sacrificial single QW (Sample D1) had a very smooth morphology, as shown in Figure 78(d). With an RMS roughness below 1 nm, this is an ideal n-side surface morphology for VCSELs. To see if these results were repeatable, another sample was cleaved from Sample D (labeled Sample D2) and PEC etching was performed in a solution of 1 M KOH solution. After PEC etching for 320 minutes, several Ti/Au pads lifted off, indicating that the sacrificial single QW fully etched in those areas. AFM was performed to measure the RMS roughness of the exposed n^{++}GaN surface after PEC etching, and the results are shown in Figure 79 for three AFM scan sizes measured in three different locations (i.e., each location was on a different mesa).

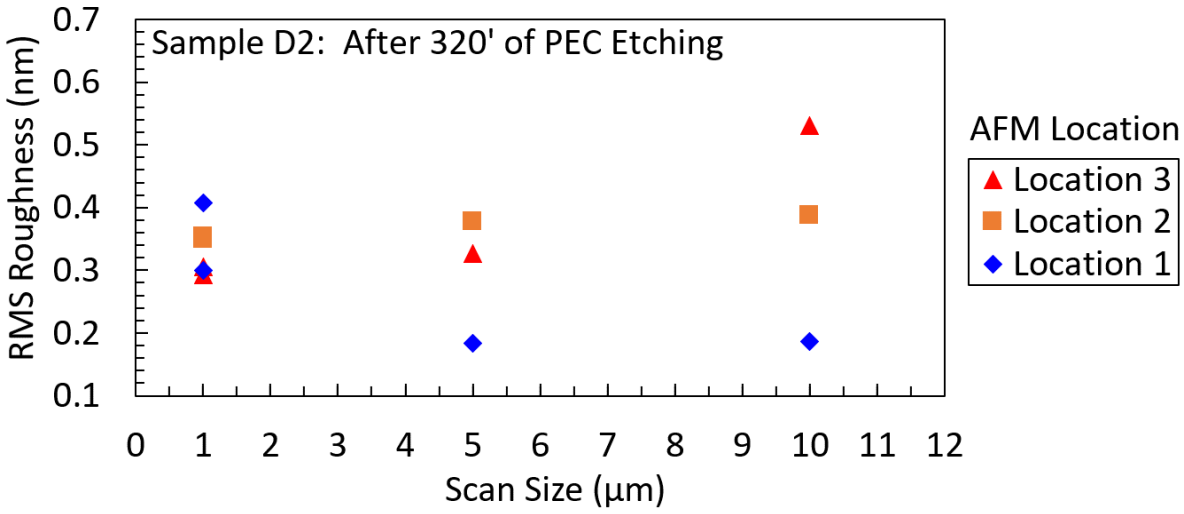


Figure 79. RMS roughness after PEC etching for 320 minutes versus AFM scan size for a PEC test sample with a sacrificial single QW (Sample D2) measured at three locations.

Similar to Sample D1, Sample D2 also had a smooth surface morphology with an RMS roughness below 1 nm. This suggested that a sacrificial single QW could be a viable alternative to replace the sacrificial MQW in the VCSEL design in order to achieve a smooth n-side surface.

To further test the repeatability of these results and study the effect of PEC etching time on RMS roughness, a third sample was cleaved from Sample D (labeled Sample D3). After PEC etching in a solution of 1 M KOH for 179 minutes, several Ti/Au pads lifted off, indicating that the sacrificial single QW fully etched in those areas. For three specific locations across the wafer, AFM was performed on the exposed n^{++}GaN surface after PEC etching for 179 minutes, 418 minutes, and 574 minutes to study the effect of PEC etching time on RMS roughness, and the results are shown in Figure 80.

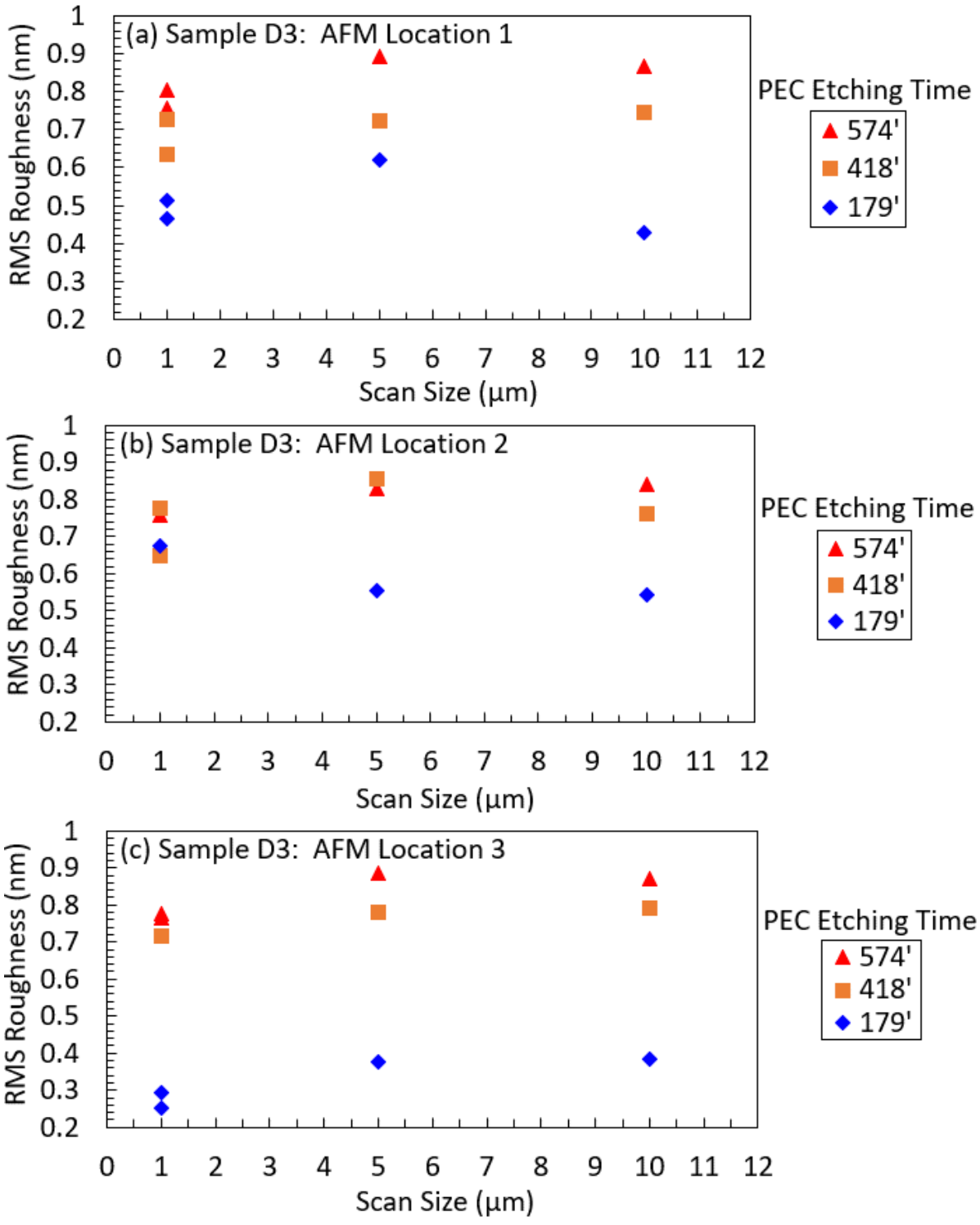


Figure 80. RMS roughness after PEC etching versus AFM scan size for a PEC test sample with a sacrificial single QW (Sample D3) measured at three locations on the wafer: (a) Location 1, (b) Location 2, and (c) Location 3. AFM scans were performed at each of these locations after PEC etching in a solution of 1 M KOH for 179 minutes, 418 minutes, and 574 minutes.

Similar to the Samples D1 and D2 with sacrificial single QWs, Sample D3 had a smooth surface morphology after PEC etching with an RMS roughness below 1 nm. Though, note that the surface roughness was somewhat nonuniform and varied based on the location on the wafer. For the three measured locations, the Ti/Au pad lifted off after 179 minutes of PEC etching, so the sacrificial single QW was likely completely etched at that point. If the sacrificial QW was not completely etched, PEC etching for longer times could potentially reduce the surface roughness; however, the opposite trend was observed. Among the three measured locations, the RMS roughness tended to increase for longer PEC etching times, but the RMS roughness never exceeded 1 nm. Figure 81(a) and Figure 81(b) show AFM scans at Location 1 of the surface after PEC etching for 179 minutes and 574 minutes, respectively.

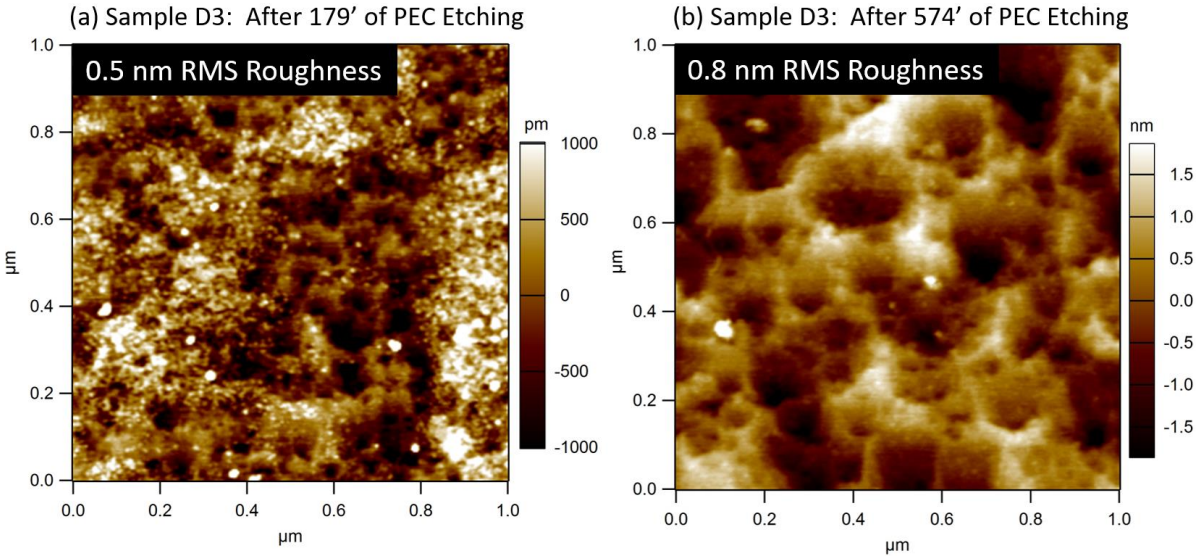


Figure 81. AFM images of the n^{++}GaN surface for a PEC test sample with a sacrificial single QW (Sample D3) after PEC etching for (a) 179 minutes and (b) 574 minutes. Both AFM scans were taken near the same location (Location 1).

Because longer PEC etching times roughened the surface, the sacrificial QW was likely completely etched after 179 minutes. As shown in Figure 81, the RMS roughness increased from 0.5 nm to 0.8 nm after PEC etching for an additional 395 minutes. With subnanometer RMS roughness after PEC etching for samples D1, D2, and D3, the sacrificial single QW

seemed like a viable solution to reduce n-side roughness in the VCSEL design; however, one potential problem is the significantly slower PEC etch rate of a sacrificial single QW compared to a sacrificial MQW because the roughness increases for longer durations of PEC etching. Fluorescence microscopy was used to measure the PEC etch rate of the sacrificial single QW. Figure 75(d) shows a fluorescence micrograph of Sample D1 after PEC etching for 30 minutes, which indicated a PEC etch rate of ~20 μm/hour in the +*c* direction, ~13 μm/hour in the -*c* direction, and ~12 μm/hour in the *a* direction. Note that these numbers are rough estimates of the PEC etch rate as the fluorescence micrographs were taken at a low magnification and resolution. During PEC etching of the test samples, the sacrificial layer etched laterally from the sidewalls toward the center of the mesas; however, unlike actual VCSEL samples, PEC etching occurred simultaneously for every mesa on the wafer for the test samples. It can take longer to completely etch the sacrificial QW for actual VCSEL samples because PEC etching initially occurs for devices near the outer perimeter of the wafer, and devices in the center do not etch until the outer ones are finished. This is likely due to the difference in geometry between the samples because unlike the PEC test structures, the actual VCSEL samples are flip-chip bonded to a submount.

During this time, the VCSELs that would eventually achieve CW operation (described in Section 4.5) were being processed with the hope of solving the n-side roughness problem before they reached the PEC etching stage. While using a sacrificial single QW looked like a promising solution to reduce n-side roughness, a sacrificial MQW was already employed in those devices. Therefore, the next step was to continue investigating the PEC etch roughness and determine if other methods could create a smooth surface.

Initially, the n-side roughness after PEC etching was presumed to be roughened n^{++}GaN. One possible explanation was chemical-related roughening in KOH solution; however, this was unlikely because although the N-face of *c*-plane GaN is susceptible to roughening in KOH solution, *m*-plane GaN should be chemically stable. Furthermore, if chemical-related etching caused the n^{++}GaN roughness, lowering the concentration of KOH during PEC etching would be expected to decrease the degree of chemical-related roughening, but this trend was not observed. Another possible cause of n^{++}GaN roughness could have been due to a PEC etching mechanism. Ideally, 405 nm illumination only creates photogenerated holes in the InGaN QWs, so the sacrificial MQW should selectively etch during PEC etching; however, PEC-related roughening of n^{++}GaN could be possible if photogenerated holes were able to diffuse into the n^{++}GaN layer. This type of mechanism was demonstrated by A. Tamboli et al. during PEC undercut etching of InGaN capped by a GaN layer: although photogenerated holes were only created within the InGaN layer for PEC etching, if a weak etchant (i.e., low electrolyte concentration) was used, photogenerated holes would have time to drift into the GaN layer to cause roughness via PEC etching.[170] PEC-related roughening of the GaN cap layer could be minimized by using a strong etchant during PEC etching, so photogenerated holes were consumed immediately before they could leave the InGaN layer.[170] Thus, if n^{++}GaN roughening was caused by this type of PEC-related mechanism, using stronger KOH concentrations during PEC etching would be expected to reduce the roughness, but this trend was not observed. PEC-related roughening of n^{++}GaN is also unlikely because the high Si doping concentration results in a short photogenerated carrier lifetime, which makes highly-doped n^{++}GaN resistant to PEC etching.[125] This suggested that the n-side roughness was not due to roughened n^{++}GaN after PEC etching, as previously presumed.

Instead of roughened n^{++}GaN, further characterization revealed that the n-side roughness was actually due to a rough residue that formed on the n^{++}GaN surface after PEC etching. Figure 82 shows optical microscope images of the rough residue that appeared on the n-side of devices after PEC etching to remove the *m*-plane GaN substrate during VCSEL processing.

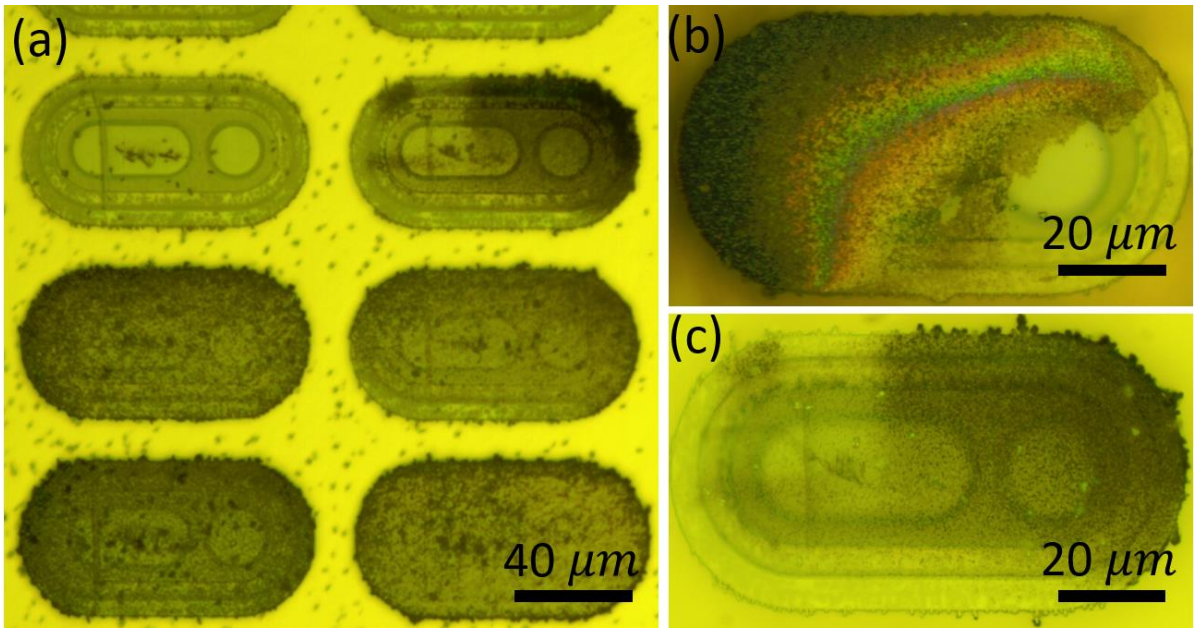


Figure 82. Optical micrographs showing a rough residue on the n-side of devices after PEC undercut etching to remove the *m*-plane GaN substrate. The residue was nonuniform and varied from device to device, as shown in (a), (b), and (c).

The rough residue was nonuniform and the degree of roughness varied among devices across the wafer. Several treatments and experiments were performed with the goal of removing the residue, but most were unsuccessful, including sonication in solvents (i.e., acetone, isopropanol, and DI water) and using various PEC etching conditions (e.g., varying the KOH concentration, varying the illumination intensity of the 405 nm LED array, using a lens to focus the 405 nm illumination on the sample, using a magnetic stirrer to stir the KOH solution, and continuing to PEC etch after the *m*-plane GaN substrate already lifted off).

The most effective way to remove the rough residue after PEC etching was to use a foam swab to wipe the sample surface in a solution of Tergitol detergent. For a PEC test sample after PEC etching, Figure 83 shows optical microscope images of the surface before and after swabbing the sample in Tergitol detergent to remove the residue.

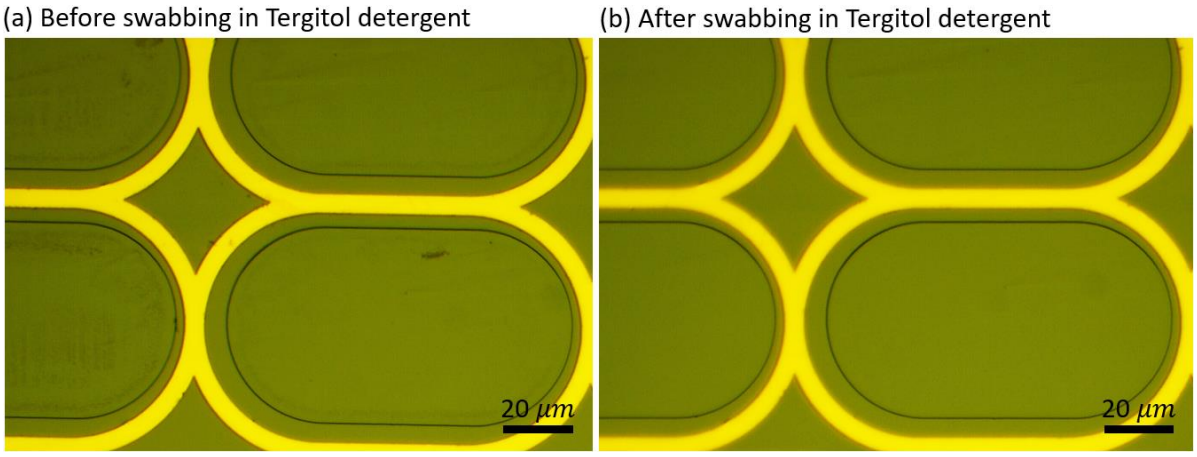


Figure 83. Optical micrographs of a PEC test structure showing (a) the rough residue that forms after PEC undercut etching and (b) the surface after removing the residue by swabbing in Tergitol detergent.

Depending on the severity of the residue, it was sometimes difficult to view the residue optically, as shown in Figure 83(a). After swabbing in Tergitol detergent, the mesas appeared smoother, as shown in Figure 83(b). Because the residue was difficult to observe via optical microscopy, SEM and AFM were mainly used to characterize the roughness. For a VCSEL sample after PEC etching, Figure 84 shows SEM images of the n^{++}GaN surface before and after swabbing to remove the residue.

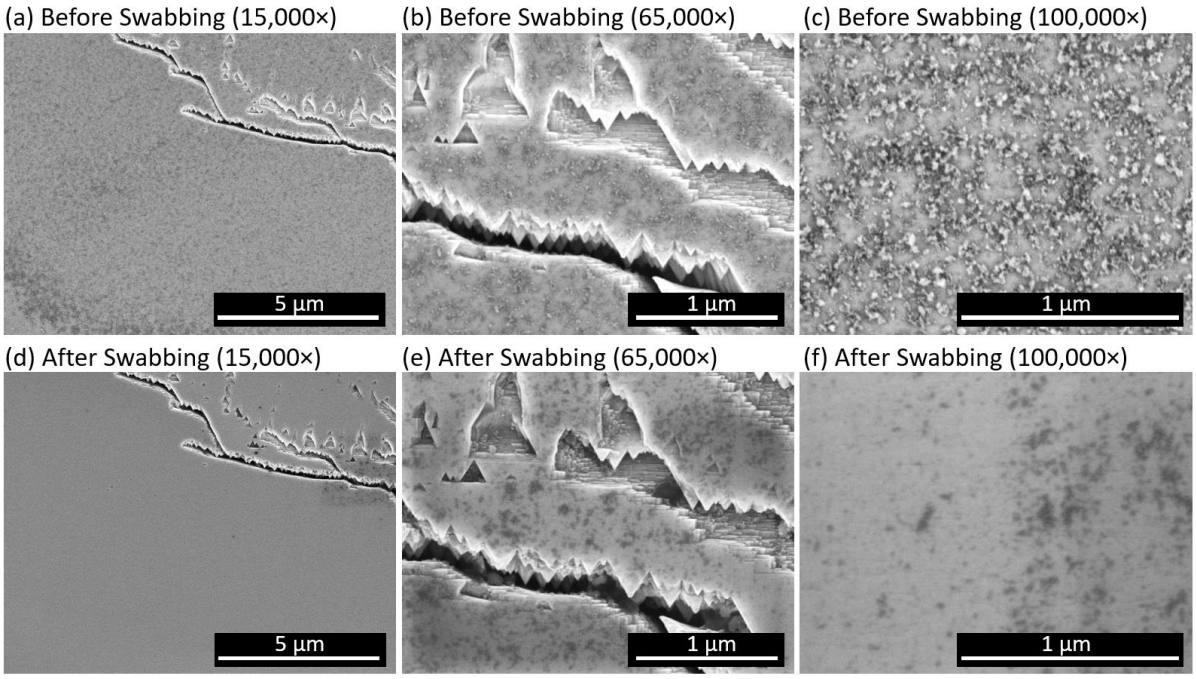


Figure 84. SEM micrographs of a partially-processed VCSEL sample showing the rough residue that forms on the n-side after PEC undercut etching to remove the *m*-plane GaN substrate. The rough residue is shown at an SEM magnification level of (a) 15,000×, (b) 65,000×, and (c) 100,000×. (d)-(f) show those same magnification levels after swabbing in Tergitol detergent to remove the rough residue.

At various magnification levels, Figure 84(a)-(c) show the n-side surface before swabbing, which shows the rough residue that forms after PEC etching. The cracks shown in Figure 84(a)-(b) were caused during Au-Au thermocompression flip-chip bonding, and Section 4.4.6 discusses experiments that were performed to reduce cracking and improve VCSEL yield. Due to cracking prior to the PEC etching, KOH crystallographic etching can be observed in the cracks shown in Figure 84(b). With the *m*-plane GaN surface oriented with the +*c* direction pointing toward the top of the SEM images, characteristic KOH roughening can be observed by the cone-shaped features on the N-face of *c*-plane GaN. KOH roughening did not affect crack-free *m*-plane GaN surfaces, but the surface was rough due to the PEC residue, which is most clearly shown in Figure 84(c). Figure 84(d)-(f) show the n^{++}GaN surface after swabbing in Tergitol to remove the residue, resulting in a much smoother surface. The dark spots shown

in Figure 84(e)-(f) were caused by SEM beam damage when viewing the residue in those areas prior to swabbing in Tergitol, and this effect is further illustrated in Figure 85.

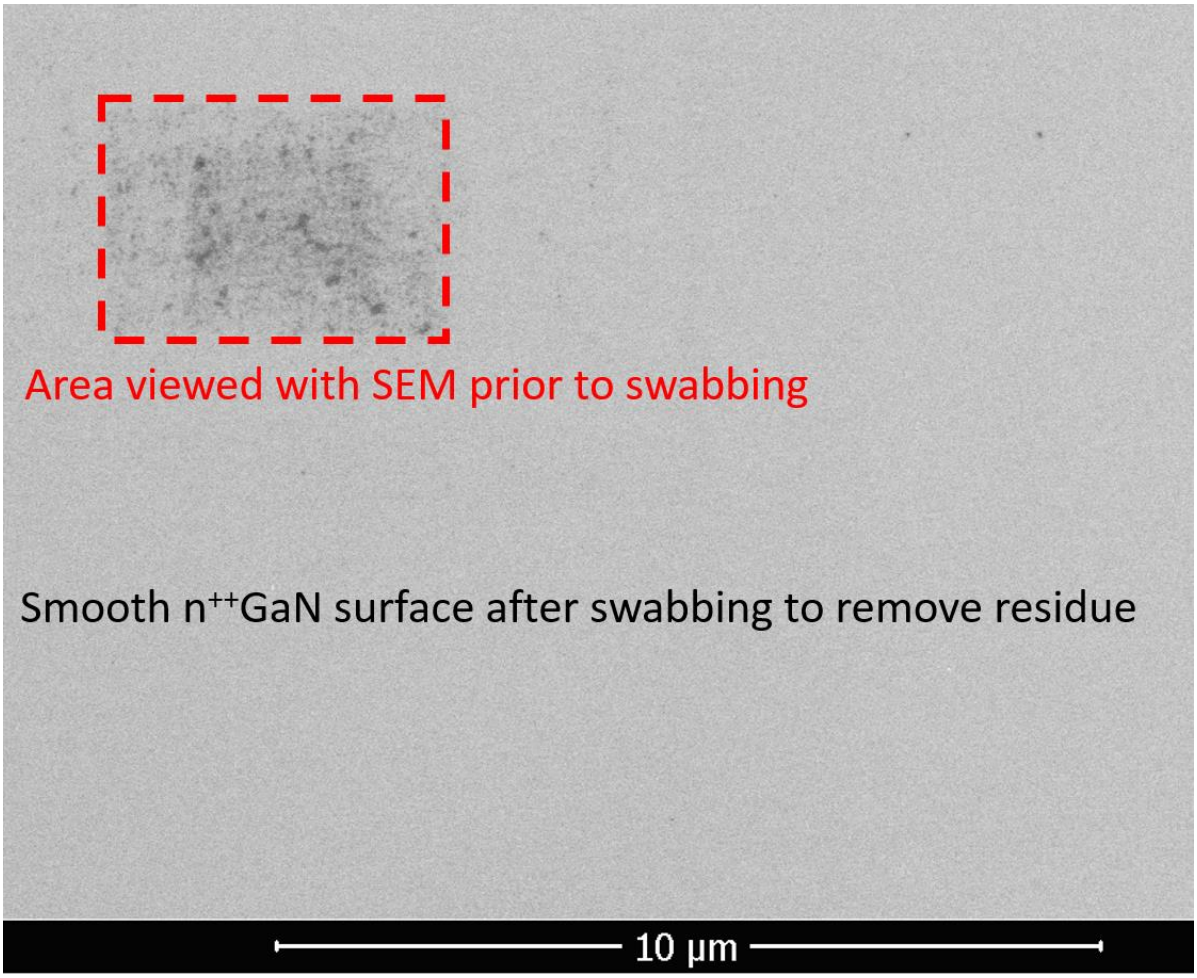


Figure 85. SEM micrograph of the n-side of a VCSEL sample after swabbing in Tergitol to remove the rough residue that forms during PEC etching. The dashed red rectangle outlines the area that was viewed with SEM prior to swabbing, resulting in dark-colored blotches due to beam damage. Areas that were not viewed with SEM at high magnification prior to swabbing had a very smooth n^{++}GaN surface after the residue was removed via swabbing.

The n^{++}GaN surface was very smooth after swabbing in Tergitol except for the dark-colored blotches in the rectangular area that was viewed with SEM at high magnification prior to residue removal. After qualitatively showing that swabbing in Tergitol can remove the PEC residue, the next step was to measure the RMS roughness of the surface with AFM. While the PEC test samples with sacrificial MQWs (Sample A1, B1, and C1) had ~7 nm RMS roughness

due to the rough residue after PEC etching, swabbing in Tergitol produced a smooth surface with subnanometer RMS roughness, as shown in Figure 86.

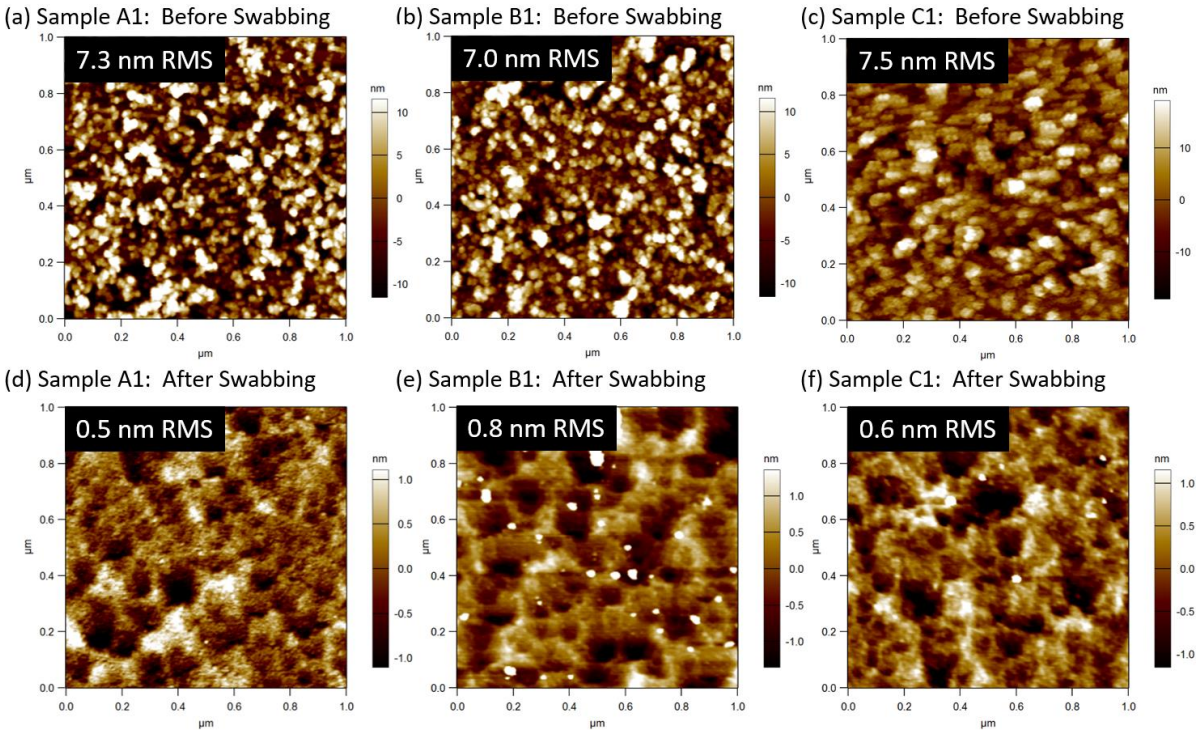


Figure 86. Optical micrographs of a PEC test structure showing (a) the rough residue that forms after PEC undercut etching and (b) the surface after removing the residue by swabbing in Tergitol detergent.

The rough residue that formed after PEC etching is shown in Figure 86(a)-(c), and the smooth surfaces after Tergitol swabbing are shown in Figure 86(d)-(f). As shown in Figure 86(d) for Sample A1 and Figure 86(f) for Sample C1, the residue appeared completely removed after Tergitol swabbing, resulting in a smooth surface with 0.5 nm and 0.6 nm RMS roughness, respectively. As shown in Figure 86(e), swabbing significantly smoothened the surface for Sample B1, but there were some remaining remnants of the residue. As expected, further swabbing in Tergitol could be performed if the residue was not fully removed. This showed that swabbing in Tergitol was an effective method to remove the PEC residue and produce a smooth n-side surface with subnanometer roughness, which is ideal for VCSELs to reduce scattering and mirror loss.

Despite its effectiveness at removing the PEC residue, there was one problem with swabbing VCSEL samples in Tergitol. After flip-chip bonding and PEC etching to remove the *m*-plane GaN substrate, the VCSEL devices are particularly fragile, and physical swabbing can fracture and fully remove devices from the flip-chip substrate. This was especially problematic because, as discussed further in Section 4.4.6, the VCSEL yield was already very low with cracks propagating through most of the devices after flip-chip bonding and PEC etching. This led to further investigation of the PEC residue with the goal of identifying its origin and finding other methods of residue removal that are less damaging to devices.

The rough residue that formed after PEC etching was found to have a similar morphology to images reported in the literature for gallium oxide (Ga_2O_3), as shown in Figure 87 for AFM images after thermal oxidation of GaN at various temperatures in a dry O_2 ambient.[171]

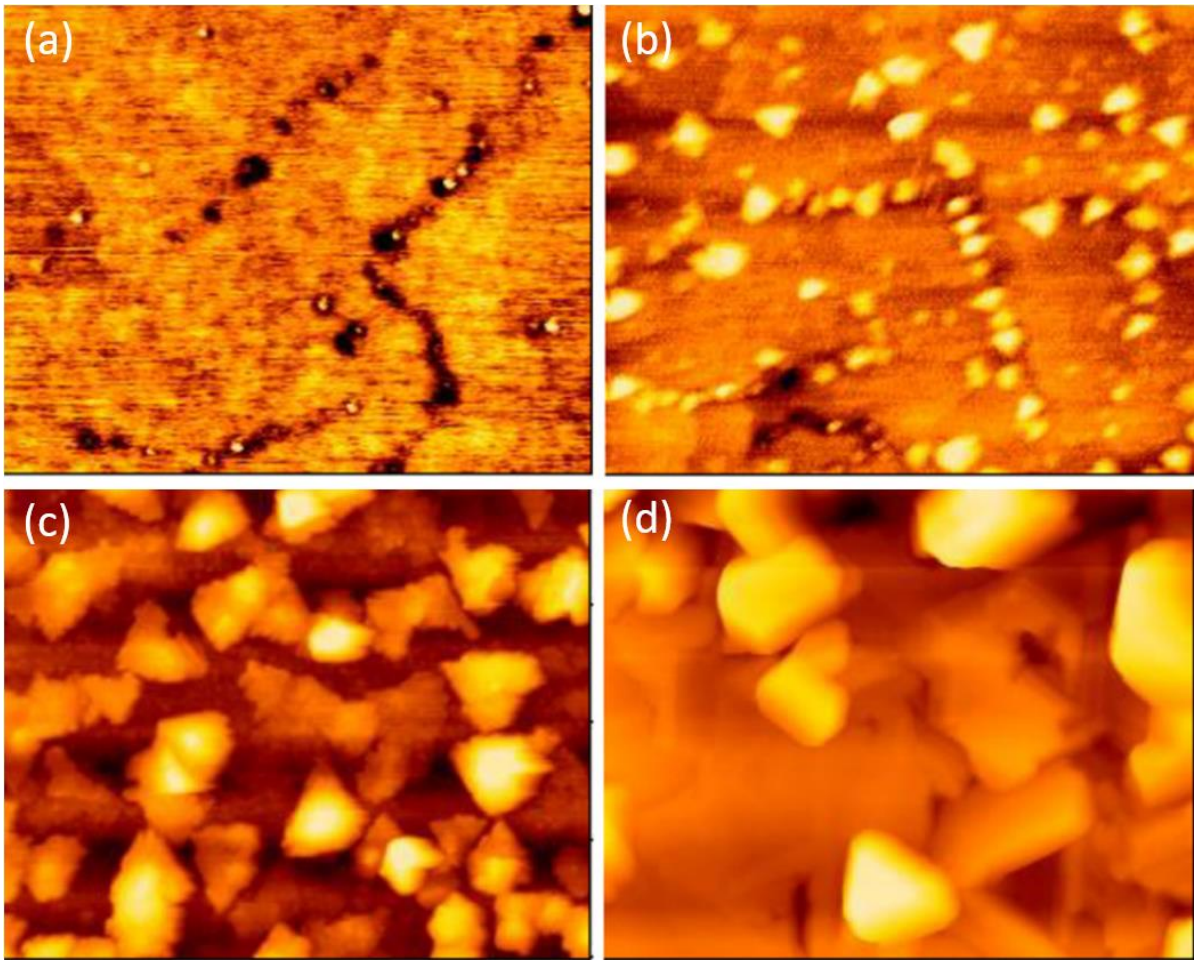


Figure 87. 1 × 1 μm^2 AFM images of gallium oxide grown on GaN by thermal oxidation at (a) 800 °C, (b) 850 °C, (c) 900 °C, and (d) 1000 °C. Reprinted from [Yamada, T., Ito, J., Asahara, R., Watanabe, K., Nozaki, M., Nakazawa, S., Watanabe, H. (2017). Comprehensive study on initial thermal oxidation of GaN(0001) surface and subsequent oxide growth in dry oxygen ambient. *Journal of Applied Physics*, *121*(3), 035303. https://doi.org/10.1063/1.4974458] with the permission of AIP Publishing.[171]

In addition to thermal oxidation, Ga_2O_3 nanostructures can also be deposited electrochemically onto substrates, as shown in Figure 88.[172]

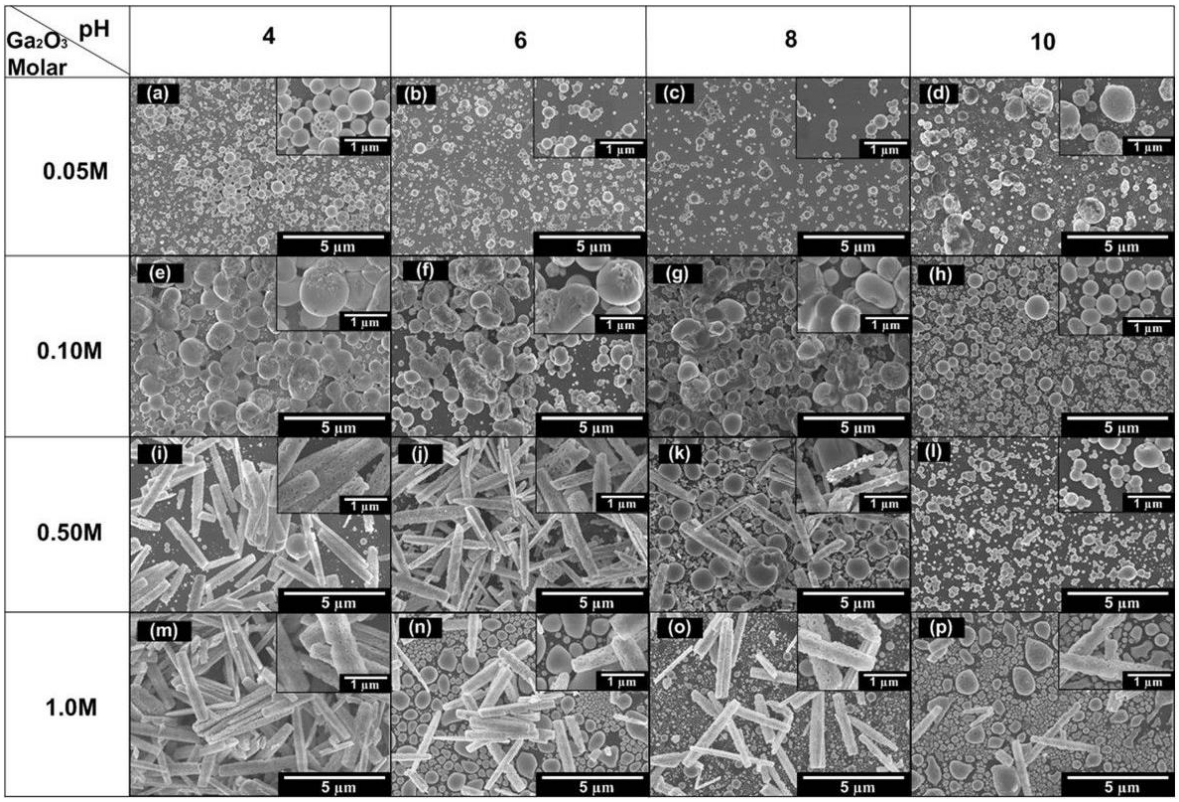


Figure 88. SEM images of electrochemically deposited Ga_2O_3 nanostructures onto Si substrates using a mixture of Ga_2O_3, HCl (36%), NH_4OH (25%), and DI water with various pH values and molarities of Ga_2O_3. Deposition was performed at a constant current density of 0.15 A/cm^2. The structure of the deposited Ga_2O_3 nanostructures varied significantly based on the molarity and pH value.[172] Reprinted from [Ghazali, N., Mahmood, M., Yasui, K., & Hashim, A. (2014). Electrochemically deposited gallium oxide nanostructures on silicon substrates. *Nanoscale Research Letters*, *9*(1), 120. https://doi.org/10.1186/1556-276X-9-120] under the Creative Commons Attribution 4.0 License (http://creativecommons.org/licenses/by/4.0/).

As shown in Figure 88, the morphology of the Ga_2O_3 nanostructures varied depending on the molarity of Ga_2O_3 and pH of the solution.[172] This was similar to the rough residue that formed on the n-side after PEC etching for VCSEL samples. After further characterization, the residue after PEC etching was found to exist in various structural forms, as shown in Figure 89.

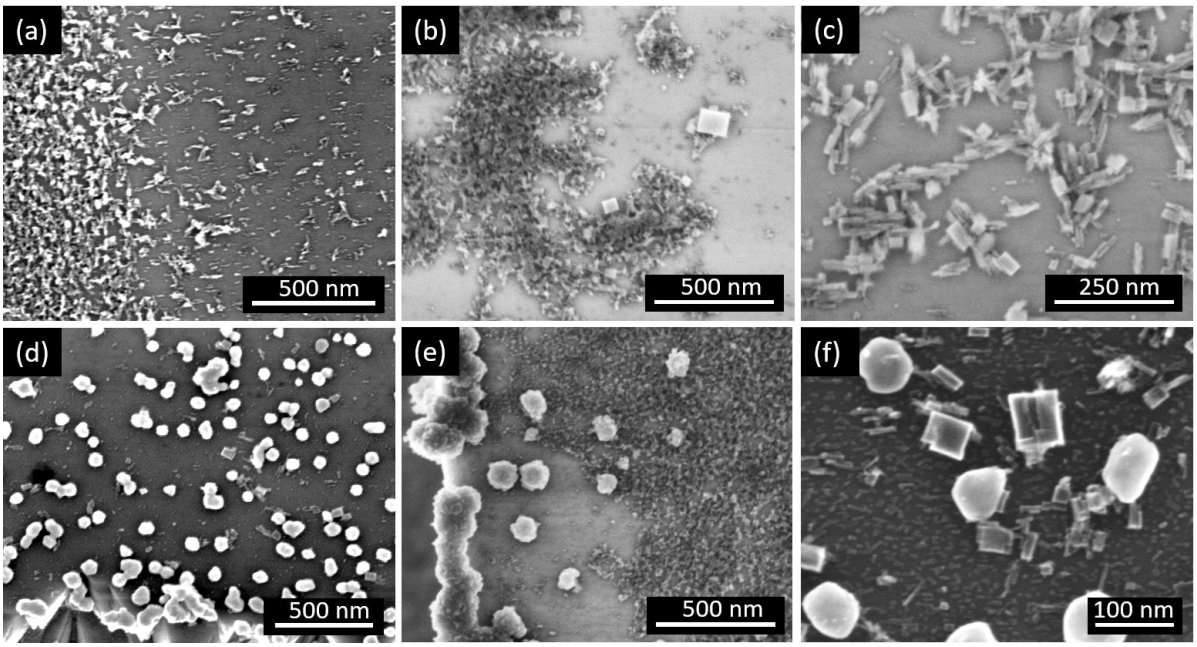


Figure 89. SEM images showing various types of rough residues that form on the n-side of VCSEL devices after PEC etching to remove the *m*-plane GaN substrate.

These structures were somewhat similar to the electrochemically deposited Ga_2O_3 nanostructures shown in Figure 88. If the PEC residue consisted of deposited Ga_2O_3 nanostructures, it should be able to be removed by dissolving Ga_2O_3 in a solution of KOH. This was tested by submerging the samples in 11.7 M KOH solution for 20 minutes, and the results are shown in Figure 90.

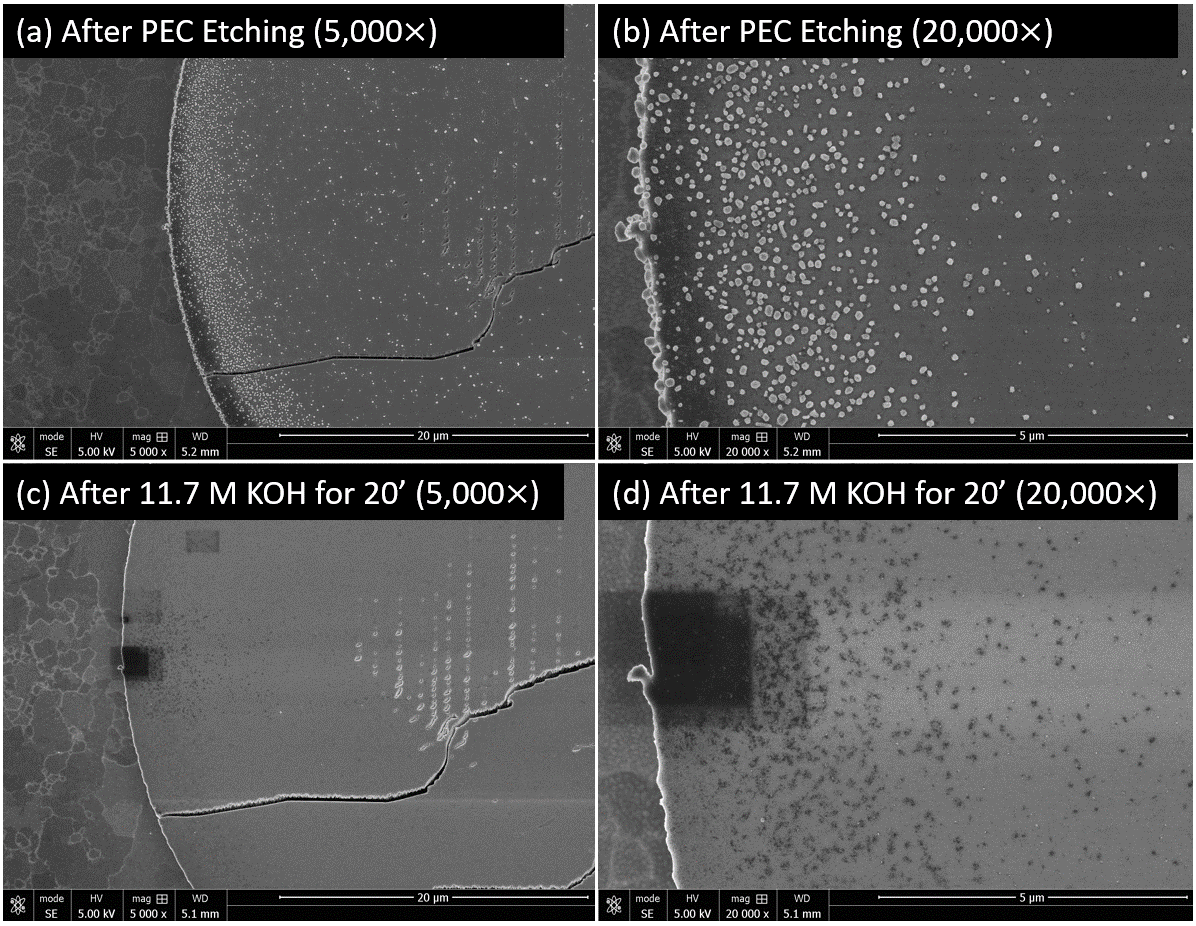


Figure 90. SEM images of partially-processed VCSELs showing the residue that forms on the n-side surface after PEC etching with an SEM magnification of (a) 5,000× and (b) 20,000×. Most of the residue could be removed by performing a 11.7 M KOH treatment for 20 minutes, as shown in the SEM images at a magnification of (c) 5,000× and (d) 20,000×.

Most of the PEC residue was able to be removed using 11.7 M KOH, which suggested that the PEC residue consisted of Ga_2O_3. Energy-dispersive X-ray spectroscopy (EDX) was used to further characterize the PEC residue that could be removed by KOH. EDX spot scans of the PEC residue compared to the uncovered n^{++}GaN surface showed a slightly higher oxygen peak, which further indicated that the residue could consist of Ga_2O_3. Although EDX did show consistent trends when studying the PEC residue, note that EDX has a large interaction volume, so it is less suitable for characterizing near-surface artifacts. For future surface composition characterization, it would be better to use X-ray photoelectron spectroscopy (XPS) or auger spectroscopy, for example. While most of the PEC residue could be removed

using KOH, some of the residue could not be removed, even with further KOH treatments. Figure 91 shows SEM images of the PEC residue that could not be removed by KOH treatments.

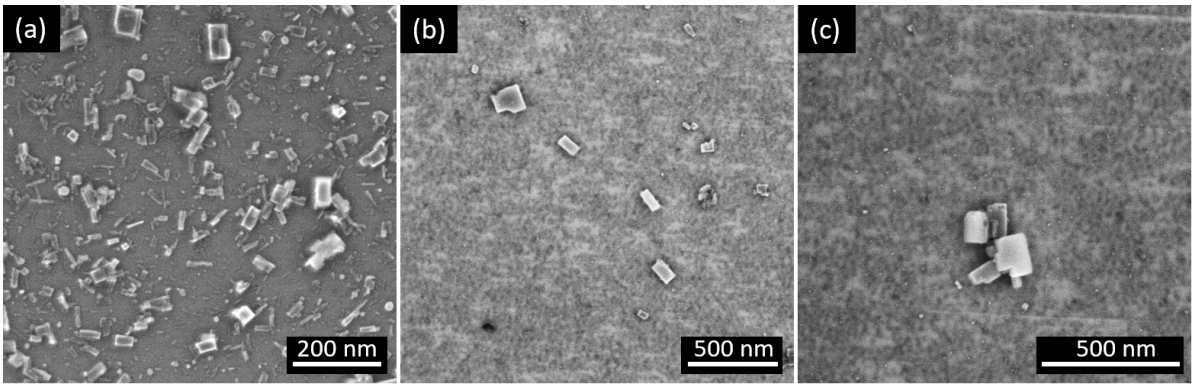


Figure 91. SEM images of the PEC residue that remained on the n-side surface after treatment in 11.7 M KOH solution.

The remaining residue after the KOH treatment could possibly consist of indium oxide (In_2O_3), which can have a cubic-like morphology.[173] This was supported by EDX spot scans that showed slightly higher indium peaks for the cubic-like PEC residue. Furthermore, while Ga_2O_3 dissolves readily in KOH solution, indium oxide has a low solubility in the basic KOH solution.[174] During PEC etching of InGaN, indium atoms react with the KOH solution to form indium oxides, which slow the PEC etch rate due to their lower solubility in KOH.[174] Indium hydroxide ($In(OH)_3$) can also have a cubic-like morphology,[175] but indium hydroxide is soluble in KOH.[176] Therefore, the remaining PEC residue more likely consisted of In_2O_3 as it was unaffected by 11.7 M KOH treatments.

This led to a series of HCl treatments to see if the remaining PEC residue (presumably In_2O_3) could be removed. In the first experiment, an 11.7 M KOH dip was performed for 20 minutes to remove the Ga_2O_3 PEC residue, and then a 3 M HCl treatment was performed for 30 seconds with the goal of removing In_2O_3 PEC residue. After the HCl treatment, both types of PEC residue were removed. This showed that HCl can be used to remove the PEC residue

without swabbing in Tergitol, which avoids the problem of physically damaging devices during swabbing. However, there was a problem with the HCl treatments because these VCSEL samples were flip-chip bonded with the new Au-In solid-liquid interdiffusion (SLID) bonding process, as discussed in Section 4.4.6.2. With a flip-chip substrate coated with Au-In, this was a problem because HCl etches indium and causes rapid bubbling as indium reacts with HCl to produce hydrogen gas. This caused relatively large features to appear on the n-side surface, as shown in Figure 92.

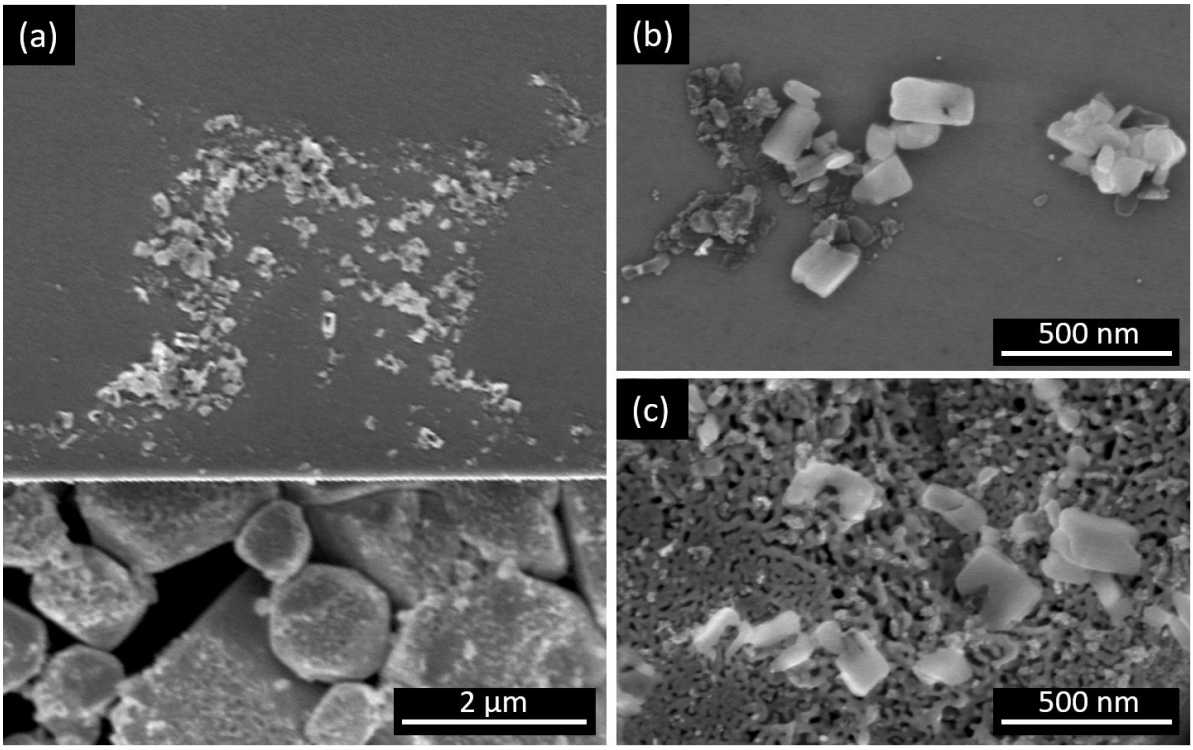


Figure 92. SEM images of a partially-processed VCSEL sample after an 11.7 M KOH treatment for 20 minutes to remove the Ga_2O_3 PEC residue and a 3 M HCl treatment for 30 seconds with the goal of removing the In_2O_3 PEC residue. Although the 3 M HCl treatment removed the PEC residue, it caused another type of material to form on the surface. (a) The upper part of the image shows the rough material that formed on the top of the n-side surface of the device after the HCl treatment, and the bottom part of the image shows the Au-In metal on the flip-chip substrate. Higher magnification SEM images are shown for (b) the rough material on the n-side surface and (c) the Au-In metal on the flip-chip substrate.

The rough material that formed on the n-side surface after the HCl treatment is shown in the upper part of the image in Figure 92(a), and the bottom of the image shows Au-In on the flip-chip substrate. Higher magnification SEM images of the rough material and Au-In on the flip-

chip substrate are shown in Figure 92(b) and Figure 92(c), respectively. The rough material likely consisted of indium because it had a similar morphology to the metal on the flip-chip substrate and it could also be etched by performing additional HCl treatments; however, HCl was not able to fully remove the material because HCl would cause additional material to form on the surface.

This led to an experiment to decrease the concentration of HCl with the goal of minimizing the HCl-related artifacts while still removing the In_2O_3 PEC residue. For another VCSEL sample after PEC etching, SEM was used to characterize the residue after PEC etching, after 11.7 M KOH for 15 minutes, and after several 1-minute treatments in HCl with concentrations of 0.06 M, 0.1 M, 0.2 M, 0.6 M, and 1.1 M. Figure 93 shows characteristic SEM images of the PEC residue after the KOH and HCl treatments.

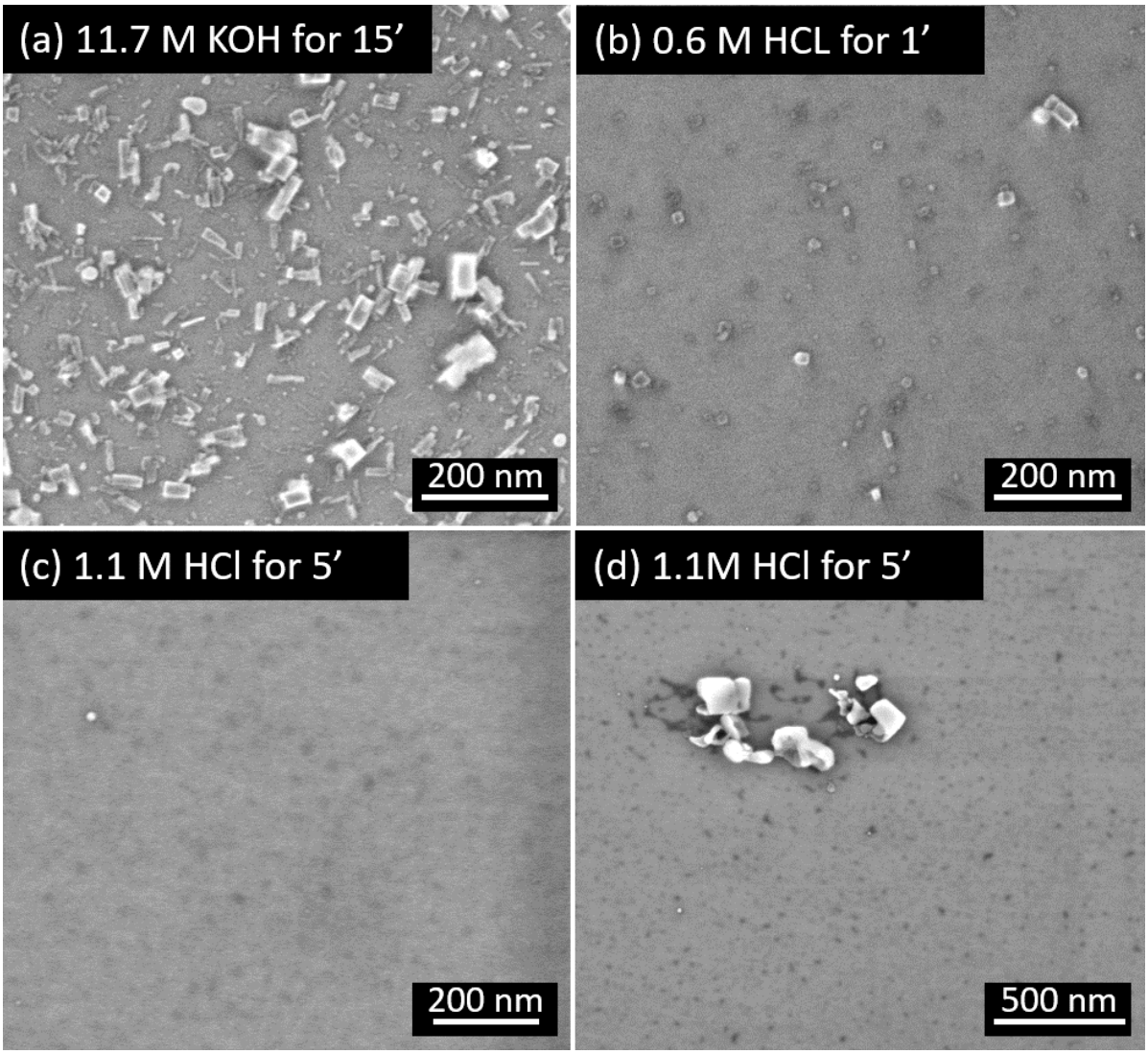


Figure 93. SEM images of the PEC residue on the n-side surface after treatment in (a) 11.7 M KOH solution for 15 minutes (b) 0.6 M HCl for 1 minute, and (c)-(d) 1.1 M HCl for 5 minutes showing different locations on the surface.

As discussed previously, 11.7 M KOH was able to remove most of the PEC residue (i.e., Ga_2O_3), but some residue remained on the surface (i.e., In_2O_3), as shown in Figure 93(a). As shown in Figure 93(b)-(c), the remaining PEC residue was able to be gradually removed using HCl, which suggests that the residue could be composed of In_2O_3. Reducing the HCl concentration helped reduce the HCl-related artifacts, but there were still many observed on the n-side surfaces, as shown in Figure 93(d). Figure 93(d) also showed that the HCl-related artifacts slowly etched during the HCl treatments, but they were not fully removed.

Although HCl seemed like a promising treatment to remove the PEC residue without causing physical damage to the devices, it appeared to cause rough indium to appear on the n-side surfaces. Lowering the HCl concentration helped minimize this problem, but further experimentation would be required to fully avoid those HCl-related artifacts. This problem would likely be avoided for Au-Au-bonded VCSEL samples, but as discussed in Section 4.4.6, switching to Au-In SLID bonding was a key design improvement that led to CW operation and significantly improved VCSEL yield. Although swabbing in Tergitol previously caused widespread damage to Au-Au-bonded VCSELs due to pre-existing cracks after bonding, Au-In-bonded VCSELs were mostly crack-free and could withstand swabbing in Tergitol with minimal damage. Therefore, swabbing in Tergitol has been the best method of PEC residue removal to create subnanometer roughness on the n-sides of devices to reduce VCSEL scattering and mirror loss.

FIB cross-sectioning revealed another problem with VCSEL samples that had BTJ apertures, as shown in Figure 94.

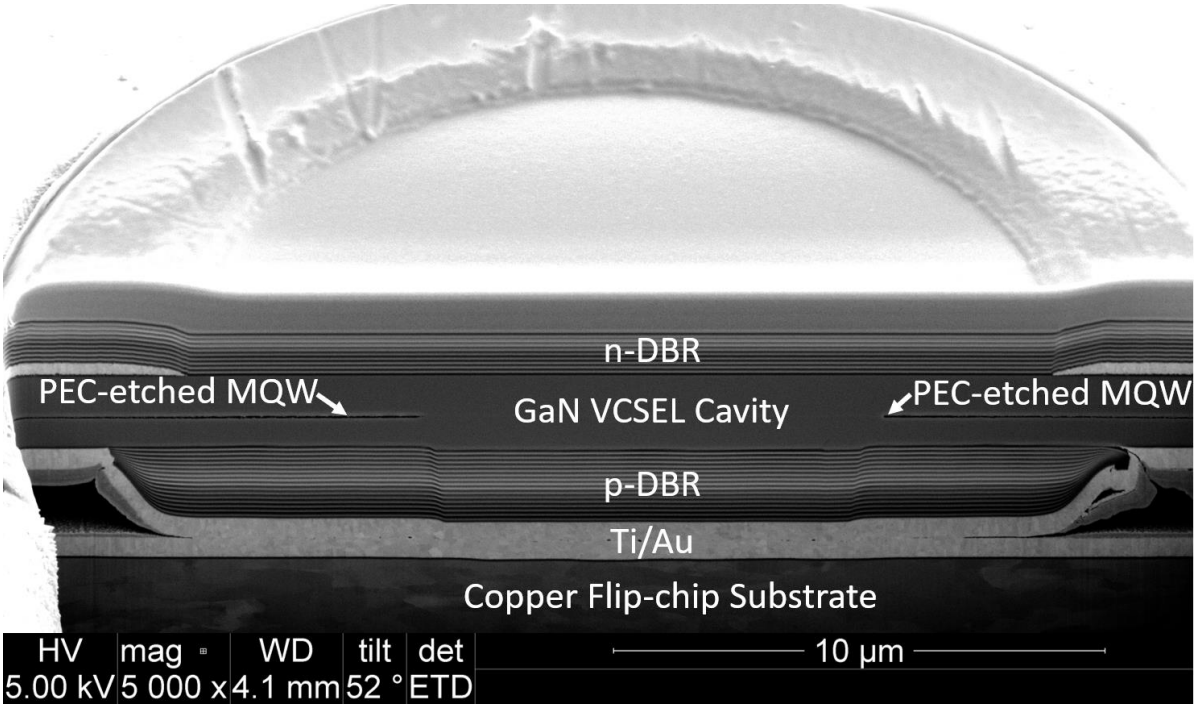


Figure 94. FIB cross-section SEM image of a BTJ aperture VCSEL showing that the active MQW partially etched during PEC etching of the sacrificial MQW to remove the *m*-plane GaN substrate.

For each of the BTJ aperture VCSEL samples, the active MQW was partially etched during PEC undercut etching of the sacrificial MQW to remove the *m*-plane GaN substrate. Another FIB cross-section image showed that SiN_x covered the sidewall of the active MQW, which should have provided protection, but the active MQW still etched during PEC etching. This showed that IBD-deposited SiN_x is not an effective method to protect the active region during PEC etching. Because the active region was only partially etched, the structure shown in Figure 94 is effectively a BTJ VCSEL with an additional PEC air-gap aperture. However, reproducing these samples could be difficult as it would require knowing the PEC etch rate of the active MQW so it does not completely etch, and this could possibly depend on the amount of SiN_x sidewall coverage. Etching of the active MQW was not a problem for ion implanted aperture VCSELs because Al ion implantation passivated the active MQW outside the aperture and protected it during PEC etching.

4.4.6. Yield and Thermal Improvements

While roughness prior to the DBRs was the main problem that prevented the 13λ and 23λ VCSELs from lasing under pulsed operation, there were two significant problems remaining. First, there was very low device yield after flip-chip bonding, and only a small percentage of crack-free VCSELs could survive the entire fabrication process. Secondly, failure analysis revealed a significant thermal issue that inhibited CW operation. While COMSOL thermal simulations predict improved heat transport using a thicker 23λ cavity, there was still a bottleneck in heat flow due to the thermally-insulating bottom dielectric DBR. According to thermal simulations, instead of heat flowing through the bottom DBR, heat flows around it through a thin metal p-side contact that conforms around the bottom DBR. FIB cross-section SEM images were taken during the failure analysis of the 13λ and 23λ VCSELs, which revealed another thermal issue as there were cracks in that p-side metal pathway, as shown in Figure 95.

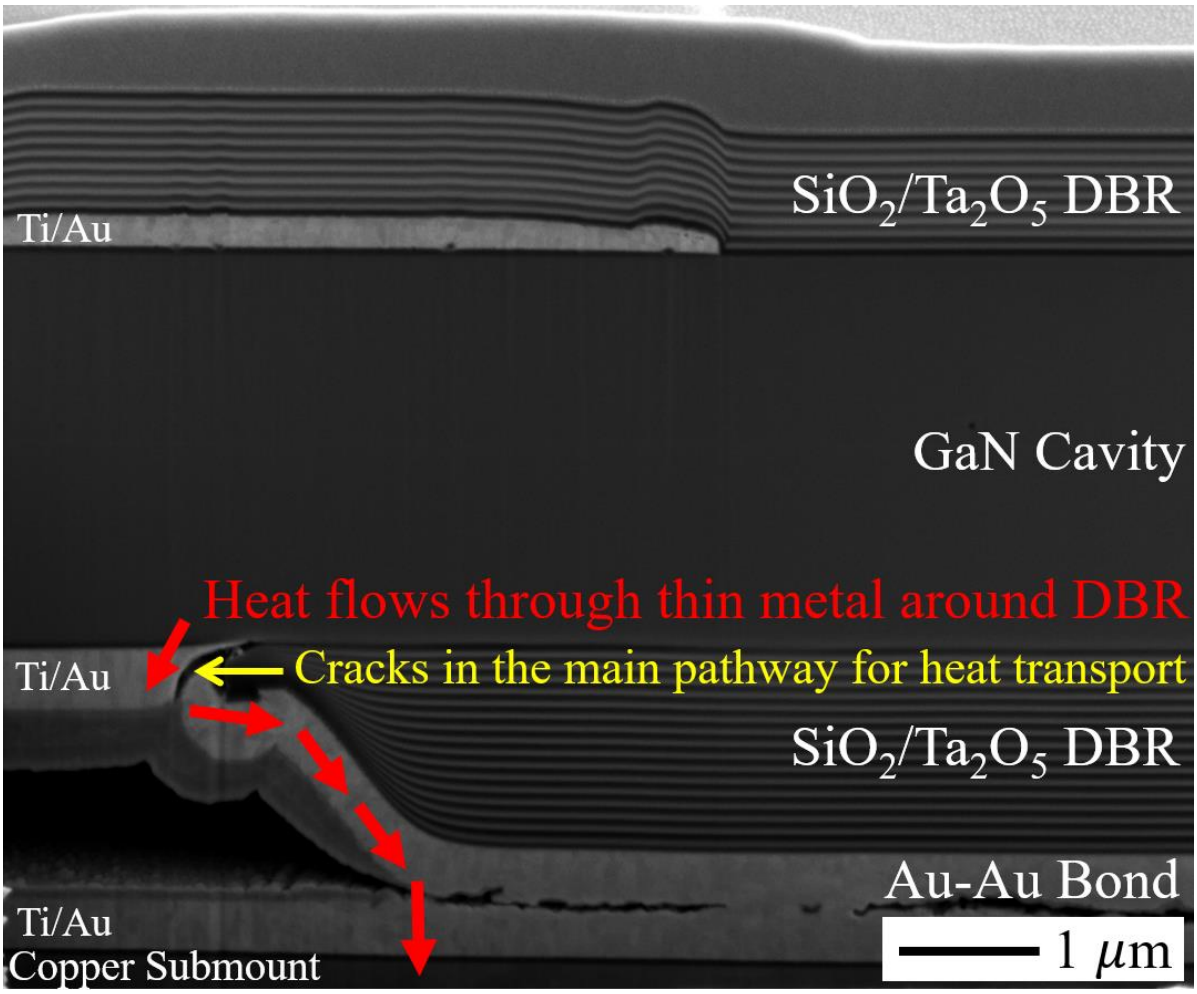


Figure 95. FIB cross-section SEM image illustrating the poor thermal performance of previous nonpolar VCSELs due to the thermally-insulating bottom dielectric DBR. Instead of flowing through the bottom DBR, heat flows around it through a thin metal p-side contact that conforms around the bottom DBR. There were cracks in this metal pathway that appeared after Au-Au bonding, which further restricted heat flow. The thermal performance was greatly improved in the recent VCSEL design by utilizing Au-In bonding to create a thicker and more robust metal pathway for heat flow.[73]

Cracks in the main metal pathway for heat transport significantly degrades the thermal performance according to COMSOL simulations and was likely one of the main factors that prevented CW operation in previous devices. A crack was simulated in the COMSOL model by inserting a small gap next to the Au on the sidewall of the bottom DBR, as shown in Figure 96.

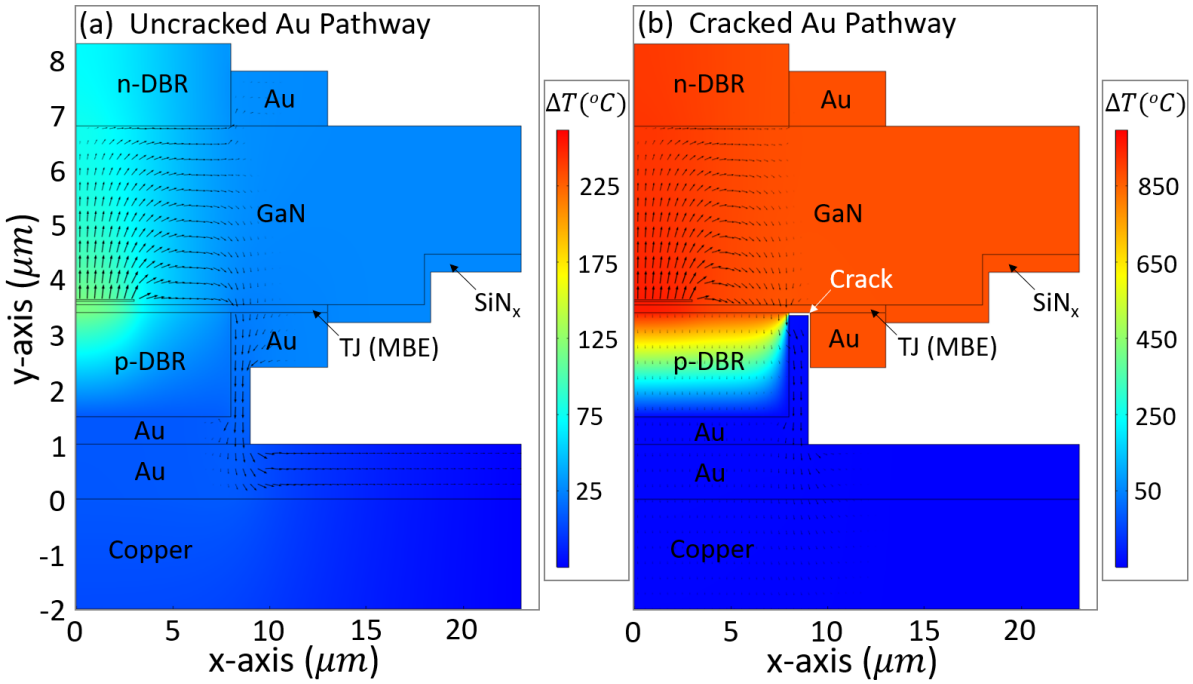


Figure 96. COMSOL thermal model of a 6 μm aperture diameter 23λ VCSEL with (a) an uncracked 1-μm-thick Au pathway for heat transport along the sidewall of the bottom DBR and (b) a device with a crack in the Au pathway for heat transport. The increase in temperature is shown by the color scheme and the thermal flux is shown by the overlain arrows. Due to the thermally-insulating bottom dielectric DBR, the main pathway for heat transport is through the thin Au contact on the sidewall of the bottom DBR toward the flip-chip substrate.

Figure 96(a) shows an uncracked device with a thermal impedance of 992 °C/W, and Figure 96(b) shows a simulation of a cracked device with a much higher predicted thermal impedance of 8700 °C/W. Therefore, it is important for devices to have crack-free metal on the sidewall of the bottom DBR. Further simulations showed that increasing the thickness of the metal on the sidewall of the bottom DBR could improve the thermal performance, but it is deposited using conformal electron beam evaporation which limits the thickness to ~1 μm.

Cracking was caused by the high temperature and pressure during Au-Au thermocompression flip-chip bonding and was exacerbated by the various coefficients of thermal expansion for the several materials within the VCSEL devices. Note that the device shown in Figure 95 appeared crack-free when viewing the device using optical microscopy, but the crack in the p-side metal contact was only visible when viewing the FIB cross-section.

Other than this, cracks through VCSEL devices were readily observable via optical microscopy. Therefore, to improve VCSEL yield and thermal performance, a series of flip-chip bonding experiments were performed. Section 4.4.6.1 discusses Au-Au thermocompression bonding experiments and Section 4.4.6.2 describes the development of Au-In solid-liquid interdiffusion (SLID) bonding, which led to the most significant improvements in yield, thermal performance, and enabled CW operation.

4.4.6.1. Au-Au Bonding Experiments

Low yield after flip-chip bonding has been a tremendous problem for each of the VCSEL designs from UCSB. This led to several Au-Au thermocompression bonding experiments with the goal of improving the yield as well as creating a more robust p-side metal contact for heat transport. There were two problems that led to low VCSEL yield after flip-chip bonding and growth substrate removal via PEC etching. The first problem was that only a small percentage of devices would successfully transfer to the flip-chip substrate. Secondly, if a device successfully transferred to the flip-chip substrate, it had a very high probability of being cracked. Before discussing flip-chip bonding improvements, it is helpful to describe the previous Au-Au bonding method. Figure 97 shows images of the Au-Au thermocompression flip-chip bonding method that was used for previous *m*-plane GaN VCSELs.

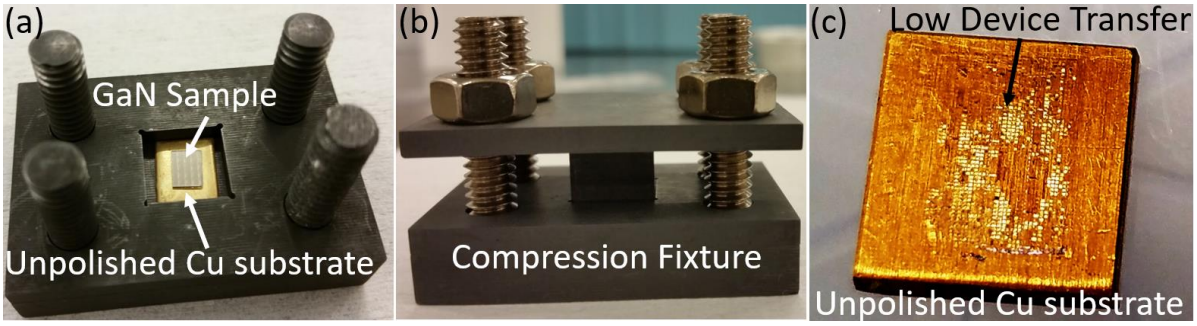


Figure 97. Au-Au thermocompression flip-chip bonding method used for previous *m*-plane GaN VCSELs. (a) GaN sample face-down on a gold-coated unpolished copper flip-chip substrate placed inside a graphite compression fixture. (b) Fully-assembled graphite compression fixture for thermocompression bonding at 200-300 °C for 2 hours. (c) After Au-Au bonding and PEC etching to remove the growth substrate, there was a low percentage of devices that successfully transferred to the unpolished copper flip-chip substrate.

In this flip-chip bonding process, the partially-processed GaN sample is placed face-down onto a gold-coated unpolished copper substrate that is placed within a graphite compression fixture, as shown in Figure 97(a). Figure 97(b) shows the fully-assembled graphite compression fixture that is subsequently placed in an oven at 200-300 °C for 2 hours for Au-Au thermocompression bonding. The bonding force was controlled by the four nuts on the graphite fixture, which were clamped finger-tight and then tightened an additional 1/8-turn. After removing the GaN growth substrate via PEC etching, there was typically a low percentage of devices transferred to the flip-chip substrate, as shown in Figure 97(c).

The first improvement that was made for the Au-Au bonding process was switching from unpolished copper substrates to polished copper flip-chip substrates, which greatly improved the average number of devices that transferred to the submount. This suggested that having a planar and uniformly gold-coated surface was important for each of the devices to bond to the submount. This makes sense as bonding is performed below the melting temperature of Au, so each device would need to be in contact with the Au-coated submount to bond, so a planar submount is ideal. Despite the improved device transfer percentage, there were cracks throughout nearly every device, as shown in Figure 98.

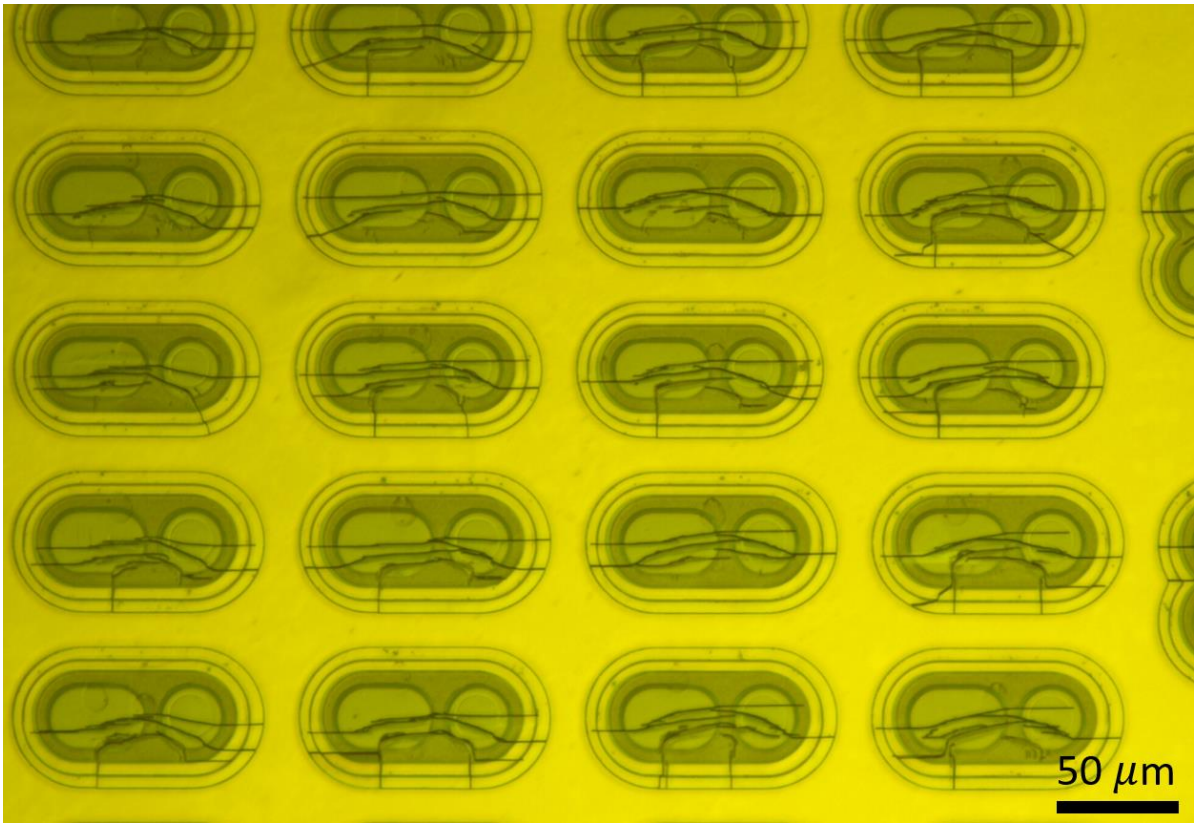


Figure 98. Optical micrograph of failed 13λ VCSELs after flip-chip bonding and growth substrate removal via PEC etching. While the polished copper flip-chip substrate improved the device transfer percentage, nearly every device was cracked.

The next goal was to decrease the number of cracked devices while maintaining a high device transfer percentage. In one experiment, the bonding force was reduced by tightening the four nuts on the graphite fixture finger-tight without the extra 1/8-turn, but the device transfer percentage was very low. Among eight different samples, bonding was attempted for cases in between those (e.g., finger-tight + ~1/16-turn), but there was always extensive cracking throughout the majority of the devices. The actual bonding force was unknown during these tests and likely varied significantly as they relied on qualitative factors (e.g., twisting the four nuts finger-tight).

The next major improvement in flip-chip bonding was accomplished by eliminating the graphite compression fixture and switching to the Finetech Fineplacer Lambda flip-chip bonder. Unlike the graphite compression mount, this tool is capable of precisely controlling the temperature, force, and time during flip-chip bonding. This led to a series of Au-Au bonding experiments with the goal of maximizing device transfer and minimizing cracking. However, at the time, there were very few remaining VCSEL samples that were ready for the flip-chip bond. Because it takes a significant amount of time to reach the flip-chip bonding stage in the VCSEL process (i.e., MOCVD calibration and growth, 6 photolithography steps, 3 dry etches, ion implantation, MBE TJ regrowth, SiN_x deposition, DBR calibration and deposition, and 2 metal depositions), simplified test samples were designed and fabricated for the initial Au-Au bonding experiment using the Finetech flip-chip bonder.

The bonding test samples were designed to have a relatively simple fabrication process compared to VCSELs while having a similar geometry that can resemble flip-chip bonding for real devices. The samples were also designed to be compatible with PEC undercut etching for growth substrate removal so that the device transfer percentage and percentage of cracked devices could be observed. Therefore, these test samples needed to have mesas with the same contact area as the VCSEL devices during bonding, Ti/Au on the mesas for bonding, a PEC metal cathode in the field (i.e., in the dry-etched region), and an exposed sidewall of the sacrificial MQW for PEC etching compatibility. While this could require up to three lithography steps, the test samples were designed with a fabrication process that only required a single lithography step for the mesa etch.

The contact area during flip-chip bonding of actual VCSEL samples consists of the circular and elliptical p-DBR structures that are coated with Ti/Au. Therefore, to have the same flip-chip bonding contact area, photolithography was performed using the *p-DBR* mask to define the mesas for the test samples. While a negative photoresist is used in a lift-off process to deposit the p-DBR in the VCSEL process, a positive photoresist (SPR 220-7.0) was used for the test samples so that mesas could be dry-etched with the same areal dimensions as the p-DBR pattern. A Cl_2 RIE dry etch was performed to etch a depth of ~3 μm, which exposed the sidewall of both the active and sacrificial MQW layers. After removing the photoresist, a blanket deposition of Ti/Au was deposited using electron beam evaporation to form the bonding metal on top of the mesas as well as the PEC metal cathode in the field between mesas. While the bonding metal is usually deposited conformally for actual VCSEL devices (to coat the sidewall of the p-DBR), non-conformal deposition was used for the test samples because the sidewall of the sacrificial MQW needed to be uncovered so that it is compatible with the PEC undercut etching process. After metal deposition, the test samples were ready to be cleaved and used for flip-chip bonding experiments. Figure 99 shows images of the test samples for flip-chip bonding.

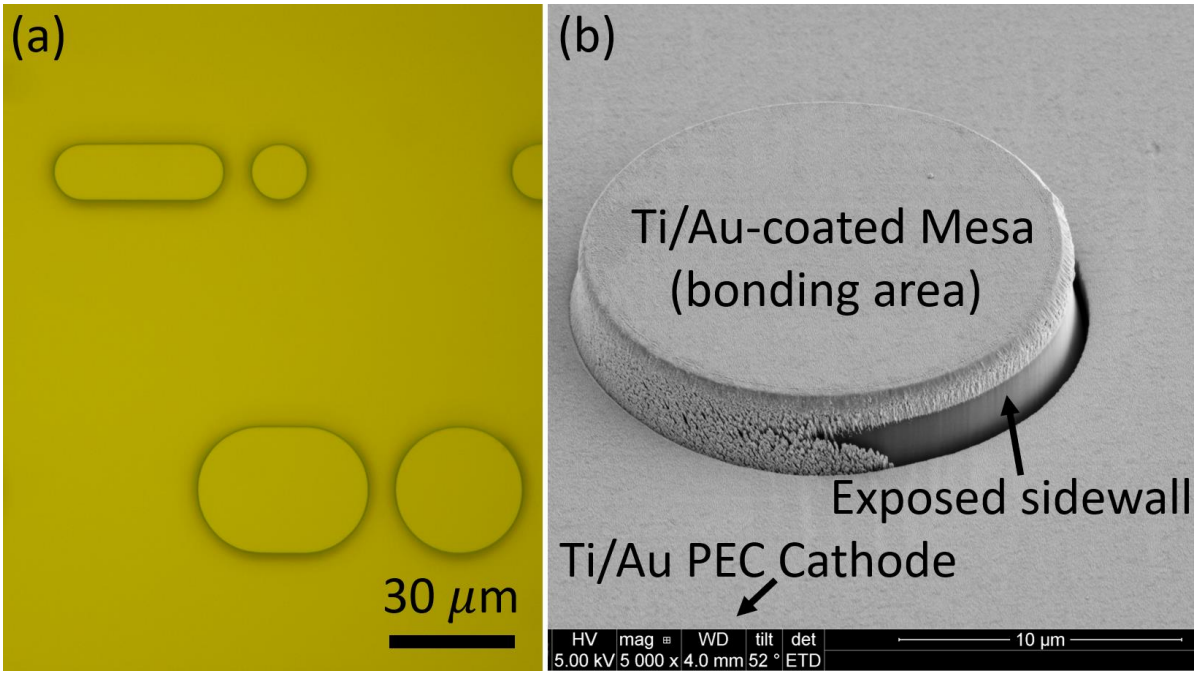


Figure 99. (a) Optical micrograph of a simplified test sample for flip-chip bonding experiments. The mesas have the same geometry as the p-DBR so that the contact area is equivalent to actual VCSEL samples during flip-chip bonding. (b) SEM image taken at a 52° tilt to view the sidewall of the mesa. Because non-conformal electron beam evaporation was performed at a slight angle, half of the mesa sidewalls were covered by Ti/Au while the other half was exposed. It is important that the sidewall of the sacrificial MQW is exposed so that these test samples are compatible with the PEC etching process for growth substrate removal.

Figure 99(a) is an optical micrograph of a test structure that shows the circular and semi-circular mesas that have the same contact area as the Au-coated p-DBR pattern on actual VCSEL devices. Figure 99(b) is an SEM image that was captured at an angle to view the sidewall of the mesa. Non-conformal electron beam evaporation was performed at a slight angle, so Ti/Au coated one half of the sidewall while the other half of the sidewall was uncovered. The sidewall of the sacrificial MQW needed to be exposed so that PEC undercut etching could be performed after bonding to remove the growth substrate. Lastly, Ti/Au (10 nm/1000 nm) was deposited onto polished copper flip-chip substrates using electron beam evaporation.

Using the bonding test samples and Ti/Au-coated polished copper flip-chip substrates, Au-Au thermocompression bonding experiments were performed using the Finetech flip-chip

bonder. With the main goal of maximizing device transfer and minimizing cracking, the aim of these experiments was to find the minimum temperature and bonding force that created a strong Au-Au bond. Based on recommended Au-Au bonding conditions for the Finetech, the first sample was bonded at a temperature of 330 °C, bonding time of 60 seconds, and an applied force of 400 N. However, the GaN substrate fractured during bonding. The next sample was bonded using the same conditions except the bonding time was reduced to 30 seconds. With an abundance of samples for bonding, the strength of the Au-Au bonds was initially characterized qualitatively by using tweezers to apply a shear force on the bonded GaN chip (i.e., using tweezers to squeeze the edge of the copper substrate and opposite edge of the GaN substrate). Using this method, the GaN substrate broke off using minimal force for the previous sample, showing that the Au-Au bond was very weak. For the third bonding test, the bonding time was increased, and the force was reduced (330 °C, 40 seconds, and 350 N). This created a much stronger Au-Au bond that could not be broken by applying a shear force on the sample using tweezers. As summarized in Table 4, additional qualitative flip-chip bonding tests were conducted with the goal of finding the minimum bonding force that created a strong Au-Au bond.

Table 4. Initial Au-Au thermocompression bonding results for test samples bonded using the Finetech flip-chip bonder.

Temperature (°C)	Time (s)	Force (N)	Result
330	60	400	GaN fractured
330	30	400	Weak bond
330	40	350	Strong bond
330	40	350	GaN fractured
330	40	330	Strong bond
330	40	315	Strong bond
330	40	305	Strong Bond

Based on these results, the lowest bonding force that created a strong bond was 305 N at a temperature of 330 °C and bonding time of 40 seconds.

Several additional flip-chip bonding tests were conducted and then PEC undercut etching was performed using 1 M KOH with a 405 nm LED array in order to remove the growth substrate. After substrate removal, optical micrographs were taken to see the percentage of devices that successfully transferred to the flip-chip substrate. The device transfer percentage was estimated based on the difference in device area before and after the bonding and PEC process. Table 5 summarizes the Finetech flip-chip bonding conditions and the approximate percentage of devices that successfully transferred to the flip-chip substrate after bonding and PEC etching.

Table 5. Finetech flip-chip bonding conditions and the percentage of devices that successfully transferred to the flip-chip substrate after bonding and growth substrate removal via PEC undercut etching.

Temperature (°C)	Time (s)	Force (N)	Device Transfer
330	60	400	100%
330	30	300	78%
330	40	350	55%
330	40	350	50%
330	40	305	80%
330	40	300	75%
300	120	280	35%
320	180	300	35%
300	280	300	78%
320	180	300	76%
300	280	300	32%
280	280	280	40%
320	180	280	77%
310	280	300	100%
300	280	300	93%
310	280	300	72%
310	280	300	80%
300	280	300	20%
310	280	300	100%
315	280	300	54%

These results indicated that it was beneficial to increase the bonding time, which enabled a high device transfer percentage at lower bonding temperatures and forces. The minimum bonding conditions for ~100% device transfer was at a temperature of 310 °C, bonding time of 280 seconds, and applied force of 300 N. However, these bonding conditions had varying results for three other trials (e.g., 72%, 80%, and 100%). Using the same conditions except reducing the temperature to 300 °C resulted in device transfer percentages of 20% and 93%. Reducing the bonding force to 280 N resulted in a device transfer percentage of 77% or lower based on the temperature and bonding time. Although there were varying results, these tests suggested that the optimal minimum bonding conditions for device transfer were 310 °C, 280 seconds, and 300 N.

The next step was to perform optical microscopy to see if there was a trend between the flip-chip bonding conditions and the percentage of cracked devices. With ~1000 devices on each sample, this was a time-consuming process that involved inspecting each device for cracking. This analysis was performed for six VCSEL samples that each had a device transfer percentage greater than 70%, and the results are summarized in Table 6.

Table 6. Finetech flip-chip bonding conditions, device transfer percentage, and the percentage of crack-free apertures and crack-free devices after flip-chip bonding and PEC etching.

Temperature (°C)	Time (s)	Force (N)	Device Transfer	Crack-Free Apertures	Crack-Free Devices
320	180	300	76%	32%	22%
320	180	280	77%	30%	1%
310	280	300	100%	49%	18%
310	280	300	72%	17%	2%
310	280	300	100%	41%	14%
300	280	300	93%	21%	4%

In addition to the percentage of crack-free devices, the percentage of crack-free apertures was also recorded because those devices may still be able to lase. The sample with the

highest yield had 100% device transfer, 49% of the apertures crack-free, and 18% of devices that were completely crack-free. That sample was bonded at a temperature of 310 °C, bonding time of 280 seconds, and force of 300 N. However, there were variable results as another sample bonded at those same conditions had 72% device transfer, 17% crack-free apertures, and only 2% of crack-free devices.

These flip-chip bonding optimization experiments helped improve the VCSEL yield, but the yield was still very low for most samples. Lowering the temperature and force further during bonding could possibly help reduce cracking, but the device transfer percentage decreased for temperatures lower than 300 °C or forces below 300 N. This led to an investigation into other types of bonding that could be performed at a lower temperature and pressure. One potential solution was to perform thermosonic bonding using the Finetech flip-chip bonder. Thermosonic bonding is similar to thermocompression bonding but it can be performed at lower temperatures and bonding forces because it also involves applying ultrasonic energy to soften the metal and promote metallic bonding at the interface.[177] However, thermosonic bonding produced very weak bonds for test samples, and Table 7 summarizes the bonding conditions and results.

Table 7. Finetech flip-chip bonding conditions, device transfer percentage, and the percentage of crack-free apertures and crack-free devices after flip-chip bonding and PEC etching.

Temperature (°C)	Time (s)	Force (N)	Ultrasonic Power (mW)	Result
165	1.2	1.5	800	No bond
165	1.2	1.5	2500	No bond
200	1.2	1.5	2500	No bond
200	1.2	1.5	4500	Very weak bond
160	1.2	8	3000	Weak bond

Most of the thermosonic bonding tests were either unsuccessful or the bonding test samples could be easily removed from the flip-chip substrate with tweezers. Thermosonic bonding was not successful likely due to the relatively large device bonding area of ~1 mm^2 for the

VCSEL samples while Finetech thermosonic bonding is usually suitable for samples with less than 0.1 mm^2 of contact area. Due to the unsuccessful thermosonic bonding results and unsuitable device bonding area, other methods of bonding were investigated. As discussed in Section 4.4.6.2, VCSEL yield and thermal performance was significantly improved by utilizing Au-In solid-liquid interdiffusion (SLID) bonding.

4.4.6.2. Au-In SLID Bonding

While the previous Au-Au bonding experiments improved the yield slightly, the largest improvement in VCSEL yield was achieved by using Au-In solid liquid interdiffusion (SLID) bonding. Furthermore, utilizing Au-In SLID bonding was one of the most significant thermal improvements that led to the first demonstration of CW lasing for *m*-plane GaN VCSELs.

Despite performing several Au-Au thermocompression bonding experiments with the goal of improving the VCSEL yield, cracking and low device transfer percentage were still significant problems. Reducing the temperature and bonding force slightly lowered the degree of cracking, but lowering the temperatures and force further resulted in low device transfer percentage. After none of the previous Au-Au bonding experiments could solve the VCSEL yield problem, this led to an idea that would simultaneously solve the yield issue while also improving the VCSEL thermal performance to achieve CW operation. Au-Au thermocompression bonding forms a bond through atomic diffusion, and requires a relatively high temperature and bonding force as the melting temperature for gold is 1064 °C. Several problems could be solved by replacing Au-Au bonding with a technique that incorporates a liquid metal phase during bonding, such as SLID bonding. This would enable flip-chip bonding at significantly lower bonding forces to help reduce cracking. The relatively soft

bonding metal could also potentially reduce cracking by providing cushioning as the bonding surfaces are pressed together. Furthermore, the VCSEL thermal performance could be greatly improved by utilizing a liquid metal phase during bonding to completely embed the p-DBR within metal. Embedding the thermally-insulating p-DBR within metal would create a much thicker metal pathway for heat transport, especially compared to previous *m*-plane VCSELs in which heat flow was bottlenecked through a cracked 1-μm-thick gold contact along the sidewall of the bottom DBR. The next step was to choose a metal alloy system that had a low melting temperature. Gold-tin (Au-Sn) alloys were one possible alternative as they have a fairly low melting temperature of 280 °C at the eutectic composition of 80% Au and 20% Sn.[178] This may have been an effective solution, but 280 °C is not much lower than the temperature used in the previous Au-Au bonding experiments, so cracking could remain a problem.

One of the best alternatives was to use Au-In SLID bonding because Au-In alloys have a unique low-temperature liquid phase above ~156 °C for In-rich alloys (above 54 wt.% In),[179] as shown in the Au-In phase diagram in Figure 100.

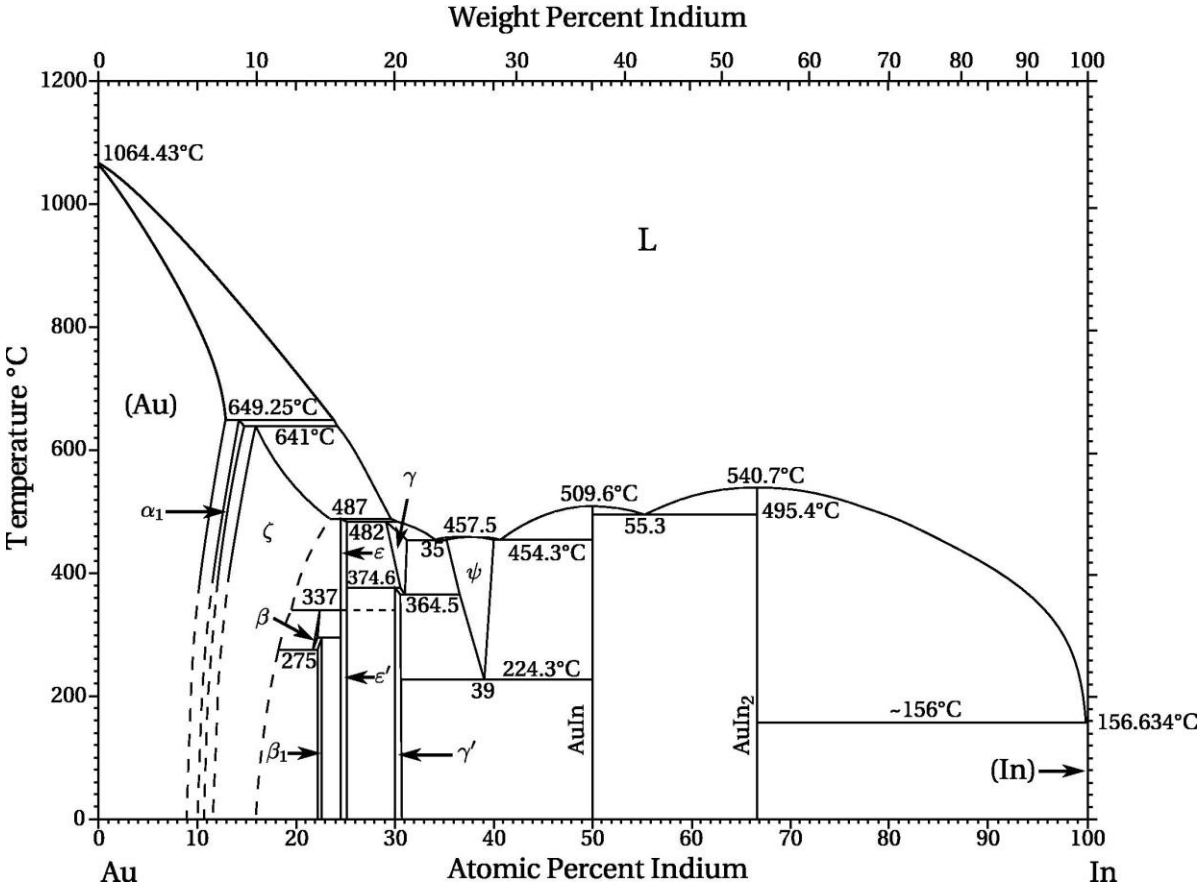


Figure 100. The Au-In binary phase diagram. In-rich Au-In alloys (above 54 wt.% In) are ideal for SLID bonding because they have a relatively low temperature liquid phase above ~156 °C. By designing the Au-In composition to be below 54 wt.% In after bonding, the Au-In bond can withstand higher temperatures without remelting, such as up to 495.4 °C for compositions between 36.8-54 wt.% In.[180] Reprinted from [Deillon, L., Hessler, T., Hessler-Wyser, A., & Rappaz, M. (2014). Growth of intermetallic compounds in the Au–In system: Experimental study and 1-D modelling. Acta Materialia, 79, 258–267. https://doi.org/10.1016/J.ACTAMAT.2014.07.025], ©2014 with permission from Elsevier.

This enables flip-chip bonding at much lower temperatures and forces compared to Au-Au or Au-Sn bonding while also incorporating a liquid metal phase. As seen in the phase diagram, Au-In alloys with In compositions above 54% consist of a mixture of an In phase and $AuIn_2$ intermetallic compound (53.8 wt.% In) with a solidus temperature of 156 °C.[179] Above 156 °C, the mixture forms a liquid phase with $AuIn_2$ grains. The alloy becomes a mixture of AuIn (36.79 wt.% In) and $AuIn_2$ intermetallic compounds for compositions between 36.8-54 wt.% In, and the solidus temperature becomes much higher with a value of 495.4 °C. This considerable difference in solidus temperatures is a particularly useful feature because it

enables a relatively low-temperature liquid phase above 156 °C during bonding (for > 54 wt.% In alloys) while the final alloy can be designed to have a lower In composition so it can withstand temperatures up to 495.4 °C without melting (for 36.8-54 wt.% In alloys).

Before proceeding with Au-In SLID flip-chip bonding experiments, a literature review was conducted to explore possible bonding designs, which are summarized in Figure 101.

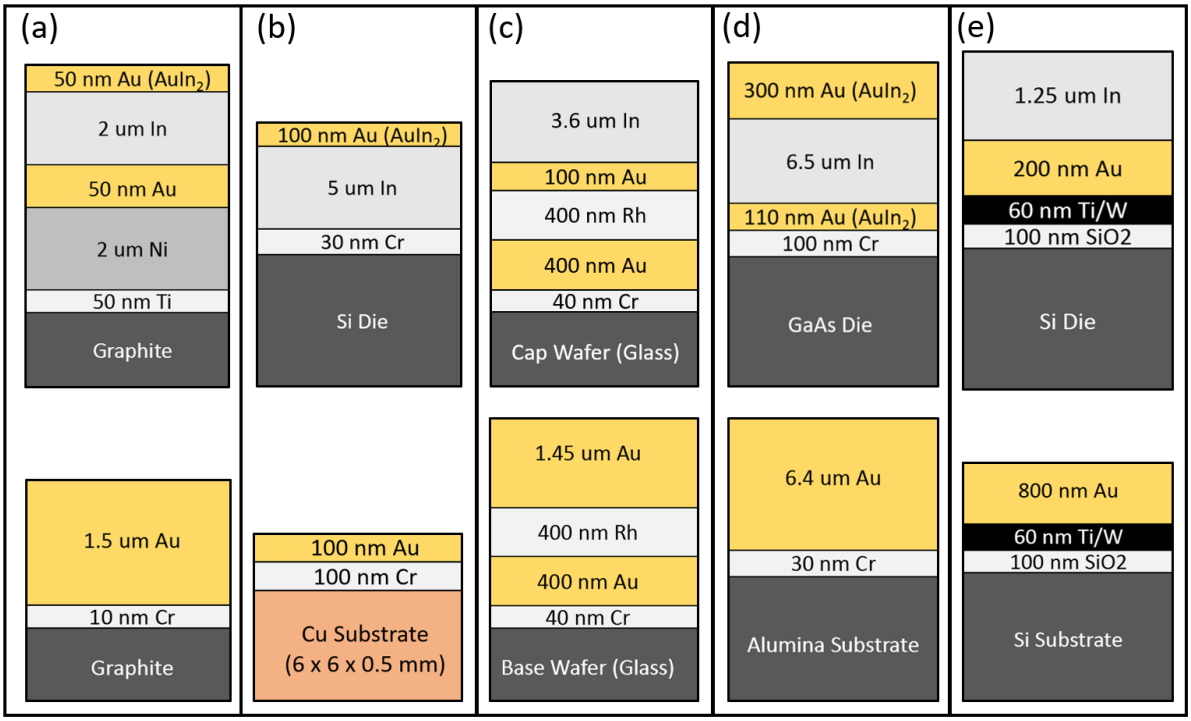


Figure 101. Schematic illustrations of five different Au-In bonding designs reported in the literature showing the top and bottom bonding structures. Note that the dimensions of the structures are not drawn to scale and the top structure is flipped upside down during bonding in each design. The bonding conditions and indium compositions are described for each design: (a) Au-In bonding was performed at 210 °C for 10 min with an applied pressure of 19.61 MPa. The indium composition before and after bonding was ~88 wt.% and ~32 wt.% indium, respectively. [181] (b) Au-In bonding was performed at 180 °C for 5 min at an applied pressure of 0.27-0.34 MPa in a H_2 ambient. The indium composition before and after bonding was ~95 wt.% and ~90 wt.% indium, respectively.[179] (c) Au-In bonding was performed at 200 °C for 15 min at an applied pressure of 2.5 MPa in an Ar ambient. The indium composition before and after bonding was ~93 wt.% and 47 wt.% indium, respectively.[182] (d) Au-In bonding was performed at 200 °C for 10-15 min at an applied pressure of 0.414 MPa. The indium composition before and after bonding was ~86 wt.% and ~27 wt.% indium, respectively.[183] (e) Au-In bonding was performed at 180 °C for 30 min. The indium composition before and after bonding was ~70 wt.% and ~32 wt.% indium, respectively.[184]

Each of the Au-In SLID bonding designs consisted of two bonding wafers. The first wafer was coated mainly with Au while the second wafer was coated with both Au and In with an

In composition greater than 54 wt.% In so that a liquid phase could obtained during bonding above 156 °C. To prevent oxidation, a thin Au layer can be deposited above In, which forms a stable $AuIn_2$ intermetallic compound after deposition.[179] After bonding the two wafers together, the composition of the Au-In alloy decreased below 54 wt.% In, which allows the Au-In alloy to withstand much higher temperatures over 450 °C without remelting. The chromium (Cr), titanium/tungsten (Ti/W), and Ti layers were used for adhesion. Nickel (Ni) was used as a wetting layer for the liquid phase, and rhodium (Rh) layer was used as a diffusion barrier during bonding.

The next step was to design and perform Au-In SLID flip-chip bonding experiments. Silicon and sapphire wafers were used for initial testing. Ti/Ni/Au (20/100/100 nm) was deposited using electron beam evaporation prior to depositing In/Au (2000/100 nm). Before bonding, the composition consisted of 79 wt.% In (21 wt.% Au), which is above 54 wt.% In so that a liquid phase could be obtained above 156 °C. After bonding to a device with 1-μm-thick Au, the composition would decrease to 39 wt.% In, which should have thermal stability at much higher temperatures. Note that after In/Au (2000/100 nm) deposition, the flip-chip substrates appeared grey-colored (as opposed to gold-colored) because In readily diffuses into the 100 nm Au layer to form $AuIn_2$. Au and In pellets were placed in tungsten boats that were heated during thermal evaporation. Due to the high temperature required during Au evaporation, In pellets were found to melt if placed in the nearby tungsten boat. To verify that In was not evaporating during Au deposition, a Au-filled tungsten boat was heated until the Au was fully evaporated and the deposition rate from the crystal monitor showed 0 nm/s. Although the In pellets partially melted, the deposition rate was negligible, so this was not a problem. Au-In SLID bonding was performed using a Finetech flip-chip bonder with the

following sequential steps: the temperature was increased to 140 °C, the metal bonding surfaces were placed into contact, 30 N of force was applied, the temperature was increased to 210 °C, these conditions were held for a duration of 300 seconds, the temperature was decreased below 40 °C, and the applied force was released as it was allowed to cool to room temperature. Placing the surfaces into contact just below the solidus temperature has been reported to reduce squeeze-out of indium.[185] Figure 102(a) shows optical micrographs for VCSELs bonded using Au-Au thermocompression bonding, and Figure 102(b) shows VCSELs that were bonded using Au-In SLID bonding.

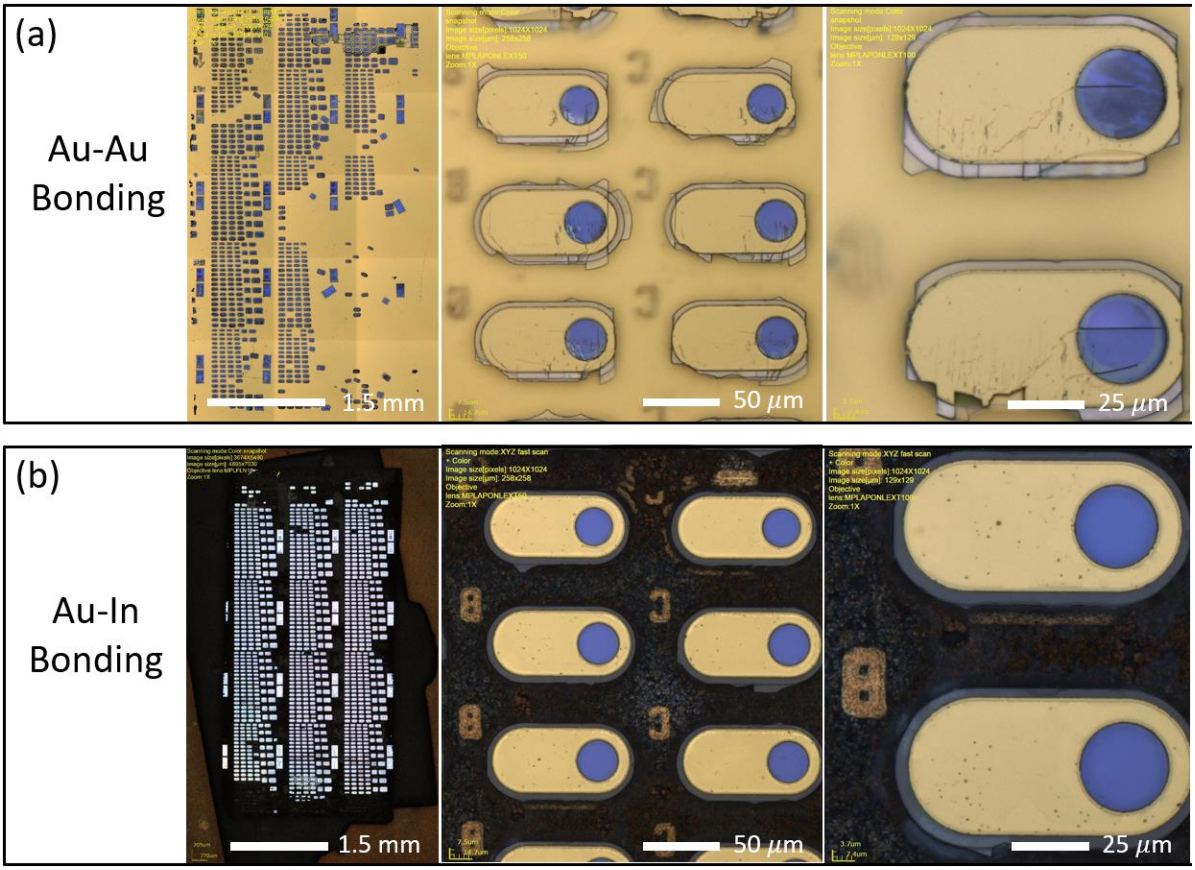


Figure 102. Optical micrographs showing VCSEL devices fabricated using (a) Au-Au thermocompression bonding and (b) Au-In SLID bonding. Au-In SLID bonding significantly improved the VCSEL yield, thermal performance, and led to CW operation.

Au-In SLID bonding significantly improved device transfer percentage and cracking compared to Au-Au thermocompression bonding. While heat flow was previously restricted

to the thin p-side metal that conforms around the bottom DBR (as shown in Figure 95), Au-In SLID bonding solved this problem by creating a much thicker metal pathway for heat transport, as shown in Figure 103.

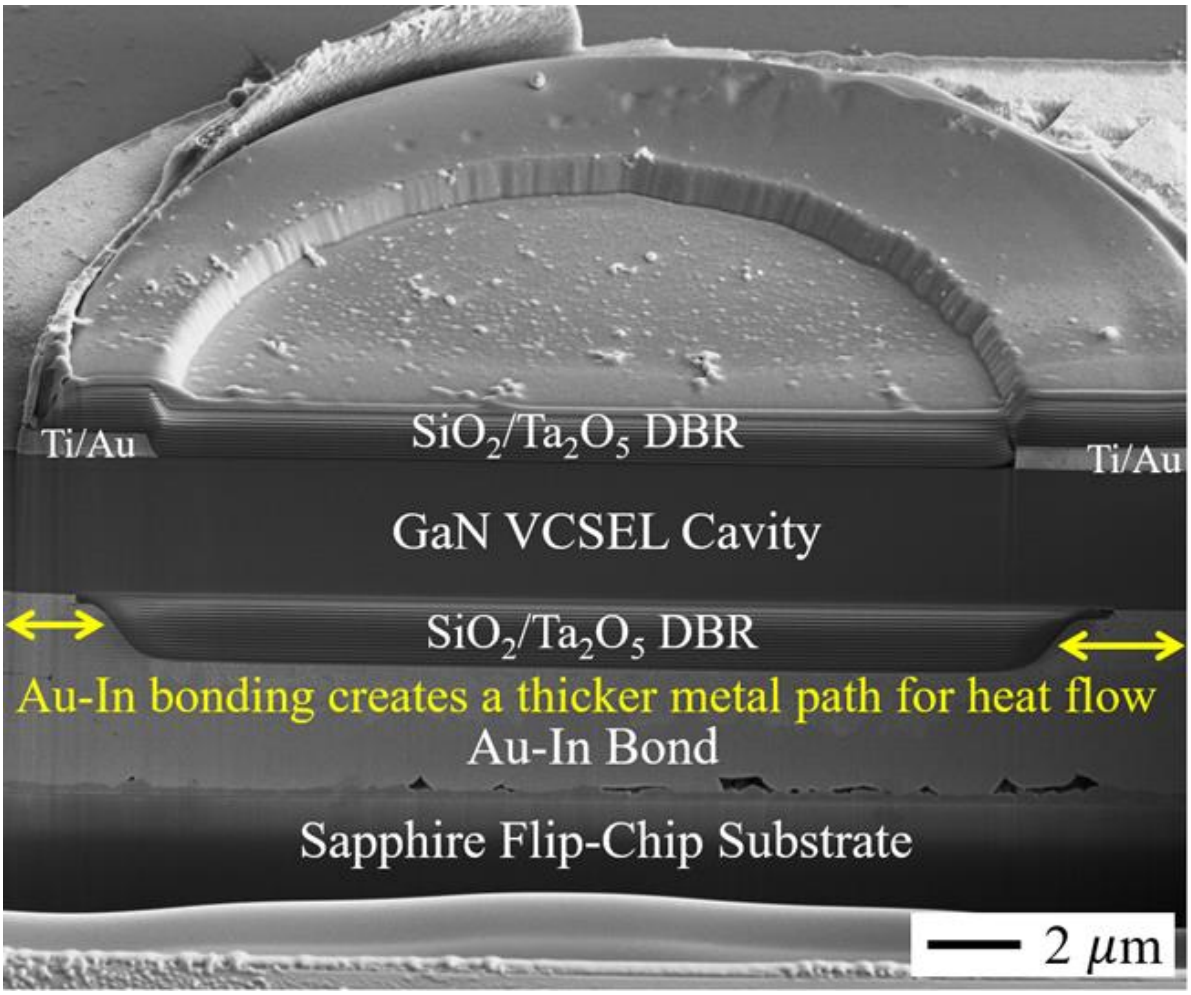


Figure 103. FIB cross-section SEM image of the recent nonpolar VCSEL design. CW lasing was achieved by using Au-In bonding to create a thicker metal path for heat flow and by implementing a longer 23λ cavity length.

The bottom dielectric DBR was completely embedded within metal due to the Au-In SLID bonding. With a thicker metal pathway for heat transport, this greatly improved the thermal performance and enabled CW operation, as further discussed in Section 4.5.

4.5. CW Operation Achieved for *m*-plane GaN VCSELs

After performing failure analysis on the previous VCSELs that were unable to lase, several improvements were made to the VCSEL design, as described in Section 4.5.1 and Section 4.5.2. The main issue that prevented lasing in previous VCSELs was roughness prior to the DBR deposition on both the n-side and p-side of the devices. Surface roughness increased the threshold for lasing by contributing both to scattering loss and mirror loss, as FIB cross-section images showed roughness propagating through the DBR mirrors. Section 4.5.2 describes the roughness improvements that were made with the MBE TJ regrowth on the p-side and surface morphology on the n-side after PEC etching. Thermal simulations showed that the main pathway for heat transport was around the bottom DBR through a relatively thin metal contact, but FIB cross-sectioning of failed VCSELs revealed cracks in that p-side metal contact which would further degrade the thermal performance and prevent CW operation. The thermal performance was significantly improved by utilizing Au-In solid-liquid interdiffusion (SLID) bonding to create a much thicker metal pathway for heat transport. This led to the first demonstration of CW lasing of nonpolar *m*-plane GaN-based VCSELs. Lasing was stable under CW operation for over 20 minutes without the presence of filamentary lasing within the aperture.

4.5.1. VCSEL Design and Experimental Methods

Similar to the previous devices, these VCSELs had a dual dielectric DBR design, ion implanted current aperture, and a TJ intracavity contact grown by MBE. Atmospheric pressure MOCVD was performed on free-standing *m*-plane GaN with an intentional 1° miscut in the [000$\bar{1}$] direction. In the order of growth, the epitaxial structure consisted of a ~1.2 μm n-GaN template, sacrificial 3×MQW with 7 nm InGaN QWs and 5 nm GaN barriers, 26 nm n^{++}GaN, 15 nm n-AlGaN, 3217 nm n-GaN, active 2×MQW region with 14 nm QWs and 1 nm GaN barriers, 5 nm p-AlGaN electron-blocking layer (EBL), 60 nm of p-GaN, and 14 nm of p^{++}GaN. The sacrificial MQW had a target emission wavelength of 420 nm and the active MQW targeted a wavelength of 405 nm. After p-GaN activation at 600 °C for 15 minutes, Ar/Cl_2 reactive ion etching (RIE) was performed to etch a mesa past the active MQW but not past the sacrificial MQW. After depositing a Pd/Au hardmask, the current aperture was formed using Al ion implantation, performed at Leonard Kroko, Inc. The Pd/Au hardmask was removed by submerging the samples for 30 minutes in a boiling solution of aqua regia (3:1 $HCl:HNO_3$). After performing a solvent clean, a one-hour 400 °C bake was performed in the ammonia MBE chamber prior to TJ regrowth (NH_3 pressure ~1×10^{-6} Torr) at 740 °C with a non-incorporating In surfactant (In flux ~4×10^{-8} Torr). The MBE regrowth consisted of n^{++}GaN/n-GaN/n^{++}GaN (39.6/61.7/39.6 nm) with respective Si concentrations of 1.1×10^{20}, 2.5×10^{18}, and 1×10^{19} cm^{-3}. After removing MBE-grown GaN from the sidewalls by RIE, IBD was used to deposit 325 nm of SiN_x to protect the active MQW sidewall during the PEC undercut etching process to remove the growth substrate at a later stage. After depositing a

16-period Ta_2O_5/SiO_2 p-side DBR using IBD, a deeper RIE step was performed to etch past and expose the sidewall of the sacrificial MQW. An angled rotating e-beam evaporation fixture was used to deposit a conformal coating of Ti/Au (20/1000 nm) around the DBR as well as to deposit the PEC cathode in the field between devices. In previous Au-Au-bonded *m*-plane GaN VCSELs, this ~1-μm-thick metal layer has been the main pathway for heat transport around the bottom dielectric DBR. On a sapphire flip-chip substrate, Ti/Ni/Au (20/100/100 nm) was deposited using e-beam evaporation and In/Au (2100/350nm) was deposited using thermal evaporation. Au-In SLID bonding was performed using a Finetech Fineplacer Lambda flip-chip bonder with the following sequential steps: the temperature was increased to 140 °C, the metal bonding surfaces were placed into contact, 30 N of force was applied, the temperature was increased to 210 °C, these conditions were held for a duration of 300 seconds, the temperature was decreased below 40 °C, and the applied force was released as it was allowed to cool to room temperature. The *m*-plane GaN growth substrate was removed by selectively etching a sacrificial MQW using PEC undercut etching in a 1 M KOH solution with an LED array ($\lambda = 390$ nm) illumination source. A residue that formed after PEC etching was removed by using a foam swab to clean the sample with Tergitol detergent. Lastly, a Ti/Au (10/500 nm) n-electrode was deposited, followed by a 12-period Ta_2O_5/SiO_2 DBR. Figure 104 shows a schematic illustration of the VCSEL structure.

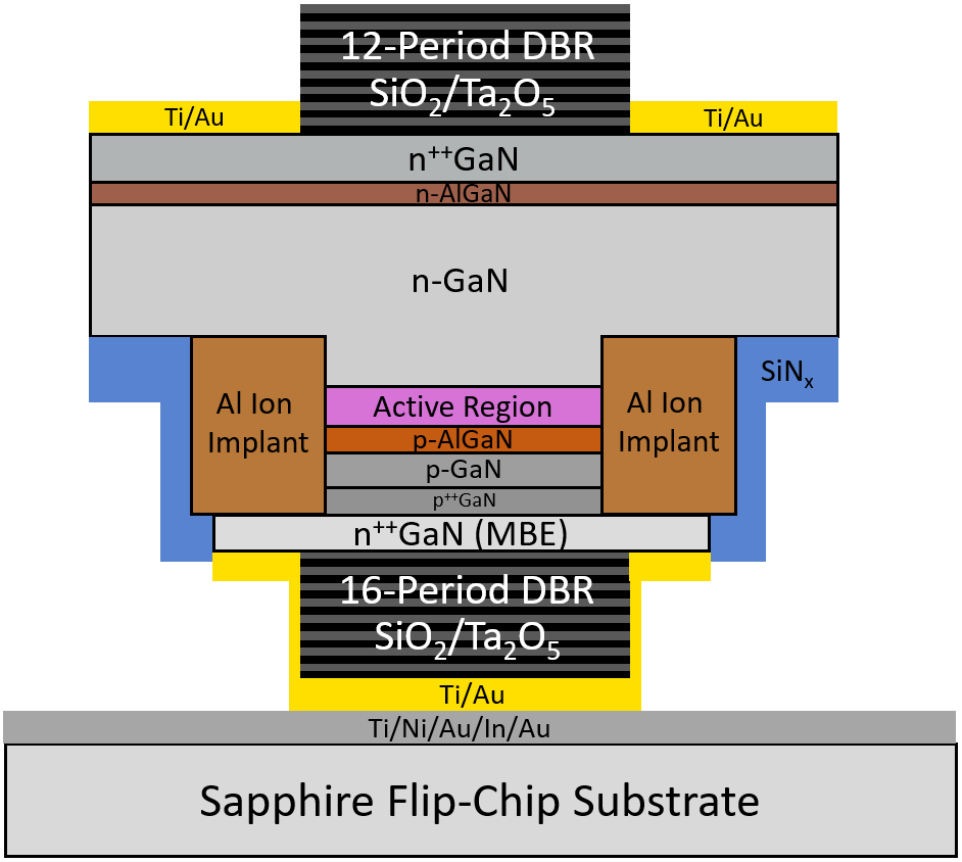


Figure 104. Schematic illustration of the VCSEL structure. Note that the metal layers on the flip-chip substrate are shown as-deposited and the effects of Au-In SLID bonding are not shown. In the actual devices, the bottom DBR was completely embedded within Au-In bonding metal, which greatly improved the thermal performance.

Sapphire was co-loaded during IBD deposition to measure the DBR reflectance using a Cary 500 spectrophotometer. Optical microscopy, SEM, and AFM were used to characterize the surface morphology and roughness in the aperture prior to DBR deposition on both the n-side and p-side of the devices. During VCSEL electrical characterization, a temperature of 21 °C was maintained using a thermoelectric stage controlled by an ILX Lightwave LDT-5948 Precision Temperature Controller. Time-averaged photocurrent vs. current data was collected using a large-area Si photodetector (API SD 444-12-12-171) connected to a Keithley 2400 SourceMeter. The VCSEL emission spectrum was collected using a 50 μm optical fiber to couple light into an Ocean Optics USB2000 spectrometer with a 2 nm spectral resolution. By

placing a thin film polarizer (Newport 10LP-VIS-B) below the multi-mode fiber, the spectrum was recorded at various polarization angles.

4.5.2. Key Design Improvements

Compared to the previous highest-performing *m*-plane GaN VCSEL in Ref. 58, the main differences in the VCSEL design were the increased cavity length of 23λ instead of 7λ, Au-In SLID flip-chip bonding instead of Au-Au bonding, MBE regrowth using an In surfactant, thicker QW active region, and the removal of a residue that appears after PEC etching.

The earlier 23λ VCSEL design was unable to lase due to the relatively thick 1642 nm MBE regrowth that created a rough morphology with 6 nm RMS roughness. This inhibited lasing due to significant levels of scattering loss with predicted values over 90 cm^{-1} for 6 nm RMS roughness.[167] This rough morphology was caused by two main factors. First, while MOCVD growth produces smooth surfaces with less than 1 nm RMS roughness on *m*-plane GaN with a -1° miscut in the *c*-direction, this is a suboptimal miscut for MBE growth which resulted in a particularly rough morphology. Secondly, the 1642 nm MBE regrowth was over ten times thicker than used in previous *m*-plane GaN TJ VCSELs,[58] which led to a higher degree of surface roughness. FIB cross-section SEM images revealed that roughness propagates through the bottom-side DBR, which would further inhibit lasing due to decreased mirror reflectance.

The roughness on the p-side was reduced in the recent VCSEL design by decreasing the MBE regrowth thickness to 141 nm and by using a non-incorporating In surfactant during growth, which has been shown to smoothen the growth surface.[168,169] This produced a

smoother surface with ~2 nm RMS roughness on the p-side prior to the bottom-side DBR, as shown in

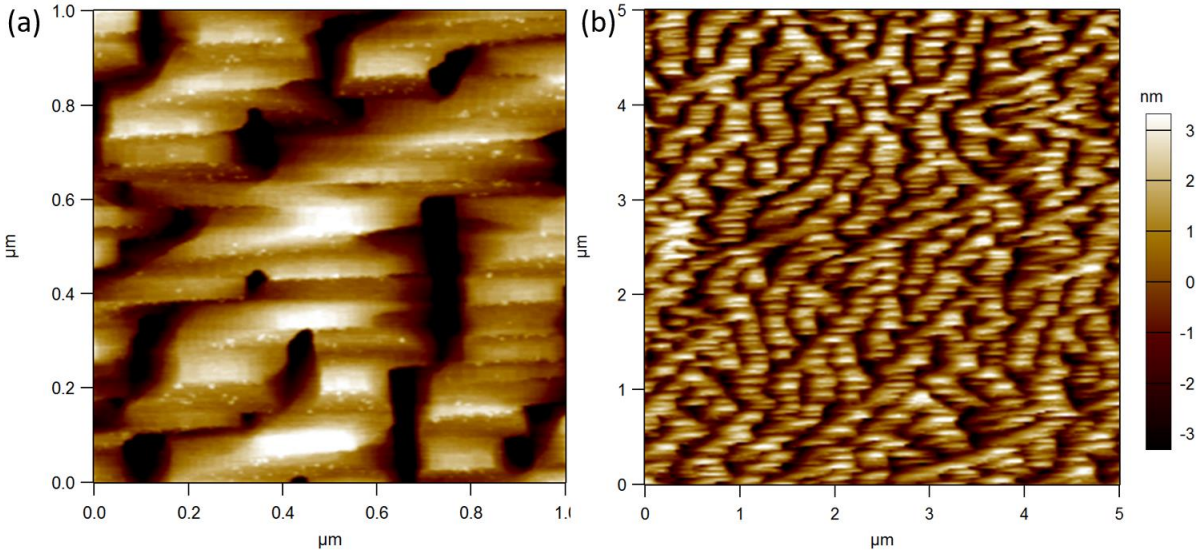


Figure 105. AFM scans after MBE TJ regrowth for a 23λ VCSEL showing roughness prior to the p-side DBR. The RMS roughness was (a) 2 nm for a 1 × 1 µm^2 AFM scan and (b) 1.5 nm for a 5 × 5 µm^2 scan.

The roughness was also reduced on the n-side of the devices prior to deposition of the topside DBR. The rough n-side surface appeared after the PEC undercut etch of the sacrificial MQW to remove the *m*-plane GaN growth substrate. After characterization with AFM, SEM, and EDX, the roughness turned out to be a residue on the surface of the n-GaN. Most of the residue could be removed using 11.7 M KOH, which suggested that it is a form of gallium oxide. SEM and AFM images were also comparable to images of gallium oxide in the literature. Furthermore, EDX revealed a higher oxygen peak on the residue. After removing most of the oxide residue in 11.7 M KOH for 45 minutes, SEM revealed a remaining cubic structure on the surface, which may be a form of indium oxide. One way to remove the remaining residue could be to submerge the samples in HCl, but HCl reacts with the indium on the flip-chip substrate. The most effective way to remove the residue has been to soak the

sample in Tergitol detergent and physically rub the sample gently using a foam swab. After removing the oxide residue, the surface was very smooth with an RMS roughness of ~0.5 nm.

Another key problem with the earlier VCSEL design was the poor thermal performance, which prevented them from lasing under CW operation. While thermal modeling predicted improved heat transport using a thicker 23λ cavity, there was still a bottleneck in heat flow due to the thermally-insulating bottom dielectric DBR. According to thermal simulations in COMSOL, instead of heat flowing through the bottom DBR, heat flows around it through a thin metal p-side contact that conforms around the bottom DBR. Thermal simulations showed that increasing the thickness of this p-side metal could improve the thermal performance, but it was deposited using e-beam evaporation which limits the thickness to ~1 μm. As shown in Figure 95, FIB cross-section SEM images revealed another problem where there were cracks in this metal pathway, which would further degrade the thermal performance. Exacerbated by the various coefficients of thermal expansion for the several materials in the VCSEL devices, cracking was caused by the high temperature and pressure during Au-Au thermocompression flip-chip bonding. Furthermore, the yield was particularly low after flip-chip bonding with cracks through entire VCSEL devices. This led to an investigation of Au-Au bonding conditions to minimize cracking, but the yield was only marginally improved. These thermal and yield issues were solved by implementing Au-In SLID bonding in the recent VCSEL design, which helped improve the thermal performance and enable CW lasing. The Au-In system is particularly suitable for flip-chip bonding because it has a relatively low-temperature liquid phase that occurs above 156 °C for Au-In alloys above 54 wt.% In.[179] This enabled bonding at much lower temperatures and pressures which significantly improved the yield and reduced cracking. While heat flow was previously

restricted to the thin p-side metal that conforms around the bottom DBR (as shown in Figure 95), Au-In SLID bonding solved this problem by creating a much thicker metal pathway for heat transport, as shown in Figure 103. This led to the first demonstration of CW operation for *m*-plane GaN-based VCSELs, as discussed in Section 4.5.4.

In summary, while roughness prior to DBR deposition prevented earlier VCSELs from lasing, the RMS roughness was reduced to 2 nm on the p-side by using an indium surfactant during MBE regrowth and the RMS roughness was reduced to 0.5 nm on the n-side after removing the oxide residue by swabbing in Tergitol. These improvements helped reduce the threshold for lasing by decreasing scattering loss and mirror loss. Based on the MOCVD growth experiments described in Section 4.4.1, a relatively thick QW active region (2×MQW with 14 nm QWs and 1 nm GaN barriers) was employed to compare to the previous design (7×MQW with 3 nm QWs and 1 nm GaN barriers). The VCSEL yield was significantly improved by switching from Au-Au bonding to Au-In SLID bonding. Au-In SLID also created a much thicker pathway for heat transport by embedding the bottom DBR within bonding metal. This improved the thermal performance and led to CW operation.

4.5.3. Lasing Characteristics Under Pulsed Operation

Photographs of an *m*-plane GaN-based VCSEL during operation above threshold are shown in Figure 106.

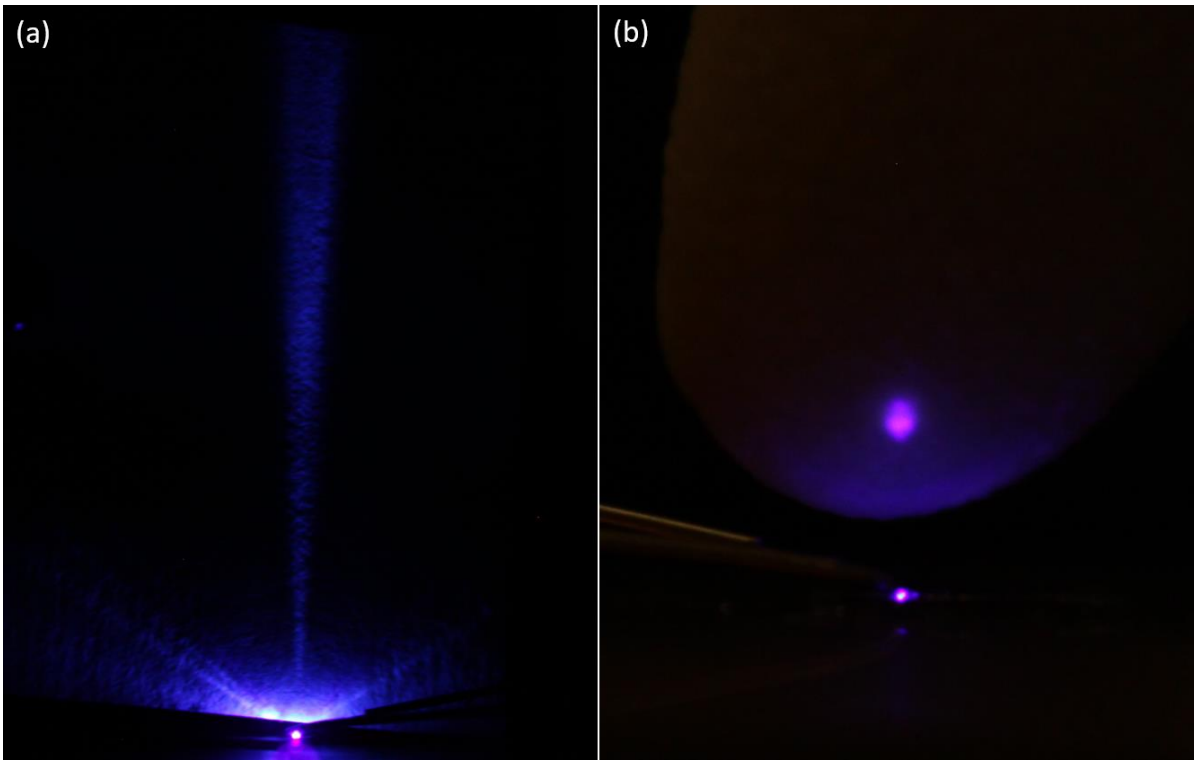


Figure 106. Photographs of a VCSEL during operation above threshold showing (a) the laser beam profile from a side-view and (b) the lasing spot illuminating a gloved finger.

The VCSELs had a low beam divergence angle, as shown by the vertical beam profile in Figure 106(a) that was photographed from a side-view (the beam is visible because a piece of paper was mounted vertically along the beam path), and Figure 106(b) shows the lasing spot illuminating a gloved finger.

Under pulsed operation (500 ns pulse width, 0.5% duty cycle), the highest peak output power was over 1 mW for a 10 μm aperture VCSEL, which had a threshold current of ~19 mA (24 kA/cm^2). This is approximately twice the peak output power compared to previous *m*-plane GaN TJ VCSELs,[58] and it was largely due to better mode alignment at higher current densities. Figure 107 shows the *L-I-V* characteristics under pulsed operation for 23λ VCSELs with various aperture diameters.

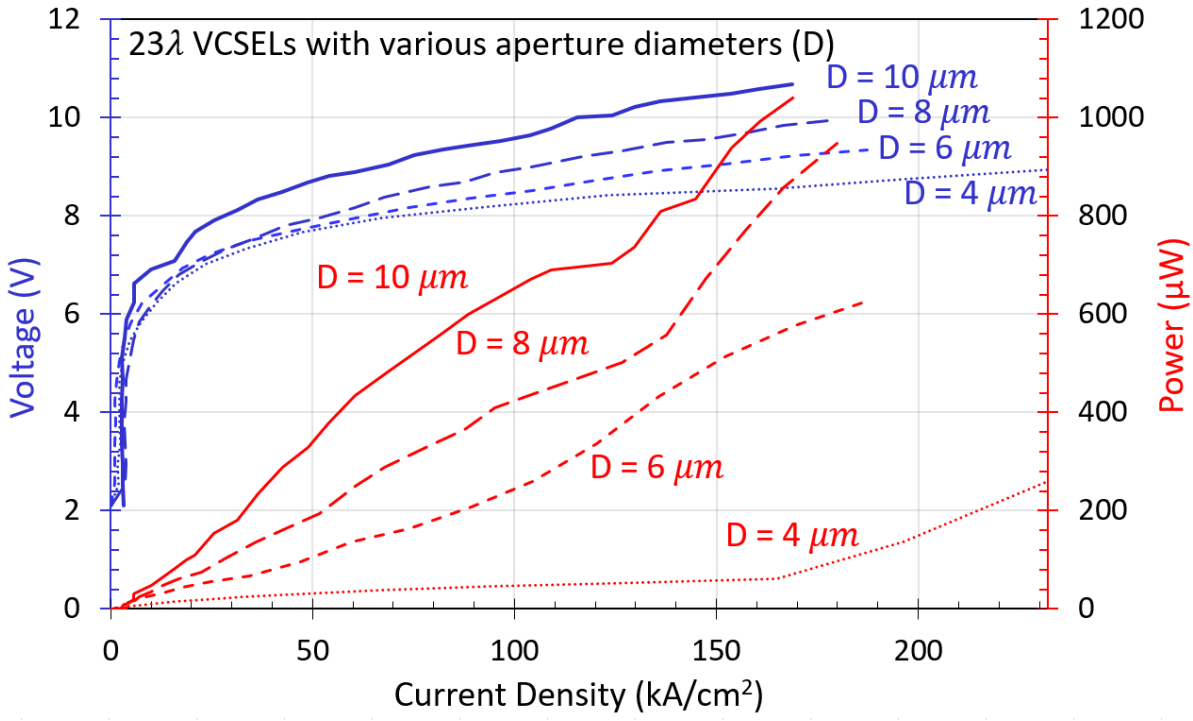


Figure 107. (a) Pulsed *L-I-V* characteristics of 23λ VCSELs with various aperture diameters and (b) pulsed emission spectrum of a 23λ VCSEL with a 6 μm aperture diameter.[73]

The threshold currents under pulsed operation for 4 μm, 6 μm, and 8 μm aperture diameter VCSELs were ~20 mA (160 kA/cm^2), ~12 mA (42 kA/cm^2), and ~12 mA (24 kA/cm^2), respectively. The lateral confinement factor is simulated to decrease with smaller VCSEL aperture diameters,[30] which could explain the higher threshold current density for 4 μm and 6 μm aperture diameters. As discussed in Section 4.5.4, only the 6 μm and 8 μm aperture diameter VCSELs achieved lasing under CW operation, which was likely due to their lower threshold current (12 mA) that enabled CW lasing at lower injection currents with less heating. Figure 108 shows the pulsed *L-I-V* characteristic for a 23λ VCSEL with a 6 μm aperture diameter.

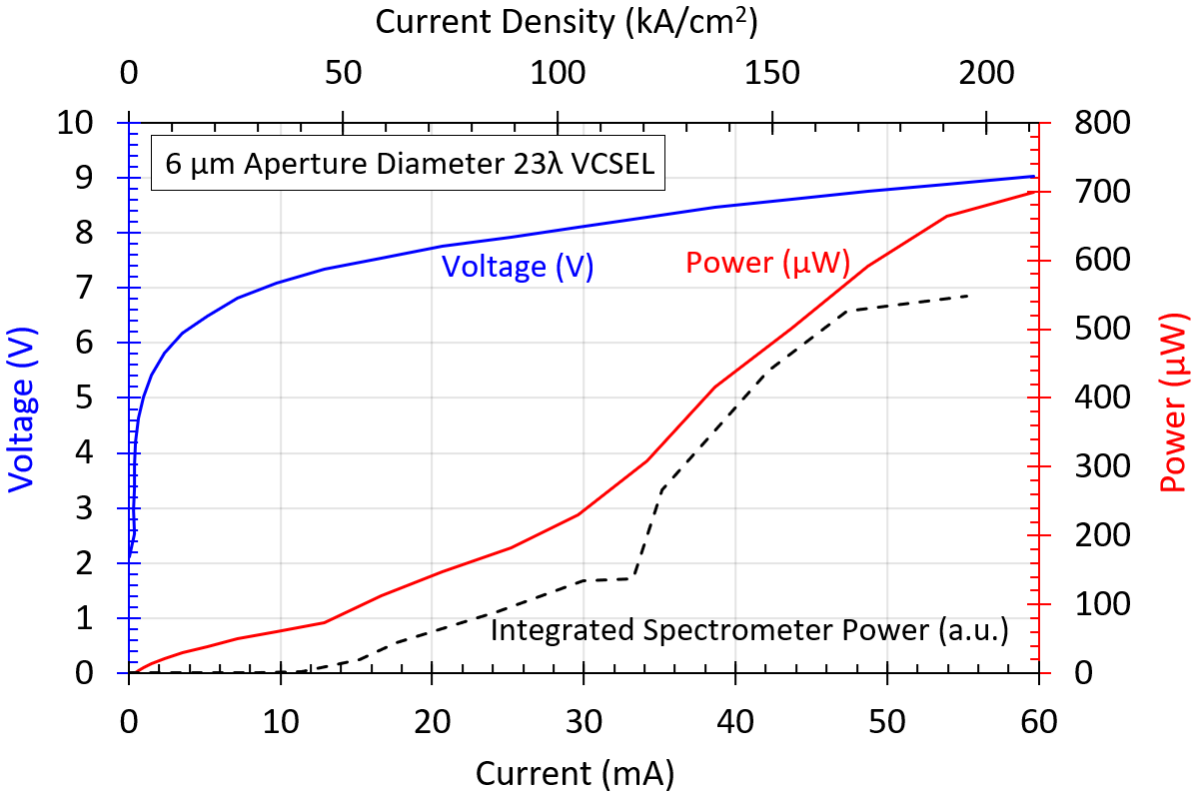


Figure 108. Pulsed *L-I-V* characteristic of a 23λ VCSEL with a 6 µm aperture diameter.

A large-area photodetector was used to measure the light output power, as shown by the red curve. The threshold current was ~11 mA (~38.9 kA/cm^2) and the peak output power was ~700 µW for the 6 µm aperture diameter VCSEL. The kink in the *L-I* curve at threshold was somewhat obscured by the spontaneous emission that was scattered from other areas of the device, as shown in Figure 109, which shows optical micrographs at various current injection levels for a 23λ VCSEL with a 6 µm aperture diameter.

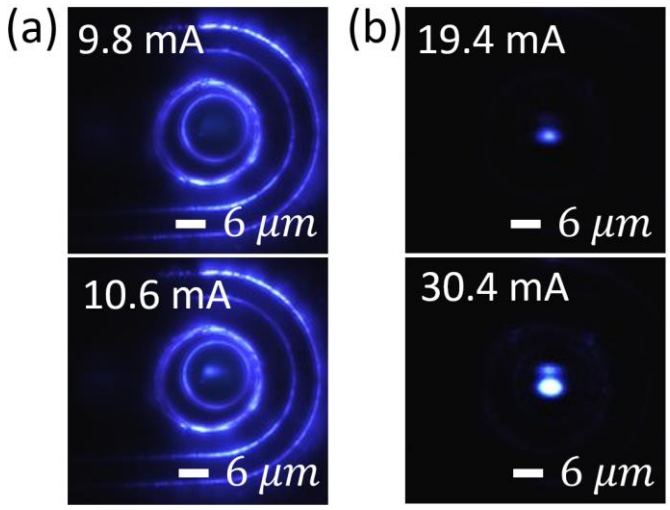


Figure 109. Optical micrographs at various current injection levels of a 23λ VCSEL with a 6 μm aperture diameter showing (a) photographs taken using a high exposure to view the spontaneous emission and (b) photographs taken using a low exposure to focus on the relatively intense lasing emission.

The top image in Figure 109(a) shows the spontaneous emission emitted from the device at a current of 9.8 mA, which is below the threshold for lasing. If this spontaneous emission was not collected by the photodetector, the *L-I* curve would have a much sharper kink at threshold, as shown by the dashed black *L-I* curve in Figure 108(a). The dashed black *L-I* curve shows a more well-defined kink at threshold because it was measured using a spectrometer optical fiber that was aligned with the lasing spot to minimize the amount of spontaneous emission that was collected. Note that the dashed black *L-I* curve shows the integrated emission spectrum intensity which has arbitrary units while the red *L-I* curve shows the light output power in μW because it was measured using a calibrated photodiode. As shown in the bottom image of Figure 109(a), the lasing spot begins to appear at 10.6 mA. As expected, the intensity of the lasing spot above threshold quickly surpassed the intensity of the spontaneous emission. This can be seen in the images shown in Figure 109(b) that were taken at a lower exposure to show the lasing mode, but the spontaneous emission was no longer visible due to its relatively weak intensity. Figure 110 shows the emission spectrum for a 23λ VCSEL with a 6 μm aperture diameter measured under pulsed operation.

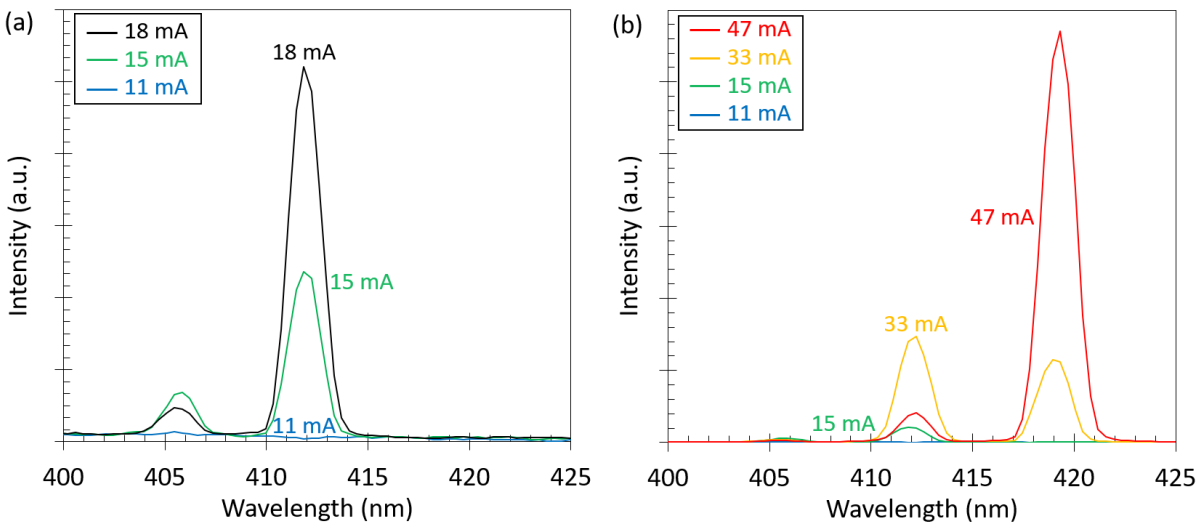


Figure 110. Pulsed emission spectrum for a 23λ VCSEL with a 6 μm aperture diameter for currents up to (a) 18 mA and (b) for higher currents up to 47 mA.

Compared to previous *m*-plane GaN 7λ VCSELs, the relatively long 23λ cavity length resulted in a reduced longitudinal mode spacing with lasing wavelengths at 406 nm, 412 nm, and 419 nm. This is similar to the predicted longitudinal mode spacing of ~6.6 nm using Equation (12) for an effective cavity length of ~3753 nm, wavelength of 405 nm, and assuming a group index of 3.3. With the peak spontaneous emission centered at ~403 nm, the initial lasing wavelengths appeared at 406 nm and 412 nm, as shown in Figure 110(a). While the effects of heating can usually be neglected during pulsed operation of edge-emitting lasers, there was a noticeable heating effect during pulsed operation of these VCSELs due to the relatively high current densities and high thermal impedance of the dual-dielectric DBR design. The peak gain redshifted at higher currents due to heating and caused longer wavelength lasing modes to increase in intensity at higher currents while shorter wavelength modes decreased in intensity. This can be seen in Figure 110(a) as the 412 nm mode increases in intensity from 15 mA (green curve) to 18 mA (black curve) while the 406 nm mode decreases in intensity. The peak gain continued to redshift at higher currents and a third longitudinal lasing mode appeared at a wavelength of 419 nm and current of 33 mA, as shown in Figure 110(b), which

shows the pulsed spectrum for a larger range of currents. As shown in Figure 110(b), the 419 nm lasing mode intensified at a faster rate and dominated in intensity compared to the shorter wavelength modes, which agreed with the increase in differential efficiency based on the *L-I* curve. The differential efficiency was 0.3% just above threshold and it increased to 0.8% above 30 mA, as shown by the slope of the *L-I* curve in Figure 108. The distinct increase in differential efficiency above 30 mA coincided with both the emergence of an additional lateral lasing mode in the aperture, as shown in the bottom image of Figure 109(b) and also with the appearance of the longer-wavelength 419 nm lasing mode shown in Figure 110(b). Several effects were considered quantitatively regarding the longer-wavelength 419 nm mode, which could explain a 75% improvement in the differential efficiency above 30 mA. Longer wavelengths have lower optical absorption, lower scattering loss, and decreased DBR reflectance for this design, which could each contribute to the observed increase in differential efficiency above 30 mA and dominance for longer-wavelength modes. The sub-band gap optical absorption for GaN decreases exponentially for longer wavelengths between 400-420 nm,[186] and for a similar Si doping concentration as in the n-GaN cavity, the absorption coefficient of n-GaN (carrier concentration of 3×10^{18} cm^{-3}) is reportedly ~20% lower at 419 nm compared to 405 nm,[187] which would correspond to a ~23% increase in differential efficiency based on TMM calculations. Longer wavelengths also have decreased scattering loss, which is inversely proportional to the square of the optical wavelength.[109–111] This results in ~9% lower scattering loss and ~7% higher differential efficiency at 419 nm, assuming a scattering loss of 30 cm^{-1} at 405 nm. Finally, based on TMM simulations, a ~33% improvement in differential efficiency at 419 nm is predicted due to the lower top-side DBR reflectance and higher mirror loss compared to the center of the DBR stopband at 405 nm.

These effects only predict a 75% increase in differential efficiency due to the longer wavelength mode, which does not fully explain the ~166% improvement in differential efficiency above 30 mA. One explanation could be a higher differential efficiency than previously calculated due to higher mirror loss because the 99% reflectance top-side DBR stopband (83 nm width) was blueshifted compared to the simulation, which would lead to higher mirror loss at 419 nm and higher η_d than previously calculated. Another possible explanation could be that the higher differential efficiency was related to the appearance of the additional lasing lobe within the aperture, but further analysis would be required to verify. The higher order lateral optical mode (i.e., two lasing lobes instead of a single fundamental lobe) likely appeared due to a thermal lens effect that increased the lateral optical confinement at higher currents. The increased lateral confinement from the thermal lens effect would also increase the normalized frequency and promote higher order lateral optical modes. Therefore, the increased lateral confinement factor could have also contributed to the higher differential efficiency above 30 mA, but further analysis would be required to quantify the extent of the increase.

The threshold current of ~11 mA (~38.9 kA/cm^2) for a 6 μm aperture diameter VCSEL was relatively high compared to the previous 12 μm aperture diameter *m*-plane TJ VCSEL with a threshold current of ~4 mA (~3.5 kA/cm^2).[58] Part of this could be explained because the 6 μm aperture diameter was much smaller, which leads to reduced lateral optical confinement.[30] In support of this, a larger 10 μm aperture diameter VCSEL measured here had a lower threshold current density of ~17.4 kA/cm^2, but this was still a relatively high threshold. Further investigation would be required, but another contribution to the high threshold could be due to the decreased confinement factor of the 23λ cavity length compared

to the 7λ cavity length in previous VCSELs. As seen in Equation (15), the fill factor is inversely proportional to the effective cavity length, so this would lead to a ~3× lower confinement factor and higher threshold for the 23λ VCSEL. Another possible explanation for the high threshold could be due to decreased valence subband separation because of the relatively thick QWs (14 nm QW thickness compared to 3 nm in the previous design). For example, nonpolar QW calculations have predicted optical gain deterioration for QW thicknesses above 5 nm due to thermal carrier redistribution between valence subbands.[188]

The scattering loss was found to be consistent between calculations from RMS roughness values and calculations from the experimentally measured differential efficiency and TMM simulations. The RMS roughness within the VCSEL apertures was ~2 nm on the p-side due to the MBE regrowth and less than 1 nm on the n-side after removing the residue that formed during PEC etching. This predicts a scattering loss of ~10-45 cm^{-1} for 2 nm RMS roughness prior to DBR deposition.[167] By expanding the threshold modal gain term in the denominator of Equation (11), the scattering loss can also be estimated based on the differential efficiency, as described by

$$\eta_{d1} = F_1 \eta_i \frac{\alpha_m}{\alpha_i + \alpha_m + \alpha_s} \tag{32}$$

where $\eta_{d1}$is the differential efficiency from one mirror, F_1 is the fraction of light that couples out of one mirror, η_i is the injection efficiency, α_i is the internal loss, α_m is the mirror loss, α_s is the scattering loss. Using the experimentally measured differential efficiency of 0.8% based on the slope of the *L-I* curve in Figure 108, assuming a 66% injection efficiency as reported for *m*-plane GaN violet edge-emitting lasers,[122] top/bottom mirror reflectance values of 99.965%/99.998% from TMM simulations, F_1 of ~0.946, mirror loss of ~0.49 cm^{-1}, and an internal loss of 11.24 cm^{-1} from TMM simulations, the calculated scattering loss is ~27 cm^{-1}.

This agrees favorably with the predicted scattering loss range of 10-45 cm^{-1} for 2 nm RMS roughness prior to DBR deposition.[167]

While previous *m*-plane GaN 7λ VCSELs suffered from filamentary lasing within the aperture (i.e., spatially nonuniform lasing spots appearing within the aperture),[58] lasing was observed to be centered within the aperture and appeared as the fundamental LP_{01} mode at currents below 30 mA, as shown in Figure 109. Above 30 mA, a 2nd lasing lobe appeared, suggesting the LP_{11} mode. This improved lasing behavior without filamentary lasing may have been related to the removal of the oxide residue that forms during PEC undercut etching to remove the growth substrate. Based on SEM and AFM images, the residue had a rough morphology that ranged between 3-12 nm RMS roughness, which could prevent lasing due to scattering loss or reduced DBR mirror reflectivity. For example, over 90 cm^{-1} of scattering loss is predicted for 6 nm RMS roughness prior to DBR deposition,[167] and the VCSELs with ~6 nm RMS roughness on the p-side were unable to lase, as described back in Section 4.4. While further experimentation would be required to verify, the nonuniformity of the residue could offer an explanation for filamentary lasing in previous *m*-plane VCSELs reported in Ref. 58 because lasing would likely occur preferentially in certain areas that have reduced roughness. An 11.7 M KOH solution was effective at removing most of the residue, which suggests that it is a form of gallium oxide. The remaining residue had a cubic structure which was likely a form of indium oxide. While KOH only partially removed the residue, the most effective method to remove the residue was to swab the sample in Tergitol detergent.

In typical edge-emitting lasers and VCSELs, heating usually increases the threshold current. For example, the threshold current is usually higher under CW operation compared to pulsed operation. Interestingly, the opposite trend was observed for these VCSELs. This is

because heating redshifted the gain spectrum to provide better mode alignment. The peak spontaneous emission was ~403 nm while the nearest Fabry-Perot resonance wavelengths were at 406 nm and 412 nm (the initial lasing wavelengths). The spontaneous emission and peak gain redshift at higher temperatures, which could lower the threshold current when the peak gain was better aligned with the resonance wavelengths. This phenomenon was demonstrated by measuring the spectrum of a 6 μm aperture diameter VCSEL at longer pulse widths to cause more heating, which reduced the threshold current for lasing. As shown in Figure 110(a), there were no lasing modes at a current of 11 mA for a 500 ns pulse width (0.5% duty cycle), but by increasing the pulse width to 1 μs (1% duty cycle), the threshold current decreased and lasing modes at 406 nm and 412 nm appeared at 11 mA, as shown in Figure 111.

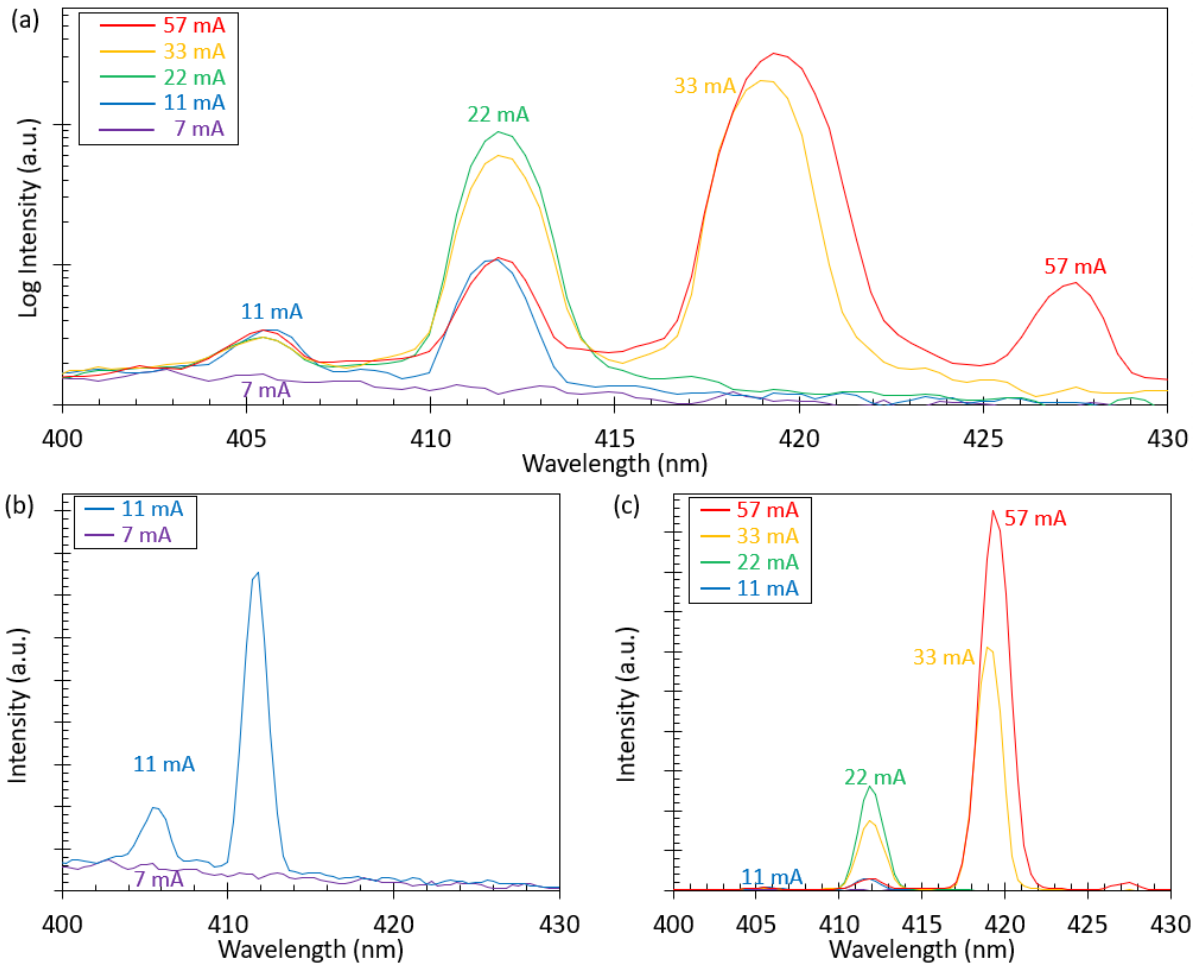


Figure 111. Pulsed emission spectrum at a longer pulse width of 1 μs (1% duty cycle) for a 23λ VCSEL with a 6 μm aperture diameter showing (a) logarithmic intensity scale showing all four lasing wavelengths at 406 nm, 412 nm, 419 nm, and 428 nm, (b) linear intensity scale showing the onset of lasing occurring at 11 mA, and (c) linear intensity scale to show the relative intensity of each mode for currents up to 57 mA.

By increasing the pulse width from 500 ns to 1 μs (1% duty cycle), Figure 111(a) shows the pulsed emission spectrum on a logarithmic intensity scale to show all four lasing wavelengths at 406 nm, 412 nm, 419 nm, and 428 nm. While the 428 nm lasing mode did not appear in the pulsed spectrum at a 0.5% duty cycle, it appeared at a 1% duty cycle due to the redshifted peak gain from heating. While lasing did not occur at 11 mA at a 0.5% duty cycle, Figure 111(b) shows the pulsed emission spectrum on a linear intensity scale at the onset of lasing at a current of 11 mA at a 1% duty cycle. Increasing the duty cycle from 0.5% to 1% decreased the threshold for lasing because the increased heating redshifted the peak gain to provide better

mode alignment for 406 nm and 412 nm resonance modes. This is the case because the peak spontaneous emission was ~403 nm, so redshifting the peak gain results in better mode alignment. Therefore, it can be ideal to design the peak gain at a shorter wavelength compared to the Fabry-Perot resonance modes to account for the redshift of the peak gain at higher temperatures. While this effect was observed by increasing the duty cycle from 0.5% to 1%, it has an even more significant effect under CW operation (i.e., 100% duty cycle). Lastly, Figure 111(c) shows the pulsed spectrum at 1% duty cycle on a linear intensity scale to show the relative intensity for each mode.

In the opposite situation with a smaller pulse width of 100 ns (0.1% duty cycle), the threshold increased, as shown in Figure 112.

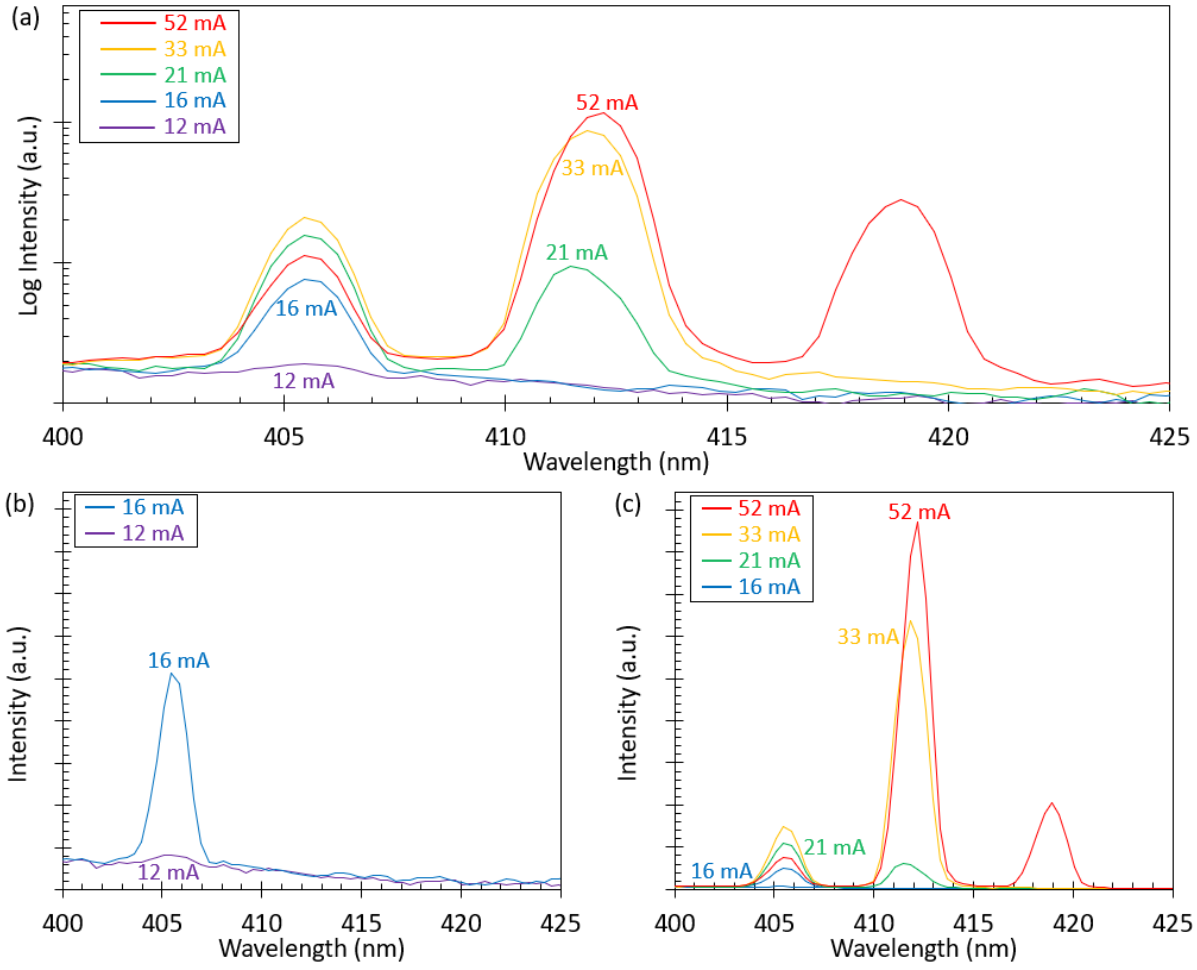


Figure 112. Pulsed emission spectrum at a shorter pulse width of 100 ns (0.1% duty cycle) for a 23λ VCSEL with a 6 μm aperture diameter showing (a) logarithmic intensity scale showing all three lasing wavelengths at 406 nm, 412 nm, and 419 nm, (b) linear intensity scale showing the onset of lasing occurring at a higher current of 11 mA at a wavelength of 406 nm, and (c) linear intensity scale to show the relative intensity of each mode for currents up to 52 mA.

By decreasing the pulse width to 100 ns (0.1% duty cycle), Figure 112(a) shows the pulsed emission spectrum on a logarithmic intensity scale to show all three lasing wavelengths at 406 nm, 412 nm, 419 nm. At a lower duty cycle of 0.1%, there was less heating, reduced peak gain redshifting, and the threshold increased. While the lasing modes initially appeared in the spectrum at 11 mA at 1% duty cycle and 15 mA at 0.5% duty cycle, Figure 112(b) shows the initial lasing mode appear at a higher current of 16 mA at 0.1% duty cycle due to the reduced heating effect. Furthermore, the reduced peak gain redshifting resulted in only the 406 nm lasing mode appearing initially, while 1% and 0.5% duty cycle measurements showed two lasing modes (406 nm and 412 nm) appear simultaneously at currents of 11 mA and 15 mA, respectively. At a 0.1% duty cycle, the 412 nm mode did not appear until a current of 20 mA as the reduced heating effect required higher currents to redshift the peak gain toward the 412 nm resonance mode. Lastly, Figure 112(c) shows the pulsed spectrum at 0.1% duty cycle on a linear intensity scale to show the relative intensity for each mode, which shows the 412 nm mode dominating due to the reduced gain redshifting while the 419 nm mode dominated for 0.5% and 1% duty cycle measurements.

By measuring the emission spectrum at various polarizer angles, the VCSELs were found to have polarized emission along the *a*-direction, as shown in Figure 113.

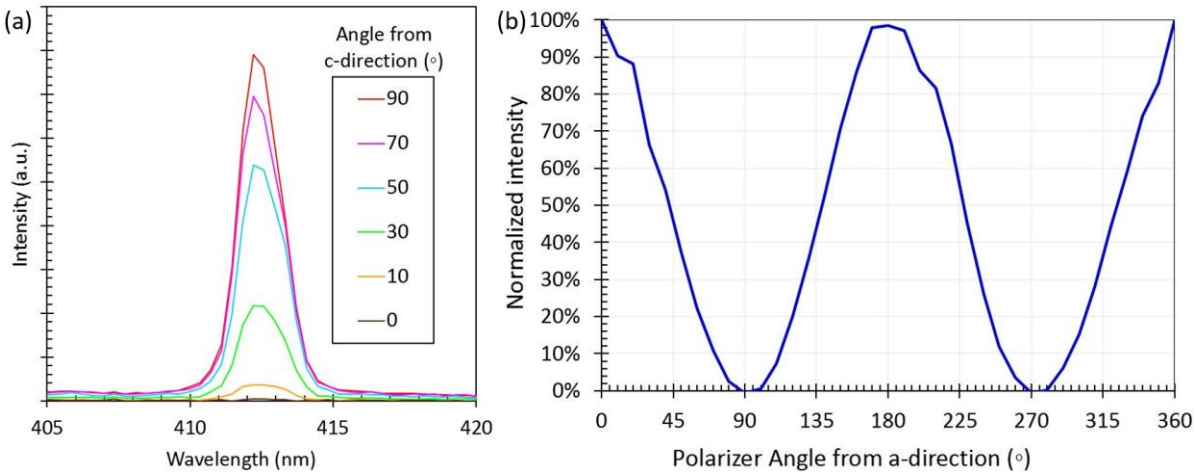


Figure 113. Emission spectrum of a 23λ VCSEL with a 6 μm aperture diameter measured at various polarizer angles. (b) Normalized emission intensity versus polarizer angle.

Figure 113(a) shows that the highest emission intensity occurred when the linear polarizer was oriented 90° from the *c*-direction, which corresponds to the *a*-direction. Figure 113(b) shows the normalized emission intensity as a function of polarizer angle, and the VCSELs were found to have a polarization ratio of 100%, which agrees with previous reports of polarized emission from *m*-plane GaN VCSELs.[3,4,29,30]

4.5.4. Lasing Characteristics Under CW Operation

Switching from Au-Au thermocompression flip-chip bonding to Au-In SLID bonding significantly improved the thermal performance and led to the first demonstration of CW operation for nonpolar GaN-based VCSELs. Increasing the cavity length from 7λ to 23λ also improved the thermal performance, but it was not the main improvement that led to CW operation as both 7λ and 23λ VCSELs were able to lase under CW operation. Searching for VCSELs that can lase under CW operation can be quickly done by using an optical microscope to view the lasing near-field pattern (e.g., lasing spot) within in the aperture. Because devices

can easily burn out under CW operation, a safer method to find CW-capable VCSELs was to test devices under pulsed operation and gradually increase the duty cycle. As another precaution, when increasing the duty cycle, the pulse generator voltage was decreased to the minimum value that lasing could be sustained (the threshold voltage decreased at higher duty cycles). For many devices, the lasing spot would disappear above ~80% duty cycle. If lasing could be sustained at the maximum duty cycle, it would be capable of lasing under CW operation, and further lasing characteristics could be measured (e.g., *L-I-V* and emission spectrum characteristics). Figure 114 shows the emission spectrum under CW operation for a 6 μm aperture diameter 7λ VCSEL with a 2×MQW active region (14 nm QWs and 1 nm GaN barriers).

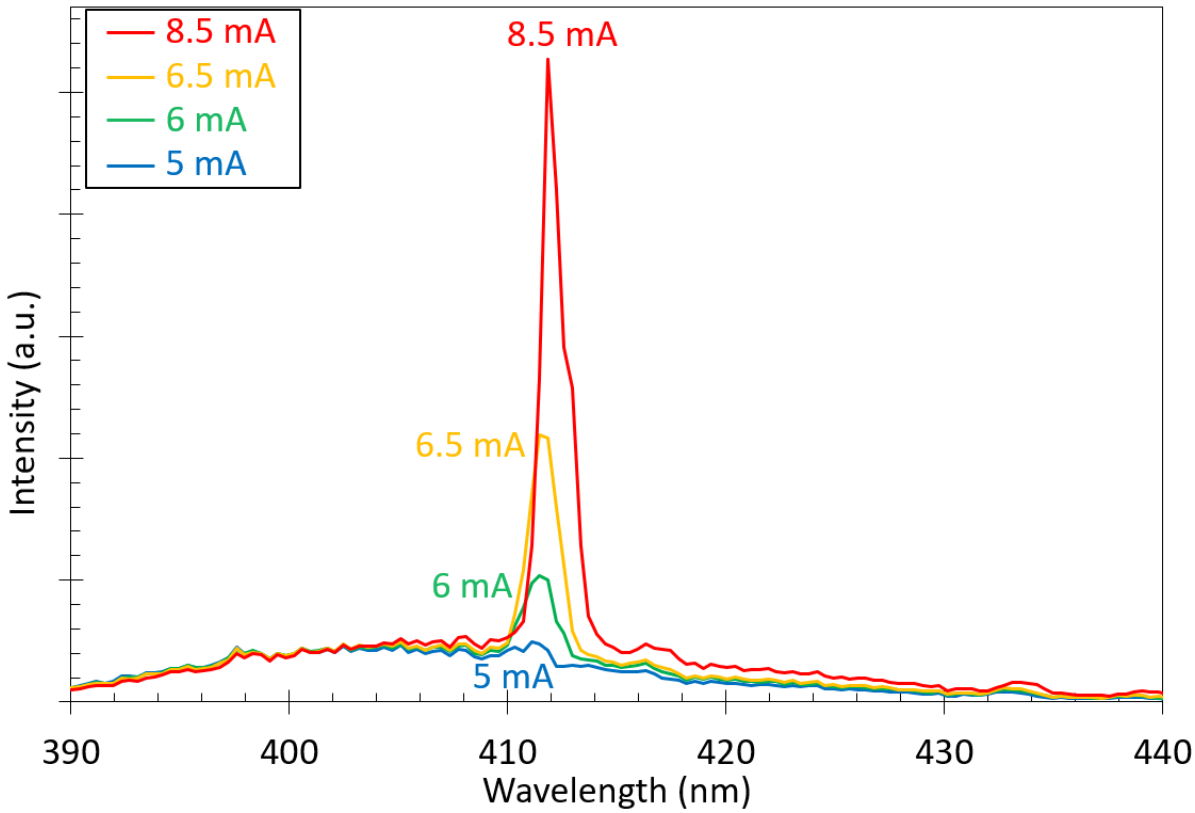


Figure 114. Emission spectrum under CW operation for a 7***λ*** VCSEL with a 6 ***μ***m aperture diameter. The threshold current was ~6 mA (~21.2 kA/cm^2) at a lasing wavelength of ~412 nm.

Based on the emission spectrum, the threshold current was ~6 mA (~21.2 kA/cm^2) at a lasing wavelength of ~412 nm. As the peak gain redshifted away from the Fabry-Perot resonance wavelength, the lasing mode disappeared at currents above ~9 mA, and the device failed above 12 mA. Nearly every device across the wafer was able to lase under pulsed operation, but only a couple of the 6 μm aperture diameter 7λ VCSELs were able to lase under CW operation. In comparison, the 23λ VCSEL sample had more devices capable of lasing under CW operation. This could have been due to the improved thermal performance of the longer cavity length design and possibly due to the Au-In SLID bond. FIB cross-sectioning of a 23λ VCSEL showed that the bottom DBR was fully embedded within Au-In bonding metal, which creates a thicker pathway for heat transport and improves the thermal performance. However, FIB cross-sectioning was not performed on 7λ VCSELs to see whether the bottom DBR was fully embedded within metal. Because there were not many 7λ VCSELs that could lase under CW operation, most of the CW lasing electrical characterization was conducted on 23λ VCSELs.

Stable CW lasing was sustained for over 20 minutes of testing for a 6 μm aperture 23λ VCSEL with emission polarized along the *a*-direction with a 100% polarization ratio, similar to previous pulsed *m*-plane VCSELs.[3] Only the 6 μm and 8 μm VCSELs were able to lase under CW operation, which was likely due to their lower threshold current (12 mA under pulsed operation) that enabled CW lasing at lower injection levels with less heating. Figure 115 shows the *L-I-V* characteristic under CW operation for a 6 μm aperture 23λ VCSEL.

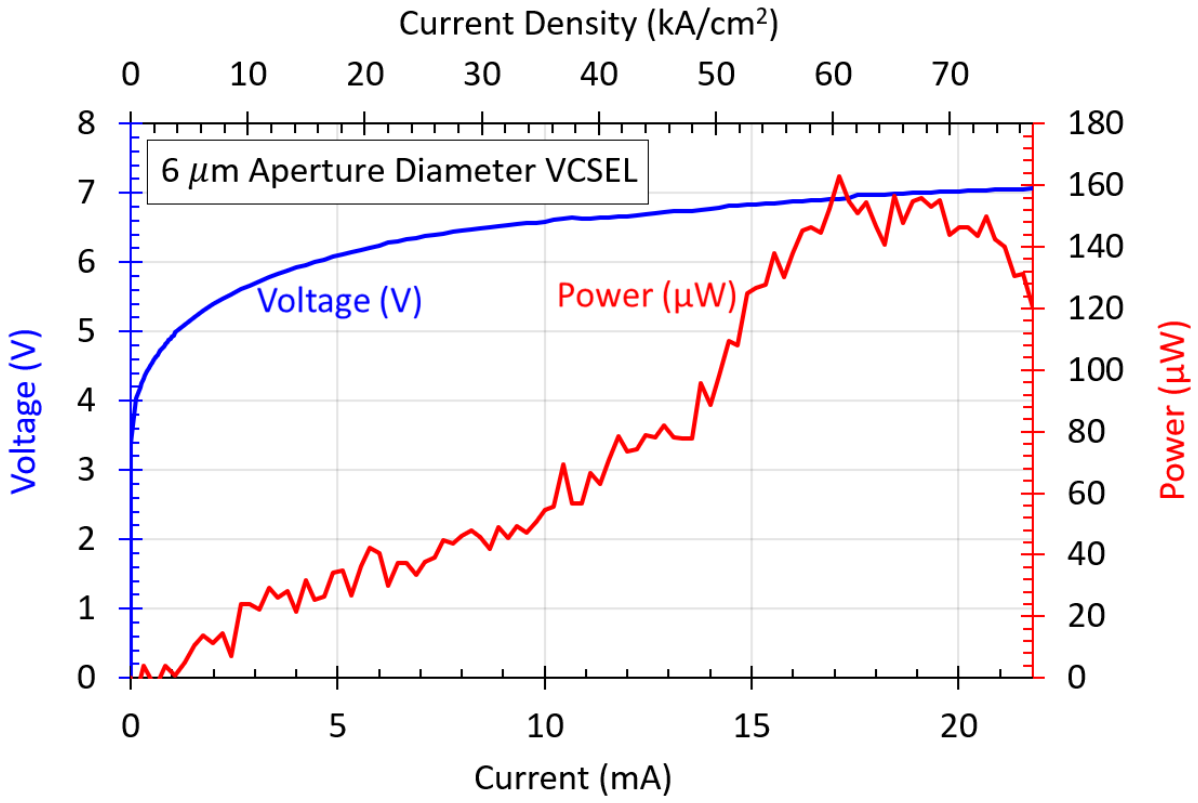


Figure 115. *L-I-V* characteristics under CW operation of a 23$\boldsymbol{\lambda}$ VCSEL with a 6 $\boldsymbol{\mu}$m aperture diameter. The peak output power under CW operation was ~150 μW with a threshold current ~10 mA (~35.4 kA/cm^2).

As discussed previously for the pulsed characteristics in Section 4.5.3, the threshold current decreased at longer pulse widths due to thermally-induced peak gain redshifting that created better mode alignment. Similarly, the threshold current decreased under CW operation. The threshold current was ~10 mA (~35.4 kA/cm^2) with a peak output power of ~150 μm before thermal rollover. The decreased confinement factor of the longer cavity length design may have contributed to the higher threshold compared to the 7λ VCSEL. The kink in the *L-I* curve at threshold was obscured by spontaneous emission collected by the large-area photodetector, as discussed earlier in Section 4.5.3. The roughness (noise) in the *L-I* curve was likely due to the faster integration time set for the Keithley 2400 SourceMeter compared to the pulsed measurement. Near the threshold current, the slope resistance corresponded to an effective contact resistivity ~$10^{-5}\ \Omega \cdot \text{cm}^2$. At a current density of 40 kA/cm^2, the voltage was 6.6 V,

which is 3 V lower than the previous TJ 7λ VCSEL and 1.4 V lower than the ITO VCSEL.[58] While further investigation is required, this improvement may be related to the improved MBE TJ regrowth or removal of PEC oxide residue prior to n-contact metal deposition. Figure 116 shows the emission spectrum under CW operation for a 6 μm aperture diameter 23λ VCSEL.

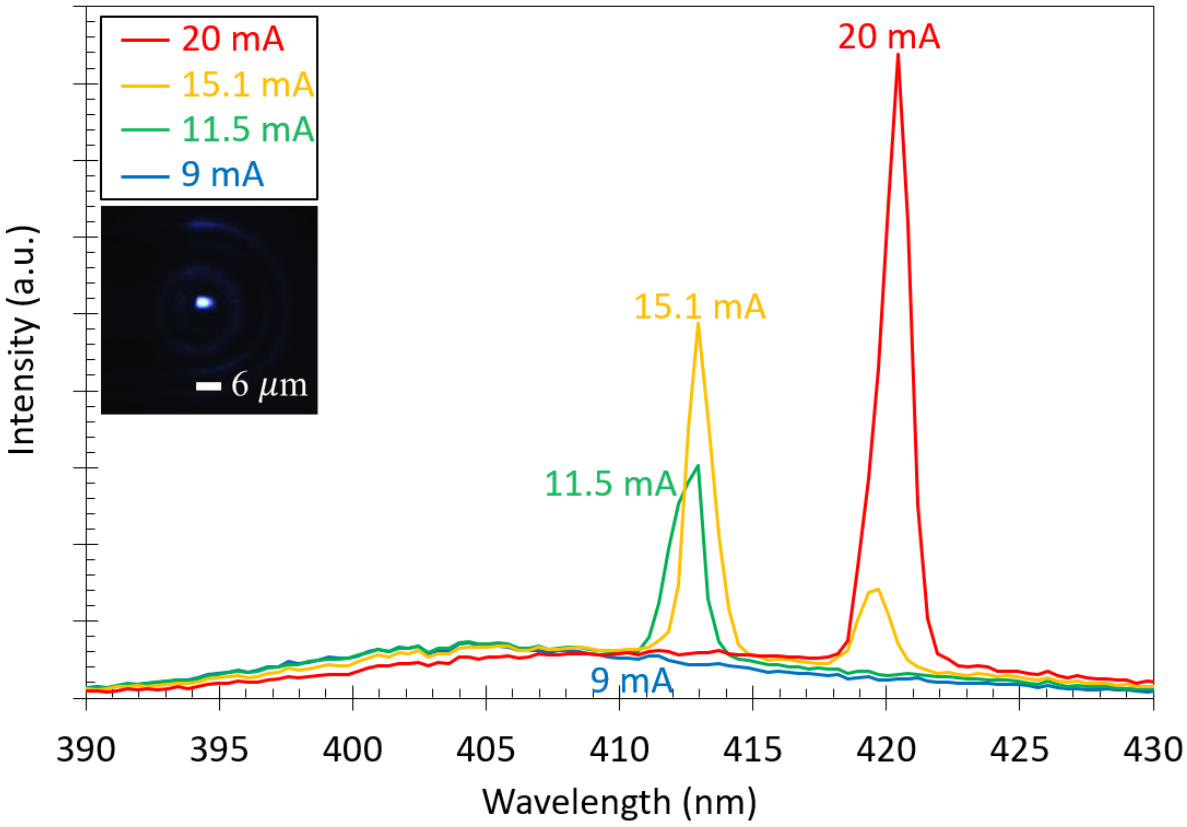


Figure 116. Emission spectrum under CW operation for a 23***λ*** VCSEL with a 6 ***μ***m aperture diameter. The inset shows an optical micrograph of lasing within the aperture during CW operation. Lasing was centered in the aperture, which suggests the fundamental lateral optical mode.

Lasing was centered in the aperture and appeared as the fundamental lateral mode, as shown in the inset in Figure 116. This differed from the filamentary lasing in previous *m*-plane VCSELs that had a stochastic distribution of lasing spots within the aperture.[58] Eliminating

filamentary lasing is still under investigation, but it may be related to the removal of a rough residue that forms after PEC etching to remove the *m*-plane GaN growth substrate.

Unlike the pulsed spectrum measurement, the 406 nm lasing mode did not appear under CW operation. This was likely due to the higher temperature under CW operation that caused the peak gain to redshift at a faster rate. While the 419 nm mode appeared at 33 mA under pulsed operation, a 420 nm mode appeared much earlier under CW operation at 15.1 mA, as shown in Figure 116(b). Due to peak gain redshifting at higher currents, longitudinal mode hopping was observed. At 15.1 mA, the 413 nm mode was at its highest intensity, but it rapidly diminished and disappeared at higher currents as the 420 nm mode intensified. The full width at half maximum (FWHM) was < 2 nm for each lasing mode and was limited by the resolution of the spectrometer.

4.5.5. VCSEL Operating Temperature

The VCSEL operating temperature was estimated by measuring the redshift in the spontaneous emission spectrum under CW operation and comparing it to the expected shift in emission wavelength with temperature, $d\lambda/dT$. The emission spectrum under pulsed operation was measured for an *m*-plane LED at stage temperatures up to 60 °C and resulted in a $d\lambda/dT$ of ~0.05 nm/°C. The emission spectrum of the 23λ VCSEL with a 6 μm aperture diameter was collected under pulsed and CW operation to measure the redshift in peak spontaneous emission, as shown in Figure 117.

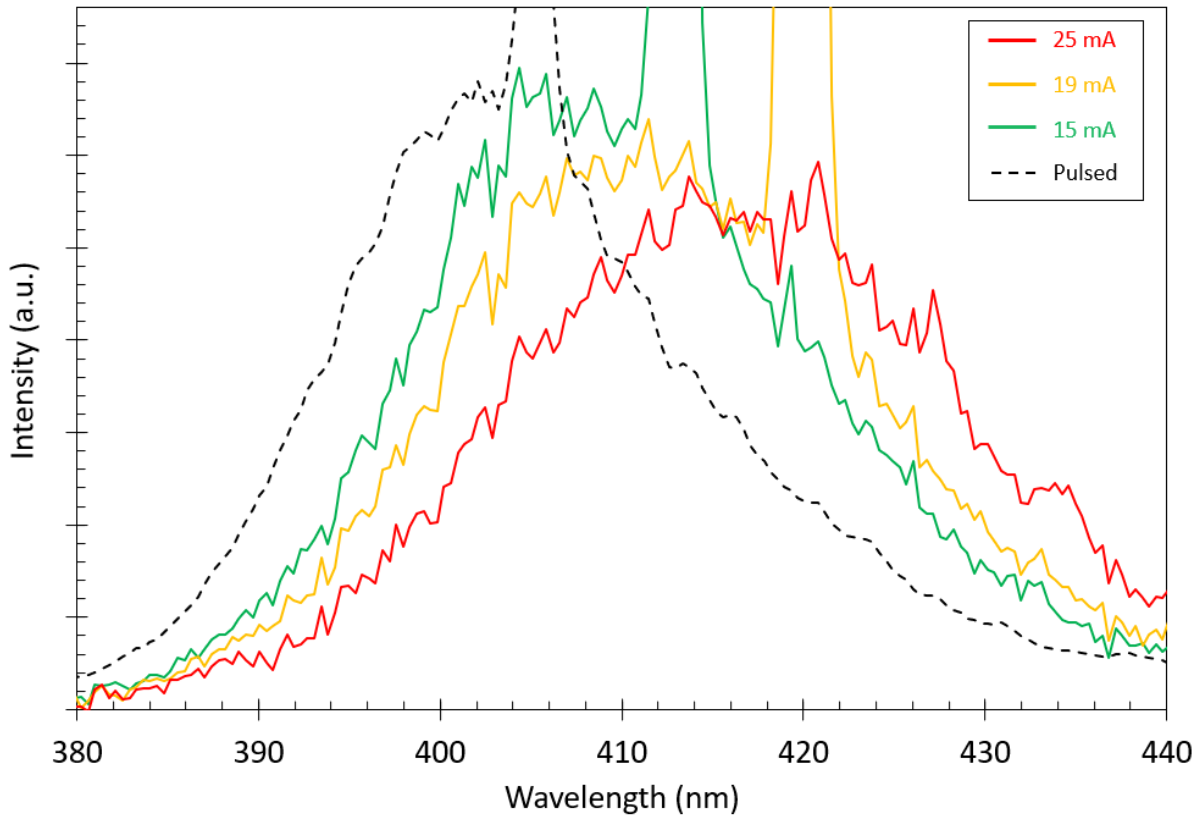


Figure 117. Emission spectrum of a 23λ VCSEL with a 6 μm aperture diameter showing the redshift in the peak spontaneous emission at higher current injection levels due to heating. The peak spontaneous emission was ~403 nm under pulsed operation (dashed black curve). Under CW operation, the peak spontaneous emission was ~410 nm at 15 mA, ~412 nm at 19 mA, and ~416 nm at 25 mA. Based on a $d\lambda/dT$ value of ~0.05 nm/°C measured for *m*-plane LEDs, the VCSEL operating temperature under CW operation can be estimated by using the redshift in spontaneous emission compared to pulsed operation. This led to an estimated thermal impedance of ~1400 °C/W with operating temperatures of ~163 °C at 15 mA, ~203 °C at 19 mA, and ~283 °C at 25 mA.

While previous spectra plots focused on the lasing wavelength peaks (406 nm, 412 nm, and 420 nm), this plot focuses on the redshift of the Gaussian-shaped spontaneous emission. The dashed black curve shows the emission spectrum under pulsed operation, showing the peak spontaneous emission centered at ~403 nm. The colored curves show that the spontaneous emission spectrum redshifts under CW operation and continues to redshift at higher currents due to heating. Under CW operation at 15 mA, the peak spontaneous emission was ~410 nm, so the spectra redshifted by ~7 nm compared to pulsed operation. Dividing the 7 nm redshift by the $d\lambda/dT$ value of 0.05 nm/°C gives an estimate for the increase in temperature compared to pulsed operation. Assuming the device was at room temperature (23°C) under pulsed

operation, this predicts a VCSEL operating temperature of ~163 °C at 15 mA (0.1 W input power) and a thermal impedance of ~1400 °C/W. At higher CW injection levels, the peak spontaneous emission redshifted to ~412 nm at 19 mA and ~416 nm at 25 mA. These correspond to VCSEL operating temperature of ~203 °C at 19 mA and ~283 °C at 25 mA. Lasing was observed at each of those injection levels except for the red curve at 25 mA. Although not shown in the figure, the VCSEL continued to lase up to a current of 20 mA with a peak spontaneous emission ~413 nm, which corresponds to a maximum predicted VCSEL operating temperature of ~223 °C. Although lasing stopped above 20 mA, higher injection levels were tested to measure the thermal stability. At 33 mA, the peak spontaneous emission was ~423 nm, which corresponds to a device operating temperature of ~423 °C. The VCSEL could lase if the current was reduced to 20 mA and lower, which showed that these devices could withstand high temperatures without failing. The highest injected current before failure was 37 mA, which had a peak spontaneous emission ~429 nm with an estimated operating temperature of 543 °C.

As expected, a shorter cavity length 7λ VCSEL showed poorer thermal performance than the 23λ VCSEL. Figure 118 shows the redshift in the peak spontaneous emission for a 7λ VCSEL with a 6 μm aperture diameter under CW operation.

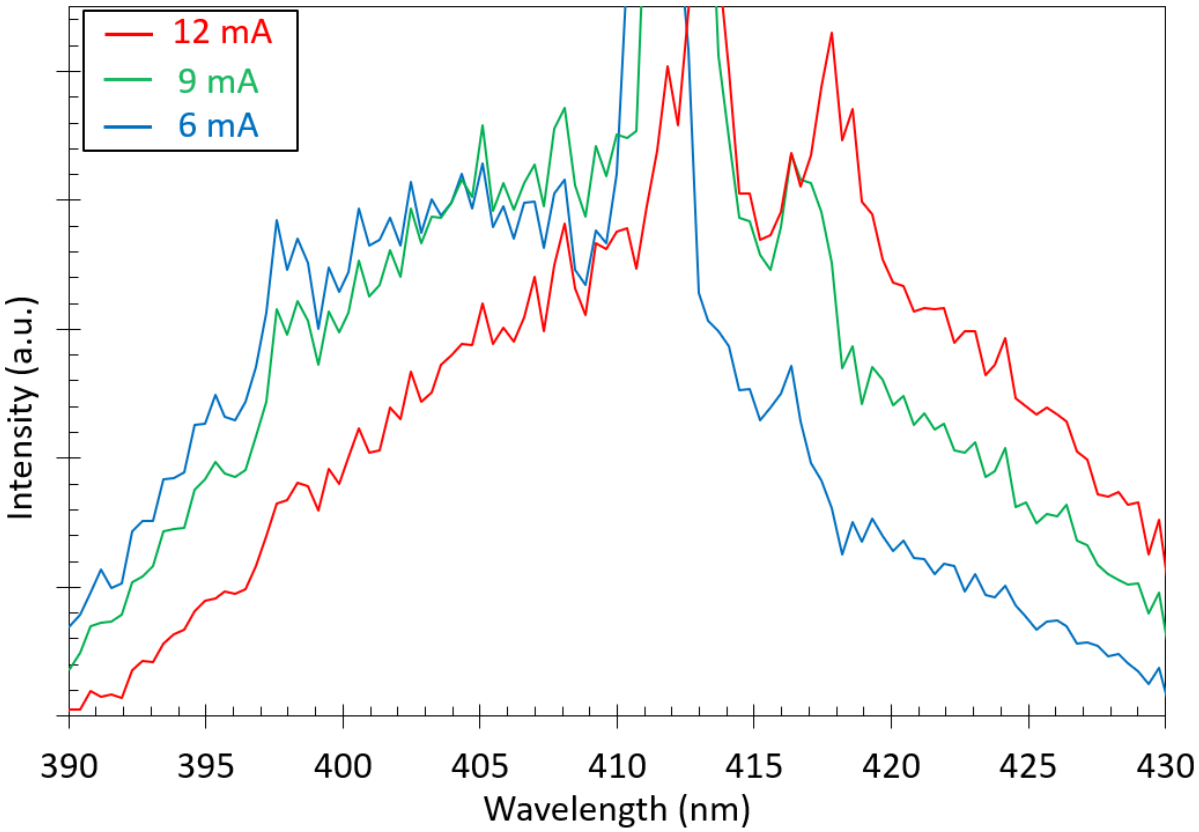


Figure 118. Emission spectrum under CW operation for a 7***λ*** VCSEL with a 6 ***μ***m aperture diameter showing the redshift in the peak spontaneous emission at higher current injection levels due to heating. The peak spontaneous emission was ~403 nm under pulsed operation and under CW operation, the peak spontaneous emission was ~406 nm at 6 mA, ~409 nm at 9 mA, and ~414 nm at 25 mA. Based on a dλ/dT value of ~0.05 nm/°C measured for *m*-plane LEDs, the VCSEL operating temperature under CW operation can be estimated by using the redshift in spontaneous emission compared to pulsed operation. This led to an estimated thermal impedance of ~2750 °C/W with operating temperatures of ~81 °C at 6 mA, ~141 °C at 9 mA, and ~243 °C at 12 mA.

With a peak spontaneous emission of ~403 nm under pulsed operation, the peak spontaneous emission redshifted to 414 nm at 25 mA, which predicts a thermal impedance of ~2750 °C/W and operating temperature of ~243 °C at 12 mA. While the 23λ VCSEL failed at currents above 37 mA, the 7λ VSCEL failed above 12 mA.

These predicted thermal impedance and operating temperature values were similar to thermal simulations performed using COMSOL, as shown in Figure 119.

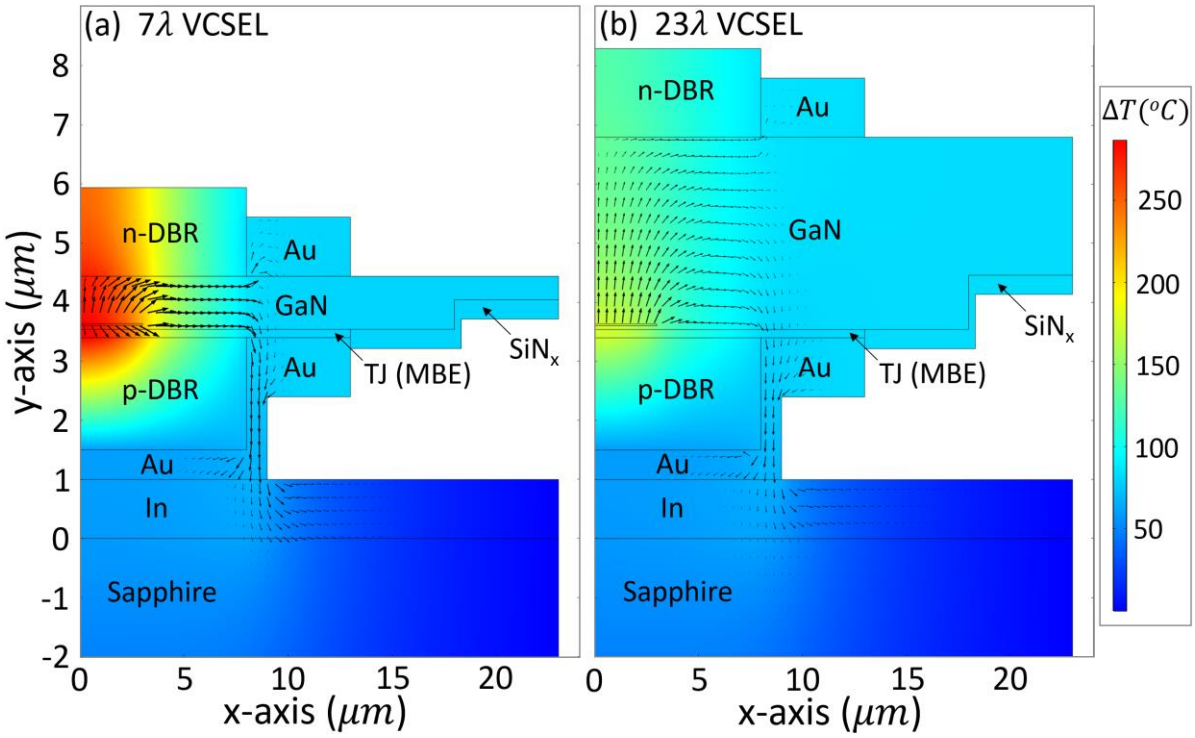


Figure 119. COMSOL thermal model of a 6 μm aperture diameter VCSEL with optical cavity lengths of (a) 7λ and (b) 23λ. The increase in temperature is shown by the color scheme and the thermal flux is shown by the overlain arrows. Due to the thermally-insulating bottom dielectric DBR, the main pathway for heat transport is through a thin Au contact (~1 μm thick) on the sidewall of the bottom DBR toward the flip-chip substrate. Reprinted from [Forman, C. A., Lee, S., Young, E. C., Kearns, J. A., Cohen, D. A., Leonard, J. T., Nakamura, S. (2018). Continuous-wave operation of m-plane GaN-based vertical-cavity surface-emitting lasers with a tunnel junction intracavity contact. Applied Physics Letters, 112(11), 111106. https://doi.org/10.1063/1.5007746] with the permission of AIP Publishing.[72]

COMSOL thermal simulations predicted a higher thermal impedance of 2470 °C/W for 7λ VCSELs, as shown in Figure 119(a), compared to a predicted thermal impedance of 1500 °C/W for longer cavity length 23λ VCSELs, as shown in Figure 119(b). The simulations shown in Figure 119 do not account for the case if the bottom DBR becomes completely embedded within Au-In bonding metal, as revealed by FIB cross-sectioning for a 23λ VCSEL, as shown in Figure 103. Figure 120 shows a COMSOL thermal simulation that accounts for this and includes a thicker metal pathway for heat transport around the bottom DBR (i.e., replacing 1-μm-thick Au with 5-μm-thick Au-In along the sidewall of the bottom DBR).

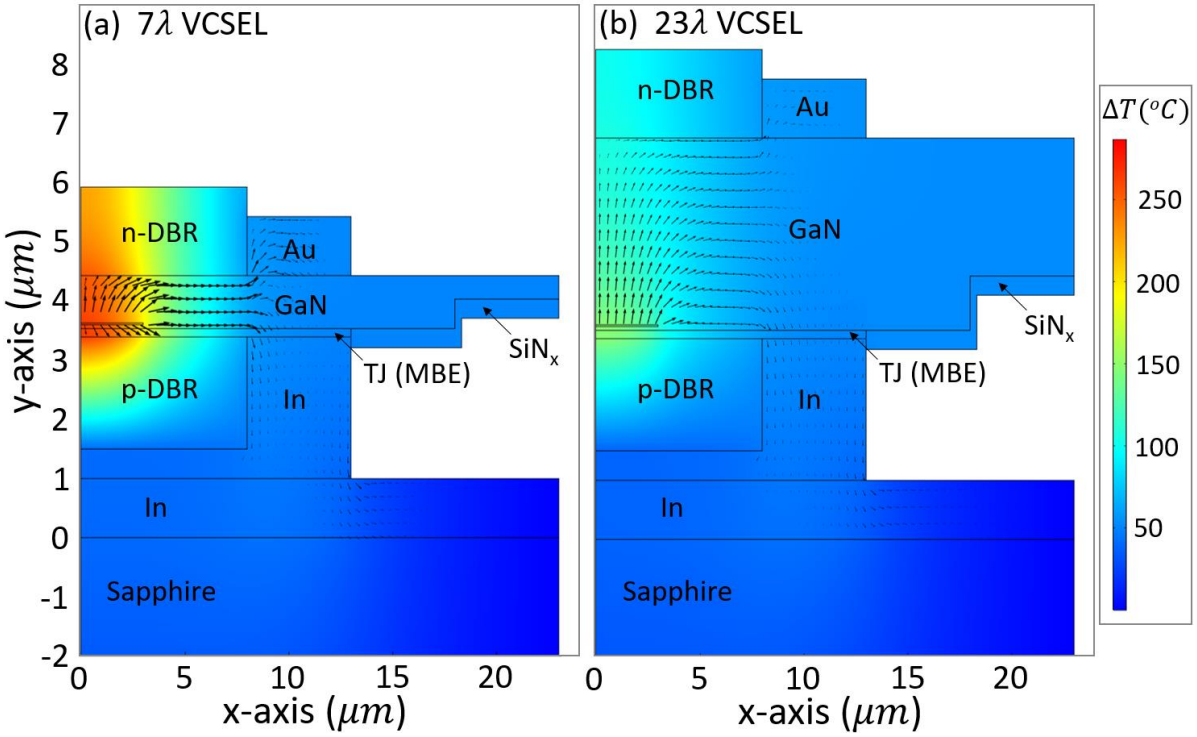


Figure 120. COMSOL thermal model of a 6 μm aperture diameter VCSEL with a 5-μm-thick Au-In pathway for heat transport around the bottom DBR for VCSELs with optical cavity lengths of (a) 7λ and (b) 23λ. The increase in temperature is shown by the color scheme and the thermal flux is shown by the overlain arrows.

Due to the thicker pathway for heat transport, the predicted thermal impedance values reduced to 2270 °C/W and 1270 °C/W for 7λ and 23λ VCSELs, respectively. Although similar, these values were smaller than the experimental thermal impedance estimated by the redshift of the spontaneous emission (i.e., 2750 °C/W and 1500 °C/W for 7λ and 23λ VCSELs, respectively). This could be due to several reasons as many simplifications were employed in the thermal model. The thermal conductivity of indium (82 W/mK) was assumed for Au-In alloys in the COMSOL simulation, but note that Au-In intermetallic layers have been reported to have relatively low thermal conductivity values (e.g., 11 W/mK for $AuIn_2$).[189] This could possibly account for the lower thermal impedance values predicted by COMSOL. The COMSOL prediction was closer to the experimentally-estimated thermal impedance values for the 23λ VCSEL compared to the 7λ VCSEL. This may have been due to structural

differences regarding the Au-In SLID bonding metal. The FIB cross-section shown in Figure 103 showed ~5-μm-thick Au-In bonding metal on the sidewall of the bottom DBR for a 23λ VCSEL device that was near the 23λ VCSEL that was tested under CW operation. However, a FIB cross-section was not performed for the 7λ VCSEL. Based on the relatively high experimentally-estimated thermal impedance compared to the COMSOL prediction, the 7λ VCSEL likely had a thinner metal pathway for heat transport along the sidewall of the bottom DBR.

The thermal performance can be easily improved in future devices by replacing the sapphire flip-chip substrate with a more thermally conductive material, such as copper or silicon carbide. By replacing sapphire with a silicon carbide substrate for the COMSOL thermal simulations shown in Figure 120, the thermal impedance decreases to 1960 °C/W and 960 °C/W for 7λ and 23λ VCSELs, respectively. Another improvement could be made by decreasing the diameter of the bottom DBR so that the metal pathway along the sidewall is closer to the aperture. For the 6 μm aperture diameter VCSELs, the bottom DBR had a diameter of 16 μm. By decreasing the bottom DBR diameter to 10 μm in the COMSOL thermal model, the predicted thermal impedance decreases to 1650 °C/W and 909 °C/W for 7λ and 23λ VCSELs, respectively. However, decreasing the bottom DBR diameter would decrease the alignment tolerance during VCSEL fabrication, which would likely require switching to using a stepper instead of a contact aligner for exposure during photolithography.

5. Conclusions and Future Work

In summary, we have demonstrated the first nonpolar GaN VCSEL that lases under CW operation. This accomplishment was largely due to the design improvements that were implemented after performing failure analysis on a 23λ VCSEL design that had a relatively thick 1642 nm MBE TJ regrowth. While the goal was to improve current spreading on the p-side with a thicker MBE regrowth, it led to a rough morphology (~6 nm RMS roughness) that prevented lasing due to scattering loss and reduced DBR mirror reflectivity. Furthermore, the n-side surface had an RMS roughness of up to 12 nm after PEC undercut etching of the sacrificial MQW for *m*-plane GaN substrate removal. This led to a series of MBE and PEC etching experiments with the goal of producing subnanometer RMS roughness on the surfaces prior to DBR mirror deposition. The p-side morphology was improved in the recent design by reducing the MBE regrowth thickness to 141 nm and by utilizing an In surfactant during MBE growth to smoothen the surface. The n-side roughness turned out to be a rough residue that formed after PEC undercut etching and likely consisted of Ga_2O_3 and In_2O_3. The most effective method of residue removal was swabbing the samples in Tergitol detergent, and this led to a smooth surface with subnanometer RMS roughness.

After solving the roughness problems that prevented lasing, there were two main challenges remaining: there was particularly low VCSEL yield after flip-chip bonding, and devices had poor thermal performance that prevented CW operation. The low yield consisted of a small percentage of devices that transferred to the flip-chip substrate, and the majority of those transferred devices were cracked due to the Au-Au flip-chip bond. Thermal modeling and FIB cross-section SEM imaging gave insight into the poor thermal performance of

previous nonpolar VCSELs. With downward heat flow inhibited by the thermally-insulating bottom dielectric DBR, the main path for heat flow was bottlenecked to a thin metal contact that conformed around the bottom DBR. Au-Au flip-chip bonding caused cracks in that metal contact, which further impaired the thermal performance. These problems were solved in the recent VCSEL design by using Au-In SLID bonding, which can be performed at a lower temperature and bonding force than Au-Au thermocompression bonding. By utilizing In-rich alloys, a liquid phase emerges above ~156 °C to soften the bonding process, and this led to significantly improved VCSEL yield. The liquid phase during bonding was also used to embed the bottom dielectric DBR within bonding metal. This significantly improved the thermal performance as it produced a much thicker and more robust metal pathway for heat flow around the bottom DBR. This led to stable CW lasing for over 20 minutes of continuous testing for a 23λ VCSEL with a 6 μm diameter ion implanted aperture with a TJ intracavity contact. With a threshold current of ~19 mA (24 kA/cm^2), the highest pulsed peak output power was over 1 mW for a 10 μm aperture diameter VCSEL. The peak output power for a 6 μm aperture VCSEL under CW and pulsed operation were 150 μW and 700 μW, respectively. Filamentary lasing was not observed, and lasing was centered within the aperture. By measuring the redshift in spontaneous emission under CW operation, the VCSEL operating temperature was estimated to be ~163 °C at 15 mA (0.1 W input power) with a thermal impedance of ~1400 °C/W for a 6 μm aperture 23λ VCSEL. CW operation was also achieved for 7λ VCSELs, but those had a higher estimated thermal impedance ~2750 °C/W due to the shorter cavity length and possibly due to structural differences regarding the Au-In bonding metal.

Achieving CW operation is an exciting milestone for nonpolar GaN VCSELs and opens the door to several exciting future directions. Many applications depend on lasers that produce a constant output power over time (i.e., CW operation). For example, CW operation is necessary for direct modulation of VCSELs for high-speed data communication. While 5 GHz of bandwidth has been achieved for violet GaN edge-emitting laser diodes,[51] GaN VCSELs have even greater potential for high modulation bandwidths due to their relatively small active region volume.[100] The next step is to measure the modulation bandwidth of CW nonpolar GaN-based VCSELs, but note that it could be difficult as the bandwidth may be limited by the response of the photodetector. It would also be useful to continue characterization to compare the lasing behavior of the devices with various aperture diameters and cavity lengths, with measurements such as: *L-I-V* and spectral emission characteristics, optical microscopy of lateral optical modes versus current injection level, emission spectrum characterization with a high-resolution spectrometer to measure the FWHM and wavelengths of various LP modes, divergence angle measurement, and reliability testing. After identifying key problems that can occur during fabrication and improving the VCSEL yield, conducting future studies on nonpolar GaN VCSELs will hopefully be more straightforward and lead to relatively rapid advancements in performance. There are several promising avenues for future research. The maximum CW output power was limited by the high operating temperature at high injection levels, so higher power could be obtained by improving the thermal performance or by reducing the threshold to enable CW lasing at lower injection levels. The simplest way to improve thermal performance in the current design is to replace sapphire with a more thermally conductive flip-chip substrate, such as copper or silicon carbide. While increasing the cavity length from 7λ to 23λ improved the thermal performance, there appeared

to be a tradeoff in terms of threshold current. This tradeoff could be studied in future research to find the optimal cavity length to maximize the CW output power. Note that the cavity length is inversely proportional to the longitudinal mode spacing, so mode alignment with the peak gain can be more difficult for shorter cavity length designs. Performance improvements could also be made by optimizing the QW thickness, GaN barrier thickness, number of QWs, and p-AlGaN EBL thickness and composition. After demonstrating GaN-based VCSELs with MOCVD-grown TJ intracavity contacts,[117] there are several future directions, such as optimizing MOCVD TJ growths and comparing to VCSELs with MBE-regrown TJ contacts. Currently, MBE TJ contacts have produced lower operating voltages while MOCVD-regrown TJ contacts have the advantage of smoother surface morphologies to reduce VCSEL scattering loss. Another promising design is to use semipolar GaN substrates for MOCVD growth, such as semipolar $(20\bar{2}\bar{1})$ or semipolar $(20\bar{2}1)$. While *m*-plane GaN VCSELs are limited to violet emission, semipolar GaN orientations enable longer emission wavelengths from blue to green. Furthermore, MBE TJ regrowth on semipolar $(20\bar{2}\bar{1})$ GaN produced much smoother morphologies compared to *m*-plane GaN. One of the most promising aperture designs is the BTJ aperture VCSEL, as described in Section 4.3.1, which could be created using MBE or MOCVD. Increased lateral optical confinement could be achieved in the BTJ aperture design by growing n-AlGaN for the current spreading layer to provide lateral index contrast with GaN within the aperture. Several other design improvements could be made, such as optimizing the gain offset parameter for CW operation or utilizing a modulated doping profile to reduce internal loss.

This is an exciting time for VCSEL technology as major companies (e.g., Apple Inc.) are investing into VCSEL development, but still, only infrared- and red-emitting VCSELs are

available in today's market. With substantial performance improvements over the past decade, GaN-based VCSELs are on the brink of commercialization to bridge the gap to shorter wavelength emission. Nonpolar *m*-plane GaN VCSELs are particularly promising due to their unique advantages, such as a 100% polarization ratio for VCSELs and VCSEL arrays. With CW operation finally achieved and significant improvements in yield, nonpolar GaN VCSELs have a bright future in next-generation display, illumination, communication, and sensing technology.

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References

[1] Michalzik, R., [VCSELs: Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers, 1st ed.], Springer, Heidelberg (2013).

[2] "Apple awards Finisar $390 million from its Advanced Manufacturing Fund - Apple.", <https://www.apple.com/newsroom/2017/12/apple-awards-finisar-390-million-from-its-advanced-manufacturing-fund/> (20 April 2018).

[3] Leonard, J. T., Cohen, D. A., Yonkee, B. P., Farrell, R. M., Margalith, T., Lee, S., DenBaars, S. P., Speck, J. S. and Nakamura, S., "Nonpolar III-nitride vertical-cavity surface-emitting lasers incorporating an ion implanted aperture," Appl. Phys. Lett. **107**(1), 11102 (2015).

[4] Holder, C. O., Leonard, J. T., Farrell, R. M., Cohen, D. A., Yonkee, B., Speck, J. S., DenBaars, S. P., Nakamura, S. and Feezell, D. F., "Nonpolar III-nitride vertical-cavity surface emitting lasers with a polarization ratio of 100% fabricated using photoelectrochemical etching," Appl. Phys. Lett. **105**(3), 31111 (2014).

[5] Nakamura, S., "Background story of the invention of efficient blue InGaN light emitting diodes (Nobel Lecture)," Ann. Phys. **527**(5–6), 335–349 (2015).

[6] "Energy savings forecast of solid-state lighting in general illumination applications.", (2014).

[7] Becerra, D. L., Kuritzky, L. Y., Nedy, J., Saud Abbas, A., Pourhashemi, A., Farrell, R. M., Cohen, D. A., DenBaars, S. P., Speck, J. S. and Nakamura, S., "Measurement and analysis of internal loss and injection efficiency for continuous-wave blue semipolar ($20\bar{2}\bar{1}$) III-nitride laser diodes with chemically assisted ion beam etched facets," Appl. Phys. Lett. **108**(9), 091106 (2016).

[8] Bridger, G., "BMW WORKING TO BRING LASER LIGHTS TO THE US," BimmerFile, 2015.

[9] Nakamura, S., Senoh, M., Nagahama, S. ichi, Iwasa, N., Yamada, T., Matsushita, T., Kiyoku, H. and Sugimoto, Y., "InGaN-based multi-quantum-well-structure laser diodes," Japanese J. Appl. Physics, Part 2 Lett. **35**(1 B), L74–L76 (1996).

[10] Zhu, D. and Humphreys, C. J., "Solid-State Lighting Based on Light Emitting Diode Technology BT - Optics in Our Time," M. D. Al-Amri, M. El-Gomati, and M. S. Zubairy, Eds., Springer International Publishing, Cham, 87–118 (2016).

[11] Armstrong, A. M., Kelchner, K., Nakamura, S., DenBaars, S. P. and Speck, J. S., "Influence of growth temperature and temperature ramps on deep level defect incorporation in m-plane GaN," Appl. Phys. Lett. **103**(23), 232108 (2013).

[12] Bernardini, F. and Fiorentini, V., "Spontaneous versus Piezoelectric Polarization in III-V Nitrides: Conceptual Aspects and Practical Consequences," Phys. Status Solidi **216**(1), 391–398 (1999).

[13] Seong, T.-Y., Han, J., Amano, H., Morkoc, H., Keraly, C. L., Kuritzky, L., Cochet, M., Weisbuch, C., Seong, T.-Y., Han, J., Amano, H., Morkoc, H., Keraly, C. L., Kuritzky, L., Cochet, M. and Weisbuch, C., [III-Nitride Based Light Emitting Diodes and Applications], Springer Singapore, Singapore (2013).

[14] Fabio, B., "Spontaneous and Piezoelectric Polarization: Basic Theory vs. Practical Recipes," [Nitride Semiconductor Devices: Principles and Simulation], Wiley-Blackwell, 49–68 (2007).

[15] Gil, B., [III-Nitride Semiconductors and their Modern Devices], OUP Oxford (2013).

[16] Feezell, D. F., Speck, J. S., DenBaars, S. P. and Nakamura, S., "Semipolar (2021) InGaN/GaN light-emitting diodes for high-efficiency solid-state lighting," IEEE/OSA J. Disp. Technol. **9**(4), 190–198 (2013).

[17] Coldren, L. A., Corzine, S. W. and Mašanović, M. L., [Diode Lasers and Photonic Integrated Circuits], John Wiley & Sons, Inc., Hoboken, NJ, USA (2012).

[18] David, A. and Grundmann, M. J., "Influence of polarization fields on carrier lifetime and recombination rates in InGaN-based light-emitting diodes," Appl. Phys. Lett. **97**(3), 33501 (2010).

[19] Kioupakis, E., Yan, Q. and Van de Walle, C. G., "Interplay of polarization fields and Auger recombination in the efficiency droop of nitride light-emitting diodes," Appl. Phys. Lett. **101**(23), 231107 (2012).

[20] Feezell, D. F., Schmidt, M. C., Farrell, R. M., Kim, K. C., Saito, M., Fujito, K., Cohen, D. A., Speck, J. S., DenBaars, S. P. and Nakamura, S., "AlGaN-cladding-free nonpolar InGaN/GaN laser diodes," Japanese J. Appl. Physics, Part 2 Lett. **46**(12–16), L284–L286 (2007).

[21] Park, S.-H., "Crystal Orientation Effects on Many-Body Optical Gain of Wurtzite InGaN/GaN Quantum Well Lasers," Jpn. J. Appl. Phys. **42**(Part 2, No. 2B), L170–L172 (2003).

[22] Park, S.-H., Ahn, D. and Chuang, S.-L., "Electronic and Optical Properties of a - and m -Plane Wurtzite InGaN-GaN Quantum Wells," IEEE J. Quantum Electron. **43**(12), 1175–1182 (2007).

[23] Scheibenzuber, W., Schwarz, U., Veprek, R., Witzigmann, B. and Hangleiter, A., "Calculation of optical eigenmodes and gain in semipolar and nonpolar InGaN/GaN laser diodes," Phys. Rev. B **80**(11), 115320 (2009).

[24] Li, Z. Q., Li, Z. M. S. and Piprek, J., "Simulations of laser diodes with nonpolar InGaN multi-quantum-wells," Phys. Status Solidi **7**(7–8), 2259–2261 (2010).

[25] Scheibenzuber, W. G. and Schwarz, U. T., "Polarization switching of the optical gain in semipolar InGaN quantum wells," Phys. Status Solidi **248**(3), 647–651 (2011).

[26] Schade, L., Schwarz, U. T., Wernicke, T., Weyers, M. and Kneissl, M., "Impact of band structure and transition matrix elements on polarization properties of the photoluminescence of semipolar and nonpolar InGaN quantum wells," Phys. Status Solidi Basic Res. **248**(3), 638–646 (2011).

[27] Melo, T., Hu, Y.-L., Weisbuch, C., Schmidt, M. C., David, A., Ellis, B., Poblenz, C., Lin, Y.-D., Krames, M. R. and Raring, J. W., "Gain comparison in polar and nonpolar/semipolar gallium-nitride-based laser diodes," Semicond. Sci. Technol. **27**(2), 024015 (2012).

[28] Kneissl, M., Rass, J., Schade, L. and Schwarz, U. T., "Growth and Optical Properties of GaN-Based Non- and Semipolar LEDs BT - III-Nitride Based Light Emitting Diodes and Applications," T.-Y. Seong, J. Han, H. Amano, and H. Morkoc, Eds., Springer Netherlands, Dordrecht, 83–119 (2013).

[29] Holder, C., Speck, J. S., DenBaars, S. P., Nakamura, S., Feezell, D., Speck, J. S., DenBaars, S. P. and Nakamura, S., "Demonstration of nonpolar GaN-based vertical-cavity surface-emitting lasers," Appl. Phys. Express **5**(9), K. D. Choquette and J. K. Guenter, Eds., 863906, IOP Publishing (2012).

[30] Leonard, J. T., Young, E. C., Yonkee, B. P., Cohen, D. A., Shen, C., Margalith, T., Ng, T. K., DenBaars, S. P., Ooi, B. S., Speck, J. S. and Nakamura, S., "Comparison of nonpolar III-nitride vertical-cavity surface-emitting lasers with tunnel junction and ITO intracavity contacts," Proc. SPIE **9748**, J.-I. Chyi, H. Fujioka, H. Morkoç, Y. Nanishi, U. T. Schwarz, and J.-I. Shim, Eds., 97481B–9748–13, International Society for Optics and Photonics (2016).

[31] Maruska, H. P. and Tietjen, J. J., "The preparation and properties of vapor-deposited single-crystal-line GaN," Appl. Phys. Lett. **15**(10), 327–329 (1969).

[32] Yoshida, S., Misawa, S. and Gonda, S., "Improvements on the electrical and luminescent properties of reactive molecular beam epitaxially grown GaN films by using AlN-coated sapphire substrates," Appl. Phys. Lett. **42**(5), 427–429 (1983).

[33] Nakamura, S., "GaN growth using gan buffer layer," Jpn. J. Appl. Phys. **30**(10A), L1705–L1707 (1991).

[34] Nakamura, S., Mukai, T. and Senoh, M., "In situ monitoring and Hall measurements of GaN grown with GaN buffer layers," J. Appl. Phys. **71**(11), 5543–5549 (1992).

[35] Nakamura, S., "Hole Compensation Mechanism of P-Type GaN Films," Jpn. J. Appl. Phys. **31**(5R), 1258 (1992).

[36] Akasaki, H. A. and M. K. and K. H. and I., "P-Type Conduction in Mg-Doped GaN Treated with Low-Energy Electron Beam Irradiation (LEEBI)," Jpn. J. Appl. Phys. **28**(12A), L2112 (1989).

[37] Nakamura, S., Mukai, T. and Senoh, M., "High-power gan p-n junction blue-light-emitting diodes," Jpn. J. Appl. Phys. **30**(12A), L1998–L2001 (1991).

[38] Nakamura, S., Mukai, T., Senoh, M. and Naruhito, I., "Thermal Annealing Effects on P-Type Mg-Doped GaN Films," Jpn. J. Appl. Phys. **139**(2B), L 139-L 142 (1992).

[39] Nakamura, S. and Mukai, T., "High-Quality InGaN Films Grown on GaN Films," Jpn. J. Appl. Phys. **31**(10B), L1457–L1459 (1992).

[40] Nakamura, S., Senoh, M. and Mukai, T., "P-GaN/N-InGaN/N-GaN Double-Heterostructure Blue-Light-Emitting Diodes," Jpn. J. Appl. Phys. **32**(1A), L8 (1993).

[41] Nakamura, S., Mukai, T. and Senoh, M., “Candela-class high-brightness InGaN/AlGaN double-heterostructure blue-light-emitting diodes,” Appl. Phys. Lett. **64**(13), 1687–1689 (1994).

[42] Nagahama, S. N. and M. S. and N. I. and S., “High-Brightness InGaN Blue, Green and Yellow Light-Emitting Diodes with Quantum Well Structures,” Jpn. J. Appl. Phys. **34**(7A), L797 (1995).

[43] Mukai, Y. N. and M. I. and D. S. and M. S. and T., “White light emitting diodes with super-high luminous efficacy,” J. Phys. D. Appl. Phys. **43**(35), 354002 (2010).

[44] Akasaki, I., Amano, H. and Nakamura, S., “Efficient Blue Light-Emitting Diodes Leading to Bright and Energy-Saving White Light Sources,” Sci. Backgr. Nobel Prize Phys. (2014).

[45] Nakamura, S., Senoh, M., Nagahama, S., Iwasa, N., Yamada, T., Matsushita, T., Sugimoto, Y. and Kiyoku, H., “Room-temperature continuous-wave operation of InGaN multi-quantum-well structure laser diodes with a lifetime of 27 hours,” Appl. Phys. Lett. **70**(11), 1417–1419 (1997).

[46] Nakamura, S., Senoh, M., Nagahama, S. ichi, Iwasa, N., Yamada, T., Matsushita, T., Kiyoku, H. and Sugimoto, Y., “InGaN Multi-Quantum-Well-Structure Laser Diodes with Cleaved Mirror Cavity Facets,” Jpn. J. Appl. Phys. **35**(2B), L217 (1996).

[47] Oh, S. H., Yonkee, B. P., Cantore, M., Farrell, R. M., Speck, J. S., Nakamura, S. and DenBaars, S. P., “Semipolar III-nitride light-emitting diodes with negligible efficiency droop up to ∼1 W,” Appl. Phys. Express **9**(10), 102102 (2016).

[48] Lee, C., Shen, C., Oubei, H. M., Cantore, M., Janjua, B., Ng, T. K., Farrell, R. M., El-Desouki, M. M., Speck, J. S., Nakamura, S., Ooi, B. S. and DenBaars, S. P., “2 Gbit/s data transmission from an unfiltered laser-based phosphor-converted white lighting communication system,” Opt. Express **23**(23), 29779 (2015).

[49] Habib, B. and Baz, B., “Hardware MIMO channel simulator for cooperative and heterogeneous 5G networks with VLC signals,” Lect. Notes Comput. Sci. (including Subser. Lect. Notes Artif. Intell. Lect. Notes Bioinformatics) **9674**, 171–183, Springer, Cham (2016).

[50] Rajbhandari, S., McKendry, J. J. D., Herrnsdorf, J., Chun, H., Faulkner, G., Haas, H., Watson, I. M., O’Brien, D. and Dawson, M. D., “A review of gallium nitride LEDs for multi-gigabit-per-second visible light data communications,” Semicond. Sci. Technol. **32**(2), 023001 (2017).

[51] Lee, C., Zhang, C., Becerra, D., Lee, S., Oh, S. H., Farrell, R. M., Speck, J. S., Nakamura, S., Bowers, J. E. and DenBaars, S. P., “High speed performance of III-nitride laser diode grown on (2021) semipolar plane for visible light communication,” 2016 IEEE Photonics Conf. IPC 2016, 809–810, IEEE (2017).

[52] Lu, T.-C. C., Kao, T.-T. T., Chen, S.-W. S. W., Kao, C.-C. C., Kuo, H.-C. C. and Wang, S.-C. C., “CW lasing of current injection blue GaN-based vertical cavity surface emitting lasers,” 2008 Conf. Lasers Electro-Optics 2008 Conf. Quantum Electron. Laser Sci. **141102**(2008), 1–2 (2008).

[53] Onishi, T., Imafuji, O., Nagamatsu, K., Kawaguchi, M., Yamanaka, K. and Takigawa, S., "Continuous Wave Operation of GaN Vertical Cavity Surface Emitting Lasers at Room Temperature," Quantum Electron. IEEE J. **48**(9), 1107–1112 (2012).

[54] Kawaguchi, M., Imafuji, O., Nagamatsu, K., Yamanaka, K., Takigawa, S. and Katayama, T., "Design and lasing characteristics of GaN vertical elongated cavity surface emitting lasers," Proc. SPIE **8986**, 89861K (2014).

[55] Liu, W.-J., Hu, X.-L., Ying, L.-Y., Zhang, J.-Y. and Zhang, B.-P., "Room temperature continuous wave lasing of electrically injected GaN-based vertical cavity surface emitting lasers," Appl. Phys. Lett. **104**(25), 251116 (2014).

[56] Hsieh, D. H., Tzou, A. J., Lin, D. W., Kao, T. S., Lin, C. C., Chang, C. Y. and Kuo, H. C., "Greatly improved carrier injection in GaN-based VCSEL by multiple quantum barrier electron blocking layer," Proc. Int. Conf. Numer. Simul. Optoelectron. Devices, NUSOD **2015**–**May**(21), 139–140 (2015).

[57] Izumi, S., Fuutagawa, N., Hamaguchi, T., Murayama, M., Kuramoto, M. and Narui, H., "Room-temperature continuous-wave operation of GaN-based vertical-cavity surface-emitting lasers fabricated using epitaxial lateral overgrowth," Appl. Phys. Express **8**(6), 6–9 (2015).

[58] Leonard, J. T., Young, E. C., Yonkee, B. P., Cohen, D. A., Margalith, T., DenBaars, S. P., Speck, J. S. and Nakamura, S., "Demonstration of a III-nitride vertical-cavity surface-emitting laser with a III-nitride tunnel junction intracavity contact," Appl. Phys. Lett. **107**(9), 091105 (2015).

[59] Furuta, T., Matsui, K., Kozuka, Y., Yoshida, S., Hayasi, N., Akagi, T., Koide, N., Takeuchi, T., Kamiyama, S., Iwaya, M. and Akasaki, I., "1.7-mW nitride-based vertical-cavity surface-emitting lasers using AlInN/GaN bottom DBRs," 2016 Int. Semicond. Laser Conf., 1–2 (2016).

[60] Furuta, T., Matsui, K., Horikawa, K., Ikeyama, K., Kozuka, Y., Yoshida, S., Akagi, T., Takeuchi, T., Kamiyama, S., Iwaya, M. and Akasaki, I., "Room-temperature CW operation of a nitride-based vertical-cavity surface-emitting laser using thick GaInN quantum wells Room-temperature CW operation of a nitride-based vertical-cavity surface-emitting laser using thick GaInN quantum wells," Jpn. J. Appl. Phys. **55**, 05FJ11 (2016).

[61] Hamaguchi, T., Fuutagawa, N., Izumi, S., Murayama, M. and Narui, H., "Continuous wave operation of high power GaN-based Blue Vertical Cavity Surface Emitting Lasers Using Epitaxial Lateral Overgrowth," 1–6 (2016).

[62] Hamaguchi, T., Fuutagawa, N., Izumi, S., Murayama, M. and Narui, H., "Milliwatt-class GaN-based blue vertical-cavity surface-emitting lasers fabricated by epitaxial lateral overgrowth," Phys. Status Solidi Appl. Mater. Sci. **213**(5), 1170–1176 (2016).

[63] Hamaguchi, T., Nakajima, H., Ito, M., Mitomo, J., Satou, S., Fuutagawa, N. and Narui, H., "Lateral carrier confinement of GaN-based vertical-cavity surface-emitting diodes using boron ion implantation," Jpn. J. Appl. Phys. **55**(12), 122101 (2016).

[64] Ikeyama, K., Kozuka, Y., Matsui, K., Yoshida, S., Akagi, T., Akatsuka, Y., Koide, N.,

Takeuchi, T., Kamiyama, S., Iwaya, M. and Akasaki, I., "Room-temperature continuous-wave operation of GaN-based vertical-cavity surface-emitting lasers with n-type conducting AlInN/GaN distributed Bragg reflectors," Appl. Phys. Express **9**(10), 102101 (2016).

[65] Leonard, J. T., Yonkee, B. P., Cohen, D. A., Megalini, L., Lee, S., Speck, J. S., DenBaars, S. P. and Nakamura, S., "Nonpolar III-nitride vertical-cavity surface-emitting laser with a photoelectrochemically etched air-gap aperture," Appl. Phys. Lett. **108**(3), 031111 (2016).

[66] Matsui, K., Kozuka, Y., Ikeyama, K., Horikawa, K., Furuta, T., Akagi, T., Takeuchi, T., Kamiyama, S., Iwaya, M. and Akasaki, I., "GaN-based vertical cavity surface emitting lasers with periodic gain structures," Jpn. J. Appl. Phys. **55**(5S), 05FJ08 (2016).

[67] Weng, G., Mei, Y., Liu, J., Hofmann, W., Ying, L., Zhang, J., Bu, Y., Li, Z., Yang, H. and Zhang, B., "Low threshold continuous-wave lasing of yellow-green InGaN-QD vertical-cavity surface-emitting lasers," Opt. Express **24**(14), 15546 (2016).

[68] Yeh, P. S., Chang, C.-C., Chen, Y.-T., Lin, D.-W., Liou, J.-S., Wu, C. C., He, J. H. and Kuo, H.-C., "GaN-based vertical-cavity surface emitting lasers with sub-milliamp threshold and small divergence angle," Appl. Phys. Lett. **109**(24), 241103 (2016).

[69] Chang, T.-C., Kuo, S.-Y., Lian, J.-T., Hong, K.-B., Wang, S.-C. and Lu, T.-C., "High-temperature operation of GaN-based vertical-cavity surface-emitting lasers," Appl. Phys. Express **10**(11), 112101 (2017).

[70] Mei, Y., Xu, R., Xu, H., Ying, L., Zheng, Z., Zhang, B.-P., Li, M. and Zhang, J., "A comparative study of thermal characteristics of GaN-based VCSELs with three different typical structures," Semicond. Sci. Technol. (2017).

[71] Xu, R. B., Mei, Y., Zhang, B. P., Ying, L. Y., Zheng, Z. W., Hofmann, W., Liu, J. P., Yang, H., Li, M. and Zhang, J., "Simultaneous blue and green lasing of GaN-based vertical-cavity surface-emitting lasers," Semicond. Sci. Technol. **32**(10), 105012 (2017).

[72] Forman, C. A., Lee, S., Young, E. C., Kearns, J. A., Cohen, D. A., Leonard, J. T., Margalith, T., DenBaars, S. P. and Nakamura, S., "Continuous-wave operation of m-plane GaN-based vertical-cavity surface-emitting lasers with a tunnel junction intracavity contact," Appl. Phys. Lett. **112**(11), 111106 (2018).

[73] Forman, C. A., Lee, S., Young, E. C., Kearns, J. A., Cohen, D. A., Leonard, J. T., Margalith, T., DenBaars, S. P. and Nakamura, S., "Continuous-wave operation of nonpolar GaN-based vertical-cavity surface-emitting lasers," Proc. SPIE **10532**, 105321C–10532–11 (2018).

[74] Kuramoto, M., Kobayashi, S., Akagi, T., Tazawa, K., Tanaka, K., Saito, T. and Takeuchi, T., "Enhancement of slope efficiency and output power in GaN-based vertical-cavity surface-emitting lasers with a SiO2-buried lateral index guide," Appl. Phys. Lett. **112**(11), 111104 (2018).

[75] Natsumi, H., Junichiro, O., Kenjo, M., Takashi, F., Takanobu, A., Sho, I., Tetsuya, T.,

Satoshi, K., Motoaki, I. and Isamu, A., "A GaN-Based VCSEL with a Convex Structure for Optical Guiding," Phys. status solidi **0**(0), 1700648 (2018).

[76] Higuchi, Y., Omae, K., Matsumura, H. and Mukai, T., "Room-temperature CW lasing of a GaN-based vertical-cavity surface-emitting laser by current injection," Appl. Phys. Express **1**(12), 1211021–1211023 (2008).

[77] Omae, K., Higuchi, Y., Nakagawa, K., Matsumura, H. and Mukai, T., "Improvement in lasing characteristics of GaN-based vertical-cavity surface-emitting lasers fabricated using a GaN substrate," Appl. Phys. Express **2**(5), 5–8 (2009).

[78] Lu, T.-C. C., Chen, S.-W. W., Wu, T.-T. T., Tu, P.-M. M., Chen, C.-H. C.-K. C. H. C. K. C.-H., Chen, C.-H. C.-K. C. H. C. K. C.-H., Li, Z.-Y. Y., Kuo, H.-C. C. and Wang, S.-C. C., "Continuous wave operation of current injected GaN vertical cavity surface emitting lasers at room temperature," Appl. Phys. Lett. **97**(7), 71114 (2010).

[79] Kasahara, D., Morita, D., Kosugi, T., Nakagawa, K., Kawamata, J., Higuchi, Y., Matsumura, H. and Mukai, T., "Demonstration of blue and green GaN-based vertical-cavity surface-emitting lasers by current injection at room temperature," Appl. Phys. Express **4**(7) (2011).

[80] Cosendey, G., Castiglia, A., Rossbach, G., Carlin, J.-F. and Grandjean, N., "Blue monolithic AlInN-based vertical cavity surface emitting laser diode on free-standing GaN substrate," Appl. Phys. Lett. **101**(15), 151113 (2012).

[81] Koyama, F., KINOSHITA, S. and IGA, K., "Room temperature cw operation of GaAs vertical cavity surface emitting laser," IEICE Trans. **71**(11), 1089–1090 (1988).

[82] Koyama, F., Kinoshita, S. and Iga, K., "Room-temperature continuous wave lasing characteristics of a GaAs vertical cavity surface-emitting laser," Appl. Phys. Lett. **55**(3), 221–222 (1989).

[83] Blokhin, S. A., Lott, J. A., Mutig, A., Fiol, G., Ledentsov, N. N., Maximov, M. V., Nadtochiy, A. M., Shchukin, V. a. and Bimberg, D., "Oxide-confined 850 nm VCSELs operating at bit rates up to 40 Gbit/s," Electron. Lett. **45**(10), 501–503 (2009).

[84] Lasers and Electro-optics Society (Institute of Electrical and Electronics Engineers), Optical Society of America., European Physical Society. Quantum Electronics and Optics Division., Quantum Electronics and Laser Science Conference (2008 : San Jose, C. . and Conference on Photonic Applications, S. and T. (2008 : S. J., [Lasers and Electro-Optics, 2008. CLEO 2008. Conference on.], Optical Society of America (2008).

[85] Chang, Y.-C., Wang, C. S. and Coldren, L. A., "High-efficiency, high-speed VCSELs with 35 Gbit/s error-free operation," Electron. Lett. **43**(19), 1022–1023 (2007).

[86] Anan, T., Suzuki, N., Yashiki, K., Fukatsu, K., Hatakeyama, H., Akagawa, T., Tokutome, K. and Tsuji, M., "High-speed 1.1-μm-range InGaAs VCSELs," OFC/NFOEC 2008 - 2008 Conf. Opt. Fiber Commun. Fiber Opt. Eng. Conf., 1–3 (2008).

[87] Park, M., "DVI and HDMI - Copper or Fiber Optics?," 2018,

<http://www.projectorcentral.com/dvi_hdmi_copper_optical.htm> (27 June 2018).

[88] Cheng, H., Gao, J., Wu, H. C., Liu, G., Lau, E., Yuan, L. and Krause, C., "Optics vs. copper - From the perspective of Thunderbolt 3 interconnect technology," China Semicond. Technol. Int. Conf. 2016, CSTIC 2016, 1–3, IEEE (2016).

[89] Pruijmboom, A., Schemmann, M., Hellmig, J., Schutte, J., Moench, H. and Pankert, J., "VCSEL-based miniature laser-Doppler interferometer," Proc. SPIE Vertical-Cavity Surface-Emitting Lasers XII **6908**(1), C. Lei and J. K. Guenter, Eds., 69080I, International Society for Optics and Photonics (2008).

[90] Rudd, M. J., "A laser Doppler velocimeter employing the laser as a mixer-oscillator," J. Phys. E. **1**(7), 723–726 (2002).

[91] Grabherr, M., Gerlach, P., King, R. and Jager, R., "Integrated photodiodes complement the VCSEL platform," Proc. SPIE Vertical-Cavity Surface-Emitting Lasers XIII **7229**, 72290E–72290E–9 (2009).

[92] Raoul, X., Bosch, T., Plantier, G. and Servagent, N., "A double-laser diode onboard sensor for velocity measurements," IEEE Trans. Instrum. Meas. **53**(1), 95–101 (2004).

[93] Mul, F. F., Koelink, M. H., Weijers, a L., Greve, J., Aarnoudse, J. G., Graaff, R. and Dassel, a C., "Self-mixing laser-Doppler velocimetry of liquid flow and of blood perfusion in tissue.," Appl. Opt. **31**(27), 5844–5851 (1992).

[94] Shinohara, S., Yoshida, H., Ikeda, H., Nishide, K. I. and Sumi, M., "Compact and high-precision range finder with wide dynamic range and its application," IEEE Trans. Instrum. Meas. **41**(9105579), 40–44 (1992).

[95] Mukoyama, N., Otoma, H., Sakurai, J., Ueki, N. and Nakayama, H., "VCSEL array-based light exposure system for laser printing," Proc. SPIE **6908**, C. Lei and J. K. Guenter, Eds., 69080H, International Society for Optics and Photonics (2008).

[96] Kondo, T., Takeda, K., Otoma, H., Murakami, A., Sakurai, J., Nakayama, H., Gu, X. and Koyama, F., "Developments of VCSELs for printers and optical communications at Fuji Xerox," 4 March 2016, 97660C, International Society for Optics and Photonics.

[97] Hallereau, S., "Apple iPhone X-IR Dot Projector" (2017).

[98] Kirkpatrick, K., "3D Sensors Provide Security, Better Games," Commun. ACM **61**(6), 15–17 (2018).

[99] Hainich, R. R. and Bimber, O., [Displays, Fundamentals & Applications], CRC Press LLC, Boca Raton, FA (2011).

[100] Satuby, Y. and Orenstein, M., "Limits of the modulation response of a single-mode proton implanted VCSEL," IEEE Photonics Technol. Lett. **10**(6), 760–762 (1998).

[101] Kharzeev, D., "Chirality : from QCD to condensed matter," 2015, <http://physik.uni-graz.at/schladming2015/LectureNotes/Kharzeev4.pdf> (16 July 2018).

[102] Crow, B., Longford, M. and Sawchuk, K., "The Wireless Spectrum," Electron. Des., 240 (2010).

[103] “United States Frequency Allocation Chart.”, 1 (2016).

[104] Evans, D., [The Internet of Things: How the Next Evolution of the Internet is Changing Everything] (2011).

[105] Moench, H., Frey, M., Grabherr, M., Gronenborn, S., Gudde, R., Kolb, J., Miller, M. and Weigl, A., “VCSELs as light source for time-of-flight sensors,” 25 February 2017, 1012204, International Society for Optics and Photonics.

[106] Pruijmboom, A., Booij, S., Schemmann, M., Werner, K., Hoeven, P., van Limpt, H., Intemann, S., Jordan, R., Fritzsch, T., Oppermann, H. and Barge, M., “A VCSEL-based miniature laser-self-mixing interferometer with integrated optical and electronic components,” 12 February 2009, 72210S.

[107] Birkbeck, A. L., Flynn, R. A., Ozkan, M., Song, D., Gross, M. and Esener, S. C., “VCSEL Arrays as Micromanipulators in Chip-Based Biosystems,” Biomed. Microdevices **5**, 47–54 (2003).

[108] Kioupakis, E., Rinke, P., Schleife, A., Bechstedt, F. and Van De Walle, C. G., “Free-carrier absorption in nitrides from first principles,” Phys. Rev. B - Condens. Matter Mater. Phys. **81**(24), 241201(R) (2010).

[109] Wu, M. C., “Micromachining for optical and optoelectronic systems,” Proc. IEEE **85**(11), 1833–1856 (1997).

[110] Marxer, C., Gretillat, M.-A., De Rooij, N. F., Battig, R., Anthamatten, O., Valk, B. and Vogel, P., “Vertical mirrors fabricated by reactive ion etching for fiber optical switching applications,” Proc. IEEE Tenth Annu. Int. Work. Micro Electro Mech. Syst. An Investig. Micro Struct. Sensors, Actuators, Mach. Robot., 49–54, IEEE (1997).

[111] Sung, C. C. and Holzer, J. A., “Scattering of electromagnetic waves from a rough surface Scattering of electromagnetic waves from a rough surface,” Appl. Phys. Lett. **28**(8), 429–431 (1976).

[112] Lin, C. K., Bour, D. P., Zhu, J., Perez, W. H., Leary, M. H., Tandon, A., Corzine, S. W. and Tan, M. R. T., “High Temperature Continuous-Wave Operation of 1.3- and 1.55-um VCSELs With InP/Air-Gap DBRs,” IEEE J. Sel. Top. Quantum Electron. **9**(5), 1415–1421 (2003).

[113] Tao, R., Arita, M., Kako, S. and Arakawa, Y., “Fabrication and optical properties of non-polar III-nitride air-gap distributed Bragg reflector microcavities,” Appl. Phys. Lett. **103**(20), 201118 (2013).

[114] Sharma, R., Haberer, E. D., Meier, C., Hu, E. L. and Nakamura, S., “Vertically oriented GaN-based air-gap distributed Bragg reflector structure fabricated using band-gap-selective photoelectrochemical etching,” Appl. Phys. Lett. **87**(5), 051107 (2005).

[115] Tao, R., Arita, M., Kako, S., Kamide, K. and Arakawa, Y., “Strong coupling in non-polar GaN/AlGaN microcavities with air-gap/III-nitride distributed Bragg reflectors,” Appl. Phys. Lett. **107**(10), 101102 (2015).

[116] Gan, K. G. and Bowers, J. E., “Measurement of gain, group index, group velocity dispersion, and linewidth enhancement factor of an InGaN multiple quantum-well laser

diode," IEEE Photonics Technol. Lett. **16**(5), 1256–1258 (2004).

[117] Lee, S., Forman, C. A., Lee, C., Kearns, J., Young, E. C., Leonard, J. T., Cohen, D. A., Speck, J. S., Nakamura, S. and DenBaars, S. P., "GaN-based vertical-cavity surface-emitting lasers with tunnel junction contacts grown by metal-organic chemical vapor deposition," Appl. Phys. Express **11**(6), 062703 (2018).

[118] Kuwano, Y., Kaga, M., Morita, T., Yamashita, K., Yagi, K., Iwaya, M., Takeuchi, T., Kamiyama, S. and Akasaki, I., "Lateral Hydrogen Diffusion at p-GaN Layers in Nitride-Based Light Emitting Diodes with Tunnel Junctions," Jpn. J. Appl. Phys. **52**(8S), 08JK12 (2013).

[119] Stephan, F., Christian, T., Timo, A. and Detlef, H., "InGaN quantum dot growth in the limits of Stranski–Krastanov and spinodal decomposition," Phys. status solidi **248**(8), 1765–1776 (2011).

[120] Hashemi, E., Bengtsson, J., Gustavsson, J., Stattin, M., Cosendey, G., Grandjean, N. and Haglund, A., "Analysis of structurally sensitive loss in GaN-based VCSEL cavities and its effect on modal discrimination.," Opt. Express **22**(1), 411–426 (2014).

[121] Hashemi, E., Gustavsson, J., Bengtsson, J. J., Stattin, M., Cosendey, G., Grandjean, N., Haglund, A. and Haglund, Å., "Engineering the Lateral Optical Guiding in Gallium Nitride-Based Vertical-Cavity Surface-Emitting Laser Cavities to Reach the Lowest Threshold Gain," Jpn. J. Appl. Phys. **52**(8S), 08JG04 (2013).

[122] Farrell, R. M., Haeger, D. A., Hsu, P. S., Fujito, K., Feezell, D. F., Denbaars, S. P., Speck, J. S. and Nakamura, S., "Determination of internal parameters for AlGaN-cladding-free m-plane InGaN/GaN laser diodes," Appl. Phys. Lett. **99**(17), 171115 (2011).

[123] Minsky, M. S., White, M. and Hu, E. L., "Room-temperature photoenhanced wet etching of GaN," Appl. Phys. Lett. **68**(11), 1531 (1996).

[124] Zhuang, D. and Edgar, J. H., "Wet etching of GaN, AlN, and SiC: a review," Mater. Sci. Eng. R **48**(1), 1–46 (2005).

[125] Lee, S., Mishkat-Ul-Masabih, S., Leonard, J. T., Feezell, D. F., Cohen, D. A., Speck, J. S., Nakamura, S. and DenBaars, S. P., "Smooth and selective photo-electrochemical etching of heavily doped GaN:Si using a mode-locked 355 nm microchip laser," Appl. Phys. Express **10**(1), 011001 (2017).

[126] Holder, C. O., "Nonpolar GaN-based VCSELs" (2013).

[127] Leonard, J. T., [III-Nitride Vertical-Cavity Surface-Emitting Lasers], ProQuest Dissertations & Theses, Santa Barbara (2016).

[128] Kelchner, K. M., Kuritzky, L. Y., Nakamura, S., DenBaars, S. P. and Speck, J. S., "Stable vicinal step orientations in m-plane GaN," J. Cryst. Growth **411**, 56–62 (2015).

[129] Farrell, R. M., Haeger, D. A., Chen, X., Gallinat, C. S., Davis, R. W., Cornish, M., Fujito, K., Keller, S., DenBaars, S. P., Nakamura, S. and Speck, J. S., "Origin of pyramidal hillocks on GaN thin films grown on free-standing m-plane GaN substrates," Appl. Phys. Lett. **96**(23), 231907 (2010).

[130] Hirai, A., Jia, Z., Schmidt, M. C., Farrell, R. M., DenBaars, S. P., Nakamura, S., Speck, J. S. and Fujito, K., "Formation and reduction of pyramidal hillocks on m-plane {1100} GaN," Appl. Phys. Lett. **91**(19), 191906 (2007).

[131] Yamada, H., Iso, K., Saito, M., Fujito, K., DenBaars, S. P., Speck, J. S. and Nakamura, S., "Impact of substrate miscut on the characteristic of m-plane InGaN/GaN light emitting diodes," Japanese J. Appl. Physics, Part 2 Lett. **46**, 2–5 (2007).

[132] Kelchner, K. M., Kuritzky, L. Y., Fujito, K., Nakamura, S., Denbaars, S. P. and Speck, J. S., "Emission characteristics of single InGaN quantum wells on misoriented nonpolar m-plane bulk GaN substrates," J. Cryst. Growth **382**, 80–86 (2013).

[133] Kuritzky, L. Y., Myers, D. J., Nedy, J., Kelchner, K. M., Nakamura, S., Denbaars, S. P., Weisbuch, C. and Speck, J. S., "Electroluminescence characteristics of blue InGaN quantum wells on m-plane GaN 'double miscut' substrates," Appl. Phys. Express **8**, 061002 (2015).

[134] Farrell, R. M., "Growth, Fabrication, and Characterization of Continuous-Wave AlGaN-Cladding-Free m-plane InGaN/GaN Laser Diodes," 300 (2010).

[135] Ryu, H. Y., Ha, K. H., Son, J. K., Lee, S. N., Paek, H. S., Jang, T., Sung, Y. J., Kim, K. S., Kim, H. K., Park, Y. and Nam, O. H., "Determination of internal parameters in blue InGaN laser diodes by the measurement of cavity-length dependent characteristics," Appl. Phys. Lett. **93**(1), 011105 (2008).

[136] Holder, C., Feezell, D., Speck, J. S., DenBaars, S. P. and Nakamura, S., "Demonstration of nonpolar GaN-based vertical-cavity surface-emitting lasers," 13 March 2013, 863906, International Society for Optics and Photonics.

[137] Schillgalies, M., Laubsch, A., Sabathil, M., Avramescu, A., Lutgen, S. and Strauss, U., "Multi-quantum well emission from blue InGaN-based laser," 2008 IEEE 21st Int. Semicond. Laser Conf., 95–96 (2008).

[138] Mackowiak, P., Sarzala, R. P., Wasiak, M., Nakwaski, W., Search, H., Journals, C., Contact, A., Iopscience, M. and Address, I. P., "Radial optical confinement in nitride VCSELS," J. Phys. D. Appl. Phys. **2041**, 2041–2045 (2003).

[139] Cao, X. A., Zhang, A. P., Dang, G. T., Ren, F. and Pearton, S. J., "Plasma Damage in p-GaN," J. Electron. Mater. **29**(3), 256–261 (2000).

[140] Cao, X. A., Zhang, A. P., Dang, G. T., Ren, F., Pearton, S. J., Shul, R. J. and Zhang, L., "Schottky diode measurements of dry etch damage in n- and p-type GaN," J. Vac. Sci. Technol. A Vacuum, Surfaces, Film. **18**(4), 1144 (2000).

[141] Cao, X. A., Pearton, S. J., Zhang, A. P., Dang, G. T., Ren, F., Shul, R. J., Zhang, L., Hickman, R. and Van Hove, J. M., "Electrical effects of plasma damage in p-GaN," Appl. Phys. Lett. **75**(17), 2569 (1999).

[142] Cao, X. A., Pearton, S. J., Dang, G. T., Zhang, A. P., Ren, F. and Hove, J. M. Van., "GaN N- and P-Type Schottky Diodes : Effect of Dry Etch Damage," IEEE Trans. Electron Devices **47**(7), 1320–1324 (2000).

[143] Perchoux, J., Rissons, A. and Mollier, J.-C., "Multimode VCSEL model for wide

frequency-range RIN simulation," Opt. Commun. **281**(1), 162–169 (2008).

[144] Degen, C., Elsaber, W. and Fischer, I., "Transverse modes in oxide confined VCSELs: Influence of pump profile, spatial hole burning, and thermal effects," Opt. Express **5**(3), 38 (1999).

[145] Jeon, S. and Yang, G. M., "Vertical-Surface-Emitting Diode Using a GaN Buried Tunnel Junction Current Aperture," J. Korean Phys. Soc. **41**(6), 1021–1024 (2002).

[146] Malinverni, M., Martin, D. and Grandjean, N., "InGaN based micro light emitting diodes featuring a buried GaN tunnel junction," Appl. Phys. Lett. **107**(5), 051107 (2015).

[147] Diagne, M., He, Y., Zhou, H., Makarona, E., Nurmikko, A. V., Han, J., Takeuchi, T. and Krames, M., "A High Injection Resonant Cavity Violet Light Emitting Diode Incorporating (Al,Ga)N Distributed Bragg Reflector," Phys. Status Solidi **188**(1), 105–108 (2001).

[148] Jeon, S. R., Song, Y. H., Jang, H. J., Yang, G. M., Hwang, S. W. and Son, S. J., "Lateral current spreading in GaN-based light-emitting diodes utilizing tunnel contact junctions," Appl. Phys. Lett. **78**(21), 3265–3267 (2001).

[149] Ozden, I., Makarona, E., Nurmikko, a. V., Takeuchi, T. and Krames, M., "A dual-wavelength indium gallium nitride quantum well light emitting diode," Appl. Phys. Lett. **79**(2001), 2532–2534 (2001).

[150] Takeuchi, T., Hasnain, G., Corzine, S., Hueschen, M., Schneider, R. P. J., Kocot, C., Blomqvist, M., Change, Y., Lefforge, D., Krames, M. R., Cook, L. W., Stockman, S. a., Schneider, Jr., R. P., Kocot, C., Blomqvist, M., Chang, Y., Lefforge, D., Krames, M. R., Cook, L. W., et al., "GaN-Based Light Emitting Diodes with Tunnel Junctions," Jpn. J. Appl. Phys. **40**(8), 861–863 (2001).

[151] Diagne, M., He, Y., Zhou, H., Makarona, E., Nurmikko, a. V., Han, J., Waldrip, K. E., Figiel, J. J., Takeuchi, T. and Krames, M., "Vertical cavity violet light emitting diode incorporating an aluminum gallium nitride distributed Bragg mirror and a tunnel junction," Appl. Phys. Lett. **79**(22), 3720 (2001).

[152] Cao, X. a., Stokes, E. B., Sandvik, P. M., LeBoeuf, S. F., Kretchmer, J. and Walker, D., "Diffusion and tunneling currents in GaN/InGaN multiple quantum well light-emitting diodes," IEEE Electron Device Lett. **23**(9), 535–537 (2002).

[153] Fedison, J. B., Chow, T. P., Lu, H. and Bhat, I. B., "Electrical characteristics of magnesium-doped gallium nitride junction diodes," Appl. Phys. Lett. **72**(22), 2841–2843 (1998).

[154] Sakowski, K., Marcinkowski, L., Krukowski, S., Grzanka, S. and Litwin-Staszewska, E., "Simulation of trap-assisted tunneling effect on characteristics of gallium nitride diodes," J. Appl. Phys. **111**(12), 123115 (2012).

[155] Chow, T. P. and Ghezzo, M., "III-Nitride, SiC, and Diamond Materials For Electronic Devices," Mater. Res. Soc. Symoposium Proc., D. K. Gaskill, C. D. Brandt, and R. J. Nemanich, Eds., 69–73, Materials Research Society, Pittsburgh, PA (1996).

[156] Young, E. C., Yonkee, B. P., Wu, F., Oh, S. H., DenBaars, S. P., Nakamura, S. and Speck, J. S., "Hybrid tunnel junction contacts to III–nitride light-emitting diodes," Appl. Phys. Express **9**(2), 022102 (2016).

[157] Zhang, Y. M., Piprek, J., Margalit, N., Anzlowar, M. and Bowers, J., "Cryogenic performance of double-fused 1.5-μm vertical cavity lasers," J. Light. Technol. **17**(3), 503–508 (1999).

[158] Kubota, M., Okamoto, K., Tanaka, T. and Ohta, H., "Temperature dependence of polarized photoluminescence from nonpolar m-plane InGaN multiple quantum wells for blue laser diodes," Appl. Phys. Lett. **92**(1), 011920 (2008).

[159] Piprek, J., "<title>High-temperature lasing of long-wavelength VCSELs: problems and prospects</title>," 4 April 1997, 182–193, International Society for Optics and Photonics.

[160] Piprek, J., Akulova, Y. A., Babic, D. I., Coldren, L. A. and Bowers, J. E., "Minimum temperature sensitivity of 1.55 μm vertical-cavity lasers at −30 nm gain offset," Appl. Phys. Lett. **72**(15), 1814 (1998).

[161] Piprek, J., Babić, D. I., Bowers, J. E., Babić, D. I. and Bowers, J. E., "Simulation and analysis of 1.55 μm double-fused vertical-cavity lasers," J. Appl. Phys. **81**(8), 3382.

[162] Kioupakis, E., Rinke, P., Delaney, K. T. and Van de Walle, C. G., "Indirect Auger recombination as a cause of efficiency droop in nitride light-emitting diodes," Appl. Phys. Lett. **98**(16), 161107 (2011).

[163] Watanabe, N., Kimoto, T. and Suda, J., "The temperature dependence of the refractive indices of GaN and AlN from room temperature up to 515 °C," J. Appl. Phys. **104**(10), 106101 (2008).

[164] Osinski, M. and Nakwaski, M., "Effective Thermal Conductivity Analysis of 1.55um InGaAsP/InP Vertical-Cavity Top-Surface-Emitting Microlasers," Electron. Lett. **29**(11), 1015 (1993).

[165] Nakamura, S., "Recent Performance of Nonpolar/semipolar/polar GaN-based emitting devices and bulk crystal growth (plenary)"," Proc. First Int. Conf. White LED Solid State Light., 64.

[166] Bohling, C. and Sigmund, W., "Self-Limitation of Native Oxides Explained," Silicon **8**(3), 339–343 (2016).

[167] Leonard, J. T., Cohen, D. A., Yonkee, B. P., Farrell, R. M., Denbaars, S. P., Speck, J. S. and Nakamura, S., "Smooth e-beam-deposited tin-doped indium oxide for III-nitride vertical-cavity surface-emitting laser intracavity contacts," J. Appl. Phys. **118**(14), 145304 (2015).

[168] Kyle, E. C. H., Kaun, S. W., Young, E. C. and Speck, J. S., "Increased p-type conductivity through use of an indium surfactant in the growth of Mg-doped GaN," Appl. Phys. Lett. **106**(22), 222103 (2015).

[169] Kaun, S. W., Mazumder, B., Fireman, M. N., Kyle, E. C. H., Mishra, U. K. and Speck, J. S., "Pure AlN layers in metal-polar AlGaN/AlN/GaN and AlN/GaN heterostructures

grown by low-temperature ammonia-based molecular beam epitaxy," Semicond. Sci. Technol. **30**(5), 055010 (2015).

[170] Tamboli, A. C., Schmidt, M. C., Hirai, A., DenBaars, S. P. and Hu, E. L., "Photoelectrochemical Undercut Etching of m-Plane GaN for Microdisk Applications," J. Electrochem. Soc. **156**(10), H767 (2009).

[171] Yamada, T., Ito, J., Asahara, R., Watanabe, K., Nozaki, M., Nakazawa, S., Anda, Y., Ishida, M., Ueda, T., Yoshigoe, A., Hosoi, T., Shimura, T. and Watanabe, H., "Comprehensive study on initial thermal oxidation of GaN(0001) surface and subsequent oxide growth in dry oxygen ambient," J. Appl. Phys. **121**(3), 035303 (2017).

[172] Ghazali, N., Mahmood, M., Yasui, K. and Hashim, A., "Electrochemically deposited gallium oxide nanostructures on silicon substrates," Nanoscale Res. Lett. **9**(1), 120 (2014).

[173] Guo, S., Zhang, X., Hao, Z., Gao, G., Li, G. and Liu, L., "In2O3 cubes: synthesis, characterization and photocatalytic properties," RSC Adv. **4**(59), 31353–31361 (2014).

[174] Hwang, J. M., Hsieh, J. T., Ko, C. Y., Hwang, H. L. and Hung, W. H., "Photoelectrochemical etching of InxGa1−xN," Appl. Phys. Lett. **76**(26), 3917 (2000).

[175] Yan, T., Wang, X., Long, J., Liu, P., Fu, X., Zhang, G. and Fu, X., "Urea-based hydrothermal growth, optical and photocatalytic properties of single-crystalline In(OH)3 nanocubes," J. Colloid Interface Sci. **325**(2), 425–431 (2008).

[176] Comey, A. M., [A Dictionary of Chemical Solubilities: Inorganic], Macmillan and Company (1896).

[177] Sa Yoon Kang, McLaren, T., Wenge Zhang and Lee, Y. C., "Thermosonic bonding for flip-chip assembly," Proc. 1995 IEEE Multi-Chip Modul. Conf., 75–80, IEEE Comput. Soc. Press.

[178] Torunbalci, M. M., Demir, E. C., Donmez, I., Alper, S. E. and Akin, T., "Gold-tin eutectic bonding for hermetic packaging of MEMS devices with vertical feedthroughs," SENSORS, 2014 IEEE, 2187–2190 (2014).

[179] So, W. W. and Lee, C. C., "Fluxless process of fabricating In-Au joints on copper substrates," IEEE Trans. Components Packag. Technol. **23**(2), 377–382 (2000).

[180] Deillon, L., Hessler, T., Hessler-Wyser, A. and Rappaz, M., "Growth of intermetallic compounds in the Au–In system: Experimental study and 1-D modelling," Acta Mater. **79**, 258–267 (2014).

[181] Sung, H.-K., Wang, C. and Kim, N.-Y., "Reliability study of Au-in solid-liquid interdiffusion bonding for GaN-based vertical LED packaging," J. Micromechanics Microengineering **25**(12) (2015).

[182] Deillon, L., Hessler-Wyser, A., Hessler, T. and Rappaz, M., "Solid-liquid interdiffusion (SLID) bonding in the Au–In system: experimental study and 1D modelling," J. Micromechanics Microengineering **25**(12), 125016 (2015).

[183] Lee, C. C., Wang, C. Y. and Matijasevic, G., “Au-In Bonding Below the Eutectic Temperature,” IEEE Trans. Components, Hybrids, Manuf. Technol. **16**(3), 311–316 (1993).

[184] Luu, T. T., Hoivik, N., Wang, K., Aasmundtveit, K. E. and Vard??y, A. S. B., “Characterization of Wafer-Level Au-In-Bonded Samples at Elevated Temperatures,” Metall. Mater. Trans. A Phys. Metall. Mater. Sci. **46**(6), 2637–2645 (2015).

[185] Thesis, D., [Solid Liquid Inter- diffusion wafer-level bonding for MEMS packaging Solid Liquid Interdiffusion wafer-level bonding for MEMS packaging Thesis submitted for the degree of Philosophiae Doctor] (2015).

[186] Pankove, J. I., Maruska, H. P. and Berkeyheiser, J. E., “Optical absoption of gan,” Appl. Phys. Lett. **17**(5), 197–199 (1970).

[187] Bentoumi, G., Deneuville, A., Beaumont, B. and Gibart, P., “Influence of Si doping level on the Raman and IR reflectivity spectra and optical absorption spectrum of GaN,” Mater. Sci. Eng. B **50**(1–3), 142–147 (1997).

[188] Kisin, M. V., Brown, R. G. W. and El-Ghoroury, H. S., “Optical characteristics of III-nitride quantum wells with different crystallographic orientations,” J. Appl. Phys. **105**(1), 013112 (2009).

[189] Mroziewicz, B., Bugajski, M. and Nakwaski, W., [Physics of Semiconductor Lasers], Elsevier Science (2017).