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Indium Antimonide Nanowires: Synthesis, Characterization, and Applications

A Dissertation submitted in partial satisfaction
of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

by

Miroslav Valentinov Penchev

June 2012

Dissertation Committee:
Dr. Mihrimah Ozkan, Chairperson
Dr. Cengiz S. Ozkan
Dr. Roger Lake

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2012

The Dissertation of Miroslav Valentinov Penchev is approved:

Committee Chairperson

University of California, Riverside

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ABSTRACT OF THE DISSERTATION

Indium Antimonide Nanowires: Synthesis, Characterization, and Applications

by

Miroslav Valentinov Penchev

Doctor of Philosophy, Graduate Program in Electrical Engineering
University of California, Riverside, June 2012
Dr. Mihrimah Ozkan, Chairperson

Indium Antimonide (InSb) nanowires with a diameter ranging from 30 nm to 200 nm, were synthesized by electrochemical disposition in anodized alumina and polycarbonate porous membranes. In addition, epitaxial single crystalline InSb nanowires with diameters ranging from 5 nm to 100 nm, were synthesized by chemical vapor deposition (CVD) using Au nanoparticles as catalyst. Structural and material characterization of InSb nanowires was carried out by scanning electron microscopy (SEM), energy dispersive X-ray spectroscopy (EDS), X-ray diffraction (XRD), and transmission electron microscopy (TEM). Electrical characterization of InSb nanowires was conducted by fabricating nanowire field effect transistors (FETs) by electron-beam lithography and direct metal deposition assisted by focused ion-beam (FIB). Conductive atomic force microscopy (CAFM) was employed in current-voltage (I-V) measurements of InSb nanowires as a local contact electrode measuring conductivity of a short cannel

InSb nanowire. In addition, CAFM probe tip was also used as a local gate electrode to InSb nanowire FET. Temperature-dependent I-V measurements were conducted to elucidate the transport mechanism through the metal contact-nanowire junction. Rapid thermal annealing was applied for fabricating Ohmic contacts to InSb nanowires.

Depletion mode n-type back-gated FETs based on CVD grown InSb nanowires, exhibited high I_{ON}/I_{OFF} ratio of 10^6, a subthreshold slope as low as 90 mV/dec, and electron mobility as high as 110 $cm^2V^{-1}s^{-1}$. Diameter-dependent dependent I-V measurements were performed on the InSb nanowires, revealing the correlation between electron mobility, doping concentrations and nanowire diameter.

InSb nanowire-based FET chemical sensors were used for detection of water, Isopropanol, and Acetone vapors. The mechanism of operation of these sensor devices was investigated. In addition, Pt nanoparticle decorated InSb nanowire sensors were employed for detection of 0.1% H_2 gas. The performance of InSb nanowire sensor was compared to a graphene-based Hydrogen sensor.

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Chapter 1

Introduction

For the past forty years transistor's size on integrated circuits has been shrinking at an exponential rate and the number of transistors on chips has doubled every two years, while the cost per functionality on chip has significantly decreased, according to Moore's law.[1] This trend in semiconductor fabrication has lead to an ever increasing computational power, which has brought great technological advancement and scientific progress, and it has had a tremendous impact on nearly every area of our lives. However, this aggressive downscaling of integrated circuits has driven the size of conventional silicon transistor in the nanoscale regime. This has given rise to two main challenges for the current conventional Si-CMOS integrated circuit fabrication and functionality. One of them being a fundamental physical law limitation, which is a direct result of new physical phenomena occurring at critical device dimensions, as they are currently approaching several nanometers. The second hurdle is technological one, it stems from the continuously increasing complexity, cost and number of fabrication processes necessary to sustain this aggressive downscaling. As the channel gate length of silicon field effect transistor approaches 10 nm the off-state leakage current becomes a serious issue due to short channel effects.[2] As a result, the increase of static and dynamic power due to short channel effects, make power consumption the limiting factor in further scaling.[3] The increase of power consumption, on the other hand leads to increase in heat generated on chip, making thermal management and dissipation one of the major obstacles.[4]

Another direct implication of device miniaturization is the compromised reliability of materials as critical dimensions continue to shrink, such as leakage through gate dielectric insulators, increase of electromigration in Al, and increased grain defects and larger resistance in Cu interconnects.[5, 6] But perhaps, the biggest challenge to overcome in order to keep up with Moore's law is one of an economic origin, most notably seen in the exponentially increasing cost of the photolithographic process, with extreme ultraviolet photolithography (EUV) becoming the most likely successor of the current UV photolithography technology.[7]

One approach to address the challenges in sustaining Moore's law is to look at alternatives to the current Si based CMOS technology in terms of implementation of new materials, novel design architectures, and new device operation concepts. One such example of an alternative to the planar CMOS geometry is the three dimensional tri-gate, FinFet transistor, a device which holds promise for better electrostatic gate control, increased subthreshold slope, and decreased off-state leakage current.[8] A similar three dimensional transistor channel approach is achieved by the nanowire transistor, especially with the wrap-around gate nanowire transistor.[9, 10] With respect to incorporating novel materials and potentially substituting conventional Si channel to address some of the challenges stated above, most notably explored materials include III-V compound semiconductors, Ge, carbon nanotubes, and graphene.[11-14]

Yet another approach to address the challenges of further miniaturizations is the bottom-up synthesis of nanostructures with controlled geometry and dimensions, which

offer some advantageous properties owing to their unique nature. The benefit of the bottom-up approach is two-fold, while it can alleviate technological limits of top-down fabrication dependent upon photolithography, at same time it can give rise to new physical phenomena observed at the nanoscale. Among those novel nanostructured materials, nanowires have attracted great amount of attention by the research community.[15-18]. Nanowires are cylindrical nanostructures in which at least two dimensions are limited to less than 100 nm, consequently nanowires can exhibit quantum confinement effects making them favorable functional materials for device applications.[17] Nanowire field effect transistors (NWFETs) with a surround gate lead to better electrostatic control and lower off-state current, furthermore 1D nanowire can exhibit ballistic electron transport due to quantum confinement thus increasing the on-state current. Integration of 3D vertical standing nanowire arrays can result in increased device density and complexity on chip.[19] Nanowires allow realization of large lattice mismatch axial hetero-structure devices due to fast lateral strain relaxation.[20] In addition, nanowires have potential to be used as interconnects between device components in integrated circuits.[21]

Group III-V compound semiconductor materials exhibit several appealing electrical and optical properties such as high electron mobility, high thermoelectric efficiency, surface sensitivity, and quantum confinement effects at relatively large dimensions. These properties make III-V materials ideal candidates for nanowire applications in electronics, optoelectronics, and sensing. Indium Antimonide is a III-V compound semiconductor of large interest, which possesses a great potential for ultra fast

and low static power dissipating transistors. InSb has a low energy band-gap of 0.17 eV, the highest electron mobility (30,000 $cm^2V^{-1}s^{-1}$), and the highest saturation velocity (5 x 10^7 cm/s) of any known semiconductor.[22] It also has high free mean path and high electron velocity. Researchers from Intel and QinetiQ have demonstrated an InSb quantum well transistor operating at 50% higher switching frequency while consuming ten times less DC power than conventional Si transistor,[23] however almost no research has been done on InSb nanowire transistors. The high electron mobility is essential property for high-speed, low-power device applications, while narrow band gap allows effective fabrication of ohmic metal contacts to nanostructures. The small effective mass of InSb provides strong quantum confinement effects and a large energy level separation in the nanoscale structures.

The objective of my research work has focused on exploring the potential of InSb nanowires as a possible candidate III-V material nanostructure, for addressing some of the challenges in current Si-CMOS technology. This survey investigates two different synthesis methods, material characterization, electrical characterization, and finally glances at some applications the InSb nanowires.

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Chapter 2

Synthesis and Material Characterization of InSb Nanowires

2.1 Introduction

Nanowires are defined as cylindrical nanostructures with a diameter of less than 100 nm, while their length can range from hundreds of nanometers to tens of microns. Nanowires may be defined by their materials make up in organic and inorganic, or they can be designated based on their properties as in the case of semiconductor, metallic, and oxide (insulator) nanowires. There are several contributing factors that have been a major drive for the increased scientific interest, research effort, and literature publications on nanowires in the last decade. The main one being, nanowires can be synthesized by a bottom-up approach allowing the precise control of critical dimensions to few nanometers with high reproducibility. Second, nanowires can be produced with high yield and high throughput at lower cost compared to conventional top-down approach. Third, nanowires exhibit unique physical phenomena due to their constrained dimensions, which may prove to be advantageous for number of applications, and perhaps can give rise to the development of new conceptual devices. Furthermore, nanowire geometry and bottom-up synthesis permit realization of novel devices architecture with increased device complexity and density. The bottom-up synthesis methods produce smooth surfaces and sharp axial and radial hetero-interfaces, thus minimizing carrier scattering and resulting in higher carrier mobility.[1, 2] In addition to this, the fact that nanowires with diameter of only several nanometers can maintain their electrical properties is the

reason applications in electronics are the main topic of interest in nanowire research, mainly due to the demands for further downscaling imposed by Moore's law. Some of the research efforts towards meeting those objectives, based on inorganic semiconductor nanowires include the realization of p-n junction within a single nanowire [3, 4] and a p-n junction established by bringing two nanowires into contact [5]. Much of the research effort has been focused on fabrication and characterization of nanowire field effect transistors (NWFETs) and developing a process methodology and technology for their integration with Si-CMOS.[3, 4]

There has been a significant interest in the area of hetero-structure nanowires, nanowires allow strain relaxation between large lattice mismatch materials, which is otherwise not possible in bulk semiconductors, thus realizing new hetero-interface devices. Nanowire based hetero-structured resonant tunneling diodes (RTDs) have been demonstrated, having the advantage of using large lattice mismatch materials leading to better device performance.[6] Furthermore, single electron transistors based on hetero-structure nanowires have been demonstrated, showing potential for low power application and sensor applications.[7] Additionally, memory devices based on hetero-structured nanowires have demonstrated superior performance to conventional flash memory.[8]

Another topic of great interest in the scientific exploration of nanowires has been in optical and optoelectronic applications of nanowires, the main reason being the ability tune semiconductor bandgap by controlling nanowire diameter.[9, 10] Light emitting

diodes (LEDs) generating different colors have been produced based on various III-V material nanowires.[5, 11, 12] Nanowire based lasers and single photon sources have been demonstrated, exhibiting good electrical performance and efficiency.[13] Ge nanowire based photoresistors have been reported [14], as well as Ge nanowire based visible light detectors [15]. Las but not least, nanowire-based solar cells have been realized, exhibiting high photon absorption due to the increased nanowire surface area. [16, 17]

Indium Antimonide (InSb) is a semiconductor material well known for its direct narrow band gap of 0.17 eV at 300 K, very high electron mobility of 7.7 x 10^4 $cm^2V^{-1}s^{-1}$, high electron saturation velocity of $5 \cdot 10^7$ $cm \cdot s^{-1}$, and ballistic length up to 0.7 μm, the highest of any known semiconductor except possibly for carbon nanotubes. The narrow energy bandgap (0.17 eV) corresponds to the mid-wavelength infrared transmission window 3-5 μm. Due to its unique electronic and optoelectronic properties InSb has been employed in a wide variety of applications, such as infrared sensors and emitters, magnetic field sensors, toxic gas sensors, and most recently in low-power high speed electronic devices[18]. Despite the increasing interest in InSb, a limited number of studies have been conducted on InSb nanowires, most of which have focused on the synthesis of nanowires and only few reported studies have investigated the electronic, optoelectronic, thermoelectric, and magnetoresistve properties of InSb nanowires. The objective of my research is the focused on the synthesis of high quality crystalline InSb nanowires and investigation of their unique electronic properties and possible application.

2.2 Nanowire synthesis methods

There are two general approaches to the synthesis of nanowires first one is the top-down approach, while the second is the bottom up approach. The top-down synthesis approach involves etching and removal of unwanted material to produce nanostructures of desired shapes and dimensions from large bulk material. This technique has been adopted from the conventional semiconductor processing, and often employs dry plasma chemical etching or wet chemical etching, therefore it depends on photolithography or some sort of a hard mask. The advantage of the top-down synthesis is that it is compatible with the already well developed semiconductor process technology and methodology, the latter however possesses a major drawback, since the critical dimensions of nanostructures are dictated by the current limitations of process technology, namely UV photolithography. There is yet another major disadvantage of a top-down fabrication of nanostructures especially significant and detrimental to nanowire applications in electronics and optoelectronics; it is a direct consequence of the etching process which produces rough crystal surfaces. With that in mind it is sensible to turn to the bottom-up synthesis approach, as a viable solution for approaching some of the technological obstacles imposed by Moore's law. The bottom-up fabrication, in contrast to the top-down approach, relies on the self assembly of atoms or molecules to form nanostructures of desired shape and dimensions. In the case of inorganic semiconductor materials it often involves the controlled formation of nanostructure crystal materials from liquid phase or vapor phase. This method can produce highly organized and uniform nanostructures with high degree of control and reproducibility.

Commonly there are two distinct methods for bottom-up synthesis of nanowires, template assisted and freestanding. In the first method a template is used to direct the growth and restrict it to the shape of the template (Figure 2.1a,b), therefore the ultimate dimensions and geometry of the nanostructures are pre-determined by the template.[19] In the second approach, free standing nanowires grow away from a nucleation point on a substrate or in a solution (Figure 2.1c,d). The latter method has some apparent advantage over the template assisted method, namely in the template assisted method control over nanowire dimensions is restricted by the limitations of the method used to fabricate the template to begin with. Dimensions of freestanding nanowires, on the other hand, are controlled during growth by the relative growth parameters and the size of the initial nucleation point.

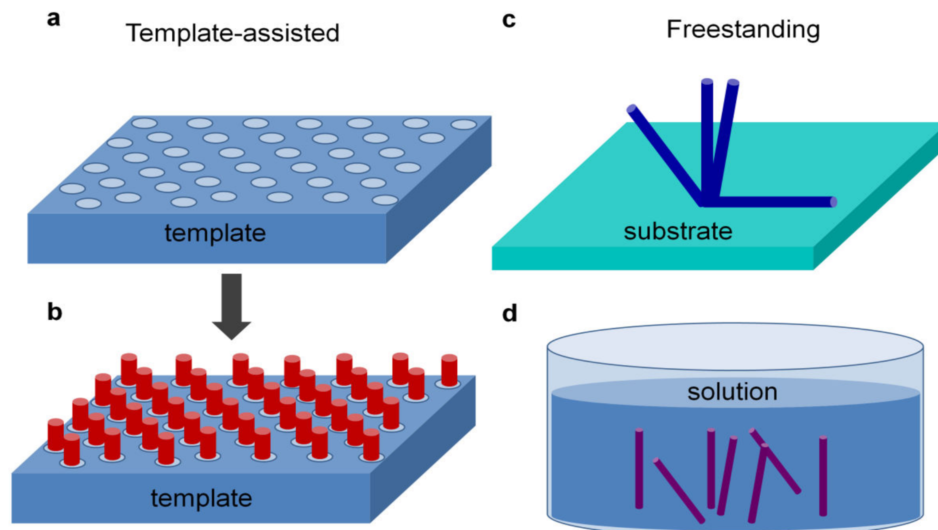

Figure 2.1 a) A negative template for nanowire synthesis. b) Nanowires grown in the pores of a template. c) Freestanding nanowire grown on a substrate. c) Freestanding nanowires synthesized in a solution.

Moreover, depending on the growth mechanism, nanowires synthesis can be divided into two sub-categories, which are solution-based synthesis and vapor phase synthesis. The solution based growth techniques include approaches such as electrodeposition, sol-gel synthesis, chemical vapor deposition, electroless deposition, hydrothermal method, and sonochemical method.[20] Most of the vapor phase growth techniques utilize templates for growing nanowires, while some of them such as hydrothermal and sonochemical methods are template free. The vapor-phase synthesis approach includes vapor-liquid-solid (VLS), vapor-solid (VS), vapor-solid-solid (VSS) mechanisms of growth. Depending on the method used to deliver the vapor precursor, nanowire synthesis can achieved by chemical vapor deposition (CVD), metal-organic chemical vapor deposition (MOCVD), laser ablation, carbothermal reduction, chemical beam epitaxy (CBE), thermal evaporation and thermal decomposition, and plasma arc discharge and current induced methods.[21] In this work only two of the mentioned above approaches were explored for the synthesis of InSb nanowires. First is template assisted, solution-based method by electrochemical deposition, the other is vapor phase method by chemical vapor deposition of freestanding nanowires.

2.3 InSb nanowire synthesis by electrochemical deposition

Different methods have been used to fabricate Indium Antimonide nanowires employing various vapor-liquid-solid methods such as chemical vapor deposition[22, 23], metal-organic vapor phase epitaxy[24], chemical beam epitaxy[25], while in liquid phase

synthesis electrochemical deposition has been successfully utilized[26]. Electrochemical deposition process, using porous membranes as templates, is an effective and low-cost method for fabricating InSb nanowires with very uniform diameter, with high yield and throughput. Therefore we have employed this method to synthesized InSb nanowires with crystalline structure, with diameters ranging from 30 to 200 nanometers by electrochemical deposition in porous anodized alumina membranes (AAM) and polycarbonate membrane templates.[27, 28]

There are two commonly used methods for fabricating membranes with hollow cylindrical pores of nanoscale diameter. First one employs nuclear track etching method, the second method is achieved by anodizing aluminum foils. Track etched membranes are prepared by irradiation of very thin membranes (5-20μm) with heavy charged particles, which leave hollow tracks through the membrane due to coulomb explosion. As the heavy charged particles knock out some the electrons of the atoms in the membrane, the repulsion of the positively charged atoms causes them to separate thus leaving a hollow channel (Figure 2.2a). The narrow channels can then be broadened to the desired diameter by chemical etching with HF or NaOH, depending on the membrane material used. Common membrane materials are mice, glass, polycarbonate and polyethylene terephthalate (PET). Another type of frequently used templates in the synthesis of nanowires is anodized alumina membranes. As their name suggests this type of membrane is produced by electrochemical anodization process, where a thin film of Al is placed in the electrolytic bath serving as the anode, while a platinum electrode serves as the cathode (Figure 2.2b). When a DC potential is applied between the anode and

cathode, aluminum oxide is formed on the Al foil surface, further reaction causes etching of the oxide layer and formation of pores. The pore diameter and pore density are controlled by the applied potential, current density, electrolyte type and concentration and pH level.

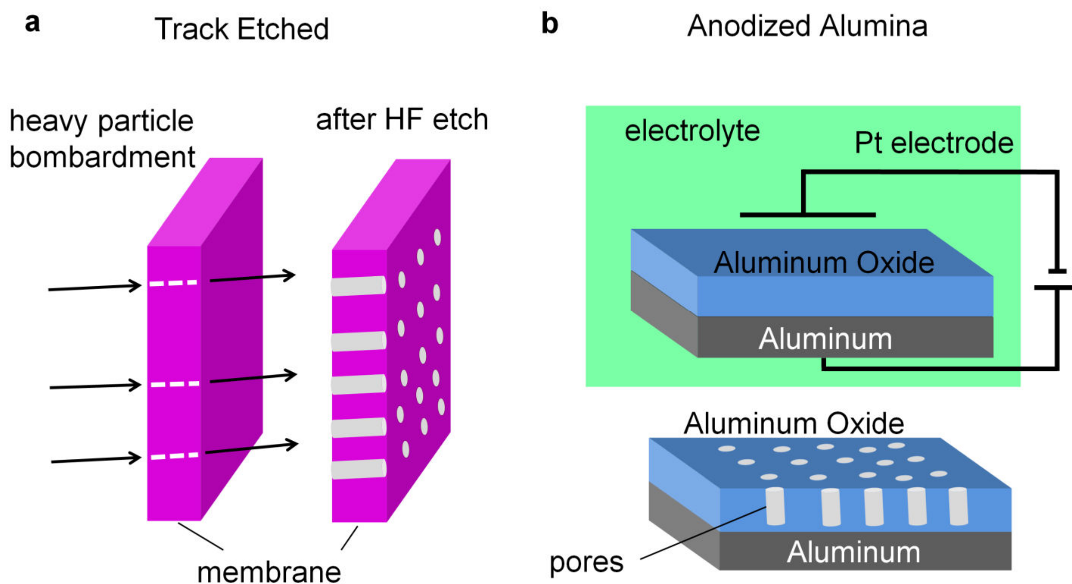

Figure 2.2 a) Fabrication of a porous membrane by track etching. b) Fabrication of anodized alumina by electrochemical etching.

The polycarbonate and anodized alumina templates used in this work for the synthesis of InSb nanowires by electrochemical deposition are commercially available from Whatman and Synkera. The diameters of the pores on the anodic alumina membranes used were 13 nm, 30 nm, 50 nm and 200 nm and the thickness of all AAMs used here is about 60 µm. While the diameter of pores on the polycarbonate templates used were about 50 nm, 100 nm and thickness of 20 µm. The electrochemical deposition was carried out in a typical three-electrode electrochemical cell with a platinum electrode

serving as the counter electrode (anode), Ag/AgCl as reference electrode, and the AAMs with Au back layer as the working electrode (cathode), a depiction of it is shown in Figure 2.3. The electrolyte used contains the In and Sb cations necessary for the nanowire growth, it is an aqueous solution of 0.1 M $SbCl_3$, 0.15 M $InCl_3$, 0.36 M citric acid and 0.17 M potassium citrate at a pH level of 1.8.[29] The citrate ions are used as the complexing agents to bring the deposition potential of In and Sb closer to maintain binary growth. Since the porous membrane is not electrically conductive a layer of gold (about 200 nm thick) is deposited on one side of the membrane, and then covered by insulative polymer on the back side, thus leavening the only conductive area exposed to electrolyte at the bottom of pores. The template serving as the working electrode is then immersed in the electrolyte, a brief ultrasonication is used to overcome the capillary action of the membrane's nanopores and force the electrolyte in the channels. A constant voltage potential is applied between the positively charged anode and the negatively charged cathode, positively charged In and Sb ions are attracted to the cathode where they are reduced by accepting electrons and are effectively deposited on the electrode, while oxidation or donation of electrons occurs at the anode. The constant voltage potential is monitored by the reference electrode and controlled by the potentiostat/galvanostat (Princeton Applied Research. Model: Potentiostat 263A), which is in turn controlled by a computer interface (Figure 3). Another parameter, which is also monitored as the reaction evolves, is the current flow between the working electrode and the counter electrode.

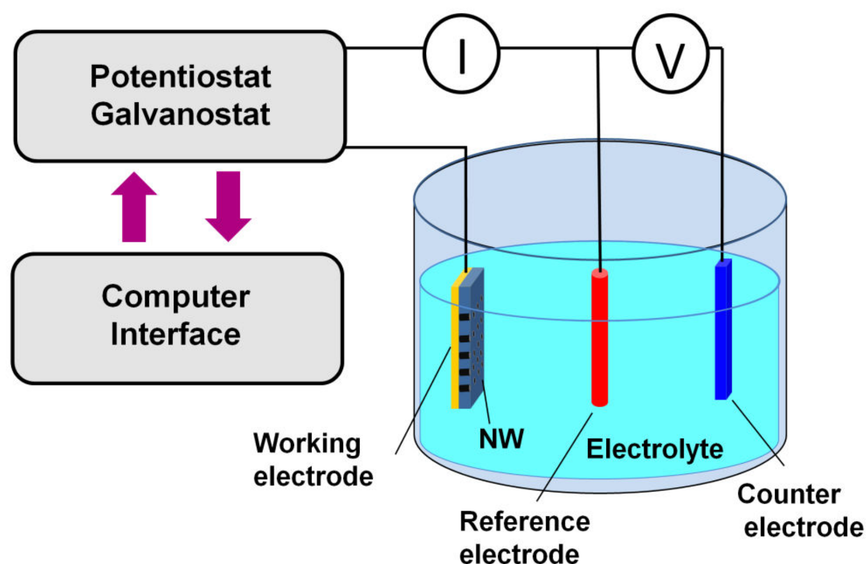

Figure 2.3 Three-electrode electrochemical deposition set-up used for synthesis of nanowires.

As In and Sb ions start filing the channels of the template, the distance between the tip of the nanowires and the anode decreases thus the current flow increases, until the pores are filled to the top surface of membrane and the current starts to saturate. Thus the length of the nanowires is controlled by the deposition time and the recorded current may be used as indicator of whether the pores have been completely filled. A typical deposition was carried out for about 40 minutes under the deposition potential of − 1.5 V vs Ag/AgCl reference electrode at room temperature.[29] After the process is completed the template is removed from the electrolyte solution and rinsed in deionized (DI) water, the sample is then transferred to an acetone bath to dissolve the polymer insulating the back of the Au layer, followed by isopropyl alcohol (IPA) rinse and N_2 blow drying. The next step involves the removing the Au layer from the template, which is achieved by wet

etching in Potassium Iodide solution. Finally, the nanowires are freed from the template by dissolving it and suspending them in the etchant solution. For the anodize alumina membrane NaOH solution was used to etch it, while for the polycarbonate template chloroform was used. The nanowires are transferred from the etchant solution to DI water by a repeated process of centrifuging, pipetteing out the solution, and replacing it with DI water. Figure 2.4 depicts a process flow chart of nanowire deposition in a porous template.

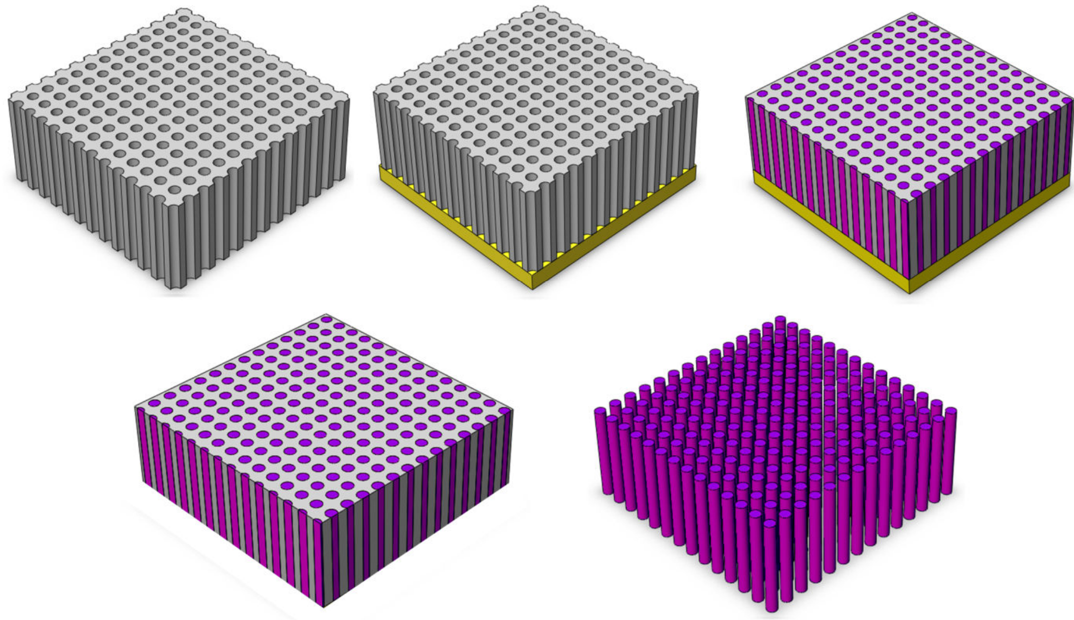

Figure 2.4 Flow chart of template-assisted electrochemical deposition of nanowires, representing the porous membrane template, with a gold layer deposited on one side of the membrane, followed by nanowire growth inside the template, consequently Au layer is etched, finally template is etched freeing nanowires in solution.

2.4 Material characterization of InSb nanowires synthesized by electrochemical deposition

The material and structural quality of the as-grown InSb nanowires suspended in DI water was characterized by scanning electron microscopy (SEM), transmission electron microscopy (TEM), X-ray diffraction analysis (XRD), and energy dispersive X-ray spectroscopy (EDS).[27, 28, 30-32] Here I will provide some background information on each of these experimental techniques and instrumentation set-up used. Particular focus is attended to scanning electron microscopy, as it is the main imaging tool used to assess nanowire quality after growth, and also used to conduct elemental EDS analysis on the InSb compound nanowires. In addition SEM is employed as a nanofabrication tool in the fabrication of nanowire devices by electron beam lithography, which shall be discussed in detail in the next chapter.

Scanning electron microscopy (SEM) has become an indispensable tool in nanotechnology. It is a fast, non destructive imaging technique with of a nanometer scale resolution, which is very versatile and can be applied on practically any type of material with minimal sample preparation. In addition to the high magnification 3D-like topographical images, scanning electron microscopy can provide information about the sample's composition, atomic number, and electrical properties. Furthermore, scanning electron beam is commonly employed in nanofabrication in electron beam lithography for creating patterns with critical dimensions of several nanometers.

One of the main advantages of SEM is its high resolution of imaging, as low as 1nm. The limit of resolution is defined as the minimum distance between two points at which the two points are perceived as identical objects. Resolution is limited by the wavelength of the illumination source due to diffraction and interference, and was formulated by Ernst Abbe with the following equation.[33]

$$d = \frac{0.61\lambda}{n \sin \alpha}$$

where d is resolution limit, λ is the wavelength of the illumination source, n is the index of refraction of medium between the object and objective lens relative to free space, and α is the half angle of the cone of light from specimen plane. Common practice to achieve higher resolution is to use a radiation source of shorter wavelength, or increase the refractive index of medium, or increase the half angle, or any combination of all three approaches. The first approach however, has greater potential than the other two, and therefore in SEM a beam of electrons of a very short wavelength, are employed as the illumination source. Electrons are accelerated by extremely high tension voltages of, usually on the order of 1 kV-40 kV, which results in wavelengths of 0.0387 nm to 0.006 nm, accordingly. Comparing this numbers to the wavelength of visible light (390-750 nm), which is five orders of magnitude larger, it can be easily seen how much more powerful SEM imaging can be compared to optical microscopy.

The concept of scanning electron microscopy was first proposed by Max Knoll, after the invention and development transmission electron microcopy TEM, which uses the same idea of beam of accelerated electrons as the illumination source.[34] Early

pioneer work in SEM was conducted by Manfred von Ardenne, who added scanning coils to a transmission electron microscope, thus constructing the first scanning transmission electron microscope (STEM).[35] Further development work on SEM was conducted from the late 1940s to the early 1960s by Prof. Charles Oatley and his students Dennis McMullan , Ken Smith, O. C. Wells, Tom Everhart, and Gary Stewart, until it became a commercial product in 1965.[36-39] Although SEM has been developed and improved throughout the years, the main components of the modern SEM instrument remain the same; electron gun, electron column, scanning system, detectors, video display, vacuum system and electronics controls are shown in Figure 2.5.[40] The source of electrons is the electron gun, which works on the principle of thermionic emission or field emission, and often employs Tungsten or Lanthanum Hexaboride as the electron source. After electrons have been emitted at very high velocity, a beam of electrons is formed by the magnetic field created by the first set of alignment coils. The electron beam then passes through the condenser aperture which constricts the beam diameter. Next the electron beam passes through two electromagnetic lenses called condenser lenses, where the electron beam cross-over diameter is further reduced. The final lens, the objective lens is used to focus the electron beam on the specimen surface. In addition to the objective lens, scan coils are sued to raster scan the beam over the sample, and a final objective aperture is used to limit the beam diameter. The incident beam of electrons scanned on the specimen's surface, generates emissions of various kinds from the sample, which can be captured by different types of detectors. The captured signals are amplified and displayed on a CRT display. All of these components must be enclosed in a high vacuum chamber,

which is achieved by number of different vacuum pumps such diffusion pump, turbo pumps, and ion pumps.

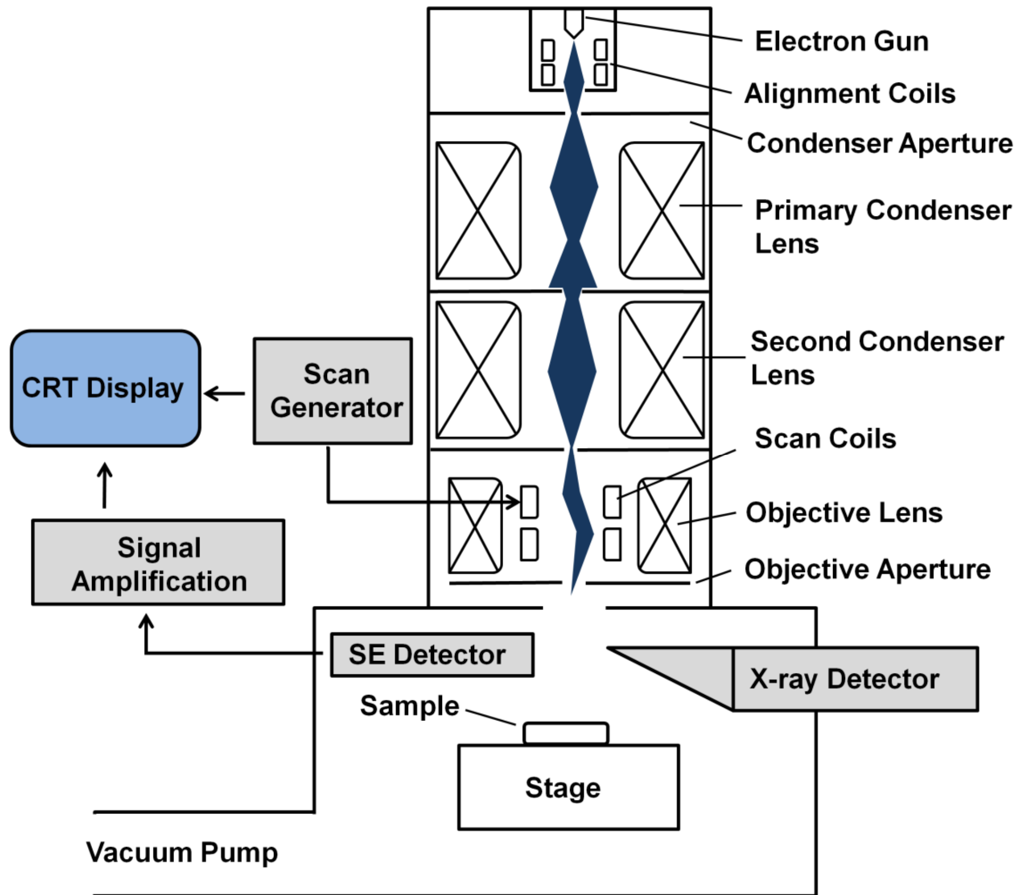

Figure 2.5 Schematic of main component of SEM instrument.

There are four types of possible interactions between an incident electron and the sample. First, the electron transmitted through the sample without any collisions. Second, the electron undergoes an inelastic collision with the nucleus of an atom in the sample, without losing any energy and is re-emitted from the sample. Third, the electron undergoes an elastic collision with electrons of an atom in the sample, losing some

energy, resulting in emissions of different types of electrons from the sample. Last, the incident electron can undergo both elastic and inelastic collisions with an atom in the sample. During elastic scattering there are several processes involved including plasmon excitation, phonon excitation, secondary electron emission, continuous X-ray generation, and ionization of inner shells of atoms. Figure 2.6a depicts both elastic and inelastic scattering due to incident electrons. One type of electrons emitted from the sample due to elastic scattering effects is secondary electrons (SE). This type of emission is most commonly used in SEM imaging. SEs have low energies (<5 eV) and escape the sample from a depth of less than 10 nm from the surface, which is the reason they produce topographical information of very high resolution (1 nm). The emitted SEs are captured by Everhart–Thornley detector, the electron signals are converted to photons by a scintillator and carried out to a photomultiplier where the photon signals are amplified and then converted to electrical signals. The electron signals are outputted on a CRT monitor where they are interpreted as brightness differences.[41] The perceived (3-D like) image of specimen’s surface roughness and texture is a result of the topographical contrast generated by SE electrons. When an electron from an inner atomic shell is emitted from the sample due to elastic collisions, an electron from outer shell would fill in the empty spot in the inner shell, and by doing so an X-ray signal is emitted from the sample. This type of characteristic X-ray emission is often used in SEM instruments to provide information about the elements present in the sample, and it is called energy dispersive x-ray spectroscopy (EDS).

In elastic scattering, there is little or no change in energy but change in momentum (angle change due to deflection) and can result in the incident electron being emitted back from the sample, This type of emitted electrons are called backscattered electrons (BSE), they provide useful topographical information as well as information about the atomic number of the sample. BSEs escape the sample surface with energy larger than 50 eV, from a depth of the sample up to 500 nm. Figure 2.6b depicts the interaction of incident beam of electrons with the sample, which is limited to a pear shaped fraction of the sample at about 1μm depth from the surface, called the interaction volume.

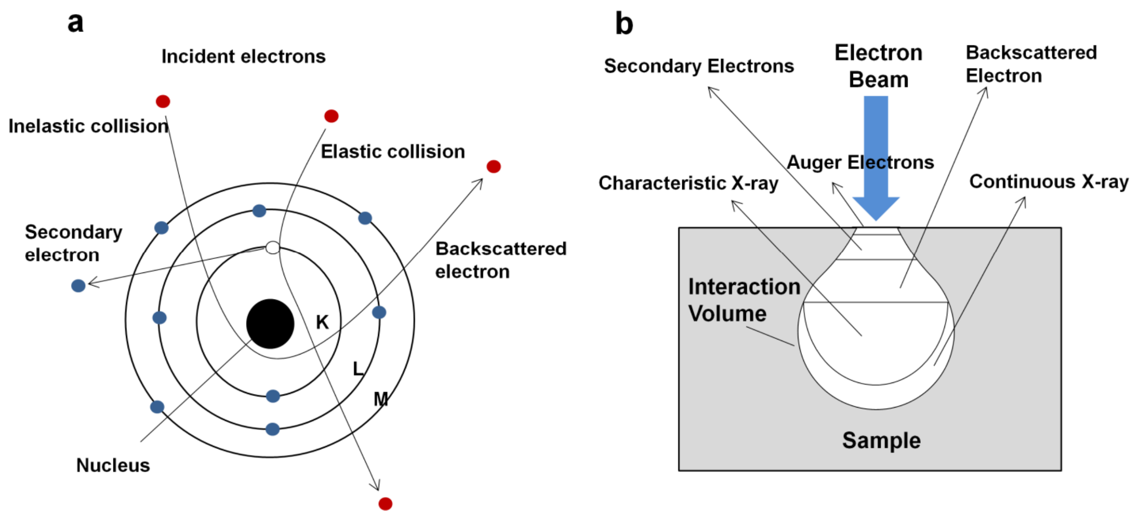

Figure 2.6 a) Inelastic and elastic scattering caused by of incident electrons. b) Interaction of incident electron beam with sample.

All of the SEM imaging and e-beam lithography work was conducted by Carl Zeiss Leo Supra 55 SEM. For SEM imaging the important parameters that need to be optimized depending on the nature of the specimen are accelerating voltage of e-beam,

objective aperture, working distance, stigmation, and aperture alignment. The accelerating voltage determines the depth of interaction volume of incident electrons with the sample, and can be reduced to provide more detailed topographical surface information, or increased to obtain composition information of the sample. Common values of accelerating voltage used for imaging NWs were in the order of 5 kV to 10 kV. The working distance is the distance from the SEM column to the sample, increasing the working distance results in larger depth of focus, which can be beneficial if imaging a sample with large topographical contrast, such as in the case of standing NWs on the growth substrate. Decreasing the working distance can result in larger resolution and is necessary when very high magnification is required, such as in the case of a nanowire with diameter less than 10nm. Common working distance used was between 3 mm to 8 mm. The aperture size used for SEM imaging in most cases was 30 μm, although smaller aperture size was used for e-beam lithography. Astigmatism in the e-beam is corrected by adjusting stigmator coils and aperture align is performed to farther improve the image resolution. EDS analyses on InSb nanowires quantifying In and Sb by atomic percentage was performed by a Carl Zeiss Leo XB1540 SEM system.

X-ray diffraction (XRD) is a versatile, rapid, non-destructive technique that reveals detailed information about the chemical composition and crystallographic atomic-scale structure of crystalline and poly-crystalline solids.[42] The concept of XRD is based on the pioneering work of William H. Bragg and son William L. Bragg who studied the interference pattern of X-rays scattered by crystals.[43, 44] Bragg's diffraction law is given by the following equation

$$n\lambda = 2d_{hkl}\sin(\theta)$$

where n is an integer, λ is the wavelength of the X-ray irradiation source, 2θ is the angle between the incident X-ray beam and the scattered beam by the crystal lattice, d_{hkl} is the spacing between two neighboring crystal planes and is defined by following equation

$$d_{hkl} = \frac{\alpha}{\sqrt{h^2 + k^2 + l^2}}$$

where α is the lattice constant and h, k, l are the crystallographic Miller indices of the crystal plane. Figure 2.7 shows a depiction of the diffraction of incident X-rays with atomic planes of a solid crystal structure.

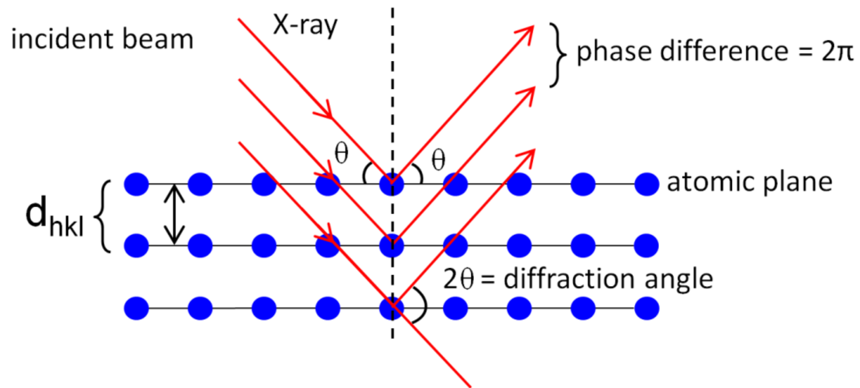

Figure 2.7 X-ray diffraction by crystal solid.

XRD is an essential tool in the material characterization of crystalline semiconductor nanowires, because of their important technological applications in

nanoelectronic and optoelectronic devices, where high structural crystalline quality is critical for device performance. XRD uses information about the position, intensity, width, and shape of diffraction peaks from a nanowire sample. The peak positions in the X-ray diffraction pattern are often used to determine the chemical composition and the crystal phase structure of nanowires. Usually nanowires are single crystalline and grow in a preferred crystal orientation, the growth direction is critical parameter for most nanowire applications, as it can greatly influence the electron and phonon transport in semiconductor nanowires. However not all nanowires in a sample grow in the same preferential direction, a quantitative phase analysis by XRD can reveal how much of each phase is present in the nanowire sample. By accurately measuring peak positions, the unit cell lattice parameters of each of the phases present in the nanowire sample can be determined. Stress analysis in nanowires can be performed by X-ray diffraction based on measuring angular lattice strain distributions by measuring the change in the d-spacing with different orientations of the nanowire sample. In binary and ternary alloy semiconductor nanowires, where compositional modulation is employed in order to tune the energy band gap, XRD analysis can be used the determine unit lattice constants corresponding to specific alloy composition. The X-ray source used in this work is a copper $K\alpha$ and the diffraction angle 2θ was scanned from 10 to 90 degrees.

Transmission electron microscopy (TEM) was the first electron microscope conceptualized and realized in 1931 by Ernst Ruska and Max Knoll. The interest in electron microscopy increased quickly due to an earlier publication by Louis de Broglie revealing the actual wavelength of electron waves, which meant that electron microscopy

had a potential of achieving atomic resolution. Only several year later the first commercial transmission electron microscopes were available in England.[45] The modern TEM instrument is similar to SEM in its design and components; it consists of high vacuum column chamber, high accelerating voltage electron source, number of electromagnetic lenses, a specimen holder, and an image acquisition and display system. A major difference between SEM and TEM, is that in the latter the electrons are accelerated by voltages of up to 300 kV so that they can go through the sample, which in turn has to be very thin (about a hundred nanometers). The images obtained by TEM are formed by the transmitted through the sample electrons, which are recorded on a phosphor screen or a CCD image sensor. A common type of TEM imaging mode is the bright field, in which contrast is produced as a result of absorption and reflection of certain electrons by the specimen. Another type of image obtained with TEM from a crystalline sample is the diffraction pattern. Diffraction pattern is a result of Bragg's scattering of the incident electrons by the crystal planes in the sample to discrete spots. Diffraction pattern can be obtained by changing the focus from the image plane to the back focal plane. Figure 2.8 shows the diffraction patterns obtained from a single crystal, a few crystals and a polycrystalline samples, distinct pattern is observed for a single crystal, while only ring patterns are observed for polycrystalline and amorphous samples.

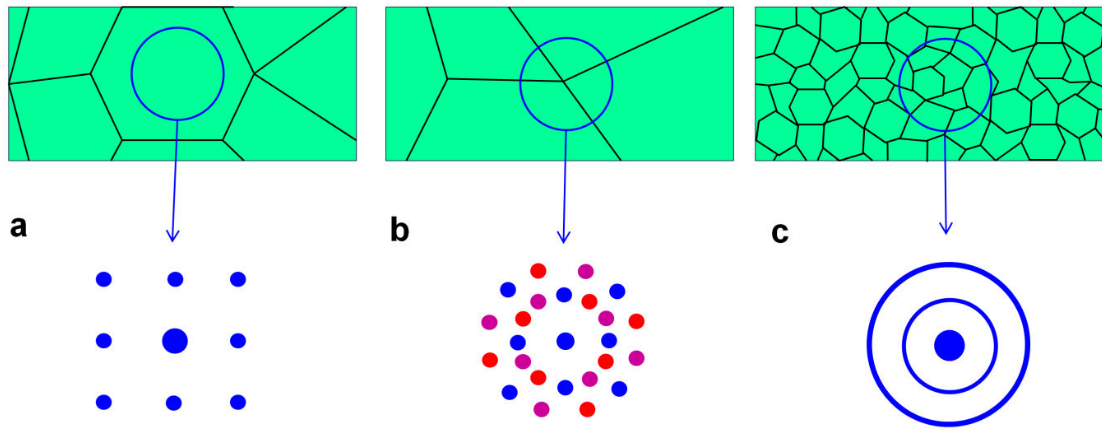

Figure 2.8 a) Diffraction pattern of cubic single crystal. b) Few crystals b) Polycrystalline sample

TEM selected area electron diffraction (SAED) pattern is particularly valuable in the study of single crystalline materials. It can reveal information about the crystallographic space group, crystal orientation relative to the electron beam, and lattice defects in the crystal. Another type of image obtained by TEM is the high resolution transmission electron microscopy (HRTEM), it is capable of achieving atomic resolution and as such it is an indispensable tool in the study of atomic arrangement of a crystal structure.[46] HRTEM image is constructed based on the phase change of electron waves exiting the specimen, due to interaction with the crystal lattice of the sample and Bragg's scattering. Figure 2.9 is showing a typical bright field image of an InSb nanowire and several diffraction patterns obtained from the InSb nanowire from different orientations achieved by tilting the nanowire specimen. TEM imaging requires special sample preparation, the specimen must be cut to a thin slice (micrometer thickness) and additionally polished or milled to about ~100 nm thickness. However, in the case of

nanowire imaging this is not necessary since nanowires are already less than 100-200 nm, instead the nanowires were deposited directly onto a carbon supported copper TEM grid. The TEM imaging was conducted by CM-300 equipped with an energy-dispersive X-ray spectroscopy (EDS) module.

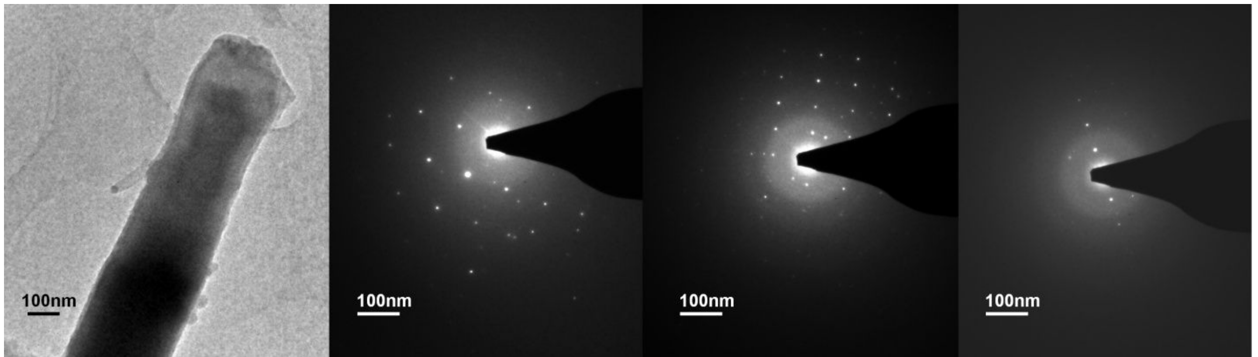

Figure 2.9 Bright field TEM image on InSb nanowire and SAED patterns obtained from different orientation of the nanowire sample.

As stated earlier, two types of templates, anodized alumina membranes (AAM) and polycarbonate (PC), were used in the synthesis of InSb nanowires by electrochemical deposition. Figure 2.10a shows a scanning electron microscopy (SEM) cross-sectional image of an AAM template with InSb nanowires embedded in it, it can be seen that the InSb nanowires are uniformly distributed inside the template's pores, highly ordered, parallel to each other, and their diameters are all about 200 nm, corresponding to the pore diameter of the AAM template used. Figure 2.10b shows the bundles of nanowires after freeing them from a membrane with diameter of 200 nm, it is observed that the nanowires are uniform in diameter and have a smooth surface, Figure 2.10c shows an image of InSb nanowires of 30nm diameter deposited on a Si substrate after AAM template removal,

while Figure 2.10c is an SEM image of a corresponding single nanowire with diameter of about 30nm, it appears to be straight with smooth surface without any visible defects. This shows that depending on the pore diameter of the AAM template, InSb nanowire arrays with different diameters can be obtained. The length of InSb nanowires varies between 5 μm to 20 μm, which corresponds with the deposition, although limited to the maximum thickness of the AAM template. Another factor affecting nanowire length is the post-synthesis procedures, since long nanowires with high aspect ratio can be broken during centrifuging and transfer process. The length of the as-grown nanowires can be modulated by changing the thickness of the AAM or the deposition time.

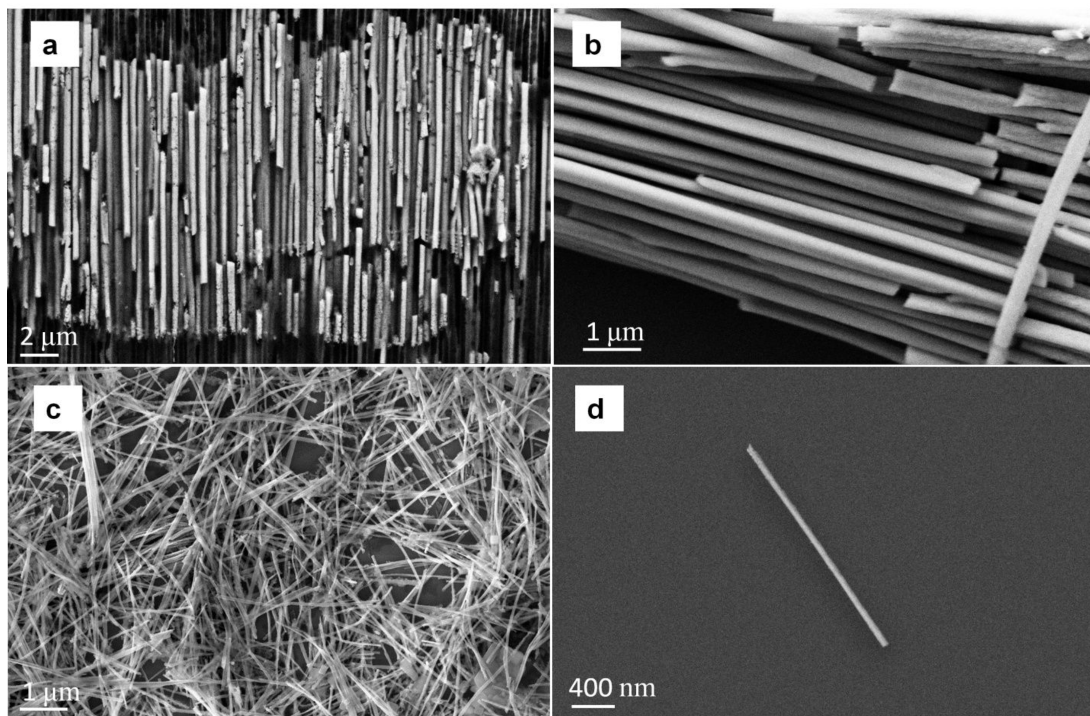

Figure 2.10 a) SEM image of InSb nanowires deposited inside an AAM membrane. b) SEM image of a bundle of 200 nm diameter InSb nanowires released from AAM template. c) SEM of a bundle of 30 nm diameter InSb nanowires after they are removed from the AAM template. d) SEM image of a single 30 nm diameter InSb nanowire.

To determine the elements present in the InSb nanowires and the crystal structure of the nanowires EDS and XRD analysis were performed, in that order.[29] Figure 2.11a shows the energy dispersive spectrum (EDS) of a single InSb nanowire and Figure 2.11b shows the X-ray diffraction (XRD) pattern of InSb nanowires. EDS analysis was performed on the bundle of nanowires, as well as on a single nanowire. The quantitative analysis on the nanowire, indicates approximately 50:50 (In:Sb) atomic % ratio, confirming the nanowires to be compound Indium Antimonide. The diffraction peaks obtained by XRD can be indexed to a cubic zinc-blended phase of InSb crystal. It can be seen that intensity of the diffraction peak at $2\theta = 39.34°$ is relatively stronger than the other diffraction peaks, indicating that the InSb nanowires deposited in AAM template grow preferentially along [220] crystal direction.

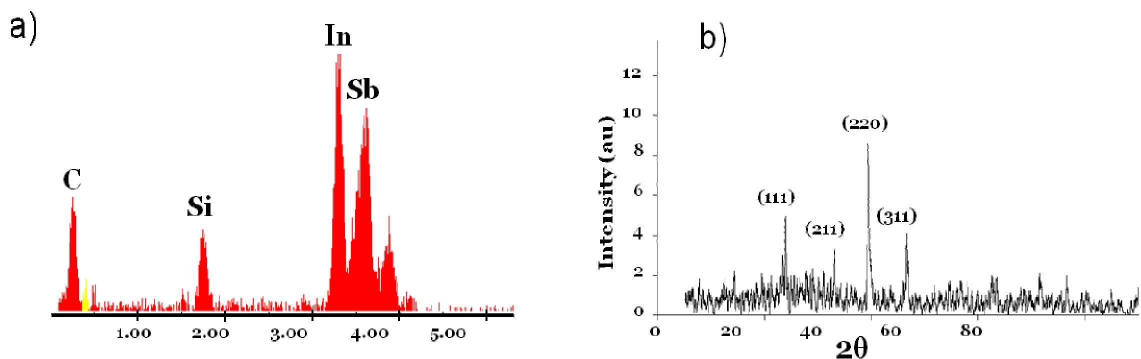

Figure 2.11 a) Energy dispersive spectrum of a single InSb nanowire. b) X-ray diffraction pattern of InSb nanowire arrays show four preferred directions of growth.

The transmission electron microscope (TEM) images of one single InSb nanowire released from AAMs is shown in Figure 2.12, the corresponding selected-area electron diffraction (SAED) pattern indicates that the InSb nanowires are single crystalline in

Figure 2.12a. The SAED pattern was taken along the nanowires, but changes along the length of the nanowires. This indicates that the nanowires are single crystaline with a slight structural deformation along the length which is seen in the high resolution TEM (HRTEM) image in Figure 2.12b revealing the twinning pattern present in the crystal structure.

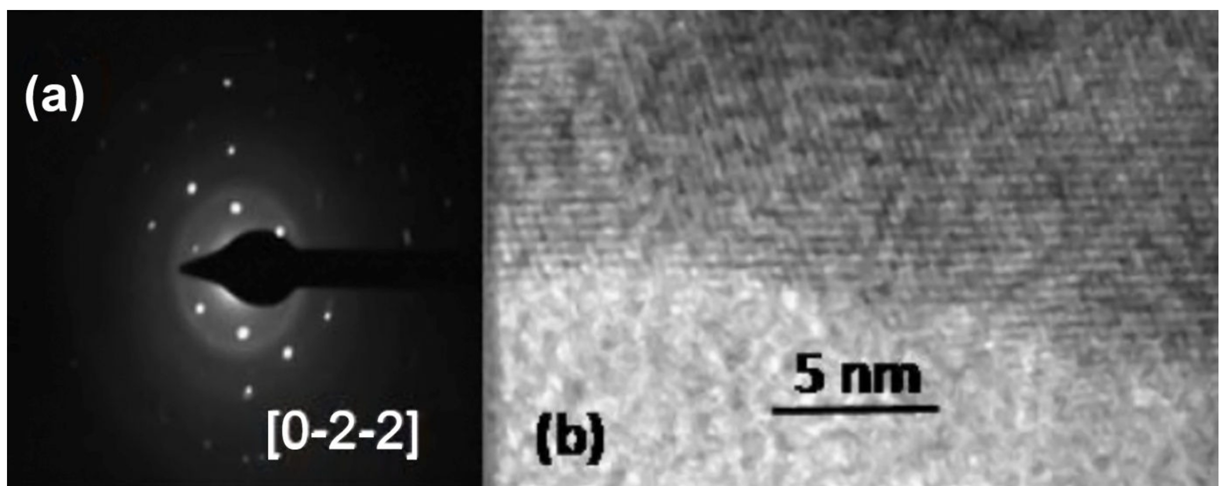

Figure 2.12 a) Selected area diffraction pattern (SAED) obtained by TEM shows hexagonal pattern on a [0-2-2] zone axis. b) High resolution TEM image of the junction between an atomically abrupt inter-twinning.

Polycarbonate templates were also used to for the synthesis of InSb nanowires, since organic membranes do not require harsh etching chemicals for their removal, and therefore latter process is less damaging to the grown nanowires.[47] Two methods were used for dissolving the PC membrane to free the nanowires. Figure 2.13a shows an SEM image of an array of InSb nanowires after the PC membrane has been etched by a brief oxygen plasma exposure, note that nanowires are still attached to the Au layer on which they were synthesized. Figure 2.13b is an SEM image InSb nanowires grown in a PC

template which has been dissolved by Chloroform. Another difference between the PC template and the AAM template is displayed by the geometry of the released nanowires, while in AAM template some nanowire exhibit branching, the nanowires produced in PC template show conical geometry, which can be seen in Figures 10a,b. These morphological differences are a consequence of the different methods used to produce the AAM and PC templates, and show that in terms of morphology and dimension, nanowires produced by template-assisted synthesis are restricted to the limitations of the templates used.

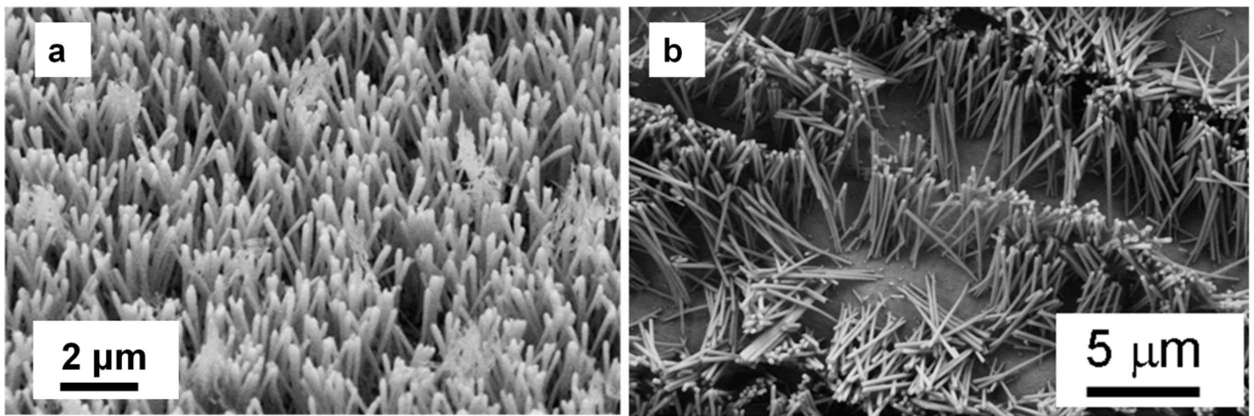

Figure 2.13 a) InSb nanowire array after polycarbonate template is etched by oxygen plasma. b) InSb nanowires after PC template is dissolved in Chloroform.

In addition to compound semiconductor nanowires, electrochemical deposition can be employed to synthesize binary and ternary alloy nanowires. Here we have shown the possibility to obtain compound $In_{0.5}Sb_{0.5}$ nanowires and alloy $In_{0.3}Sb_{0.7}$, antimony rich nanowires by selectively applying a deposition potential during growth of -0.6V or -1.8V, respectively.[47] Figures 2.14a and b show typical SEM images of as-grown composition

modulated $In_{0.5}Sb_{0.5}$ and $In_{0.3}Sb_{0.7}$ nanowire bundles respectively. The nanowires were synthesized in a PC with pore diameter of 100 nm. The images were taken after the as-grown nanowires were freed and suspended in DI water, from the conductive Au thin film, by a gentle sonication. The relative composition of In and Sb in the electrodeposited $In_{1-x}Sb_x$ nanowires was determined from energy dispersive X-ray spectroscopy in SEM, measurements obtained from an individual nanowire. Using the measured radiations from the EDS spectra we quantitatively determined the relative In and Sb at % composition as representatively shown for $In_{0.5}Sb_{0.5}$ and $In_{0.3}Sb_{0.7}$ nanowires in Figures 2.14c and d, respectively. In both cases the EDS spectrum shows that the as-grown nanowires consist of In and Sb in an atomic ratio of approximately 1:1 and 3:7 and the In:Sb composition along individual nanowires varies within 5% difference. This finding suggests that appropriate alloying of In and Sb within the nanowires has been achieved without forming any obvious disorder in the structure or stoichiometric composition. The EDS results were reproducible over the entire axial length of single nanowires obtained from random locations over the entire growth substrate, demonstrating that this technique is capable of producing $In_{1-X}Sb_x$ nanowires with uniform and well controlled compositions over large areas.

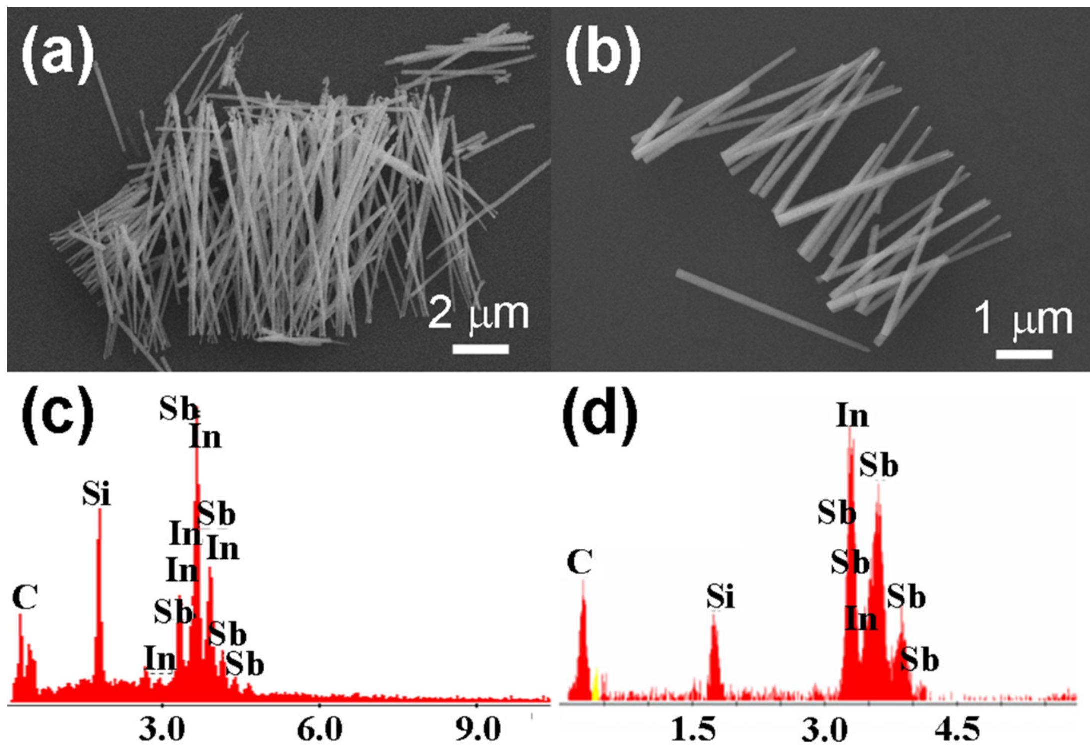

Figure 2.14 a) and b) SEM image of a representative bundle of as-grown $In_{0.5}Sb_{0.5}$ and $In_{0.3}Sb_{0.7}$, NWs respectively. c) and d) EDS spectrum taken from the NW bundles shown in a) and b).

2.5 Synthesis of InSb nanowires by chemical vapor deposition

Despite the low cost and high throughput of the electro-chemical synthesis method for InSb nanowires, TEM studies showing twining defects along the nanowire crystal structure and morphological defects imposed by the templates used have persuaded us to explore alternative nanowire synthesis techniques that can address those shortcomings. To that end, vapor-phase methods for synthesizing nanowires can provide a greater degree of control over nanowire morphology and crystal quality, as well as

control over preferential growth direction. Therefore we have set up a chemical vapor deposition (CVD) system for synthesis of InSb by vapor-liquid-solid (VLS) method.

VLS growth mechanism is most widely employed of all vapor-phase growth techniques, for producing nanowires and of high crystalline quality. It was first proposed by Wagner and Ellis to elucidate the growth of Si nanowhiskers in the early 1960s.[48] VLS growth has been extensively researched throughout the years and has especial gained popularity in the last ten years.[49] In VLS a metal catalyst is often used as a preferential site for deposition of the precursor gas phase, after a liquid alloy forms and transition of the precursor from vapor phase to liquid phase continues super-saturation in the alloy occurs, which leads to precipitation of the precursor in a solid crystal phase.[50] As additional precursor vapor is introduced to the liquid alloy the crystal continues to grow from the substrate, pushing up the alloy droplet. Thus the substrate has a twofold use, it provides a support and temperature control of the metal catalyst particles, but it also determines preferential one directional growth of the solid phase crystal precipitating on the substrate.[20] It has been widely reported that the diameter of catalysts-assisted grown nanowires depends on the size of the liquid alloy droplet, thus strongly related to the size of metal catalysts particles. In this case, a variety of different size Au colloidal particles (10, 30, 60 nm) suspended in a solution (Ted Pella). Au has been commonly used in CVD growth of III-V, Si, and Ge nanowires and as such it is a well developed system. Figure 2.15a shows a phase diagram of Au and InSb, indicating the transition from solid phase to liquid phase as a function of temperature and atomic percentage ratio of Au to InSb. It can be seen that as more of InSb is incorporated with Au the melting

temperature of the resulting alloy decreases. Figure 2.15b depicts the Au catalyst particles deposited over a single crystal InSb substrate, followed by the nucleation and precipitation of InSb crystal, as a result initiating and perpetuating the InSb nanowire growth.

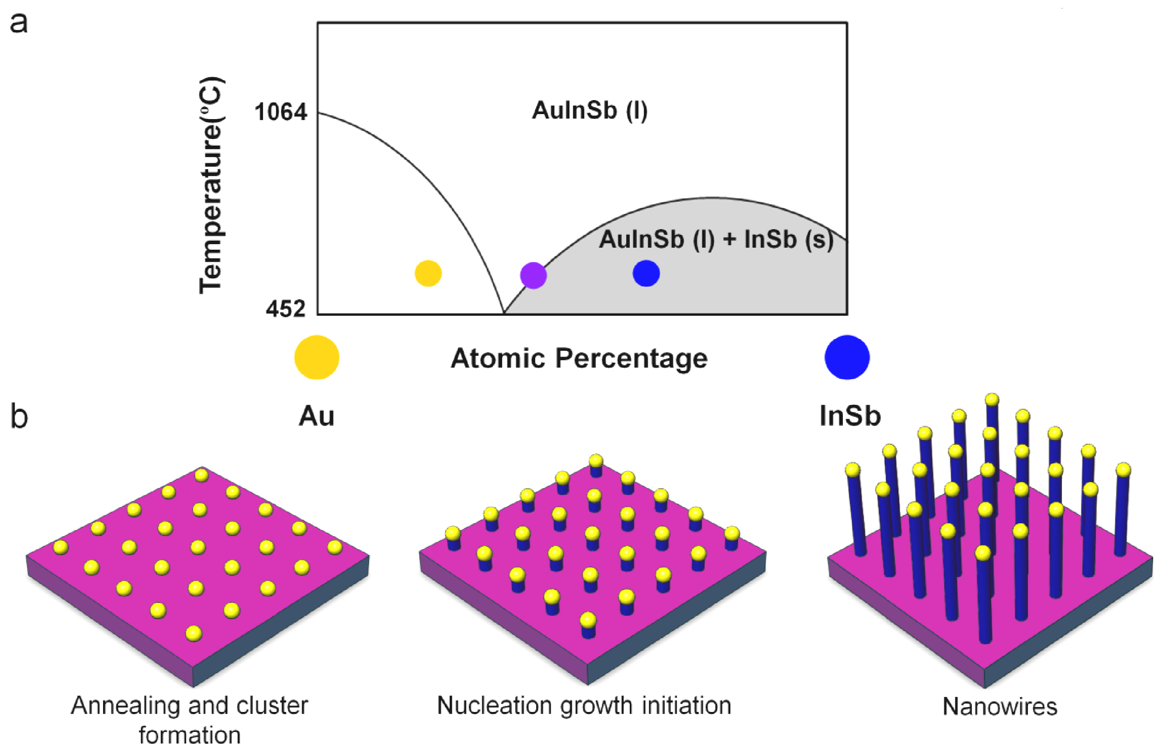

Figure 2.15 a) Phase diagram of Gold-Indium Antimonide alloy. Au catalyst nucleation, supersaturation, precipitation and initiation of nanowire growth.

Figure 2.16 depicts the growth process of InSb nanowires in our CVD system. InSb NWs were grown on InSb (100) substrates inside a vacuumed quartz tube. InSb powder (99.99%) was used as source during growth process. First, the native oxide on the substrate was removed by using chemical etching in hydrochloric acid:water (1:10) solution and dried by argon blowing. Solutions of 20 nm gold colloids were diluted with

isopropyl alcohol to the concentration of 10^4-10^{10} particles/ml which serve as growth catalysts, then deposited uniformly on InSb growth substrate by spin coating. Then the catalyst coated substrates were placed inside the furnace. Upon which, the substrates were annealed at 400 °C for 10 min for catalyst annealing purpose. After that, InSb powder was then placed at the upstream position, 15 cm away from the target substrates in our setup. Hydrogen and Ar gases (1:1) with flow rates of 100 sccm were introduced into the reactor chamber. H_2 serves as the carrier gas and Ar prevents oxidation during the growth process. Furnace temperature was then raised to 550 °C, which was measured at the center of the furnace tube. This translates to source powder temperatures of ~550 °C and growth substrate temperature of 380-450 °C. depending on its position. After 1 hour at this temperature, the furnace was cooled down to room temperature immediately, and the target substrates were taken out.

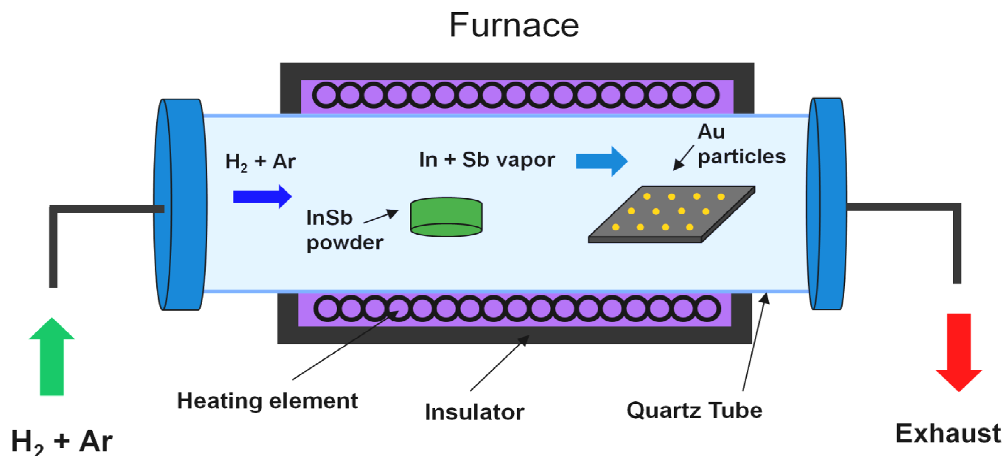

Figure 2.16 Schematic diagram of our in-house CVD set up for synthesis of InSb nanowires.

2.6 Material characterization of InSb nanowires grown by CVD

The detailed morphology of the InSb nanowires was investigated using scanning electron microscopy, and transmission electron microscopy equipped with an X-ray energy-dispersive spectroscopy (EDS) module was used to characterize the crystal structure of the synthesized NWs.[51] Figure 2.17a shows SEM image and b TEM bright field images of the InSb nanowires synthesized at ~420º C. From the scanning electron microscopy image can be observed that InSb nanowires cover the growth substrate with high density. The diameter of the InSb nanowires is in the range of 10-60 nm and their length is approximately 3 μm. The variation of the diameter can be attributed to the Ostwald ripening during the annealing phase, which causes an increase in the diameter of the growth catalyst. Multiple nanowire growth from one catalyst particle is also observed, which is due to multiple nucleation site on a single catalyst particle, as a result the nanowire diameter, in this case is decreased. Figure 2.17b reveals a TEM image of InSb nanowire with a diameter of ~40 nm, the corresponding high resolution transmission electron microscopy (HRTEM) shown in Figure 2.17c reveals that the InSb nanowire has a straight morphology, without any stacking faults, and is covered by and oxide layer 2-3 nm thick. The interplanar d-spacing measured from the fringe pattern, as indicated in Figure 2.17c, was about 0.23 nm corresponding to the {220} planes of InSb crystal system. Figure 2.17d shows the selected area electron diffraction (SAED) pattern, which indicates a single crystalline phase and showed a zinc blend crystal structure having a lattice spacing of 6.47Å the growth direction of <110>.

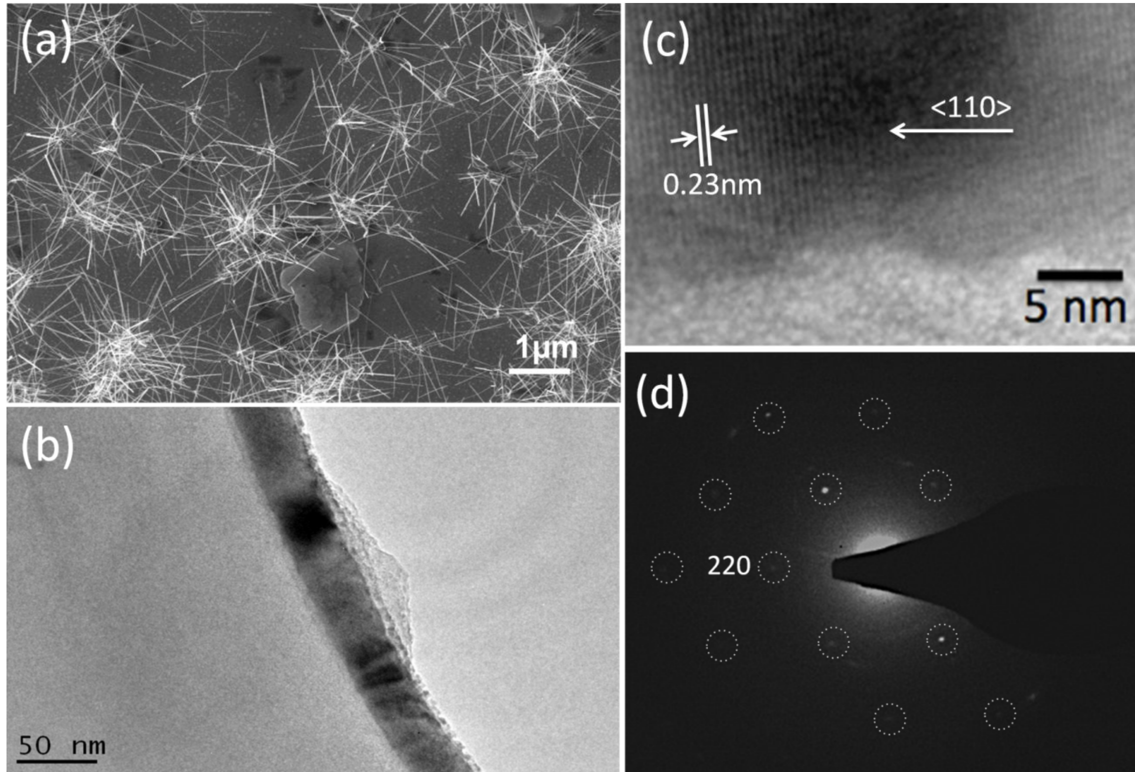

Figure 2.17 a) SEM image of InSb nanowires synthesized by CVD shows diameter ranges from 20 to 50 nm. b) HRTEM image of InSb nanowire. c) HRTEM image showing the growth direction of <110>. d) SAED pattern

Additional TEM analysis performed on a 30nm diameter InSb nanowire is shown in Figure 2.18a a bright-field image of the nanowire, Figures 2.18b and 2.18c show the EDS analyses performed by TEM on two points P and Q along the nanowire shown in Figure 2.18a. The EDS measurements reveal the presence of In and Sb elements, and the atomic percentage ratio is of the two is about 50:50. The presence of Cu and C elements can be attributed to TEM grid used to support the nanowire specimen, while O can indicate presence of oxides on the sample.

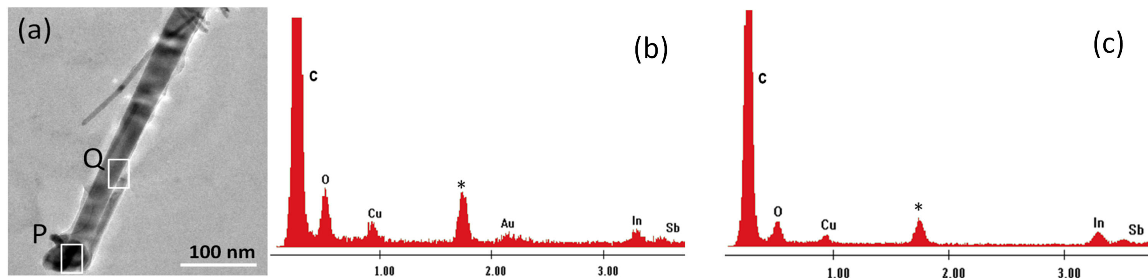

Figure 2.18 a) Bright field TEM image of 30 nm InSb nanowire. b) and c) EDS measurements taken from the points P and Q framed in a), respectively.

The parameters in CVD growth that have an effect on the nanowire structural integrity and morphology are growth temperature, molar flow rate of the precursor gas phase, group III to V ratio, chamber pressure, growth substrate, and growth time. In this work all InSb nanowire growth was carried out in an atmospheric pressure of ~740 Torr. The III-V ratio could not be determined quantitatively, nor controlled experimentally due to the fact that InSb vapor was produced from an InSb powder melt. Therefore, the parameters investigated to determine their effect on nanowire growth were growth temperature, InSb powder amount by weight, and growth time. The experiments revealed that all three parameters affected nanowire morphology and nanowire growth. Increasing the growth temperature, starting at 350 º C, led to increase in axial growth rate of nanowires, due to the enhanced adatoms diffusion mobility. However, increasing growth temperature beyond 450º C led to significant tapering of the nanowires resulting in cone shaped nanowires, due to the migration of Au catalyst and increased radial nanowire growth. The optimal temperature for relatively cylindrical shaped nanowires at maximum growth rate was obtained at 450º C.

The InSb vapor molar flow rate was indirectly controlled by the amount of InSb powder melted at 550º C. Initial increase of the amount of InSb led to increase in the axial nanowire growth rate to about a certain point where an additional amount increase of powder led to increase in the radial growth rate and no change in the axial growth rate. In addition a 2D InSb layer deposited on the growth substrate was also observed. This suggests that an increase flow rate of the InSb vapor leads to vapor-solid-solid growth mechanism, responsible for the direct InSb deposition to sidewalls of the nanowires and the growth substrate. A vapor-solid-solid mechanism resulting in radial growth competing with vapor-liquid-solid mechanism is frequently the cause of cone shaped nanowires. Axial growth, on the other hand, was not affected by a continual increase of InSb vapor since In and Sb atoms direct impingement through the Au catalyst reaches a limit, and so does the adatoms diffusion.

The total growth time affected the final nanowire length as expected, but surprisingly it also affected the nanowire morphology, with longer growth time leading to more tapered InSb nanowires. This can be explained by the migration of Au atoms from the liquid catalyst droplet to the nanowire, resulting in reduction of catalyst droplet size and consequently reduction of nanowire diameter as axial growth progresses, and in addition an increase in the radial growth rate leads to tapering. This effect of growth duration is shown in Figure 2.19, SEM images of InSb nanowire grown for a) 10min, b) 30min, c) 60min, and d) 90min.[52]

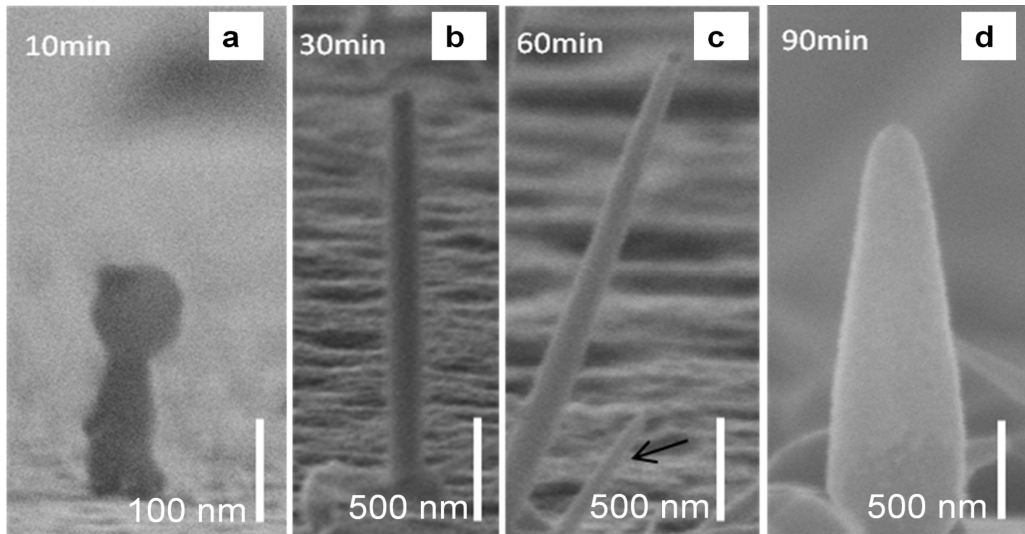

Figure 2.19. SEM images illustrating the morphology InSb NWs after a) 10, b) 30, c) 60, and d) 90 min. The growth temperature was 450°C and 20mg powder source was used.

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Chapter 3

Electrical Characterization of InSb Nanowires

3.1 Device fabrication

The accurate electrical characterization of nanowires and their ultimate implementation in electronic devices necessitates fabrication of metal contacts to semiconductor nanowires with good ohmic behavior and low contact resistance. Contacting nanowires is usually done either by electron beam lithography (EBL) followed by metal deposition,[1, 2] or by direct writing using focused-ion beam (FIB) assisted metal deposition[3].

In addition to microscopy use, SEM instruments are more frequently finding application in micro and nanofabrication, in the form of electron beam lithography. Since it was first demonstrated in 1960[4], it has become a common lithographic technique used to achieve critical features in the order of 5-100nm. In electron beam lithography, in contrast to UV photolithography where UV light is used to expose a photosensitive polymer resists, electron beam is used to expose polymer sensitive to e-beam radiation. The advantage of e-beam lithography also arises from the much shorter wavelength of electrons compared to UV light, resulting in much smaller resolution. Practically any SEM instrument which allows external X-Y movement of electron beam and digital control of stage movement and parameters such as; magnification, focus, aperture, can be converted or used as an e-beam lithography system. The pattern used for lithography can be generated by a CAD software and written by the SEM's e-beam while it is raster scanning over the sample. Beam blanker is used to prevent writing over areas that are not

to be exposed and enable writing over areas that are part of the pattern. A more advanced approach utilizes vector writing, where the beam only scans over the areas that are part of the pattern to be exposed.

Polymethyl methacrylate (PMMA) polymer dissolved in Chlorobenzene or Anisole, is commonly used as a positive tone e-beam resist.[5] It can be spun coat over any substrate of interest at a desirable thickness depending on the spin speed and PMMA concentration and molecular weight. It is then baked in order to evaporate the solvent and harden the resist. When PMMA is exposed by electron beam the polymer undergoes chain scission and the exposed area can be resolved by a solvent such as Methyl Isobutyl Ketone (MIBK) in the developing process. PMMA resist can achieve a resolution of less than 10 nm. The ultimate resolution of the exposed resist depends on several factors such as, the thickness of the resist, the accelerating voltage of electron beam, the beam diameter, the type of substrate on which resist is spun coat. After exposure and developing, PMMA patterns posses a natural undercut geometry, however it may be beneficial to use a co-polymer resist or PMMA of lower molecular weight in conjunction with PMMA to achieve a more pronounced undercut geometry for lift-off applications. The advantage of using a bi-layer of e-beam resists with metal lift-off process can be seen in Figure 3.1, the resulting undercut feature of the bi-layer polymer allows for metal to be deposited on the substrate without being in contact with the polymer, and therefore not be affected during the removal of the polymer with the rest of the resist.

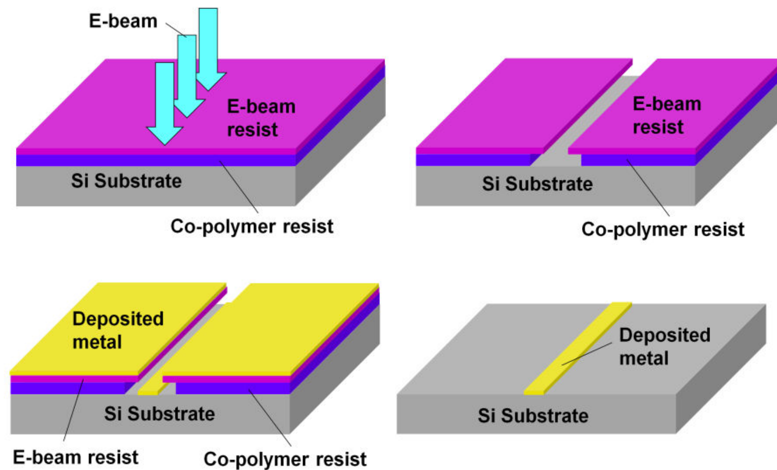

Figure 3.1 Lift-off process by e-beam lithography using a bi-layer resist approach.

All of the SEM imaging and e-beam lithography work was conducted by Carl Zeiss Leo Supra 55. For electron beam lithography nanowire suspended in Isopropyl alcohol (IPA) solution were drop-cast deposited on a heavily doped p-type silicon (p-Si) substrate with insulator oxide layer on the surface. Prior to this step alignment marks and number grid had already been fabricated on the substrate by e-beam lithography and metal deposition and lift-off (Figure 3.2a). After the IPA solution had evaporated, scanning electron microscopy imaging was used to determine the locations of the individual NWs of interest, according to the number grid square as seen in Figure 3.2b. A pattern defining the contacts to be made to individual nanowire was prepared using a CAD software in conjunction with NPGS software. A bi-layer of methyl methacrylate-methacrylic acid (MMA-MAA) and PMMA positive tone electron-beam resists were each spun coat over the nanowire substrate, and then baked one a hot plate at 180 ºC. The spin speed used was from 3100 to 3700 RPM and PMMA concentration was 4% in Anisole, which resulted in roughly 150 nm thickness of PMMA, and 300 nm thickness of

the underlying co-polymer resist. The sample was then loaded in the SEM chamber and the pattern of nanowire contacts was then exposed by the e-beam after the sample was properly aligned using the four corner alignment marks (Figure 3.2a). Important parameters in e-beam lithography exposure are accelerating voltage, beam current determined by aperture size, exposure dose, working distance and optimization of SEM beam by focus, stigmation compensation, and aperture alignment. The highest possible accelerating voltage of 30 kV was used, due to shorter electron wavelength. The aperture sized used for critical dimension features (<100 nm) was 10 µm, which resulted in a beam current of roughly 50 pA. Large aperture sizes of 60 µm and even 120 µm were used for exposing non-critical features, in order to speed up the process. The working distance was fixed to 6 mm, for all exposures. Typical area doses used for exposure were from 250 to 350 $\mu C/cm^2$, while line dose was 3-5 nC/cm. Following the e-beam exposure the sample was developed in MIBK:IPA (1:3) mixture for 75 s and then blow dried. After developing and inspection under optical microscope the sample was exposed to mild oxygen (O_2) plasma to remove any residual polymer resist. The sample was then submerged in ~24% Ammonium Sulfide ($(NH_4)_2S$) solution in order to remove any native oxides and passivate the InSb NW surface. Metal deposition by e-beam evaporation of 40 nm Nickel (Ni) followed by 80 nm Au, was carried out using an e-beam evaporator (Temescal, BJD-1800). A lift-off process was carried out by placing the sample in acetone to dissolve the polymer resist and remove the all of the deposited metal except for the e-bean exposed pattern (Figure 3.1). After lift-off the nanowire contacts are

inspected by SEM, the distance between source and drain contacts is measured, as is the diameter of each individual nanowire.

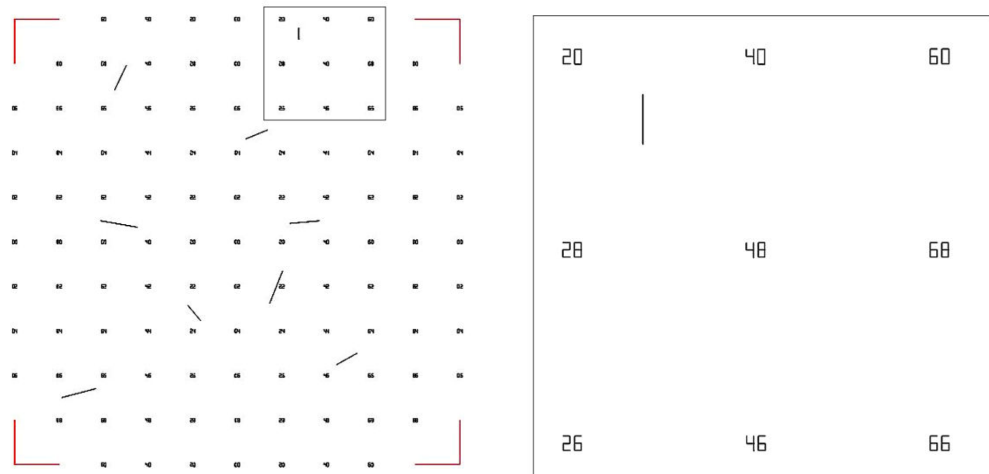

Figure 3.2 Depiction of grid pattern on substrate, used for identifying location of individual nanowires and alignment during pattern writing by electron beam lithography.

3.2 Electrical characterization of InSb nanowires grown by electrochemical deposition

3.2.1 Making ohmic contacts to InSb nanowires

Metal contacts to Indium Antimonide (InSb) nanowires with diameter of 200 nm and 30 nm were made by depositing the nanowires in water solution on a Si/SiO_2 substrate with pre-patterned metal pads. Ohmic contacts between individual nanowire and metal electrodes on substrate were made by Platinum deposition using Focused Ion Beam (FIB) assisted deposition in Carl Zeiss Leo XB1540. The length of the nanowire between contacts for the 200 nm InSb nanowire is approximately 7 μm (Figure 3.3a), while for the 30 nm nanowire it is approximately 1.6 μm (Figure 3.3b).

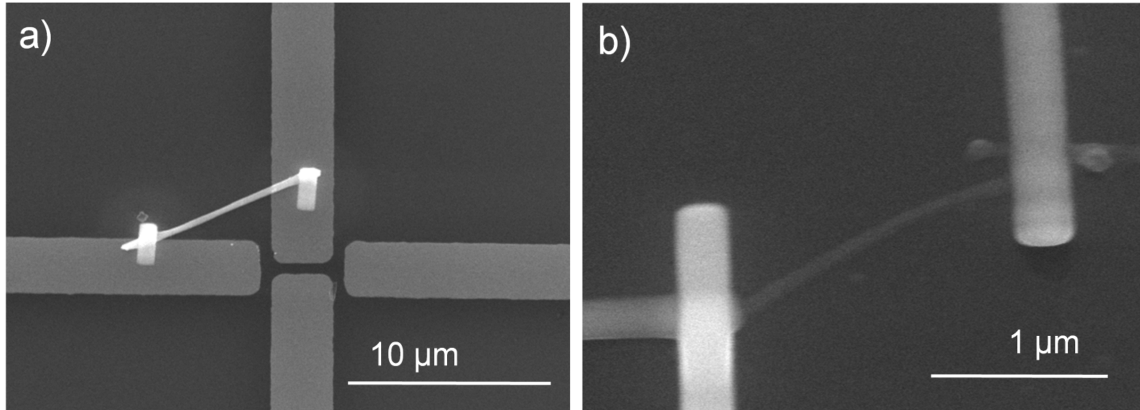

Figure 3.3 Ohmic contacts between individual nanowire and metal electrodes on substrate were made by Platinum deposition using focused ion beam (FIB). a) InSb nanowire with diameter of 200nm. b) InSb NW with diameter of 30 nm.

Figure 3.4a shows the current-voltage (I-V) characteristics of 200 nm diameter InSb nanowire, while Figure 3.4b shows the I-V characteristics of a 30nm diameter InSb nanowire, with metal contacts fabricated through FIB deposition. DC I–V characteristics were obtained at room temperature using Agilent 4155C semiconductor parameter analyzer. The 30 nm InSb nanowires exhibit strong linear I-V behavior indicating ohmic contact, with total resistance for 200 nm nanowire device of 25 MΩ, and resistance for 30 nm InSb nanowire device of 9 MΩ. It can be seen that the smaller diameter nanowire exhibits a conductivity two orders of magnitude larger. This can be attributed to the grain boundaries defects, assuming equal grain size of InSb, the larger nanowire can accommodate bigger number of grains resulting in a larger number of scattering sites for the charge carriers.

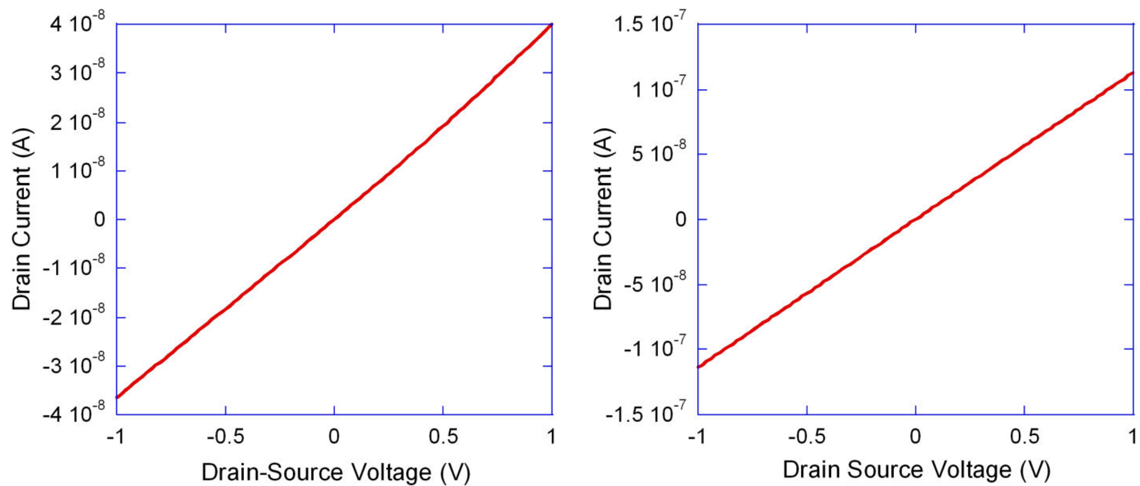

Figure 3.4 a) I-V characteristics of 200nm InSb nanowire at 300K. b) I-V characteristics of 30nm InSb nanowire at room temperature.

Despite the fact that direct Pt deposition by FIB results in ohmic contacts to the InSb nanowires, there have been reports revealing that the irradiation of Ga^+ ions present in FIB assisted metal deposition causes amorphization and other disorders in semiconductor nanowires under the metal contacts.[6, 7] These defects induced by FIB become more significant especially for nanowires with smaller diameter as in the case on 30 nm diameter InSb nanowires. Some evidence, observed on nanowire sample shown in Figure 3.5, suggests that during metal deposition by FIB a residual Pt metal layer is deposited in the near vicinity of the nanowire contacts. This can affect the actual I-V measurements and can have an increasingly significant effect on the obtained nanowire resistance as the distance between contacts is decreased.

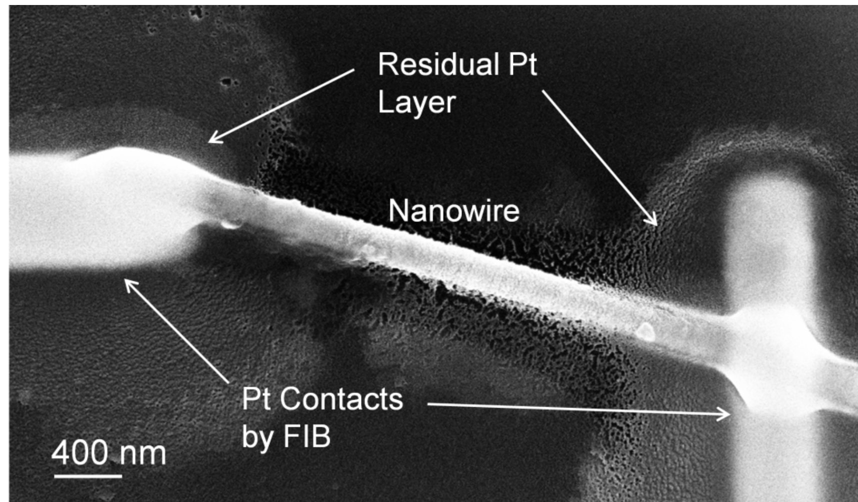

Figure 3.5 SEM image of nanowire contacts fabricated by FIB assisted Pt deposition reveal residual Pt layer around the contacts.

For reasons mentioned above, we concluded that FIB is not an ideal approach to nanowire device fabrication. Therefore all further nanowire device fabrication was conducted by electron beam lithography and lift-off process, which was described in detail in the previous section.

Here we present the electrical performance of InSb nanowires with Ti/Au metal contacts deposited by electron beam metal evaporation. Using metal-semicondcutor-metal model where two Schottky barriers in series form, the potential barriers at these junctions are evaluated using temperature dependent current on the basis of thermionic emission theory. Effects of rapid thermal annealing of the device are also discussed.

First, InSb nanowires with an average diameter of 70 nm (Figure 3.6a) were fabricated by a template assisted electrochemical deposition, described in Section 2.3. Metal contacts to individual InSb nanowires (Figure 3.6b) were fabricated using electron-

beam lithography and metal deposition by electron-beam evaporation of 10 nm thick Ti and 100 nm thick Au (Details in Section 3.1). Temperature dependant I-V measurements were obtained using Agilent 4155C Semiconductor Parameter Analyzer, while sample temperature was varied between 75-300 K, with increments of 25 K in an MMR variable temperature system. Following the measurements, samples were annealed by rapid thermal annealing at 350°C for 30s under Nitrogen ambient. I-V measurements were recorded at the same temperature conditions.

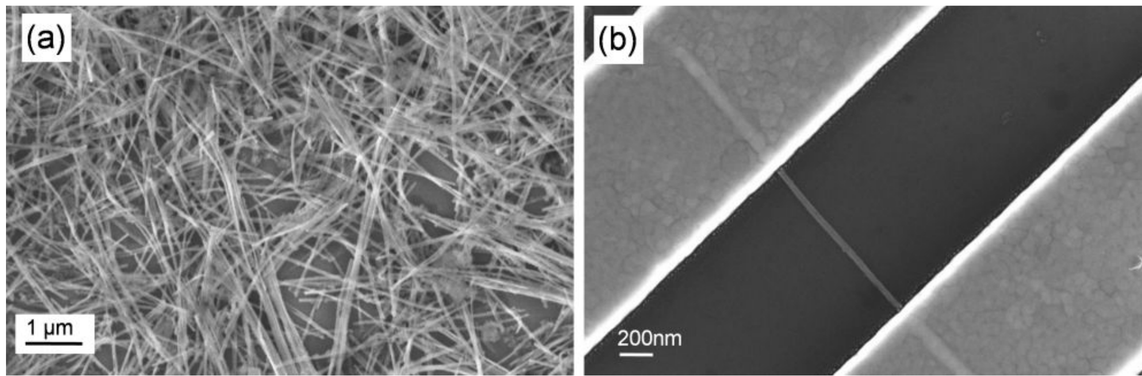

Figure 3.6 a) SEM image of metal contacts to a single InSb nanowire (70 nm diameter) fabricated by electron beam lithography. b) I-V characteristics from two-probe measurements of InSb nanowires with temperature varied from 75 K to 300 K.

Temperature dependant I-V characteristics of InSb nanowire (Figure 3.7a) reveal rectifying behavior for all temperatures, which is due to the formation of a Schottky barrier at the metal/semiconductor interface.[8] The metal-nanowire-metal (M-S-M) structure can be modeled as two back-to-back Schottky diodes in series with the nanowire, as shown in Figure 3.8a.[9] Based on this model, the conduction current through the device is limited by the reversed biased diode which explains the symmetrical I-V curves measured under bias sweep from -1V to 1V. Figure 3.8b shows

the band diagram of the metal-p-type semiconductor-metal structure under applied voltage bias, where E_{FS} and E_{FD} are the Fermi levels of the metal at the source and drain contacts, E_F is the Fermi level of the p-type semiconductor, E_C and E_V are the conduction and valence band of the semiconductor, and φ_{bS} and φ_{bD} are the Schottky barriers formed at the source and drain contacts. It can be seen that the Schottky barriers at both ends have equal height and are independent of the applied bias; therefore under applied bias the current is limited by the metal/semiconductor junction in reverse bias.

The current of a Schottky diode can be determined based on thermionic emission model[10] and is given by

$$I = I_S\left[\exp\left(\frac{qV}{k_B T}\right) - 1\right]$$

where I_s is the saturation or reversed biased current in the diode , T is temperature, q is the charge of electron, and k_B is Boltzmann's constant. The saturation current is given by

$$I_S = AA^{**}T^2 \exp\left(\frac{-q\phi_b}{k_B T}\right)$$

where A is the contact area, A^{**} is the effective Richardson's constant, and φ_b is the Schottky barrier height. Using the latter equation the barrier height can be obtained from the slope of a linear plot of $\ln(I/T^2)$ vs $1/T$, shown in Figure 3.7b, in which we observed negative slope, constant at low bias voltages which is in agreement with thermionic emission model and existence of a positive Schottky barrier. The average barrier height obtained at low bias was φ_b = 17 meV. We must note that this analysis based on two

point-probe measurements that is valid only if the contribution of nanowire resistance is negligible compared to the contact resistance. In a separate study of these InSb nanowires,[11] we determined mobility and carrier concentration based on FET measurements. The InSb nanowires show p-type behavior with hole concentration N_A = 1.5×10^{17} cm^{-3} at room temperature. Based on this result, we assumed that the nanowire resistance is much lower than the total device resistance.

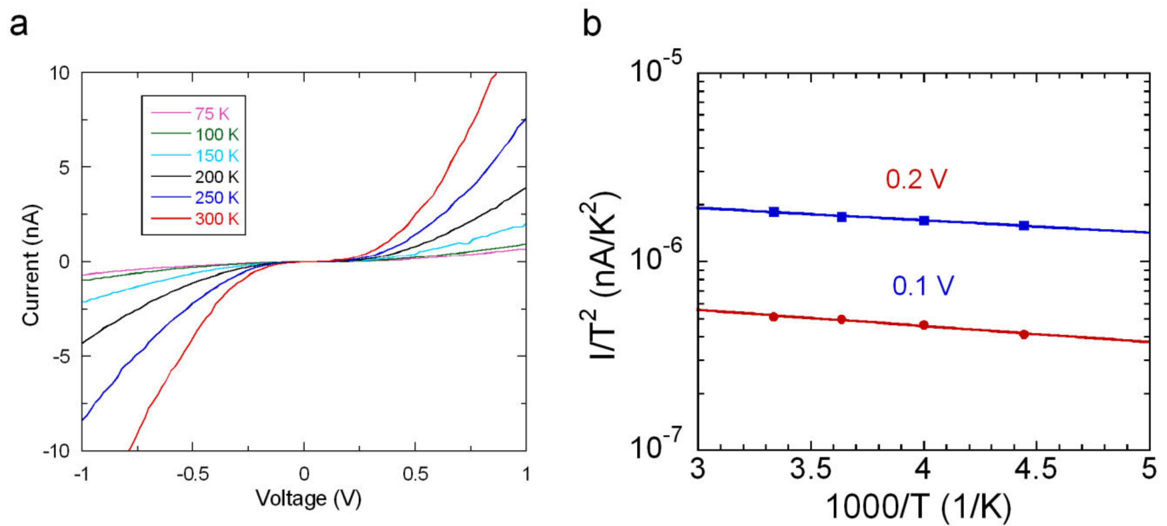

Figure 3.7 a) I-V characteristics from two-probe measurements of InSb nanowires with temperature varied from 75 K to 300 K. b) A plot of ln(I/T^2) vs $1/T$ at low bias voltage.

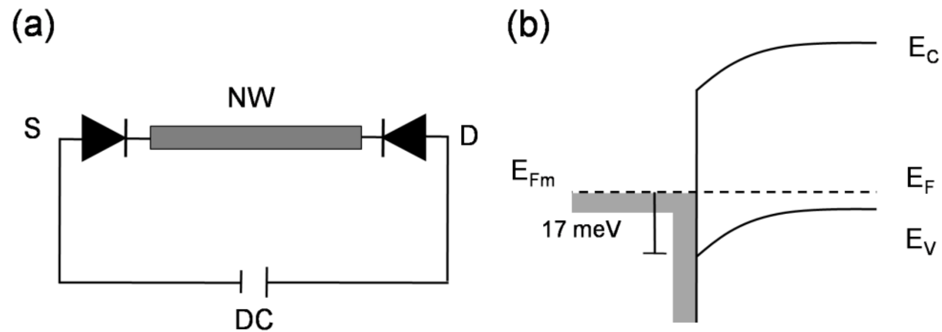

Figure 3.8 a) Schematic of the M-S-M back-to-back Schottky barrier model, with diodes depicting the Schottky barriers formed at the metal/semiconductor interface at source and drain. b) Band diagram of semiconductor nanowire-metal contact.

Temperature dependant *I-V* measurements of InSb nanowire obtained subsequent to rapid thermal annealing Figure 3.9 show linear characteristics throughout the entire temperature range, implying a zero Schottky barrier height. The formation of ohmic contacts can be attributed to the diffusion of Au in the InSb nanowire during the thermal annealing, which acts as a local dopant in the vicinity of the nanowire-metal interface. It has been demonstrated that Au can migrate in InSb during annealing at temperatures in the range from 200 to 300˚ C.[12] Furthermore, the lowering of contact resistance could be assisted by the increase in contact area between the metal contacts and InSb nanowire, due to possible roughening of the metal-semiconductor interface during the thermal annealing process. [13, 14]

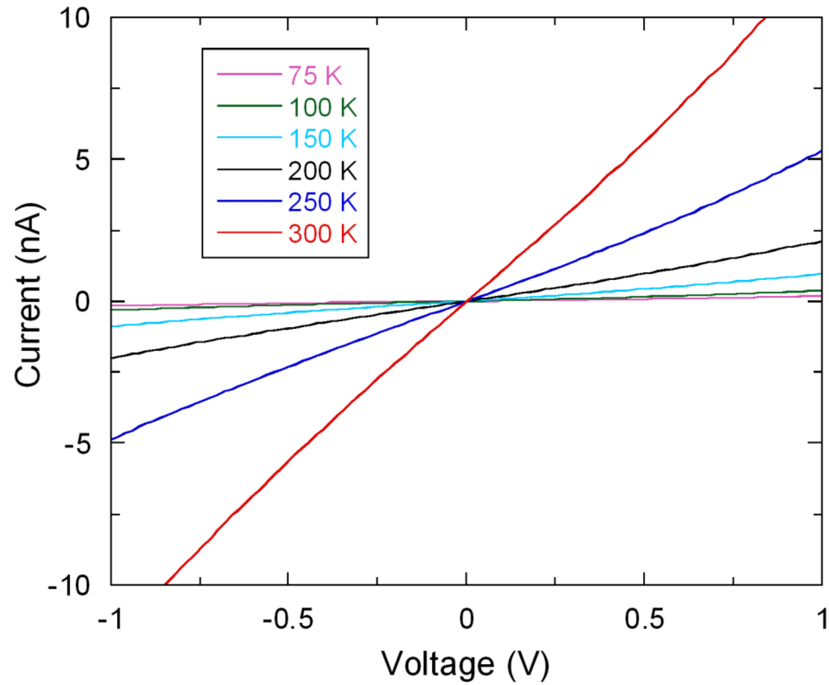

Figure 3.9 *I-V* characteristics from two-probe measurements of InSb nanowires, recorded after rapid thermal annealing, with temperature ranging from 75 K to 300 K.

3.2.2 Electrical characterization of InSb nanowires by conductive atomic force microscopy

Atomic force microscopy (AFM) is type of imaging technique, which belongs to the group of scanning probe microscopy (SPM). The latter name derives from the fact that in this group of imaging techniques, a small probe is employed to raster scan the sample surface, measuring the relief and creating a 3D image of the surface with a very high resolution. Atomic force microscopy was developed in 1985 by Gerd Binning and his team at IBM Zurich Research Laboratory [15], after they had already developed

scanning tunneling microscopy (STM) in 1981[16]. AFM functions on a similar principle of STM, by raster scanning a tiny probe tip over the sample surface, while continuously adjusting the height of tip to keep the distance between the sample and tip constant and recording the movement of the tip to recreate a depiction of the sample surface. While in STM the signal recorded and used to determine the distance between sample and probe tip was tunneling current, in AFM that entity was atomic force between the probe tip and the atoms on the sample surface.[17] This means that AFM can be used to image non conductive samples at the same atomic resolution of STM. In addition to imaging non conductive samples AFM has been used for imaging soft samples, biological samples and samples in liquid.[18-20] Moreover, AFM has been used to measure nanomechanical and elastic properties of various materials[21-23], as well as magnetic forces, electrostatic forces and chemical forces[24-26]. AFM has also been employed as a tool for nanofabrication in AFM lithography, nanoindentation, and "dip-pen" lithography.[27-29]

When the distance between the AFM probe tip and the sample is less than ~1nm the probe tip is experiencing repulsion atomic forces due to electronic orbital overlap with the atoms of the sample surface, these forces are used in hard contact AFM mode. In this mode of operation the deflection of the AFM cantilever due to the repulsive forces from the interaction with the sample is used to measure the surface profile. Contact mode AFM can be used to achieve atomic resolution imaging on many different types of samples, however one drawback is the frictional force applied by the AFM probe tip on the sample, which can damage the sample, or in some cases the tip. Attractive forces responsible for the probe tip tracking are due to water vapor molecules adsorbed on the

sample's surface forming a meniscus layer, or electrostatic forces on the sample surface. One approach to avoid the capillary forces due to the water layer on the sample surface is to immerse sample and AFM cantilever in liquid, this can be advantageous for some samples like biological samples, but is not applicable to all types of samples. Another approach to overcome the problem of probe traction and sticky probe tip is the noncontact mode of AFM operation. When the distance between tip and sample is about few nanometers, the tip is experiencing attractive atomic forces mainly van der Waals forces. These attractive forces are used in dynamic (non-contact) mode of operation of AFM, where the probe tip is held at a distance few nanometers and is oscillated at frequency near its resonant frequency. Non contact mode AFM can be carried out in either frequency modulation, where the change in oscillating frequency of the cantilever, due to the interaction forces with the sample is measured, or in amplitude modulation mode in which the change in amplitude of oscillating cantilever and the change in phase are recorded.

Tapping mode is a form of non contact operational mode, in which an AFM cantilever is oscillated over the sample surface at its resonant frequency, and it comes into intermittent contact with the surface at its lowest point of oscillation. This gentle tap on the sample surface is responsible the high imaging resolution achieved by taping mode, while the high frequency of probe oscillation prevents the tip from sticking to the sample surface or damaging the sample. Tapping mode can be used on soft or sensitive samples without damaging them, while achieving very high resolution. In addition it is

not affected by attractive forces or adhesion due to water meniscus or electrostatic forces on the sample surface.

Figure 3.10 depicts basic setup and components of an atomic force microscope. The AFM cantilever is one of the main components of the system, it is usually fabricated out of Si or SiN using conventional microfabrication techniques, at the base of the cantilever is the pyramid shaped tip, the tip apex radius is critical for the ultimate resolution of AFM image. The specimen to be imaged is placed on a tube scanner made out of piezoelectric material. The lower tube is split in four, and is used to raster scan the sample in X-Y direction, while the upper part of the tube is used to move the sample up and down in Z direction, in order to keep the force interaction between the probe tip and specimen constant. The deflection of the AFM cantilever (contact mode), and the change in oscillation frequency, amplitude and phase (tapping mode) is detected by a laser beam reflected from the cantilever and directed by a mirror to a split photodiode detector. The signal from the photodiode is converted to an AC signal and is then amplified, this signal is used to interpret the change in height of the sample and is combined with the signal from a raster scan generator, scanning the sample in X-Y direction, to produce and display a three dimensional map of the sample surface. In addition to this, the amplified signal from the photodiode is continuously fed back to the controller, responsible for moving the sample in Z direction.

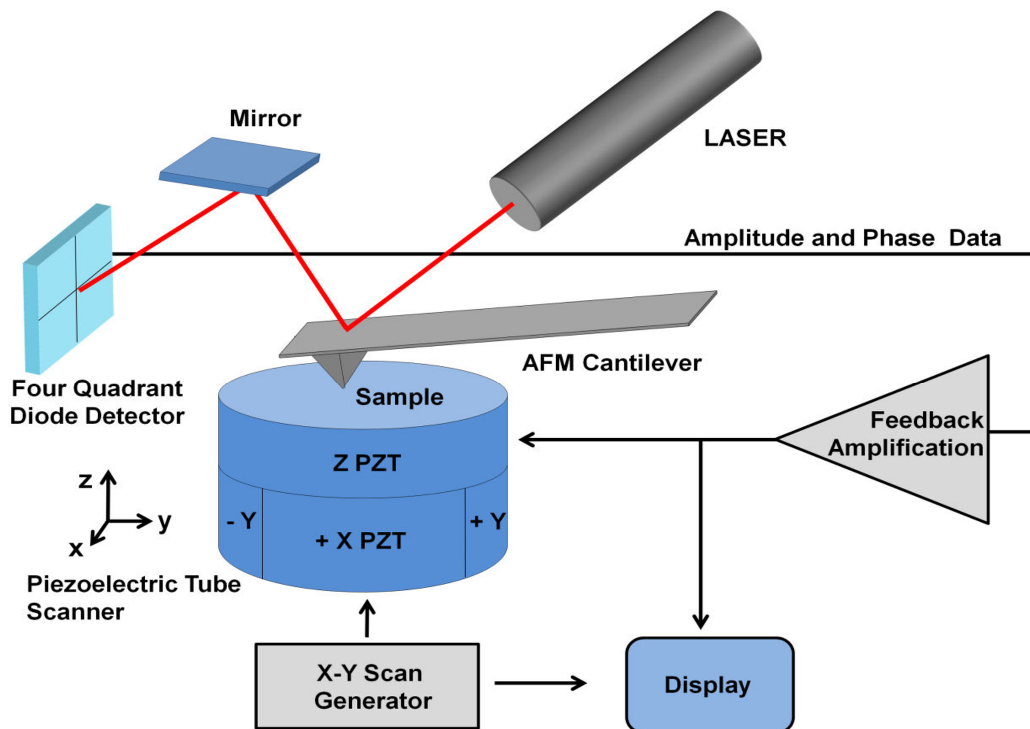

Figure 3.10 Atomic force microscopy instrumentation setup.

Conductive atomic force microscopy (CAFM) is a mode of AFM that can obtain electrical probe measurements while the AFM probe is raster scanned over the sample.[30] In CAFM a conductive probe is used to apply voltage potential between tip and the sample, while measuring the current through the tip. CAFM is carried out in contact mode AFM, since the conductive tip is in hard contact with the sample. CAFM is capable of conducting simultaneous electrical measurements on the sample together with obtaining a topographical image of the sample, thus creating a current map revealing the electrical properties of the sample across its entirety. As such CAFM is employed as a scanning probe technique for nanoscale electrical characterization, due to its high lateral and vertical resolution.[31, 32] Two terminal resistance measurements on InAs nanowires

have been performed using a conductive AFM probe as a mobile local contact along the nanowire axis, thus effectively controlling the distance between the two contacts.[33, 34]

The tunneling atomic force microscopy (TUNA) module, employed in this work, together with Veeco Multimode AFM allows current-voltage measurements of sub-pA current sensitivity and a lateral resolution of less than 10 nm. Figure 3.11a shows a schematic of CAFM I-V measurement using the AFM probe as a scanning local electrode on the InSb nanowire, while applying a DC bias between a fixed metal contact and the conductive AFM probe. Figure 3.11b reveals a topographic image, obtained by CAFM, of InSb nanowire with metal contact electrodes.

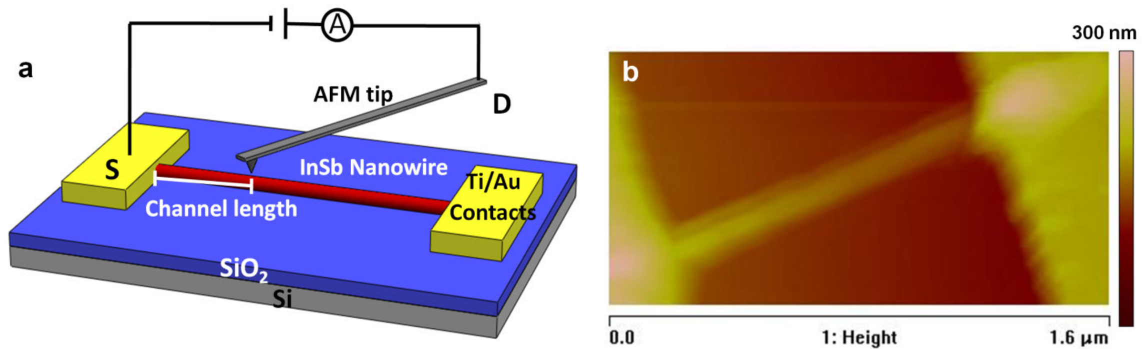

Figure 3.11 a) Schematic of conductive AFM tip used as an adjustable mobile probe. b) Topographic image of InSb nanowire obtained by conductive AFM tip.

Figure 3.12a show and AFM image of a 200 nm diameter InSb nanowire, with a single metal contact (Ti/Au) fabricated by e-beam lithography. Figure 3.12b shows the corresponding TUNA current map obtained by the conductive Pt/Ir coated AFM probe tip. The current color scale is shown on the right adjacent to the current map image with the maximum value being 2.5 µA. The parallel white doted lines indicate the outline of the nanowire transferred from the AFM height image in Figure 3.12a. The AFM current

map reveals that the nanowire resistance measured between the electrode and the AFM probe is approximately constant to a distance of about 150 nm from the metal contact. Resistance gradually decreases to ~500 nm from the electrode and becomes practically non-detectable thereafter.

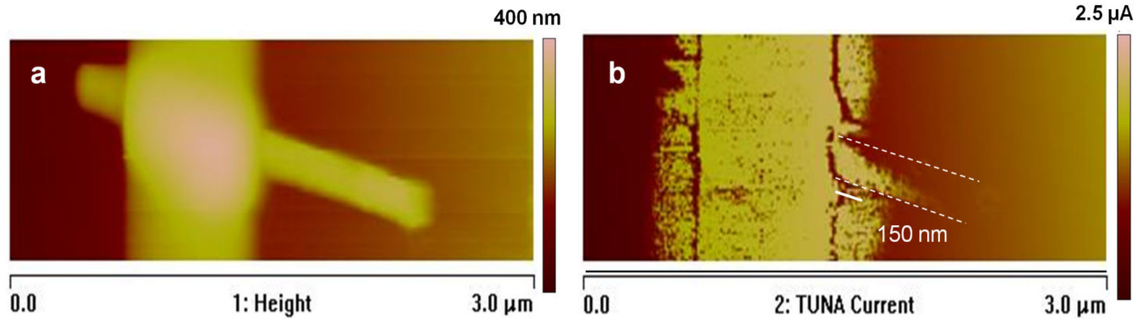

Figure 3.12 a) AFM height measurement of an InSb nanowire and metal contact. b) Corresponding current map measurement obtained by conductive AFM tip.

Besides using CAFM probe tip as a local contact, it was also used as a floating gate electrode on a nanowire field effect transistor. Scanning gate AFM was employed to study the transfer characteristics of single composition modulated $In_{1-x}Sb_x$ nanowire field effect transistor devices. A conductive AFM probe was used as a local mobile gate electrode[35] to induce a local change of the electron or hole density as a method to modulate the free carrier concentration in the nanowire device channel. Since the diameter of nanowires used here is about 100nm, the nanowire device sensitivity to local gating can be significant as a small gated region of the nanowires can effectively limit the total conductance through the nanowire device.[36]

Nanowires synthesized by electrochemical deposition with In and Sb composition effectively modulated to $In_{0.5}Sb_{0.5}$ and $In_{0.3}Sb_{0.7}$ (Chapter 2), were used to fabricate the field effect transistor devices. Source-drain contacts to the nanowires were fabricated

through e-beam lithography. The resulting nanowire devices were covered by a 20 nm film of Al_2O_3 deposited by atomic layer deposition. Source and drain contacts of the nanowire FET were connected to a semiconductor parameter analyzer, while a Pt/Ir coated AFM probe tip, was used as a local gate electrode over the nanowire channel covered by the alumina dielectric layer.

Figure 13.3a shows a schematic depicting the $In_{1-x}Sb_x$ nanowire device with source and drain contact and the conductive AFM probe as a scanning local gate electrode. Figure 13.3b displays a topographical AFM image of a single $In_{1-x}Sb_x$ nanowire FET. Figure 13.3c shows the I_D-V_{DS} I-V characteristics of n-type ($In_{0.5}Sb_{0.5}$) nanowire FET for various constant voltages applied by the AFM tip in the middle of the nanowire channel. Figure 13.3d shows the the I_D-V_{DS} I-V characteristics of a p-type ($In_{0.3}Sb_{0.7}$) nanowire devices different V_{GS} values. Both graphs indicate that the I-V characteristics of $In_{0.5}Sb_{0.5}$ and $In_{0.3}Sb_{0.7}$ nanowire devices exhibit a significant current modulation due to the gate voltage applied by AFM probe. In the case of the $In_{0.5}Sb_{0.5}$ nanowire device (Figure 13.3c), when V_{GS} is biased from 0V to 9V, drain current I_D increases for increasingly positive values of V_{GS}. In contrast, the $In_{0.3}Sb_{0.7}$ nanowire device (Figure 13.3d) shows an increase in drain current I_D as increasingly negative V_{GS} values are applied to the nanowire.

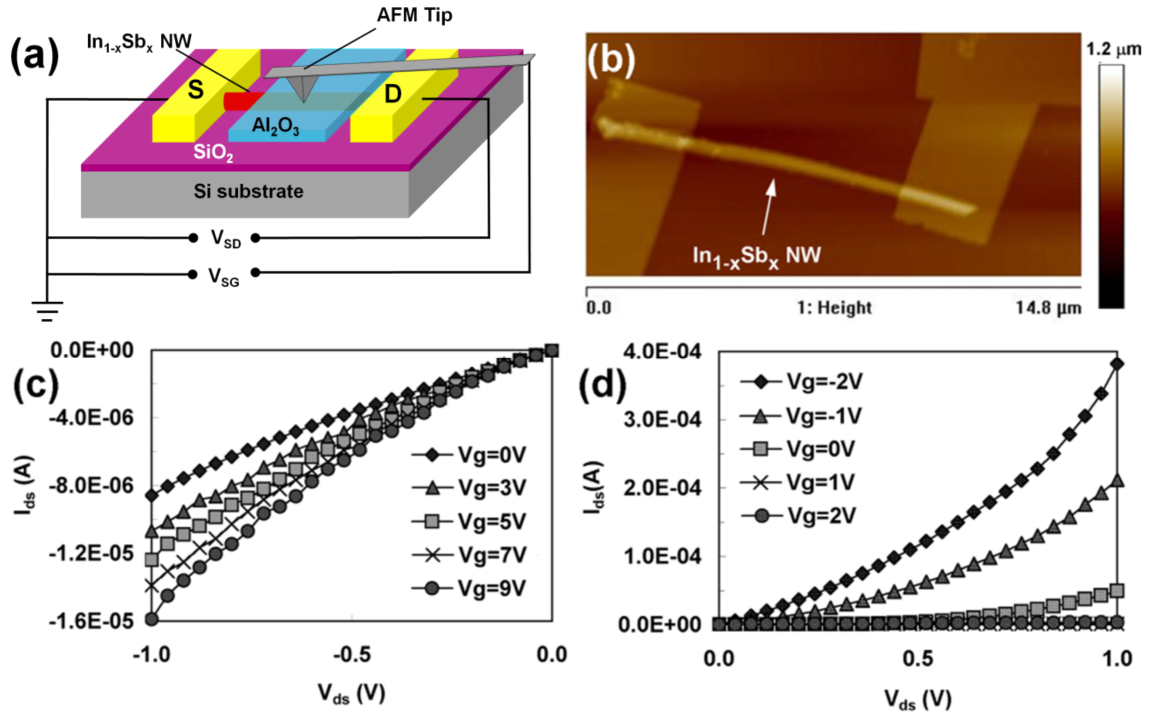

Figure 3.13 a) Schematic of the SGM setup for characterization of $In_{1-x}Sb_x$ NWFET. b) AFM height image of an $In_{1-x}Sb_x$ NW FET device characterized in this study. c) and d) I_{ds}-V_{ds} characteristic curves as a function of V_g for $In_{0.5}Sb_{0.5}$ and $In_{0.3}Sb_{0.7}$ NW- FET devices respectively.

The observed conductance modulation can be explained in terms of a tip-induced local energy band bending.[37] Since the conductive AFM probe has a radius of curvature of ~30nm, its localized electrostatic potential has a pronounced effect on the electronic structures on the composition modulated $In_{1-x}Sb_x$ NWs. It is known that band structure modulation by a local electrostatic potential could significantly alter the transport characteristics of quasi one-dimensional nanosystems.[35, 38]

3.3 Electrical characterization of InSb nanowires grown by chemical vapor deposition

3.3.1 InSb nanowire contact resistance and field effect transistors measurements

InSb nanowire field effect transistors were fabricated by making ohmic contacts to InSb nanowires by e-beam lithography as explained in detail in Section 3.1. Figure 3.14 depicts the back gate nanowire FET configuration (left-hand side), where InSb nanowires are deposited on the heavily doped Si p+ serving as the back gate, with thermally grown SiO_2 used as the gate dielectric. Top gated nanowire FET (Figure 3.14 right), requires few additional steps; after the source and drain contacts to the InSb nanowire have been fabricated, a high-k dielectric (HfO_2) is deposited over the nanowire by atomic layer deposition (ALD), followed by fabrication of the metal gate by e-beam lithography and metal deposition by e-beam evaporation.

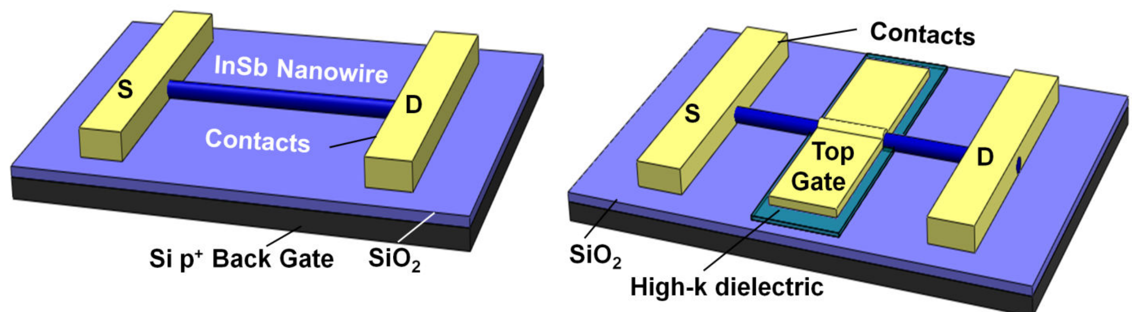

Figure 3.14 Schematic representation of back gated nanowire field effect transistor device (left-hand side). On the right a depiction of a top gated nanowire FET device employing a high-k dielectric.

InSb nanowire FET device (including back-gate and top-gated design) can be treated as a depletion mode MOSFET (metal oxide semiconductor field effect transistor), which is normally ON (current flows between drain and source of an applied bias between the two terminals) at zero gate voltage, in order for the device to be turned off a gate voltage potential is applied to deplete the transistor channel out of free charge carriers. Figure 3.15a displays the transfer characteristic (I_{DS} vs V_{GS}) of the n-type depletion mode InSb nanowires FET, shown by the black curve.

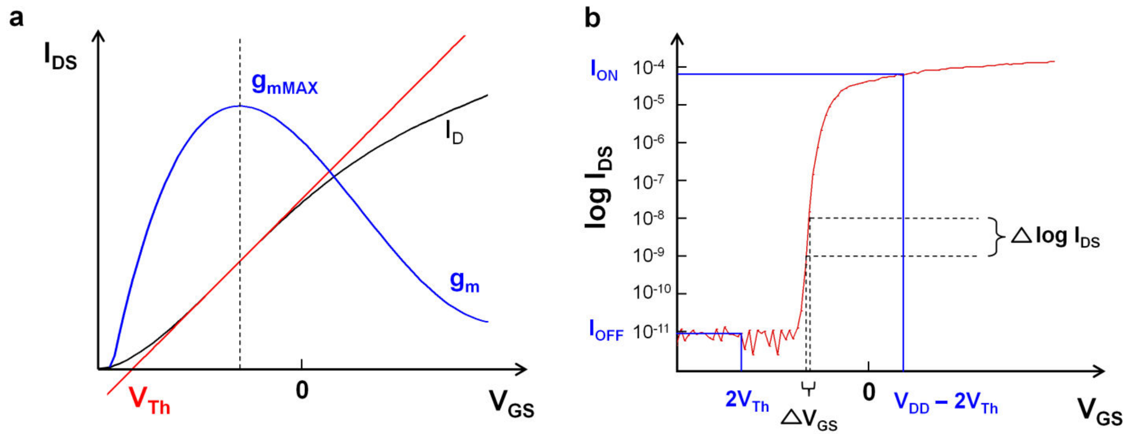

Figure 3.15 a) Transfer characteristics of depletion mode n-type nanowire FET. b) Transfer characteristics in LOG scale, used to extract I_{on}/I_{off} ratio and subthreshold slope.

The transconductance g_m (blue curve) is determined by the derivative of the drain current and is given by

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} .$$

The threshold voltage, necessary to invert the channel and switch the FET OFF can be determined by finding the gate voltage value V_{GS} for which the transconductance g_m has

a maximum value, then drawing a tangent line to the transfer characteristics curve at that point, the point at which the line intersects the x-axis is the threshold voltage (Figure 3.15). This holds true if the device operates in the linear region of operation, in other words for small values of applied bias voltage V_{DS}.

The transconductance value can used to determine the field effect mobility of charge carriers in the nanowire channel, and is given by the following relation

$$\mu = g_m \frac{L^2_{eff}}{C_{OX} V_{DS}}$$

where μ is the carrier mobility, L is the channel length, C the gate capacitance, I_{DS} the source-drain, and V_{GS} the gate-source voltage.[39] The capacitance for back gate NWFET can be modeled as cylinder on an infinite plate and can be expressed as

$$C_{OX} = \frac{2\pi\varepsilon_0\varepsilon_r L_{eff}}{\ln\left(\frac{2d_{OX}}{r_{NW}}\right)}$$

where $\varepsilon_r\varepsilon_0$ is dielectric constant, t is the thickness of the SiO_2 dielectric, L the channel length, and r is radius of nanowire. The use of “cylinder on plate” model for estimating the gate oxide capacitance of a back-gated nanowire FET is commonly used in literature. However, since the nanowire is not embedded in the oxide, instead it is deposited on the oxide, this model overestimates the capacitance, therefore an effective dielectric constant ε_r of 2.2 is used here, since it has been shown to be an accurate estimation compared to

the modeled capacitance data, if the ratio of oxide thickness to nanowire radius falls between 6 to 100. [40]

The right-hand side of Figure 3.15 shows the transfer characteristics of a nanowire FET plotted in a logarithmic scale for the y-axis of the drain current I_{DS}. This graph reveals two important parameters characterizing the nanowire transistor device performance. The first one is I_{on}/I_{off} ratio, determined by the maximum and minimum drain current I_{DS} value within the allowed range by the supply voltage V_{DD}. A high I_{on}/I_{off} ratio is desirable with a small I_{off} value to minimize off-state leakage current and dissipated power, while high I_{on} is desired in order to increase device drivability and is critical in high speed transistors. The other important figure of merit of device performance, which can be extracted from the same graph, is the subthreshold slope, which is defined as the change in gate voltage V_{GS} necessary to change the drain current 10 times (measured as volts/decade). This determines how fast a device can be switched from ON state to OFF state and vice versa. The subthreshold slope SS is given by the following equation

$$SS = \frac{\partial V_{GS}}{\partial(\log(I_{DS}))}$$

Almost all nanowire device are currently fabricated, by electron beam lithography or photolithography followed by the deposition of metal electrodes as the source and drain contacts. However, the inability to degenerately dope the nanowire sections where metal source and drain contacts are made, often results in the existence of positive Schottky barriers at the metal-semiconductors interface, as it was demonstrated earlier. In

the case of non-rectifying Schottky barriers (ohmic contacts), even where I-V characteristics exhibit linear behavior, the contact resistance can be significant in some cases and can greatly influence nanowire FET performance. Nanowire contact resistance is not negligible especially in the case of nanowires in the 10 nm diameter range, due to small contact surface area.

Various experimental methods and models have been employed to accurately determine the resistance between metal contacts and semiconductor nanowires.[41-44] A straight forward method to achieve that goal is the four-point probe measurement, depicted in the schematic diagram of Figure 3.16. It can be seen that the intrinsic nanowire sample resistance Rs, can be accurately determined. In the two-point probe configuration, the measured resistance is the sum of nanowire resistance plus the two contact resistances, subtracting the nanowire resistance measured from the four-four probe measurement, we can determine the sum of the two contact resistances.[45] Here we have assumed that the two metal contacts are (almost) symmetric, because they were fabricated simultaneously under the same conditions on the same nanowire.

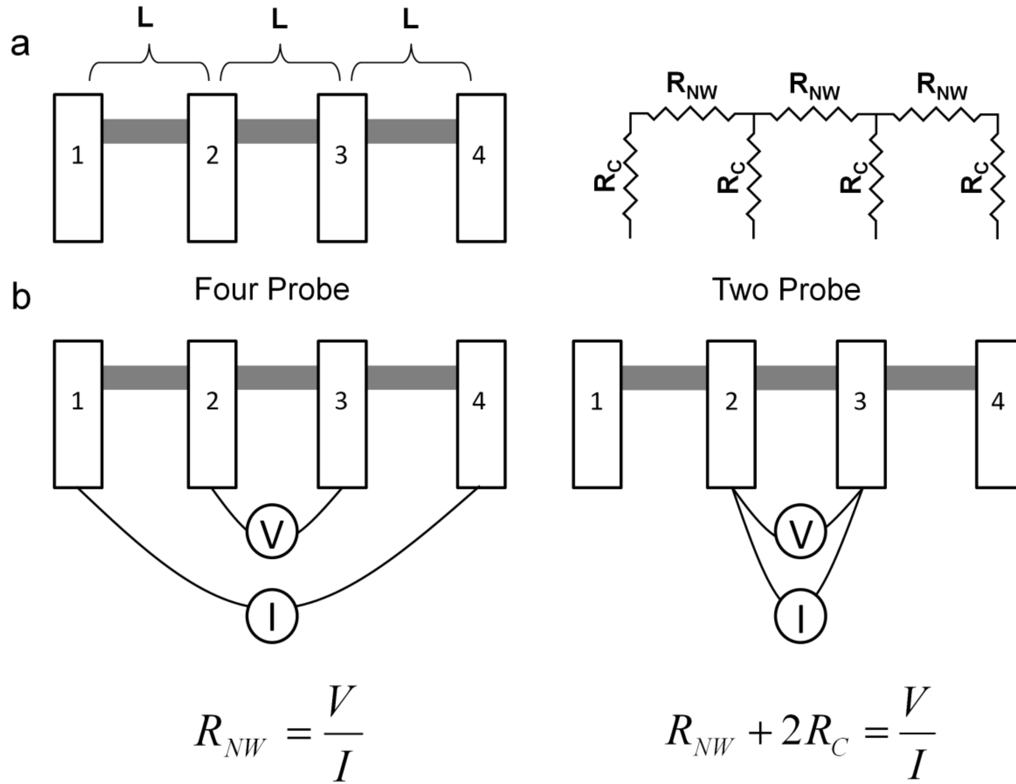

Figure 3.16 a) Schematic diagram for a single nanowire with four electronic contacts and the equivalent circuit model showing the corresponding contact resistance. b) Four-point probe measurement configuration two-probe measurement configuration.

The effect of contact resistance at the drain and source contacts, on the nanowire FET transconductance is given by the following equation:

$$g_{ex} = \frac{g_{in}}{1 + g_{in}R_s + \frac{(R_s + R_d)}{R_{in}}}$$

where g_{ex} is the measured transconductance, g_{in} is the intrinsic nanowire transconductance, R_s is the contact resistance at the source, R_d is the contact resistance at

the drain, R_{in} is the intrinsic nanowire channel resistance.[46] Furthermore, the calculated values of carrier mobility of nanowire FET are often underestimated not only due to the effect of contact resistance on transconductance but also because of the voltage drop across source to drain due to contact resistance. Therefore Equation 1, used to determine carrier mobility must be modified to:

$$\mu = g_{in} \frac{L^2{}_{eff}}{C_{OX} V'_{DS}}$$

$$V'_{DS} = V_{DS} - 2(I_D \cdot R_C)$$

V'_{DS} is used to account for the loss due to the contact resistance. To accurately characterize the performance of InSb nanowire FETs, the contact resistance was first determined by four-point probe measurement.

Four metal contacts to InSb nanowires were fabricated using electron-beam lithography to define the contact areas. Metal deposition by e-beam evaporation of 40 nm nickel (Ni) followed by 80 nm Au, was carried out using an e-beam evaporator. The relatively small size of Ni metal grains allows for the fabrication of good ohmic contacts to NWs having sub-20 nm diameters.[47] The average separation between metal electrodes was 500 nm, while the typical NW diameter was 10-20 nm. Figure 3.17a shows the four metal contacts to InSb nanowire of 17 nm diameter, while Figure 3.17b is a graph of the four-point-probe voltage current measurements. The blue I-V curve indicates the voltage applied at the outer two probes versus the current measured through

the nanowire, while the green curve indicates the voltage drop across the two probes in the middle versus the current through the nanowire.

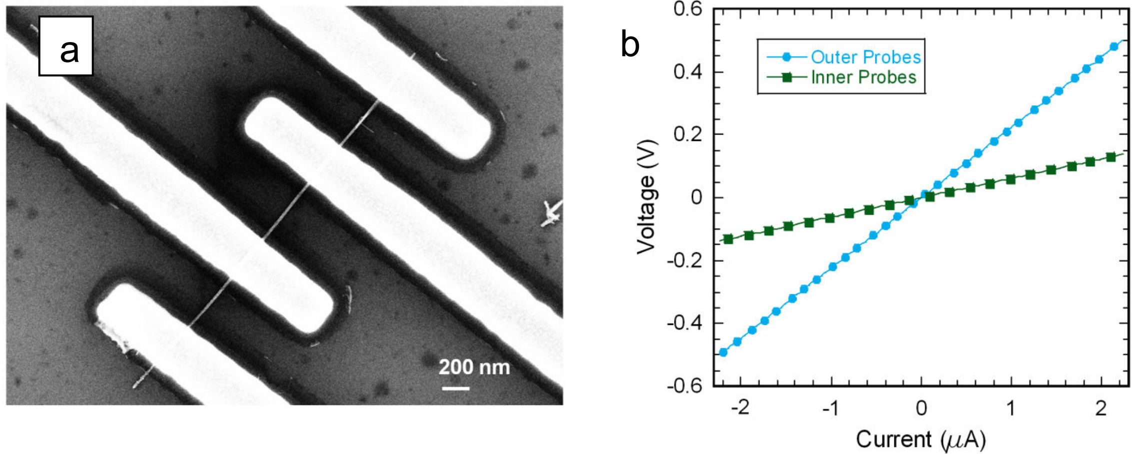

Figure 3.17 a) SEM image of four metal contacts to an InSb nanowire with diameter of 17 nm. b) Corresponding four-point probe current-voltage measurement.

Form this measurement we demined the source/drain contact resistance $R_s = R_d =$ 18 kΩ, which translates to ~3.9 x 10^{-6} $\Omega \cdot cm^2$ and the nanowire resistance of 1 μm length to be equal to R_{NW} = 62 kΩ. It can be seen that Ni makes good ohmic contact to InSb nanowires, however the contact resistance value should be taken into consideration in the evaluation of nanowire FET parameters.

Back-gated nanowire FET device were fabricates by suspending the nanowires on a heavily doped p-type silicon substrate with 300 nm thermally grown silicon dioxide, and following the same procedure for fabricating ohmic source and drain contacts described above. The gate length of the devices presented in this work varies from 0.75 μm to 1.5 μm. We are assuming that at these channel lengths (above 0.75 μm) there will

not be any considerable short channel effects.[48] The transfer characteristics of four nanowire FET devices are displayed in Figure 3.18.

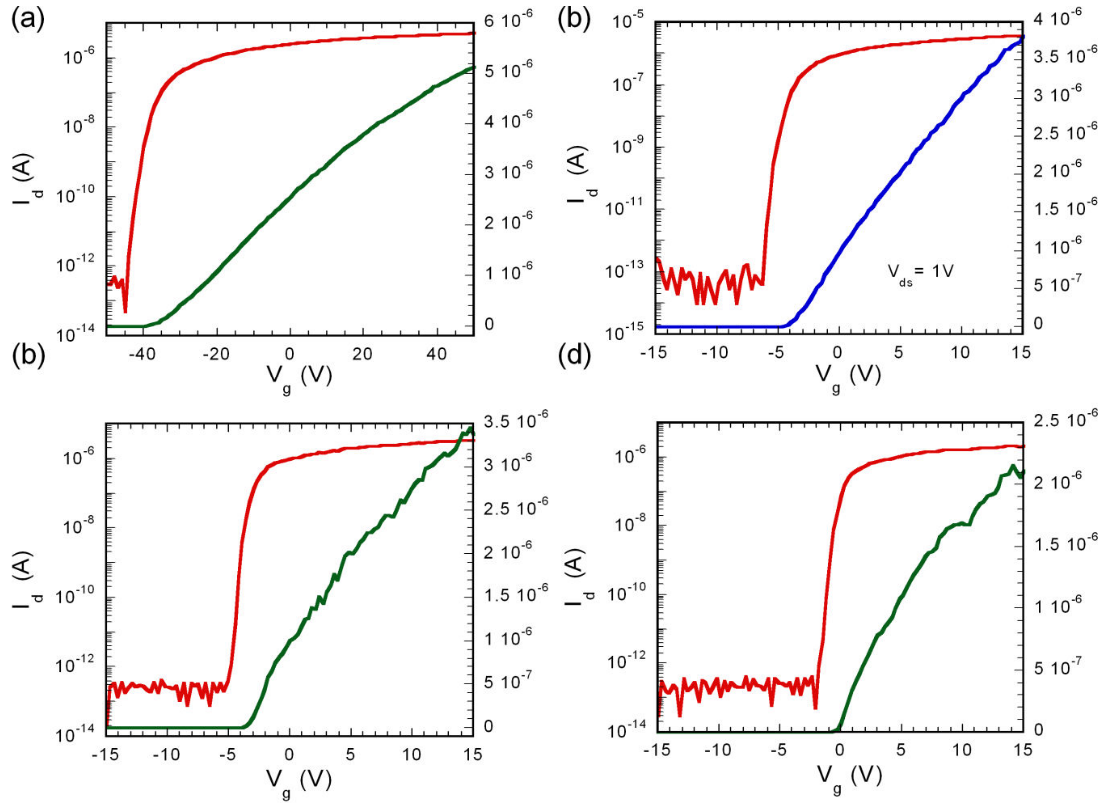

Figure 3.18 Transfer characteristics (I_D-V_{GS}) of InSb nanowire back-gated FET devices. a) nanowire diameter ~ 20 nm. b)nanowire diameter is ~ 10 nm. c) nanowire diameter ~ 10 nm, d) nanowire diameter ~ 7nm.

It can be seen that the nanowires are n-type, and the conduction channel can be completely depleted from electron carriers, and the FET operating in depletion mode can be turned off. The devices exhibit a very high I_{on}/I_{off} ratio of ~ 10^6 with the ON current in the order of 3-5 μA, at a bias voltage V_{DS} of 1V. A subthreshold slope *S* of 90-300 mV/dec was observed. It appears that the threshold voltage V_{Th}, varies from -1.5 V to -

45V volts, which is strongly correlated to the nanowire diameter. In Figure 3.18a we have the I_d-V_{gs} curve of a nanowire with diameter above 20 nm and V_{Th} is -45V. In Figure 3.18b and c, the diameters of the nanowires, whose I-V characteristic are shown, are roughly 10 nm and the threshold voltage is about – 5V, while in Fig. 3.18a we have the I_d-V_{gs} curve of nanowire with a diameter of bellow 10 nm (~7 nm), having a threshold voltage of -1.5V. This correlation can be explained by the carrier concentration in the nanowire channel, as nanowire diameter decreases the effective volume also decreases, thus the number of free charge carriers is decreased and lower gate voltage is required to fully deplete the nanowire channel.

The electron carrier density in the nanowire channel can be estimated by the total charge Q_{tot} in the nanowire is given by

$$Q_{tot} = C \cdot V_{th}$$

where V_{th} is the threshold voltage required to deplete the nanowire channel from carriers, and C is the gate capacitance given by Equation (2). The electron concentration n_e is then given by the fowling equation

$$n_e = \frac{Q_{tot}}{e\pi r^2 L_{eff}}$$

where e is the charge of electron, r is radius of the nanowires and L_{eff} is the length on nanowire channel.[39] The calculated value of electron density in InSb nanowire FET channel is in order of 1-5 x 10^{19} this value is three orders of magnitude larger than the

intrinsic carrier concentration in bulk InSb, which means that the as-grown InSb nanowires are unintentionally, slightly doped n-type, during the growth process.

Calculated electron mobility values of InSb nanowire FETs are in the order of 26-110 $cm^2V^{-1}s^{-1}$, which is large improvement from the InSb nanowires grown by electrochemical deposition, due to the higher crystalline quality of InSb nanowires grown by chemical vapor deposition, which has been indicated from the high resolution TEM images. However, this mobility value is far lower than the electron mobility observed in bulk InSb. One factor contributing to the lower electron mobility in InSb nanowire could be charge carrier scattering from the nanowire surface. From HRTEM image in Fig. 13(b) it can be seen that the nanowire surface is covered by few nanometer thick, amorphous layer. This claim can be further supported by the fact that electron mobility decreases with decrease in nanowire diameter, translating to a higher surface area to volume ratio, indicating that nanowire surface can have a significant effect in electron transport, especially in nanowires with sub 10nm diameter.

Top-gates InSb nanowire FET device were fabricated following the same procedure for making the source and drain contacts as described earlier, then a 30 nm high-k dielectric hafnium dioxide (HfO_2) was deposited over the nanowire devices, by atomic layer deposition carried at 250 ºC. The top gate was then fabricated by electron beam lithography and deposition of a 10 nm Ti/60 nm Au layer by electron beam evaporation. An SEM image of the top gated device is shown in Figure 3.19a, and the device transfer characteristics are shown in Figure 3.19b. It can be seen that that the drain

current increases linearly with change in gate voltage from -2V to 2V, and the nanowire channel cannot be depleted in the -2V to 2V gate voltage range. Higher gate voltages measurements were attempted however, they resulted in large leakage current through the gate dielectric and in some cases to the current burned the InSb nanowire. This shows that the breakdown of HfO_2 dielectric used was much lower than the expected theoretical value. Furthermore, parallel plate capacitors were fabricated to determine the relative permittivity ε_r the hafnium oxide gate dielectric, the results show that dielectric constant about 15, this much lower than the expected value of 25. Further research efforts must be done towards optimizing the deposition recipe, for improving the oxide reliability produced by our current atomic layer deposition system.

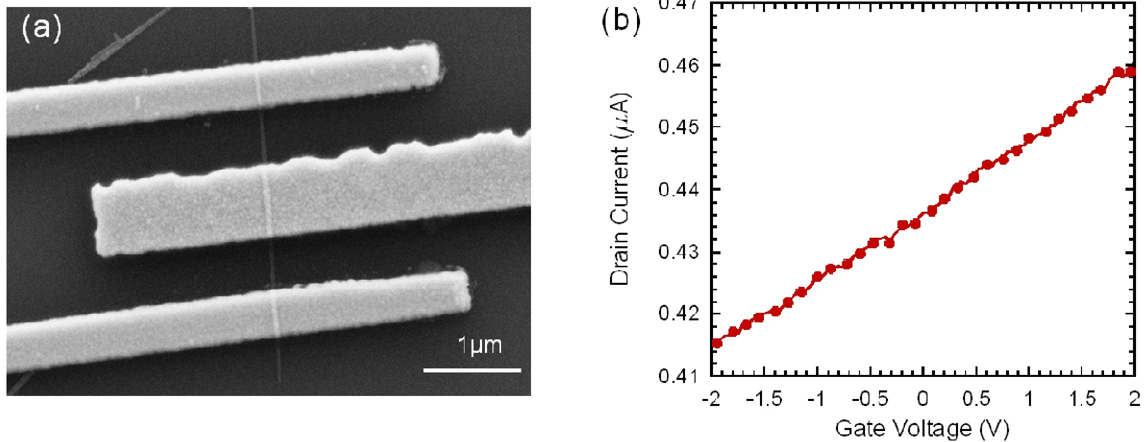

Figure 3.19. a) SEM image of InSb nanowire top gate FET. b) Transfer characteristics (I_D vs. V_{GS}) recorded on the top gate FET.

Electron mobilities obtained from the top gated InSb nanowire FET were in the range of 5-14 $cm^2V^{-1}s^{-1}$. This is almost an order of magnitude lower than what we have seen from the back-gated nanowire FETs, it can be explained by the existence of surface

state between the semiconductor and HfO_2 dielectric, which cause scattering of electrons and lower their mobility.[49] This technical issue necessitates that the nanowire surface must be passivated before depositing dielectric material.

3.3.1 Temperature dependent and diameter dependent I-V characterization of InSb nanowires.

Figure 3.20a, shows the transfer characteristics of InSb NWFET with temperature varied from 300 K to 100 K (V_{DS} is kept at 0.05V). A parallel downward shift of the I_D-V_{GS} curves is observed with decrease in temperature, however the NW channel cannot be fully depleted even at 100 K, and the “off current” at the lowest gate voltage is 0.205 μA. A liner correlation of InSb NWFET drain current with temperature is reveled in Figure 3.20b. The drain current, with no back gate voltage applied, changes from 0.21 μA at 100 K to 0.31 μA at 300 K. From the transfer characteristics in Figure 3.20a it can be see observed that electron mobility decreases as temperature decreases due to electron scattering from ionized impurities, as the thermal energy of electrons decreases. The downward trend in transfer characteristics as temperature decreases can be explained by the increases in drain and source contact resistance.

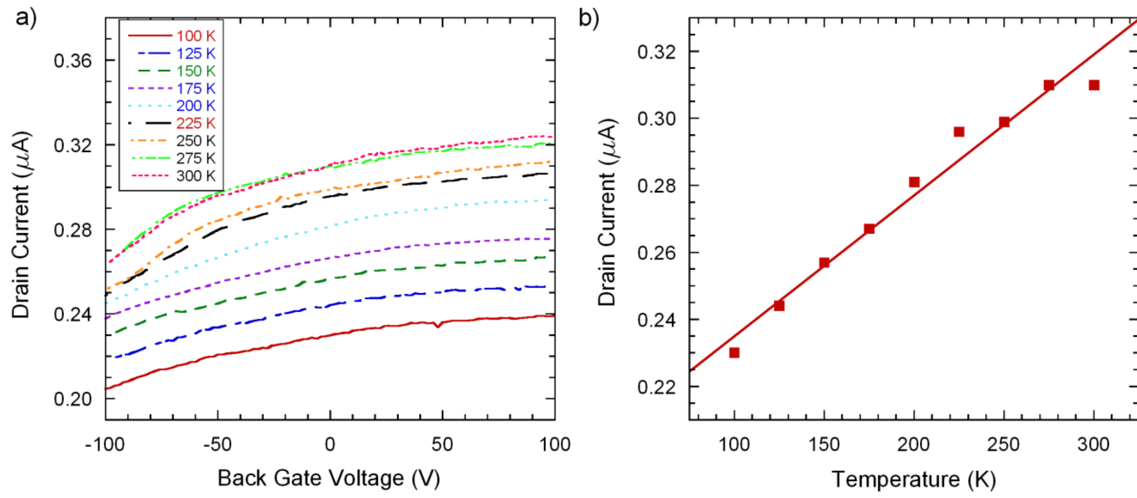

Figure 3.20 a) Temperature dependant transfer characteristics of InSb NWFET, with diameter 16 nm and channel length 1.2 μm, V_{DS} = 0.05V, b) InSb NWFET drain current vs. temperature.

Figure 3.21 displays SEM images of InSb nanowire devices of various diameters used in the diameter-dependent I-V measurements.

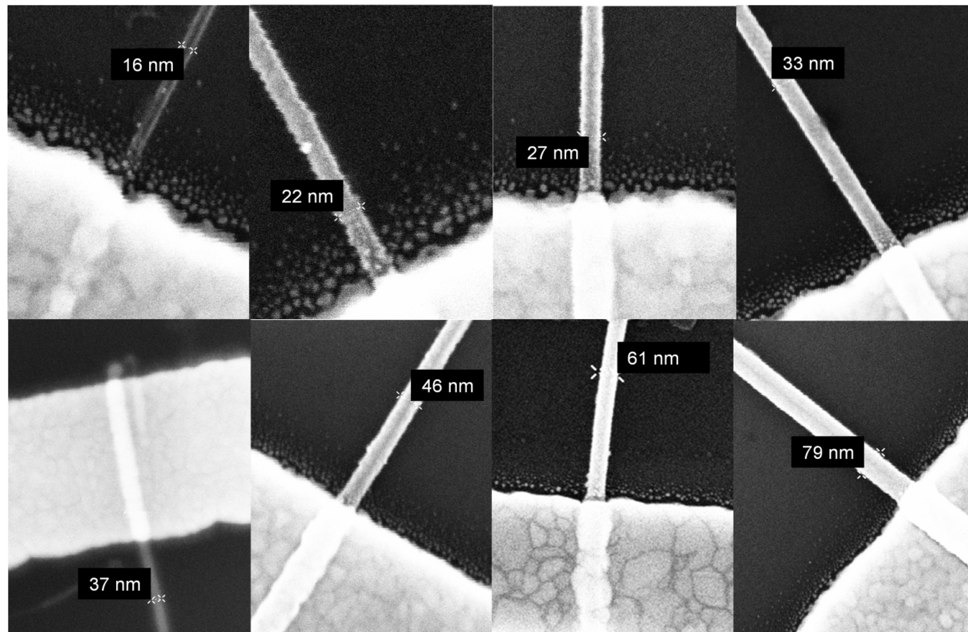

Figure 3.21 SEM images of individual InSb nanowire devices with diameters varying from 16nm to 79nm.

Figure 3.22a shows the electron mobility obtained from various InSb NWFETs versus their NW diameter. It was observed that the highest electron mobility of (17-19 $cm^2V^{-1}s^{-1}$) was obtained for nanowires with diameter in the range of 25-35 nm. Mobility decreases as the diameter decreases below 20 nm and also decreases as the NW diameter increases above 35 nm. The carrier concentration, n_e for all devices, was calculated using the following equation [50, 51]

$$n_e = \frac{C_{OX}\left(V_g - V_t\right)}{e\pi r_{NW}^2 L_{eff}}$$

where, V_{Th} is the threshold voltage and is determine from maximum transconductance in the linear operation region. Carrier concentration versus nanowire diameter is shown in Figure 3.22b, which shows that for all nanowires the electron density is above 10^{19} cm^{-3}, this a relatively high number compared to the intrinsic carrier concentrations of InSb ($2 \cdot 10^{16}$ cm^{-3}) at 300 K. The nanowire devices with diameter above 60 nm exhibit carrier concentration exceeding 10^{20} cm^{-3}, this high concentration of impurities can be a contributing factor to the lower electron mobility and the weak gating control observed in the larger diameter (60-80 nm) nanowires.[52] Other factors, such as surface roughness, may also be contributing to the overall low electron mobility for all InSb nanowires. Furthermore, due to the dielectric mismatch between the nanowire and the surrounding it environment, the donor ionization energy can increase, thus reducing free carrier density as the nanowire radius becomes smaller. [53, 54] This can explain the decrease in carrier concentration in InSb nanowires with diameter smaller than 60 nm. Another plausible explanation for the different doping concentrations is a diameter-dependent incorporation

mechanism of dopant impurities in the InSb nanowires during growth, such as transition from surface dopant incorporation to bulk incorporation as the nanowire radius increases. Another factor which can account for different carrier concentrations is the existence of surface states on the nanowire surface resulting in a depletion layer at the nanowire surface. Depending on the depth of the depletion layer the actual nanowire diameter will be decreased resulting in a smaller number of charge carriers in the nanowire channel.

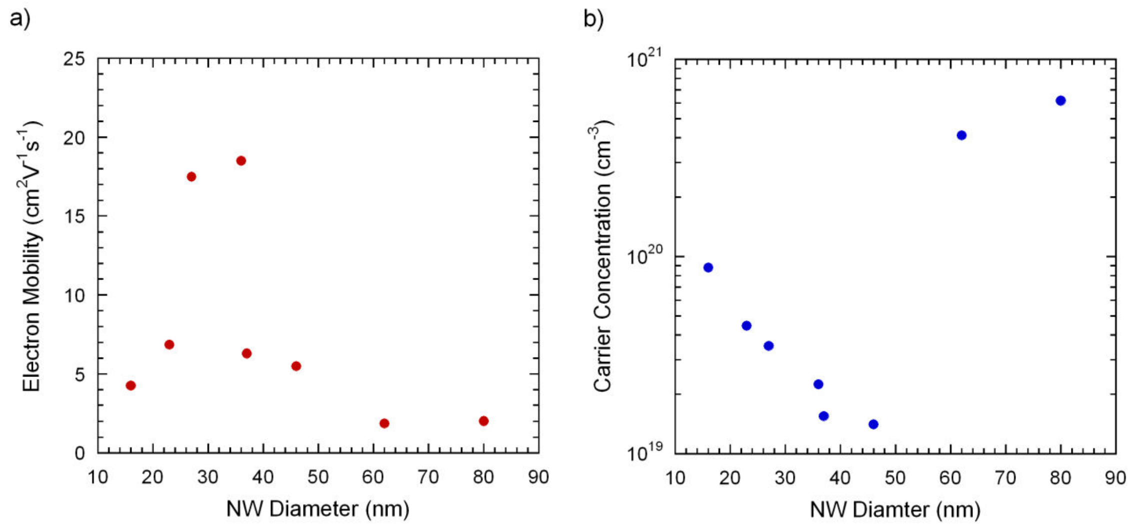

Figure 3.22 a) Electron mobility versus InSb nanowire diameter. b) Carrier concentration in InSb nanowires versus nanowire diameter.

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Chapter 4

Applications of InSb Nanowires in Gas Sensing

4.1 InSb nanowire field effect transistor for sensing Isopropanol, Acetone, and water vapors

Nanowires have many inherent properties owing to their nanoscale structure, which can be employed in applications of biological and chemical sensing. They exhibit high surface to volume ratio, leading to increased number of absorbed species.[1] The one dimensional nature and confinement of the nanowire channel, leads to increase sensitivity due to Debye screening length.[2] Other changes of properties such increase in reactivity can also be attributed to the nanoscale dimensions of nanowires. The presence of surface states and electron accumulation layer can lead to increased sensitivity to adsorbed species on the nanowire surface.[3] Various materials have been employed in nanowire sensing such as polymer, metal, metal-oxide, and inorganic semiconductor nanowires.[4-7] Among those, most notable ones are the metal-oxide nanowires sensors based on ZnO[8], SnO[9, 10], In_2O_3[11], Ga_2O_3[12], and CeO_2[13] nanowires.

Change in resistance is the most widely used property for detection by nanowire-based sensors. Based on the mechanism of operation, nanowire sensor devices can be divided in three groups. First group are chemresistors, in which the change of resistance is due to doping or direct charge transfer between the nanowire and the adsorbed analyte species on the surface of the nanowire. Second group is chemfets, where the change of carrier concentration is induced by the field effect of charged analyte species adsorbed on

the surface of nanowires. Third group is Schottky contact devices, where the Schottky barrier (thus device resistance) is modulated by the charge associated with the analyte species adsorbed on the surface of the metal contacts to the device. Although other mechanisms of analyte species interaction with nanowires can be responsible for the change in nanowire device resistance. For example, a recent study on InAs nanowire-based gas sensor has demonstrated that the change in conductance of InAs nanowire is due to enhancement of electron mobility combined with the effect of direct charge transfer from the adsorbed vapor species.[14] In addition, the study suggests that the electron surface accumulation layer on InAs nanowire can play a significant role in the sensing mechanism of analyte species.

Despite the many interesting electrical properties of InSb nanowires, which they share with InAs nanowire, such as small effective mass, high electron mobility, large Bohr radius, there are limited reports of InSb nanowires used in sensor devices. A recent journal publication has reported the use of InSb nanowire arrays for NO_2 gas detection with sensitivity down to 1 ppm (part per million).[15] The observed increase of InSb device was attributed to reduction of electron carrier concentration in the n-type InSb nanowire due to the NO_2 molecules adsorbed on the nanowire surface, acting as electron acceptors. These significant results reveal the potential of InSb nanowires in chemical sensing due to their high sensitivity.

In this work we have employed single InSb nanowires in field effect transistor sensor devices to detect the vapors of water, Isopropanol, and Acetone. The gas sensor

testing set-up is depicted in Figure 4.1, showing the gas cylinders of pre-diluted analyte gas and inert carrier gases. The gas flow is controlled by mass flow controllers connected to an interface controller box. The vapors of analyte gases are produced by passing an inert gas through a bubbler held at atmospheric temperature and pressure. The analyte gas is then additionally diluted to the desired concentration and carried through a gas line to the glass chamber enclosing the InSb nanowire device. The nanowire device is mounted on a chip carrier by wire-bonding, with wire leads connected to a semiconductor parameter analyzer (HP Agilent 4155C) for DC current-voltage measurements.

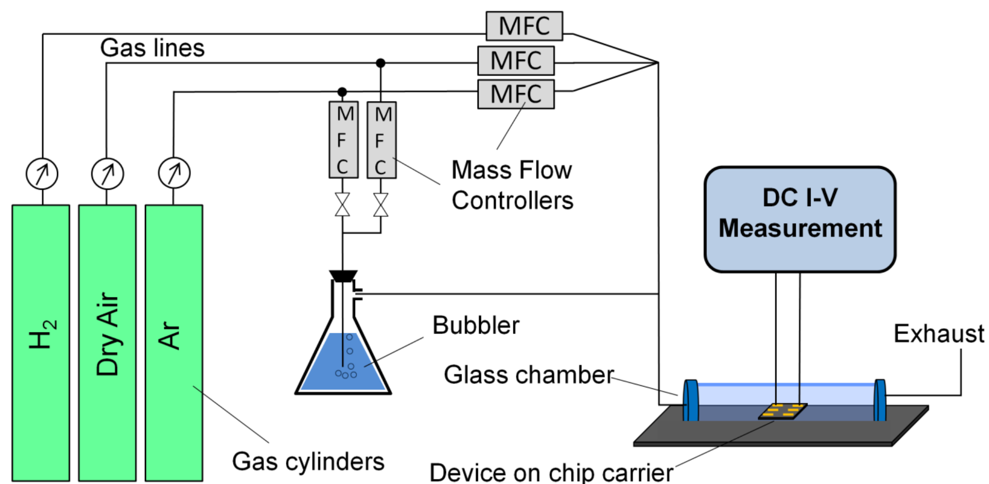

Figure 4.1 Schematic of instrumentation set-up for gas sensor measurements.

Figure 4.2a displays a picture of the InSb nanowire device on a chip carrier with soldered wire leads, covered by a glass chamber and air-tight sealed with silicone elastomer. Figure 4.2b depicts the back-gated InSb nanowire FET sensor, shown with analyte molecules adsorbed on the nanowire surface.

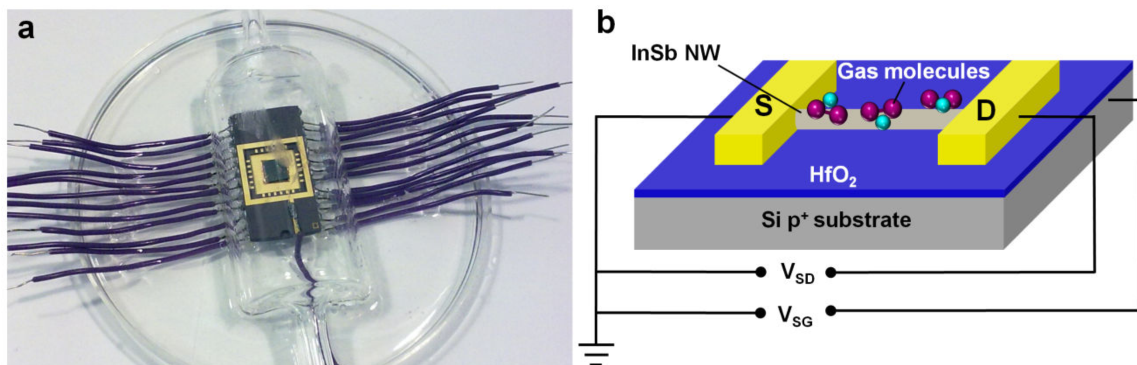

Figure 4.2 a) Photograph of InSb nanowire device mounted on chip-carrier, sealed in a glass chamber. b) Schematic depiction of back-gated InSb nanowire gas sensor FET device.

Figure 4.3a reveals the actual InSb nanowire device with Ti/Au metal contacts fabricated through e-beam lithography. The CVD grown InSb nanowires were deposited on heavily doped Si substrate with 30 nm HfO_2 deposited by atomic layer deposition. Figure 4.3b reveals the nanowire diameter to be 26 nm.

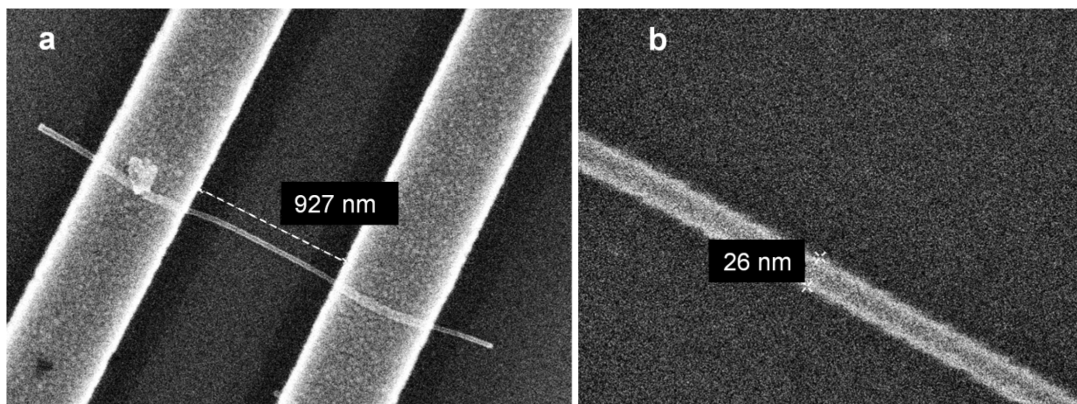

Figure 4.3 a) SEM micrograph of source and drain contacts to InSb nanowire FET device. b) SEM image indicating nanowire channel diameter of 26 nm.

Current-voltage measurements were conducted on the InSb nanowire device after it was sealed in glass chamber and Ar gas was purged at 50 sccm for several hours to

allow the device to stabilize and purge out any residual water vapor and oxygen molecules. The graph in Figure 4.4a shows the device resistance response to introduction of water vapor (generated by passing 70 sccm of Ar gas through a bubbler filled with deionised water) after Ar gas was flowed for ten minutes. A significant increase in nanowire resistance is observed, due to the adsorbed water vapor species, which begins to saturate after 10 min. Upon discontinuation of water vapor and introduction of Ar gas, no change is noted, suggesting that water molecules cannot readily be desorbed from the nanowire surface. In order to provide some energy necessary for the desorption of H_2O molecules from the nanowire surface, a UV light (wavelength of 365 nm and power intensity of $4W/cm^2$) was shone over the InSb nanowire device. Figure 4.4b shows the recovery of the InSb sensor device upon exposure to UV light, it can be seen that recovery takes less than 2 min when current starts to saturate.

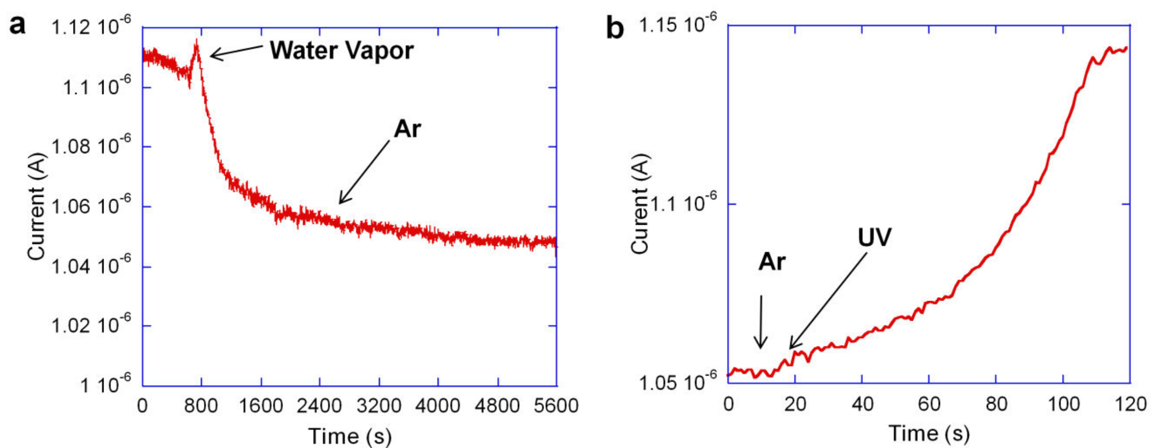

Figure 4.4 a) Current response upon exposure to water vapor, followed by purging Ar gas. b) Current response after exposure to UV light while purging Ar gas.

After complete recovery of the device, the InSb nanowire sensor was tested with Isopropyl Alcohol (IPA) replicating the procedures of the water vapor measurement. Figure 4.5a shows the sharp response of nanowire resistance to exposure of IPA vapor, the current drops and approaches saturation after about 2 min. Upon switching off the IPA vapor and switching on the Ar gas flow very little increase in current is observed. Once again UV light is used for the desorption of IPA molecules from the nanowire surface, as it can be seen from Figure 4.5b it takes 5 min for complete recovery of device. Figure 4.5c shows a graph of nanowire response to alternating exposure of IPA vapor followed by UV light exposure, this pattern shows that the InSb nanowire sensor device can be fully recovered, rest and activated again.

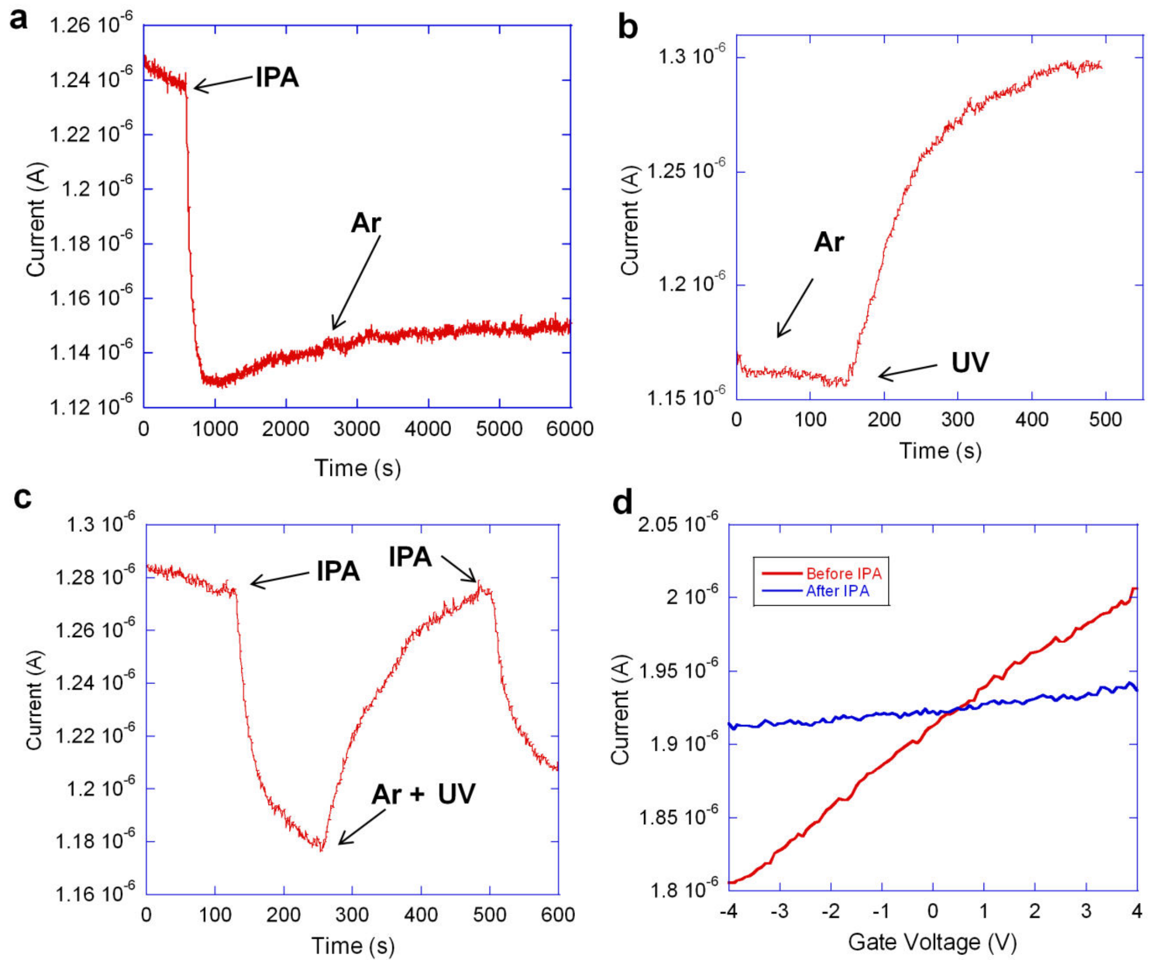

Figure 4.5 a) Current response upon exposure to IPA vapor, followed by Ar gas. b) Current recovery by UV light exposure while purging Ar gas. c) Current response to IPA vapor exposure alternated by recovery by UV light exposure. d) Transfer I_D-V_{GS} characteristics of InSb FET device before and after exposure to IPA vapor.

To elucidate the mechanism responsible for the nanowire resistance change transfer I-V characteristics (I_D-V_{SG}) of the nanowire device were obtained prior to and after the exposure of IPA vapors (Figure 4.5d). The change in carrier concentration, threshold voltage and electron mobility were calculated and compared. The field effect

electron mobility of InSb nanowires was determined from maximum transconductance of InSb NWFET, in the linear operation regime given by the equation

$$g = \frac{\partial I_{DS}}{\partial V_{GS}}$$

and the charge carrier field effect mobility is given by the equation

$$\mu = g \frac{L^2{}_{eff}}{C_{OX} V_{DS}}$$

where μ is the carrier mobility, L is the nanowire channel length, C the gate oxide capacitance, I_{sd} the source-drain current, and V_{gs} the gate-source voltage.[16] The capacitance for back gated NWFET can be expressed as

$$C_{OX} = \frac{2\pi\varepsilon_0\varepsilon_r L_{eff}}{\ln\left(\frac{2t_{OX}}{r_{NW}}\right)}$$

The carrier concentration, n_e for all devices, was calculated using the following equation [17]

$$n_e = \frac{C_{OX}\left(V_g - V_t\right)}{e\pi r_{NW}^2 L_{eff}}$$

where, V_T is the threshold voltage and is determined by linearly extrapolating the I_D-V_{GS} curve to cross the x-axis at zero drain current I_D, since the nanowire channel cannot be fully depleted. It is observed that after the exposure to IPA the electron mobility in InSb nanowire dropped from 13.8 to 1.3 $cm^2/(V \cdot s)$, while charge carrier concentration increased from $6.65 \cdot 10^{19}$ cm^{-3} to $6.6 \cdot 10^{20} cm^{-3}$. This finding suggests that the decrease in

conductivity of InSb is due to drop in electron mobility, which dominates over the electron transfer or donation from the adsorbed IPA molecules to the InSb nanowire.

Similar I-V behavior in InSb nanowire is observed upon exposure to Acetone vapor. The conductance drops and begins to saturate after 2 min (Figure 4.6a), upon discontinuing Acetone vapor flow and introducing Ar gas, very little recovery is observed. Figure 4.6b shows that the device can be recovered by exposure to UV light. Figure 4.6c shows the current response to exposure to Acetone vapor alternated by UV light, it can be seen that compete recovery to initial state takes longer than in the case of IPA vapor. From the transfer characteristics I_D-V_{GS}, in Figure 4.6d, before and after exposure to Acetone, it is observed that I_D-V_{GS} is not linear after the exposure to Acetone. The calculated electron mobility in InSb nanowire after Acetone exposure at zero gate voltage was 8.5 $cm^2/(V \cdot s)$ and electron carrier concentration n $9.9 \cdot 10^{19}$ cm^{-3}. This result indicates that there was reduction in electron mobility from the initial InSb nanowire state, however it is not as large as in the case of IPA. Same holds true for the electron concentration an increase is observed due to charge transfer from Acetone molecules to InSb nanowire.

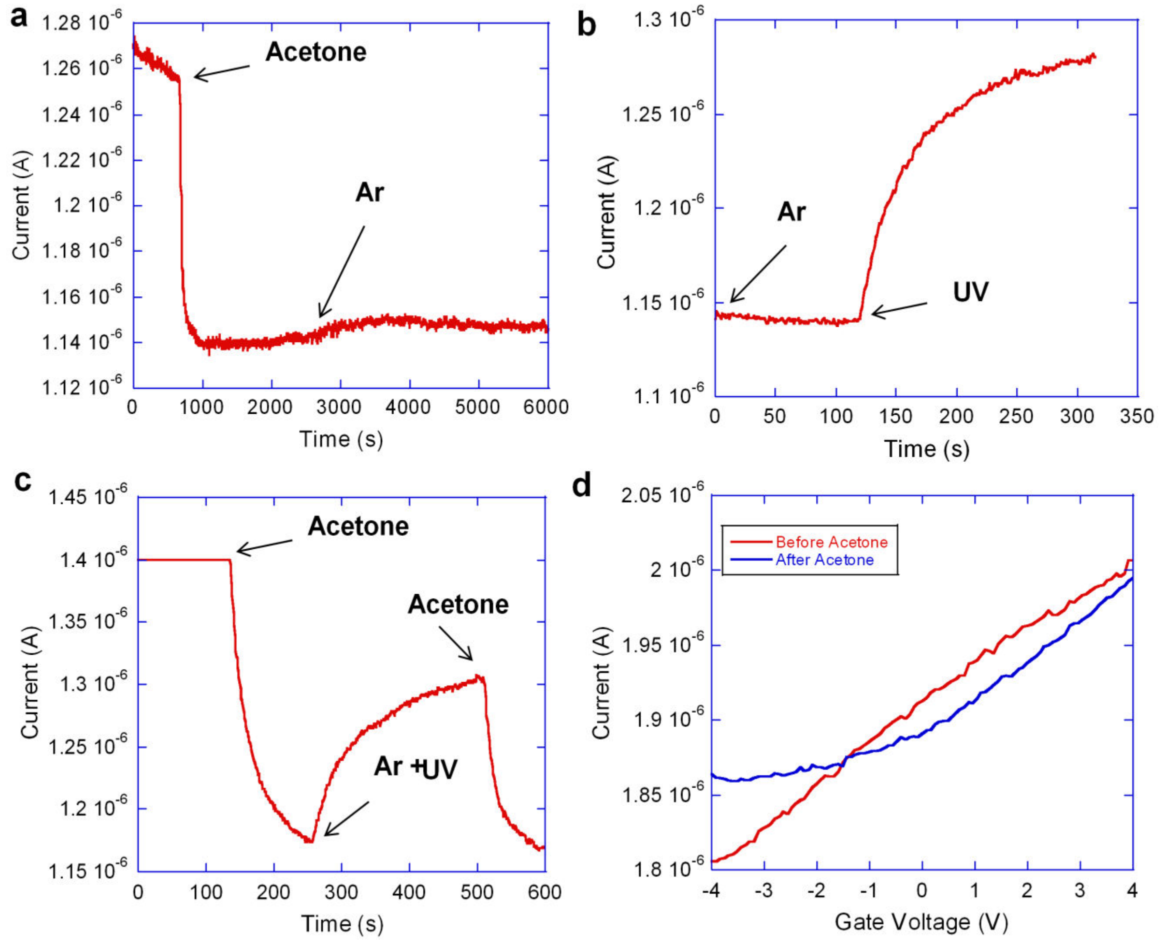

Figure 4.6 a) Current response upon exposure to Acetone vapor, followed by purging Ar gas. b) Current recovery by UV light exposure while purging Ar gas. c) Current response to Acetone vapor exposure and recovery by UV light exposure. d) Transfer I_D-V_{GS} characteristics of InSb FET device before and after exposure to Acetone vapor.

Similar effect was observed in the case of water vapor adsorption on InSb nanowire, with electron mobility decreasing to 3.4 $cm^2/(V \cdot s)$ and electron concentration increasing to $2.5 \cdot 10^{20} cm^{-3}$.

4.2 Sensing of Hydrogen gas by Pt nanoparticle coated InSb nanowire field effect transistor.

There is an increased interest in developing Hydrogen gas sensors at low cost, high sensitivity and fast response rates, since H_2 is combustible even when diluted down to 7% with air, and it is a colorless, odorless gas.[18] Commonly Platinum and Palladium have been employed in chemresistor H_2 sensors, due to the ability of these two metals to act as catalyst on H_2, by absorbing H_2 and undergoing a phase change resulting in change of resistance. Pt and Pd have also been applied to chemfet and Schottky contacts H_2 sensor devices, due to their ability to absorb H_2 and decompose it into a H-H, the associated charge of which is used to modulate the gate voltage or Schottky barrier in the respective devices.

There have been reports on using Pt nanowires[19] and Pd nanowires[18, 20] in chemresistors for H_2 detection, which show some promise. A different approach to sensing H_2 is achieved by utilizing Pt and Pd nanoparticles deposited on semiconductor nanowires or thin films[21, 22], thus combining the catalytic effect of Pt and Pd with the sensitivity and fast response of semiconductor devices.

In this work we have fabricates single InSb nanowire field effect transistors and tested their potential in H_2 detection. InSb nanowire devices were fabricated and gas sensing measurements were carried out following the protocol described in detail in previous section (4.1). A diluted gas mixture of dry air and H_2 0.1% was used in this study. Figure 4.7a shows the current response in InSb nanowire upon exposure to 0.1% H_2 gas. It appears there is no significant change in resistance due to H_2, this can be

attributed to low adsorption rate of H_2 molecules on the nanowire surface due the low affinity of H_2 for InSb. Therefore, Pt nanoparticles were deposited on the InSb nanowire devices acting as a catalyst for absorbing H_2 molecules. A layer of 1nm Pt was deposited by electron beam evaporation, resulting in discreet Pt nanoparticles rather than a conductive thin film. It should be noted that metal deposition by e-beam evaporation is anisotropic resulting in deposition of Pt nanoparticles on top half cylinder of the nanowire and increased density at the top of nanowire where deposition direction is normal to the nanowire surface. Figure 4.7b displays the current response Pt nanoparticle decorated InSb nanowire to 0.1% H_2. An increase in conductivity is observed, followed by a fast recovery when H_2 flow is terminated and dry air gas is purged through the chamber. The InSb sensor device exhibits fast response and quick recovery at room temperature. The signal to noise ratio for 0.1% H_2 is about five.

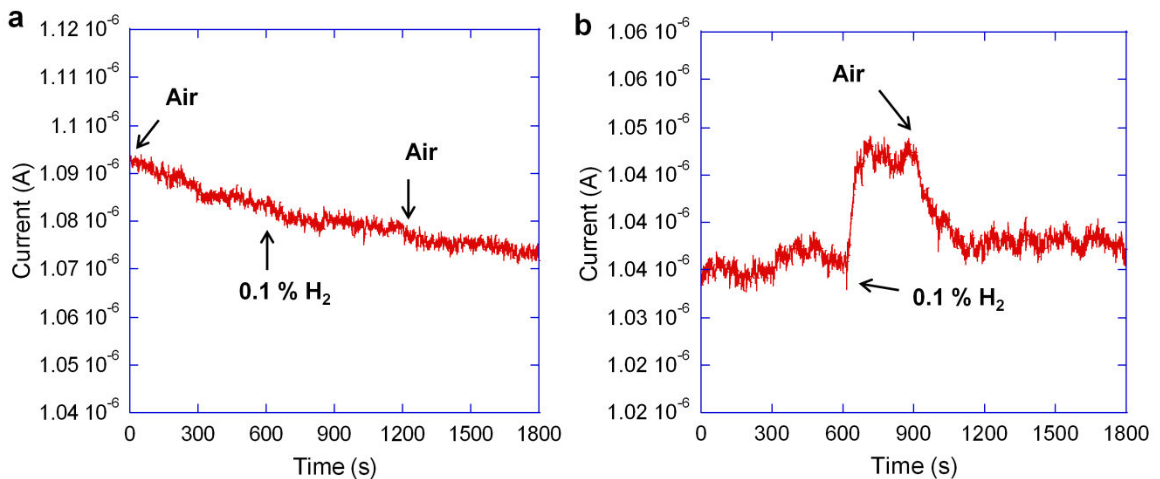

Figure 4.7 a) Current response of InSb nanowire device upon exposure to 0.1% H_2 gas. b) Current response of Pt nanoparticle covered InSb nanowire device upon exposure to 0.1% H_2 gas.

The mechanism of hydrogen sensing by solid state device using a catalyst such as Pt or Pd as the metal gate over insulator is already well-known.[23] The Pt metal serves as a catalyst for decomposing H_2 into H dipole. The hydrogen gas molecule is absorbed by the Pt metal and dissociated in H atoms, which defuse to the metal insulator interface, creating a dipole layer and effectively shifting the gate potential voltage.[24] In the case of n-type InSb nanowire a H-H dipole would form at the Pt-nanowire interface with a positive potential on the nanowire surface side, resulting in increase of the number of electrons in the nanowire channel. This proposed mechanism can elucidate the increase in conductivity of InSb nanowire. The recovery of the device is achieved by the oxygen molecules present in the dry air gas, which adsorb on Pt surface and dissociate in O atoms, forming OH and consequently H_2O molecules, which are purged out by the flowing gas.

4.3 Performance of graphene-based versus InSb nanowire-based FET sensor for detecting Hydrogen.

Graphene, a monoatomic carbon layer, has attracted a tremendous scientific interest due to its exceptional electronic and structural properties.[25, 26] Being a truly two dimensional material, its high surface to volume ratio, high electron mobility, low electronic noise and chemical stability render graphene an ideal candidate for chemical and bio-sensing applications.[27-29] It has been demonstrate that graphene is capable of detecting individual gas molecules due to its low noise.[30] Sensing mechanism of grpahene has been explained in terms of chemical doping, which is a direct result of the gas species being adsorbed on the surface of graphene, acting as either donors or acceptors, consequently changing the charge carrier concentration in graphene and its conductivity accordingly.[30] However a more recent study has revealed that intrinsic graphene has very low affinity for a number of different gas species, in which case gas molecules do not readily adsorb on the surface of graphene.[31] Furthermore, the adsorption of gas molecules on graphene surface was attributed to the polymer (photoresist/electron-beam resist) residue left on graphene surface after device fabrication process.

In the case of Hydrogen gas sensing by graphene, it is necessary to create a platform that would facilitate the adsorption of H_2 and the subsequent chemical doping of graphene. Different configurations of graphene have been used to demonstrate its potential in H_2 sensing, for example graphene/polyaniline nanocomposite [32],

Platinum/graphene like nanosheets [33], CVD graphene covered by Palladium nanopraticles [34], and Platinum coated graphene on SiC[35]. In this study we aim to elucidate sensing mechanism of H_2 by CVD graphene covered with Pt nanoparticles, detection limit, saturation and recovery of the device are also explored.

Graphene films were grown on a 25 μm thick copper foil (Alfa Aesar) by CVD method as reported.[22] Copper foil treated with acetic acid and rinsed with deionized water to ensure the surfaces were completely clean and free from oxides. Next, the pretreated copper foil foils were loaded into a quartz-tube furnace, heated to 1000° C in a 2 Torr Ar/H_2 (200:200 sccm) atmosphere, and thermally annealed for 30 min. For the growth of graphene, methane (100 sccm) was introduced into the chamber under 20 Torr total pressure, for 20 min, after which the chamber temperature was reduced to room temperature at an average cooling rate of 50 °C min^{-1}. After the sample was cooled, poly methyl metha acrylate (PMMA) was spun coat over the graphene on copper and baked at 110º C for 5 min. The copper foil was then etched in $FeCl_3$ aqueous solution of 0.2 M, mixed with HCl 2% by volume. The graphene sheets covered by PMMA were rinse in DI water and transferred to Si/SiO_2 substrate, where the heavy doped Si p+ substrate is used as a back gate, and 300 nm thermally grown SiO_2 acts as a gate dielectric.

Graphene rectangles of size 1mm by 0.3mm (Figure 4.8a) were fabricated by photolithography followed by O_2 plasma to etch away the rest of graphene. Subsequent lithography step was used to pattern the contact area, followed by deposition of Ti/Au

(10/100nm) by electron beam evaporation (Figure 4.8a). Figure 4.8b shows a Si chip containing a dozen of devices, mounted on a chip carrier and wire bonded.

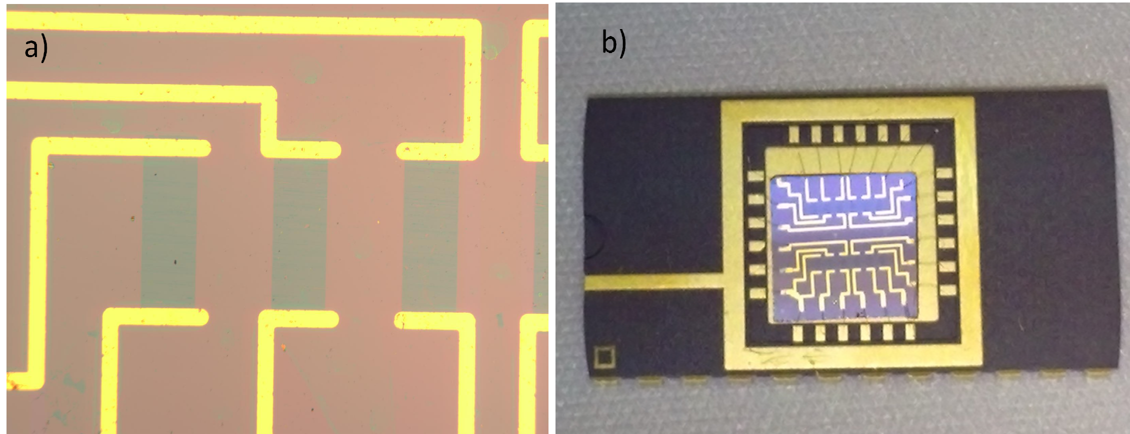

Figure 4.8 a) Patterned graphene devices, graphene dimensions of 1 mm by 0.3 mm. b) Chip containing a dozen devices mounted and wire-bonded on a chip carrier.

The quality and morphology of graphene were investigated by Raman spectroscopy, scanning electron microscopy (SEM), and optical microscopy. Optical and scanning electron microscopy indicate a continuous graphene film without any visible wrinkles or cracks (Figure 4.9a). Raman data indicates the presence of an intense G band at 1581 cm^{-1}, 2D band at 2709 cm^{-1} peaks (Figure 4.9b). Presence of islands of two graphene layers are visible in SEM image and indicated by the ratio of the 2D to G peaks in the Raman spectra. Four-point-probe measurements reveal that graphene exhibits a sheet resistance of 500-1000 Ohm/Sqr. Back-gated FET measurements show the typical ambipolar current-voltage (I-V) characteristics of graphene with carrier mobility in the order of 1000 $cm^2V^{-1}s^{-1}$.

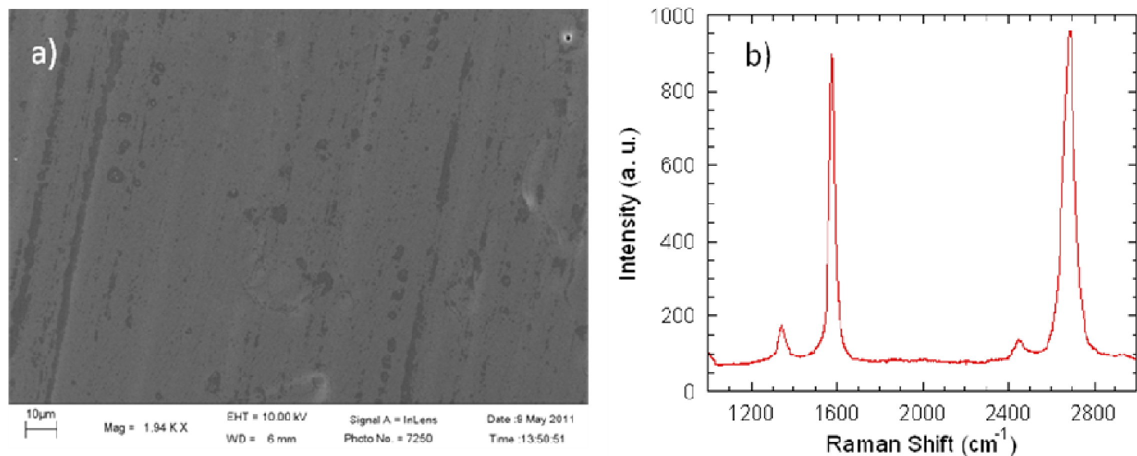

Figure 4.9 a) SEM image of graphene on Si/SiO_2 substrate. b) Raman spectra of graphene on Si/SiO_2 substrate.

Chip carrier containing graphene devices was placed and air-tight sealed in a quartz chamber through which dry air gas and hydrogen gas were introduced, the gas flow was controlled by mass flow controllers (MFCs) as described in Sec.4.1. Bare graphene device does not show any change in conductivity upon introduction of 1% H_2 diluted in dry air (Figure 4.10a). This result indicates that pristine graphene has a low affinity for H_2, and by itself is not suitable for H_2 sensing. As a result of this we deposited Pt layer of 1nm nominal thickness over the graphene devices by electron-beam evaporation. It should be noted that the resulting film was not continuous conductive layer, but rather individual Pt nanoparticles. Pt was chosen here due to its catalytic effect on H_2, due to which it has been long used in solid state gas sensors.[24] Figure 4.10b shows the conductivity response of graphene devices, with Pt nanoparticles deposited over them, upon exposure to Hydrogen gas. It can be clearly seen that device conductivity decreases with H_2 and recovers back up when only dry air is flowed through the chamber.

Back gated measurements confirmed that graphene's Dirac point was shifted to the left after exposure to H_2, which leads to the drop of conductivity. It should be noted that the Dirac point of intrinsic graphene devices, prior to H_2 gas exposure was not situated at 0V but shifted right at about +20 to +40V, therefore a shift leftward would cause reduction of charge carrier (holes) concentration and reduction in conductivity. Most of our CVD graphene samples are intrinsically p-type, after synthesis and transfer on Si/SiO_2 substrates.

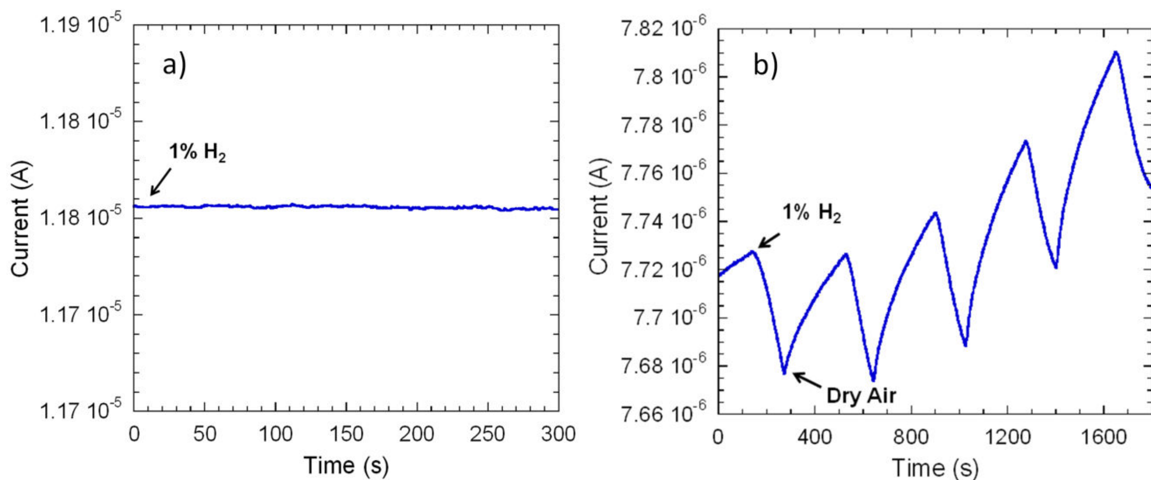

Figure 4.10 a) Current response of bare graphene vs. time upon exposure of 1% H_2. b) Current response of graphene/Pt nanoparticles upon exposure to 1% H_2 alternated by dry air alone.

In the case of Pt nanopraticles over graphene being exposed to H_2, a H dipole would form at the Pt-graphene interface with a positive potential on the graphene side, resulting in an increase of the number of electrons in graphene, thus doping it n-type. This proposed mechanism would explain the decrease in conductivity of graphene, however after prolonged exposure to 1% H_2 diluted in dry air the conductivity initially

decreases and then after 500 s starts to increase and goes above its initial value prior to the introduction of H_2 (Figure 4.11a). This behavior was not observed when the sensor was exposed to 1% H_2 diluted in Argon gas, as it is seen from Figure 4.11b the conductivity of graphene drops and starts to saturate after about one hour.

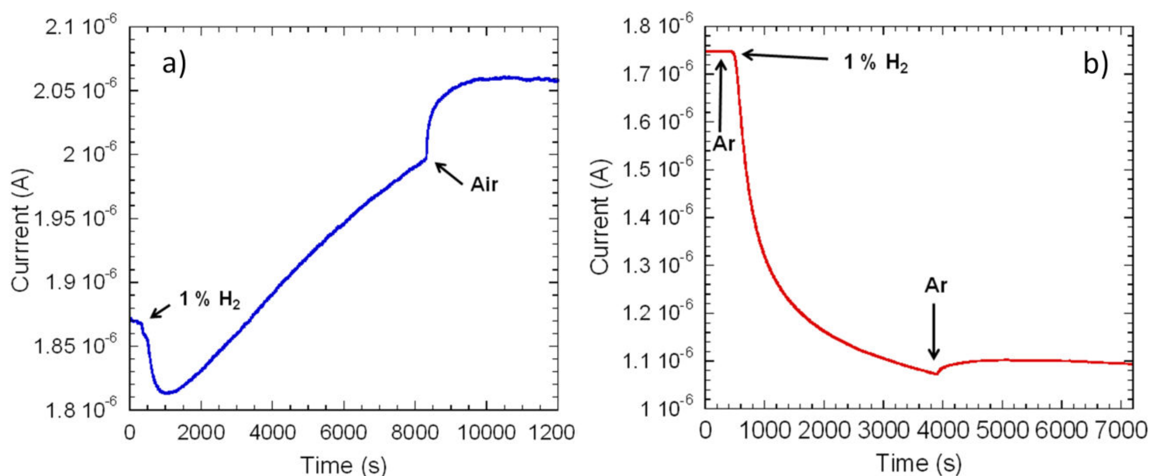

Figure 4.11 a) Current response upon exposure to 1% H_2 diluted in dry air for 2 h, followed by dry air alone. b) Current response to exposure of 1% H_2 diluted in Ar followed by purging Ar alone.

The increased conductivity of graphene upon prolonged exposure of H_2 diluted in air, can be explain by the presence of O_2, which adsorbs on Pt surface and dissociates in O atoms, forming OH and consequently H_2O molecules in a recombinative process. It has been shown that water molecules adsorbed on graphene surface can dope graphene p-type.[36] This rightward shift of Dirac point can explain the increase of graphene's conductivity to a point higher than its intrinsic conductivity. Furthermore, it appears that the p-type doping of graphene due to H_2O molecules dominates over the doping effect of H dipole, strengthened by the fact that as the reaction goes on H_2O molecules continue to

form and accumulate on the graphene surface, while the absorbed H atoms in Pt reach a maximum level. It should not be disregarded that Oxygen playas an instrumental role in the desorption of H atoms from the Pt-graphene interface, and thus the recovery of the H_2 sensor. It can be seen from figure 4b that the graphene device conductivity cannot be fully recovered to its initial value after purging with Ar for 1h. This result indicates that the H atoms cannot be desorbed from Pt.

From Figure 4.12a it can be seen that the graphene-Pt devices show good sensitivity to 0.1% H_2 diluted in dry air with large signal to noise ratio. Furthermore, it is observed that the conductivity of graphene after a prolonged exposure of 0.1% H_2 diluted in dry air decreases and begins to saturate (Figure 4.12b). These results indicated that the resulting H_2O molecules are not adsorbed on the graphene surface, or the amount is not substantial to cause a noticeable p-type doping and an increase in device conductivity.

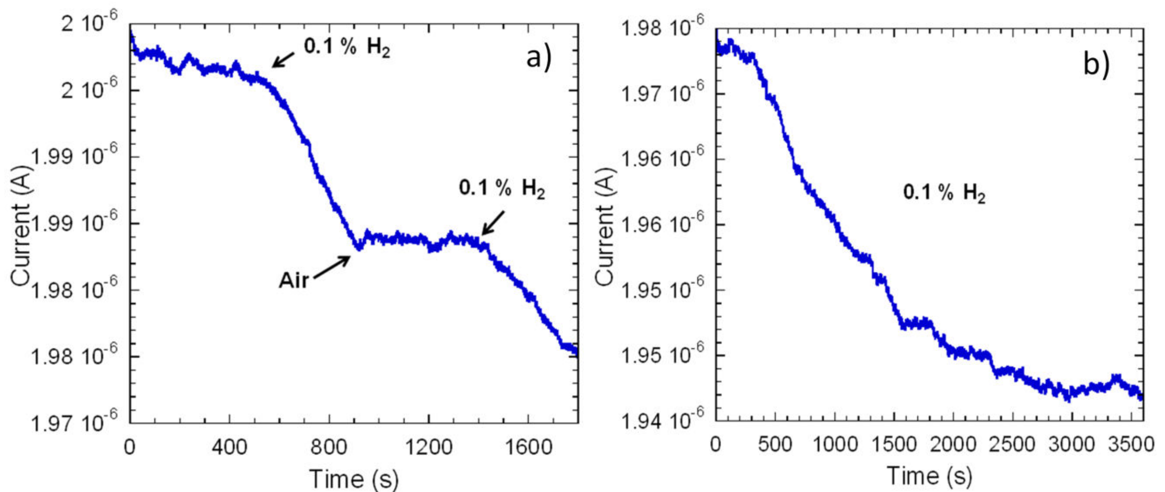

Figure 4.12 a) Current response to 0.1% H_2 diluted in dry air alternated by air alone. b) Prolonged exposure graphene sensor to 0.1% H_2 diluted in dry air.

Comparing the graphene-based sensor response to 0.1% H_2 (Figure 4.12a) to that of InSb nanowire devices (Figure 4.7b), it can be seen that InSb nanowire device exhibits faster response and faster recovery. Graphene-based device, on the other hand, shows much lower noise figure with high signal to noise ratio, allowing for increase in its detection limit beyond 0.1% H_2.

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