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SUMMARY

The application of many CCDs (Charge-Coupled-Device) in a large system requires efficient clock drivers capable of delivering to capacitive loads large voltage swing, fast rise and fall times with low power consumption. The driver circuit described meets these requirements using off-the-shelf inexpensive transistors. Notable aspect is the absence of bias-current in the drivers with each output capable of delivering 17 V in 5 ns.

INTRODUCTION

Analog-to-digital (A/D) converters with eight-bits resolution and 10 MHz bandwidth are available but expensive. Coupled to these specifications the need to digitize many channels in a proposed high-energy physics experiment, the total cost of A/D converters in such a large system would be prohibitive. A solution to this problem is to use CCDs as low-cost analog sampled preprocessors¹. Two advantages are: a) provision for analog delay, and b) sample and hold, thereby reducing the cost of subsequent A/D converters.

A difficulty in the application of many CCDs is the design of a high performance and inexpensive clock driver circuit. Each driver must be capable of delivering to a relatively large capacitive load large voltage swing with small rise and fall times. In addition, low operating power is a factor which must be met for operational economy in a large system. A driver circuit which meets these requirements has been designed and tested to specifically drive Fairchild CCD 321, a dual channel 455-bit analog shift register². During the early development stage, it was necessary to investigate the maximum clock frequency at which the CCD continues to function reliably. An arbitrary design minimum of approximately 20 MHz rate and 17 V swing was thought necessary. The load to be driven is approximately 30 pF, representing one (1) transport clock input.

CIRCUIT DESCRIPTION

Basic Driver Circuit

The basic clock driver circuit shown in Fig. 1 essentially consists of two functional blocks: a) a differential voltage amplifier Q1 and Q2, and b) a complimentary emitter-follower output amplifier Q3 and Q4. The circuit operates in the following manner: Q1 is driven through 50 Ω coaxial cable with pulses of

MECL* 10,000 logic levels. Current switching between Q1 and Q2 produces 17 V swing across the collector load (430 Ω) which is coupled to the bases of Q3 and Q4.

Fig. 1. Basic CCD clock amplifier/driver

Figure 1a shows Q3-Q4 output voltage waveform across a 70 pF capacitive load--representative of two (2) CCD clock inputs. Output rise and fall times is approximately 5 ns with relatively small overshoot.

The complimentary emitter-follower output pair operates without the usual bias current which contributes to increased standby power. To function efficiently, the design incorporates the parasitic inductance in series with the load capacitance to form a series resonant circuit. The "fly-wheel" effect of the resonant circuit provides additional charge to the load to compensate for voltage lost through base-emitter drop. Series damping resistor is necessary to minimize overshoots.

Fig. 1a. CCD clock driver output into 70 pF load

*This work was done under the auspices of the United States Department Of Energy.

**References to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

Multi-Output Driver Circuit

Figure 2 shows the final design of a four (4) output version of the basic driver circuit. Operation is similar except for the following additions: Q3-Q4 now provides additional current-gain and buffering between the amplifier and output drivers; the 10 Ω - 100 pF network in the emitter circuit of Q1-Q2 prevents the amplifier from breaking into oscillations; collector diode H-P 2800 prevents Q2 from saturation; and amplifier peaking coil (0.3 μ H) contributes to smaller rise and fall times. 10 Ω resistors at the emitter-follower output stage minimize pulse overshoot and ringing.

Fig. 2. CCD clock driver with four (4) outputs.

Figure 2a shows one of four outputs with each driving 17 V into a 70 pF load.

Fig. 2a. CCD clock driver output with four (4) outputs each into 70 pF load.

DISCUSSION AND CONCLUSIONS

Complimentary emitter-follower output transistors, 2N2222 - 2N2907 appears to offer the best compromise in performance vs. cost. These transistors have moderate bandwidth but are able to withstand high voltage and high peak current. However, to operate these devices at high pulse rate, saturated-switching must be avoided because of large storage time.

Tests results show the multiple clock drivers exceeded design goals. Each output is capable of more than 17 V swing with rise and fall times of 5 ns into a single CCD transport clock input. However, for economy reasons, two input-loads (approximately 60 pF) are driven by a single output driver with small increase in rise and fall times. The drivers are stable so reproducibility should pose no problem.

REFERENCE

1. Yazgan, E. and Kirsten, F., Characterization of Charge-Coupled Analog Memories for Nuclear Data Acquisition", IEEE Trans. Nucl. Sci. NS-25, No. 1, (1978).

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