Title
Electric Field Modulation of Light Emission in Silicon Gated Diodes

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Publication Date
2014

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA,
IRVINE

Electric Field Modulation of Light Emission in Silicon Gated Diodes

DISSERTATION

submitted in partial satisfaction of the requirements
for the degree of

DOCTOR OF PHILOSOPHY

in Electrical Engineering and Computer Science

by

Kaikai Xu

Dissertation Committee:
Professor Guannpyng Li, Chair
Professor Chen S. Tsai
Professor Chin C. Lee

2014

DEDICATION

To

my family

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ACKNOWLEDGMENTS

I would like to express the deepest appreciation to my committee chair, Professor Guannpyng Li (G. P. Li). Without Professor G. P. Li's support, guidance and persistent help, this dissertation would not have been possible.

I should like to thank Professor Weifeng Sun (in the National ASIC Systems Engineering Research Center, the Southeast University, Nanjing, China) and his research group for their help and discussion in the simulation section in the dissertation. I am grateful to the colleagues at the Chongqing University for their valuable technical support and useful discussion.

I would like to thank my committee members, Professor Chen Tsai and Professor Chin Lee, for their careful review, useful comments, and constructive suggestions on the dissertation.

I am deeply indebted to my parents who provide much-need encouragement while I am finishing the work toward the doctoral degree. Finally, much is owed to my wife Wenjia Kong and my son Haobo Xu for putting up with a part-time husband and father for nearly 4 years.

R. Newman's work on light emission observed in the material of silicon ("Visible light from a silicon p-n junction," Phys. Rev., vol. 100, no. 2, 1955,) is the first work to report silicon p-n junction under avalanche breakdown could emit visible light. A. Grove, O. Leistiko, and W. Hooper's classic work on gate-controlled diode ("Effect of surface fields on the breakdown voltage of planar silicon p-n junctions," IEEE Trans. Electron Devices, vol. ED-14, no. 3, 1967) inspires me to build a bridge between MOSFET and LED from electronics to photonics. As such, I am grateful to these great pioneers.

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[1] K. Xu and G. Li, "A three terminal silicon-PMOSFET like light emitting device (LED) for optical intensity modulation," IEEE Photonics Journal, vol. 4, no. 6, pp. 2159-2168, 2012.

[2] K. Xu and G. Li, "A novel way to improve the quantum efficiency of silicon light emitting diode in a standard silicon complementary metal-oxide-semiconductor technology," Journal of Applied Physics, 113, 10, 103106, 2013.

[3] K. Xu and G. Li, "Hot-carrier induced photon-emission in silicon metal-oxide-semiconductor field-effect-transistor," Journal of Physics: Conference Series, **488**, 132036, 2014 (XXVIII International Conference on Photonic, Electronic and Atomic Collisions (ICPEAC 2013)).

[4] K. Xu and G. Li, "Light-emitting device with monolithic integration on bulk silicon in standard complementary metal oxide semiconductor technology," Journal of Nanophotonics, vol. 7, no. 1, 073082, 2013.

[5] K. Xu and G. Li, "A light-emitting-device (LED) with monolithic integration on bulk Silicon in a standard CMOS technology," in International Photonics and Optoelectronics Meetings (POEM), OSA Technical Digest (online) (Optical Society of America, 2013).

[6] K. Xu and G. Li, "Silicon electro-optic modulator based on the theory of gate-controlled diode," in International Photonics and Optoelectronics Meetings (POEM), OSA Technical Digest (online) (Optical Society of America, 2013).

ABSTRACT OF THE DISSERTATION

Electric Field Modulation of Light Emission in Silicon Gated Diodes

By

Kaikai Xu

Doctor of Philosophy in Electrical Engineering and Computer Science

University of California, Irvine, 2014

Professor Guannpyng Li, Chair

A silicon gated diode, being evolved from MOSFET technology and utilizing a half of MOSFET, has been developed as LED) for the first time to demonstrate unique electric field modulation of light emission characteristics. In contrast to a reverse biased traditional two-terminal Si-diode possessing light emission modulation by current signal, this three-terminal Si-gated diode is capable of modulating optical emission by applied gate voltage signal, which is directly compatible with a standard CMOSFET circuit operation easing monolithic integration of logic circuit implementation and a light emission diode on silicon technology. The gate applied voltage can produce two effects on the gated diode. Firstly, it induces carrier concentration modulation at both channel and source/drain region underneath the gate, thus modulating electric field strength and distribution. Secondly, an inversion layer of surface carriers underneath the gate in the source or drain overlap region can be formed at a certain gate applied voltage. Since the inversion layer of carriers is formed at heavily doped semiconductor, a tunneling current can be observed in such a field induced junction. These two combined effects of electric field modulation and

tunneling current injection in the high electric field region lead to unique light emission characteristics. Fabricated in a standard CMOS process technology, silicon p-n junction diodes (source/substrate or drain/substrate) and gated p-n junction diodes (gate/source/substrate or gate/drain/substrate) are used in this study to compare their light emission characteristics and device performance. The pn junction diode operating at avalanche breakdown conditions has visible light emission originating from the depletion region as confirmed by 2D device simulation and experimental measurement results. It is believed that this optical radiation comes from carriers generated by impact ionization losing their kinetic energy by colliding with immobile charged centers in the avalanche region. A theoretical model is presented to show the correlation of photonic emission with the electric field strength, also known as the hot carrier effect with the related high electric field. The gated pn junction diode operating at electric field assisted tunneling current conditions has visible light emission originating from the gate/drain or gate/source overlap region as confirmed by 2D device simulation and experimental measurement results. Both pn junction diode and gated pn junction diode exhibits a linear dependence of light emission intensity on the device terminal current. The only difference between them is that the pn junction diode is controlled by the avalanche current initiated by the junction leakage current while the gated diode by the tunneling current. It has been discovered that, at the same terminal current, the optical output power in gated diode is higher than that in diode, indicating higher quantum efficiency in the gated diode. To compare LED device performance, the electro-optic modulation schemes and speed in the pn diode and the gated diode are analyzed in detail, showing a modulation speed of a few tens of gigahertz

achievable in the gated LED. The gated LED promises its potential in realizing silicon optoelectronic integration.

INTRODUCTION

Silicon photonics has become one of the most promising photonic integration platforms in the last years. This can mainly attributed to the combination of a very high index contrast and the availability of CMOS fabrication technology, which allows the use of electronics fabrication facilities to make photonic circuitry.

Integration of light sources in silicon is considered to be unpractical, since silicon has an indirect band-gap, implying that light-emitting devices (LED) are very inefficient. As one of the candidates of Si-based light emitters, the premier observation on the enhanced light emission from a novel SiO_x/nano-Si-pyramid/Si structure based on Fowler-Nordheim (F-N) tunneling mechanism is demonstrated [1]. In mot cases, the light transmitter is made of III-V group materials on bulk silicon [2], whereas the photo-receiver is a silicon electronic circuit. The hybrid integration with a layer of different material bonded on the silicon chip is very expensive and difficult because of the lattice mismatch at the interface, which causes the formation of defects, but it should be mentioned that III-V integration is already on the ITRS roadmap [3]. A major current problem is that, although this bulk-silicon based LED with emitting wavelength around 1550 nm that is eligible for traditional optical communication show reasonable quantum efficiencies, they are not compatible to CMOS integrated circuit technology.

Being different from the silicon photonics work that is done at wavelengths around 1550 nm, it is observed that visible light emitted from reverse-biased silicon p-n junctions at highly localized region where avalanche breakdown is taking place has been, for the first time in the world, reported by Newman in 1995 [4]. Visible light with a typical spectral distribution curve in the wavelength range of 365 to 689 nm is emitted by silicon p-n

junctions both in avalanche breakdown and in breakdown by internal field emission [5]. Several physical mechanisms regarding the type of light generation were proposed in [6–10]. One of the most important advantages is the Si-diode LED (i.e., a reverse-biased silicon p-n junction) is fully integrated with relevant silicon integrated circuits and is fully compatible with the standard Si-CMOS process technology [11].

Since the Si-diode LED is a two-terminal device in which the light intensity is controlled by the relatively high avalanche diode current, the modulation of light intensity is related to loading the driving circuits. As an improvement, a three-terminal Si LED (i.e., Si gate-controlled-diode LED named TRANSLED) has been fabricated and investigated, in which the control of the avalanche current and the light emission intensity is performed via the injection of carriers into the avalanche region through the adjustment of gate voltages. In other word, the TRANSLED device current and thus the light intensity is controlled by an insulated gate terminal voltage V_g, so a number of signal processing operations that can not be achieved with the two terminal Si-diode LED are enabled [12].

In general, the silicon diode LED is an avalanche-based LED, whereas the silicon gate-controlled diode MOS-like LED is field-emission-based LED. A discussion of the differences observed between avalanche and field emission LED performance is presented in [13].

In practice, the light emission observed in the reverse-biased silicon p-n junctions is attributed to the hot-carrier population under the condition of avalanche breakdown, which can be used for high-speed light-emitting devices, high-speed light amplifiers, and the analytic investigation of hot carrier distribution. Further, Kamieniecki defined that the mechanism of such photonic emission was Bremsstrahlung radiation [14]. Such radiative

phenomenon was also found in MOSFET working in saturation mode with avalanche breakdown occurring at the corner of "substrate to drain" junction [15]. Tam and Hu [16] had proven that the avalanche-breakdown-induced photonic emission occurring in NMOSFET and CMOS belongs to Bremsstrahlung radiation in theory by calculation. Some of these photons with high energy will be absorbed by silicon material to generate photoinduced current. Takeda *et al*. demonstrated the existence of that current by finding the paradox between theory and measurement for the dependence of the correlation of gate current with substrate current on temperature [17], [18]. The photoinduced current also makes the carriers have a longer diffusion length and a longer life time [16]. Toriumi also measured photon energy emitted from near the drain and investigated the relationship between hot-carrier effects and electron temperature [19]. The energy distribution function of photon intensity is given by

$$f(E) = C\exp(-E/kT_e) \tag{1}$$

which is similar to that of lucky electron model [20], Maxwell-Boltzmann distribution, and ionization rates for electrons and holes in depletion region of silicon p-n junction [21]– [23]. The same result was also reported by Tao *et al.* [24].

In addition to the Si-diode LED, a silicon p-channel metal oxide semiconductor field effect transistor LED (Si-PMOSFET LED) which can function as electro-optic modulator is proposed, fabricated, and analyzed in [25]. It is important to note that the PMOSFET device is able to work as two identical gate-controlled diodes (i.e., the p^+ source to n-substrate and p^+ drain to n-substrate junctions with varying gate voltage V_g) if the substrate voltage is of a fixed value, if drain and source are grounded, and if the gate voltage is a variable.

The dissertation is organized as follows: Chapter 1 provides the theory and design of the silicon light-emitting device (i.e., a device with the physical structure of PMOSFET), with the simulation results regarding the electric characteristics occurring in the semiconductor device itself; Chapter 2 introduces the experimental procedure/design and the FET device layout/implementation. Next, in Chapter 3 it presents the experimental results and the discussions on these experimental results; the significance of the Si-PMOSFET LED is reviewed by simulating the dependence of breakdown voltage BV of the p+ source/drain to n-substrate junction on gate voltage V_g, BV decreases with increasing V_g, so reverse current flowing through the p^+ n junction increases with V_g; since light emission is linearly related to the reverse current, the reduction in BV can explain why light emission intensity increase with V_g; The physical mechanism that is probably related to the photon emission is further investigated to prove such linearity; the results of comparison of spectrum and quantum efficiency under different biasing conditions are also given. In Chapter 4, details of the optical intensity modulation using gate-terminal in order to further investigate the application of the three-terminal silicon gate-controlled diode as electro-optic modulator; since the current injection (modulation) efficiency is dependent on the carrier lifetime and a shorter carrier lifetime corresponds to a higher speed, the tradeoff between speed and modulation efficiency is carefully analyzed, thus making the reverse-biased configuration of the avalanching light emitting junction offers modulation capabilities of the silicon device to within the GHz range. Finally, conclusions and future work are drawn in Chapter 5.

CHAPTER 1: Theory and Design of the Silicon P-N Junction Device

P-N junction diode is of great importance both in modern electronic applications and in understanding other semiconductor devices. The first section of the chapter is used to develop the ideal static characteristics of p-n junctions, especially the junction breakdown due to avalanche multiplication, is considered in detail, after which some of the important simulation results regarding the electronic characteristics are presented. It is noted that p-n junction diode is a two-terminal device that can perform various terminal functions depending on the doping profile, device geometry, and biasing condition. Gate-controlled diode, with the metal-insulator-semiconductor (MIS) capacitor, is the most useful device in the study of semiconductor surfaces. Actually, a Si-PMOSFET device is comprised of two identical p-n junctions connected in parallel if the substrate voltage V_{sub} is greater than 0 V, if the source and drain terminals are connected to the ground (i.e., V_d = V_s = 0 V), and if the insulated-gate is floated (i.e., without applying gate voltage V_g). On the other hand, the device can work as two identical gate-controlled diodes in parallel if it operates as follows: source and drain are connected to the ground (i.e., V_d = V_s = 0 V), substrate voltage (i.e., V_{sub}) is a certain value, and the gate voltage V_g is the variable. Simulation is implemented by the 2-D device simulator MEDICI [26].

1.1 Silicon p-n junction diode

The avalanche breakdown occurring in p-n junction diode in the Si-PMOSFET device is simply presented in both Fig. 1.1. The numerical calculations show that the breakdown voltage (*BV*) of the "P^+ Source/Drain to N-Substrate" junction is about 30 V. It is noted that above mentioned *BV* is a breakdown voltage used to denote soft breakdown in which the

multiplication factor *M* is a limited value. A "soft" reverse current-voltage characteristic in comparison with the corresponding "hard" breakdown characteristic in which *M* is approaching infinity is illustrated in [27]. The transition from soft breakdown to hard breakdown produces the evidence that a large excess reverse current, which is due to localized breakdown in small high-field regions around metallic precipitates present within the crystal, already flows through this diode at reverse voltages well below the avalanche breakdown voltage.

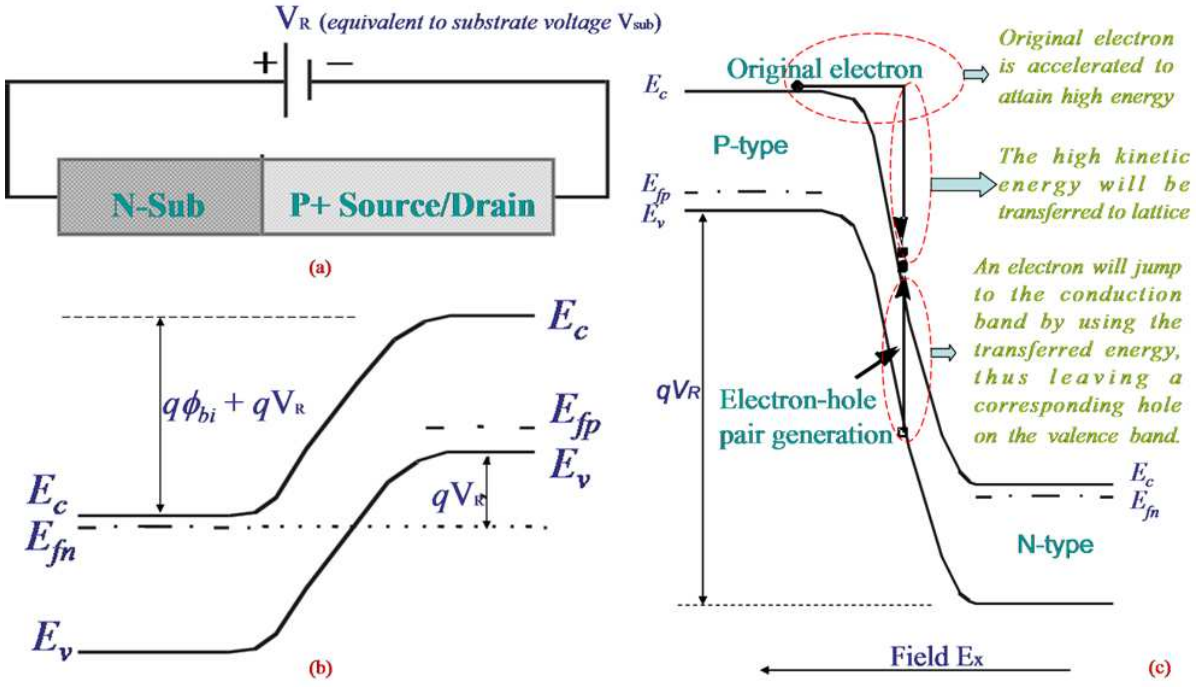


Fig. 1.1 One-half of the Si-PMOSFET: (a) Schematic diagram; (b) Energy-band diagram; (c) Impact ionization in which an energetic electron generates a new electron-hole pair.

Since the threshold voltage V_t of the PMOSFET is in the range -1.5 V to -2.0 V and the thickness of SiO_2 layer ranges from 400 Å to 500 Å, a detailed deduction based on the

empirical threshold voltage formula is presented in Fig. 1.2. For a one-sided p^+ n abrupt-junction, the critical field for avalanche breakdown is given by

$$\mathrm{E}_{BR}(T) = \sqrt{\frac{2qN_d}{\varepsilon_{si}}[BV(T)]} \tag{1. 1}$$

where q is the elementary charge, N_d is the background doping concentration, and ε_{si} is the permittivity of silicon. Assuming that the electric field is a fixed value and the impact ionization rate is taken into consideration, the breakdown voltage at room temperature can be approximately expressed as

$$BV = 60\left(\frac{E_g}{1.1}\right)^{1.5}\left(\frac{N_d}{10^{16}}\right)^{-0.75} \tag{1. 2}$$

Since N_d is the doping concentration at the surface of the n-type substrate of the Si-PMOSFET device, the *BV* of this one-side abrupt p-n junction (i.e., "P^+ Source/Drain" to "N-Substrate" junction) with the background doping concentration of 2.5×10^{16} cm^{-3} at the surface is accordingly equal to 30 V [28].

$$V_t = V_{fb} + 2\phi_f - \frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} \sqrt{\frac{4qN_d}{\varepsilon_{si}\varepsilon_0}\left(-\phi_f\right)}$$

For n-type substrate with the doping concentration of 2.5×10^{16} cm^{-3},

Buck potential:

$$\phi_f = -\left(\frac{kT}{q}\right)\ln\left(\frac{N_d}{n_i}\right) = -(0.026)\ln\left(\frac{2.5\times10^{16}}{9.65\times10^{9}}\right) \approx -0.384V$$

Background doping concentration

Surface potential of substrate at threshold:

$$\phi_s = 2\phi_f \approx -0.768V$$

Voltage drop across SiO_2 layer:

$$V_{ox} = -\frac{Q_{ox}}{C_{ox}} = -\frac{\varepsilon_{si}}{\varepsilon_{ox}} t_{ox} \sqrt{\frac{4qN_d}{\varepsilon_{si}\varepsilon_0}\left(-\phi_f\right)} = -\frac{11.8}{3.9} t_{ox} \sqrt{\frac{4\times\left(1.6\times10^{19}\right)\times\left(2.5\times10^{16}\right)}{11.8\times8.854\times10^{-14}}\times 0.384}$$

Flat-band voltage:

$$V_{fb} = -\left(\frac{E_g}{2q} + \phi_f\right) = -(0.56 - 0.384) = -0.176V$$

For

$$t_{ox} = 400\times10^{-8}\,cm$$

$$V_t = (-0.176) + (-0.768) + (-0.928) = -1.872V$$

For

$$t_{ox} = 500\times10^{-8}\,cm$$

$$V_t = (-0.176) + (-0.768) + (-1.16) = -2.104V$$

Calculated range of threshold voltage Vt

Fig. 1.2 Numerical calculations of breakdown voltage of the "P+ Source/Drain to N-Substrate" junction

The above discussion can be further verified by a two-dimensional (2-D) device simulator, and the simulated current-voltage (*I-V*) characteristics are shown in Fig. 1.3(a). Source and drain are always grounded (i.e., $V_d = V_s = 0$ V). With gate floated, the Si-PMOSFET device will work as Si-diode LED in which "P^+ Source to N-Substrate" junction diode and "P^+ Drain to N-Substrate" junction diode are connected in parallel. As shown in Fig. 1.3(b), the reverse current flows through the "P^+ Source/Drain to N-Substrate" junction uniformly.

The electric field is schematically presented in Fig. 1.4 clearly, and the details of field distribution at different reverse-biases are presented in Fig. 1.5. Peak electric field occurs at the interface of "P^+ Drain to N-Substrate". It is noted that visible light is emitted from reverse-biased silicon p-n junctions at highly localized regions where avalanche breakdown is taking place. Critical field values calculated from measured avalanche breakdown voltages in silicon are shown in [28] as a function of the impurity concentration of the substrate of one-sided abrupt-junctions. Normally, avalanche breakdown occurs when the peak electric field in the p-n junction reaches a critical value below $\sim 10^6$ V/cm. Although the reverse-bias of the "P^+ Drain to N-Substrate" junction is as high as 51.2 V, simulated results shows that the field is still less than $\sim 10^6$ V/cm which implies the evidence that avalanche breakdown is the prerequisite for light emission from reverse-biased p-n junctions.

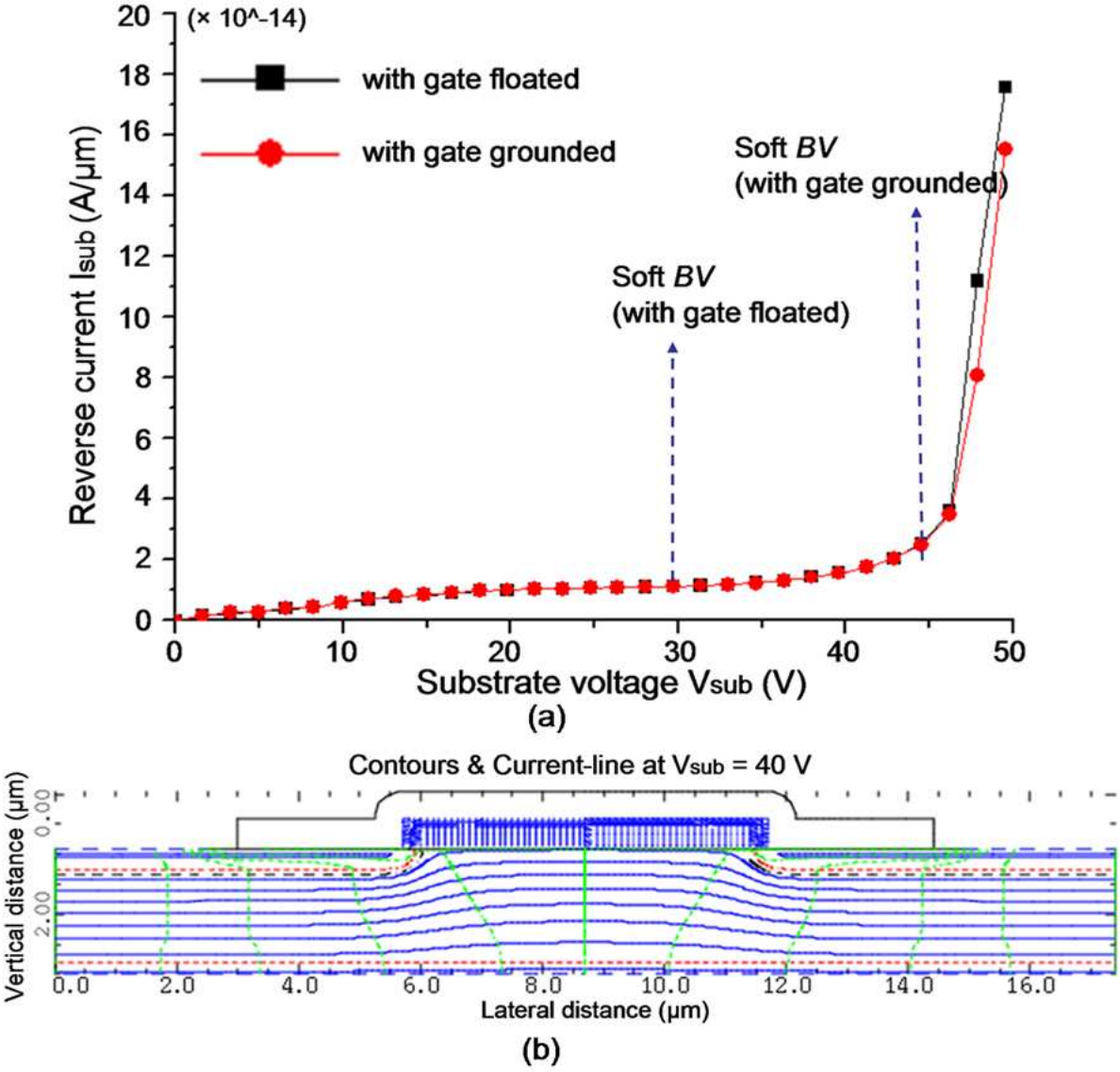


Fig. 1.3 Simulated electric characteristics of Si-diode in PMOSFET device: (a) *I-V* characteristics of the Si-PMOSFET LED in both Si-diode and Si gate-controlled-diode modes; (b) The distribution of electric potential (in blue) and the patch of reverse current I_{sub} (in green) on the following biasing conditions: substrate voltage V_{sub} = 40 V, $V_d = V_s$ = 0 V, and with gate floated.

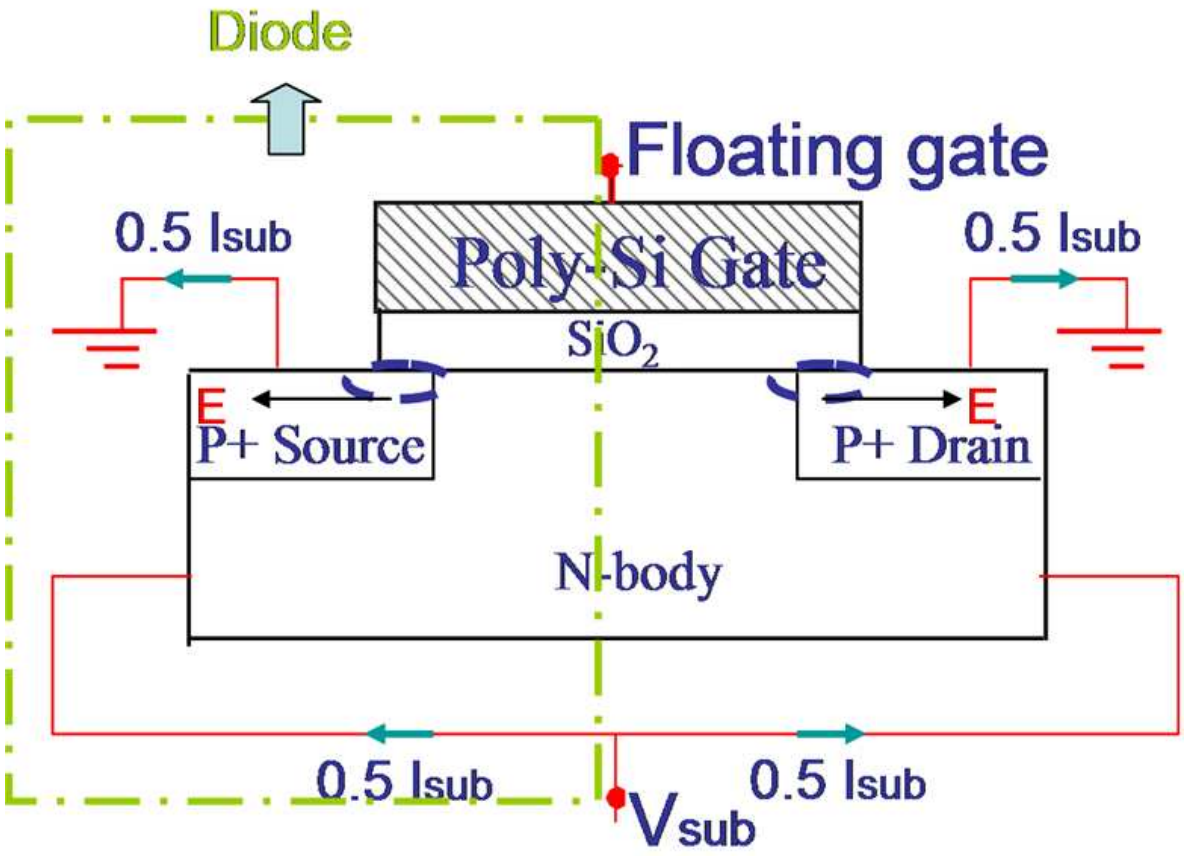


Fig. 1.4 The Si-PMOSFET device operates in the diode mode

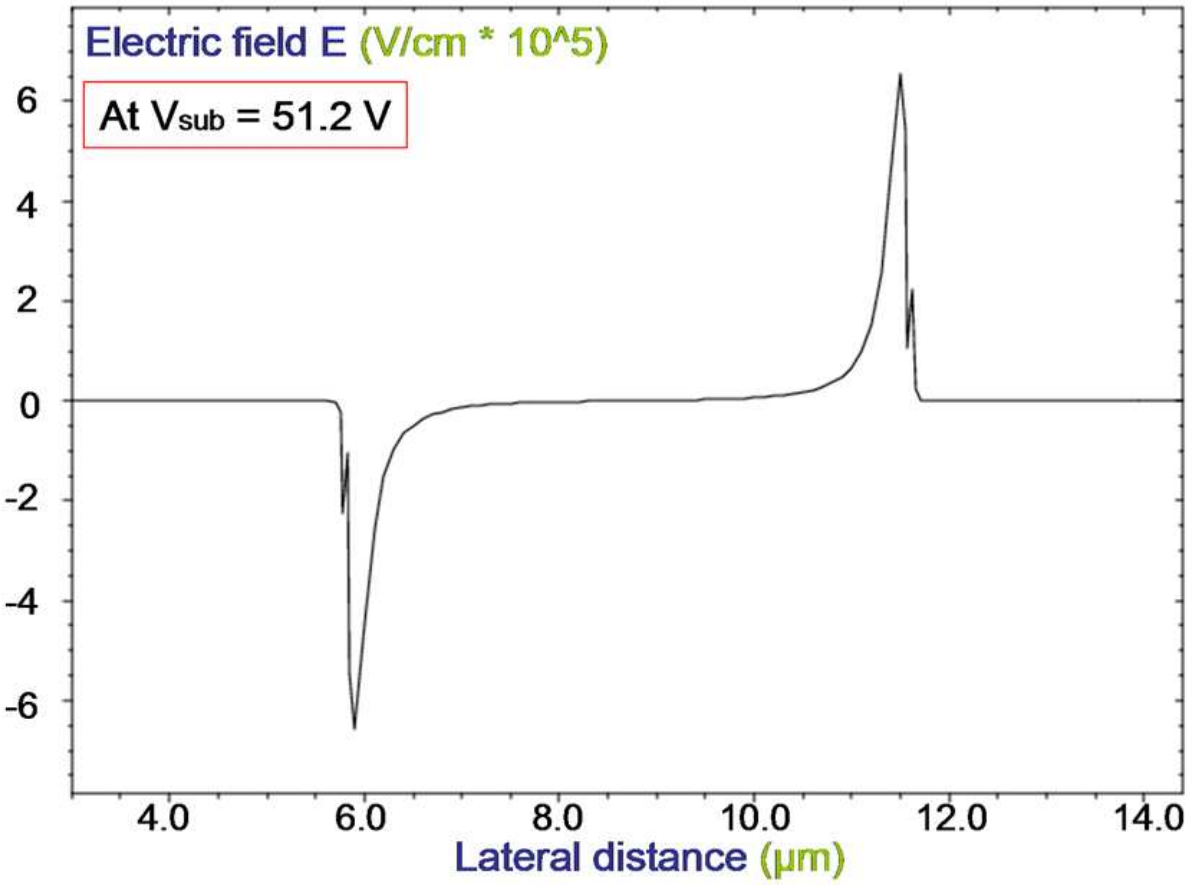


Fig. 1.5 The field distribution along the surface of the Si-diode LED while the Si-PMOSFET device is operating at: V_{sub} = 51.2 V, $V_s = V_d$ = 0 V, and with gate floated.

1.2 Silicon gate-controlled-diode

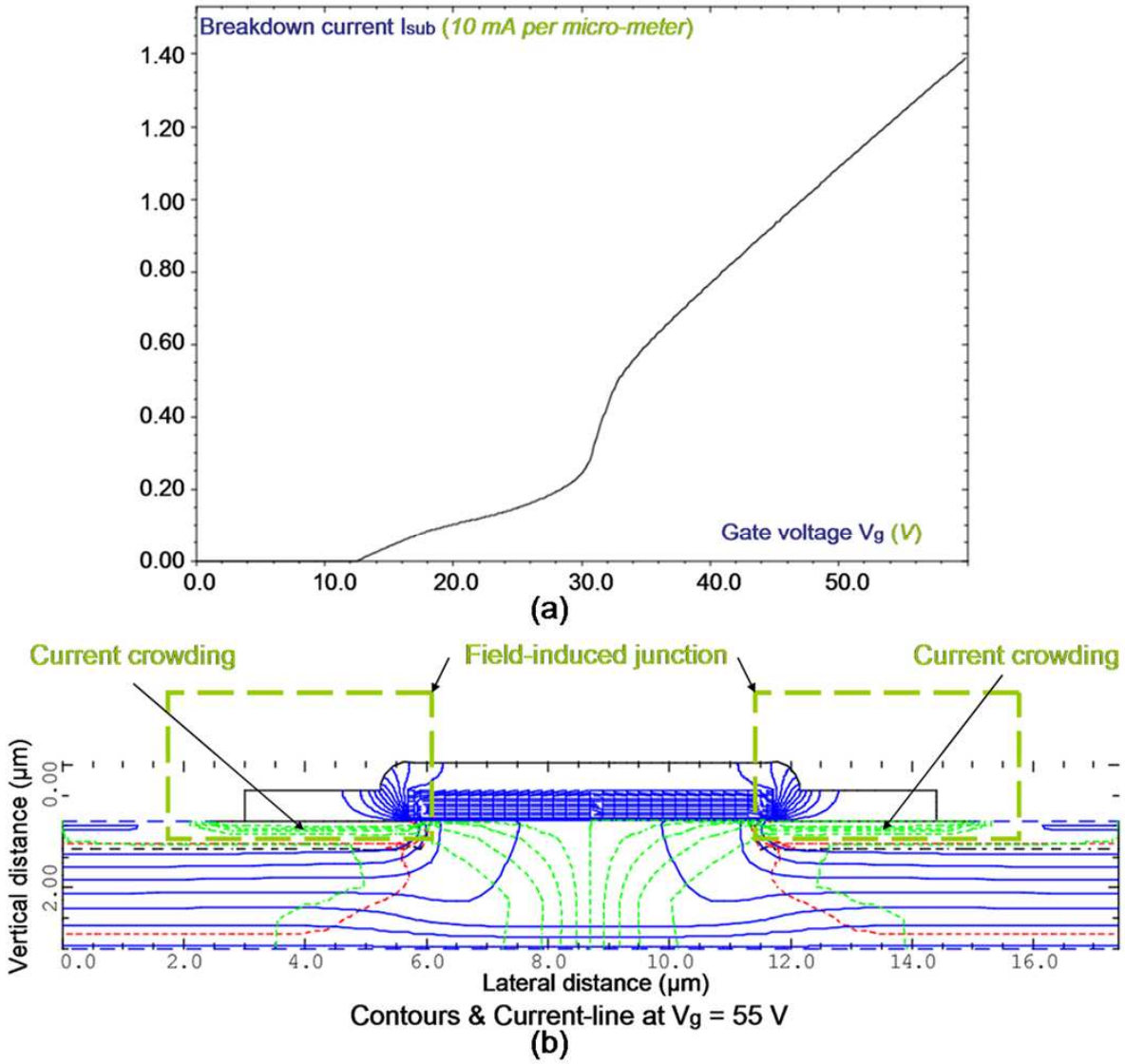


Fig. 1.6 Simulated electric characteristics of Si gate-controlled-diode in PMOSFET device: (a) Simulated *I-V* characteristics of the Si-PMOSFET LED in the Si gate-controlled-diode mode; (b) The distribution of electric potential (in blue) and the patch of reverse current I_{sub} (in green) on the following biasing conditions: gate voltage V_g = 55 V, substrate voltage V_{sub} = 35 V, and $V_d = V_s$ = 0 V

The simulated current-voltage (*I-V*) characteristics of the two parallel-connected Si gate-controlled-diodes LED are illustrated in Fig. 1.6(a). With gate voltage V_g applied, the Si-PMOSFET device will work as Si gate-controlled-diode LED in which "P^+ Source to N-Substrate" junction diode and "P^+ Drain to N-Substrate" junction diode are connected in parallel under the control of V_g. As shown in Fig. 1.6(b), the reverse current flowing through the "P^+ Source/Drain to N-Substrate" junction is non-uniform.

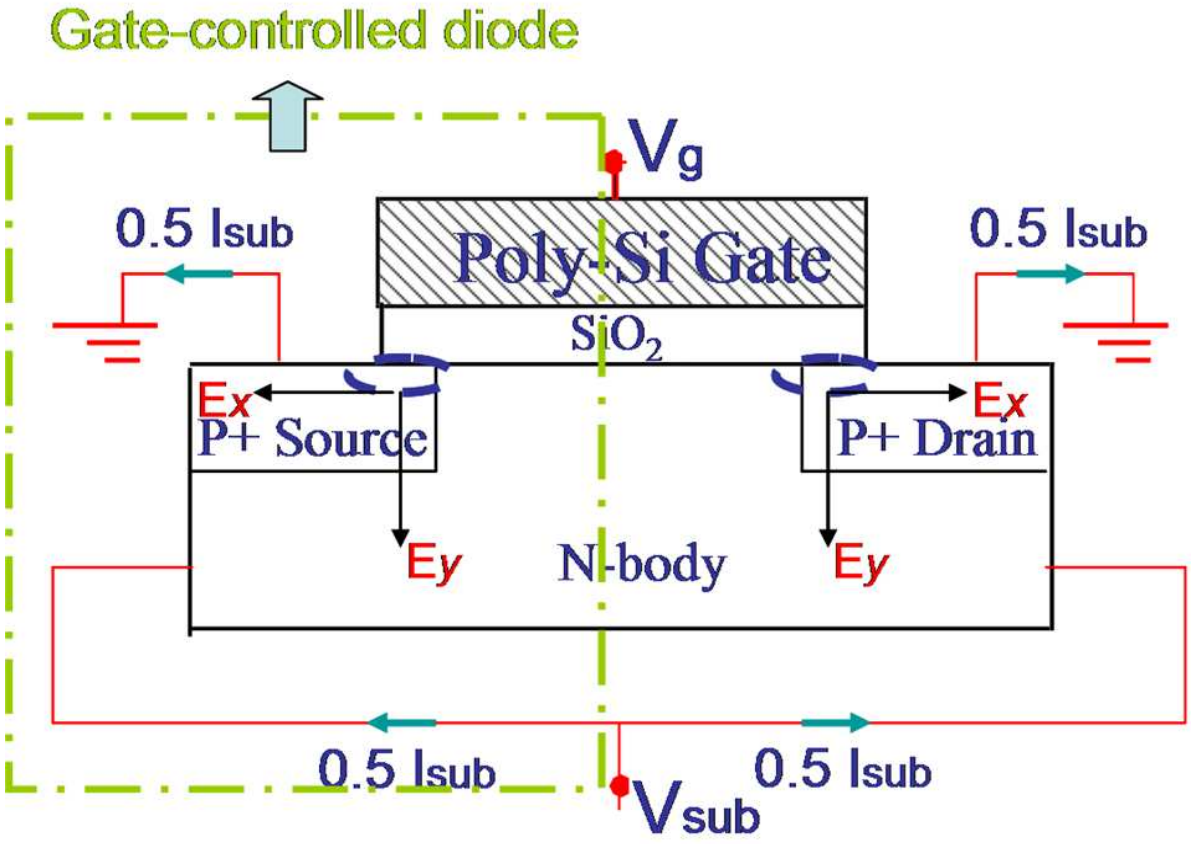


Fig. 1.7 The Si-PMOSFET device operates in the gate-controlled diode mode

Because of the increase in V_g, there will be a so-called field-induced junction generated in the overlap region of "P^+ Source/Drain to Gate" just underneath the gate. The field-induced junction build-up is important because it results in a variation of the "P^+ Source/Drain to N-Substrate" junction breakdown voltage *BV* as a function of gate voltage V_g, leading to the lower *BV* in the "P^+ Source/Drain to Gate" overlap region than in the central section of the "P^+ Source/Drain to N-Substrate" junction [29]. This, in turn, results in the higher current density near the overlap region. This condition is referred to as current crowding.

Furthermore, the lateral field in the Si gate-controlled-diode LED, which is induced by the reverse bias V_{sub}, is a constant. Meanwhile, the vertical field in this LED, which is introduced by gate voltage V_g, is varied to change the field distribution in the device. The two fields are schematically presented in Fig. 1.7 clearly, and the total field is approximately equal to $E = \sqrt{E_x^2 + E_y^2}$. Due to the combination of two different types of electric field, the breakdown mechanism occurring in this Si-PMOSFET LED tends to be a mixture of avalanche breakdown and Zener breakdown that is too complicated to be solved only by the above mentioned field-analysis of p-n junction.

More specifically, since the voltage drop of Gate-to-Drain/Source is determined by V_g, a positively increased V_g tends to attract more electrons to the surface of drain/source region that is underneath the gate. In result, the "Drain/Source to Gate" overlap region will be depletion of holes, and continue to approach the inversion layer status. The P^+ Source/Drain with the overlap region will constitute a p^+ n^{++} diode that is parasitic on this gate-controlled diode. In other words, the breakdown mechanism is transiting from

avalanche breakdown to Zener breakdown due to the leakage current induced by tunneling.

Accordingly, both the electric field E and the reverse current I_{sub} which is linear with optical emission power could be modulated by the gate voltage V_g. Although electric field is one of the most important parameters of investigating the modulation of light intensity by the insulated-gate terminal, the field distribution existed in the Si gate-controlled-diode LED is impossible to be captured by experimental measurement directly. To further clarify the profiles of field distribution, the two-dimensional (2-D) semiconductor device simulation tool, Avanti-Medici, is applied to obtain the details of electric field at different gate voltages, as indicated in Fig. 1.8.

As discussed before, in the gate-controlled-diode mode, there may be a tunneling current as a part of the reverse current I_{sub}. At the same time, the relationship between the tunneling current density J and the electric filed E is expressed as [30]

$$J = G\exp\left(-\frac{H}{\mathrm{E}_{crit}}\right) \tag{1.3}$$

where G and H are constants for a given semiconductor, and the critical field E_{crit} is about 10^6 V/cm for silicon material. It should be pointed out that, the values of field, as shown in Fig. 1.7, on the order of 10^6–10^7 V/cm imply the concurrence of avalanche breakdown and tunneling. In particular, tunneling can take place only if the electric field is very high, and it is experimentally found that the critical filed E_{crit} at which tunneling becomes probable, i.e., at which *Zener breakdown* commences, is approximately 10^6 V/cm [31]. Simulated results indicate that, in the Si-PMOSFET device, the maximum field corresponding to the reverse current I_{sub} is uniformly distributed across the active region

of "P^+ Source/Drain to N-Substrate" junction in the mode of Si-diode LED, but that the distribution of maximum field with the reverse current I_{sub} in Si gate-controlled-diode LED is non-uniform because of the existence of the field-induced junction in the "P^+ Source/Drain to Gate" overlap region.

The above mentioned theory and design will be used for the analysis of the two-terminal silicon p-n junction diode LED (Si-diode LED) and for the analysis of the three-terminal silicon gate-controlled-diode LED (Si gate-controlled-diode LED) in the next chapters.

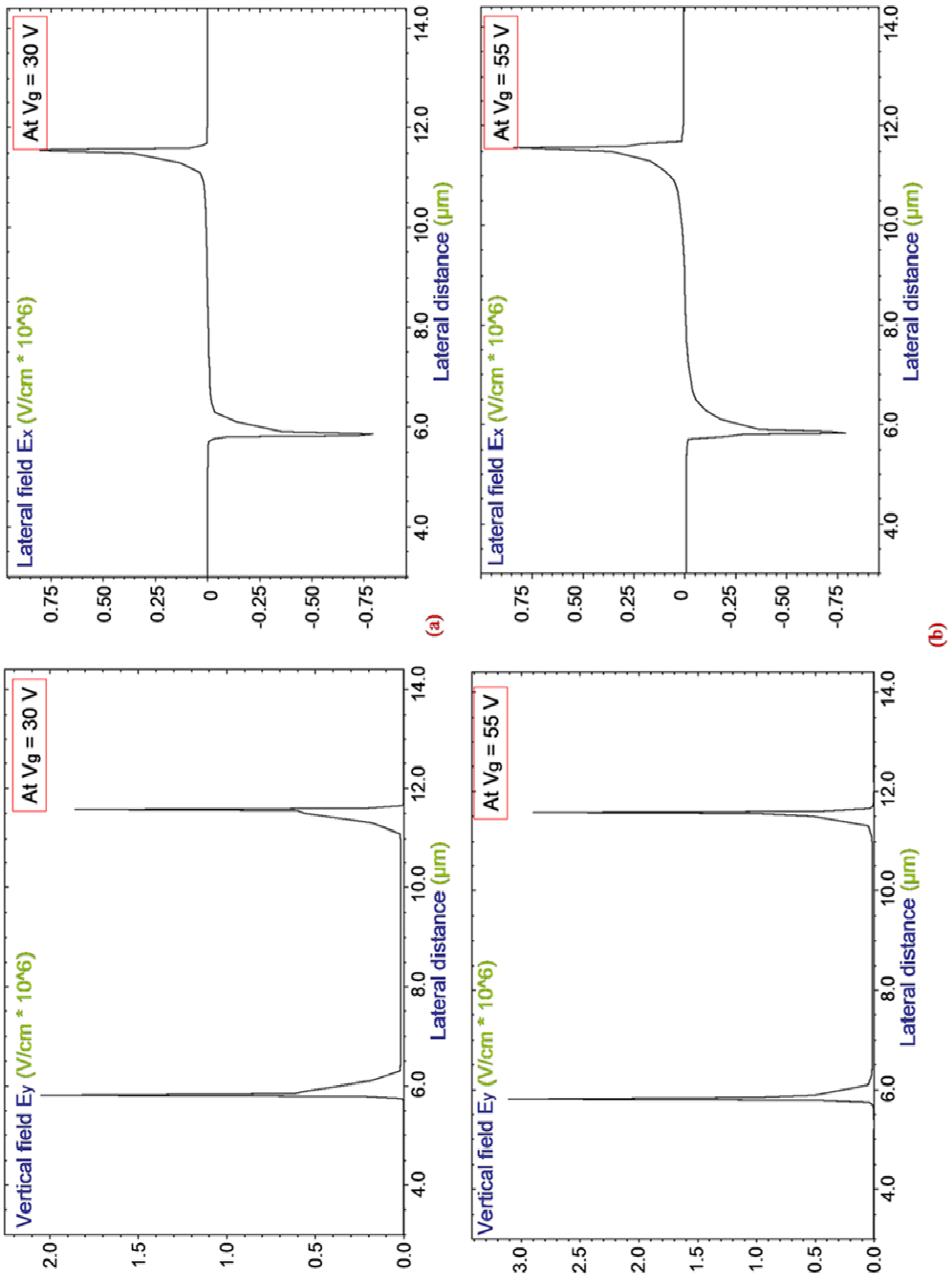


Fig. 1.8 The field distribution along the surface of the Si gate-controlled-diode LED while the Si-PMOSFET device is operating at: (a) V_g = 30 V, V_{sub} = 35 V, and V_s = V_d = 0 V; (b) V_g =55 V, V_{sub} = 35 V, and V_s = V_d = 0 V

CHAPTER 2: Design and Fabrication of the Device

A simplified cross-sectional view of a p-channel metal-oxide-semiconductor field-effect-transistor (PMOSFET) is shown in Fig. 2.1. Layout design with Design Rules Check (DRC), EXTraction (EXT), and Layout Versus Schematics (LVS) was done by Cadence Virtuoso®. Fig. 2.2(a) shows a PMOSFET with blue strip for the poly gate and the external square n^+ guard ring for substrate ohmic contact. The contact holes are patterned and etched into the wafer. A 3μm-wide contact has been used on both the source and the drain of the PMOSFET. Distance between the edge of contact metal and the edge of poly gate is 3μm [32].

Standard 3μm CMOS process with self-aligned technology is utilized for the device fabrication. The starting wafer is an n-type <100> Si with resistance of 0.8–1.2 Ω•cm, thickness of 525 ± 25 μm, and diameter of 100 mm. Typical processes are introduced as follows. Well drive-in is done in the ambient of 1 hour N_2, 2 hours O_2, and 4 hours N_2 at the temperature of 1200℃ by implanting boron with dose 10^{13} cm^{-2} and energy 60 keV. In regard to ion implantation, for p ring, it is 3×10^{15} cm^{-2} with 80 keV; for n ring, it is 5×10^{15} cm^{-2} with 80 keV. for p^+ Source/Drain, it is 3×10^{15} cm^{-2} with 80 keV; for n^+ Source/Drain, it is 3×10^{15} cm^{-2} with 80 keV. Annealing is implemented at 850 ℃ for 30 minutes [33].

Final chip (i.e., Fig. 2.3) in which five identical PMOSFETs are connected in parallel is presented in Fig. 2.4. For each transistor in this device, thickness of gate oxide is 400 – 500 Å, thickness of poly-Si gate is 4000 – 5000 Å, and threshold voltage V_t is -1.5 – -2.0 V.

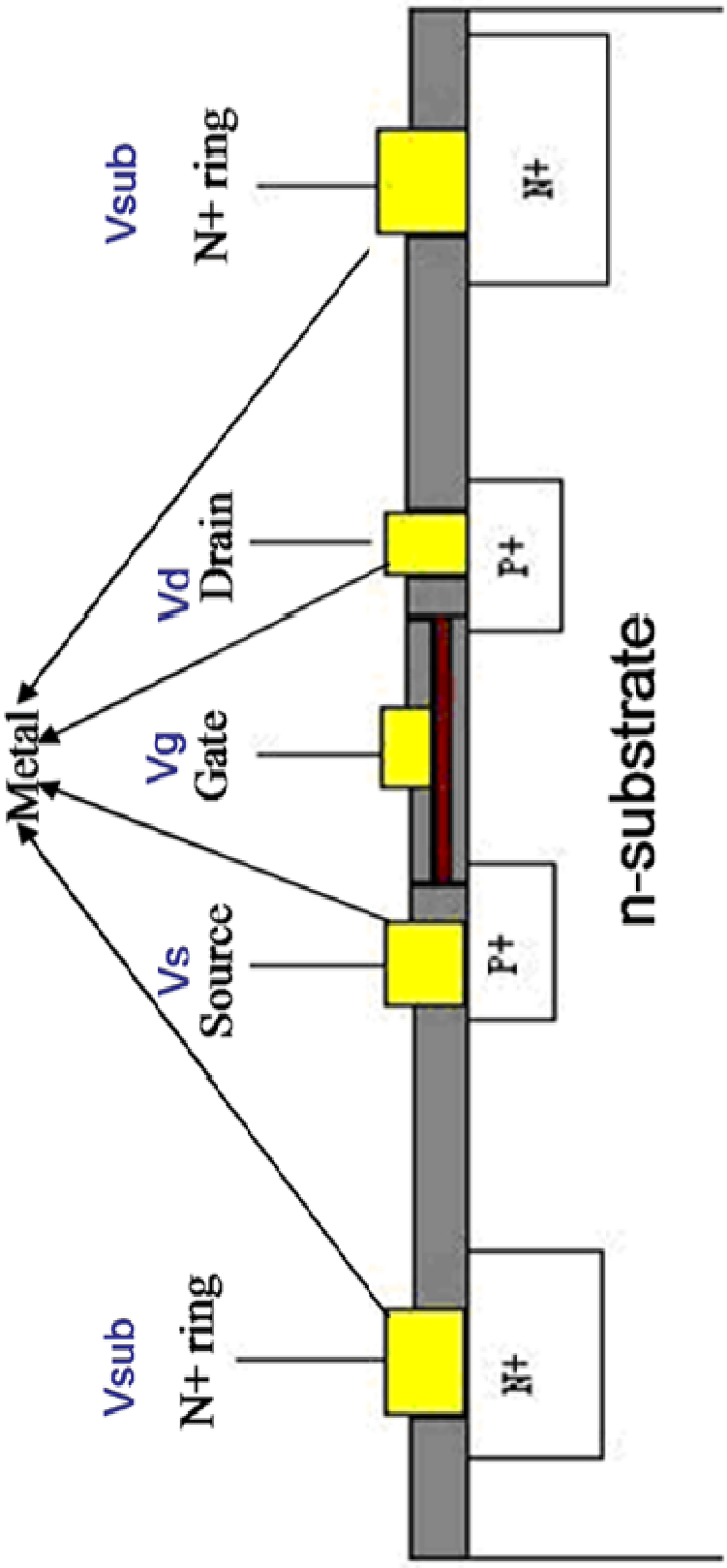


Fig. 2.1 Simplified cross-sectional view of the device structure

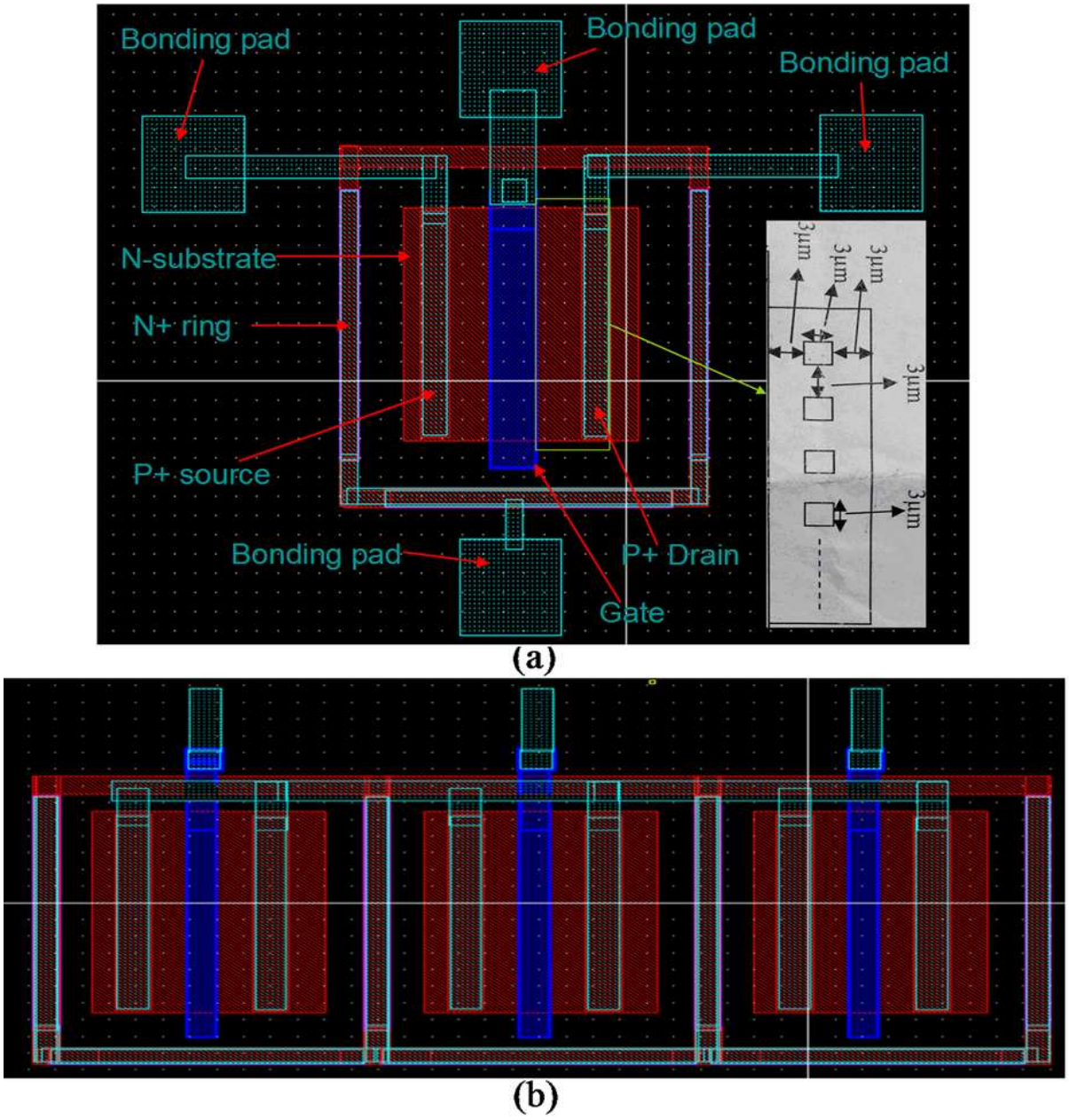


Fig. 2.2 Partial layouts of the PMOSEFT: (a) A single PMOSFET with bonding pads (b) A partial array of PMOSEFT

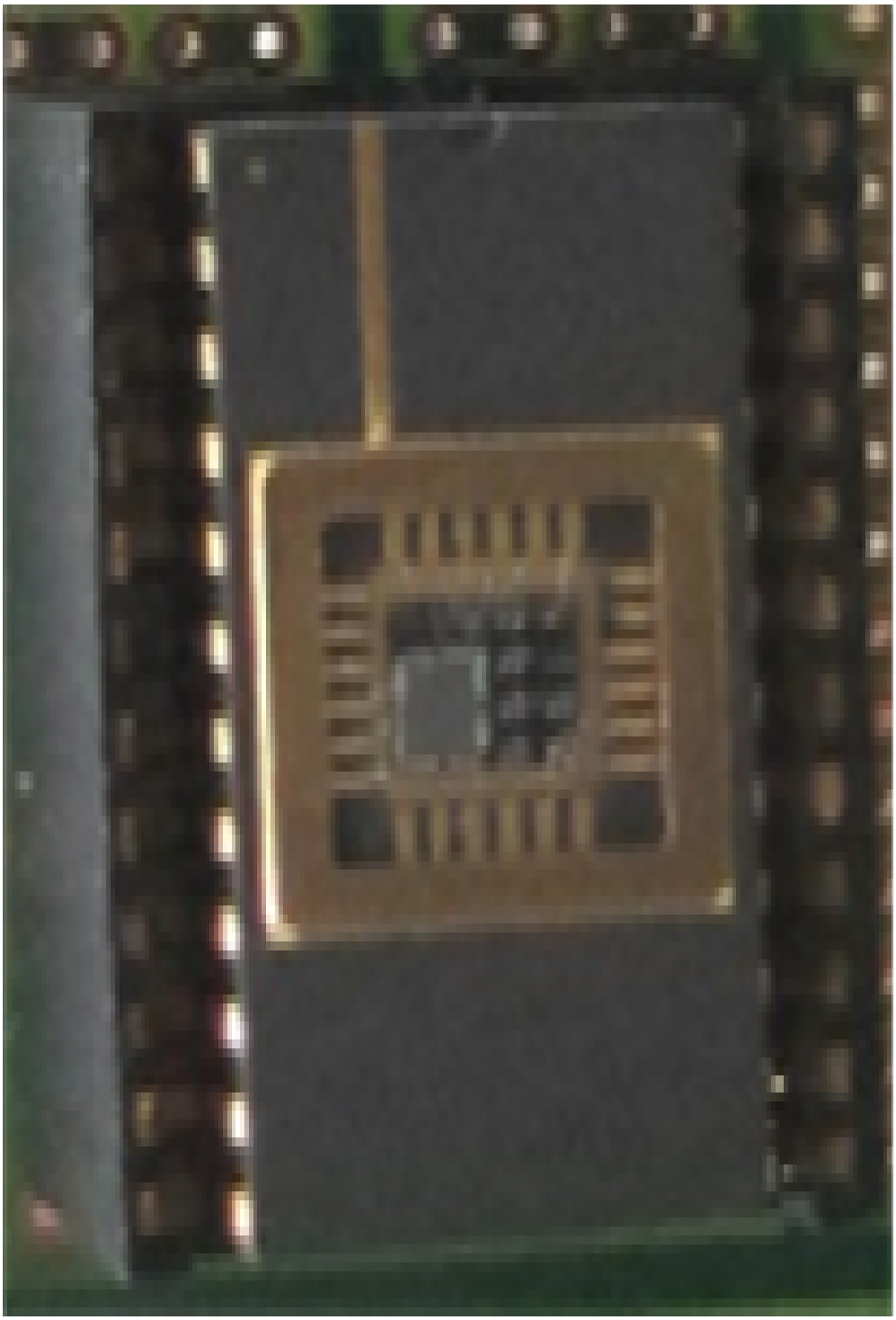


Fig. 2.3 Final Chip

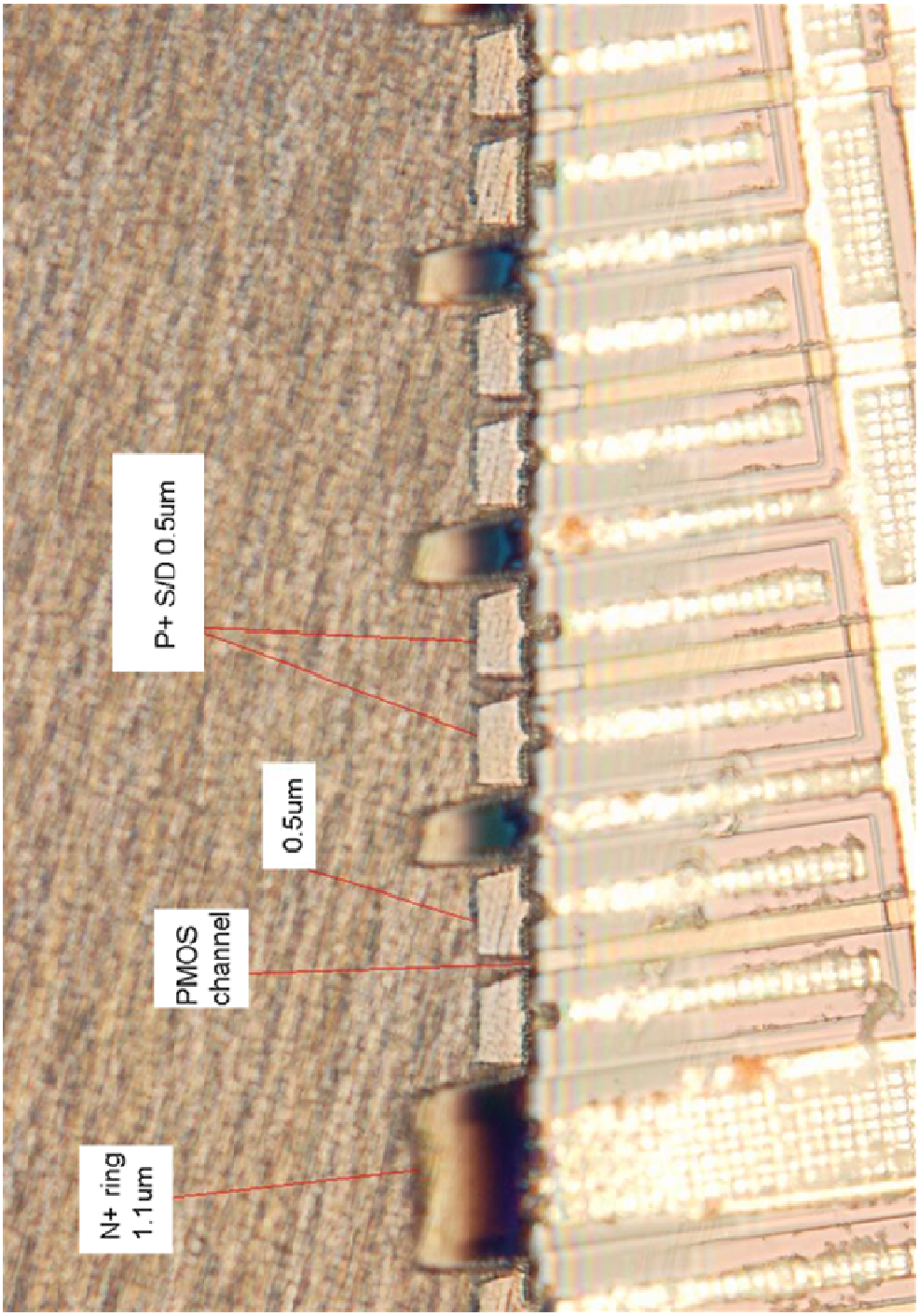


Fig. 2.4 Photomicrograph of the cross-sectional view of the IC cell: 5 PMOSFETs in parallel, for each PMOSFET, gate width: 6 μm, length: 175.5 μm

Indeed, the Si-PMOSFET device can be treated as two identical gate-controlled diodes in parallel. As shown in Fig. 2.1, source and drain are grounded (i.e., $V_d = V_s = 0$ V), the reverse bias of the two p-n junctions is equal to the substrate voltage V_{sub} which is a fixed value. By varying the gate voltage V_g, the channel layer of the PMOSFET can be categorized by the following three types: (a) inversion layer as $V_g = 0$ V < V_{sub}; (b) depletion layer; (c) accumulation layer as $V_g > V_{sub} > 0$ V.

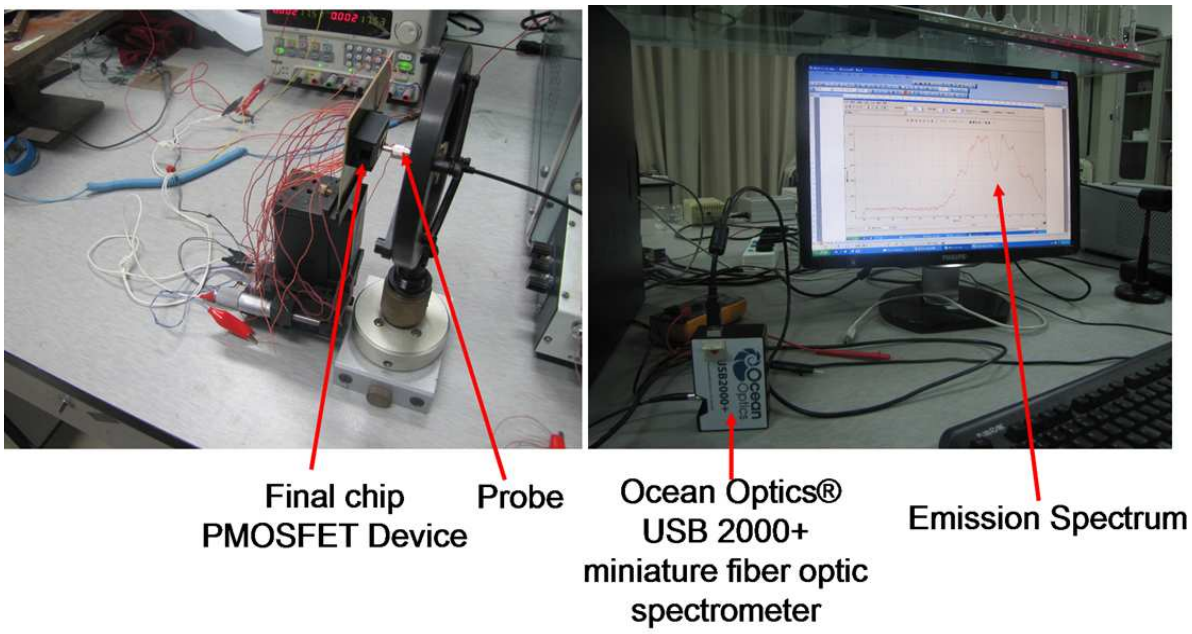


Fig. 2.5 Experimental setup for the light emission measurement

In Fig. 2.5 it shows the experimental setup used for the electroluminescence measurements.

CHAPTER 3: Silicon-based Visible Light-emitting Devices Integrated into Microelectronic Circuits

A silicon-based light emitter compatible with CMOS technology would potentially open the door toward the true integration of micro-photonics and electronics on the scale of a single chip. So far, however, no suitable light source has been found. The most widely investigated options include silicon p-n junction diodes, especially light emission from silicon devices has been realized in reverse-biased p-n avalanche structure about sixty years ago. In this chapter, the original observation of light emission from the reverse-biased p-n junction is reviewed, a proposed device with the MOS-like structure is used to investigate the electrical characteristics and the optical properties of the two-terminal Si-diode LED and the three-terminal Si gate-controlled diode LED, and then a comparison between the two different types of light sources is presented.

3.1 Electrical properties of a p-n junction

The potential barrier height ϕ_{bi}, its width W_D and their variations as a function of the applied bias are determining factors of the behavior of the p-n junction. Assuming the donors of concentration N_D in the n region and acceptors of concentration N_A in the p region are fully ionized, so the concentrations of the n-type and of the p-type semiconductors are approximately equal to N_D and N_A, respectively. Hence, the diffusion voltage ϕ_{bi} in the depletion region is given by

$$\phi_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \tag{3. 1}$$

where n_i is the intrinsic carrier concentration in the semiconductor under study. For silicon, it is of the order of 10^{10} cm^{-3} in the room temperature.

The width of the depletion layer W_D depends on the concentrations N_D and N_A. The higher these concentrations are, the narrower the region of the semiconductor that has to be depleted of free carriers in order to form the diffusion voltage ϕ_{bi}. Therefore, W_D decreases with increasing N_A and N_D. By applying an external bias in the forward direction, the electrons and the holes will return to the n region and the p region, respectively. Consequently, W_D will decrease with increasing the external bias V by the resulting expression below

$$W_D = \sqrt{\frac{2\varepsilon_{si}}{q}(\phi_{bi} - V)\left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \qquad (3.2)$$

Naturally, application of the reverse bias (i.e., V is of a negative value) will have the opposite effect and the depletion layer's width will increase with the reverse bias.

As the depletion region has a high electrical resistance, the applied bias easily decreases or increases the potential barrier height. As mentioned earlier, under forward bias the electrons and holes are injected as minority carriers into the regions of opposite conductivity type, which makes a current flowing across the p-n junction; this current increase with increasing bias. By solving the continuity equation, and taking the generation and recombination mechanisms of carriers into consideration, the current density is given by the Shockley equation below

$$J = qn_i^2\left(\sqrt{D_p/\tau_p}\,\frac{1}{N_D} + \sqrt{D_n/\tau_n}\,\frac{1}{N_A}\right)\exp\left(\frac{qV}{kT} - 1\right) = J_s \exp\left(\frac{qV}{kT} - 1\right) \qquad (3.3)$$

Here, D_n and D_p denote the diffusion coefficient of electron or hole, respectively. τ_n and τ_p stand for the lifetime of electron or hole as minority carrier, respectively. If the external bias V is negative enough to make $\exp\left(\frac{qV}{kT}\right)$ far less than the unity, a current flowing in the opposite direction will no longer depends on the external bias V :

$$J = qn_i^2\left(\sqrt{D_p/\tau_p}\,\frac{1}{N_D} + \sqrt{D_n/\tau_n}\,\frac{1}{N_A}\right) = -J_s \tag{3. 4}$$

, and the current of density J_s is called the saturation current, and far lower than the forward current.

However, if a very high reverse-biased voltage is applied to a p-n junction resulting in sufficiently high electric field, the junction breakdown (e.g, thermal instability, tunneling, and avalanche multiplication) conducts a very large current [34].

3.2 Photon emission from reverse-biased silicon p-n junctions

It has been observed that when low-voltage breakdown silicon p-n junctions are biased in the reverse direction to breakdown that a weak yellowish light is emitted from the junction region. Same studies of this effect are presented in [4].

Various theories have been put forward in order to explain the phenomenon. These include phonon-assisted intraband relaxation phenomena, as well as phonon interband recombination processes [35]. In-depth theoretical modeling and experimental evidence indicated that the dominant photonic generation processes include direct and phonon-assisted inter-conduction band radiation [8].

3.3 Silicon p-n junction diode light-emitting device (Si-diode LED)

To make the PMOSFET device work as p-n junction diodes, both p^+ Drain and p^+ Source are grounded while the gate is floated. Substrate voltage V_{sub} is defined as the reverse bias of the p-n junction diode. In fact, the device is working as two identical p^+ n junction diodes connected in parallel. Measurement of the electroluminescence is carried out with a setup shown in Fig. 3.1.

Ocean Optics USB 2000^+ Miniature Fiber Optic Spectrometer is used for the study of the optical properties observed in this silicon light source. Calibrated CCD detector, which is responsive to 200 – 1100 nm, is positioned immediately above the device in order to collect most of the emitted light. The shape of the spectra and the peaks of emission are basically unchanged under different reverse-bias conditions. Two distinguished wavelength peaks are observed to occur at 650 nm and 750 nm, as shown in Fig. 3.2.

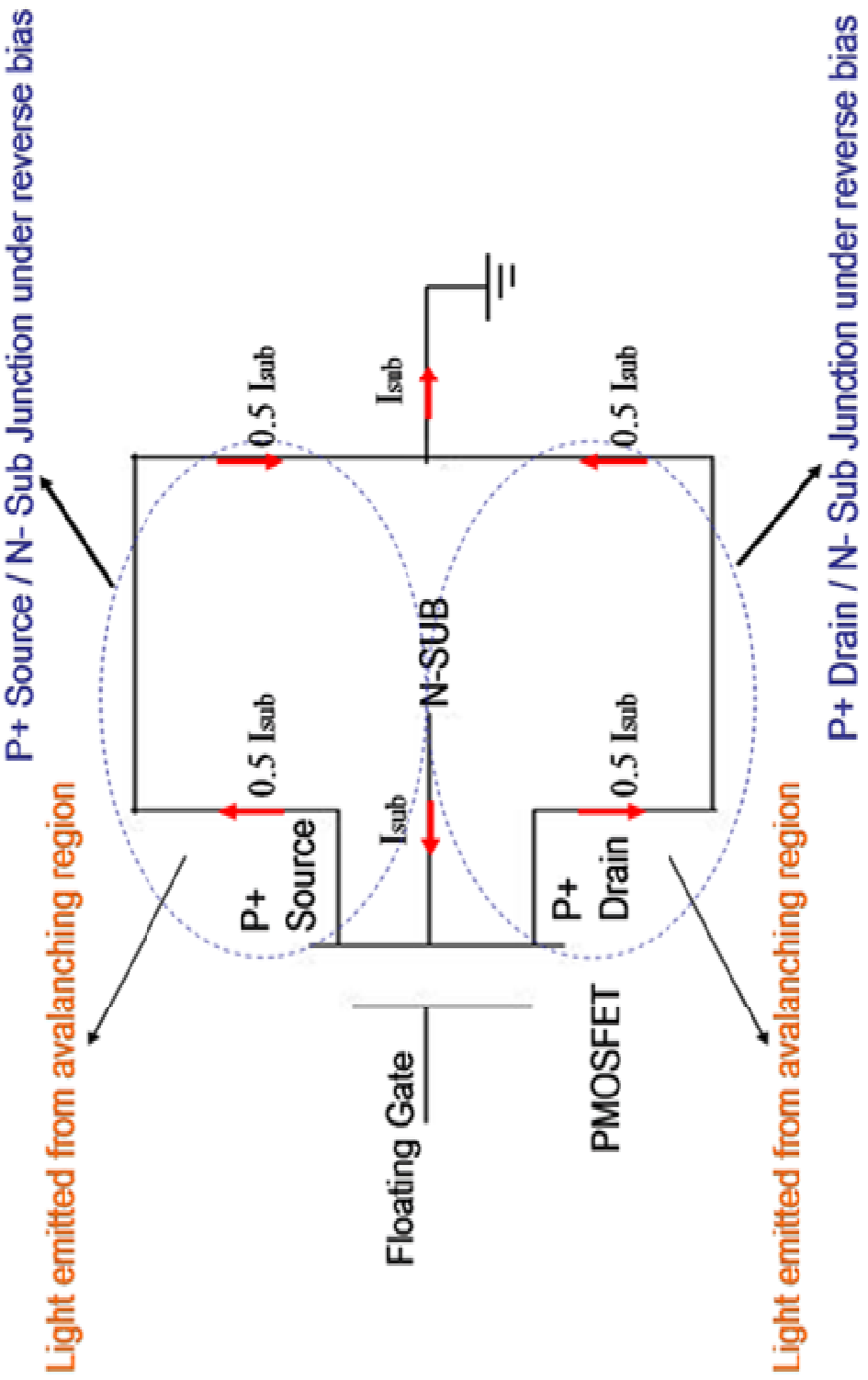


Fig. 3.1 The experimental configuration for measuring reverse current I_{sub} accompanying photon emission in the p-n junctions

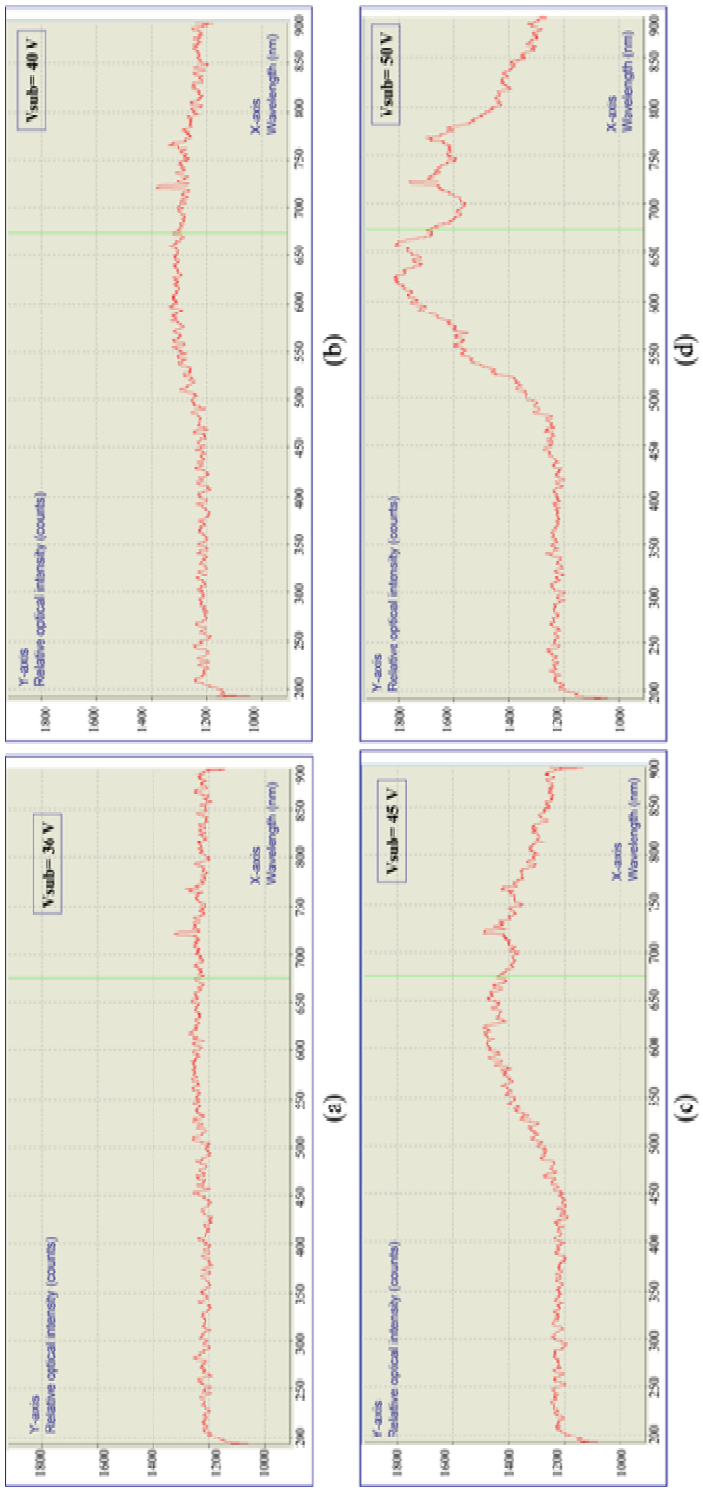


Fig. 3.2 Output emission spectra of the Si light-emitting-device, gate is floated, $V_s = V_d = 0$ V. Emitting wavelength ranges from 500 nm to 850 nm in the measured range of 200 to 900 nm.

Normally, in the microplasma (the prerequisite for the assumption of Braking radiation) or avalanche region of the reverse-biased p-n junction, both the holes and hot electrons are presented up to 2.4 eV (corresponding to wavelength ~550 nm) of the pair production threshold for holes and up to 1.8 eV (corresponding to wavelength ~650 nm) of the pair production threshold for electrons due to high accelerating field [36]. On the other hand, the accelerated carriers will lose some kinetic energies through the collision with artificial atoms (i.e., immobile charged centers) in the depletion region of p-n junction, and the lost energies will be released in the form of photons. On the origin of Bremsstrahlung radiation mentioned previously, the primary wavelength peak 650 nm and the subsidiary wavelength peak 550 nm may be explained by the two threshold values. In fact, the mechanism behind the light emission under the avalanche breakdown condition is extremely complicated, and there are other possible mechanisms contributing to this type of light emission besides Bremsstrahlung radiation. A reasonable model proposed by Akil *et al.* indicates that avalanche emission in silicon longer than ~620 nm is primarily due to indirect interband transition by high-field carrier populations, that Bremsstrahlung (i.e., indirect intraband transition) dominates the range of ~539 nm to ~620 nm, and that direct intraband transition should be the main reason for the photon emission with wavelength shorter than ~539 nm [35]. Accordingly, it is suggested that the overall mechanism is too complicated to be explained by Bremsstrahlung only. The influence of the defects on the localized emitting spots also should be taken into consideration. In addition, the interference of the emitted light by the passivation layer on the surface of the silicon substrate may account for some of the light intensity sub-crests exhibited in Fig. 3.2.

The visible light emitted from silicon p-n junction reverse-biased at high voltages has been studied and analyzed. This hot-electron electroluminescence has been seen to offer a useful mean for the study of high-field effects, device integrity, transport, real-space transfer and electron energy distributions. Examination of the electroluminescence distribution reveals the electrical weak spots of the silicon device and may indicate the presence of localized breakdown. Spectral measurements suggest that a number of mechanisms contribute to the visible light emission, including indirect intraband transitions and band-band recombination. Lacaita *et al.* [9] explained that the light emission processes in avalanching reverse-biased p-n junctions should be due to electron and hole relaxation and recombination processes occurring in the high-field avalanching region in theory. In contrast, from experimental evidence and models, Bude *et al.* [8] concluded that intraband electron relaxation processes of electrons occurring within the conduction band of the silicon itself should be the major reason. It should be noted that a detailed study of the spectrum further allows analysis of the carrier distribution, scattering direction and conduction electron temperature in the space-charge region of silicon p-n junctions.

Commonly, the mechanism of this optical radiation could be explained by the classical electromagnetic theory in which an electron collides with a singly charged Coulombic center. Furthermore, the phenomenon and the rate expression of continuous x-ray spectrum (i.e., Bremsstrahlung radiation) are able to interpret the optical emission observed in the reverse-biased silicon diode if the space-charge region is approximately treated as micro-plasma. It is noted that the x-ray scattering process is distinguished from optical scattering because the energy of the incident x-ray photon with frequency v_0

becomes large enough with respect to the rest energy of the electrons to give a significant frequency shift to the scattered radiation [37]. In fact, the incident carriers generated by impact ionization will be accelerated by the high field in order to collide with the Coulombic charged centers (i.e., artificial atoms [38]), and then the loss of kinetic energy will be released in the form of photons. The ratio of the Coulombic interaction energy to the thermal energy is given by

$$\Gamma_e = \frac{1}{4\pi\varepsilon_{si}} \frac{q^2}{rkT_e} \tag{3.5}$$

where k is the Boltzmann constant, T_e is the effective temperature, ε_{si} is the dielectric constant of silicon, and q is the magnitude of elementary charge. r, which is defined as the inter-particle spacing (i.e., Wigner-Seitz radius), is

$$r = \left(\frac{3}{4\pi n} \right)^{1/3} \tag{3.6}$$

where n denotes the ion density. In accordance with the theory of "hot carrier", the condition for full ionization usually means that the thermal energy of the particles exceeds the ionization energy of the atoms from which the plasma is formed

$$E_{thermal} = \frac{3}{2} kT_e > E_{ion} \tag{3.7}$$

In addition, the lifetime of the excited state is expressed as [39]

$$\tau = \frac{h}{kT_e} \tag{3.8}$$

where h is the Planck constant. Since Coulomb collisions serve for distribution of the reduced velocity of carrier, the variation of velocity is usually written as

$$\Delta v = \frac{hK}{m} \tag{3. 9}$$

where K is the photons wave number and m is the ions mass.

The motion of thermal carriers resembles that of a dilute gas, and the distribution of the kinetic energy of thermal carriers can be described by the Maxwell-Boltzmann distribution, derived from the kinetic theory of gases. The probability of carriers having an energy E is expressed in the form

$$\frac{n(E)dE}{n} = \frac{2\pi\sqrt{E}}{\left(\sqrt{\pi kT_e}\right)^3}\exp\left(-\frac{E}{kT_e}\right)dE \tag{3. 10}$$

where $n(E)dE$ is the number of carriers of energy from E to $E + dE$, n is the total number of carriers in the space-charge region which approximately is gas-microplasma, k is the Boltzmann constant, and T_e is the absolute temperature. This distribution gives an energy corresponding to the most probable velocity, or 0.025 eV at 300 K. The temperature, T_e, associated with a Maxwell's distribution of a carrier population, is also called the "carrier temperature".

Using Maxwell's equation in which the particles are the sources for current and charge distribution, the exact field at the position of the particle can be obtained from self-consistent calculation. Consequently, the kinetic equation becomes

$$\frac{\partial f_\alpha}{\partial t} + \vec{v} \bullet \nabla f_\infty + \frac{q}{m}\left(\vec{\mathrm{E}} + \vec{v} \times \vec{\mathrm{B}}\right) \bullet \nabla_v f_\alpha = \left(\frac{\partial f_\alpha}{\partial t}\right)_{coll} \tag{3. 11}$$

where the left hand side contains only averaged quantities and the so-called collision terms on the right hand side contains all microscopic interactions [40]. In general, the existence of radiative elastic collisions (*Bremsstrahlung*) is the scattering of an electron by an external

field, accompanied by the emission of a photon. Considering charge-charge or charge-neutral elastic collisions, the collision frequency is calculated as follows. The collision time $\tau = \frac{1}{\nu}$ is the time for a charge to experience a significant deflection (i.e., change in momentum). The equation of conversion of momentum for the species α is obtained by multiplying Eq. (3. 11) by $m v_\alpha$ and then integrating over v_α. The collision term for momentum transfer can be evaluated for drifting Maxwell distribution functions, and it is found that

$$\int_{-\infty}^{+\infty} dv_\alpha m v_\alpha \left(\frac{\partial f_\alpha}{\partial t}\right)_{coll} = \sum_\beta m_\alpha n_\alpha \nu_{\alpha\beta} \left(\mu_\alpha - \mu_\beta\right) \tag{3. 12}$$

where μ_α and μ_β are the drift velocities of species α and β. The *charge-charge* collision frequency is given by

$$\nu_{\alpha\beta} = \frac{\left(m_\alpha + m_e\right)}{3\pi^{3/2} m_\alpha^2 m_\beta} \frac{q_\alpha^2 q_\beta^2}{\varepsilon_{si}^2} n_\beta \left(\frac{2\kappa T_\alpha}{m_\alpha} + \frac{2\kappa T_\beta}{m_\beta}\right)^{-3/2} \ln\left(\frac{12\pi\varepsilon_{si}\kappa T}{q_\alpha q_\beta}\sqrt{\frac{\varepsilon_{si}\kappa T}{e^2 n}}\right) \tag{3. 13}$$

where the symbols of α and β denote charge 1 (electron or hole) and charge 2 (hole or electron), respectively. For charge-neutral collisions,

$$\nu_{q\beta} = \frac{8\pi^{1/2}}{3} \frac{m_\beta}{m_\alpha + m_\beta} n_\beta \sigma^2 \left(\frac{2\kappa T_\alpha}{m_\alpha} + \frac{2\kappa T_\beta}{m_\beta}\right)^{1/2} \tag{3. 14}$$

where σ is the sum of the effective radii of the interacting particles and q denotes the quantum dot which has many properties of natural atoms and is also known as artificial atom.

The optical radiation may also occur via a number of independent competing processes, including the transfer of energy to lattice vibrations (creating one or more

phonons) or to another free electron (Auger process). Different types of transition may also take place at surfaces and indirectly via traps or defect centers, which are energy levels associated with impurities or defects associated with grain boundaries, dislocations, or other lattice imperfections that lie within the forbidden band. An impurity or defect state can act as a recombination center if it is capable of trapping both an electron and a hole, thereby increasing their probability of recombining. The presence of these defects and the high electric field inside the junction result in both a reduction in free carrier density and a reduction of their mobility due to increased scattering of the remaining free carriers with the additional charge centers [41]. Hence, impurity-assisted recombination, which is radiative, should be able to partially characterize the light emission spectrums.

Moreover, Fig. 3.2 clearly presents that the peak energy shifts toward higher values when the reverse-bias increases. The shift is probably a consequence of the energy band variation with reverse-bias. The peak intensity also increases for an increasing reverse-bias due to the increase in impact ionization rate. In fact, at increasing reverse-bias, the multiplication rate increases due to the reduced phonon scattering. Hence, the density of hot carriers traveling through the depletion region is increased and lead to an important reverse current. As a result, radiative recombination rate is increased and emitted light intensity is also increased.

It is also observed that there is a very weak photon emission at a wavelength of 375 nm, which corresponds to photon energy of 3.3 eV. Emission at wavelength of 375 nm (equivalent to a photon energy of 3.3 eV) corresponds closely to the energy of 3.2 eV required by a hot electron to surmount the silicon-silicon dioxide barrier and be injected into the gate oxide. Hence, it is suspected that this emission represents the injection of

electrons into the silicon dioxide. An attempt was also made to measure the emission from the device once secondary breakdown occurred. On the other hand, silicon has a high absorption coefficient (10^{-4} to 10^{-5} cm^{-1}) for light with wavelengths from 300 to 400 nm, so the majority of the emitted light at this wavelength range would be absorbed at the surface silicon layer before it escapes out of the device. As a result, no detectable emission was obtained over the wavelength range of 300 to 900 nm because secondary breakdown is a thermal runaway phenomenon and most of the emission appears as heat instead of light [42].

It is once again noted that the Si-PMOSFET device works as two identical p-n junction diodes (i.e. p^+ Source/Drain to n-Substrate junction) if the insulated-gate is floated. Because source and drain are grounded (i.e. $V_d = V_s = 0$ V), the reverse bias on such p-n junction is defined as V_{sub}, the substrate voltage. Avalanche breakdown voltage of the "n-Substrate to p^+ Source/Drain" is 30 V, and it is shown in Fig. 3.3. As illustrated in Fig. 3.4, the correlation shown in Fig. 3.3 implies that there is a close relationship between the reverse current I_{sub} and the optical emission power. At lower reverse current, the correlation between the output optical power and input current is approximately linear, but the output optical power tends towards saturation when the input current increases to above 40 mA. The curves at different emitting wavelengths are quite similar, but are with different relative optical intensity/optical emission power.

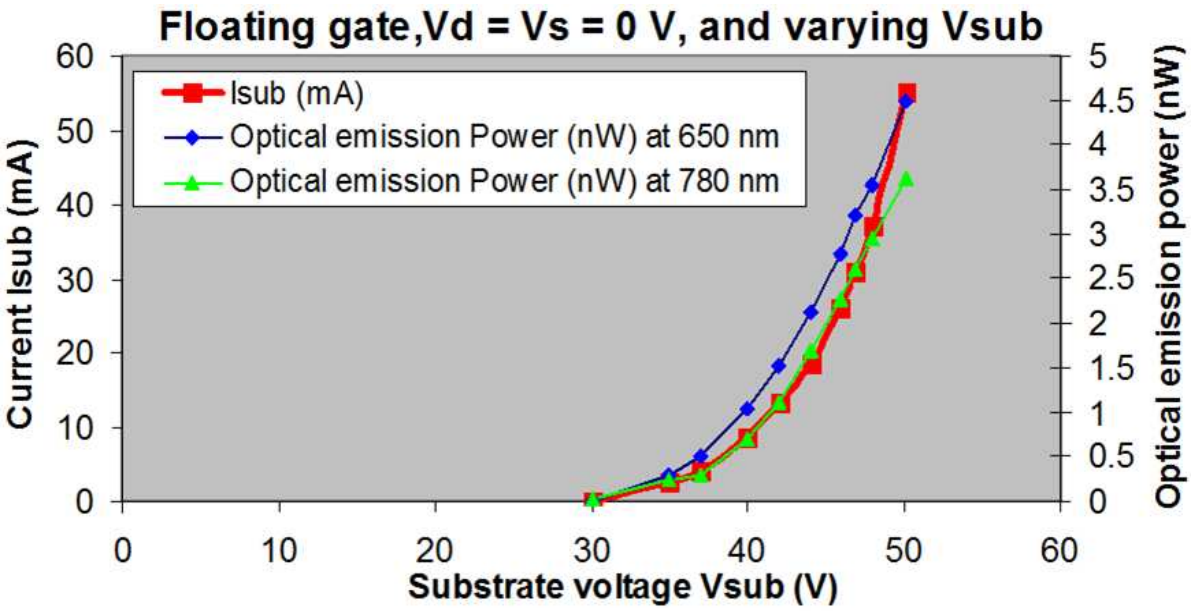


Fig. 3.3 Correlation between the optical emission power and the reverse current I_{sub} as a function of the substrate voltage V_{sub} (i.e., the reverse bias of the "n-Substrate to p^+ Source/Drain" junction)

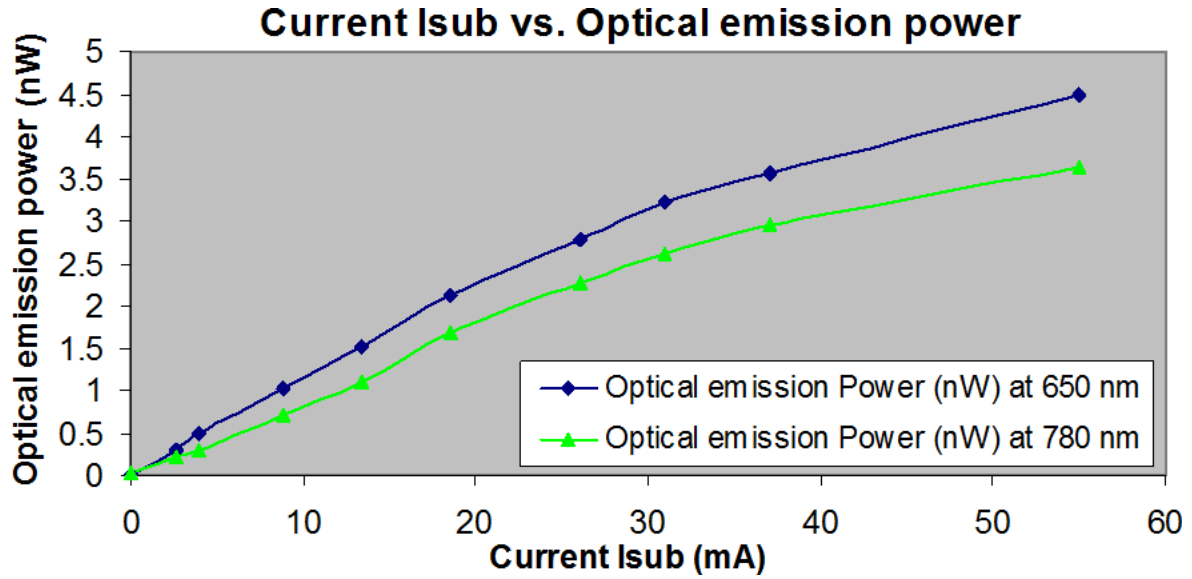


Fig. 3.4 Relationship between the optical emission power and the reverse current I_{sub} at various reverse-bias voltages V_{sub}

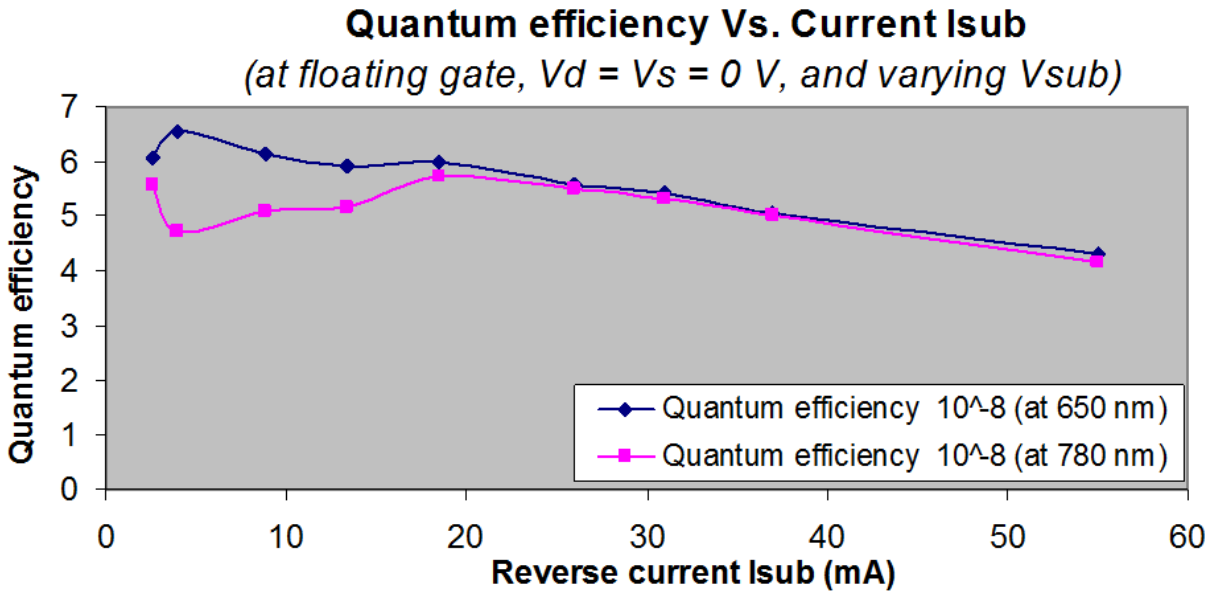


Fig. 3.5 Quantum efficiency at different bias current conditions

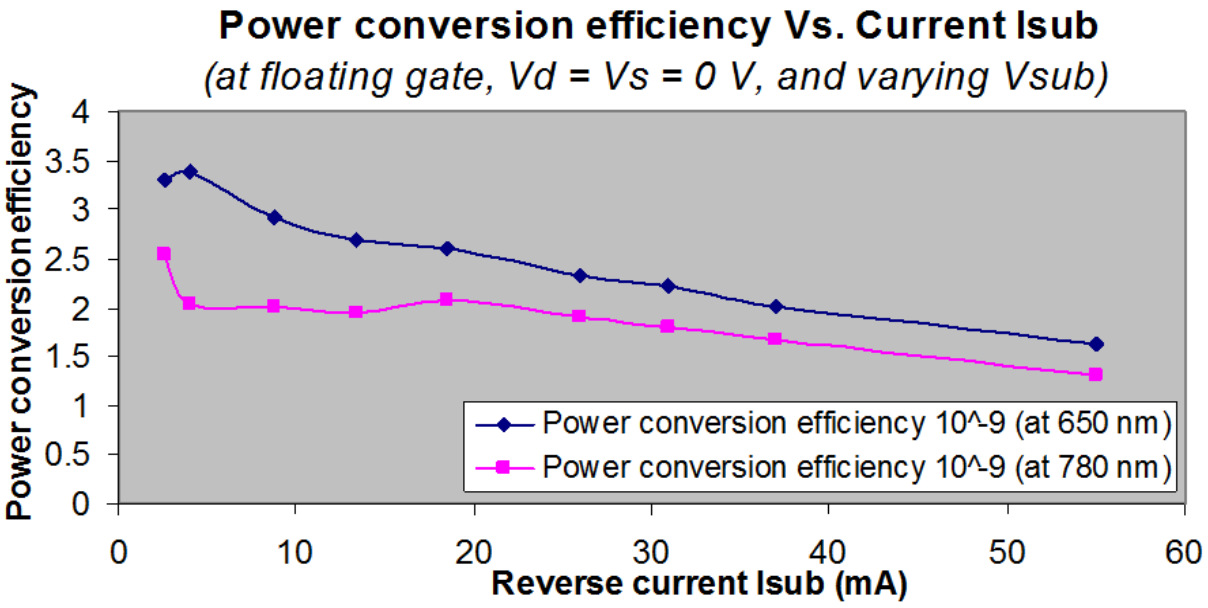


Fig. 3.6 Power conversion efficiency at different bias current conditions

The quantum efficiency has the maximum of ~6.6×10^{-8} and the minimum of ~3.9×10^{-8} at V_{sub} = 36 V and V_{sub} = 37 V, respectively. For the electrical-to-optical power conversion efficiency, the maximum is ~3.5×10^{-9} (measured at V_{sub} = 36 V) and the minimum is ~1.6×10^{-9} (measured at V_{sub} = 50.1 V). Since the quantum efficiency is the ratio between "the number of photons per second" and "the number of carriers per second" and the power conversion efficiency is the ratio between "the input electric power (i.e., the product of reverse-bias voltage V_{sub} and breakdown current I_{sub}) and "the output optical power", it is worth paying special attention to the relation of efficiency to breakdown current I_{sub}. Fig. 3.5 shows the relationship between quantum efficiency and breakdown current I_{sub}. At the same time, the relationship between power conversion efficiency and breakdown current I_{sub} is shown in Fig. 3.6. The spectral light intensities at 650 nm and 780 nm as a function of the reverse current I_{sub} is shown in Fig. 3.4.

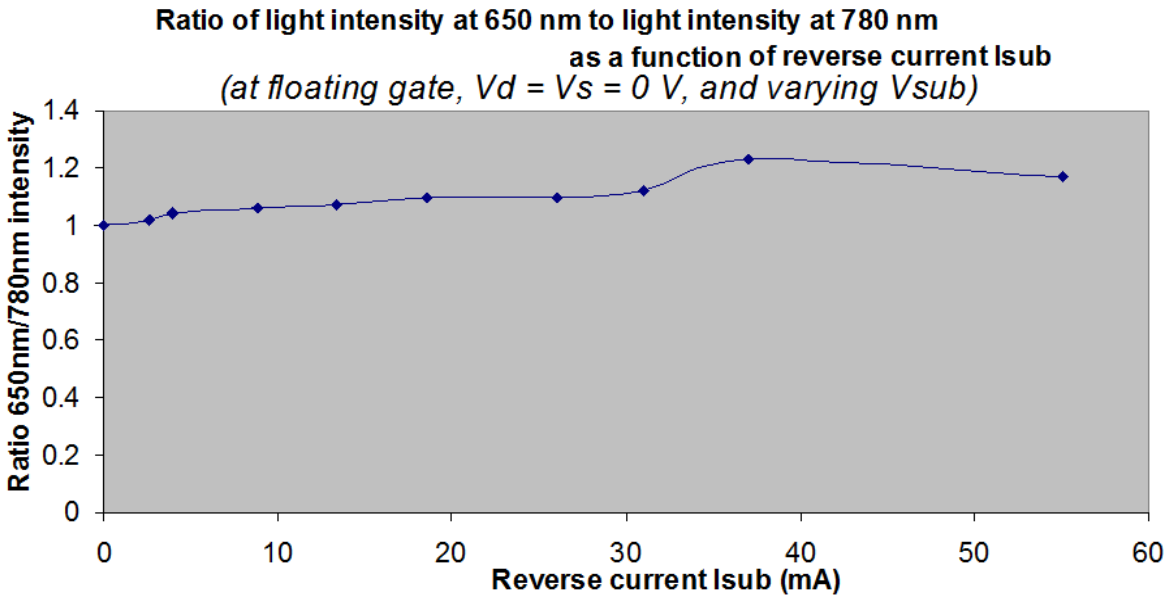


Fig. 3.7 Relationship between the ratio of light intensity at 650 nm to light intensity at 780 nm and the reverse current I_{sub}

Correspondingly, Fig. 3.7 shows the ratio of emitted light intensity at 650 nm to the light intensity at 780 nm, again as a function of the reverse current I_{sub}. In spite of the increase in reverse current I_{sub}, the ratio between wavelength peaks of 650 nm and 780 nm remains almost constant, which is shown in Fig. 3.7. From this figure it is evidence that 650 nm and 780 nm are the major two peaks which have nearly the same increase in light intensity.

Although the electrical-to-optical conversion efficiencies are low, the operating voltage and operating current are compatible with standard voltage and current used in the 3μm CMOS integrated technology. On reverse biasing the "p^+ Source/Drain to n-Substrate" interface, light-emitting regions extend right up to the Si-SiO_2 interface regions just below the poly-Si gate, since the depletion region, where the light is emitted, of the p^+ n junction becomes much wider if a higher reverse bias V_{sub} is applied. Due to the extension mentioned above, the SiO_2 and poly-Si layers will absorb some of the optical emission power. In order to realize efficiency enhancement by reducing the absorption mentioned previously, the following approaches should be taken into consideration.

- Increasing the proximately of the emission area at the planar p^+ n junction interface as close as possible to the Si-SiO_2 interface.
- Minimizing the absorption of the emitted light from the structure by narrowing the areas of Si-SiO_2 surface and over-layers on the light-emitting regions.

Once again, the fundamental of EPIC is the monolithic integration of silicon VLSI electronics with silicon photonics on a single silicon chip in a commercial state-of-the-art CMOS SOI (Silicon-on-Insulator) foundry [43]. The seamless photonics-electronics interface

will piggyback upon CMOS infrastructure and progress. Regarding for the EPIC system, it is therefore important that the individual components within the optical system be carefully designed and selected to optimize the individual light coupling efficiency. Poor coupling efficiency between the emitted light cone and the light guide may result in significant light loss in the entire spectral analysis system.

3.4 Silicon p-n junction gate-controlled diode light-emitting device (Si gate-controlled diode LED)

Essentially, the Si-PMOSFET (in this measurement, $V_{sub} > 0$, $V_d = V_s = 0$ V, and varying V_g) can be treated as two identical p^+ n gate-controlled diodes connected symmetrically and in parallel. For a p^+ n gate-controlled diode, its breakdown voltage (BV) is inversely proportional to the gate voltage V_g, and so, current flowing through the p^+ n junction will be modulated by varying V_g as the reverse bias applied to this p^+ n junction is always at V_{sub}, a constant. As optical emission power is closely dependent on the reverse current I_{sub} (i.e., the number of carriers per second), it is expected that V_g can modulate optical intensity very well. This essence, the core of this study, will be discussed in detail by the experimental results in the following section.

In the electronic measurements, it has been shown that the avalanche breakdown voltage across the "p^+ Source/Drain to n-Substrate junction" is ~ 40-45 V at $V_g = 0$ V. So, $V_{sub} = 35$ V has been chosen to prevent such junction breakdown in order to avoid light emission at $V_g = 0$ V. Actually, "V_g-V_{sub}" versus "optical power/intensity" is the most important part of interest.

The designed device channel length of about 6 μm in this study is much larger than the sum of the depletion width for "p^+ Source to n-Substrate" and the depletion width for "p^+ Drain to n-Substrate" in order to prevent "Source to Drain punch through" when V_{sub} = 35 V, $V_d = V_s = 0$ V and gate voltage V_g is varied. The Si LED device with the physical structure of PMOSFET essentially consists of two identical gate-controlled diodes [43] ("p^+ Source/n- Substrate" & "p^+ Drain/n-Substrate") symmetrically. For $V_g < V_{sub}$, channel layer is an inversion layer; for $V_g = V_{sub}$, the depletion width for "p^+ Source/Drain to channel" approximately is equal to the depletion width for "p^+ Source/Drain" as such inversion channel layer is replaced with n-substrate; for $V_g > V_{sub}$, depletion width for "p^+ Source/Drain to channel" varies from the minimum on the surface of channel layer to the maximum that equals the depletion width for "p^+ Source/Drain to n-Substrate", furthermore, channel layer is an accumulation layer with the highest concentration at the surface and the lowest concentration approximately equal to the doping concentration of n-substrate at the bottom boundary where the interface between channel accumulation layer and n-substrate is [44]. From the discussions above, the maximal depletion width in channel is horizontally the sum of the depletion widths for two identical gate controlled diodes (i.e., "p^+ Source to n-Substrate" diode and "p^+ Drain to n-Substrate" diode, both diodes having the same reverse bias of 35 V), or about 2×2.16 μm with the doping concentrations of $N_a \sim 10^{20} cm^{-3}$ and $N_d \sim 10^{16} cm^{-3}$. In addition, the light will come from points A and B in Fig. 3.8, where the maximal field of "p^+ Source/Drain to n-Substrate" junction locates.

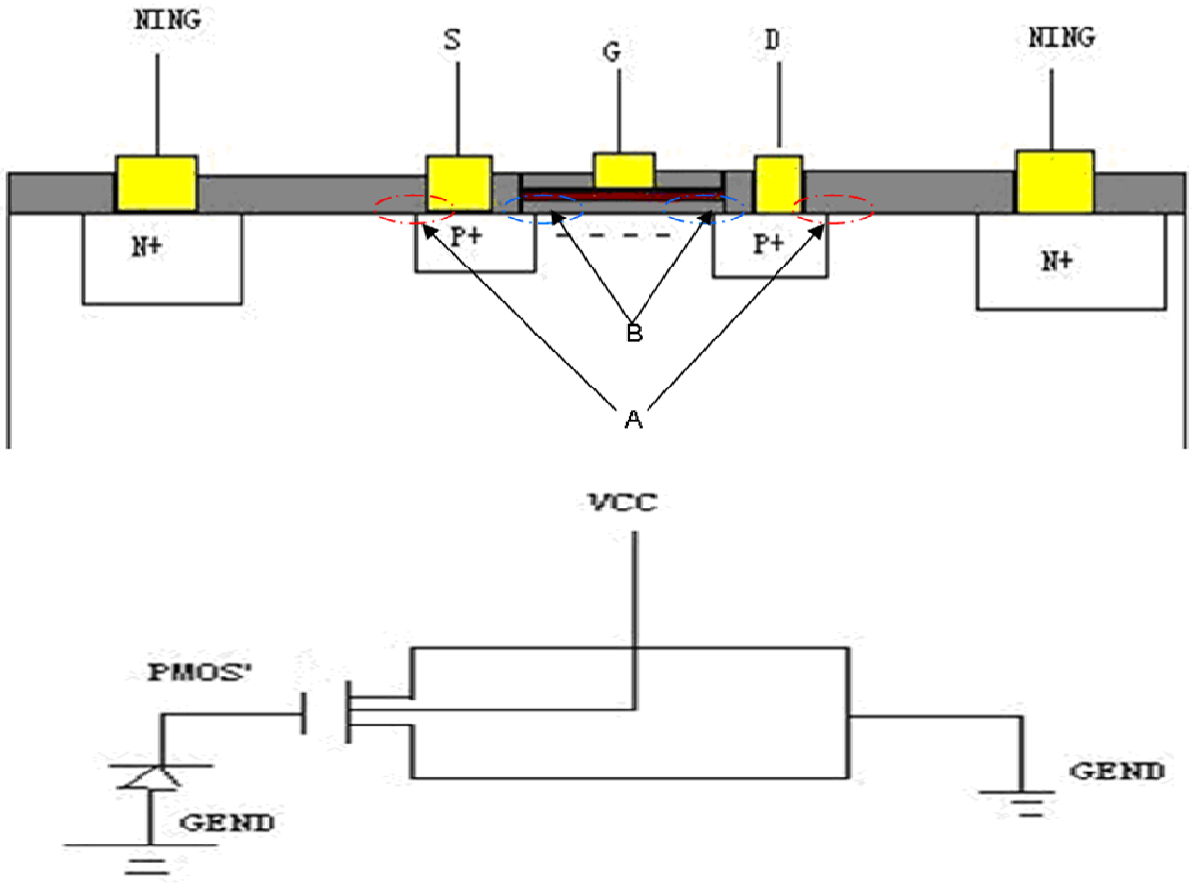


Fig. 3.8 Cross-section and schematic diagram of the semiconductor device

In order to find the breakdown voltage *BV*, both P^+ diffusion regions (i.e., source and drain) are connected to the ground. As shown in Fig. 3.9, the Semiconductor Parameter Analyzer (SPA) is used to sweepingly find the *BV* of the "N-Substrate to P^+ Source/Drain" junction. By varying gate voltage V_g at $V_d = V_s = 0$ V, this PMOSFET will work as two identical gate-controlled diodes in parallel.

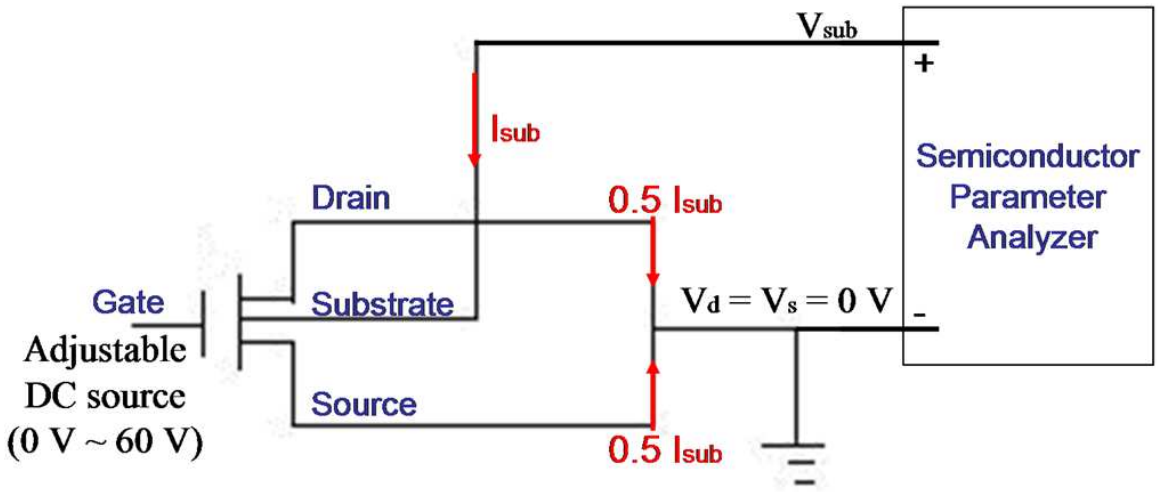


Fig. 3.9 Schematic for measuring breakdown voltage of the p-n junctions

Fig. 3.10 presents "gate voltage V_g versus *BV* of the gate-controlled diode in this PMOSFET". *BV* is the breakdown voltage of "P^+ Source/Drain to N-Substrate" junction while I_{sub} is the reverse current flowing from N-Substrate to P^+ Source/Drain due to junction breakdown. It should be noted that *BV* does not show a drastic decrease until V_g is as high as 30 V. It has also been discovered that the relationship between *BV* of such gate-controlled diode in the PMOSFET and gate voltage V_g is almost linear when V_g ranges from 30 V to 40 V as shown in Fig. 3.11. In the range of $0 < V_g < 30$ V, it can be explained as

follows: the breakdown voltage *BV* tends to saturation at a maximum (i.e., 40 V, the breakdown voltage observed at V_g = 0 V) that is little related to the value of V_g.

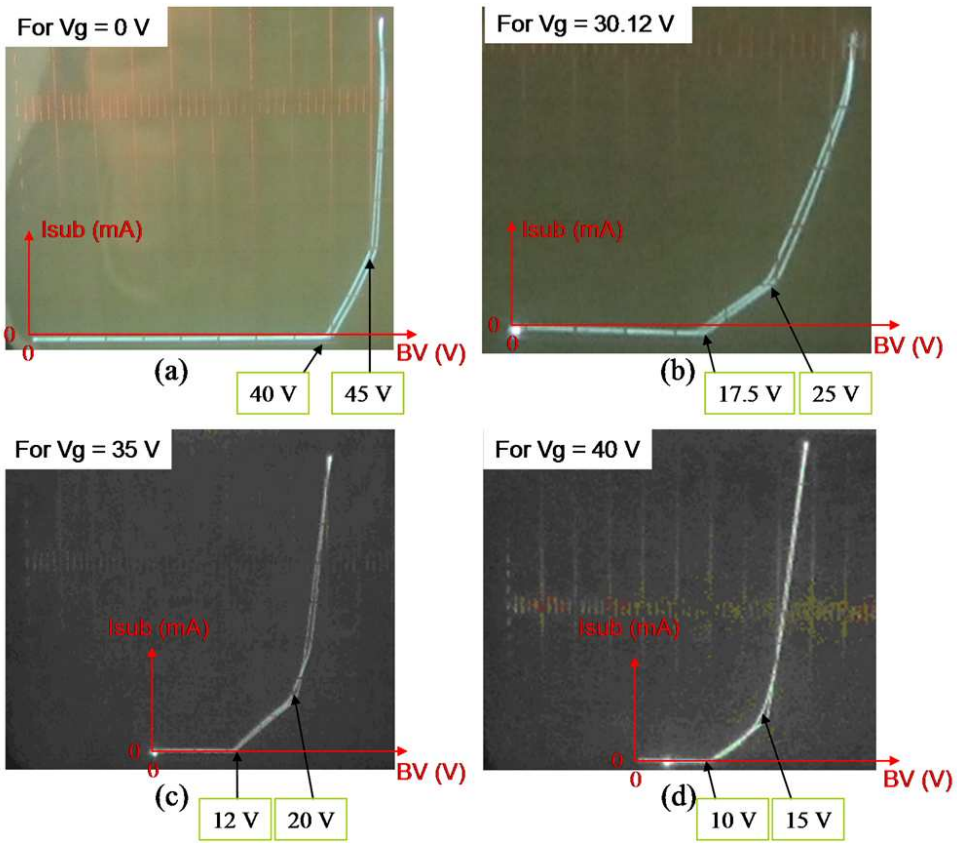


Fig. 3.10 Gate voltage V_g versus breakdown voltage BV by sweeping V_{sub} from 0 V to 50 V, X-axis is breakdown voltage with 5 V/decade; Y-axis is Isub with 5mA/decade. (a) V_g = 0 V, device starts breakdown at 40 V (corresponding to soft breakdown-voltage), and completely breakdown at 45 V (corresponding to hard breakdown-voltage); (b) V_g = 30.12 V, device starts breakdown at 17.5 V, and completely breakdown at 25 V; (c) V_g = 35V, device starts breakdown at 12 V, and completely breakdown at 20 V; (d) V_g = 40 V, device starts breakdown at 10 V, and completely breakdown at about 15 V

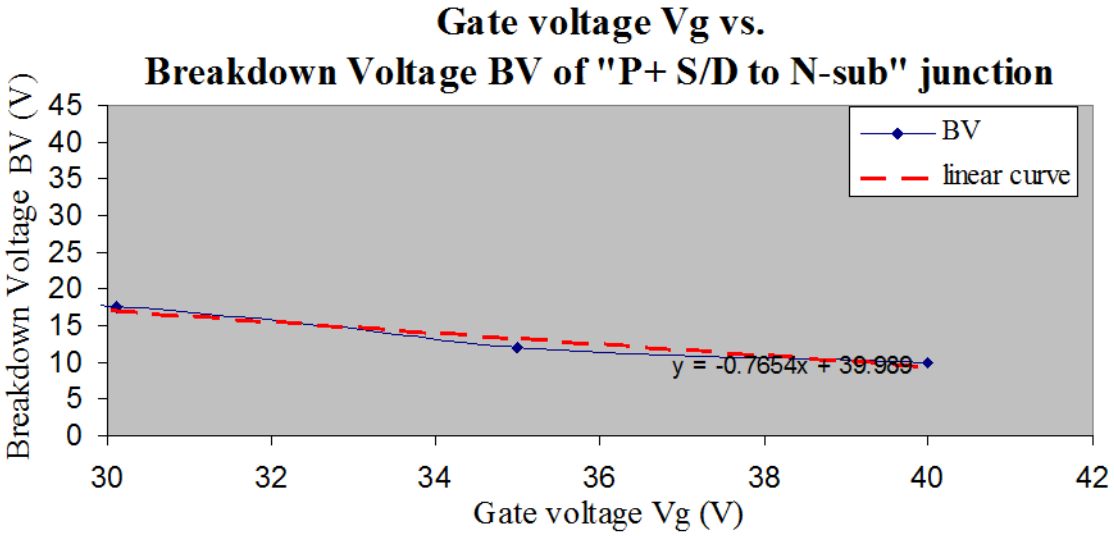


Fig. 3.11. Correlation between the "V_g vs. Breakdown voltage" curve and the linear curve at V_{sub} = 50 V and $V_d = V_s$ = 0 V

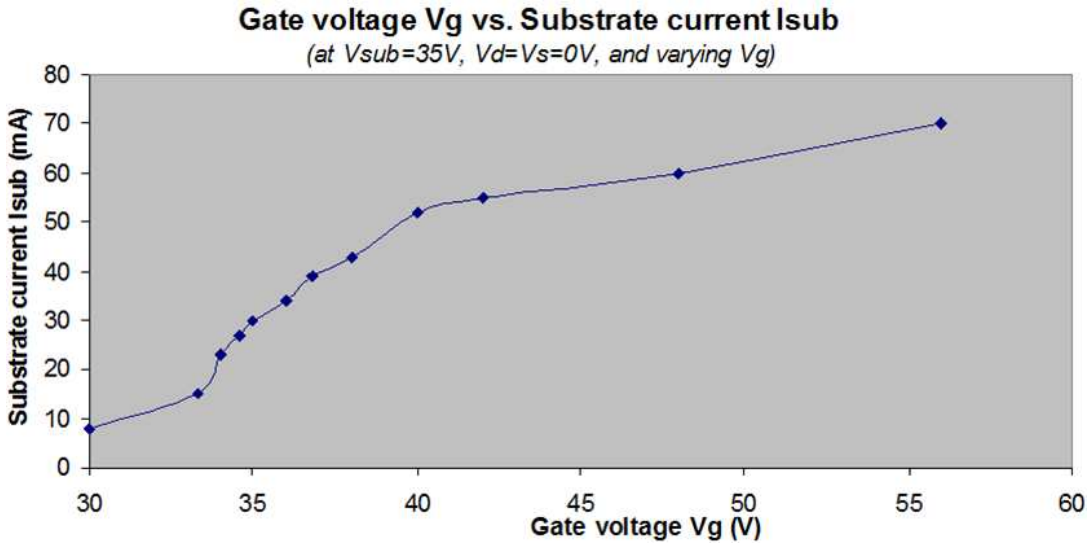


Fig. 3.12 Gate voltage V_g versus reverse current I_{sub} at V_{sub} = 35 V and $V_d = V_s$ = 0 V. It reveals that there is I_{sub} of 8 mA at V_g = 30 V, that a relatively significant increase in current occurs while V_g increases from 33.3 V to 40 V, that a relatively slow increase in current occurs while V_g increases from 40 V to 56 V, and that the device will be devastated very quickly due to heat breakdown when V_g is over 60 V

From the previous discussions, it has been known that the increase in gate voltage V_g will reduce the breakdown voltage BV of "p^+ Source/Drain to n-Substrate". The breakdown mechanism at this junction corner is transiting from avalanche (relatively high BV) to tunneling (relatively low BV) in the whole process where V_g ranges from 30 V to 56 V as the current is increasing due to the decrease of BV. More specifically, BV of "p^+ Source/Drain to n-Substrate" will be low and the current (i.e., substrate current I_{sub} shown in Fig. 3.12 and Fig. 3.13) flowing through the two p^+ n gate-controlled diodes will commence at a small value of the reverse biased voltage (i.e., V_{sub}). In other words, the reverse current I_{sub} will be much higher, as presented in Fig. 3.12, if a higher gate voltage V_g is applied to make BV reduction, for the reverse biased voltage across the two p^+ n diodes is always kept at 35 V. Consequently, the breakdown accompanying photonic emission effectively has already taken place in the PMOSFET at V_g ~30 V, even if V_{sub} is just 35 V, a reverse bias that is lower than the BV of "p^+ Source/Drain to n-Substrate junction" at V_g = 0 V, BV ~40 V–45 V as mentioned above. It should be kept in mind that the reverse current I_{sub} has a relative drastic increase at V_g ~33.3 V, whereas the increase in I_{sub} becomes slower again when V_g is over 40 V. The surface effect of Field Effect Transistor (FET) on breakdown voltage BV should be an appropriate solution that can be adequately used to explain the I-V curve in the shape of the letter "*Z*", as presented in Fig. 3.12.

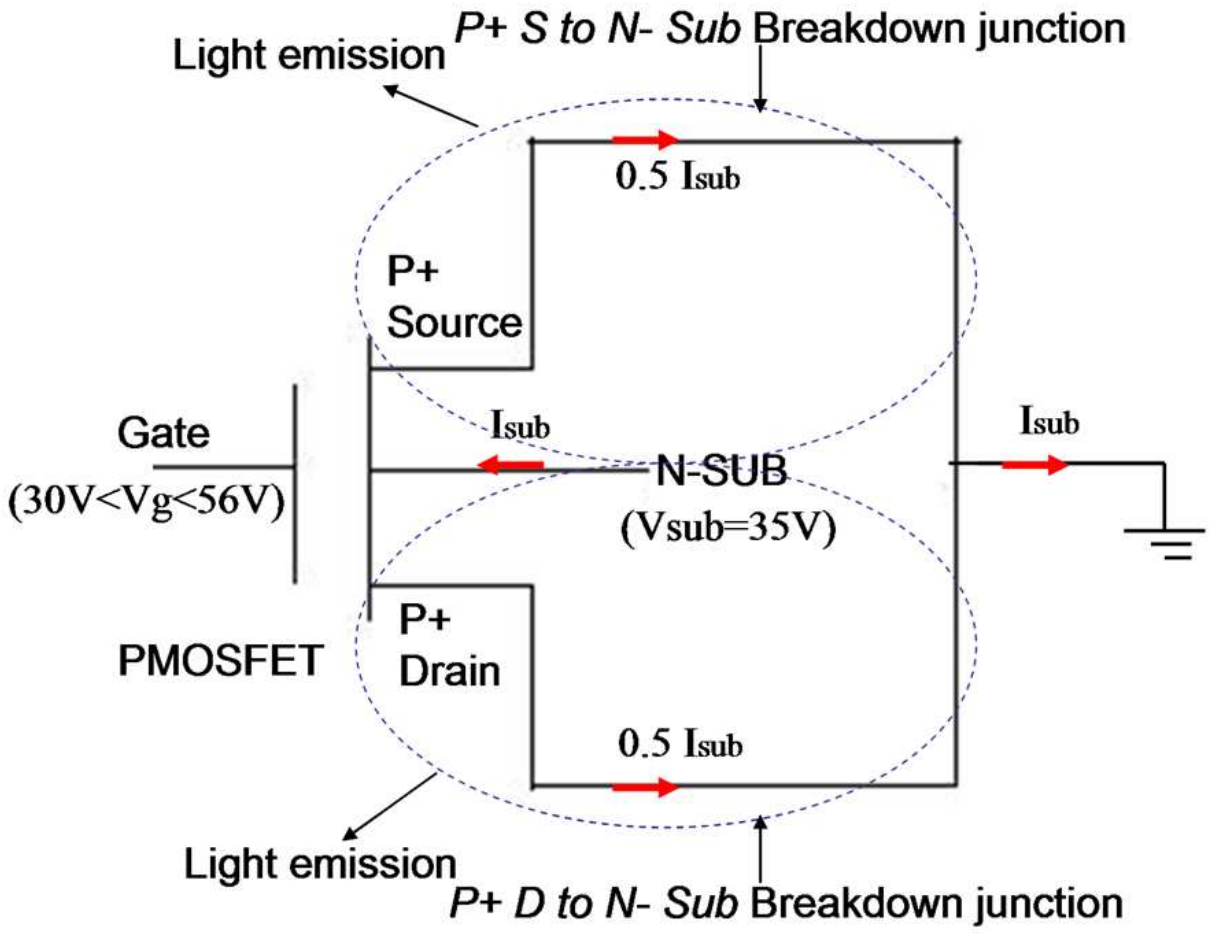


Fig. 3.13 Substrate current I_{sub} flows from n-substrate to p^+ Source/Drain diffusion region. Simultaneously, Bremsstrahlung based light emission will take place in the avalanching depletion region.

It is very important to note that this PMOSFET device can be treated as two identical p^+ n gate-controlled diodes in parallel under breakdown condition as the bias conditions are $V_{sub} > 0$ V and $V_d = V_s = 0$ V. According to the theory of gate-controlled diode, the breakdown voltage (i.e., BV of "n-Substrate to p^+ Source/Drain junction") starts from a relatively high value at positive gate voltages, decreases as the gate voltage is made more positive and approaches the *plane* rather than *planar* value of the breakdown voltage. The gate voltage that must be applied in order to approach the plane breakdown voltage values is approximately that required to bring about the formation of a field-induced junction over the substrate, i.e., the turn-on voltage [44]. In the case of this Si-PMOSFET LED, the high voltage extreme for BV saturation occurs at V_g ~33.3 V (i.e., the turn-on voltage) and the low voltage extreme for BV saturation occurs at V_g ~40 V. Moreover, Grove et *al*. [46] presents that a p^+ n gate-controlled diode, which is one half of a PMOSFET in fact, had been measured in [46]. As the gate potential V_g is decreased, the increase in BV becomes less rapid and the characteristic tends toward saturation at a maximum BV [46]. This voltage is considerably higher than the BV of the corresponding planar diode without a gate BV_{planar}, and approaches the BV of the corresponding plane diode, BV_{plane}. In the other extreme, as the gate potential V_g is increasingly positive, the decrease in BV diminishes and the BV tends toward saturation at a minimum value [46]. In the intermediate range between the two extremes, V_g is almost inversely proportional to BV with the following linearity

$$BV = mV_G + \text{constant} \tag{3. 11}$$

It has also been presented in Fig. 3.11 that, due to such BV saturation, the increase in reverse current I_{sub} with gate voltage V_g in the range of 33.3 V > V_g and in the range of V_g >

40 V is not that drastic and is becoming relatively slow, compared to the increase in reverse current I_{sub} observed in the intermediate range (i.e., from 33.3 V to 40 V) of V_g.

No significant shift of spectrum in wavelength peaks was observed at different gate voltage V_g. The emitting wavelength range is very broad, from 450 nm to 850 nm, as shown in Fig. 3.14. There are one extremely distinct peak at wavelength 600 nm, two distinct peaks at wavelengths 650 nm and 750 nm, and one secondary peak at 550 nm in the measured range of 300–900nm. In addition, there are a number of sub-crests.

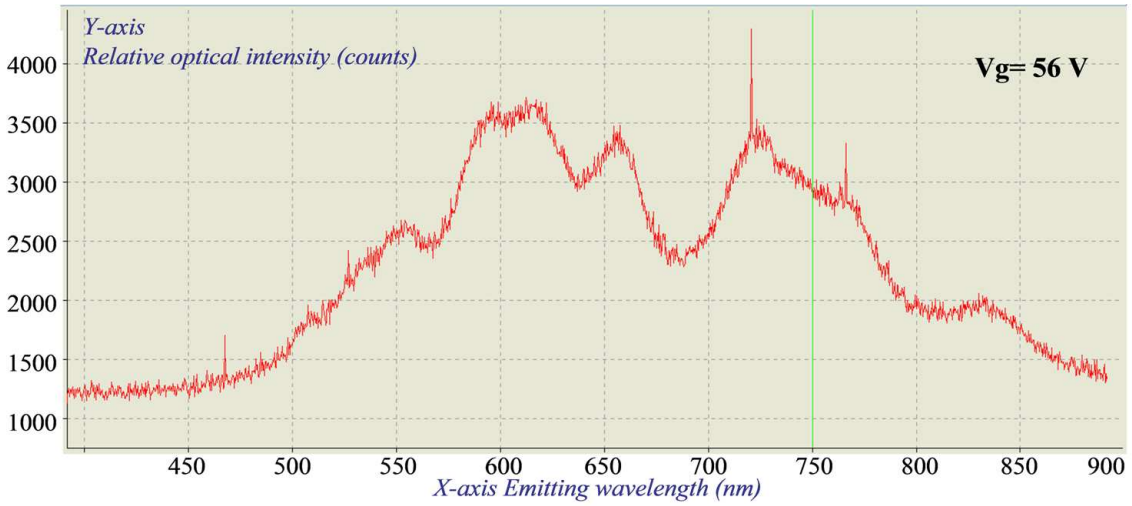


Fig. 3.14 Optical spectrum observed at V_g = 56 V based on V_{sub} = 35 V (i.e.,, *the reverse bias across "p⁺ Source/Drain to n- Substrate" junction*). The emitting wavelength range is very broad, from 450 nm to 850 nm

As have been discussed in previous section, such light emission is due to avalanche breakdown generated carriers colliding with immobile charge centers in the depletion region. Essentially, in the micro-plasma (the p-n junction depletion region can be treated as gas micro-plasma while the photon emission in avalanched p-n diode is approximately to

be Bremsstrahlung radiation) or avalanche region itself, both hot holes and hot electrons are present up to the pair production threshold for holes (2.4 eV) and that for electrons (1.8 eV) due to high accelerating field. In [47], it is explained as follows. The 650 nm peak may be related to the threshold for pair production during ionization of the Si host atoms with electrons (1.8 eV), whereas the 550 nm peak may be related to the pair production threshold with holes (2.4 eV). Furthermore, the peak of 550 nm may also reasonably relate to some correlation with phonon-assisted conduction-conduction-band transitions that was predicted by in [48]. Both the distinguished peaks and the subsidiary peaks may of course also relate to other hot-carrier transitional and defect interaction effects at the heavily defect-containing p^+ Source/Drain to n-Substrate interface. Therefore, it is reasonably important for us to pay special attention to these wavelength peaks (e.g., around 550nm or around 650nm) in the measurement.

Fig. 3.12 being very similar to Fig. 3.15 in the style of the curves implies that the relationship between substrate current I_{sub} and optical emission power (or light intensity) is nearly linear, as shown in Fig. 3.16. Meanwhile, optical power saturation tends to take place when current I_{sub} is over 55 mA. It is identical with the linearity between breakdown current (i.e., the reverse current flowing through the avalanching p-n junction) and optical power discovered in a Si-diode LED, as reported by [49]. Such linearity shows the strong dependence of the phenomenon of photonic emission on breakdown current (i.e., the number of carriers) and can probably give some explanations for the mechanism that light emission in avalanche breakdown of silicon p-n junction originates from Bremsstrahlung radiation.

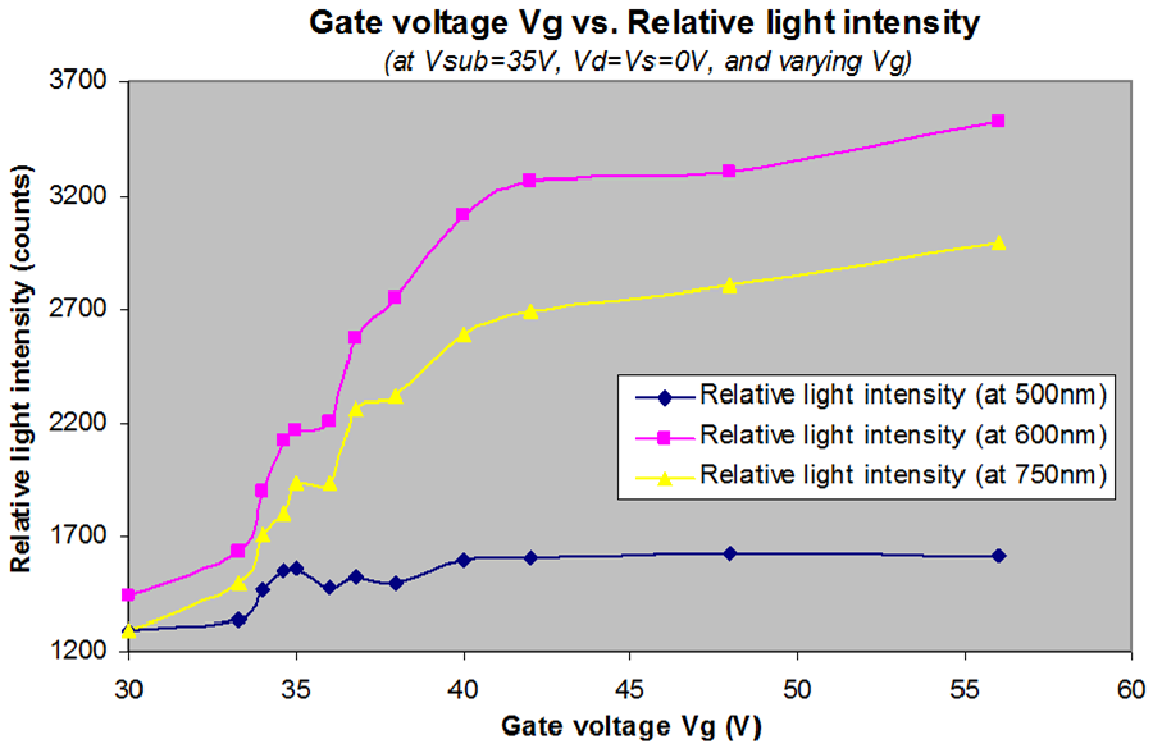


Fig. 3.15 Relationship between the gate voltage V_g and the relative light intensity; Curves at different emitting wavelengths are so similar as to be like a "*Z*" style, and the difference is only the values of relative light intensities.

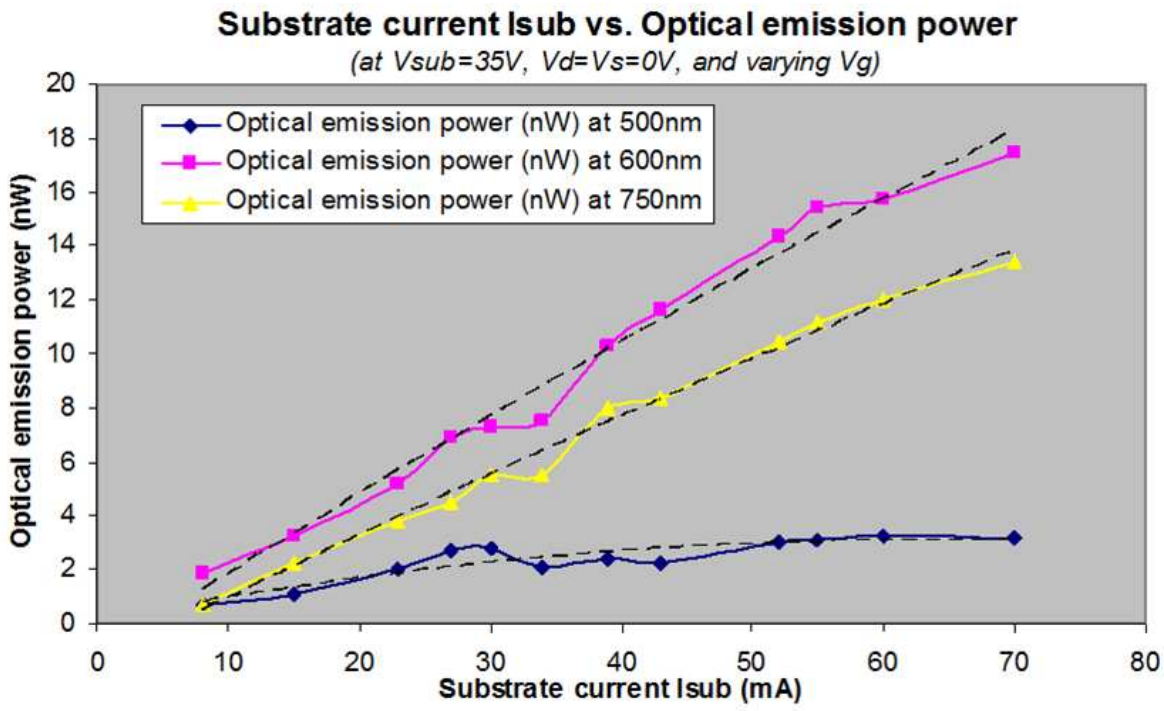


Fig. 3.16 Relationship between the reverse current I_{sub} and the optical emission power: Black dotted lines indicate the *approximate* linearity between the reverse current I_{sub} and the optical emission power. Starting from I_{sub} ~55mA, optical emission power tends towards saturation. Curves at different emitting wavelengths are so similar as to be *almost* linear; the difference is only the values of optical emission powers.

The emitted power from the Si-PMOSFET device operating as a Si gate-controlled diode LED was measured using a calibrated power meter positioned immediately above the device in order to collect most of the emitted light, though a great amount of output power is dissipated during the measurement because of the dispersion by silicon dioxide layer and optical lens and the absorption by silicon materials itself. For optical emission power at emitting wavelength 600 nm, it is 1.83 nW at V_g = 30 V, 3.27 nW at V_g = 33.3 V, 15.45 nW at V_g = 42 V, and 17.44 nW at V_g = 56 V as shown in Fig. 3.16.

External quantum efficiency (i.e., the number of photons at wavelength 600 nm / the number of electrons due to reverse current I_{sub}) is of the order of 10^{-7}. External power conversion efficiency (i.e., the optical emission power at wavelength 600nm / the electric power due to the product of reverse current I_{sub} and reverse bias V_{sub} = 35 V) is of the order of 10^{-9}. The quantum efficiency has the maximum of 1.473×10^{-7} at the gate voltage of V_g = 42 V and the minimum of 1.143×10^{-7} at the gate voltage of V_g = 33.3 V. The power conversion efficiency has the maximum of 8.026×10^{-9} at the gate voltage of V_g = 42 V and the minimum of 6.230×10^{-9} at the gate voltage of V_g = 33.3 V. Undoubtedly, the actually total emitting power should be even much higher, and the internal efficiency should be several orders of magnitude higher than the external efficiency calculated above.

3.5 Comparison between the Si-diode LED and the Si gate-controlled-diode LED in the Si-PMOSFET device

It has been shown that, by operating a Si-PMOSFET device, both the two-terminal Si-diode LED and the three-terminal Si gate-controlled diode LED are investigated in detail. Since the device is realized using conventional VLSI design rules and CMOS device

processing without any adaptation to the process, the device as a silicon light source enables the production of all-silicon monolithic optoelectronic integrated circuits (OEICs) systems.

In Si-diode LED, the light emission is attributed to the avalanche breakdown of the p^+ Source/Drain to n-Substrate junctions and the optical emission power increases with the reverse bias of the p-n junction. In Si gate-controlled diode LED, the light emission is attributed to a tunneling-assisted avalanche breakdown of the p^+ Source/Drain to n-Substrate junctions with the generation of a parasitic field-induced junction near the p-n junction corner and the optical emission power increases with the gate voltage V_g while the reverse bias of the p-n junction is a constant.

3.6 Increased efficiency of Si light-emitting diodes (Si-LEDs) in a standard 3-μm Si CMOS technology

3.6.1 Introduction

Silicon diode at avalanche breakdown has visible light emission in the depletion region. It is believed that this optical radiation comes from the kinetic energy loss of carriers generated by impact ionization colliding with immobile charge centers in the avalanche region. A theoretical model is presented to show the correlation of the hot carrier effect with the related photonic emission in high field. Meanwhile, a PMOSFET-like silicon light source device fabricated completely in the standard silicon CMOS process technology is measured to demonstrate that avalanching current is linearly proportional to optical emission power whether this light source acts as a two-terminal device (i.e., diode, the "p^+ Source/Drain to n-Substrate junction" with floating the gate) or acts as a three-

terminal device (i.e., gate-controlled diode, the "p^+ Source/Drain to n-Substrate junction" in the course of varying the gate voltage). Such linearity implies that control of the increasing current is a significant way to enhance the quantum efficiency of this light source device no matter what the physical structure (i.e., two terminals or three terminals) of the device is. For the first time, it has been discovered that, at the same avalanching current, the optical output power in gate-controlled diode structure is higher than the optical output power in diode structure. In other words, for this PMOSFET-like device, the three-terminal operating mode is more efficient than the two-terminal operating mode.

3.6.2 Visible light from a reverse-biased silicon p-n junction

Physical mechanisms responsible for avalanche emission observed in this and previous work are discussed below. The Bremsstrahlung based radiative phenomenon was observed in MOSFET working in saturation mode with avalanche breakdown occurring in the corner of "substrate to drain" junction [50]. Tam *et al.* have proved that such avalanche breakdown induced photonic emission occurring either in NMOSFET or in CMOS belongs to Bremsstrahlung radiation in theory by calculation [51]. Some of these photons with high energy will be absorbed by silicon material to generate photon-induced current. Takeda *et al*. demonstrated the existence of that photon-induced current by finding the paradox between the theoretical calculation results and the experimentally measured results for the dependence of the correlation of gate current and substrate current on temperature [52]. More specifically, the expression for drain current I_d can be shown to be $I_d \infty A\, I_{sub}$, where $A = \int \alpha dx$ is the ionization integral and α is the effective ionization rate. Then,

$$\left|\frac{\Delta \log I_d}{\Delta T}\right| = \left|\frac{\Delta \log A}{\Delta T}\right| + \left|\frac{\Delta \log I_{sub}}{\Delta T}\right| > \left|\frac{\Delta \log I_{sub}}{\Delta T}\right| \quad (3.12)$$

However, measurement shows I_d exhibits much less temperature dependence than I_{sub}, implying the existence of photon induced current. Such photon-induced current also compels the carrier to have a longer diffusion length and a longer life time [53]. Toriumi [54] also measured photon energy emitted from near the drain and investigated a relationship between hot-carrier effects and electron temperature. The energy distribution function of photon intensity is given by

$$f(E) = C \exp(-E / kT_e) \quad (3.13)$$

where C is a constant, k is the Boltzmann's constant, and T_e is the effective temperature of the hot carrier. The exponential distribution is in good agreement with the expression of ionization rates for electrons and holes in the depletion region of silicon PN junction [55]. It is important to note that Bremsstrahlung depends on applied electrical field and material properties including the ionization length of electrons and holes. According to the Bremsstrahlung concept, a theoretical model has been proposed for investigating the correlation between hot carriers and emitted photons, especially localized injected carriers can initialize charge multiplication processes in the presence of a strong electric field in the depletion region with breakdown mechanisms. When carriers are drifting in the electric field, acceleration of carriers can be taken into account during the break between two continuous scattering cases. The duration of such a break is the Free Time (FT). The accurate values of free time for different carriers are not identical. The average value obtained from the sum of all the FT values is defined as the Mean Free Time (MFT), which is represented by τ.

MFT and Scattering Probability (SP) are two important parameters that are being exclusively used for the description of scattering process. The relationship between the two parameters can be obtained by considering the movement of electron carriers. It is assumed that there are N electrons that are randomly moving in a defined direction starting from the moment $t=0$, and that $N(t)$ represents the number of electrons that do not suffer from the scatterings at the moment t. According to the definition of Scattering Probability, the number of electrons during the time from t to $t+\Delta t$ is

$$N(t)P\Delta t \tag{3. 14}$$

Therefore, the number of non-scattering electrons during the time t to $t+\Delta t$ is $N(t)P\Delta t$ less than $N(t)$

$$N(t)-N(t+\Delta t)=N(t)P\Delta t \tag{3. 15}$$

As Δt is very small, Eq. (3. 15) can be rewritten as

$$\frac{dN(t)}{dt}=\lim_{\Delta t\to 0}\frac{N(t+\Delta t)}{\Delta t}=-PN(t) \tag{3. 16}$$

The solution of Eq. (3. 16) is

$$N(t)=N_0\exp(-Pt) \tag{3. 17}$$

where N_0 is the number of non-scattering electrons. Substituting Eq. (3. 16) into Eq. (3. 17), the number of scattering electrons during the time t to $t+\Delta t$ will be

$$N_0P\exp(-Pt)dt \tag{3. 18}$$

The MFT for every electron during the time t to $t+\Delta t$ is t, and $tN_0\exp(-Pt)dt$ is the sum of these electrons' MFTs. The sum of the MFTs for N_0 electrons can be obtained by integrating over the time variable dt, thus, the MFT can be expressed as

$$\tau = \frac{1}{N_0}\int_0^{\infty} N_0 P \exp(-Pt)dt = \frac{1}{P} \tag{3. 19}$$

Substituting Eq. (3. 19) into Eq. (3. 17), the number of non-scattering electrons at the moment t is

$$N(t) = N_0 \exp\left(-\frac{t}{\tau}\right) \tag{3. 20}$$

If the velocity is reasonably assumed to be a constant, then the distance for which a non-scattering electron drifted in the duration $0 \to t$ will be $d = t \times v$. Subsequently, the Mean Free Path (MFP) can be written as $\lambda_m = \tau \times v$. In the result, we obtain

$$N(t) = N_0 \exp\left(-\frac{d}{\lambda_m}\right) \tag{3. 21}$$

, which is the empirical equation for the description of the lucky electron model. Eq. (3. 21) means the probability of an electron being able to avoid any scattering collision and transit for a distance d will be equal to $\exp\left(-\frac{d}{\lambda_m}\right)$. Deduction above corresponding reasonably well with the energy distribution function of photon intensity (i.e., Eq. (3. 13)) implies the existence of Bremsstrahlung radiation in the avalanched depletion region of the reversely biased silicon PN junction.

On the other hand, Bremsstrahlung was thought to be a dominant mechanism previously, but that view was not supported by much evidence after 1993. Because the theoretical calculation based on the Bremsstrahlung mechanism does not agree well with the experimental results when the variation of the channel electric field with bias is taken into account, Tao *et al*. concluded that the Bremmstrahlung of hot electrons in Columbic field is unlikely to be the dominant mechanism of photonic emission in n-channel MOSFETs

[56]. Akil *et al*. did mention Bremsstrahlung as one possible mechanism, but covering only a very small region of the emission spectrum [57]. Furthermore, Gurfinkel *et al*. only mentioned Bremsstrahlung in passing as one of the several possible mechanisms [58].

In general, the photon generation mechanism of this phenomenon is very complicated and still not conclusive. Possible mechanisms include transition from predominantly indirect interband to indirect intraband process and transition from predominantly intraband to direct interband process [57]. It indicates that there are other dominant mechanisms contributing to the optical emission besides the Bremsstrahlung radiation. Nevertheless, the number of carriers per second (i.e., avalanching current/q) will undoubtedly play an important role significantly in determining the optical emission power emitted from reverse-biased silicon PN junction. It is noted that q denotes the magnitude of electronic charge.

When a MOS transistor operates in the saturation mode, a substrate current, which is comprised of impact ionized minority carriers induced by drain avalanche, is found to exist at the high drain voltages due to the high electric fields around the Drain-Substrate corner. A linear relationship was also observed between the minority carriers' current and the optical emission power in the saturation-MOS field effect transistor [59]. That hot-carrier induced luminescence in MOSFET channels had also been used to investigate defects in switching integrated circuits for the purpose of device reliability [60].

Huang *et al*. observed that the avalanching current was linearly related to optical emission power in the simple silicon PN junction diode [49]. Similar linearity between the avalanching current and the optical emission power was also observed in the silicon gate-controlled diode [61]. For the device shown in Fig. 3.17 with a physical structure of p-type

MOSFET, it can works either as PN junction diode if the gate is floated or as gate-controlled diode if the gate voltage is added. Multi-mechanism for the optical radiation observed in this device will be discussed in detail later.

Moreover, as one half of a MOS field effect transistor is a gate-diode (p^+ Source/Drain to n-Substrate with the gate control) in fact, a p-type MOSFET is used to introduce the gate-diode concept into the traditional PN junction as a means of making quantum efficiency enhancement which will make this study valuable as it should be. It should be noted that this device with the structure of PMOSFET does not operate as a transistor, but purely as a diode with gate control of the breakdown voltage of the "p^+ Source/Drain to n-Substrate" junction. The substrate current in a MOS transistor in saturation is not the same as the avalanching substrate current I_{sub}, which is presented in Fig. 3.17, of a transistor connected as a diode.

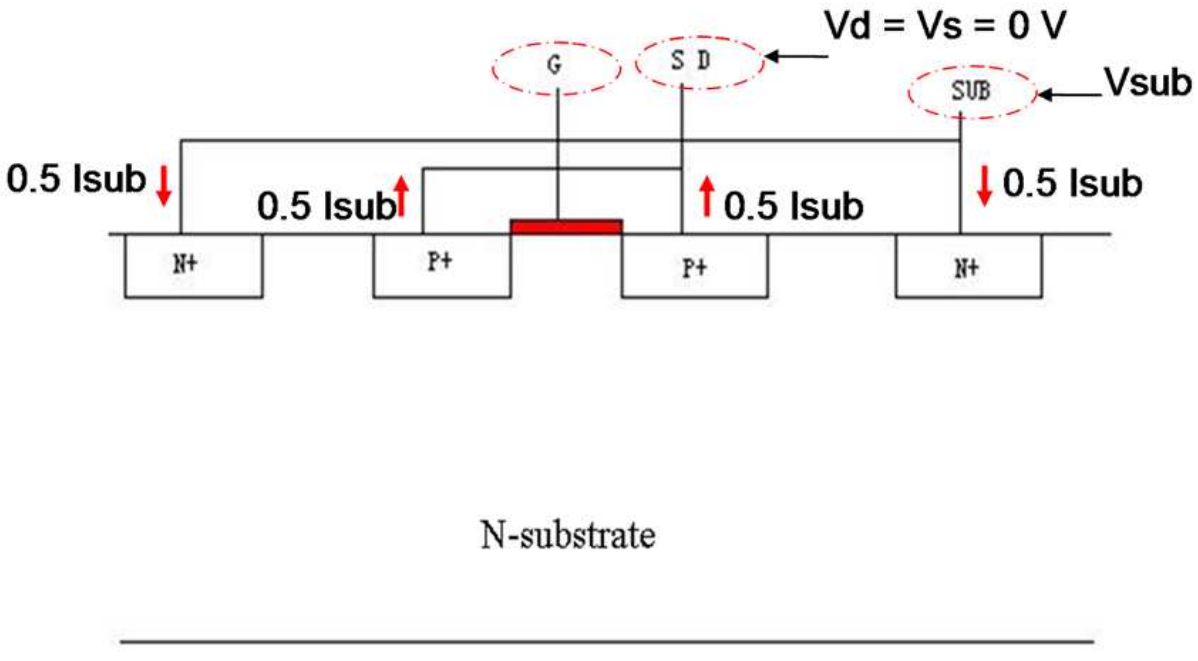


Fig. 3.17 Simplified cross-section view of a single transistor

3.6.3 Emission Efficiency

Considering the measured optical output, the external quantum efficiency could be derived from the relationship

$$\eta_Q = \left(\frac{q\lambda V_{sub}}{hc} \right) \eta_P \tag{3. 22}$$

where η_P denotes the electric-optical power conversion efficiency, q is the elementary charge magnitude, λ is the emitting wavelength, V_{sub} is the applied voltage of the reverse-biased p-n junction, h is the Planck constant and c is the speed of light. The power conversion efficiency is calculated by dividing the externally measured optical output, by the applied total electrical power as applied to the device in terms of current-voltage product, that is,

$$\eta_P = \frac{P_{optical}}{I_{sub} V_{sub}} \tag{3. 23}$$

where $P_{optical}$ is the optical emission power. Therefore, the external quantum efficiency, which is calculated by dividing the number of photons emitted per second by the number of carriers per second, is then expressed as

$$\eta_Q = \left(\frac{P_{optical}}{hc/\lambda} \right) \Big/ \left(\frac{I_{sub}}{q} \right) \tag{3. 24}$$

3.6.4 Enhancement of Emission Efficiency

It has been already presented that the optical emission power is almost linear with the reverse current I_{sub}, whether the Si-PMOSFET device acts as a two-terminal Si-diode LED or as a three-terminal Si gate-controlled diode LED.

Schematics and experimental results are presented in Fig. 3.18 and Fig. 3.19, respectively. In the case of acting as PN junction diodes, the reverse current I_{sub} flows from substrate to drain/source and the light emission is attributed to the avalanche breakdown of the p-n junctions. The relationship between the output optical power and input current is approximately linear, but as the reverse current increases above 30 mA, the output optical emission power will show a trend of saturation as illustrated in Fig. 3.19. In the case of acting as gate-controlled diodes, the reverse current I_{sub} flows from substrate to drain/source as well, the output optical power is linearly proportional to input current, but saturation of optical emission power occurs when the reverse current is higher than 55 mA, as shown in Fig. 3.19.

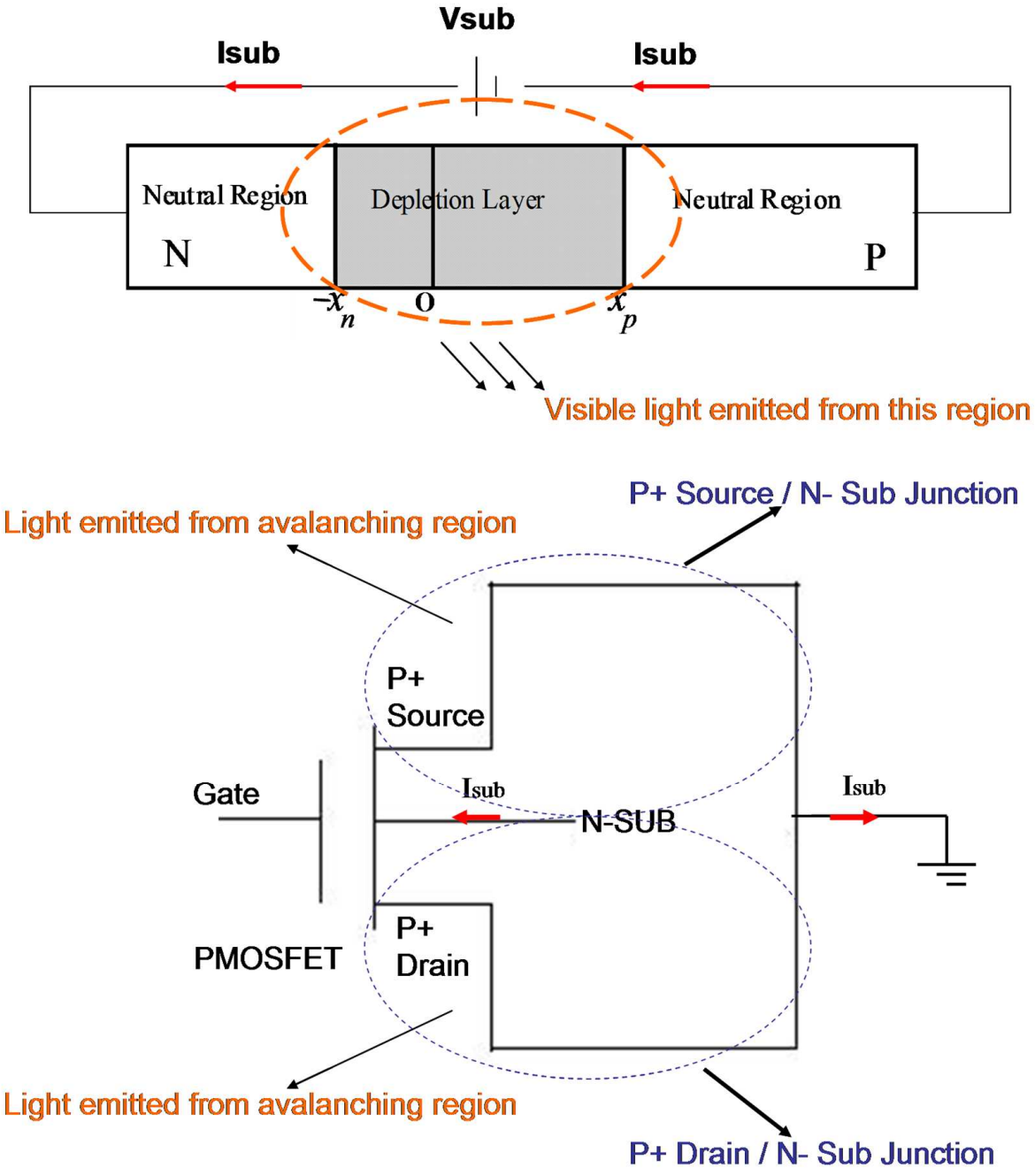


Fig. 3.18 Reverse current I_{sub} flows from n-Substrate to p^+ Source/Drain diffusion region. Simultaneously, light emission will take place in the depletion region where breakdown occurs

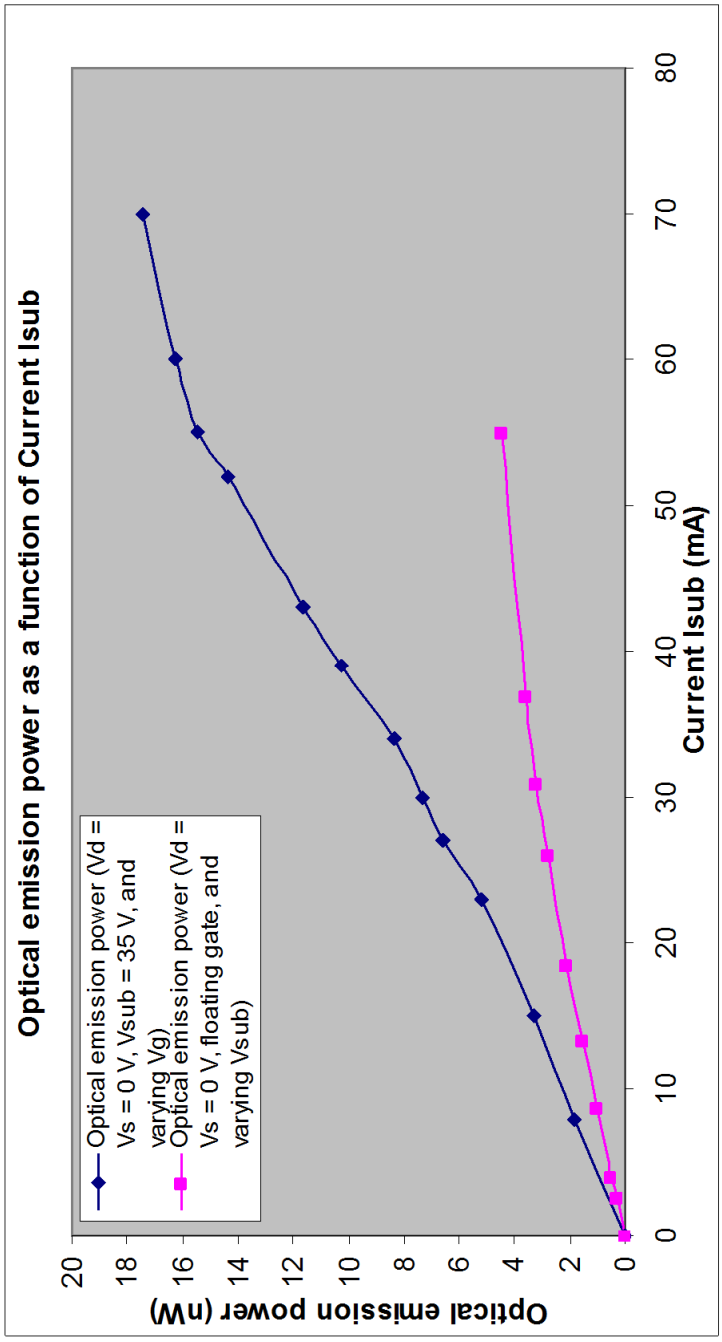


Fig. 3.19 Relationship between the reverse current I_{sub} (i.e., the product of the number of carriers per second and the magnitude of electronic charge) and the optical emission power

Fig. 3.19 also implies that control of increasing current is a potential way to enhance the efficiency of this light source device, regardless of the physical structure of this device. Especially, under the same current condition, the optical output power in gate-controlled diode structure is much higher than that in diode structure. In other words, gate-controlled diode structure will be more efficient than diode structure, for the quantum efficiency depends directly on the number of carriers (which relates closely to the reverse current I_{sub} flowing through the "n-Substrate to p^+ Source/Drain" junction) and the number of photons (which relates closely to the optical emission power).

A larger current means more electron-hole pairs are generated in the "P^+ Source/Drain" / "N-Substrate" depletion region due to the impact ionization. In other words, the more the electron-hole pairs, the higher the possibility that carriers will collide with immobile charged centers to emit photons in the depletion region, thus increasing the light intensity.

Under the operating conditions of floating gate, $V_d = V_s = 0$ V, and varying V_{sub}, the optical emission power is directly controlled by the reversely biased voltage drop V_{sub} across the "P^+ Source/Drain to N-Substrate" junction, which is exclusively dominating the electric field and the impact ionization rate in depletion region. In the way in which reverse current I_{sub} is changed, the reverse bias V_{sub} is able to modulate the optical emission power.

Under the operating condition of $V_{sub} = 35$ V, $V_d = V_s = 0$ V, and varying V_g, this device acts as gate controlled diodes. The reverse bias across "P^+ Source/Drain to N-Substrate" is kept at 35 V, which is unable to make any change on depletion region's condition. However, a positively increased gate voltage V_g will effectively reduce the breakdown voltage across the "P^+ Source/Drain to N-Substrate" junction. As $V_d = V_s = 0$ V, a

positively high V_g will generate a high field between gate and P^+ Source/Drain to sweep electrons onto the P^+ Source/Drain surface just overlapped by insulated gate to produce a field-induced junction shown in Fig. 3.20. The breakdown characteristics of field-induced junction are strongly affected by the surface concentration. At low surface concentration, the breakdown mechanism is avalanche breakdown; at high surface concentration, it is Zener or tunneling breakdown. As such, the breakdown mechanism of "P^+ Source/Drain to N-Substrate" is transiting from avalanche to tunneling while the gate voltage V_g is being increased [43]. In other words, the value of *BV* is being decreased. As a result, reverse current I_{sub} flowing through the "P^+ Source/Drain to N-Substrate" depletion region will increase as the operating reverse bias of the "P^+ Source/Drain to N-Substrate" junction is still 35 V (i.e., V_{sub} is equal to 35 V, and both source and drain are grounded) while the *BV* of "P^+ Source/Drain to N-Substrate" junction is reduced. Due to the linear relationship between the reverse current I_{sub} and the optical emission power, optical emission power can be modulated by adjustment of current I_{sub} at gate voltage V_g. Experimental results, as shown in Fig. 3.20, demonstrate that "gate-controlled diodes configuration" is more efficient than "traditional diodes configuration" in the aspect of light emission. It is possible that the mechanism of Zener breakdown assists silicon PN junction at avalanche breakdown to have more improved performance of light emission with the higher quantum efficiency since the field-induced junction underneath the gate may contribute some parts of the increase in quantum efficiency. On the other hand, the enhanced intensity should be mainly due to two possible reasons. One reason is that electron accumulation under the gate oxide with band bending will take place if the positive gate voltage V_g is applied, thus the rate of minority carrier injection into the n-substrate is determined jointly by the P^+

S/D to N-sub bias (i.e., V_{sub} in this measurement because $V_d = V_s = 0$ V) and the gate to P^+ S/D bias (i.e., V_g in this measurement because $V_d = V_s = 0$ V). At a certain PN junction reverse bias, the injection rate could be significantly higher if the gate voltage V_g is applied to make the diode be a gate-diode. This phenomenon is very similar to the carrier barrier lowing effect that occurs in the lateral bipolar transistor [64].

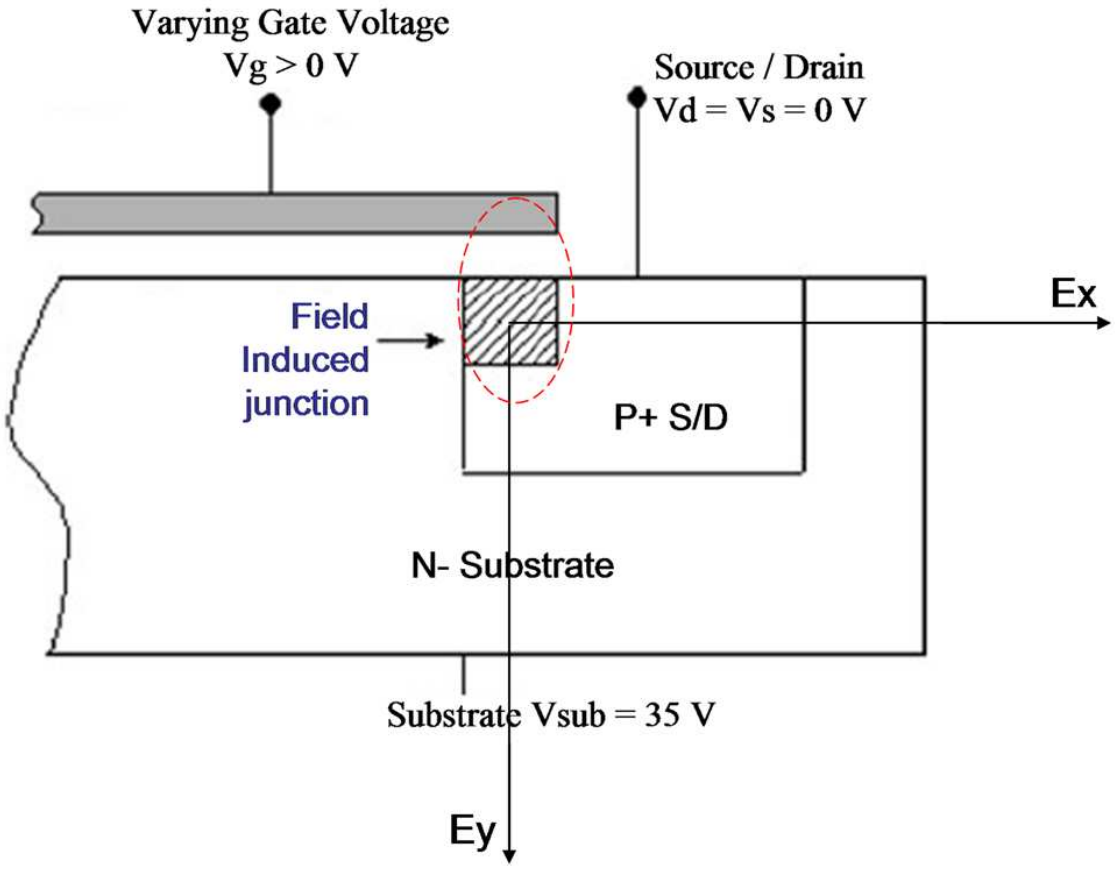


Fig. 3.20 Field-induced junction generated in gate-to-drain overlap region due to the gate voltage induced field. Lateral field E_x is induced by the voltage drop between substrate and source/drain (i.e., substrate voltage V_{sub}), whereas the vertical field E_y is determined by the voltage drop between gate and source/drain (i.e., gate voltage V_g)

The increased injection rate caused by the positively increased gate voltage V_g may lead to the enhanced emission power observed in the three-terminal device, gate-diode. The other reason why the gated-diode has obviously enhanced emission intensity is that the accumulation of electrons at the surface of the N-Substrate confines the photon emission to the surface of the device, thus reducing the optical absorption by the silicon material itself.

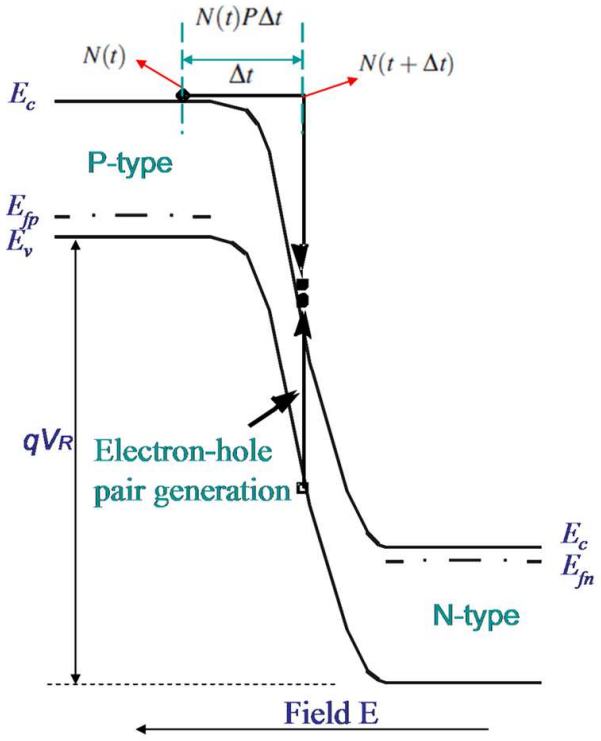
In general, an improved quantum efficiency of the gate-controlled diode Si-LED can be obtained, with respect to avalanche Si-LED operating at the same reverse currents (i.e., the breakdown current I_{sub} in this study).

3.6.5 The correlation between electric field, reverse current, and light intensity

Assuming that the classic Bremsstrahlung model is approximately applicable, the origin of optical radiation observed in the reverse-biased silicon p-n junction could be explained by the Coulomb interaction between impact ionized carriers and charged centers in the depletion region. The charged center, also known as quantum dot, is an artificial atom in fact even if it has a mass that is approximately equal to the one of atom. Besides the properties of atom such as discreet energy level and shell structure, the artificial atom, quantum dot, including tenability and comparability of level spacing, Coulomb scattering, and thermal energy is more advanced than natural atom by allowing transport measurement.

Since the number of carriers is proportional to that of emitted photons, the number of light spots increases with the current rather than with individual spots growing brighter.

It is concluded that the breakdown current is carried through the junction by these localized light emitting spots (i.e., the quantum dots).



$$N(t) - N(t+\Delta t) = N(t)P\Delta t$$

As Δt is very small

$$\frac{dN(t)}{dt} = \lim_{\Delta t \to 0} \frac{N(t+\Delta t)}{\Delta t} = -PN(t)$$

$$N(t) = N_0 \exp(-Pt)$$

Substituting $N(t)P\Delta t$ into $N(t) = N_0 \exp(-Pt)$

$$N_0 P \exp(-Pt)dt$$

Integrating over the time variable dt.

$$\tau = \frac{1}{N_0}\int_0^{\infty} N_0 P \exp(-Pt)dt = \frac{1}{P}$$

$$N(t) = N_0 \exp\left(-\frac{t}{\tau}\right)$$

$$N(t) = N_0 \exp\left(-\frac{d}{\lambda_m}\right)$$

Fig. 3.21 A schematic illustration of the injected electron in the potential-distance space; the lucky electron travels a distance *d* (corresponding to time interval Δt) to gain the energy needed to generate photons; parameters are defined as follows: *N (t)* is the number of electrons at the moment *t*, *N (t + Δt)* is the number of electrons at the moment $t + \Delta t$, *P* is the scattering probability, N_0 is the number of electrons at $t = 0$, τ is the mean-free-time, λ_m is the mean-free-path, and *d* is the distance an electron has been accelerated in the time interval *t*.

Furthermore, an expression of the statistical distribution of photoelectron count can be derived from the classic model of Bremsstrahlung. Assuming that the probability of registering n counts during a time interval T is $p(n,T)$, the probability of registering a single pulse over a very short counting time $(T, T+\Delta T)$ is proportional to the instantaneous light intensity $I(T)$ and the counting interval ΔT. In other words,

$$\frac{\partial}{\partial T} p(n,T) = \sigma I(T)\left[p(n-1,T) - p(n,T)\right] \tag{3.25}$$

where σ is a proportionality constant that includes both the quantum efficiency of the photo-cathode and any factors related to detection geometry.

Through an ensemble average over the distribution function $P(W)$ for the random variable W, the probability $P(W)dW$ of measuring the integrated intensity to be between W and $W+dW$ will lead the approximate expression of the photon count distribution to be

$$p(n,T) = \int_0^\infty \frac{1}{n!}(\sigma W)^n e^{-\sigma W} P(W) dW \tag{3.26}$$

This result above, which is also known as Mandel's formula [65], is equivalent to taking the generating function to be

$$G(\lambda, T) = \exp(-\lambda \sigma W(T)) \tag{3.27}$$

where the average is over the distribution $P(W)$. Therefore, it can be obtained that energy distribution function $f(E_{photon})$ of photon intensity can be given by

$$f(E_{photon}) \sim \exp\left(-\frac{E_{photon}}{kT_e}\right) \tag{3.28}$$

where E_{photon} is the energy of photon and T_e is the effective temperature.

Regarding lucky-electron model of hot-electron injection, the distribution of the density of carrier is presented in Fig. 3.21. The energy distribution of lucky carrier becomes $f(E_{carrier}) \sim \exp\left(-\frac{E_{carrier}}{q \times \mathrm{E} \times \lambda_m}\right)$ by taking the field E into consideration. As $q\mathrm{E}\lambda_m = kT_e$, the distribution, which is based on Maxwell-Boltzmann approximation, can be expressed as

$$f(E_{carrier}) \sim \exp\left(-\frac{E_{carrier}}{kT_e}\right) \tag{3. 29}$$

where $E_{carrier}$ is the energy of photon and T_e is the effective temperature of carrier. The similarity between Eq. (3. 29) and Eq. (3. 28) in exponential distribution implies the linear relationship between the breakdown reverse-current and the optical emission power [66]. The deduction above is in good agreement with the measured results shown in Fig. 3.4 and Fig. 3.16. Integrating the distribution function over the emitting wavelength, the total electroluminescence intensity can be obtained

$$\Phi(h\nu) \sim \left(\frac{1}{h\nu}\right)\int_{h\nu}^{\infty} f(E_{photon})dE \tag{3. 30}$$

Using the formula of photon-emission-rate in which the phenomenon of continuous X-ray spectrum (i.e., Bremsstrahlung) is theoretically interpreted, the solution for $\Phi(h\nu)$ is

$$\Phi(h\nu)d\nu \sim \left(\frac{1}{h\nu}\right)\exp\left(-\frac{1}{h\nu}\right) \qquad \text{for } h\nu < E_c$$

$$\Phi(h\nu) \sim \left(\frac{1}{h\nu}\right) \qquad \text{for } h\nu > E_c \tag{3. 31}$$

where $h\nu$ is the energy of photon and E_c is the energy level at the lower edge of conduction band [67]. As the integration above covers the whole region of conduction band, it is suggested that Eq. (3. 31) is a reasonable model that can testify to the existence

of intraband transition in the conduction band (i.e., the *c-c* transition). On the other hand, Eq. (3. 28) can be re-written as

$$f\left(E_{photon}\right) \sim \exp\left(-\frac{E_{photon}}{q \times \mathrm{E} \times \lambda_m}\right) \tag{3. 32}$$

where the mean-free-path λ_m is a constant.

As discussed previously, optical emission power increases with operating voltage (for Si-diode LED, it is the reverse-bias substrate voltage V_{sub}; for Si gate-controlled-diode LED, it is the gate voltage V_g). In fact, the light intensity is proportional to the peak electric field in the depletion region. Assuming the condition for breakdown process is initiated by electrons or by holes, the reverse current I_{sub} is a product of the multiplication factor *M* and the leakage current I_{R0} of the reverse-biased "P^+ Source/Drain to N-Substrate" junction without any breakdown-producing mechanism in the depletion region. That is,

$$I_{sub} = MI_{R0} \tag{3. 33}$$

At the same time, *M* can be expressed as

$$M = \frac{1}{1-\int_0^W \alpha dx} = \frac{1}{1-\int_0^W A\exp\left(-\frac{B}{\mathrm{E}}\right)dx} \tag{3. 34}$$

where α is the impact ionization rate, *A* and *B* are constants, E is the electric field in the depletion region, V_R is the reverse bias of p-n junction, *BV* is the breakdown voltage, and *n* varies between 3 and 6 for silicon and is mainly a function of junction material parameters. Measured results, for Si-diode LED and for Si gate-controlled-diode LED, in Fig. 3.20, indicate that optical emission power in Si gate-controlled-diode LED is much higher than that in Si-diode LED. Furthermore, Si gate-controlled-diode LED having a much stronger light emission than Si-diode LED shows the evidence that the variation of gate voltage

could be treated as a novel method to realize quantum efficiency enhancement in the reverse-biased silicon p-n junctions [66]. Regarding the distribution of light intensity, Eq. (3. 32) provides the evidence that light intensity increases with electric field E [67]. A comparison of the simulated results in Fig. 1.5 and Fig. 1.8 indicates that the peak field in Si gate-controlled-diode LED is about one order of magnitude higher than that in Si-diode LED. Eq. (3. 33) and Eq. (3. 34) show that reverse current I_{sub} actually increases with electric field E. Since optical emission power is proportional to reverse current I_{sub}, it is evident that in Si gate-controlled-diode LED the optical emission power is relatively high because of the much higher peak field. At last, it comes to the most dazzling achievement that the gate voltage V_g is able to increase the field more effectively than the reverse-bias of the p-n junction, thus realizing the enhancement of light emission in the reverse-biased silicon p-n junctions.

It is noted that the two operating modes (i.e., Si-diode and Si gate-controlled-diode) are realized in the same device structure (i.e., a Si-PMOSFET device). In Si-diode, the electric-optical power conversion efficiency and the external quantum efficiency (EQE) are about 10^{-9} and 10^{-8}, respectively [68]. In Si gate-controlled-diode, the electric-optical power conversion efficiency and the external quantum efficiency (EQE) are about 10^{-8} and 10^{-7}, respectively. The real value (i.e., internal quantum efficiency, IQE) is beyond that. Due to the difficult in measuring the optical power output inside the device, a reasonably derived theoretical limit of light emission efficiency is presented alternatively. The internal quantum efficiency $\eta_{\text{int}\,ernal}$ gauges what fraction of transition of the high energy carriers produced at breakdown in the reverse-biased p-n junction are radiative and therefore lead to photon emission. The reverse current I_{sub} is determined by the total rate of transitions

whereas the number of photons emitted per second Φ_{ph} is determined by the rate of optical radiations.

$$\eta_{\text{int ernal}} = \frac{\Phi_{ph}}{I_{sub}/q} = \frac{P_{opt(\text{int ernal})}/h\nu}{I_{sub}/q} \tag{3.35}$$

where $P_{opt(\text{int ernal})}$ is the optical power generated internally and I_{sub}/q is the number of electrons generated per second. The extraction efficiency $\eta_{extraction}$ is defined as a ratio between photons emitted into the free space and photons emitted by the active region. In a real diode the extraction efficiency never reaches unity. There are many factors, such as the re-absorption of the photon by the substrate or by the metallic contact, having an influence on photon emission into the free space. Also the phenomenon of total internal reflection, also referred to as the trapped light phenomenon reduces the ability of the light to escape from the semiconductor. The extraction efficiency is defined by

$$\eta_{extraction} = \frac{P_{opt}/h\nu}{P_{opt(\text{int ernal})}/h\nu} \tag{3.36}$$

where P_{opt} is the optical power emitted into free space. Next, the external quantum efficiency is equivalent to the ratio of number of useful photons to the number of injected charge carriers.

$$\eta_{external} = \frac{P_{opt(external)}/h\nu}{I_{sub}/q} = \eta_{\text{int ernal}}\eta_{extraction} \tag{3.37}$$

where $P_{opt(external)}/h\nu$ is the number of photons emitted into free-space per second and I_{sub}/q is the number of electrons generated per second. The $\eta_Q - I_{sub}$ characteristics as measured in different biasing conditions are shown in Fig. 3.22. It provides the evidence

that quantum efficiency is different in different operating conditions; especially higher quantum efficiency is obtained although the driving current I_{sub} is much lower [69].

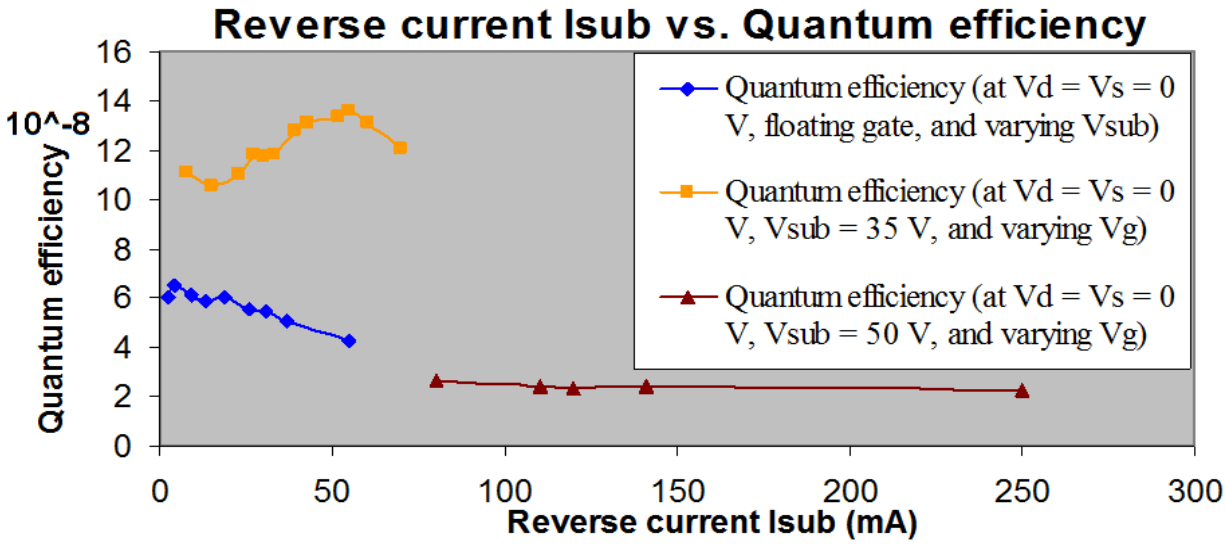


Fig. 3.22 External quantum efficiency as a function of reverse current I_{sub} that flows through the p^+ Source/Drain to n-Substrate junction

The internal efficiency should be much higher than the external efficiency because a number of looses occur as a function of different mechanisms within the silicon device itself. For instance, emitted photons with energies greater than the silicon band-gap energy are absorbed by the bulk silicon and poly-Si gate, and some of the light is reflected at the Si-SiO_2 interface. Most recently, Cheng *et al.* proposed an approach to increase the external quantum efficiency of metal-oxide-semiconductor light-emitting diodes (MOSLEDs) made on the SiO_x film by narrowing the Si quantum dots (Si-QDs) to enhance electron-hole recombination [70]. On the other hand, Lin *et al.* used the nanopillar roughened Si surface to improve the turn-on characteristics of the MOSLEDs [71]. Regarding the power loss

when coupling light from the Si-PMOSFET LED to the fiber or photo-receiver, a simple, robust, and sensitive fiber interferometer could be used in the photonic-electronic-integrated-circuits (PEICs) domain [72].

In addition, light emission from silicon MOSFET device operating in the saturation region is observed. The observation provides the direct evidence for the phenomenon of photon generation in the substrate of the MOSFET device. In the case above, photon emission rate is determined by two parameters: the number of carriers flowing through the channel and the probability of photon emission. The emitted photon flux N_{PH} is approximated as [73]

$$N_{PH} \approx \frac{I_S}{q}\left(V_{DS} - V_{DSsat}\right)\exp\left(\frac{-\beta}{V_{DS} - V_{DSsat}}\right) \tag{3.38}$$

where I_S, V_{DS}, and V_{DSsat} are the source current, drain-source voltage and saturation voltage, respectively, while β is a process dependent constant. On the other hand, substrate current I_{sub} can be derived from I_S

$$I_{sub} = I_S\left(A_i / B_i\right)\left(V_{DS} - V_{DSsat}\right)\exp\left[-L_e B_i / \left(V_{DS} - V_{DSsat}\right)\right] \tag{3.39}$$

where A_i and B_i are the ionization constants and are mainly a function of silicon material parameter itself, and L_e is the effective ionization length in the breakdown region. The similarity between Eq. (3. 29) and Eq. (3. 32) provides the evidence that emitting light intensity in this case is linear with the substrate current [74]. It is noted that this substrate current is different from the previously mentioned reverse-current in the reverse-biased p-n junctions.

3.6.6 Physical mechanisms

The physical mechanism that is probably related to the photon emission is further investigated in this section to prove that light emission is linearly related to the reverse current. Since a charged particle (i.e., electron or hole) can be deflected by the Coulomb forces of the artificial atoms (i.e., positively and negatively charged centers that are immobile in the depletion region) in such a way that energy and momentum are conserved, the photon emission energy may be provided by the loss of kinetic energies during charged-particle collisions with artificial atoms.

More specifically, when a free electron approaches the positively charged nucleus, it experiences an attractive force that deflects its electron and causes the electron to accelerate. This sudden acceleration causes the emission of a pulse of radiation in the form of a photon. This in turn causes the electron to los kinetic energy, and it slows down. The emitted radiation is, therefore, called the braking or impulse radiation, or, more, commonly, the Bremsstrahlung [75]. As a result, the linearity between the reverse current, I_{sub}, flowing through the p-n junctions and the optical emission power can be reasonably interpreted by the theory of carrier interaction with charged centers [66].

The physical model of lucky-electron model [76] is taken into account to investigate the mechanisms behind the photon emission. Considering that in the depletion region there are N_0 electrons at time $t = 0$, let λ be the probability per unit time that an electron will decay (i.e., lose some kinetic energies), in one way or another. The probability that an electron will not decay within a short time interval Δt is then $p = 1 - \lambda \Delta t$. That is, pN_0 electrons will remain without decay after Δt, after $2\Delta t$, and so on. Therefore, within n sequential time intervals, adding up to a total time period, t, the number of electrons

remaining without decay in the nth time interval, $N(t)$, is then $N(n\Delta t)=N(t)=p^n N_0$. As $\Delta t \to 0$ and $n \to \infty$, it is obtained

$$\frac{N}{N_0}=\lim_{n\to\infty} p^n=\lim_{n\to\infty}(1-\lambda\Delta t)=\lim_{n\to\infty}\left(1-\lambda\frac{t}{n}\right)^n=\exp(-\lambda t) \tag{3.40}$$

The above mentioned exponential law of decay, corresponding reasonably well with the distribution function of photons, implies that the light emission should be probably attributed to the collision induced kinetic energy loss. In addition, the relationship between probability λ and mean-free-time τ_m is given by [66]

$$\lambda=\frac{1}{\tau_m} \tag{3.41}$$

Accordingly, the mean–free–path (MFP) of electron-phonon interaction as a function of temperature is given by [77]

$$l_m=l_0\tanh\left(\frac{E_{p0}}{2kT_e}\right) \tag{3.42}$$

where l_0 is about 76 Å for silicon material, E_{p0} is the optical phonon energy, k is the Boltzmann's constant, and T_e is the effective temperature. If the space-charge region of the p-n junction is approximately treated as micro-plasma, the electron-ion Breamsstrahlung power emitted by the volume of plasma V_p into the solid angle $d\Omega$, and in the wavelength interval $\lambda_s \to \lambda_s + d\lambda_s$, is [78]

$$P_B d\Omega d\lambda_s = 2.09\times10^{-36}\left(\frac{n_e n_i}{\lambda_s^2\sqrt{kT_e}}\right)\exp\left(-\frac{1.24\times10^{-4}}{\lambda_s kT_e}\right)V_p\frac{d\Omega}{4\pi}d\lambda_s(W) \tag{3.43}$$

where $P_B \infty \sum_Z \frac{Z^2 n_i}{n_e}$ is the probability of Bremsstrahlung radiation, n_e in units of cm^{-3} is the concentration of electrons, n_i is the intrinsic concentration of silicon, the unit of λ_s is cm. The model presented in Eq. (3. 43) applies the "lucky electron" concept to describe impact ionization, and takes the hot-electron injection effects into account, so the probability of emission of a photon with energy in the interval $[hv, h(v+\Delta v)]$ is given by

$$Q_{V_{pv}v} dV_p dv = \frac{32\pi^2 \sqrt{\varepsilon_r} q^6 N_i}{\left(\sqrt{3}c\right)^3 2m^* \left(\varepsilon_r^*\right)^2 \left(4\pi\varepsilon_0\right)^3 E \cdot hv} dv \tag{3. 44}$$

where ε_r is the relative dielectric constant of silicon, ε_r^* is the effective dielectric constant of silicon, E is the electron energy, N_i is the volume density of the Coulomb scattering centers and c is the speed of light in vacuum. The number of photons with energy between hv and $h(v+\Delta v)$ is

$$P_V dv dE = [Q_V dv] \cdot [f(E) \cdot D(E) \cdot V(E) dE] \tag{3. 45}$$

where $D(E)$ is the density of states, $f(E)$ is the energy distribution of the electrons, and $V(E)$ is the velocity distribution of the electrons. Therefore, the energy radiated in the frequency range $[v, v+dv]$ per unit due to all hot electrons with initial kinetic energies greater than hv is given by

$$W_v dv = \int_{hv}^{\infty} P_V hv dv dE \tag{3. 46}$$

Bremmstrahlung radiation is emitted when hot electrons are decelerated in the electrostatic field of the impurity atoms. As the energy of the emitted photons reflects the energy of the hot electron, there should be a close correlation between the photon energy distribution and the energy distribution of the electron population. In fact, a theoretical

model of Bremsstrahlung radiation derived from the integration of Eq. (3. 46) presents that Bremsstrahlung mechanism can explain the linear relationship between reverse current and light intensity in theory [79]. The linearity between the two parameters is also observed experimentally [66].

Using an overlapping charged-coupled-device gate structure to shift the hot-electron population from the drain junction to the inter-electrode gap, *Wong* [80] showed that, for photons with energies slightly above the energy of band-gap, Bremsstrahlung is not the only mechanism that is responsible for the hot-carrier-induced photon emission. Other experimental and theoretical studies have also suggested that Bremsstrahlung is not a dominant mechanism that is responsible for the hot-electron-induced photon emission [81], [82]. Akil *et al.* summarize light emitting processes using a multi-mechanism model for photon generation by silicon p-n junctions [35].

CHAPTER 4: Modulation Speed of the Si PMOSFET Device

In this chapter, the switching characteristics as associated with p+ n gated MOSFET silicon LED are reviewed. By employing the insulated-gate terminal, which allows the adjustment of P^+ source/drain to N-substrate junction breakdown voltage, it is demonstrated that the electro-optical modulation in the Si-PMOSFET device operates as gate-controlled diodes. The PMOSFET device can operates as Si-diode LED or a Si gate-controlled diode LED. The main features of switching transitions of Si-diode LED and Si gate-controlled diode LED are characterized, and a model is developed to explain the modulation speed, which is then reviewed. The upper limit derived value for the expected maximum modulation of the device could be in the range of a few hundred GHz. According to the best of my knowledge, despite the low efficiency, the Si-PMOSFET light-emitting device will be a potential key component for silicon photonic integrated circuits for future computing I/O applications.

4.1 Speed limitation in the silicon modulator

The intrinsic modulation speed of a silicon modulator based on the free carrier dispersion effect is determined by how fast the free carriers are injected. Different modulator device configurations have different free carrier dynamics mechanisms. Therefore, the carrier lifetime is very important for analyzing the response of high-speed semiconductor devices.

In silicon (indirect band-gap semiconductor), the carrier lifetime strongly depends on the concentration of recombination centers. The rate of generation of electron-hole pairs in steady state is given by [83]

$$U = \frac{\sigma_p \sigma_n v_{th} N_t \left(pn - n_i^2\right)}{\sigma_n \left[n + n_i \exp\left(E_t - E_i \diagup kT\right)\right] + \sigma_p \left[p + n_i \exp\left(E_i - E_t \diagup kT\right)\right]} \quad (4.1)$$

In a reverse-biased p-n junction, the electric field increases with the applied revere voltage to sweep the carriers out of the depletion region, and the concentrations of carriers are reduced below their equilibrium concentrations. This leads Eq. (4. 1) to

$$U = \frac{\sigma_p \sigma_n v_{th} N_t n_i}{\sigma_n \exp\left(E_t - E_i \diagup kT\right) + \sigma_p \exp\left(E_i - E_t \diagup kT\right)} \equiv -\frac{n_i}{2\tau_0} \quad (4.2)$$

where τ_0 is defined as the effective lifetime within a reverse-biased depletion region. Since one electron-hole pair generated provides one electronic charge to the external circuit, the current due to generation within the depletion region is given by

$$I_{gen} = 0.5q\left(n_i / \tau_0\right) W_D A \quad (4.3)$$

where I_{gen} is equivalent to the reverse current I_{sub} in the PMOSFET device working in the mode of Si-diode LED. W_D and A are the depletion region width and the cross-sectional area of the p^+ Source/Drain to n-Substrate junction, respectively. Again, the proposed Si-PMOSFET device can be utilized to realize both the Si-diode LED (*without the function of gate voltage*) and the Si gate-controlled-diode LED (*with the function of gate voltage*) simultaneously.

In the diode mode, some characteristics of the Si-PMOSFET device are shown in Fig. 4.1. For the reverse biased p-n junction diode, the free carrier density change in silicon is achieved through current injection. In other words, the light intensity is modulated by the reverse current directly. Since the minority carrier lifetime in Si is in general relatively as long as 1μs–100 ns, the Si-diode LED's speed will be limited to the MHz range. Regarding

Fig. 4.1, the speed limitation of the reverse-biased Si-diode modulator can be simply considered due to the device *RC* time constant and the capacitance of the p^+ Source/Drain to n-Substrate junction is primarily determined by the depletion width. The per-unit length capacitance of the reverse-biased p-n junction diode is given by

$$C_{dep} = (\varepsilon_{si}/W_D)L_m \tag{4. 4}$$

where ε_{si} is the silicon permittivity and L_m is the length of the p-n junction that is related to the metallurgical channel length in the PMOSFET device. As the depletion width W_D is reveres bias V_{sub} dependent, the capacitance C_{dep} is also dependent of the driving voltage V_{sub}.

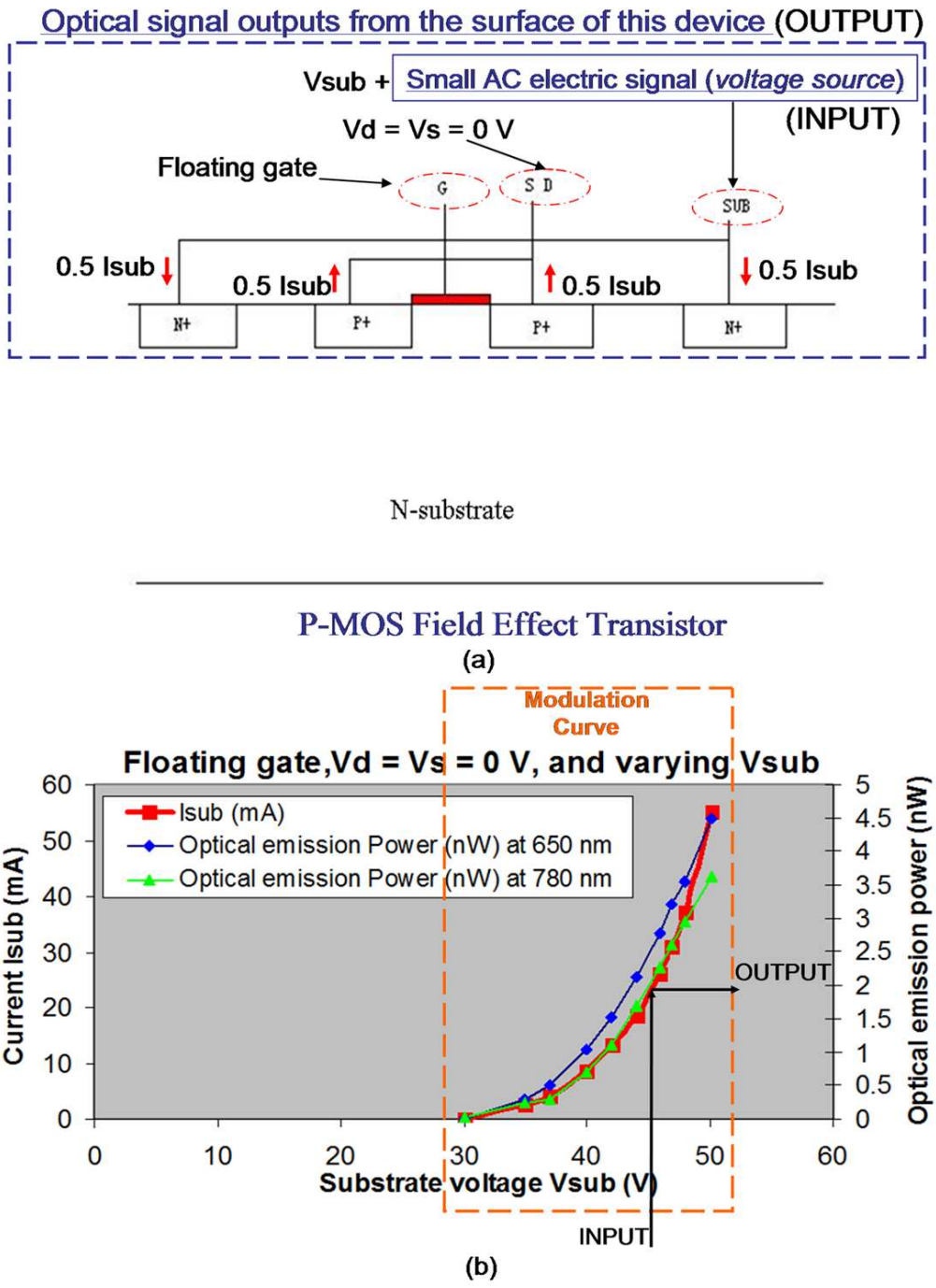


Fig. 4.1. (a) V_{sub}, a DC source, is the reverse bias across the "p^+ S/D to n-Sub" junction. (b) V_{sub} is varied to realize optical modulation in the two-terminal device. The transfer function between the electric input and the optical output is determined by the slope of the Modulation Curve

Fig. 4.2 shows the modeled direct current (DC) capacitance of the p^+ Source/Drain to n-Substrate junction diode with $N_a \sim 10^{19} cm^{-3}$ (where N_a is the Source/Drain doping concentration) and $N_d \sim 10^{16} cm^{-3}$ (where N_d is the substrate doping concentration). It is seen that that the capacitance decreases with an increase in the bias voltage V_{sub}, because the depletion width increases with an increase in the bias V_{sub}. Although there is a bias dependent DC capacitance change, the high-speed response of the Si-diode LED may be analyzed using the *RC* time constant with a capacitance at the DC bias voltage.

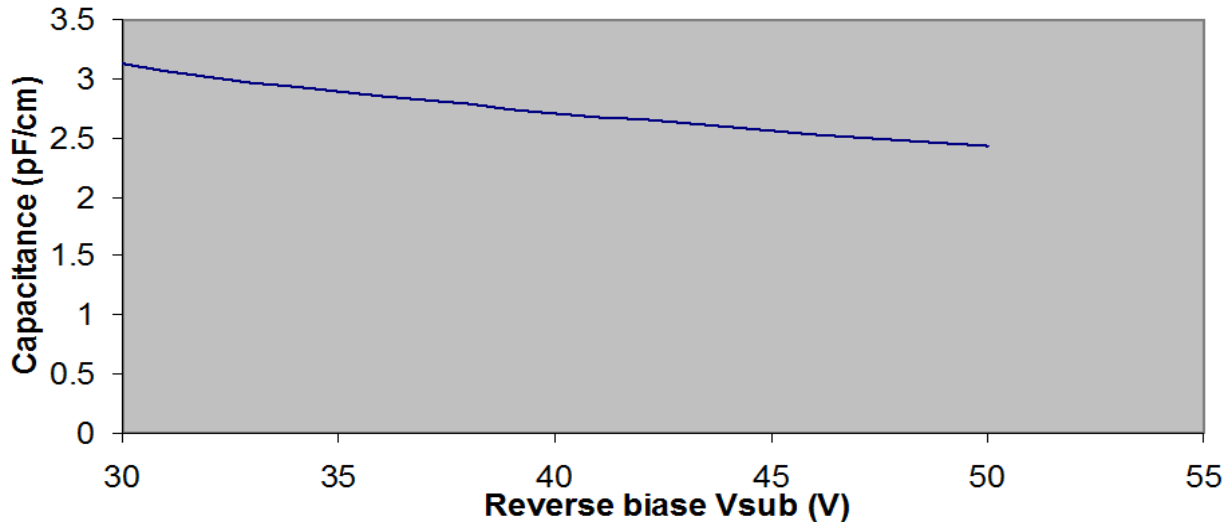


Fig. 4.2. Modeled capacitance of the reverse-biased "p^+ S/D to n-Sub" junction diode per unit length as a function of the DC reverse bias V_{sub}

In the gate-controlled-diode mode shown in Fig. 4.3, the Si-PMOSFET device will operate on the principle of the MOS capacitor and not on the standard p-n junction. The natural carrier lifetimes are replaced by the discharge time of a metal-oxide-semiconductor (MOS) capacitor-based LED (i.e., Si gate-controlled-diode LED). The lifetime of MOS-

capacitor LEDs should be controlled via the capacitor discharge time, with speeds approaching those of a Schottky-diode configuration when the gate oxide is ultrathin [84].

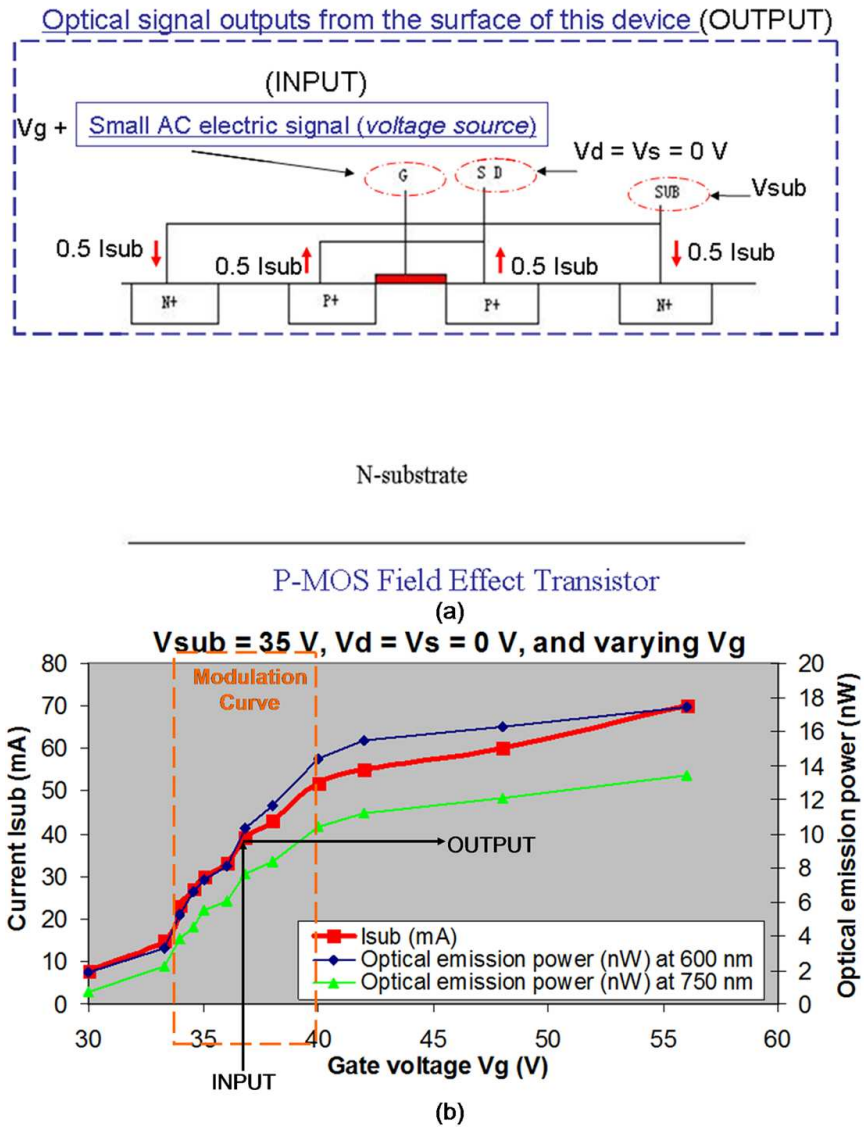


Fig. 4.3 (a) V_g, a DC source, is the gate voltage. V_{sub}, a DC source, is the reverse bias across the "p^+ S/D to n-Sub" junction. (b) V_g is varied to realize optical modulation in the three-terminal device. The transfer function between the electric input and the optical output is determined by the slope of the Modulation Curve.

In other words, for the MOS capacitor-based reverse-biased p-n junction electro-optic modulator, the free carrier modulation is achieved through the electric-field effect. Recalling the relationship between electric field and breakdown voltage, the modulation in Si gate-controlled-diode LED could be reasonably explained by Fig. 4.3.

The speed of the gate-controlled-diode modulator is also determined by the *RC* time constant, so the modulator speed can be designed by properly choosing the device capacitance and resistance. In the PMOSFET device, the capacitance per unit length is approximately given by

$$C_{ox} = (\varepsilon_{ox} / t_{ox}) L_{gate} \tag{4.5}$$

where ε_{ox} is the oxide permittivity and L_{gate} is the gate length of the PMOSFET device. The total series resistance of the device is mainly due to the doped silicon regions because the metal contact has very small resistance assuming a good Ohmic contact between silicon and metal. Assuming the driving voltage is constant along the unit length of the MOS capacitor modulator, the total series resistance per unit length is given by

$$R = R_P + R_N = \rho_P \frac{L_p}{W} + \rho_N \frac{L_N}{W} \tag{4.6}$$

where ρ_P and ρ_N are the resistivity of p^+ Source/Drain and n-Substrate, respectively [85]; L_P and L_N are the length of p^+ Source/Drain and n-Substrate, respectively; W is the width of the PMOSFET device. The 3-dB bandwidth due to the *RC* time limit is given by the well-known formula

$$f_{3dB} = 1/(2\pi RC) \tag{4.7}$$

Fig. 4.4 shows details about the composition and structure of the Si-PMOSFET light-emitting device structure which is realized using 3-μm field oxide-based technology. The structure consists of a heavily doped P^+, $\sim 10^{19}$ cm^{-3} doped layer of ~0.5 μm thickness which is defined and realized in a 0.8–1.2 Ω•cm n-type silicon substrate by means of appropriate ion beam implantation, masking and acceptor activation procedures. Appropriate N^+ guard-ring structures are placed on the periphery of the P^+ diffusion region in order to ensure a uniform and planar breakdown at the planar P^+ N interface. The field oxide and metal layers are etched away in order to expose the P^+ layer to the surface and to enable effective injection of energetic electrons into the junction by means of the electron beam. The device used in this study is a conventional poly-silicon gate p-channel MOSFET, with gate oxide thickness of 4000 Å. The width of the device is ~175.5 μm and the channel length is ~6 μm. The poly-silicon gate thickness is ~400 Å.

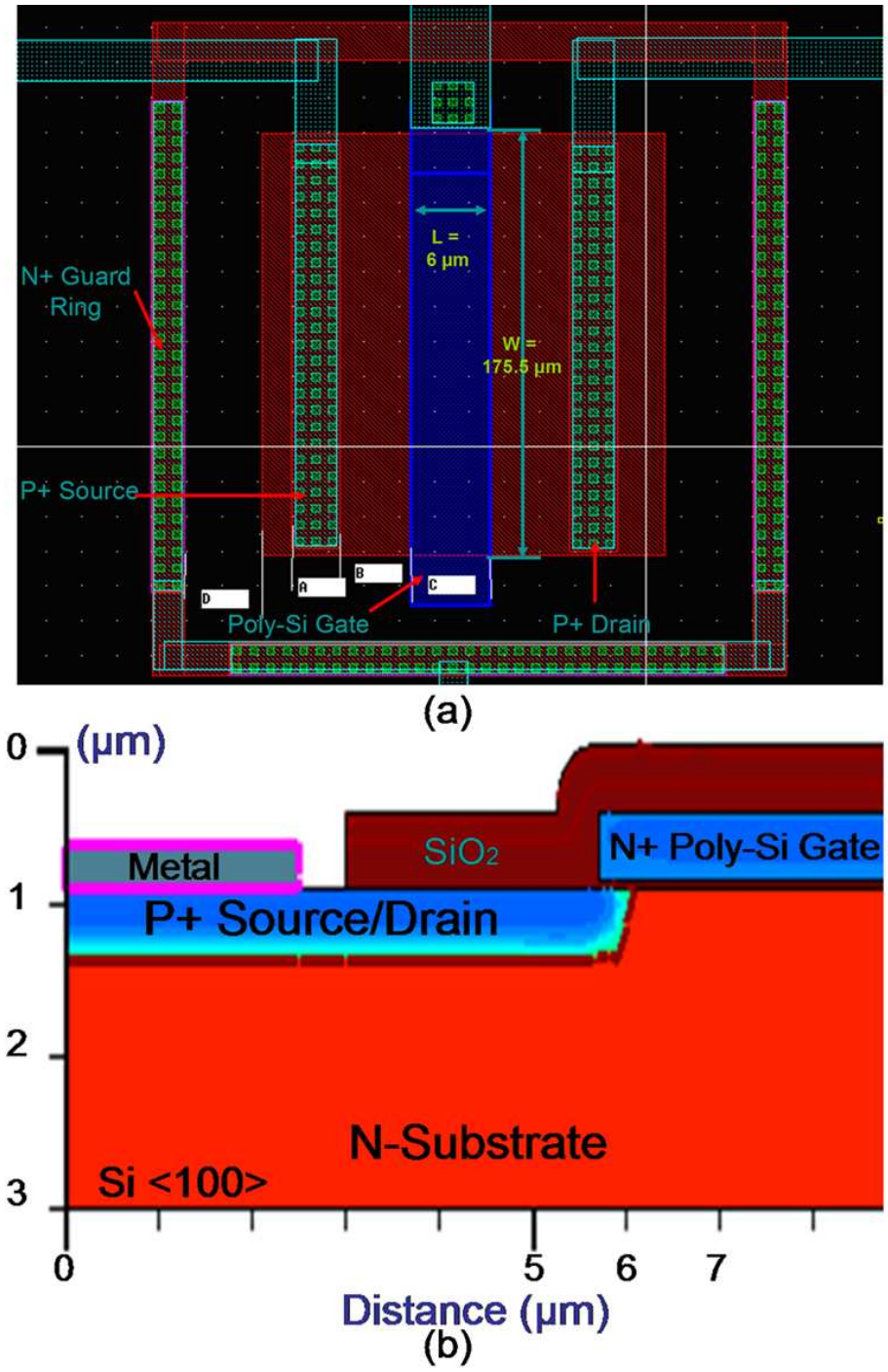


Fig. 4.4. Structural details of a Si-PMOSFET device which are used for analysis in this work: (a) Top-view planar layout of the silicon device using 3 micro Bi-CMOS technology; (b) Cross-section of one half of the Si-PMOSFET device

These important device parameters above are given in Fig. 4.4. Taking these values into Eq. (4.5)–(4.7), it is obtained that C_{ox} ~4.366×10^{-11} F/cm, R ~1.743×10^{-11} Ω·cm, and f_{3dB} ~0.21 THz. Fig. 4.5 shows the simulated 3-dB bandwidth of the MOS capacitor modulator as a function of doping concentration. In the simulation, it is assumed that the p$^+$ Source/Drain and n-Substrate doping density is the same (i.e., N_a and N_d have the same value). It is observed from Fig. 4.5 that the MOS capacitor modulator is clearly capable of high data rate operation. Of course, photon absorption due to the silicon absorption coefficient is also dependent on the doping concentration. Therefore, there should be a balance between the device speed and the optical loss for the MOS capacitor-based modulator.

It is noted that the device speed described above is the intrinsic speed, that is, driving voltage is constant along the modulator and driver impedance is assumed to be zero. In real device operation, the driver impedance as well as the RF signal attenuation along the modulator should be taken into account. Hence, the speed of the combined driver and modulator depends on the drive schemes.

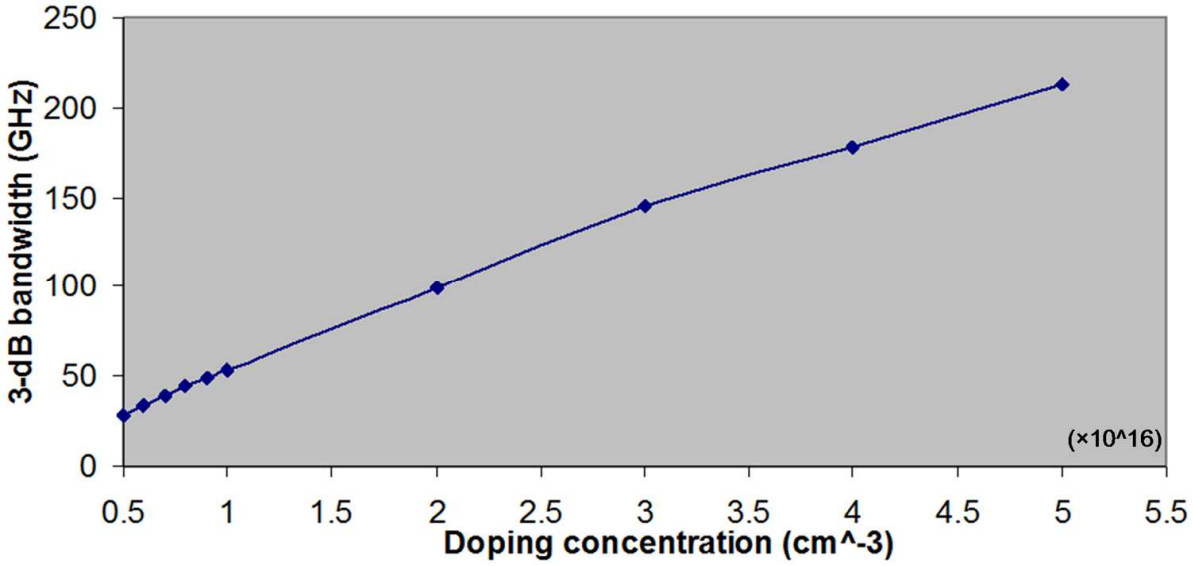


Fig. 4.5 Modeled 3-dB bandwidth of the MOS capacitor modulator (i.e., Si gate-controlled-diode LED) as a function of doping concentration

The optical power emitted from the reverse-biased p-n junctions in the wavelength range 400 to 900 nm is just few nanowatts. This prohibits to measure in a meaningful way the emitted power. However, since the actual speed is somewhat lower than the intrinsic speed, a maximum frequency of few tens of GHz could be estimated.

In addition, a comparison between the Si-diode LED and Si gate-controlled-diode LED in the field of phase modulation can be obtained from the modulation curves shown in Fig. 4.1(b) and Fig. 4.3(b). For Si-diode LED, the depletion width of the reverse-biased p-n junction depends on the bias voltage and doping concentration; the charge density change associated with the depletion width change due to the bias voltage V_{sub}. Because the depletion width is not linearly dependent on the drive voltage V_{sub}, it is similarly expected that the phase shift not to be linearly dependent on the voltage. Accordingly, the modulation curve shown in Fig. 4.3(b) is non-linear. This is quite different from the MOS-

capacitor modulator, which shows linear dependence of the phase shift vs. the drive voltage V_g. Accordingly, the modulation curve shown in Fig. 4.3(b) is almost linear.

4.2 Analyses of the modulation characteristics as associated with P+ N MOSFET LEDs

As shown in [86], the silicon light source under a forward bias could produce an emission spectrum centered at ~1120 nm, corresponding to the silicon bandgap energy, and the same device under a reverse bias could emit a much broader visible spectrum that with red-orange color. The difference between reverse-bias breakdown spectrum and the forward-bias luminescence spectrum could be explained as follow: the reverse-bias spectrum contains the fundamental near-edge emission corresponding to indirect transitions (also observed under forward-bias) and a higher-energy emission which is not seen under forward bias.

In the case of forward bias, the total variation of the electrostatic potential across the p-n junction is reduced, bringing about a narrowing of the depletion region. The junction capacitance per unit area is given simply by

$$C_{dep} = \frac{\varepsilon_{si}}{W_d} \tag{4.8}$$

where ε_{si} is the permittivity of silicon and W_d is the depletion region width. Forward biased p-n junction is with a low-speed light modulation, since the *RC* delay time increases with the forward bias voltage of the p-n junction. As a result, the light emission process from a p-n junction in the forward-bias condition is slow to respond to modulating signals due to the indirect band structure of silicon. Moreover, it was presented that the luminescence lifetimes in the forward-biased silicon p-n junction are typically several tens

to hundreds of microseconds. Since the photon emission in the forward-biased silicon p-n junction is mainly caused by the radiative indirect recombination which is a slow process that will lead the operating speed in the MHz range [87].

Avalanche breakdown has been known to occur along the depletion region, approximated treated as "micro-plasma", and they are visible as shining points. These luminescence micro-plasma spots are connected with defects of the crystal lattice and when they are excited each "micro-plasma" site light up at its own breakdown voltage. It is noted that avalanche process is generally known as an inherently fast process. The modulation speed for the avalanche breakdown mode in the Si-diode LED is also determined by the *RC* time constant. With the dynamic on-resistance *R* of the "P^+ Source/Drain to N-Substrate" junction in the 10^{-2} Ω•cm range and the reverse-bias junction per-unit length capacitance in the range of pF/cm, the *RC* time constant will be in the range of tens of femto-second. Although the capacitance-voltage characteristics of reverse biased p-n junction decreases slowly with reverse-bias voltage V_{sub} as the depletion width W_d in Eq. (4.8) increases with reverse-bias voltage V_{sub}, a strong recombination in the avalanche region will induce negative capacitance phenomena that make the capacitance $C_{dep}L_m$ decreases rapidly when the Si-diode LED is fully turned on to avalanche breakdown with hard characteristics (i.e., the multiplication factor is equal to infinity) [88]. Therefore, it is reasonably predicted that the *RC* time will be in the range of tens of pico-second, and such a time delay is capable of producing modulation in excess of 10 GHz. The transit time of the excited carriers is given by

$$\tau_0 = \frac{W_d}{v_s} \tag{4.9}$$

where W_d is the depletion width of the "P+ Source/Drain to N-Substrate" junction and is the saturated drift velocity of the carriers. Here v_s is also known as the thermal velocity of the carriers, i.e.,

$$v_s \equiv \sqrt{3kT/m} \cong 10^7\, cm/s \tag{4. 10}$$

Hence, a carrier drifting at v_s ~10^7 cm/s through the length of the depletion region of ~2 μm will set the theoretical limit of light modulation at 20 psec, thus leading to a switching speed ~10 GHz in the Si avalanche electroluminescence devices [89].

To find the relationship between the transit time τ_0 and the reverse current I_{sub}, the characteristics of the p-n junction depletion region is analyzed in detail via the rate of electron-hole generation rate R.

$$R + \Delta R = \frac{(n_0 + \Delta n)(p_0 + \Delta p)}{n_0 p_0} R = \frac{n_0 p_0 + p_0 \Delta n + n_0 \Delta p + \Delta n \Delta p}{n_0 p_0} \tag{4. 11}$$

On the other hand, "depletion" is equivalent to saying that most of the space-charge region will be completely depleted of carriers, and the product of excess carrier concentrations, $\Delta n \Delta p$, is a very small term that is negligible. For this case, Eq. (4.11) reduces to

$$\frac{\Delta R}{R} = \frac{\Delta n}{n_0} + \frac{\Delta p}{p_0} \tag{4. 12}$$

Thus the radiative lifetime of excess carriers is

$$\tau_0 = \frac{\Delta n}{\Delta R} = \frac{1}{R} \frac{n_0 p_0}{n_0 + p_0} \tag{4. 13}$$

Within the depletion region, $n_0 = p_0 = n_i$; therefore, the effective lifetime, also called transit time, within a reverse-biased depletion region is given by [83], [90]

$$\tau_0 = \frac{n_i}{2R} \tag{4. 14}$$

and the reverse current generated in the reverse biased "P+ Source/Drain to N-Substrate" junction can also be expressed as

$$I_{sub} \sim (\tau_0)^{-1} \tag{4. 15}$$

Light modulation as high as 20 GHz was observed in a reverse-biased silicon p-n junction operating in avalanche breakdown mode, and this speed is much higher than that of forward-biased silicon p-n junctions [91].

In the advancement of Si-diode LED to Si gate-controlled diode LED, the motivation is to sidestep the natural recombination times in order to provide fast switching. In Si-diode LED, the speed is limited by how fast the excess carriers can be removed from the avalanche region of p-n junctions. In Si gate-controlled diode LED, the speed is limited by the discharge time of the metal-oxide-semiconductor (MOS) capacitor instead of the natural carrier lifetime. The high-frequency characteristics of the MOS capacitor are defined by the two components (i.e., the oxide capacitor, which is $C_{ox}L_m$ ~43.66 pF/cm, and the silicon depletion charge based substrate capacitor connected in series). The minimum MOS capacitance per-unit area is then given by

$$\frac{1}{C_{\min}} = \frac{1}{C_{ox}} + \sqrt{\frac{4kT\ln(N_d/n_i)}{\varepsilon_{si}q^2N_d}} \tag{4. 16}$$

Therefore, $C_{\min}$ is about 2.65562×10^{-8} F/cm^2, and the per-unit length capacitance $C_{\min}L_m$ is about 15.934 pF/cm.

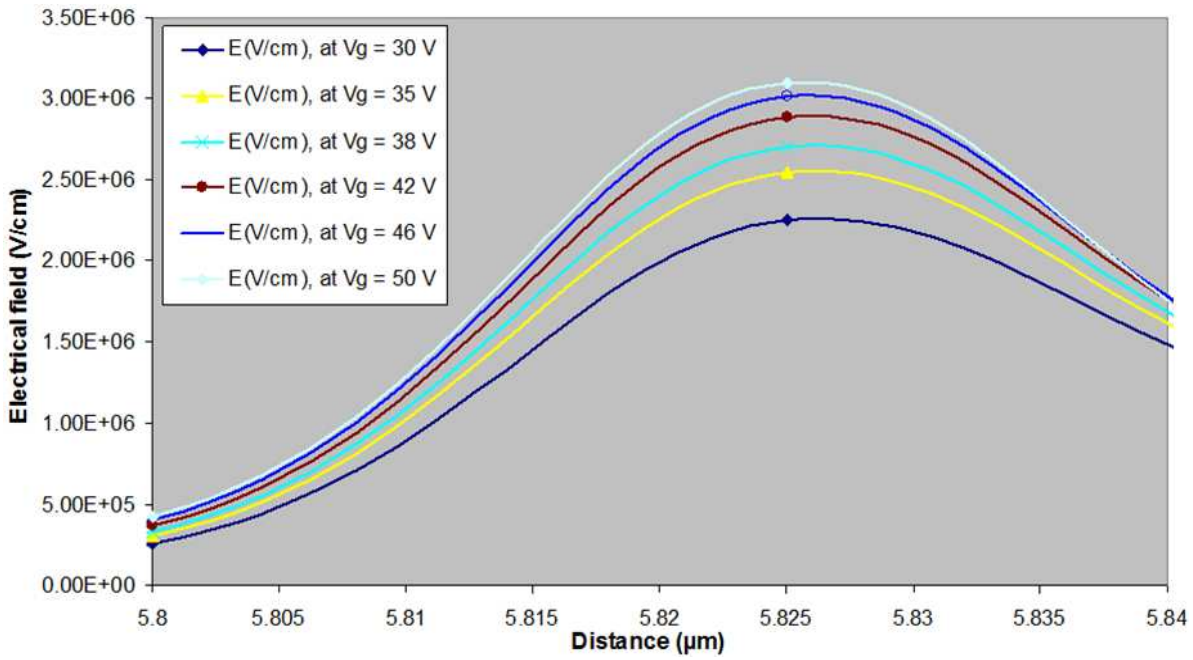


Fig. 4.6 The variation in the electric field (in V/cm) as a function of position in the Si gate-controlled diode LED. The Si-PMOSFET is operating at: V_{sub} = 30 V, $V_d = V_s$ = 0 V, and varying V_g

On the other hand, the thermal carrier lifetime is given by [92]

$$\frac{1}{\tau_{th}} = \frac{1}{L}\sqrt{\frac{kT}{2\pi m^*}}\exp\left(-\frac{\Delta E}{kT}\right) \qquad (4.17)$$

where L is the quantum-well width, T is the effective temperature of the carrier, m^* is the carrier effective mass, and ΔE strongly depends on the local electrical field. A simulation of the electric field distribution near the "P^+ Source/Drain to N-Substrate" junction corner is carried out to understand the transient nature of the Si gate-controlled diode LED using the device simulator TCAD Sentaurus by Synopsys [93]. Fig. 4.6 shows that, for the reverse bias of V_{sub} = 30 V, the electric field increases with gate voltage V_g, and the X-axis distance (i.e., the location of electric field peak) fitting Fig. 4.4(b) provides the evidence that the highest

field occurs at the "Gate to Source/Drain" overlap region. It is worth noting that the maximum electrical field is about 3×10^6 V/cm, the τ_{th} is evaluated to be 7.5 psec for a zero electric field, and less than 0.1 psec for electrical field of 3×10^6 V/cm. Taking the dynamic series resistance into account, it is found that the Si gate-controlled diode LED has an intrinsic frequency capability of a few hundred GHz in theory.

Recalling the schematic of Si gate-controlled diode LED shown in Fig. 4.3(b), it is obtained that the electrical ac input goes into the gate-source/drain port and the optical ac output is extracted at the drain-source port, so a small-signal equivalent circuit model below is applied for the analysis of expected modulation speed as a result of parasitic capacitances [94].

The intrinsic transconductance of the "P^+ Source/Drain to N-Substrate" junction is given by

$$g_m = \left(\frac{\partial I_{sub}}{\partial V_g} \right)_{V_{sub}} \tag{4. 18}$$

According to the "reverse current I_{sub} versus gate voltage V_g" at reverse bias V_{sub} = 35 V shown in [90], g_m is ~4.0625 mA/V in the electro-optic modulation range of 33.3 V < V_g < 40 V. In addition to the MOS capacitance, there are also some parasitic capacitances (e.g., the junction capacitance between the source or drain diffusion region and the substrate, the overlap capacitance between the gate and the source or drain region) that can have a significant effect on the time delay in the Si-PMOSFET device. The gate-to-source/drain overlap-region per-unit length capacitance is simply given by

$$C_{ov} l_{ov} = \frac{\varepsilon_{ox}}{t_{ox}} l_{ov} \tag{4. 19}$$

where l_{ov} is the length of the source or drain region under the gate. As shown in Fig. 4.7, l_{ov} is ~0.265 μm for the Si-PMOSFET in this study. Hence, $C_{ov}l_{ov}$ is ~1.9283 pF/cm.

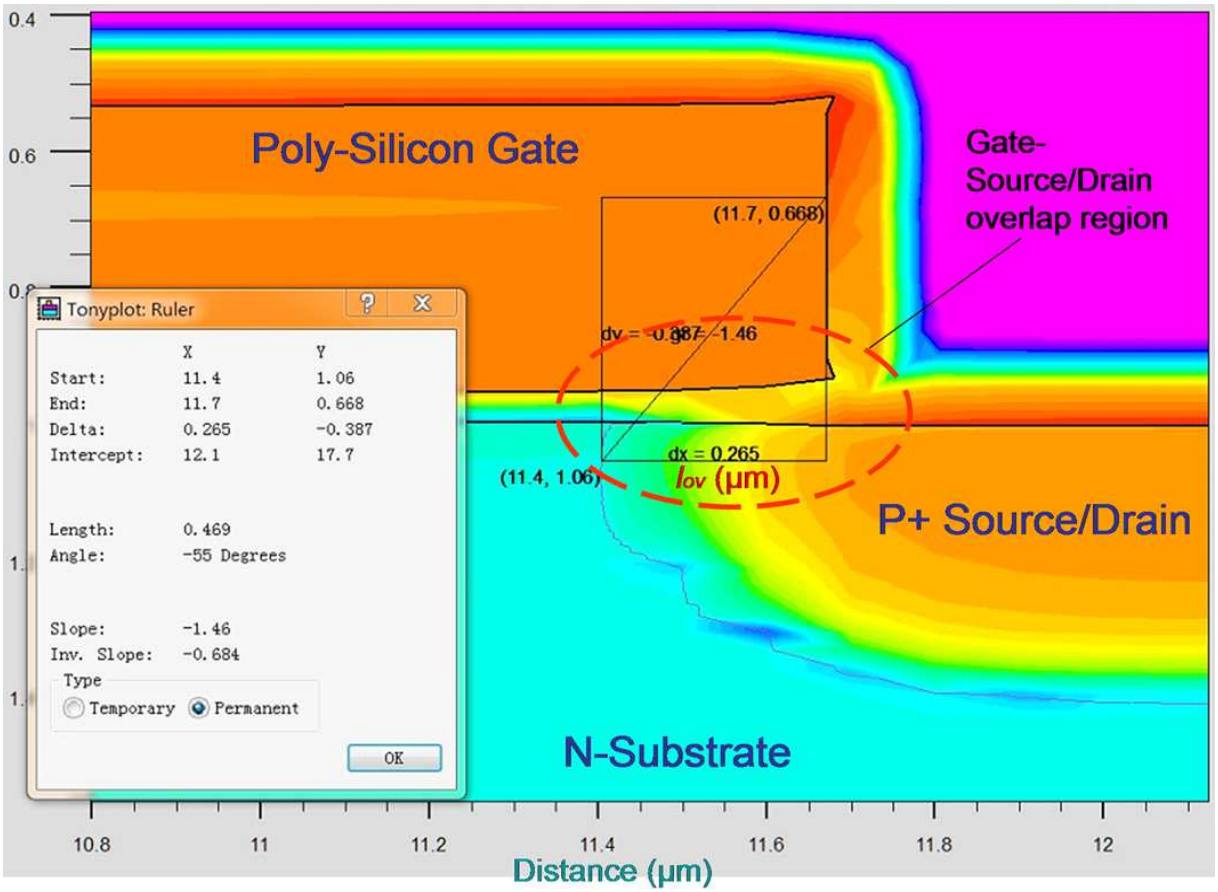


Fig. 4.7. Gate-to-Source/Drain overlap region (in the red dashed circle) where field-induced junction occurs in the Si-PMOSFET device operating as the Si gate-controlled diode LED

According to the small-signal analysis of a two-port network in the Si-PMOSFET device frequency domain, the intrinsic unity-current-gain frequency is then obtained by

$$f_T = \frac{g_m}{2\pi C_{ov} l_{ov} W_m} \tag{4. 20}$$

where W_m ~175.5 μm is the width of the Si-PMOSFET device. It is calculated that f_T ~19.10565 GHz.

In the fabrication of the Si-PMOSFET device, silicide is formed over the poly-silicon gate to lower the resistance and provide ohmic contacts to n^+ gate. For the 3-μm CMOS technology, the sheet resistivity ρ_{sheet} of silicide is ~10 Ω/square. Since the number of squares is equal to the channel length-width ratio, the parasitic gate resistance is then given by

$$R_g = \rho_{sheet}\left(\frac{L_m}{W_m}\right) \tag{4. 21}$$

, so the gate resistance is ~0.34188 Ω. The unity-power-gain frequency is then calculated by

$$f_{\max} = \sqrt{\frac{f_T}{8\pi R_g C_{mos}}} \tag{4. 22}$$

where C_{mos} denotes the MOS capacitance which has the maximum of $C_{ox}L_mW_m$ and the minimum of $C_{\min}L_mW_m$ that are given in Eq. (4. 16). Hence, for the reverse-bias of V_{sub} = 35 V, the maximum modulation frequency is in the range of ~ 53. 87 to 89.17 GHz. Since the 3-dB cut-off frequency f_{3-dB} is somewhat lower than the maximum modulation frequency $f_{\max}$, the model presented above can reasonably fit the results of a few tens of GHz that were discussed in [90], [95]. More detailed experimental results will be presented to gain more in-depth understanding of the device operation in the field of electro-optic modulation and to verify the theoretical analyses in advance in near future.

More experimental results regarding “electrical-optical characteristics” are given in Fig. 4.8 for further analyzing the effect of gate voltage on the light emission modulation.

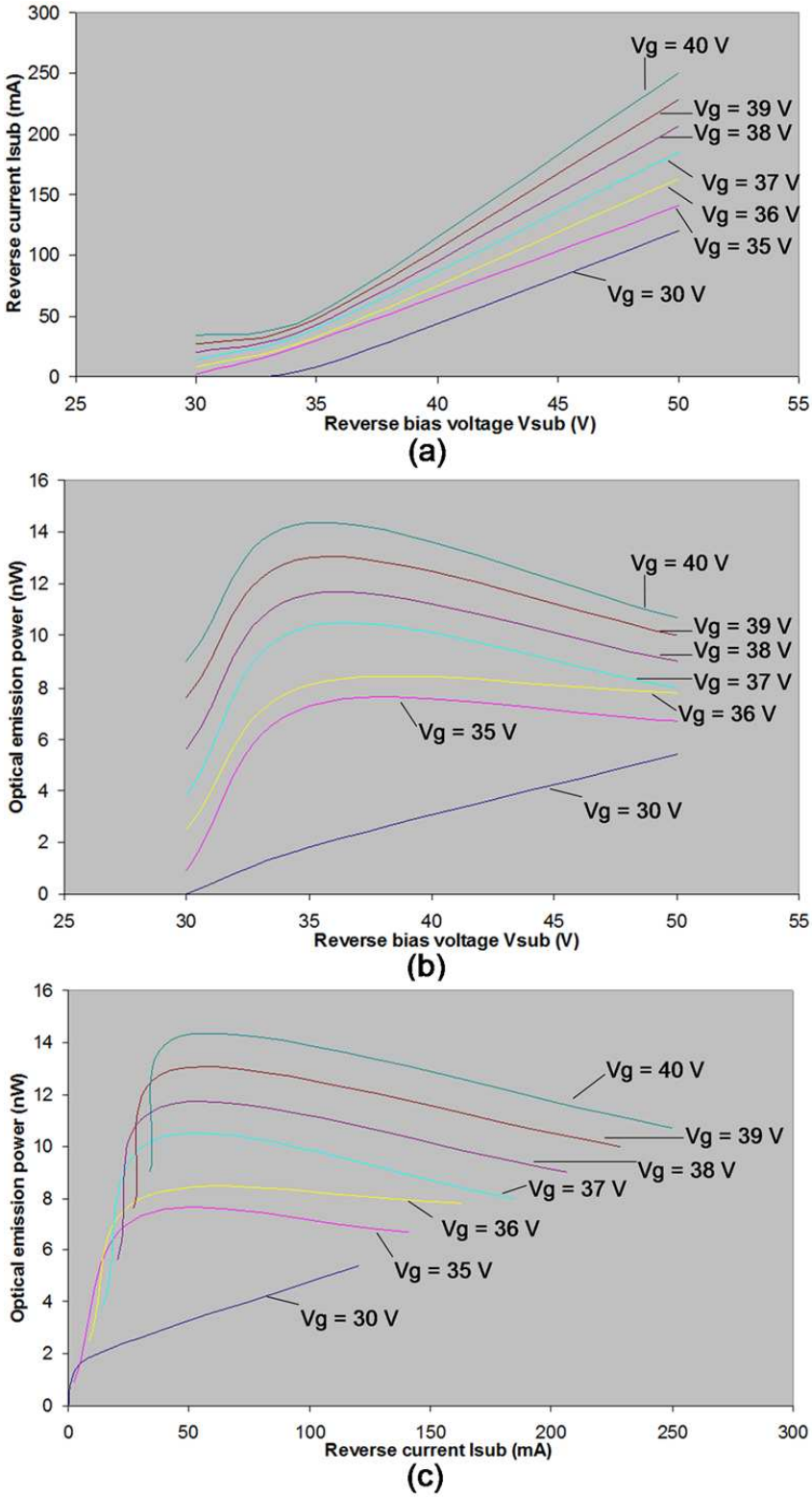


Fig. 4.8 The current-voltage-intensity characteristics for the Si-PMOSFET device operating at a fixed gate voltage

Because the gate voltage V_g is fixed in the experiment, a higher reverse-bias of the "P^+ Source/Drain to N-Substrate" junction, V_{sub}, means a larger lateral electric field in the junction depletion region and this leads to more carriers being generated, so reverse current I_{sub} is proportional to the reverse bias V_{sub} for a given gate voltage V_g as shown in Fig. 4.8(a). Fig. 4.8(b) and (c) demonstrate that the slope of the curves of "reverse bias versus optical emission power" and "reverse current versus optical emission power" decrease as the reverse bias V_{sub} increases. The reduction in the curve slope is explained as the ratio of the high energy photons to the total emitted photons increases with the depletion region electric field.

The random and highly nonlinear character of avalanche ionization is reflected also in the optical emission power dependence of electroluminescence. It implies that, for the nonlinear revere current dependence of electroluminescence intensity occurring in the Si-PMOSFET device (whose thin layer is surrounded by oxide barriers, metal electrodes, a covering layer, etc.), it is always necessary to think of the occurrence of pre-avalanche breakdown (i.e., a transition from tunneling to avalanche) in the reverse-biased "P^+ Source/Drain to N-Substrate" junction depletion layers.

CHAPTER 5: Conclusion and Outlook

In this dissertation, the following major topics are presented and discussed:

a) A Si- P-channel Metal Oxide Semiconductor Field Effect Transistor (PMOSFET)-like LED has been developed for light emission modulation. In contrast to a two-terminal Si-diode LED modulated by current signal, a major advantage of this three-terminal Si-PMOSFET LED is that the optical intensity modulation can be controlled by gate voltage signal, a standard CMOSFET operation to ease both logic circuit implementation and light modulation. The gate applied voltage induces carrier concentration modulation at both channel and source/drain region under the gate, thus modulating electric field distribution and its light emission. Fabricated in a standard CMOS process technology, this Si-PMOSFET LED ensures its potential on realizing silicon optoelectronic integration [25].

b) Silicon diode at avalanche breakdown has visible light emission in the depletion region. It is believed that this optical radiation comes from the kinetic energy loss of carriers generated by impact ionization colliding with immobile charge centers in the avalanche region. A theoretical model is presented to show the correlation of the hot carrier effect with the related photonic emission in high field. Meanwhile, a PMOSFET-like silicon light source device fabricated completely in the standard silicon CMOS process technology is measured to demonstrate that avalanching current is linearly proportional to optical emission power whether this light source acts as a two-terminal device (i.e., diode, the "p^+ Source/Drain to n-Substrate junction" with floating the gate) or acts as a three-terminal device (i.e., gate-diode, the "p^+ Source/Drain to n-Substrate junction" in the course of varying the gate

voltage). Such linearity implies that control of the increasing current is a significant way to enhance the quantum efficiency of this light source device no matter what the physical structure (i.e., two terminals or three terminals) of this device is. For the first time, it has been discovered that, at the same avalanching current, the optical output power in gate-diode structure is higher than the optical output power in diode structure. In other words, for this PMOSFET-like device, the three-terminal operating mode is more efficient than the two-terminal operating mode [66].

c) The breakdown phenomenon in silicon p^+ n junctions is also of importance because of their light emission capabilities in the visible part of the spectrum in the range of 500 to 850 nm and their potential for application in next-generation silicon optoelectronic devices. To interpret the electroluminescence spectra obtained under avalanche breakdown conditions, several mechanisms are proposed for different spectral domains. The charged carriers in high field regions are ionized by impact ionization scattering in the presence of acoustical and optical phonon scattering. The newly generated carriers will maintain the discharge, and the number of carriers being just sufficient to replenish those swept out from the junction by the field. The multiplication of the carriers produced by impact ionization is small for low reverse-bias, but it increases rapidly with increasing reverse-bias and eventually approaches a large value at the critical breakdown field. In this process, the accelerated carriers with high energies return to a lower energy state and again start acceleration and obtain energy from the high field. The generated electron-hole pairs drift in high field and cause further ionization as well. Apart from this type of phenomenon, the scattering due to lattice vibration also

takes place by means of photon emission. In order to further understand the mechanism responsible for the generation of visible radiation, a multi-mechanism model for photon generation by silicon junction in avalanche breakdown is recommended [33].

d) At the end of the dissertation, the electrical-optical characteristics and the theoretical calculation and simulation modeling for the topic of modulation speed are discussed. The forward-biased silicon p-n junction could emit light through the recombination of minority carriers, but that process is very slow, inefficient and unreliable. The limiting speed of light modulation in reverse-biased silicon p-n junction is analyzed by using a Si-PMOSFET device operating in the modes of Si-diode LED and Si gate-controlled diode LED. In Si-diode LED, light emission is due to the avalanche breakdown of the "P^+ Source/Drain to N-Substrate" junction and the modulation speed of a few tens of GHz is induced by the intraband transitions of hot carriers and the transit time for sweeping the minority carriers out of the depletion region. In Si gate-controlled diode LED, the "P^+ Source/Drain to N-Substrate" junction breakdown process is triggered by the gate voltage V_g, leading to a localized fall in the breakdown field and enhancement of fields near the "P^+ Source/Drain to N-Substrate" junction corner underneath the gate, and the field of the order of 10^6 V/cm is higher than the critical field for avalanche breakdown. Because of the enhancement in electric field, the light modulation speed in Si gate-controlled diode LED will be even much higher [90], [96], [97].

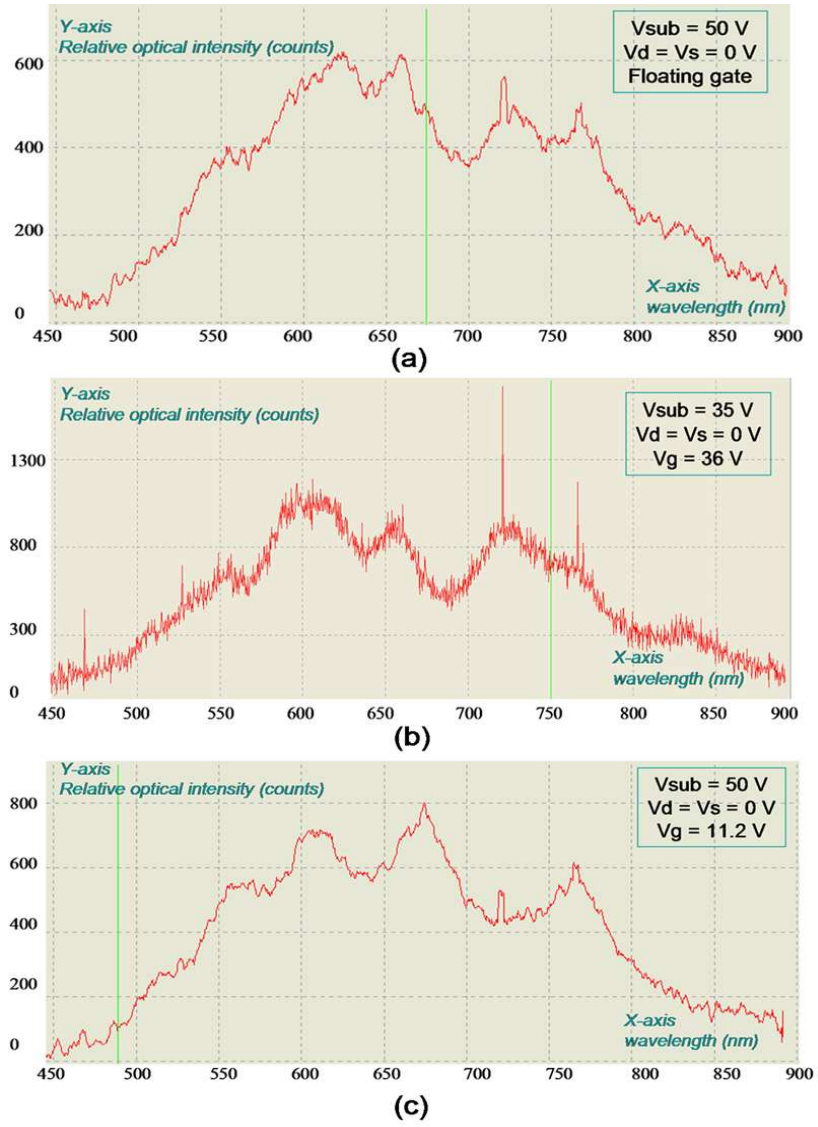


Fig. 5.1. Photon emission spectra obtained at different bias conditions. Emitting wavelength range is 450 nm to 900 nm

In conclusion, this work demonstrates the effect of gate voltage on the light intensity modulation through changing the BV. As a multi-functional silicon LED in which different spectra (e.g., Fig. 5.1) can be realized simultaneously and as a Si-LED that can be fabricated by the conventional VLSI silicon technology, the light source (i.e., Si-PMOSFET LED) put forward in this study can be potentially used as an electro-optic modulator for short-

distance electro-optic interconnect in the silicon PEICs. It is noted that a weak light emission at reverse breakdown due its poor light output efficiency does not qualify the device as a light source, in comparison to the III-V compound light emitting sources, for most of the optical systems. But the device seems to have potential for VLSI optical interconnect because the light source can be fabricated along with the rest of components in the silicon integrated circuit on the same substrate. Since the proposed P-MOSFET device is fabricated using a relatively old 3-μm CMOS technology, the junctions with more lightly doped layers require the application of high voltages. If the injection depth and concentration are optimized by a more advanced CMOS technology, the whole device is in a heavy doping area to decrease the voltage. On the other hand, both the external quantum efficiency and the internal quantum efficiency could be improved by means of further innovative design and processing procedures without deviating too far from the existing technological routes.

Future work includes the following three topics: *a)* p-n junction diodes operated in the avalanche mode can be made with standard silicon processing and are known to be reliable, so the light output from an avalanching silicon diode is very linear with current and has essentially independent of the temperature; Although the quantum efficiency of the avalanche silicon LED is as low as 10^{-8}, it is enough to make practical opto-couplers in applications [98]; *b)* Both the quantum efficiency and the power conversion efficiency are observed to have obvious enhancement although the reverse-bias of the p-n junction is reduced and the corresponding reverse-current is much lower, in future a practical approach is suggested to explain why there is an quantum efficiency enhancement at here [69]; *c)* Since the electrical-optical characteristics of the silicon device and the theoretical

calculation and the simulation modeling regarding the silicon device modulation speed are described, more detailed experimental results will be presented to gain more in-depth understanding of the device operation in the field of electro-optic modulation and to verify the theoretical analyses in future.

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