### Title

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# An Investigation of Electrical and Dielectric Parameters of Sol–Gel Process Enabled $\beta$-$Ga_2O_3$ as a Gate Dielectric Material

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***Abstract*— In this paper, $\beta$-$Ga_2O_3$ thin films were grown on a p-Si substrate using the sol–gel method. Structural characterization of the films was performed using X-ray diffraction. Electrical parameters such as breakdown field, interface traps density ($D_{it}$), and series resistance ($R_S$) were investigated at room temperature. The interface trap density was found to be $10^{12}$ $eV^{-1}cm^{-2}$ using the Hill–Coleman method. This result is valuable for MOS capacitor applications. Dielectric parameters were investigated in the wide frequency range (20 kHz–1 MHz) at room temperature. We observed that these parameters have a strong dependence on frequency and voltage.**

***Index Terms*— $\beta$-$Ga_2O_3$ dielectric film, dielectric properties, electrical properties.**

## I. Introduction

IN RECENT years, there has been a strong demand for high-$k$ gate dielectrics able to provide an increased gate capacitance at small thickness. Gate oxides are no longer restricted to the silicon dioxide commonly used in the past. Materials such as aluminum oxide ($Al_2O_3$) [1], zirconium oxide ($ZrO_2$) [2], hafnium oxide ($HfO_2$) [3], aluminum nitride (AlN) [4], and gadolinium oxide ($Gd_2O_3$) [5] have all been used as gate dielectrics for semiconductor devices. The gate dielectric is an important part of a MOS capacitor because of its effect on the gate capacitance. In order to achieve a high gate capacitance, a material with a high dielectric constant should be used. For this reason, $Ga_2O_3$ thin films with a dielectric constant of between 9.93 and 10.2 [6] are a promising dielectric material. This is far greater than silicon dioxide, which has a dielectric constant of only 3.9 [7]. Due to its higher dielectric constant, $Ga_2O_3$ thin films are more resistant to tunneling of carriers through the gate of the capacitor. $Ga_2O_3$ also has a wide bandgap (~4.9 eV) and high chemical and thermal stability.

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Shih *et al.* [8] used $Ga_2O_3$ films as both a gate dielectric for an AlGaN/GaN MOS high-electron-mobility transistors (HEMT) and as a passivation layer for a gate-stack and found that the leakage current was reduced by two orders of magnitude. Jevasuwan *et al.* [9] grew a monolayer of $Ga_2O_3$ on InGaAs and inserted it into an $Al_2O_3$/InGaAs stack, observing that it reduced trap density and reduced the formation of native oxide. Allen *et al.* [10] showed that $Ga_2O_3$ thin films can be used to passivate Si solar cells by reducing trap density and contributing to a high negative charge density. Seok *et al.* [11] sputtered $Ga_2O_3$ onto AlGaN/GaN HEMTs and discovered that it reduced the leakage current and increased the breakdown voltage. Lin *et al.* [12] used a layer of $Ga_2O_3$ in an InGaN light-emitting diode for passivation and to reduce leakage current. A theoretical study also showed that layers of $Ga_2O_3$ can be grown on $\alpha$-$Fe_2O_3$ to passivate surface states that would otherwise trap holes [13]. These examples show that a $Ga_2O_3$ film is an excellent dielectric material.

In this paper, the sol–gel method was used to as simple and in expensive method. However, the quality of thin film obtained is not as high as that obtained using other deposition methods. Kumar *et al.* [14] used the sol–gel method to grow titanium dioxide films of different thicknesses in fabricating MOS capacitors. Amiri *et al.* [15] prepared a gel electrolyte for a supercapacitor consisting of KCl and potassium poly (acrylate) (PAAK) polymer and used spin coating to create a uniform surface of the gel electrolyte. These examples show that the sol–gel method is a valid way of growing thin films for dielectrics in capacitors. Therefore, we fabricated an MOS capacitor using the sol–gel method to grow $Ga_2O_3$ as the gate dielectric and measured its dielectric properties using impedance spectroscopy.

To better understand the effectiveness of sol–gel enabled $Ga_2O_3$ as a dielectric, it is important to know the electric and dielectric properties of the grown material. For this purpose, the Hill–Coleman method [16] and impedance spectroscopy was performed on the $Ga_2O_3$ heterostructure. Impedance spectroscopy is a useful method for revealing internal dynamics of a system across the frequency spectrum. Alifragis *et al.* [17] used impedance spectroscopy to determine the structure of a GaN gas sensor. Lazarescu *et al.* [18] found that pH and applied potential had a significant impact on

the GaAs-cysteine thiolate interface using impedance spectroscopy. Impedance spectroscopy was used to find dielectric parameters of $\beta$-$Ga_2O_3$ thin film as function of frequency and voltage.

## II. Experiments

MOS capacitors were fabricated on (100) p-type Si wafers doped with boron. The wafers were 280-$\mu$m thick and had a resistivity between 0.005 and 0.08 $\Omega$ cm. The Si wafer was cleaned using acetone for 5 min and then in methanol for 5 min in an ultrasonic bath. Following that, the wafer was rinsed with deionized water for 5 min. To grow the $Ga_2O_3$ thin film, first gallium nitrate hydrate ($Ga(NO_3)_3 \cdot xH_2O$) powder was dissolved in ethanol ($C_2H_6O$) to form a solution. Then, this solution was drop-cast onto a bare p-Si substrate and spun for 30 s at 3000 rpm in the ambient atmosphere.

Afterward, the film was heated at 100 °C on a hot plate for 30 min to evaporate the ethanol and then annealed in a furnace at 800 °C for 2 h in Ar ambient. In the literature, different annealing temperatures for $Ga_2O_3$ have been used to improve film crystallinity. Cheng *et al.* [19] annealed $Ga_2O_3$ films in $N_2$ and $O_2$ at 1000 °C for 1 h. This caused grain size to increase significantly and photoluminescence intensity to greatly increase. The absorption edges of the films also shifted to shorter wavelengths. Suzuki *et al.* [20] annealed $Ga_2O_3$ photodiodes in $N_2$ at temperatures ranging from 100 °C to 500 °C for 10 min. This led to a reduction of the forward turn-on voltage and at 400 °C, the photocurrent and responsivity were dramatically enhanced. Goyal *et al.* [21] annealed $Ga_2O_3$ thin films at 600 °C, 800 °C, and 1000 °C in air for 24 h. At higher temperatures, the surface feature size of the $Ga_2O_3$ film increased. Higher annealing temperatures were also correlated with a wider bandgap. Berbenni *et al.* [22] explain the process through which $Ga(NO_3)_3 \cdot xH_2O$ thermally decomposes into $Ga_2O_3$.

X-ray diffractometer characterization of films after the 800 °C anneal step was performed with a Bruker D8 Discover high-resolution X-ray diffraction system equipped with a Cu K-alpha X-ray source. Measurements were performed in a grazing incidence angle to minimize diffracted intensity from the Si substrate geometry maximizing the intensity from the $Ga_2O_3$ film. After structural characterization of the films, electron beam evaporation was used to deposit 20 nm of Ni and 200 nm of Au for contacts through a shadow mask. A Keithley 4200-SCS parameter analyzer was used to measure $C$–$V$ characteristics using a sweep rate of 100 mV/s, ac amplitude of 30 mV, and a voltage step of 0.1 V at various frequencies. A HP4156B semiconductor parameter analyzer was used to measure the $I$–$V$ characteristics between 5 and −45 V with a voltage step of 0.5 V. A schematic of the device and a cross-sectional SEM image of the $Ga_2O_3$/Si interface are presented in Fig. 1.

## III. Results and Discussion

### A. Structural Properties

Grazing incidence X-ray diffraction measurements on a ~50-nm $Ga_2O_3$ film at an incidence angle of 0.6° are presented in Fig. 2 over the diffracted angle range of $2\theta$ = 15-100°. The experimental peak positions and intensities correspond well to a nearly randomly oriented monoclinic $\beta$-$Ga_2O_3$ phase (JCPDS card 00-041-1103) with peak reflections as indicated. No significant peaks indicative of rhombohedral $\alpha$-$Ga_2O_3$ (JCPDS card 01-074-1610) or other phases are present in the experimental pattern.

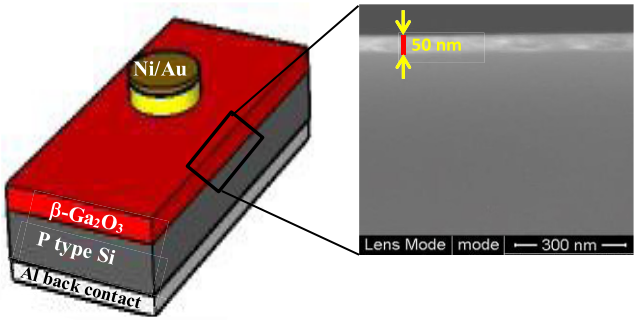


Fig. 1. Schematic of the device and cross-sectional SEM image of $\beta$-$Ga_2O_3$/Si interface shows the smooth thin film with 50-nm thickness.

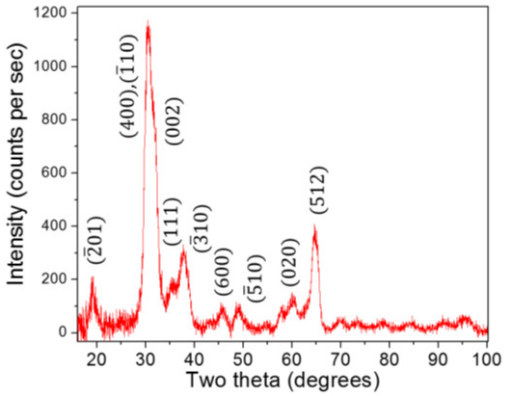


Fig. 2. X-ray diffraction pattern of $Ga_2O_3$ film annealed at 800 °C in Ar ambient, with peak labels corresponding to strong monoclinic $Ga_2O_3$ reflections.

### B. Electrical Properties

It is well-known that $Ga_2O_3$ has a high breakdown field and that therefore it is suitable for high-temperature applications. $I$–$V$ plots were measured between 5 and −45 V with a voltage step of 0.5 V (Fig. 3). The breakdown field was determined for a 50 nm $Ga_2O_3$ thin film which was grown via the sol–gel method and annealed at 800 °C in Ar ambient. As can be seen from Fig. 3, the breakdown field was calculated to be 7 MV/cm. In the literature, for thermally oxidized $Ga_2O_3$ thin films, breakdown fields of 0.65 [23], 1 [24], 3.85 [25], 3.6 [26], and 18 MV/cm [27] have been reported. As seen in Fig. 3, the high leakage current can be attributed to native oxide in between the $Ga_2O_3$ and Si interface. The presence of this native oxide reduces the performance of the MOS capacitor by increasing leakage current and the roughness of the surface. The presence of a native oxide also leads to the generation of traps due to stress between the oxide and the silicon substrate [28].

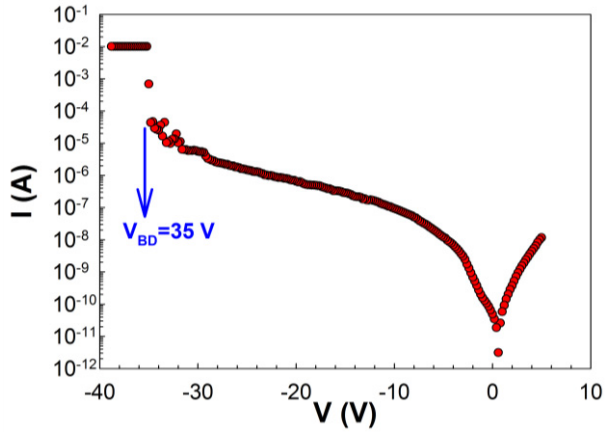


Fig. 3. Reverse bias semilogarithmic *I–V* curve of the Ni/Au/$\beta$-$Ga_2O_3$/p-Si MOS capacitor at room temperature. The breakdown field was determined to be 7 MV/cm.

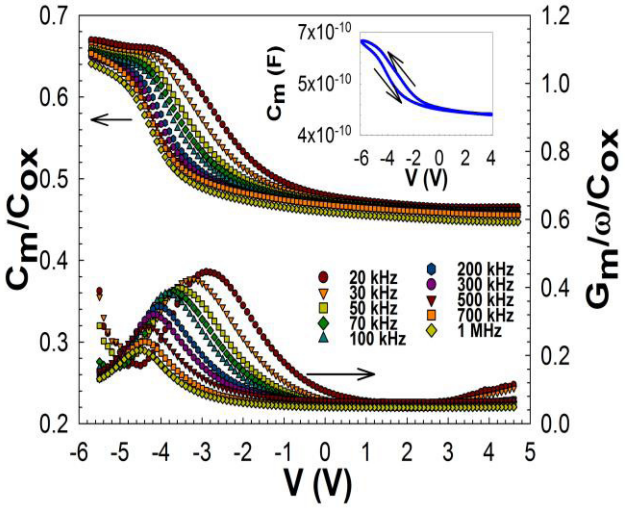


Fig. 4. Measured capacitance ($C_m$) and conductance ($G_m/\omega$) of MOS capacitor ($C_mG_m$-$V$) were normalized by the oxide capacitance ($C_{ox}$) as a function of bias voltage. $C_mG_m$-$V$ was measured with a voltage step of 0.1 V and swept between frequencies 20 kHz–1 MHz. The oxide thickness of the Ni/Au/$\beta$-$Ga_2O_3$/P-Si MOS capacitor is 50 nm. Inset: the hysteresis of $C_m$ versus $V$ with sweeps in two different directions.

The measured capacitance ($C_m$) and conductance ($G_m$/W) values were normalized by the oxide capacitance ($C_{ox}$) and are given in Fig. 4. The three regimes of accumulation, depletion, and inversion are shown in the $C_m/C_{ox}$-$V$ plot (Fig. 4) and a typical MOS capacitor behavior can be seen. However, the $C_m/C_{ox}$-$V$ behavior of the Ni/Au/$\beta$-$Ga_2O_3$/p-Si MOS capacitor is nonideal. The nonideal MOS capacitor capacitance curve can experience a parallel shift from the ideal curve due to the flat band voltage, fixed charge, oxide trapped charge, interface trapped charge, and mobile oxide charge effects [29], [30].

The $C_m$-$V$ curves of the inset of Fig. 4 show that there is an interface layer between the metal and semiconductor. Hysteresis of $C_m$-$V$ with two sweep directions, one from the negative voltage to positive voltage and the other positive to negative, can be observed. This behavior can be attributed to mobile charges in an interfacial layer [27], [29]–[31]. Also,

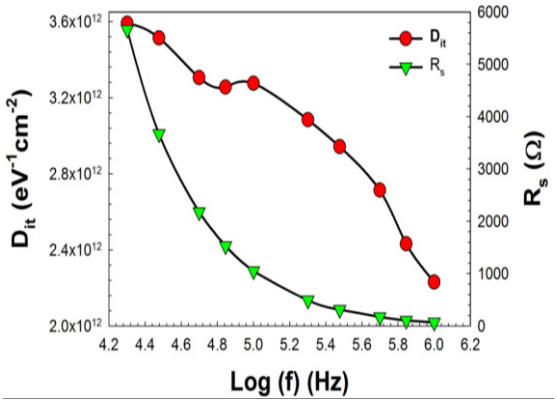


Fig. 5. Variation of interface traps density ($D_{it}$) and series resistance of the MOS capacitor were obtained from $C_mG_m$-$V$ characteristics in the frequency range of 20 kHz–1 MHz. $D_{it}$ of the MOS capacitor decreases with increasing frequency. This result is reflected by the $G_m/\omega/C_{ox}$ peak and frequency dispersion at depletion. $R_s$ decreases with increasing frequency due to interface trapped charges, voltage-dependent fixed charges, and mobile charges effect.

there is a hysteresis width due to electron and hole trapping in the interfacial layer [31].

The $C_m/C_{ox}$-$V$ values have large frequency dispersion at the depletion region because of interface traps. The trapped charges at trap sites can easily follow the external ac signal because it is well known that the lifetime of interface trapped charges is lower than $1/(\omega = 2\pi f)$. Thus, interface trapped charges can affect the device's capacitance measurement. However, the trapped charges at trap sites cannot follow the external ac signal because the lifetime of interfacial trapped charges is much longer than $1/(\omega = 2\pi f)$ of the ac signal at high frequencies ($\geq$500 kHz) [29]–[33]. Therefore, interface trapped charges do not affect the device's capacitance measurement. The $G_m/\omega/C_{ox}$-$V$ values have peaks for each frequency in the depletion region due to the exchange of low quantities of majority carriers in between the localized interface states and relevant band [29]–[33]. The magnitude of the peaks increased with decreasing frequency and shifted toward a lower voltage because of interface traps. This peak height can be directly attributed to $D_{it}$.

There are several methods to obtain the interface trap density $D_{it}$. The low-high frequency method is the most widely used method, but it is useful only if the density of interface traps is higher than $10^{10}$ $eV^{-1}cm^{-2}$ [29], [30], [32], [33]. Another method to obtain interface traps is the conductance method. It is considered the most sensitive method [29], [30], [32], [33]. In addition, interface traps can be identified by using the Hill–Coleman method [16]

$$D_{it} = \frac{2}{qA}\frac{G_{mmax}/\omega}{\left[\left(\frac{G_{mmax}}{\omega}/C_{ox}\right)^2 + (1 - C_m/C_{ox})^2\right]} \quad (1)$$

where $A$, $\omega$, $G_{mmax}$, $C_m$, and $C_{ox}$ are the area of the device, angular frequency, maximum measured conductance value, capacitance value, and oxide capacitance of the device (or capacitance in the strong accumulation region), respectively. As can be seen in Fig. 5, the $D_{it}$ of the MOS capacitor

decreases with increasing frequency. This result is reflected by the $G_m/\omega/C_{ox}$ peak and frequency dispersion at depletion in Fig. 4.

Another important electrical parameter, the series resistance ($R_s$) value, also has a large effect on the $C_mG_m$-$V$ measurements and must be considered in the calculations. $R_S$ has the potential to seriously affect admittance measurements. In order to prevent this as well as limitations on sensitivity, $R_s$ should be minimized during fabrication of the sample. Alternatively, when measuring series resistance a correction factor should be applied to the measured $C$ and $G/\omega$ before the information is extracted [29], [30].

The series resistance of the diode was calculated by using following equation:

$$R_s = \frac{G_m(V)}{G_m^2(V) + (\omega C_m(V))^2}(2) \tag{2}$$

where $C_m$ and $G_m$ are the measured capacitance and conductance values and $\omega$ is the angular frequency ($=2\pi f$) [33], [34]. Thus, the corrected capacitance ($C_c$) and corrected equivalent parallel conductance ($G_c$) equivalent frequency of interest are

$$C_c = \frac{\left[G_m^2 + (\omega C_m)^2\right]C_m}{\alpha^2 + (\omega C_m)^2} \tag{2a}$$

and

$$G_c = \frac{\left[G_m^2 + (\omega C_m)^2\right]\alpha}{\alpha^2 + (\omega C_m)^2} \tag{2b}$$

respectively, where $\alpha = G_m - [(G_m)^2 + (\omega C_m)^2]R_s$ and $C_m$ and $G_m$ are the capacitance and the equivalent parallel conductance measured across the terminals of the MOS capacitor.

The causes of $R_s$ are varied but include contact made by a probe to the gate or back contact of the semiconductor, the existence of impurities or dislocations in the material, high resistance in the quasi-neutral region in the bulk of the semiconductor and a nonuniform dopant concentration [29], [30], [35], [36]. As shown in Fig. 5, $R_s$ decreases with increasing frequency. The frequency dependence of series resistance is the result of interface trapped charges, voltage-dependent fixed charges, and mobile charges [29], [30], [34], [36].

The $C_m$ and $G_m/\omega$ were corrected in order to eliminate the effect of $R_s$. The corrected capacitance ($C_c$) and conductance ($G_c/\omega$) are a function of the voltage at 1 MHz for the MOS capacitor [30]. Since the corrections were done on the capacitance and conductance values for the effect of $R_s$, while the values of $C_c$ are higher than $C_m$, especially in the deplation and accumulation region, the corrected $G_c/\omega$ values are lower than the $G_m/\omega$ values.

As shown in Fig. 6(a) and (b), $R_s$ is more effective in the depletion and accumulation region. However, it is easy to see that there is no significant error in the inversion region due to $C_c$ being small (e.g., $(\omega R_s C_c)^2 \ll 1$).

### C. Dielectric Properties

Dielectric parameters of the Ni/Au/$\beta$-$Ga_2O_3$/p-Si MOS capacitor, $\varepsilon'$ and $\varepsilon''$ are described by the following equations

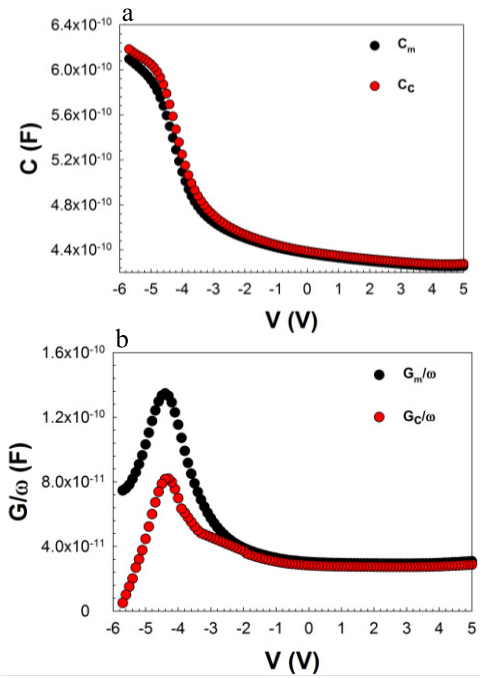


Fig. 6. Measured and corrected values of (a) $C_m$ and $C_c$-$V$ and (b) $G_m$ and $G_c/\omega$-$V$ of Ni/Au/$\beta$-$Ga_2O_3$/p-Si MOS capacitor at 1 MHz. $R_S$ is more effective in the depletion and accumulation region, although there is no significant error in the inversion region due to $C_c$ being small [e.g., $(\omega R_S C_c)^2 \ll 1$].

[1]–[4]:

$$\varepsilon' = \frac{C_m}{C_o} \tag{3}$$

$$\varepsilon'' = \frac{G_m/\omega}{C_o}. \tag{4}$$

Here, $C_o$ is the capacitance of free space ($C_o = \varepsilon_o A/d_i$). $A$, $\varepsilon_o$, and $d_i$ are the rectifier contact area, the permittivity of free space charge, and interfacial $Ga_2O_3$ thin film thickness, respectively. The loss tangent can be defined using the following equation [5], [6]:

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'}. \tag{5}$$

As seen in Fig. 7 (a)–(c), the $\varepsilon'$, $\varepsilon''$, and tan$\delta$ are depend on frequency and voltage in the depletion region. The $\varepsilon'$ values have a frequency distribution in the depletion region. On the other hand, the $\varepsilon''$ and tan$\delta$ have peaks for each frequency and the peak position shifts toward lower voltages with decreasing frequency. Conversely, the magnitude of the peaks decreases with increasing frequency due to interface traps [29], [33]. There are several parameters which affect $\varepsilon'$ $\varepsilon''$ and tan$\delta$, such as $D_{it}$, $R_s$, the thickness of the oxide layer and interfacial polarization [29], [33], [34], [37]. It is well known that interface traps can easily follow the ac signal at low frequencies, but at high frequencies, they cannot follow the ac signal due to the interface trap charge lifetime. Thus, dipolar and interfacial polarization types can contribute to $\varepsilon'$ and $\varepsilon''$ values at low frequencies. This dispersion can also be attributed to Maxwell–Wagner type interfacial polarization [38], [39]. As seen in Fig. 7(a), the value of $\varepsilon'$ decreased with increasing frequency for each voltage at the depletion

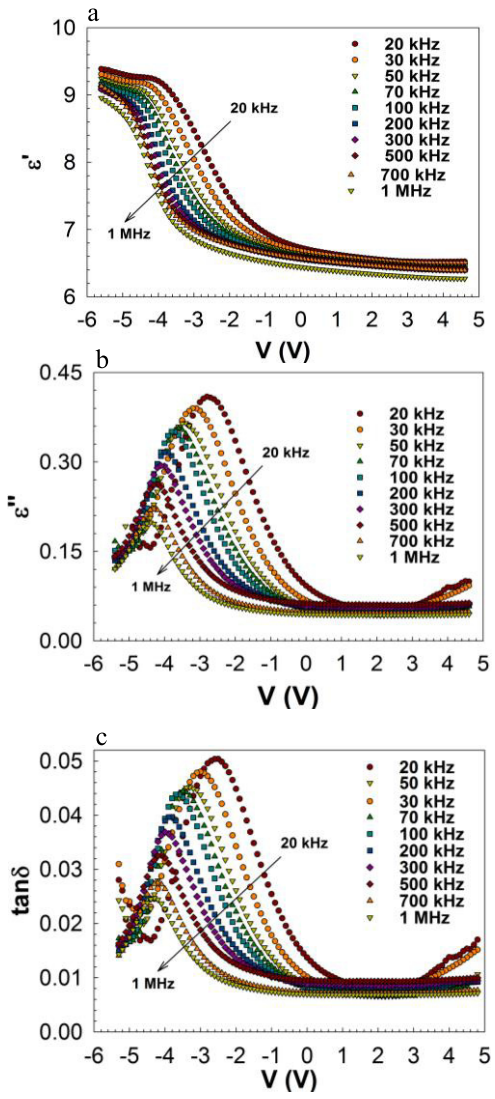


Fig. 7. Voltage and frequency dependence (a) dielectric constant ($\varepsilon'$) values have a frequency distribution in the depletion region due to interface traps. (b) Dielectric loss ($\varepsilon''$) and (c) loss tangent ($\tan\delta$) of Ni/Au/$\beta$-$Ga_2O_3$/p-Si MOS capacitor have peaks and the magnitude of the peaks decreases with increasing frequency due to interface traps.

region. The interfacial and dipolar polarizations do not have enough time to orient themselves in the direction of the electric field. Therefore, dipolar and interfacial polarization become ineffective in the depletion region as the frequency increases [40]–[42].

Dielectric properties provide a great deal of information about thin films. However, it is difficult to see the dielectric relaxation peak in transition metal oxides due to the conduction current dominating the dielectric loss current. On the other hand, even without a clear dielectric relaxation peak, it is still possible to acquire information about the relaxation mechanism by looking at the dielectric modulus representation, which is the reciprocal of the dielectric permittivity [43]–[45]. $M'$ and $M''$ are defined as follows:

$$M^* = M' + iM'' = \frac{\varepsilon'}{(\varepsilon')^2 + (\varepsilon'')^2} + i\frac{\varepsilon''}{(\varepsilon')^2 + (\varepsilon'')^2}. \quad (6)$$

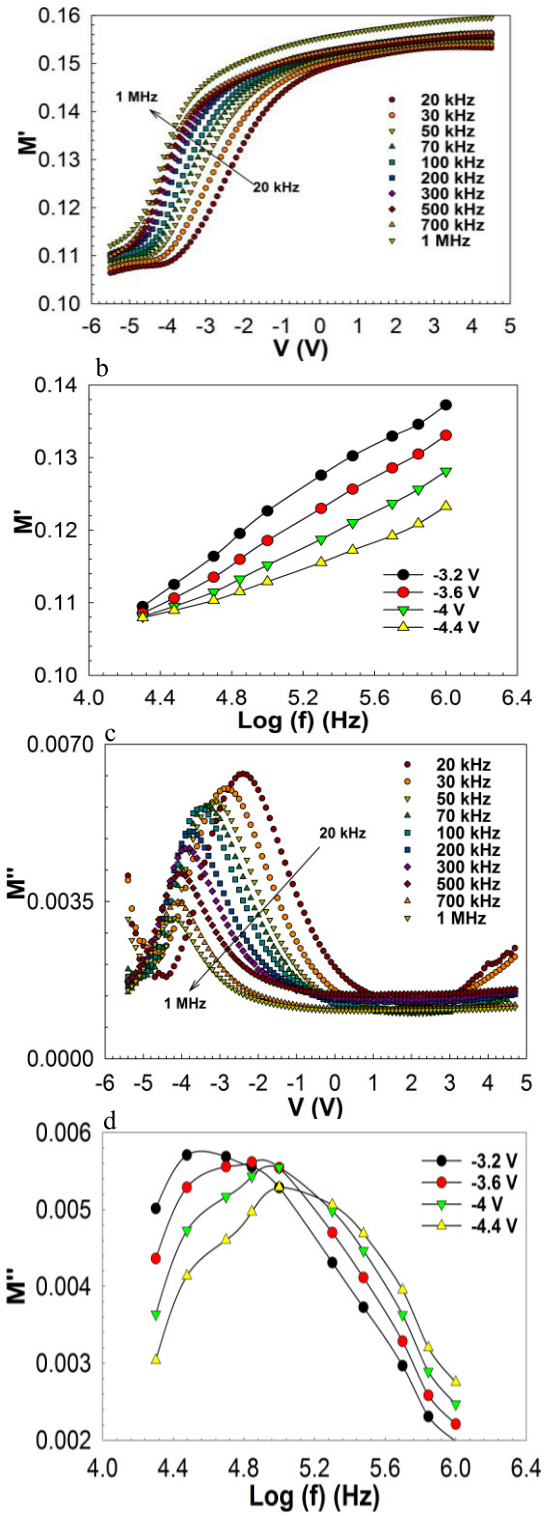


Fig. 8. Voltage and frequency dependence (a) real electrical modulus ($M'$) values have dispersion in the depletion region and (b) $M'$ values decreased with increasing frequency for each voltage due to relaxation process. (c) Imaginary electrical modulus ($M''$) values have a peak for each frequency in the depletion region and (d) also $M''$ versus log (f) also has a peak for each voltage.

As can be seen in Fig. 8(a), the $M'$ values have dispersion in the depletion region and increase with increasing frequency for each voltage due to the relaxation process [Fig. 8(b)]. At lower frequencies, the value of $M'$ is close to zero, which shows that electronic polarization does not occur. The $M''$ values have a

peak for each frequency in the depletion region [Fig. 8(c)]. And as seen in Fig. 8(d), $M''$ versus log $(f)$ has a peak for each voltage. The angular frequency $(\omega = 2\pi f)$ at which the peak for $M''$ occurs can be determined using the equation $\omega\tau = 1$, where $\tau$ is the relaxation time for a given angular frequency. Related results can be seen in the literature [43], [45]–[47].

## IV. Conclusion

In this paper, we have grown $\beta$-$Ga_2O_3$ thin film on p-type Si using the sol–gel method. The films were characterized using X-ray diffraction, and a detailed study of the electrical and dielectric properties were also performed. The experimental peak positions and intensities correspond well to a nearly randomly oriented monoclinic phase ($\beta$-$Ga_2O_3$). The electrical parameters of the diode such as breakdown field, interface trap density, and series resistance were obtained. The interface trap density was found to be $10^{12}$ $eV^{-1}cm^{-2}$ using the Hill–Coleman method. This result is valuable for MOS capacitor applications. Dielectric parameters of the Ni/Au/$\beta$-$Ga_2O_3$/p-Si MOS capacitor were investigated in the wide frequency range (20 kHz–1 MHz) at room temperature. We observed that these parameters have a strong dependence on frequency and voltage. This is especially true in the depletion region. All these factors demonstrate the interesting characteristics of sol–gel assisted $\beta$-$Ga_2O_3$ thin film which could be implemented as a good gate dielectric in MOSFETs.

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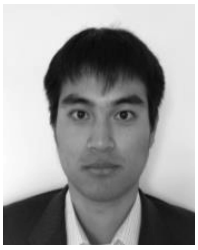

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