Title
On Decoupling Capacitor Size in GaN-Based Power Converters

Author
Horowitz, Logan

Publication Date
2022-06-01

Peer reviewed

2022 IEEE Workshop on Control and Modeling for Power Electronics (COMPEL 2022)

On Decoupling Capacitor Size in GaN-Based Power Converters

L. Horowitz
R. C. N. Pilawa-Podgurski

On Decoupling Capacitor Size in GaN-Based Power Converters

Logan Horowitz and Robert C.N. Pilawa-Podgurski
Department of Electrical Engineering and Computer Sciences
University of California, Berkeley
Email: {logan_h_horowitz, pilawa}@berkeley.edu

***Abstract*—High-performance hard-switched converters suffer from significant voltage overshoot and ringing upon switching transitions. This increases switch stress and electromagnetic interference, while also reducing reliability. Attempts to mitigate these drawbacks with increased gate resistance, or a slower switching device, yield reduced efficiency. Large bulk capacitors are typically required to meet voltage ripple constraints under load. As such, their package inductance is considerable and they may be placed far from the power path. A smaller decoupling capacitor is often placed near the switching devices in order to reduce overshoot. In this work, a circuit model is developed to describe converter operation during the switching transition, and a simple empirical equation for optimal decoupling capacitor sizing is proposed. The analyses are validated via experimental measurement of double pulse tests on a variety of hardware prototypes.**

I. Introduction

For a power converter operating under hard-switching conditions, significant dv/dt and di/dt will occur during the switching transition. When a device turns on, its conducted current must rise rapidly while its blocking voltage falls, and the reverse is true during turn-off. Ideally, these changes would happen instantaneously and the overshoot/settling time would be minimal. In reality, there is a parasitic inductance associated with the loop connecting the switching components, known as commutation loop inductance [1]. This causes the circuit to have a high quality factor, leading to large voltage overshoot and oscillation during switching transitions. As such, switch stress and electromagnetic interference (EMI) are increased, while reliability is diminished. These problems are especially relevant for wide-bandgap devices such as gallium-nitride high-electron-mobility transistors (GaN HEMTs) [2]–[5], which offer an improved figure of merit as compared to other technologies [6]. The small on-resistance and output capacitance of these devices causes the switching circuit to be especially underdamped, so excessive overshoot can occur.

In order to mitigate these issues, the quality factor of the circuit must be reduced. This is typically done by increasing the gate resistance, thereby slowing the switching transition, but converter efficiency will be reduced due to the increased overlap loss. Another option is to decrease the commutation loop inductance. This can improve performance somewhat, but large bulk capacitors are typically required to meet voltage ripple constraints under load. As such, their package inductance is considerable and they may need to be placed far from the power path. The use of a much smaller capacitor located closer to the switches, called a decoupling capacitor, allows for a reduced commutation loop inductance. Advanced layout techniques can be used to reduce this inductance further, but they are not always feasible as they require extra board area and increase manufacturing cost [7]–[9].

The process for decoupling capacitor sizing in power delivery networks (PDNs) has been studied [10], [11]. Power converter switching transitions differ from PDN load steps, however, because both the voltage and current at the converter input change throughout the switching interval. A detailed analysis specific to this application is therefore in order. Prior art has developed analytical models for transistor switching performance [12], [13], but these works focus on a boost-type switching circuit and utilize simplified models which neglect non-linear effects that are shown in this paper to be important. Reference [14] determined the proper sizing of decoupling capacitance to minimize EMI, but did not include the dependence on load current. This work builds upon these efforts by developing a model of the switching dynamics which provides insight for an empirically determined optimal decoupling capacitance in GaN-based power converters. The remainder of this paper is organized as follows: Section II introduces a simplified circuit model describing the switching dynamics and uses it to draw conclusions about decoupling capacitor sizing. Next, Section III validates the proposed model with simulation results and experimental measurement of double pulse tests on a variety of switching cells. Finally, Section IV concludes the paper.

II. Model Analysis

A. Simplified Circuit Model

Fig. 1a shows the simplified schematic of a synchronous buck converter undergoing a high-side turn-on, with the switch node voltage, V_{SW}, labeled. Subsequent analysis will focus on this circuit. The input voltage source may be ignored because it is assumed to have a higher impedance path than C_{IN}. The output filter and load can be treated as a current sink because the current through the large filter inductance will be roughly constant during the short switching interval. These simplifications yield Fig. 1b. Next, the input capacitor is separated into bulk and decoupling capacitance, each with a corresponding series parasitic inductance. Mutual inductance between these paths is neglected. The large bulk capacitance may be approximated as a voltage source because its voltage will be constant during the switching event. This gives Fig. 1c. Q_{LS} is off during the high-side turn-on, so its equivalent circuit is C_{OSS} in parallel with a body diode. The diode is on during the dead-time, but not during the transition itself, so it affects the initial conditions of the model but can be excluded

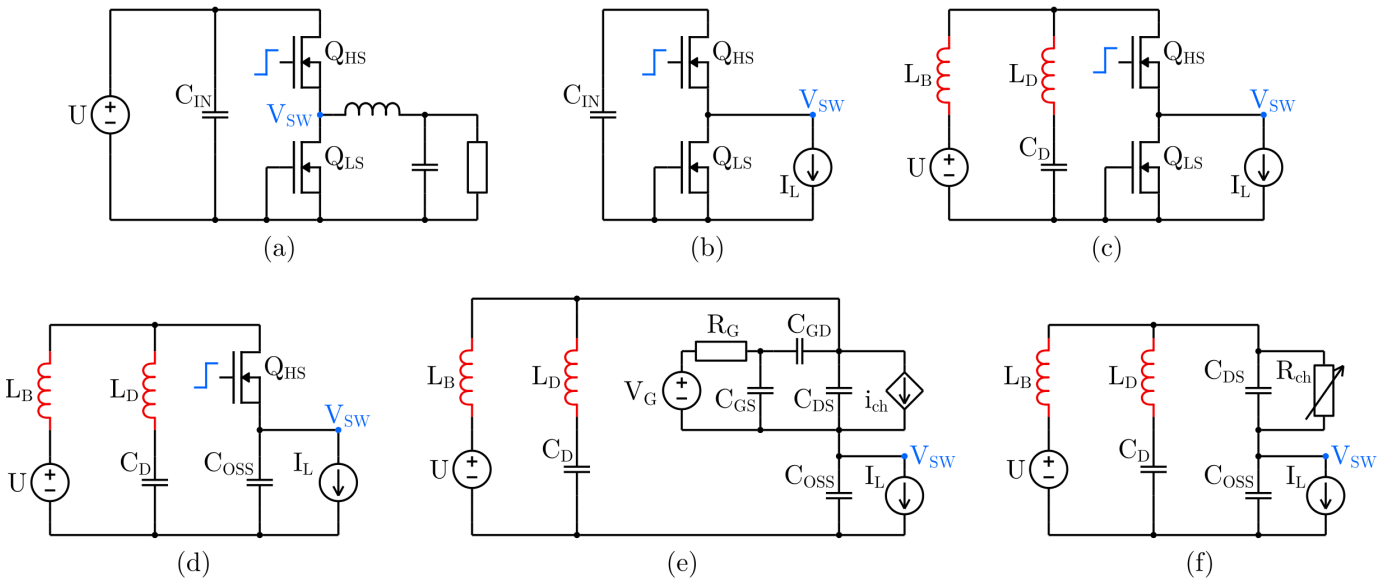

Fig. 1: Switching transition circuit models. (a) Synchronous buck converter high-side turn-on, (b) Input voltage removed and output filter treated as current sink, (c) Input capacitance separated into bulk and decoupling loops with bulk capacitance approximated as voltage source, (d) Low-side transistor replaced with output capacitance, (e) High-side transistor device model included, (f) Gate drive removed with channel modeled as controlled resistance.

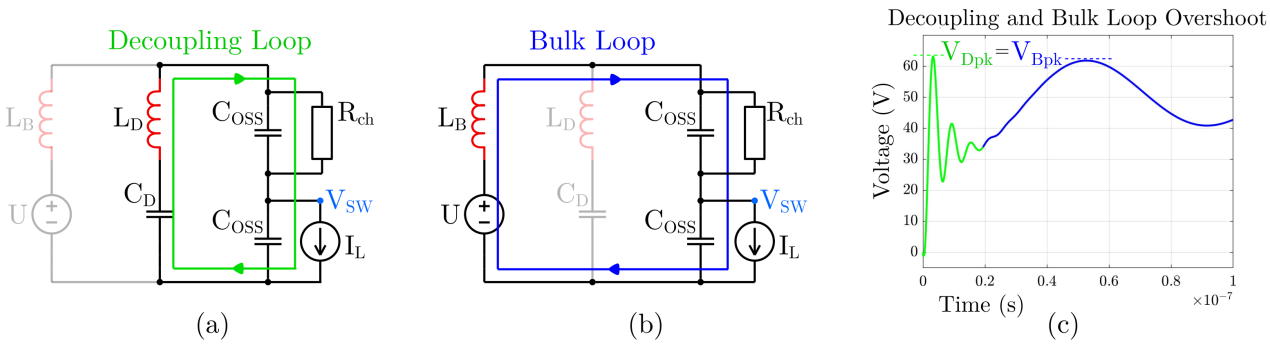

Fig. 2: Linear second order circuits. (a) Decoupling loop, (b) Bulk loop, (c) Simulation illustrating initial decoupling loop overshoot followed by bulk loop overshoot for V_{SW}.

from Fig. 1d. The device model of Q_{HS} is considered in Fig. 1e. Most of the current through Q_{HS} will be conducted by the channel, i_{ch}, and drain-to-source capacitance, C_{DS}, so the gate drive can be treated separately. Miller feedback is still considered, but the current through C_{GD} is not included in the main circuit. Finally, the voltage across and current into Q_{HS} are both strictly positive during the switching transition, so its channel can be viewed as a variable resistance controlled by the gate voltage, as in Fig. 1f.

B. Linear System Model

If a linear charge-equivalent capacitance value is used for C_{OSS}, and R_{ch} is assumed roughly constant, the circuit in Fig. 1f can be treated as a linear fourth order system. These assumptions will be dropped later, but are useful for intuition. In the following analysis, it will be assumed that both the bulk and decoupling loops are underdamped, which is reasonable for a well-designed, high-efficiency converter. In addition, it is assumed that L_D is much smaller than L_B. This is always true in practice, because otherwise the decoupling path serves no purpose. Given these assumptions, the circuit can be treated as two weakly coupled linear second order systems. The linear loop models are shown in Fig. 2, along with simulation results demonstrating the decoupling and bulk overshoots.

The initial dynamics are due almost entirely to the decoupling loop, which acts first before the current in L_B ramps up. C_D begins fully charged to the input voltage. During the switching transition, charge transfers to the output capacitance and load current. If C_D is too small, it loses all of its voltage during this process. The underdamped bulk loop will then generate significant overshoot as it charges up C_{OSS} the rest of the way. If C_D is large enough, however, it will maintain its voltage, so the bulk overshoot will be small because C_{OSS} is already charged up. If C_D is too large, it causes excessive decoupling loop overshoot on the switch node.

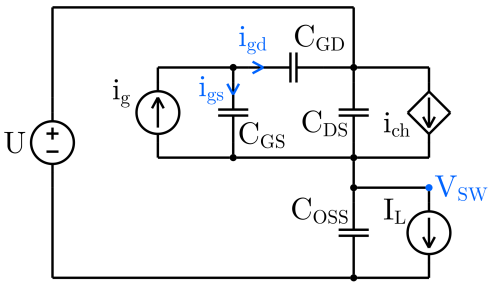

Fig. 3: Simplified schematic highlighting Q_{HS} device model.

C. Non-Linear Effects

The gate-to-drain capacitance of Q_{HS} is a non-linear component which significantly affects the switching dynamics. Fig. 3 shows a simplified circuit model without inductances, which are neglected here so that a useful analytical derivation of V_{SW} may be computed.

$$\dot{V_{GS}} = \frac{i_{gs}}{C_{GS}} = \frac{i_g - i_{gd}}{C_{GS}} \tag{1}$$

$$i_{gd} = C_{GD}\dot{V_{GD}} \approx C_{GD}\dot{V_{SW}} \tag{2}$$

$$\dot{V_{SW}} = \frac{i_{ch} - I_L}{C_{SW}} \tag{3}$$

$$\dot{i_{ch}} = \frac{\partial i_{ch}}{\partial V_{GS}}\frac{\partial V_{GS}}{\partial t} \approx g_m \dot{V_{GS}} \tag{4}$$

Equations (1)-(3) can be obtained through visual inspection, while (4) is derived from the saturation model of a transistor. Here, $i_g = (V_G - V_{GP})/R_G$, where V_{GP} is the gate plateau voltage of the device for the given load current. $C_{SW} = C_{OSS} + C_{DS}$, is the total capacitance on the switch node. The approximation in (2) is valid because the $\mathrm{dv/dt}$ of the switch node is much greater than that of V_{GS}. Combining (1)-(4) leads to (5).

$$\dot{i_{ch}} = \frac{g_m}{C_{GS}}(i_g - C_{GD}\dot{V_{SW}}) = \frac{g_m}{C_{GS}}(i_g - C_{GD}\frac{i_{ch} - I_L}{C_{SW}}) \tag{5}$$

The differential equation in (5) can be solved for i_{ch}, with an initial value of I_L.

$$i_{ch} = I_L + \gamma C_{SW}(1 - e^{-\alpha t}) \tag{6}$$

$\dot{V_{SW}}$ can be computed by combining this result with (3).

$$\dot{V_{SW}} = \gamma(1 - e^{-\alpha t}) \tag{7}$$

Here, $\gamma = i_g/C_{GD}$ and $\alpha = (g_m C_{GD})/(C_{GS}C_{SW})$. It is clear by looking at (7) that the maximum derivative of the switch node voltage is γ. V_{SW} cannot change faster than this because of the negative feedback loop with the gate drive through C_{GD}. When the device begins to turn on, this capacitance is small, so L_D and L_B restrict the rise of V_{SW}. As the drain-to-source voltage drops, however, the value of C_{GD} rises dramatically. For example, the EPC2218 GaN HEMT exhibits a 50x increase in the value of C_{GD} when its V_{DS} value goes to zero [15]. This is a non-linear characteristic which causes more damping at higher switching speeds. Skin and proximity effect are also increased at higher switching speeds [16]. As a result, the decoupling loop overshoot is damped more than the bulk loop overshoot, and much more than the linear model predicts. Decoupling loop overshoot is actually not a concern in practice due to these non-linear effects, and large C_D values do not increase overshoot. Fig. 4 plots simulation results with linear C_{GD} versus non-linear C_{GD} and illustrates this damping effect.

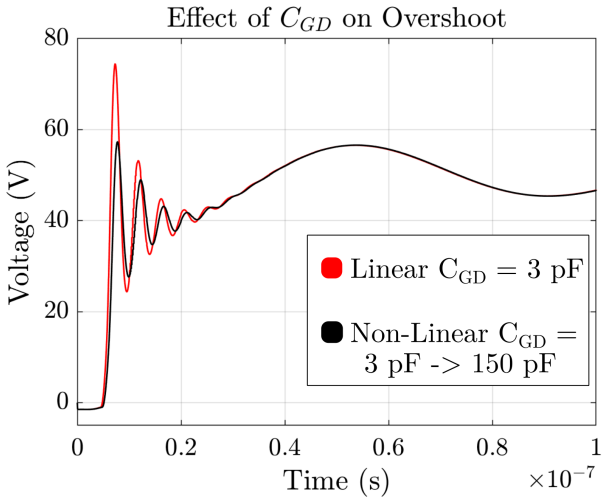

Fig. 4: Simulation results demonstrating effect of non-linear C_{GD} on voltage overshoot. Using actual datasheet gate-drain capacitance curve for EPC2218.

D. Optimal Decoupling Capacitor Sizing

An approximate optimal value for C_D can be estimated based on the previous conclusions, using voltage overshoot and decoupling capacitor size as the performance metrics. The decoupling loop must source the initial load current before the bulk inductor current ramps up. During this time, as the switch node voltage rises from $0V$ to the input voltage, U, the average voltage across L_B is approximately $U/2$. Given the fundamental inductor equation, $di_L/dt = v_L/L$, the following equation calculates the time necessary for the bulk inductance to carry the full load current, in the worst case.

$$t_D = \frac{2L_B I_{ML}}{U_{ML}} \tag{8}$$

Here, I_{ML} is the max load current and U_{ML} is the minimum input voltage for which that current will be drawn. The charge required from the decoupling capacitance during this time is

$$Q_R = \frac{2L_B I_{ML}^2}{U_{ML}} \tag{9}$$

while the charge on C_D is

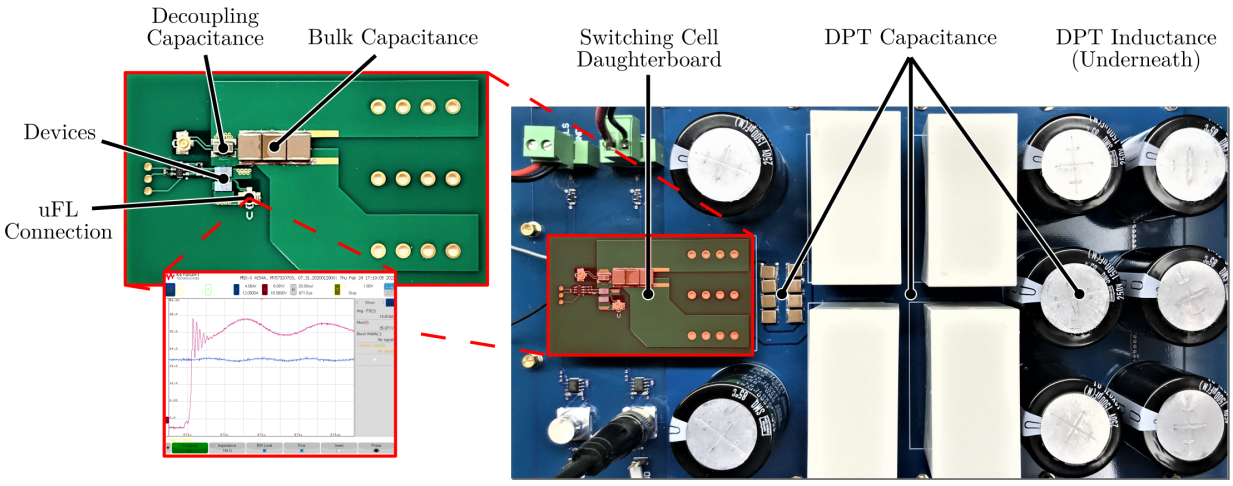

Fig. 5: Hardware setup with double pulse testing motherboard and half-bridge switching cell daughterboard.

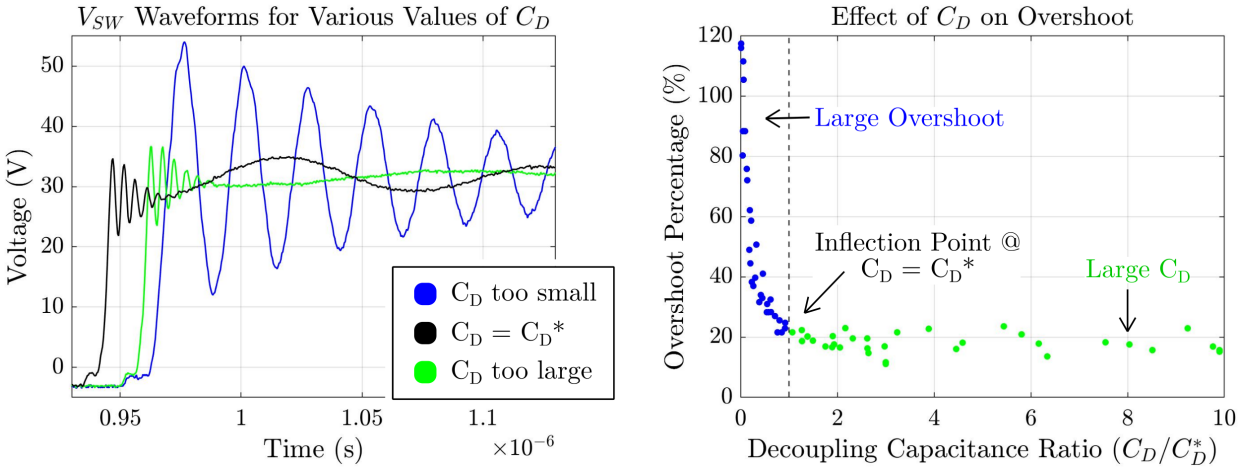

Fig. 6: (a) Experimental waveforms demonstrating minimal overshoot at $C_D = C_D^*$, (b) Experimental results showing inflection point at $C_D = C_D^*$ and that overshoot percentage is small for $C_D > C_D^*$.

$$Q_D = C_D U_{ML} \tag{10}$$

These equations can be rearranged to determine the required capacitance value to source the load current.

$$C_{R1} = \frac{2L_B I_{ML}^2}{U_{ML}^2} \tag{11}$$

The decoupling capacitor must be large enough to charge up C_{OSS} as well.

$$C_{R2} = C_{OSS} \tag{12}$$

C_D must be larger than these two requirements; if $C_D = C_{R1}$ or $C_D = C_{R2}$, the voltage on the decoupling capacitor will drop all the way to zero during t_D. It is empirically determined that a margin of 10x provides enough charge to source these loads, without excess size. Larger values of C_D require bigger packages with more package inductance, which is detrimental to performance, while smaller values exhibit more overshoot. As such, $C_D = C_D^*$ is deemed optimal. This is the inflection point in Fig. 6b, yielding the following design guideline for the optimal sizing of C_D.

$$C_D^* = 10 * \max\{C_{OSS}, \frac{2L_B I_{ML}^2}{U_{ML}^2}\} \tag{13}$$

III. Hardware Results

In order to validate the proposed model and conclusions, a system for double pulse testing (DPT) is employed. The design utilizes a motherboard which houses the large inductance and capacitance required for the test. Modular daughterboards can be swapped in, each containing a different half-bridge switching cell. This setup allows for the following parameters to be swept: blocking voltage, load current, switching device, decoupling capacitance, bulk capacitance, decoupling loop inductance, and bulk loop inductance. For switch node measurements, a 1.5 GHz, 5 GSa/s, Keysight InfiniiVision MSOX4154A oscilloscope is used with 750 MHz N2894A

Table 1: Switching Cell Parameters

Parameter	Value(s)
Switching Device	EPC2218, EPC2212
Blocking Voltage	10 V – 80 V
Load Current	0 A – 40 A
Gate Resistance	5 Ω, 10 Ω
Decoupling Capacitance	0 nF – 300 nF
Bulk Capacitance	6.6 uF
Decoupling Loop Inductance	1 nH
Bulk Loop Inductance	3.5 nH, 14.5 nH

passive probe connected to a surface-mount uFL connector. EPC GaN HEMTs are used as the switching devices for all of the tests. Fig. 5 shows the setup.

Fig. 6a shows V_{SW} waveforms for three different values of decoupling capacitance, with a blocking voltage of 30 V, load current of 27 A, 10 Ohm gate resistance, 1 nH decoupling loop inductance, 3.5 nH bulk loop inductance, and EPC2218 switching device. The overshoot percentage is very large (80%) with $C_D = 5.6nF$, and much smaller (13%) for the optimally sized $C_D = 60nF$. When the decoupling capacitance is increased beyond the optimal point, to $C_D = 300nF$, the peak overshoot percentage increases slightly to (23%).

More than 200 DPT measurements are made across various operating points. Table 1 lists the parameter variations for these tests. Fig. 6b plots the percent overshoot of V_{SW} as a function of C_D/C_D^*. The inflection point at $C_D = C_D^*$ is clearly visible. Experimental data shows consistently that throughout all measurements, a C_D value below C_D^* leads to increased overshoot, while increasing the value of C_D beyond C_D^* has little effect. According to the linear model, there would be excessive decoupling loop overshoot at high values of C_D/C_D^*, but the damping effect of C_{GD} counteracts this so that overshoot remains constant beyond the inflection point.

IV. Conclusion

This work has presented a simplified circuit model describing converter operation during the high-side turn-on switching transition of a synchronous buck converter. Weakly coupled linear second order systems are derived and it is determined that separate decoupling and bulk loop overshoots will occur. The most important deviation from the linear model is described: non-linear gate-drain capacitance, which causes decoupling loop overshoot to be highly damped. Finally, a simple empirical optimal point is found for the sizing of C_D, which achieves minimal overshoot without excess size. Future work will expand these results to other switching transitions and devices.

V. Acknowledgments

The authors gratefully acknowledge support for this work from the U.S. Department of Energy through the Electric Drive Technologies Consortium under award DE-EE0008712.

References

[1] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Springer, 2001.

[2] D. Reusch, F. C. Lee, D. Gilham, and Y. Su, "Optimization of a high density gallium nitride based non-isolated point of load module," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 2914–2920.

[3] N. C. Brooks, L. Horowitz, R. Abramson, and R. C. N. Pilawa-Podgurski, "Low-inductance asymmetrical hybrid gan hemt switching cell design for the fcml converter in high step-down applications," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 9–15.

[4] T. Modeer, N. Pallo, T. Foulkes, C. B. Barth, and R. C. N. Pilawa-Podgurski, "Design of a gan-based interleaved nine-level flying capacitor multilevel inverter for electric aircraft applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 12 153–12 165, 2020.

[5] Y. Lei, C. Barth, S. Qin, W.-C. Liu, I. Moon, A. Stillwell, D. Chou, T. Foulkes, Z. Ye, Z. Liao, and R. C. N. Pilawa-Podgurski, "A 2-kw single-phase seven-level flying capacitor multilevel inverter with an active energy buffer," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8570–8581, 2017.

[6] J. Azurza Anderson, G. Zulauf, J. W. Kolar, and G. Deboy, "New figure-of-merit combining semiconductor and multi-level converter properties," *IEEE Open Journal of Power Electronics*, vol. 1, pp. 322–338, 2020.

[7] L. Horowitz and R. C. Pilawa-Podgurski, "Modular switching cell design for high-performance flying capacitor multilevel converter," in *2022 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2022, pp. 342–347.

[8] N. Pallo, T. Modeer, and R. C. Pilawa-Podgurski, "Electrically thin approach to switching cell design for flying capacitor multilevel converters," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, 2017, pp. 411–416.

[9] K. Wang, L. Wang, X. Yang, X. Zeng, W. Chen, and H. Li, "A multiloop method for minimization of parasitic inductance in gan-based high-frequency dc–dc converter," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4728–4740, 2017.

[10] G. Han, "Simple and fast method of on-board decoupling capacitor selection and placement," in *2017 IEEE Electrical Design of Advanced Packaging and Systems Symposium (EDAPS)*, 2017, pp. 1–3.

[11] A. Sanna and G. Graziosi, "Optimization of on-package decoupling capacitors considering system variables," in *2018 IEEE 22nd Workshop on Signal and Power Integrity (SPI)*, 2018, pp. 1–4.

[12] W. Teulings, J. Schanen, and J. Roudet, "Mosfet switching behaviour under influence of pcb stray inductance," in *IAS '96. Conference Record of the 1996 IEEE Industry Applications Conference Thirty-First IAS Annual Meeting*, vol. 3, 1996, pp. 1449–1453 vol.3.

[13] Y. Xiao, H. Shah, T. Chow, and R. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on mosfet switching characteristics," in *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition, 2004. APEC '04.*, vol. 1, 2004, pp. 516–521 Vol.1.

[14] Z. Chen, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of dc-link decoupling capacitors," in *2013 IEEE Energy Conversion Congress and Exposition*, 2013, pp. 1886–1893.

[15] (2022) Epc2218 datasheet. [Online]. Available: https://epc-co.com/epc/Portals/0/epc/documents/datasheets/EPC2218_datasheet.pdf

[16] E. E. Kriezis, T. D. Tsiboukis, S. M. Panas, and J. A. Tegopoulos, "Eddy currents: theory and applications," *Proceedings of the IEEE*, vol. 80, no. 10, pp. 1559–1589, 1992.