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High-Speed Sub-THz/THz Interconnects with Advanced Spatial Multiplexing

By

Xuan Ding

DISSERTATION

Submitted in partial satisfaction of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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DAVIS

Approved:

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Committee in Charge

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Contents

Abstract iv

Acknowledgements vi

Acronyms vii

List of Figures xi

List of Tables xvii

Chapter 1. Introduction 1

1.1. Sub-THz/THz Applications 2

1.2. Sub-THz/THz Interconnects 4

1.3. Outline of the Dissertation 6

Chapter 2. Key Blocks and Techniques for Sub-THz/THz Interconnect 9

2.1. Passive Components 9

2.2. Active Components in CMOS 24

2.3. sub-THz/THz Detection and Key Blocks 29

2.4. Multiplexing Schemes at sub-THz/THz 40

2.5. Conclusion 46

Chapter 3. Dual-band Sub-THz Interconnect 47

3.1. FDM Implement: Dual-band Si DWG Channel 48

3.2. Dual-band sub-THz Interconnect system 55

3.3. Transmitter 57

3.4. Receiver 63

3.5. Fabrication and System Packaging 66

3.6. Measurement Results and Conclusion 69

Chapter 4. Theoretical Analysis and Demonstration of Multi-drop DWG 72

4.1. Mode in Rectangular DWGs 72

4.2. Directional Mode Coupler 81

4.3. Multi-Drop Si DWG Channel Design 99

4.4. Demonstration and Measurement 108

4.5. Conclusion 112

Chapter 5. Multi-mode and Multi-drop Sub-THz Interconnect 113

5.1. MDM Implement: Multi-mode and Multi-drop sub-THz Interconnect 114

5.2. Transmitter 118

5.3. Receiver 120

5.4. Fabrication and Packaging 126

5.5. Measurement Results and Conclusion 129

Chapter 6. Conclusions 135

6.1. Summary 135

6.2. Future Directions 137

Bibliography 139

High-Speed Sub-THz/THz Interconnects with Advanced Spatial Multiplexing

Abstract

Ever-increasing data generation and transmission demands have been driving great advancements in wireline communications from both electrical and optical approaches for short- and long-distance scenarios, respectively. In the meter range scenario, both electrical and optical approaches face great challenges. That is, the lossy and bandwidth limited channels are the bottlenecks of electrical interconnect. For optical interconnect, the features, such as the required complex fabrication and the high environment sensitivity, increase the power and cost budgets significantly, making it uneconomical for short-distance communications. To mitigate these issues, low-loss dielectric channel-based interconnects have been investigated and demonstrated. However, all the design reported are all for point-to-point configurations, not suitable for multi-drop distributed architectures.

Besides CMOS transmitters and receivers, advanced spatial multiplexing schemes are fully investigated and architectures of wireline communication system at sub-THz/THz are selected according to the application scenarios. This dissertation also investigates the most used passive and active, on-chip and off-chip components, circuit modeling, layout optimization, and design strategies, such as neutralization and power maximization methods.

Two sub-THz interconnect systems, frequency division multiplexing (FDM) based dual-band sub-THz interconnect and mode division multiplexing (MDM) multi-drop sub-THz interconnect, are proposed and demonstrated.

A low-loss and wideband Si dielectric waveguide (DWG) coupled with a pair of diplexers is employed to support two highly isolated and low loss sub-channels simultaneously. The proposed sub-THz interconnect achieves the energy efficiency of 1.58 pJ/b with the aggregate data rate of 22.6 Gb/s and BER better than 10^{-12}. It demonstrates the record bandwidth density of 150.7 Gb/s/mm^2. Channelization provides a venue to boost the interconnect key metric of bandwidth density by taking full advantages of the abundant THz spectrum resource.

The theory of DWG mode coupler is derived and explained in Chapter 4, and it can guide the multi-mode multi-drop waveguide design and provide optimization strategies effectively. Then

a multi-drop sub-THz interconnect system is demonstrated, enabling three simultaneous logical channels for E_{11}^{y}, E_{21}^{y} and E_{31}^{y} mode and supporting data rates of 24 Gb/s, 22 Gb/s and 19 Gb/s, respectively, with the BER better than 10^{-12}. The demonstrated aggregate data rate of the three channels is 65 Gb/s with the energy efficiency of 1.6 pJ/b.

To the authors' knowledge, This is the first time to demonstrate multi-mode multi-drop DWG based interconnect. One note to make is that although the demonstration channel length is 5.2 cm, this is due to the size constraint of the wafer used to fabricate the channel. This interconnect system can be readily extended to the meter range due to the channel ultra-low loss feature. Furthermore, it can also scale to more modes to support more logic channels per physical link and can be extended to multi-dimension, two-/three- dimension, interconnect systems. Besides, with more advanced semiconductor technologies for active circuits, the data rate per channel will be further increased. Therefore, we believe that demonstrated multi-mode multi-drop sub-THz interconnect systems open a new path with high potentials to complement the existing electrical and optical interconnect to address the challenging meter range wireline communication scenarios.

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Lastly, I would like to thank my family. Their words of encouragement and company never failed to cheer me up and help me through the difficult time.

Acronyms

ADC: analog to digital converter. 41

ASK: amplitude-shift keying. 58

AWG: arbitrary waveform generators. 129, 131

BCB: Benzocyclobutene. xiii, 10, 43, 51, 53, 54, 66, 67

BER: bit error rate. iv, v, xi, 5–7, 47, 56, 69, 70, 114, 130, 132, 136

BiCMOS: bipolar complementary metal-oxide-semiconductor. 19, 25, 29, 30

BJT: bipolar iunction transistor. 25

BPF: band-pass filter. xiii, 42, 43, 50, 51, 53

CMOS: complementary metal oxide semiconductor. iv, xi, xvi, 2–4, 6, 7, 9, 10, 12, 13, 15, 16, 18–20, 22, 24–27, 29–31, 33, 37, 46, 55, 57, 58, 66, 116, 118, 125–127, 130, 135, 136

CPW: coplanar waveguide. xi, 10, 14, 15, 101

CPWG: grounded coplanar waveguide. xi, 10, 14, 15

CTLE: continuous time linear equalization. xvi, 8, 116, 118, 120, 124, 125, 136

DAC: digital to analog converter. 41

DCOC: DC offset cancellation. xiv, 65

DRIE: deep reactive ion etching. 67, 68, 100, 108, 137

DWG: dielectric waveguide. iv, v, xiii–xv, 5, 7, 8, 15, 41–45, 47–50, 53–55, 67, 68, 72, 73, 76, 77, 81, 82, 84, 95, 98–109, 111–116, 126, 127, 133, 136, 137

ED: envelope detector. xiv, 29, 55, 56, 63, 64, 115–118, 120–122, 124

EI: electrical interconnect. 4, 5

EIRP: effective isotropic radiated power. 3

EM: electromagnetic. 7, 15, 18, 87

FDM: frequency division multiplexing. iv, xi, 6, 7, 9, 42, 47, 48, 70, 72, 113, 134, 136, 137

FDTD: finite-difference time-domain. 105

FEM: finite element analysis. 105

FET: field-effect transistor. 30

GaAs: gallium arsenide. 13

GaN: gallium nitride. 13

GSG: ground-signal-ground. xi, 11, 13–15, 43, 50, 51, 101, 109, 124, 129

HBT: heterojunction bipolar transistor. 25, 30

HEMT: high-electron-mobility transistor. 25

HPF: high-pass filter. 65

IC: integrated circuit. 2, 5, 22, 24

InP: indium phosphide. 25

IoT: internet of things. 24

LA: limiting amplifier. xiv, 63–65

LNA: low noise amplifier. xvi, 3, 8, 28–31, 56, 115–118, 120–124, 133, 136

LO: local oscillator. 3, 6, 30, 32, 48, 130, 131

LPF: low-pass filter. 63, 65

MDM: mode division multiplexing. iv, 7, 42, 44, 72, 99, 113, 134, 137

MESFET: metal-semiconductor field-effect transistor. 25

MOS: metal oxide semiconductor. 18

MSL: microstrip line. xiii, xv, 7, 42–45, 48–50, 54, 72, 100–102, 104, 115, 116, 136

NEP: noise equivalent power. xii, xvi, 29–31, 56, 64, 116, 117, 120–122

NF: noise figure. 56, 120–122, 124

NMOS: N-channel metal oxide semiconductor. 57, 118

OI: optical interconnect. 4, 5

OOK: on-off keying. 47, 48, 55–57, 62, 63, 115, 117, 118, 127, 129, 132, 136

PA: power amplifier. 55, 57, 59, 115

PCB: printed circuit board. 126, 127, 129

PCell: parameterized cell. 15

PDE: partial differential equations. 76

PLL: phase locked loop. 30, 41, 55

PN: phase noise. 33, 37–40

PRBS: pseudorandom binary sequence. 47, 69, 70, 129, 131, 136

Q: quality factor. xi, xii, 10, 16, 18–24, 28, 34, 35, 42, 52

QAM: quadrature amplitude modulation. 30, 138

QPSK: quadrature phase-shift keying. 138

RBW: resolution bandwidth. 3

RMS: root-mean-square. 3

SiGe: silicon germanium. 25, 29, 30

SNR: signal-to-noise ratio. 3, 4, 29, 30, 40, 56, 57, 117, 120, 129, 132

SOA: State-of-the-Art. 7, 137

SOC: system on chip. 24

SPST: single pole single throw. xiv, 62, 63, 118

TC: temperature coefficient. 16

TDM: time division multiplexing. 7, 9, 136

TEM: transverse electromagnetic. 6, 11

THz: terahertz. 1

TSV: through-substrate via. 11, 15

VCO: voltage-controlled oscillator. xii, 32, 33, 37, 38, 46, 47, 62

VLSI: very large scale integration. 24

List of Figures

1.1 THz range and applications along the spectrum [K. Fukunaga et al. Applied Physics, 2010] 2

1.2 (a) Configuration and (b) measurements of a THz imaging system 3

1.3 (a) Structure, (b) E-field distribution and (c) measurements of micro-ring based THz sensor 4

1.4 (a) System configuration, (b) measurement setup, (c) measured data rate and bit error rate (BER) of an ortho-mode sub-THz interconnect 5

1.5 (a) System architecture, (b) measurement setup, (c) measured received power, data rate, eye diagrams and BER of an FDM THz Interconnect 6

2.1 Different types of transmission lines: (a) microstrip Line, (b) strip line, (c) CPW, (d) CPWG, (e) differential line, (f) grounded differential line, (g) slot line and (h) grounded slot line 11

2.2 Cross-section configuration of a microstrip line 12

2.3 Typical microstrip-lines on thin substrates (quartz): (a) microstrip-line with AC-coupled GSG, (b) CPWG and (c) CPW 14

2.4 (a) First-order transverse mode at 55 GHz and (b) second-order transverse mode at 66 GHz in a CPWG configuration 14

2.5 Metallization of a RF and mix-signal purpose CMOS technology. 16

2.6 MOM capacitors: (a) parallel-plate capacitor and (b) multi-finger capacitor. 18

2.7 Simulated (a) capacitance and (b) Q 19

2.8 MOS capacitor configuration and modeling 19

2.9 Inductor (a) without dummy fills, (b) with external dummy fills, (c) with internal dummy fills, (d) with both external and internal dummy fills, (e) with larger internal dummy fills and (f) with all layer (including M9) dummy fills. (g) Simulated inductance, self-resonance frequency and (h) Q-factor for all cases. 21
2.10 (a) Schematic and layout of transformers (b) on Metal 9; (c) on Metal 8 and Metal 9. 22
2.11 Lumped element model of a transformer. 23
2.12 Breakdown voltage and f_T of standard semiconductor technologies [J. Zhang et al., SiRF, 2020] 25
2.13 (a) Schematics of a transistor and (b) embedding network 26
2.14 (a) Schematic and (b) layout of a capacitor neutralized transistor pair. G_{max} (c) before and after capacitor neutralization. 28
2.15 Example of transformer neutralization. 29
2.16 NEP comparison of Si-based receivers [D. Yoon et al., EuCAP, 2013] 30
2.17 Diagrams of direct detection and homodyne detection 30
2.18 Active and resistive (passive) detectors. 31
2.19 Schematic of the proposed superharmonic injection based quadrature VCO. 32
2.20 (a) The equivalent model, (b) phasor relationship, and (c) the maximum phase difference at the edge of injection lock. 34
2.21 (a) Schematic of a cross-coupled oscillator and (b) its equivalent circuit 35
2.22 (a) Top view of the transformer in EM simulation. (b) Equivalent parallel resistance Z_{in} and boosted Z_{load} by tuning the coupling coefficient k of the transformer. 36
2.23 (a) Block diagram of I/Q signal test chip for phase and aptitude mismatch. Die micrographs of (b) the I/Q test chips and (c) standalone quadrature VCO. 37
2.24 Measurement setups for output power, frequency at G-band, and phase and amplitude error at down-converted frequency. 38
2.25 (a) Spectrum, (b) measured output power, DC-to-RF efficiency and oscillation versus the bulk control voltage, (c) phase noise at 152.4 GHz. 38
2.26 Measured quadrature signals down-converted to 3.7 GHz. 39
2.27 Spatial multiplexing schemes [P. Winzer, Nature Photonics, 2014] 40

2.28 (a) Frequency division, (b) mode division, and (c) polarization multiplexing. 41
2.29 (a) Structure of the dual-band channel, (b) MSL-to-DWG transition, and (c) diplexer on BCB substrate. 43
2.30 (a) Stucture of the ortho-mode channel, (b) single-ended to differential transition, (c) probe-based MSL-to-DWG transition. (d) Comparison of the simulated and measured S-parameters. 44
2.31 (a) Structure of the multi-drop channel, (b) mode coupler between $E_{11}^{y} - E_{21}^{y}$ and $E_{11}^{y} - E_{31}^{y}$, and (c) the E field distribution. 45
3.1 Si-based DWG, its E field distribution and S-parameters. 48
3.2 (a) Configuration, (b) E-field distribution and (c) S parameters of the MSL-to-DWG transition 49
3.3 (a) A straight DWG and (b) its measured S-parameters 50
3.4 Structure of the BPF based diplexer 50
3.5 Input impedance of the BPFs. 51
3.6 Resonator based dielectric sensor 52
3.7 Simulated S-parameters of the BPFs 53
3.8 Structure of the dual-band Si DWG channel. 53
3.9 Photo and G-band S-parameter measurement setup. 54
3.10 Measured S-parameter. 54
3.11 Architecture of the dual-band sub-THz interconnect. 55
3.12 Link budget and bandwidth budget of the dual-band sub-THz interconnect. 56
3.13 Schematic of the transmitter. 57
3.14 (a) Topology of an colpitts oscillator and (b) its equivalent two-port network model . 58
3.15 (a) Transistor with parasitic elements and (b) its large-signal model 59
3.16 Transistor with (a) lumped element feedback network and (b) synthesized transformer model. 60
3.17 (a) Calculated optimum ϕ versus frequency. (b) Procedure of power maximization for an oscillator. 61

3.18 (a) Measurement setup for sub-THz oscillator. The measured spectrum at (b) 140 GHz and (c) 180 GHz. 62

3.19 Shunt transistor SPST and its on-/off- circuit model. 63

3.20 (a) Architecture of the receiver and (b) schematic of the ED 64

3.21 Baseband LA with DCOC loop. 65

3.22 Diplexer board fabrication 66

3.23 Si DWG fabrication 67

3.24 Dual-band sub-THz interconnect assembling 68

3.25 The photo of transmitter and receiver chipsets, system board and full-duplex measurement setup for the dual-band sub-THz interconnect 69

3.26 (a) Maximum error-free date rate and (b) the corresponding eye diagrams in full-duplex configuration 70

4.1 A multi-mode dielectric waveguide and its E field distribution and magnitude for E^y_{11}, E^y_{21} and E^y_{31} modes. 73

4.2 Cross-section and dimensions of a rectangular DWG 77

4.3 Wavenumber Relation in a Rectangular Waveguide 78

4.4 Simulated effective refractive index n_{eff} for the three modes (E^y_{11}, E^y_{21} and E^y_{31}) in Si DWG versus waveguide width at 165 GHz 82

4.5 (a) Cross-section and E field profiles of a rectangular DWG coupler. (b) Refractive index distribution N^2, (c) $N^2 - N_1^2$ and (d) $N^2 - N_2^2$ 84

4.6 Calculated and simulated coupling coefficient versus the waveguides' (a) width of W and (b) gap of G. 91

4.7 (a) Geometry illustration of a DWG coupler. Calculated power intensity $P_1(z)$ in waveguide 1 and $P_2(z)$ in waveguide 2 along z-direction with different coupling efficiency factor F, coupling coefficient κ and attenuation constant α: (b) $\kappa = 0.4$, $\alpha = 0$ and $F = 0.6, 0.8, 1$; (c) $F = 1$ (δ_β=0), $\alpha = 0$ and $\kappa = 0.3, 0.4, 0.5$; (d) $F = 1$ ($\delta_\beta = 0$), $\kappa = 0.4$ and $\alpha = 0.02$. 94

4.8 Frequency-dependent parameters of the DWG and mode coupler for the three different modes with different DWG widths: (a) effective refractive index n_{eff}, (b) coupling coefficient κ and (c) δ_β^2/κ^2 which is the only determining variable in the coupling efficiency factor F theoretical representation. 95

4.9 Calculated coupling efficiency η, coupling efficiency factor F and mode crosstalk for (a) E_{11}^y-E_{11}^y, (b) E_{11}^y-E_{21}^y and (c) E_{11}^y-E_{31}^y mode couplers 97

4.10 Simulated coupling efficiency for (a) E_{11}^y-to-E_{11}^y, (b)E_{11}^y-to-E_{21}^y and (c) E_{11}^y-to-E_{31}^y mode couplers versus the frequency and coupler length L_C. 98

4.11 (a) 3-D view of the new mode-coupler-based multimode Si dielectric waveguide, and (b) the top view of mode couplers. 99

4.12 (a) Dimensions of the acrshortmsl-to-acrshortdwg transition. Simulated propagation constant comparison between (b) TEM mode in MSLs of width of 10 $\sim$ 200 μm and (c) E_{11}^y mode in DWGs of width of 50 $\sim$ 300 μm. 101

4.13 E field distribution in (a) straight DWG mode couplers, and (b) bended DWG mode couplers. 102

4.14 (a) Top view of the DWG mode coupler, and (b) E field distribution. 103

4.15 Calculated and simulated performance of uniform-width and one-side tapered mode couplers: Coupling efficiency of (a) E_{11}^y-E_{21}^y and (b) E_{11}^y-E_{31}^y; Crosstalk from (c) E_{11}^y and (d) E_{31}^y modes in E_{11}^y-E_{21}^y coupler; Crosstalk from (e) E_{11}^y and (f) E_{21}^y modes in E_{11}^y-E_{31}^y coupler. 104

4.16 (a) Top view of the DWG mode coupler, and (b) E field distribution. 105

4.17 Light ray trace inside (a) rectangular, (b) one-side tapered and (c) symmetric tapered DWG. 106

4.18 Bending loss analysis: E field distribution of (a) E_{11}^y in $W = 0.34\ mm$ and $R = 0.66\ mm$, (b) E_{21}^y in $W = 0.76\ mm$ and $R = 1.0\ mm$, (c) E_{31}^y in $W = 1.2\ mm$ and $R = 1.4\ mm$, (d) E_{11}^y in $W = 1.2\ mm$ and $R = 1.4\ mm$, (e) E_{21}^y in $W = 1.2\ mm$ and $R = 1.4\ mm$, (f) E_{31}^y in $W = 1.2\ mm$ and $R = 1.4\ mm$ and (g) their S parameters 107

4.19 Assembling process with a flip-chip bonder and photo of the DWG. 109

4.20 (a) Measurement setup with network analyzer and frequency extender. Photos of the (b) sample and (c) testbench . . . 110
4.21 (a) Measurement setup with tripler and down-convert mixer. (b) Through and (c) crosstalk tests . . . 110
4.22 Simulated and measured S-parameters of the multimode Si dielectric waveguide. . . 111

5.1 A communication networks with multi-drop channels. . . . 114
5.2 Multi-drop system diagram. . . . 115
5.3 Si multi-drop waveguide and package. . . . 116
5.4 Link budget and bandwidth budget of the multi-drop sub-THz interconnect. . . . 117
5.5 (a) Schematic of the transmitter. (b) EM modeling and (c) simulated S parameter of the switch modulator. . . . 119
5.6 (a) Die photo of the transmitter, (b) measurement setup and (c) measured power and spectrum . . . 120
5.7 Schematic of the receiver. . . . 121
5.8 Simulated R_v and NEP versus LNA's volatage gain. . . . 121
5.9 (a) Schematic of LNA. EM modeling of the (b) input matching and (c) transformers. 123
5.10 Simulated S parameters of the LNA. . . . 123
5.11 Schematic and simulated voltage gain of the CTLE. . . . 124
5.12 Schematic CTLE unit and its frequency response. . . . 125
5.13 Package design of the multi-drop sub-THz interconnect . . . 126
5.14 Flip-chip bonding process for CMOS dies . . . 127
5.15 System packaging process . . . 128
5.16 Die photos of the transmitter and receiver . . . 129
5.17 Single link measurement . . . 130
5.18 Photos of the multi-drop sub-THz interconnect system and measurement setup . . . 131
5.19 Measured waveforms, eye diagrams and bathtub curves at multi-mode configuration. 132
5.20 Power consumption breakdown. . . . 133

List of Tables

2.1 Comparison of the probe testable interfaces. 15

2.2 Comparisons of Semiconductor Technologies for RFIC. 25

2.3 Comparison with state-of-the-art QVCO at mm-wave/sub-THz in Si. 39

3.1 Dimensions of the diplexer (unit: μm). 51

3.2 Comparison of state-of-the-art duplex sub-THz/THz interconnect. 71

4.1 Comparison with the state-of-the-art multi-channel transmission above 100 GHz. . . 112

5.1 Comparison of state-of-the-art sub-THz/THz interconnect. 134

CHAPTER 1

Introduction

terahertz (THz) spectrum and applications have been actively studied in these decades. THz waves (0.1∼10 THz) are non-invasive, can penetrate opaque materials, and can be used to obtain fingerprint spectra whose characteristics depend upon molecular and inter molecular behavior [**1**]. Unlike the mid-infrared region, no commercial spectral library is available for the THz region. Consequently, a spectral database of artists' materials was developed in order to include THz spectroscopy among conservation science techniques. Most pigments and some synthetic polymers have characteristic fingerprint spectra in the THz region. With this technique most of these materials used in paintings can be identified alone or as paint, a combination of pigments and binders. Although the meaning of the spectral features has so far not been fully explained, previous studies on optical materials suggest that phonon absorption and the behavior of hydrogen bonds contribute to their spectral features. Examples of THz spectra of various art materials are discussed on the basis of measurements obtained using a conventional Fourier transform system [**2**].

The THz waves is comprised in 0.1∼10 THz range (0.03∼3 mm in wave length), just at the border between phonics and electronics. Unlike the millimeter or the mid-infrared regions, in the past this frequency range was used only for specialized high profile academic researches, such as astrophysics and semiconductor physics, by using in-house or custom made systems. In addition, the lack of stable THz sources was a significant impediment for its more extensive use. Consequently, this 'void' in the use of the THz radiation is referred to as 'THz gap' as shown in Figure 1.1 [**3**]. Thanks to the recent development of stable sources [**4**], THz is becoming more widely used as non-invasive test equipment. In the previous years, THz spectroscopy and imaging have mostly been utilized as nondestructive methods for the inspection of products which require high quality standard of production, such as materials for space industry. It is also considered a reliable solution for security problems. For instance, in several airports THz inspection systems have been installed to detect the presence of substances considered dangerous [**5**]. Due to the fact that THz technique is

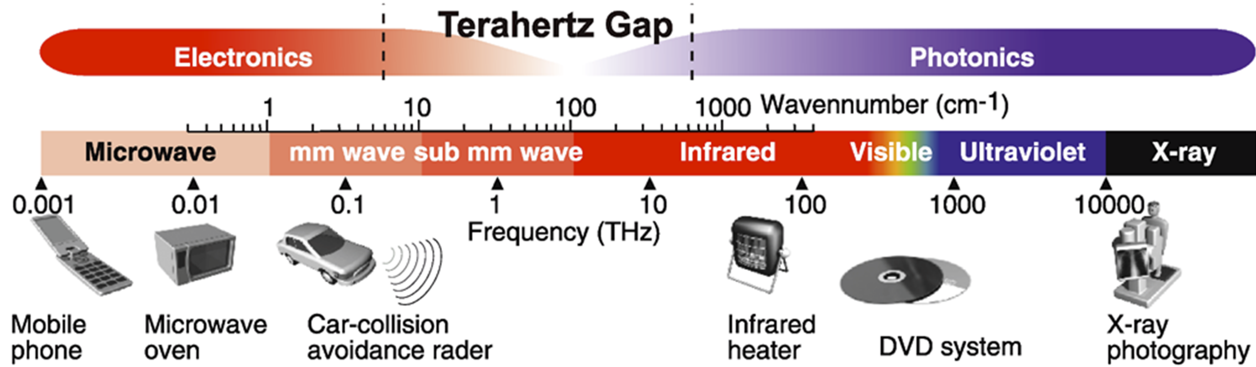


FIGURE 1.1. THz range and applications along the spectrum [K. Fukunaga et al. Applied Physics, 2010]

non-invasive and can penetrate opaque materials, it can be used to characterize different materials, diverse, for instance, from those easily detected by X-ray devices.

1.1. Sub-THz/THz Applications

Due to the mentioned advantageous properties of the THz frequency range, this range is perfectly suitable for developing numerous applications. With the advancement of semiconductor technologies, many low-cost and multi-function active integrated circuit (IC)s can be implemented at mm-wave (30∼100 GHz), sub-THz (100∼300 GHz) or even above 300 GHz, which realizes the ideas and greatly enriches the applications at sub-THz/THz [**6**]. The applications can be divided into three main groups: imaging and radar, sensing and high-speed wireless and wireline communications.This section introduces some design examples to implement those popular applications at sub-THz/THz.

1.1.1. THz Imaging.

THz frequency band shows quite promising potential for imaging and radar applications. In the case of imaging, compared to lower frequency bands, such as the mm-wave band, the systems operating at THz frequencies offer finer spatial resolution as a result of the smaller wavelengths. The high-resolution imaging in visually impaired conditions is a critical and necessary capability to enable autonomous systems, and a wide variety of industrial and other applications. The high yield and ability to support a large chip area makes THz complementary metal oxide semiconductor (CMOS) technology one of the leading choices for implementing the imaging systems.

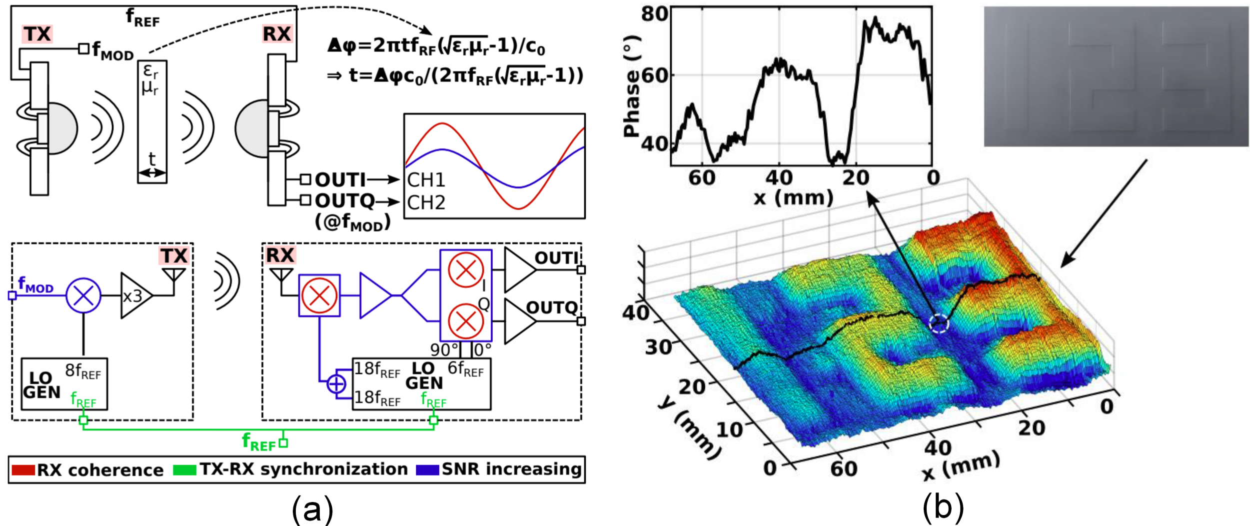


FIGURE 1.2. (a) Configuration and (b) measurements of a THz imaging system

One example is shown in Figure 1.2, which is a 420-GHz phase imaging system is designed in a 40-nm CMOS technology [**7**]. Transmitter is modulated with a low frequency sine-wave signal, while a two-way local oscillator (LO) power combining is implemented for the RX first mixer. Those techniques result in a measured transmitter effective isotropic radiated power (EIRP) of 10 dBm and receiver low noise amplifier (LNA) of 27 dB, leading to the overall signal-to-noise ratio (SNR) of 52 dB (at a distance of 25 cm and a resolution bandwidth (RBW) of 100 kHz). Furthermore, the measured phase-detection root-mean-square (RMS) precision is equal to 1.7° (on a 400° range, at a distance of 25 cm and processing time of 500 ns).

A 426-GHz concurrent transceiver imaging pixel in 65-nm CMOS that has the capability to scale and form a two-dimensional focal plane array is presented in [**8**]. The pixel integrates a transmitter, a coherent receiver using a star-type triple-push oscillator and an ON-chip patch antenna. The pixel achieves a sensitivity of -89.6 dBm for a 1-kHz bandwidth with the third order subharmonic self-oscillating mixing in RX mode. This sensitivity is the lowest for imagers operating above 300 GHz and tested under foggy weather condition.

1.1.2. THz Sensing.

Non-invasive dielectric measurement offers valuable information for material properties inspection, which has broad applications, such as medical diagnostics, drug development, environmental

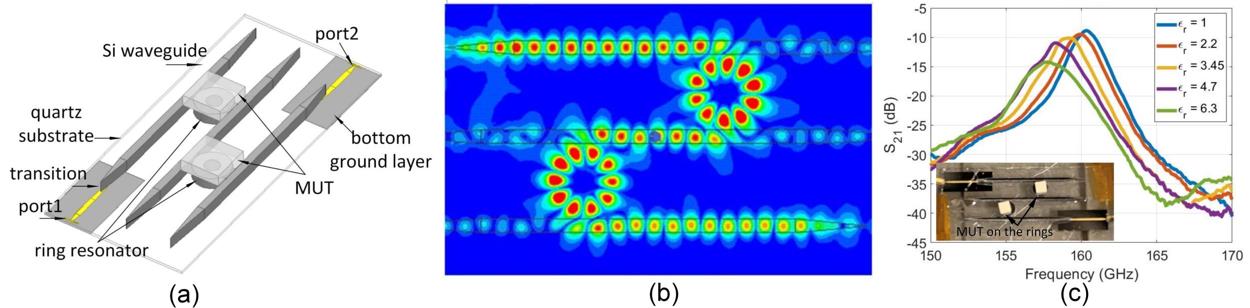


FIGURE 1.3. (a) Structure, (b) E-field distribution and (c) measurements of micro-ring based THz sensor

monitoring and food quality control. Numerous designs have been demonstrated at frequencies below 10GHz. However, for dielectric sensing at mm-Wave/Sub-THz, which have advantages of compact size and fast sensing time. Figure 1.3 introduces a high-resolution dielectric sensor at 162 GHz [**9**]. The proposed system consists of a fundamental oscillator as the transmitter, a ring resonator based dielectric sensor, and a low noise super-regenerative receiver. The active transmitter and receiver are fabricated in CMOS technologies. Due to the ring resonator's high sensitivity and receiver's ultra-low noise, the sensor can achieve the best dielectric constant sensing resolution of 3.10×10^{-4} at the frequency range above 100 GHz.

1.2. Sub-THz/THz Interconnects

According to the Shannon Theorem [**10**], channel bandwidth and attenuation constant, which determine SNR, are the key factors to determine communication systems' data capacities.

$$C = BW \times \log(1 + SNR) \tag{1.1}$$

There are two interconnect research directions, optical interconnect (OI) and electrical interconnect (EI), to address the interconnect issue. OIs [**11**] [**12**] have been investigated for several decades. The typical key component is the fiber, which has a huge bandwidth and a low insertion loss. The integration methods are studied a lot, but it is still a challenging issue and not cost effective for chip-to-chip communications. By utilizing the mature and low-cost CMOS processes, the studies of the EIs grow fast [**13**] [**14**]. However, the limitation of high insertion loss and narrow bandwidth constrains the improvements of traditional EIs [**15**] [**16**].

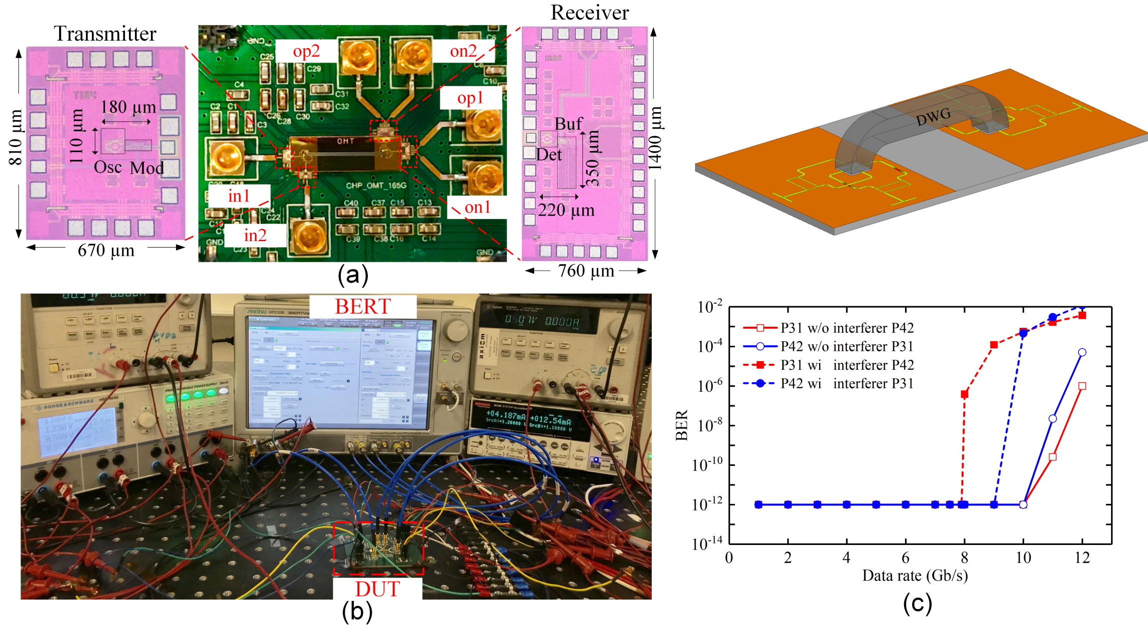


FIGURE 1.4. (a) System configuration, (b) measurement setup, (c) measured data rate and bit error rate (BER) of an ortho-mode sub-THz interconnect

Ever-increasing data generation and transmission demands inspires the researches of wireline links at mm-Wave and sub-THz/THz [**17**] [**18**] [**19**] [**20**], because mm-Wave, sub-THz/THz interconnects have broad available fractional bandwidth, low insertion loss and compact size. The other driving force comes from developments in THz materials, components, active semiconductor devices, packaging processes, and IC techniques. In [**21**], a Si dielectric waveguide (DWG) based sub-THz/THz interconnect demonstrates high potential to address the long-standing challenge to satisfy ever-increasing data rate and energy efficiency requirements by leveraging the advantages of EI and OI, especially in the most challenging meter-range scenario. The data rates of microstrip line based interconnect with 0.06-dB/mm channel loss and DWG based interconnect with 0.04-dB/mm channel loss are up to 12.2 Gb/s and 12.1 Gb/s, respectively. The highest energy efficiency and bandwidth density achieved are up to 0.32 pJ/b and 100 Gb/s/mm^2.

Single-channel interconnects at mm-wave and sub-THz/THz have been developed for years. By employing complex modulation and powerful transceivers, the channel bandwidth is fully utilized and data rate is pushed to tens of gigabits per second and quickly reaches the ceiling of speed. Researchers start to seek advanced multi-channel solutions for the interconnect. Figure 1.4 shows an

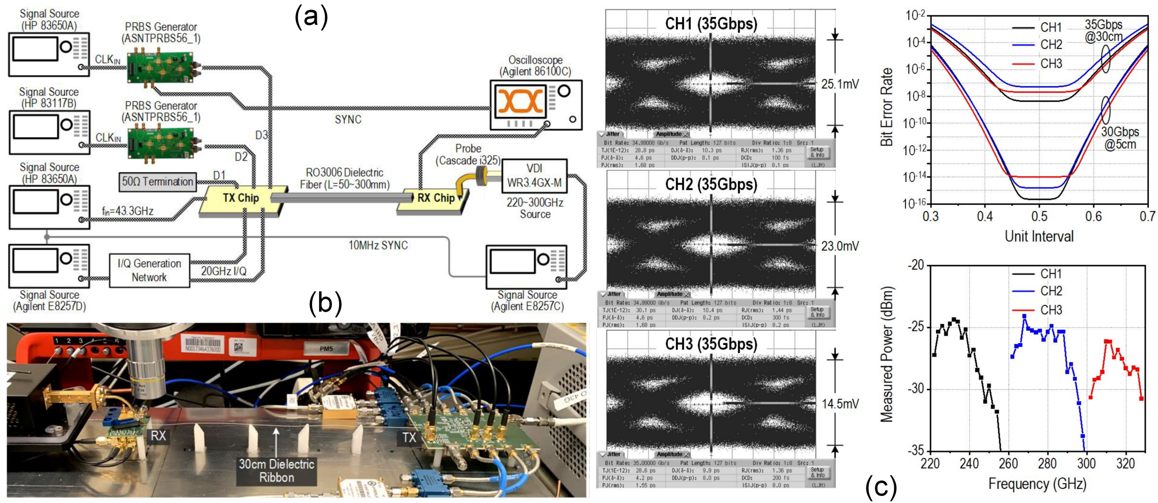


FIGURE 1.5. (a) System architecture, (b) measurement setup, (c) measured received power, data rate, eye diagrams and BER of an FDM THz Interconnect

ortho-mode sub-THz interconnect for planar chip-to-chip communications [**22**]. A novelty transition is designed to transfer quasi-TEM to E_{11}^{y} and E_{11}^{x} modes and combine them orthogonally. The measured minimum insertion losses for the E_{11}^{y} mode and E_{11}^{x} mode are 6.6 dB with 20.3-GHz 3-dB bandwidth and 6.5 dB with 55.2-GHz 3-dB bandwidth, respectively. The maximum simultaneous data rates obtained from the measurements are 8 Gb/s and 9 Gb/s, respectively.

Figure 1.5 presents a multi-channel, multiplexer/coupler-integrated transmitter that delivers a data rate of 105 Gb/s (3×35 Gb/s) using a 130-nm SiGe BiCMOS technology [**23**]. The system is an implement of frequency division multiplexing (FDM) by dividing the frequency of dielectric waveguide into bands at 220∼340 GHz. To demodulate each channel, a 35 Gb/s coupler-integrated receiver is also developed. The interconnect system, including the chipset and a 0.4 mm wide, 30cm long dielectric ribbon, experimentally demonstrates the potential speed and efficiency advantages of THz fiber links. However, the accurate off-chip local oscillator (LO) synchronization limits the total simultaneous channels and application of this architecture.

1.3. Outline of the Dissertation

This doctoral work aims to provide a comprehensive study on sub-THz/THz interconnect system in standard CMOS technologies, including passive and active, on-chip and off-chip circuits

design, communication system architectures, EM and waveguide theory, material physics, packaging and nano-manufabrication processes. According to the theoty and techniques, two Si DWG based multi-channel sub-THz interconnect systems are demonstrated to realize FDM and mode division multiplexing (MDM) shemes in this dissertation. The measured data rate, BER and energy efficiency prove the successful implements of the proposed sub-THz interconnect communication architectures.

Chapter 2 portrays the passive and active most commonly used in the sub-THz/THz CMOS circuits. Section 2.1 presents on-chip and off-chip passives in a frequency range from baseband to sub-THz. Section 2.2 introduces actives in CMOS devices including transistor modeling, layout optimization, neutralization and so on. Section 2.3 of this chapter presents the coherent and non-coherent detection for commercial communication systems. The elements in both non-coherent and coherent detection are discussed, and several design techniques are introduced to optimize sub-THz/THz blocks in standard CMOS technologies. Section 2.4 introduces multiplexing schemes, besides the traditional FDM, time division multiplexing (TDM), quadrature division multiplexing and more advanced spatial multiplexers are designed.

Chapter 3 percents a full-duplex sub-THz interconnect system based on FDM scheme. The system consists of a dual-band transmitter, receiver, and a DWG-based channel that provides low in-band insertion loss and high isolation for the adjacent band. Section 3.1 starts with the FDM Si DWG channel design. Section 3.2 analysis the system-level consideration and component selection based on the power link budget and bandwidth budget. Section 3.3 and 3.4 elaborate the tranmiter and receiver design. Section 3.5 introduces the system implement including fabrication and packaging. At last, Section 3.6 discusses the measurement setup and compares the results with the State-of-the-Art (SOA)s

Chapter 4 proposes a mode-coupler based multi-drop Si DWG with MSL-to-DWG transitions on quartz boards, and theoretical analyzes and explains the design DWG mode coupler. Many analysis methods and solutions, such as bandwidth analysis and taper analysis with light ray tracing method, are firstly proposed. Section 4.1 drives the eigen modes in rectangular dielectric waveguides; Section 4.2 analyzes the waveguide mode directional coupler design, including mode coupling

condition, coupling coefficient extraction, coupling efficiency maximization and verification. Section 4.3 introduce all the detailed building structures and the mechanism behind them. Section 4.4 shows the fabrication and measurement results of the multi-drop Si DWG channel.

Chapter 5 demonstrates a multi-drop sub-THz interconnect system based on the multi-drop Si DWG channel designed in the Chapter 4. the system aims to achieve more than 60 Gb/s data rate (20 Gb/s per channel). Therefore, the system architecture is investigated again and modified to improve the bandwidth and sensitivity of the receiver. Section 5.2 and 5.3 improve the transmitter and receiver by adopting broadband modulator, LNA and CTLE. Section 5.4 presents the package design and fabrication and replace all bonding wires with flip-chip bumps in RF signal chain. In section 5.5, the multi-drop data rates are 24 Gb/s, 22 Gb/s and 19 Gb/s for E_{11}^{y}, E_{21}^{y} and E_{21}^{y} modes, respectively with the BER better than 10-12. The demonstrated aggregate data rate of the three channels is 65 Gb/s with the energy efficiency of 1.6 pJ/b.

Chapter 6 will summarize the techniques and designs in this dissertation, then proposed the technical trend and research direction in this field based on the author's understanding.

CHAPTER 2

Key Blocks and Techniques for Sub-THz/THz Interconnect

In sub-THz/THz integrated circuits and systems, any of the technique schemes or components would be the bottleneck of the overall performance if it hasn't been fully investigated and properly designed. As the scaling of modern CMOS technologies and advance of EDA tools, many novel components at mm-Wave and THz were implemented in the past years [2-5], but there are still plenty of different engineering possibilities when designing sub-THz/THz systems. The proposed sub-THz/THz interconnects employ a bunch of on-chip and off-chip, passive and active components. To achieve a high speed and high energy-efficiency performance, thorough analysis and understanding of those techniques and components are crucial for a successful system level design. This chapter investigates communication solutions, summaries TX and RX architectures, analysis critical passive and active components, introduces optimized circuit typologies, and compare their advantages and disadvantages.

Section 2.1 presents on-chip and off-chip passives in a frequency range from baseband to sub-THz. Section 2.2 introduces actives in CMOS including transistor modeling, layout optimization and neutralization. Section 2.3 of this chapter presents the coherent and non-coherent detection in commercial communication systems. The elements in both directions are proposed and several design techniques are introduced to optimize mm-wave and THz blocks in standard CMOS technologies. Section 2.4 introduces multiplexing schemes, besides the traditional frequency division multiplexing (FDM), time division multiplexing (TDM) and quadrature division multiplexing, more advanced spatial multiplexers are designed.

2.1. Passive Components

Passive components are an essential part of every RF, mm-wave/THz integrated circuit. Almost all the circuits need passive components to form matching networks, resonators, reflectors, radiation structures, filters, and interface between circuit elements. As the frequency increases, the modeling

of passives requires strict procedure and accurate extraction due to the increasing parasitic effects. The passives used in sub-THz/THz interconnects are divided into two groups: off-chip and on-chip.

Off-chip passive components have relatively large size due to the fabrication process constrain. The feature size on PCB is 4 mil ($\approx$ 101.6 μm) and tolerance of in-house fabrication process is about ± 0.5 μm. Besides the precision, large-size components with very pronounced distributed and parasitic effects at high frequency leads to dramatic performance degradation. That is the reason why sub-THz/THz components are mostly implemented on chips or on a substrate fabricated in-house, meanwhile, baseband signal traces, interfaces, and DC supply routing are designed on PCB or fabricated substrates.

On-chip passives has much smaller feature size and more accurate fabrication process in nanometer level. However, advanced CMOS technologies have very strict metal density requirement, which is rarely met by RF passive components, such as, transmission line, inductor, antenna etc. Too dense dummy fills decrease their quality factor (Q), defined Eqn. (2.1), thus a trade-off is necessary. All the off-chip or on-chip passive components for different purposes are analyzed and simulated in the corresponding frequency range.

$$Q = 2\pi \frac{energy\ stored}{average\ power\ dissipated} \tag{2.1}$$

2.1.1. Off-chip Passives Components.

In sub-THz/THz interconnect system, baseband signal (DC$\sim$ up to 30 GHz) travels through traces on PCB, thin substrates (e.g., Benzocyclobutene (BCB), quartz), while sub-THz signal (100$\sim$200 GHz) travels through components on thin substrates and CMOS chips. The signal traces and interfaces are required to well designed to minimize the path loss and reflection.

(1) Transmission line

Transmission lines are the most common used components to transmit RF, mm-wave and THz signals between blocks in a short distance but non-negligible to the signal wavelength. They also can be matching networks to convert impedance, resonators to form filters, coupling and radiation structures to conduct signal transportation wirelessly. Figure 2.1 presents different types of transmission lines: (a) microstrip line, (b) strip line (c) coplanar waveguide (CPW), (d) grounded coplanar waveguide (CPWG), (e) differential line, (f) grounded differential line, (g) slot line and

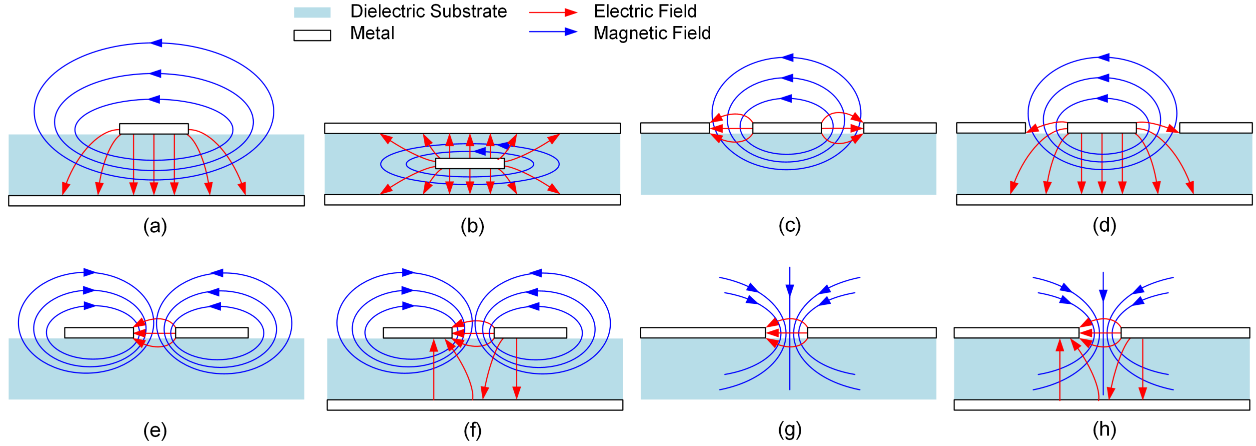


FIGURE 2.1. Different types of transmission lines: (a) microstrip Line, (b) strip line, (c) CPW, (d) CPWG, (e) differential line, (f) grounded differential line, (g) slot line and (h) grounded slot line

(h) grounded slot line with their corresponding E field and H field vectors. The transmission line selection is made based on the operation frequency, electric properties of dielectric substrate and fabrication tolerance. In term of fabrication consideration, it is difficult to deposit an internal metal layer or build a metalized through-substrate via (TSV) on thin substrates, such as a 100-μm quartz substrate, thus strip line or microstrip line with DC-coupled ground-signal-ground (GSG) interface that needs TSV is challenging to realize on quartz with an in-house fabrication process. The analysis and comparison of trace's performance will be conducted in the next subsection.

A transmission line is often schematically represented as a two-wire line since transmission lines always have at least two conductors, which can support transverse electromagnetic (TEM) or quasi-TEM wave propagation. The model of a transmission line cascaded by pieces of line with infinitesimal length, and each section can be modeled as a lumped-element circuit constructed by R, L, G and C that are per-unit-length series resistance, series inductance, shunt conductance and shunt capacitance, respectively [**24**].

The telegrapher equations of current and voltage in time domain can be derived from Kirchhoff's voltage law, and represented with per-unit-length lumped-element. Then a function of frequency for traveling wave is obtained with a complex propagation constant γ that is given by

$$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)} \tag{2.2}$$

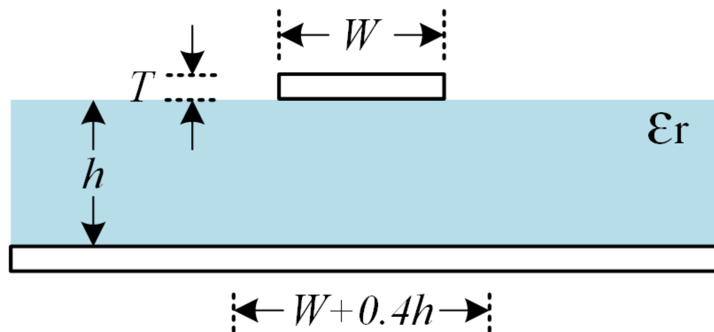


FIGURE 2.2. Cross-section configuration of a microstrip line

where α attenuation constant and β phase propagation constant. And the characteristic impedance Z_0 of a transmission line is calculated in Eqn. (2.3).

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{2.3}$$

The characteristics of a transmission line are determined by lumped-element circuit parameters that are related to the geometry (e.g., width and thickness of conductor, thickness of dielectric substrate) and electric properties (e.g., conductivity, permittivity).

Microstrip line is a good example to start with. In Figure 2.2, a microstrip line consists of a conductor of width W, a dielectric substrate of thickness T and permittivity ε_r. The presence of the dielectric substrate (commonly thickness $h \ll \lambda$) concentrates the field lines in the region between the between the conductor and the ground plane. There are many approximation equations in terms of W/h and ε_r to calculate the characteristic impedance Z_0. Ansys HFSS and Keysight ADS Linecalc taking parameters like frequency and conductor thickness T into account are suggested for a more accurate Z_0.

The loss of a transmission line comes from conductor loss, dielectric loss, radiation loss and magnetic loss if magnetic materials, such as ferrite or garnet, exist in the element. The conductivity of the metal, the skin effect, and surface roughness affect conductor loss in microstrip lines. Microstrip lines will experience more ohmic loss with reduced conductivity. The loss tangent of dielectric substrate drives the dielectric loss. Normally, dielectric loss is directly proportional to frequency. In CMOS integrated circuits, dielectric and conductor loss is almost equal due to lower resistivity of

silicon substrates. To the contrast, III-V compound semiconductor using high-resistivity GaAs or GaN as the substrate has lower dielectric loss. Designers need to pay high attention to the loss introduced by current return path on an extremely thin ground plane, which usually happens in advanced CMOS technologies. For a lossless transmission line, we can simply set $R = G = 0$ and propagation constant becomes

$$\gamma = j\omega\sqrt{LC} \tag{2.4}$$

and

$$\begin{cases} \alpha = 0 \\ \beta = \omega\sqrt{LC} \end{cases} \tag{2.5}$$

Microstrip line has operating frequency limitation. The higher-order microstrip mode above the quasi-TEM mode, which is similar to TE mode in parallel plates, occurs when there is a half-sinusoidal variation of the electric field between the strip and the ground plane, and the first higher-order microstrip mode can exist at frequency as low as Eqn. (2.6) [**25**]. Therefore, thinner substrate ($h \ll \lambda$) and lower dielectric constant substrate is preferred for high-frequency designs, because it has higher cutoff frequency that avoids higher-order mode excitation.

$$f_{cutoff} = \frac{c}{4h\sqrt{\varepsilon_r - 1}} \tag{2.6}$$

The grounded strip structures with underneath ground planes, e.g. CPWG, grounded differential line and grounded slot line as shown in Figure 2.1, have the same problem. On the other hand, CPW, differential line and slot line are able to operate at high frequency, which will be discussed and compared in the GSG-type interface subsection.

(2) GSG-type interface

Beside the fabrication complexity, the feature and performance is the most important criteria when selecting an interface. For a complex RF system, designers must consider probing capability of the components since all the blocks must be tested to ensure the correct specification and port impedance before they are cascaded in the signal chain. Microwave probing is a standard and reliable method to evaluate the performance of RF components. Commercial 100-μm pitch GSG probes can cover the frequency range from DC to THz and verify components accurately after

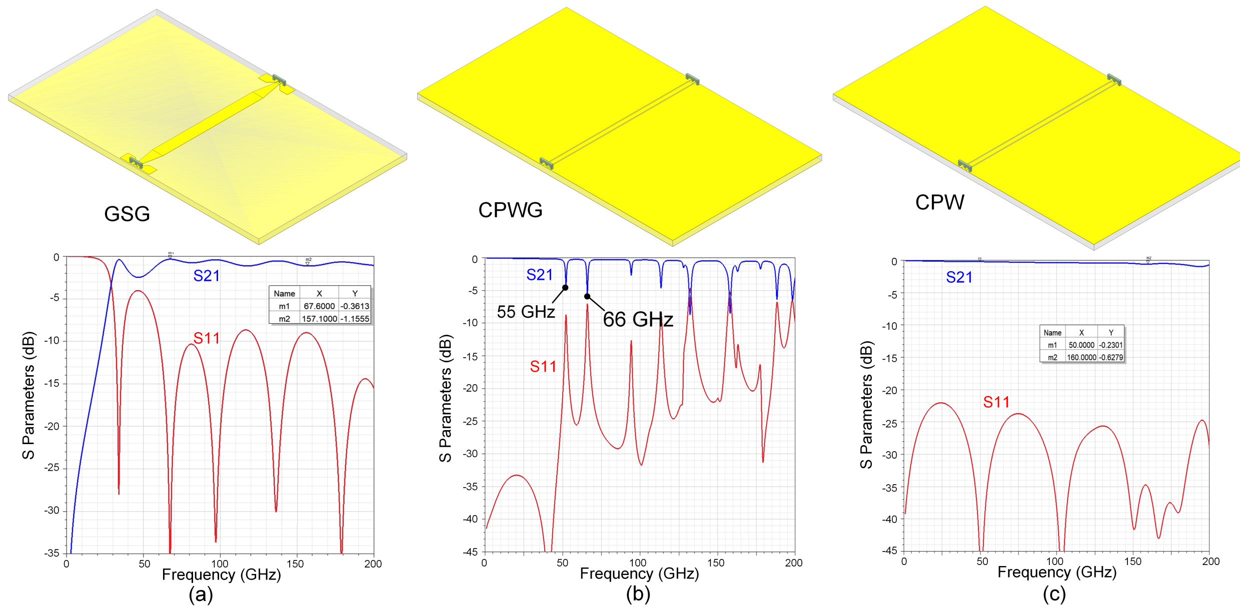


FIGURE 2.3. Typical microstrip-lines on thin substrates (quartz): (a) microstrip-line with AC-coupled GSG, (b) CPWG and (c) CPW

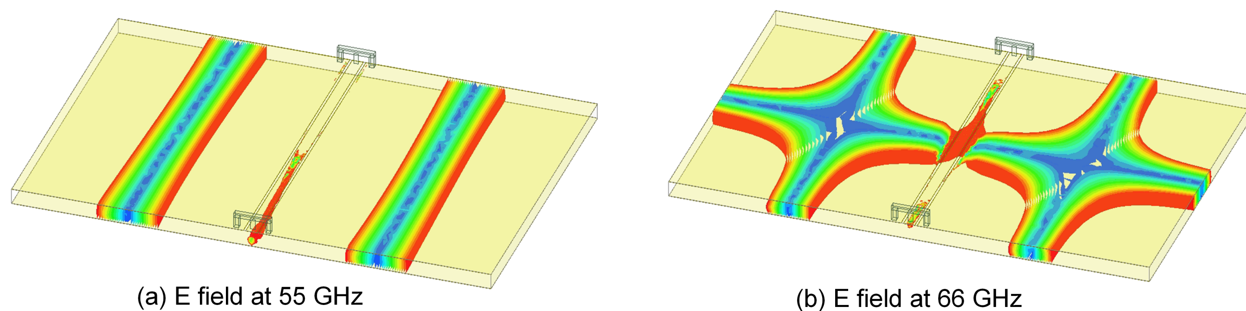


FIGURE 2.4. (a) First-order transverse mode at 55 GHz and (b) second-order transverse mode at 66 GHz in a CPWG configuration

calibration and de-embedding. GSG interface is a transition from CPW to microstrip line, as shown in Figure 2.3. It also a good choice for system integration with wire bonding or flip bonding, because it extends the CPW structure and reduces the inductance brought in by wire connection that could be significantly detrimental to the impedance matching at sub-THz/THz.

There are four types of interfaces employed in the sub-THz/THz interconnect and optimized for the signals at the different frequency. As mentioned before, baseband data has a bandwidth up to 25 GHz and travels through PCB and thin substrate. According to Figure 2.3 (b) and (c), both

Table 2.1. Comparison of the probe testable interfaces.

	GSG on-Quartz	**CPWG on-Quartz**	**CPW on-Quartz**	**CPWG on-Chip**
Dominant GND	Bottom layer	Top layer	Top layer	Bottom layer
TSV	No	No	No	Yes
AC/DC Coupled	AC	DC	DC	DC
Freq. Response	Band-pass	Low-pass	Low-pass	Low-pass
Bandwidth	100∼200 GHz	DC∼50 GHz	DC∼200 GHz	DC∼400 GHz
Cons.	Band-pass and ripples	Higher-order transverse mode	No shielding on bottom	Hard fabrication
Pros.	Easy routing	Shielding on bottom	Easy fabrication and broadband	Broadband

CPWG and CPW have low-pass features and can satisfy the baseband requirement. CPW has very good matching performance with a bandwidth up to 200 GHz, but it lack of a shielding layer that is necessary for high-quality RF signals. To contrast, CPWG with a shielding metal layer underneath can protect the signal from complex EM environment. However, higher-order transverse modes occur, as shown in Figure 2.4, when the wavelength is considerable to the substrate thickness. The bandwidth of CPWG needs to be verified before it is adopted in the system. GSG cascaded with microstrip line is another option, and it is very convenient to connect to any microstrip-type circuits such as microstrip to DWG transition. Figure 2.3 (a) shows an AC-coupled GSG of a band-pass frequency response. Although the matching is not as good as CPW, GSG can meet the requirement for the sub-THz signal at 100 $\sim$ 200 GHz. For standard CMOS technology, through-substrate via (TSV) is available and DC-coupled GSG expands the bandwidth from DC to 400 GHz due to the precise and nanometer level feature size. The characteristics of off-chip and on-chip interfaces are compared in Table 2.1.

2.1.2. On-chip Passives Components.

Standard semiconductor technology provides scalable parameterized cell (PCell) of lumped components (e.g., resistors, capacitors, and inductors), including schematic, layout, and RF models in the PDK. The RF models are usually built below 20 GHz by fitting the measurements, which is inaccurate at mm-wave and THz. Designers should create their own passive libraries and model

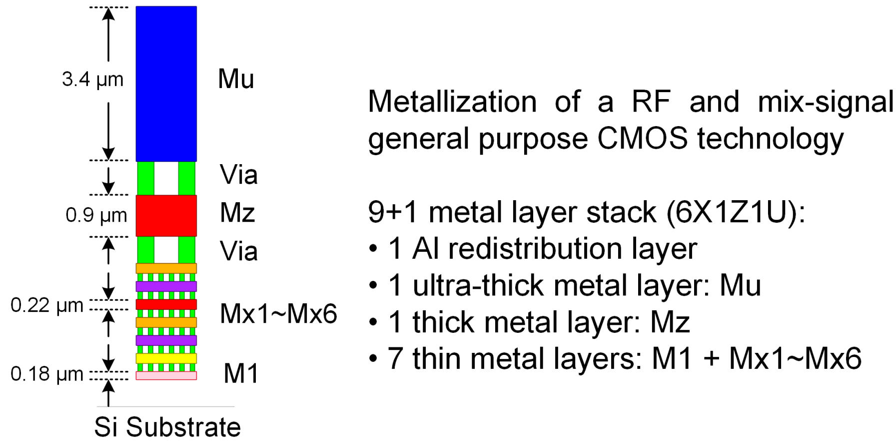


FIGURE 2.5. Metallization of a RF and mix-signal purpose CMOS technology.

the lumped and distributed components at the desired operation frequency, because lumped components like capacitors and inductors, and distributed components like transformers, CPW and slot-line, are widely used for matching and interconnection in RF integrated circuits, especially at mm-wave and THz. Their characteristics and modeling accuracy are as crucial as active circuits and architecture to the system. Metallization is the process by which the components are interconnected by aluminum conductor. This process produces a thin-film metal layers that serve as the required conductor pattern for the interconnection of the various components on the chip and metallization layers are connected through vias, as shown in Figure 2.5. In RF purpose CMOS technologies, there are one or more high-Q thick metal layers available for RF path routing. The electrical properties to the semiconductor physics and process are not the key points of this thesis. Therefore, this subsection focuses on their characteristics, modeling, and design strategies.

(1) Resistor

There are a few types of resistors in standard CMOS technologies: polysilicon (known as poly), source-drain diffusion, wells and MOS transistor.

The resistivity of poly resistors tends to be $5 \sim 10\ \Omega$ per square, so poly is appropriate small-valued resistors. It often has a poor tolerance of 35% and a moderate temperature coefficient (TC) that is defined as Eqn. (2.7), and it depends on doping and composition and is typically about 1000 $ppm/^{\circ}C$ [**26**]. In addition, poly resistors have a reasonably low parasitic capacitance per unit area and the lowest voltage coefficient of all the resistor materials available in a standard CMOS

technology.

$$TC = \frac{1}{R}\frac{\partial R}{\partial T} \tag{2.7}$$

Resistors made from source-drain diffusion is another option. The resistivities and TC are generally similar to poly resistors with lower TC associated with heavier doping. However, there is significant parasitic capacitance as well as a noticeable voltage coefficient. The parasitic capacitance limits the application at high frequency range, while voltage dependency limits the dynamic range of voltages that may be applied on the resistor and introduces significant distortion. Additionally, source-drain diffusion resistor must avoid forward-biasing. All these characteristics limit the use of diffused resistors.

Wells could be used for high-value resistors, since resistivities are typically in the range of $1 \sim 10\ k\Omega$ per square. Nevertheless, well resistor must be used with care, because of the substantial parasitic capacitance formed by the large-area junction between the well and substrate, poor tolerance ($\pm 50 \sim 80\%$), large TC ($3000 \sim 5000\ ppm/^{\circ}C$, owing to the light doping), and large voltage coefficient.

MOS transistor can be used as a variable resistor with a tunable gate-to-source voltage. According to the first-order theory, recall that the resistance of MOS transistor in the triode region is represented by

$$r_{ds} = \left\{\mu C_{ox}\frac{W}{L}[(V_{GS} - V_T) - V_{DS}]\right\}^{-1} \tag{2.8}$$

At sub-THz/THz, on-chip resistors have limited application. Normally, poly resistor with less parasitic and voltage dependency is preferred. The RCC model can be extracted Clibre tool by counting the squares, but the variation of resistance needs to be considered especially in a circuit that is sensitive to the renaissance. The other types of resistors could be selected carefully, and it is highly relying on design experience.

(2) Capacitor

Capacitors have numerous application scenarios in RF, mm-wave and THz circuits: it can be a DC block in the signal path, and the bypass capacitor in biasing/supply path to minimize noise and eliminate possible ringing and circuit instability; it also can be used to form matching networks

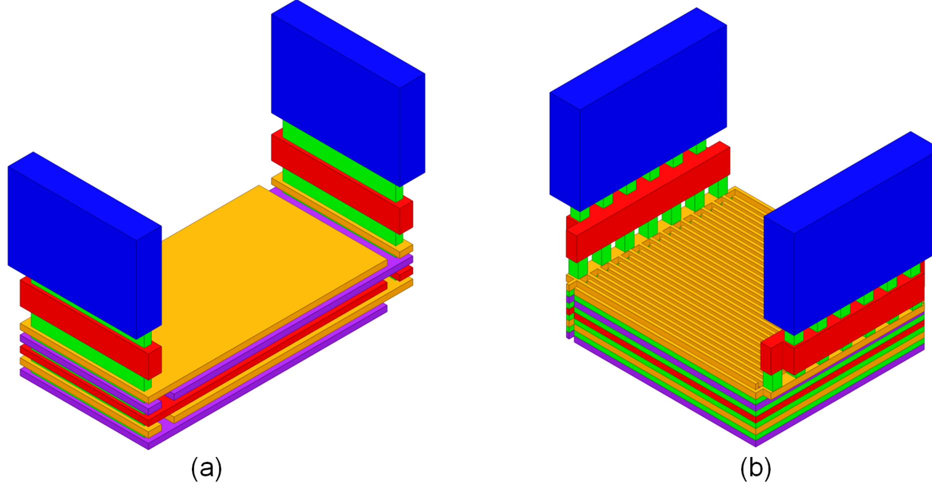


FIGURE 2.6. MOM capacitors: (a) parallel-plate capacitor and (b) multi-finger capacitor.

and resonators; another scenario is in neutralization or embedding networks, which is a helpful approach to boost the maximum available gain G_{ma} of a transistor.

The accurate parasitic extraction of the designed capacitor is usually done using EM solvers (e.g., HFSS, CST and ADS momentum) or Cadence Calibre by counting the overlapped area of metals. For pure passive capacitor (except MOS capacitor), EM solvers like HFSS are preferred at sub-THz/THz for accurate parasitic extraction. Then, capacitance and Q are calculated based on the obtained S-parameters, according to the Eqn. (2.9) and (2.10). Due to the influence of the parasitic, mostly inductance, the obtained capacitance and Q values are frequency dependent, and the self-resonate frequency is finite.

$$C = \frac{1}{z\pi f Im(Z_{11})} \tag{2.9}$$

$$Q_{cap} = \frac{Im(Z_{11})}{Re(Z_{11})} \tag{2.10}$$

where Z_{11} is the simulated impedance of the capacitor.

MOM capacitors are fully implemented in CMOS chips, using horizontal or vertical overlapping between metal layers. Those metals can be arranged in different ways, where the two most common ways are parallel-plate capacitors and multi-finger capacitors and, as shown in Figure 2.6. Parallel-plate and multi-finger capacitors of the same capacitance value have very similar Q and

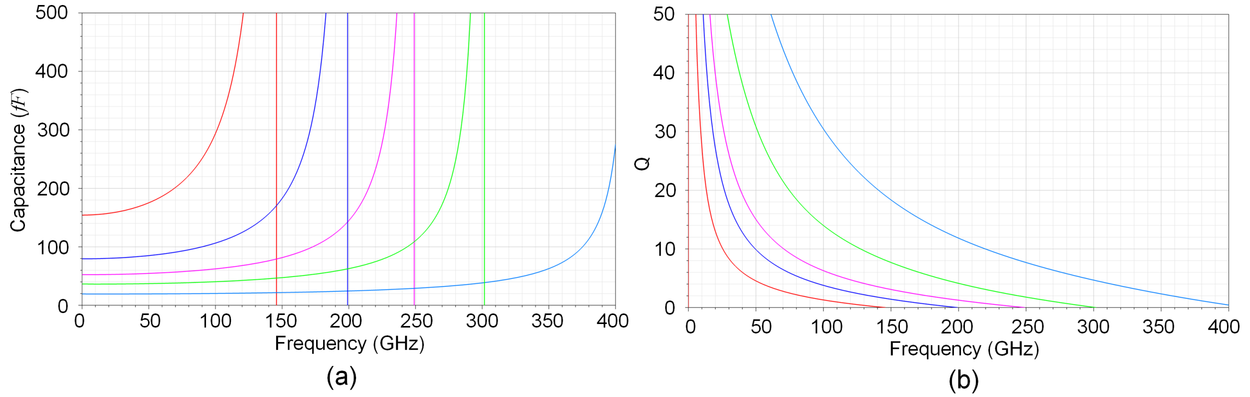


FIGURE 2.7. Simulated (a) capacitance and (b) Q factor for MOM capacitors in variant size

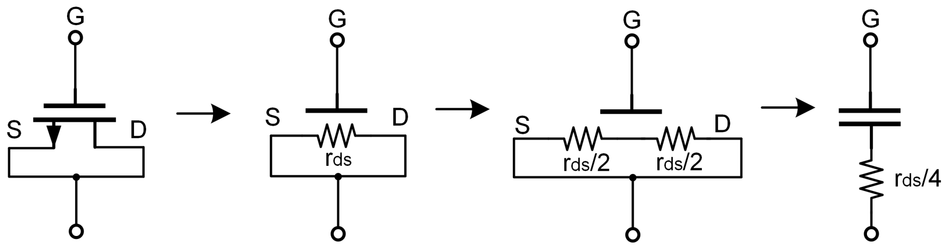


FIGURE 2.8. MOS capacitor configuration and modeling

self-resonance frequency, but both Q and self-resonance frequency declines quickly as the capacitance or frequency increases, as depicted in Figure 2.7, which compares the capacitance and Q of MOM capacitors in different sizes in a frequency range from DC to 400 GHz. Large capacitors ($\geq 50\ fF$) are barely employed in the designs above 100 GHz due to the low Q and self-resonance frequency. The advantage of the multi-finger capacitor is with a higher capacitance density, which leads to a more compact size. In contrast, the parallel-plate capacitor is easier for modeling and can be simulated in a shorter period.

MIM capacitors use a special, thin, high permittivity dielectric layer, which allows them to achieve a higher Q, higher self-resonance frequency, and higher capacitance density compared to MOM capacitors. However, their disadvantage is a requirement of additional process steps and usually come with a higher cost.

MOS capacitors are available in standard CMOS and some BiCMOS processes. The gate and channel are separated by a thin layer of SiO_2, therefore, they form a capacitance that varies along

with gate voltage when the gate-source voltage is above the threshold. It is controlled by the input gate to source voltage and hence, acts like a voltage-controlled variable capacitor (varactor). When using a gate capacitor in a CMOS process, it is important to keep the transistor in strong inversion ($V_{GS} \geq V_{th}$); otherwise, the capacitance will be small, lossy, and highly nonlinear. For gate capacitors, the Q depends on the channel resistance, as modeled in Figure 2.8. The model identifies the maximum resistance from the center of the channel to the source-drain connection and puts that worst-case value in series with all the capacitance, and correctly predicts that the way to Q should use the minimum allowable device length to minimize r_{ds} for a given bias.

(3) Inductor

Similar to capacitors, inductors are an essential part of mm-wave and sub-THz/THz systems. In signal chains, they are primarily used as part of resonators and matching networks; in the basing and supply paths, they are often used as DC chokes, creating high impedance for RF signals. Inductors are designed using EM simulation tools, where inductance value is extracted from obtained S-parameters using Eqn. (2.11). The most common performance metrics of inductors are self-resonance frequency and Q-factor, as defined in Eqn. (2.12). The definition is consist with the Q-factor in Eqn. (2.1) that the total stored energy divided by the average dissipated power in a passive component.

$$L = \frac{Im(Z_{11})}{z\pi f} \tag{2.11}$$

$$Q_{ind} = \frac{Im(Z_{11})}{Re(Z_{11})} \tag{2.12}$$

where Z_{11} is the simulated impedance of the inductor.

If expanding this concept to a LC tank that consists of an inductor and capacitor and resonates at f_0, the Q is related to its 3-dB bandwidth (BW) as calculated in the expression below.

$$Q = \frac{f_0}{BW} \tag{2.13}$$

Parasitic capacitances between the inductor and shield, which is the physical reason for self-resonance frequency of an inductor. The simulated inductance, self-resonance frequency and Q of the inductor in a diameter of 50-μm are plotted in Figure 2.9, and the self-resonance frequency is around 200 GHz and inductance is about 100 pH that might be the maximum on-chip inductance

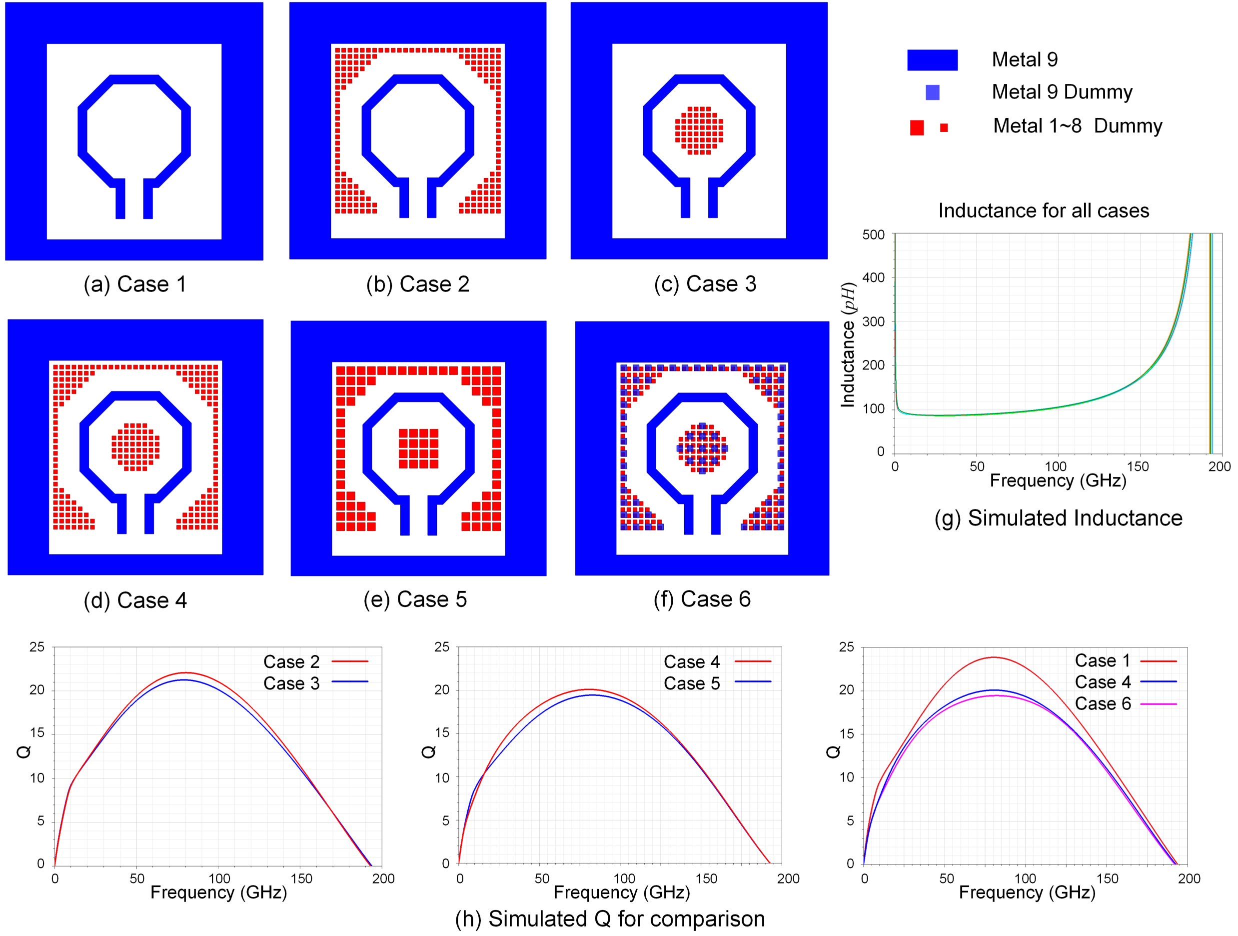


FIGURE 2.9. Inductor (a) without dummy fills, (b) with external dummy fills, (c) with internal dummy fills, (d) with both external and internal dummy fills, (e) with larger internal dummy fills and (f) with all layer (including M9) dummy fills. (g) Simulated inductance, self-resonance frequency and (h) Q-factor for all cases.

available at sub-THz/THz, because larger physical area makes parasitic effects more pronounced and leads to lower self-resonance frequency. The optimum Q is obtained at half of the self-resonance frequency (∼100 GHz). The coil size has to be reduced if selecting a higher operation frequency, and the obtained inductance value decreases accordingly.

When talking about Q-factor or inductor loss, there are two main physical reasons: metal resistance and substrate loss. Metal resistance increases approximately with the square root of frequency due to the skin effect and the current crowding effect. To optimize the metal loss the inductor should be designed in the thickest possible metal layers. As shown in Figure 2.5, Mu (M9)

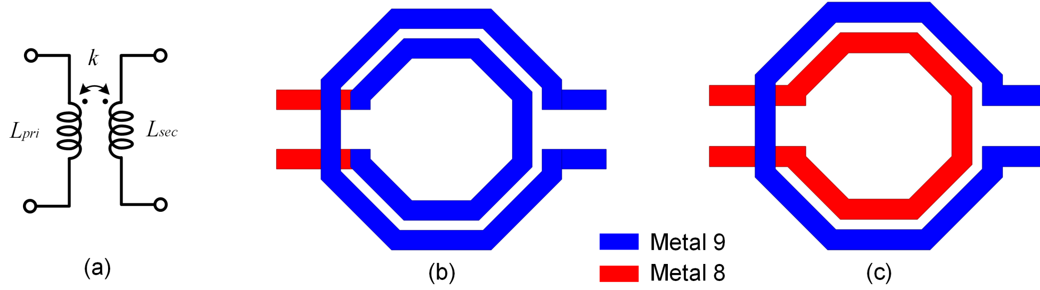


FIGURE 2.10. (a) Schematic and layout of transformers (b) on Metal 9; (c) on Metal 8 and Metal 9.

in a thickness of 3.4 μm and Mz (M8) in a thickness of 0.9 μm are optimized especially for the RF components that need low loss and high-Q. Another irresistible factor affecting inductor loss is dummy fills due to the strict metal density requirement in advanced CMOS processes. Figure 2.9 also illuminates the inductor with different dummy filling strategies and their performance comparison. There are six different dummy fill cases shown in Figure 2.9 (a)$\sim$(f). All of them have similar inductance and resonate frequency as shown in Figure 2.9 (g). The optimum dummy filling could be selected by comparing their Q-factor in Figure 2.9 (h): the one without any dummy fills definitely has the highest Q, but it is not allowed in the CMOS technologies; By comparing case 2 and 3, the internal dummy fills have higher impact on the Q than the outside ones; Smaller size dummy is preferred if comparing the case 4 and 5 with small and large pieces of dummy; The dummy on the same altitude that is closest to the inductor has more influence than other layers, which is concluded from the case 4 and 6. This dummy filling strategy also applies to the other passive components, such as transmission lines and transformers.

(4) Transformer

Transformer is another important passive component in mm-wave and sub-THz/THz CMOS ICs. They are majorly utilized in matching networks, baluns, power combiners, power splitters, and so on. A two-coil transformer can be modeled similarly to inductors, as shown in Figure 2.10 (a). Electric and magnetic coupling form between the coils when they are approaching to each other, and the magnetic (inductive) coupling could the dominant one for the cases in Figure 2.10 (b) and (c), because the magnetic field is fully overlapped compared to the conductor area overlapping that forms the electric (capacitive) coupling. L_{pri} and L_{sec} are inductance in the primary and secondary

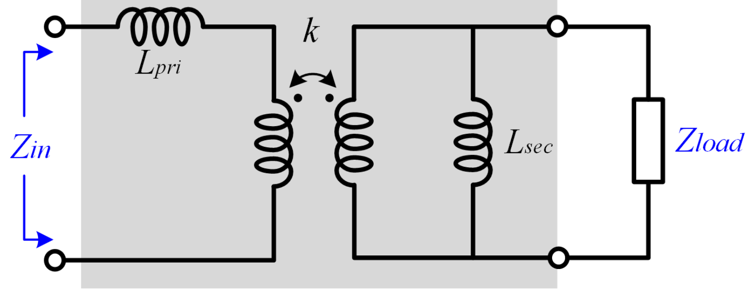


FIGURE 2.11. Lumped element model of a transformer.

coils, respectively, and they are defined in Eqn. (2.14) and (2.15), which is similar as the inductance expression.

$$L_{pri} = \frac{Im(Z_{11})}{z\pi f} \tag{2.14}$$

$$L_{sec} = \frac{Im(Z_{22})}{z\pi f} \tag{2.15}$$

k is the coupling factor or coupling coefficient, defined Eqn. (2.17) that is the mutual inductance M in Eqn. (2.16) over the square root of the product of L_{pri} and L_{sec}. The mutual inductance that exists between the two coils can be greatly increased by increasing the number of turns of either coil in a transformer. The coils of the transformer can be conducted on the same layer (Metal 9) or different layers (Metal 8 and Metal 9). The one of both coils on the same layer has limited coupling coefficient (typically 0.2 $\sim$ 0.5), because of the weak edge coupling and constrained distance, on the other hand,it could achieve the highest Q if the coils are on the thickest metal layers (such as Metal 9). The coupling coefficient can be dramatically increased (up to 0.7) when the two coils on the adjacent layers (such as Metal 8 and Metal 9) are perfectly overlapped.

$$M = \frac{Im(Z_{21})}{z\pi f} \tag{2.16}$$

$$k = \frac{M}{\sqrt{L_{pri} \cdot L_{sec}}} \tag{2.17}$$

The last parameter of a transformer is turning ratio, definded in Eqn. (2.18), which is critical to the impedance conversion in a matching network.

$$TR = \frac{\sqrt{L_{sec}}}{\sqrt{L_{pri}}} \tag{2.18}$$

The model of a transformer can be simplified to an ideal coupling model and external primary inductance L_{pri} and secondary inductance L_{sec}, as shown in Figure 2.11. The transfer impedance Z_{in} can be calculated by Eqn. (2.19). In reality, there are parasitic resistors determining the Q-factor, and capacitors affecting the self-resonance frequency and electric coupling in a transformer. The simplified model can not represent a real transformer any more. To extract accurate models, transformers are also designed using EM simulation tools same as capacitors and inductors.

$$Z_{in} = \frac{k^2}{TR^2} Re(Z_{load}//sL_{sec}) + j\left[\frac{k^2}{TR^2} Im(Z_{load}//sL_{sec}) + sL_{pri}\right] \quad (2.19)$$

2.2. Active Components in CMOS

Besides the passive components discussed in the last section, the active components also make an essential part of the sub-THz/THz interconnect systems. Similar to the passives at sub-THz/THz, their active design and modeling need to be done with special care to accurately predict circuit behavior and achieve optimal circuit performance due to the high operation frequency. Therefore, a large afford is spent on actives modeling, and schematic, layout optimizations and post-simulation when designing a sub-THz/THz circuit.

Firstly, the semiconductor technologies capable for sub-THz/THz designs are compared. Secondly, CMOS transistor modeling and parameters with fundamental schematic and layout level optimization techniques for operation in mm-wave and THz frequency bands are presented. Then, two methods for transistor's gain boosting is introduced introducing stability and power gain definitions and circuit typologies.

2.2.1. Semiconductor Technologies for sub-THz/THz designs.

The selection for semiconductor technologies needs to be made specific to application and operation frequency. For example, internet of things (IoT) applications requiring significant portion of logic and lower-power operations, a bulk CMOS technology that is suit for an integrated solution with high density and low-cost. For high performance RF, mm-wave front-end and sub-THz/THz designs, CMOS technologies appear constrains due to the relative low transconductance g_m. For very large scale integration (VLSI), large-scale digital IC and system on chip (SOC), high density, low-power and low-cost CMOS is the best choice. The comparison among the state-of-the-art

Table 2.2. Comparisons of Semiconductor Technologies for RFIC.

	Si CMOS	**SiGe HBT**	**Si BJT**	**III-V MESFET**	**III-V HBT**	**III-V HEMT**
Freq. resp.	Good	Very good	Good	Very good	Excellent	Excellent
Phase noise	Fair	Excellent	Very good	Poor	Good	Poor
BW Noise	Good	Very good	Good	Very good	Very good	Excellent
Linearity	Very good	Very good	Very good	Excellent	Very good	Excellent
g_m**/area**	Poor	Excellent	Excellent	Fair	Excellent	Fair
Power	Fair	Excellent	Very good	Fair	Very good	Good
Integration	Excellent	Excellent	Excellent	Poor	Poor	Poor
IC cost	Very good	Good	Good	Fair	Fair	Poor

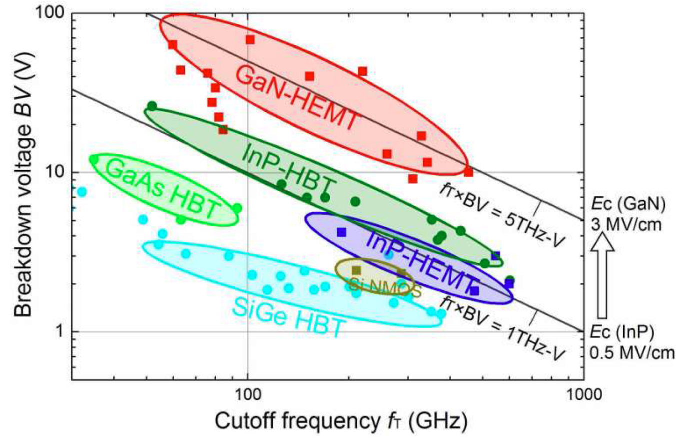


Figure 2.12. Breakdown voltage and f_T of standard semiconductor technologies [J. Zhang et al., SiRF, 2020]

semiconductor technologies, including RF CMOS, SiGe BiCMOS, and III-V compound technologies are summarized in Table 2.2.

This performance comparison in the breakdown voltage vs. f_T trade-off curves are also plotted in Figure 2.12 [**27**]. III-V compound technologies usually are superior compared to silicon-based technologies. For sub-THz/THz, ultra-wide band, high power, or mission-critical applications, III-V technologies, especially indium phosphide (InP) and heterojunction bipolar transistor (HBT), are undoubtedly favored for their device RF characteristics. Though falling behind in device performance, SiGe BiCMOS and RF CMOS technologies outshine III-V technologies from low power, low cost, high yield, and high-level integration [**28**]. As a result, there has been increasing interests in advanced RF CMOS and SiGe BiCMOS technologies as potential candidates for sub-THz/THz applications.

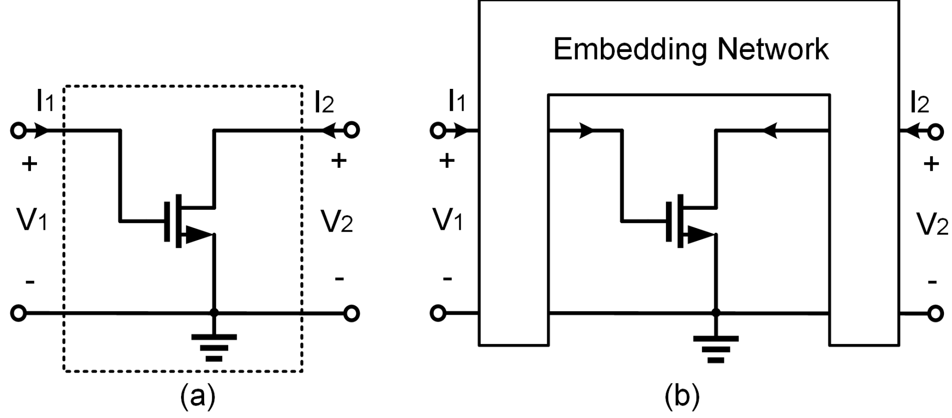


FIGURE 2.13. (a) Schematics of a transistor and (b) embedding network

2.2.2. CMOS Transistor Optimization and Neutralization.

In analog circuits, the transistor voltage gain is defined as in Eqn. (2.20). To boost the voltage gain, we can simply increase G_m or R_o. However, when operation frequency goes to sub-THz/THz, all the parasitic parameters, such as C_{GS} (gate-source capacitance), C_{GD} (gate-drain capacitance), C_{DS} (drain-source capacitance) and r_g (gate resistance) become non-negligible. That is the reason why transistor voltage gain drops with the increasing of frequency.

$$A_V = -G_m R_o \tag{2.20}$$

The frequency-depended current gain H_{21} is given by Eqn. (2.21) when the output of the transistor is shorted. The dominant parasitic capacitance is C_{GS}, approximates $(2/3)WLC_{OX}$, in the denominator. Once the frequency increases, H_{21} will drop, thus the voltage gain will drop. The strategy to boost the voltage gain is minimize the parasitic capacitance C_{GS}, which is applied in the baseband circuits.

$$H_{21} = \frac{g_m}{2\pi f(C_{GS} + C_{GD})} \tag{2.21}$$

The frequency at which the short circuit current gain of an intrinsic MOS transistor drops to unity is called transit frequency f_T, defined as

$$f_T = \frac{g_m}{2\pi(C_{GS} + C_{GD})} \tag{2.22}$$

For the circuits, such as power amplifier and oscillator, the power gain is superior to voltage gain, and it can be derived as Eqn. (2.23). Not only parasitic capacitors but also gate resistor need to be minimized to maximize the power gain and f_{MAX}. At the same time, transistor length should be as small as possible to obtain the maximize r_o, which is benefit to G_{MAX} and f_{MAX} as well. In summary, the layout optimization strategies are selected based on the categories (analog or RF) and operation frequency of the circuit. There is no hurt to minimize all the parasitic element parameters.

$$G_{MAX} = \frac{r_o}{4r_g}\left(\frac{g_m}{2\pi f C_{GS}}\right)^2 = \frac{r_o}{4r_g}\left(\frac{f_T}{f}\right)^2 \tag{2.23}$$

$$f_{MAX} = \frac{1}{2}\frac{f_T}{\sqrt{2\pi f_T C_{GD} r_g + r_g/r_o}} \tag{2.24}$$

As motioned before, power gain is the fundamental metric related to power generation or amplification. At sub-THz/THz, it is more challenging to achieve a decent power gain, because the maximum power gain G_{MAX} is constrained by the parasitics. However, the G_{MAX} value can be significantly improved by adding an embedding network, as shown in Figure 2.13 (b). The embedding network could parallel or series. Their theory and design procedures are explained clearly in [**29**] [**30**] and this dissertation will not repeat them again.

One of the transistor embedding application is neutralization. There are two types of neutralization: capacitor and transformer neutralization. Transistors in advanced CMOS technology are usually not unconditionally stable because of the positive feedback between transistor gate and drain terminals caused by the capacitance C_{GD}. In a differential transistor pair, one popular way to compensate the C_{GD}, is capacitor neutralization as shown in Figure 2.14.

Capacitors C_n connected between gates and drains of the opposing transistors in the differential pair behave as negative capacitances in the differential operating mode, acting against C_{GD} capacitances of the transistors themselves. Theoretically, if those capacitors are equal to C_{GD} and connected at the same node as C_{GD}, the gate-drain capacitances are completely canceled, resulting in an unconditionally stable stage. An additional advantage of this structure is an operation in the differential mode, leading to a closed signal current loop inside the differential pair and facilitating the circuit operation modeling. Due the extra parasitic at the nodes, it is better to tune optimize C_n and get the highest G_{MAX} at the given frequency. As shown in the bottom right plots in Figure

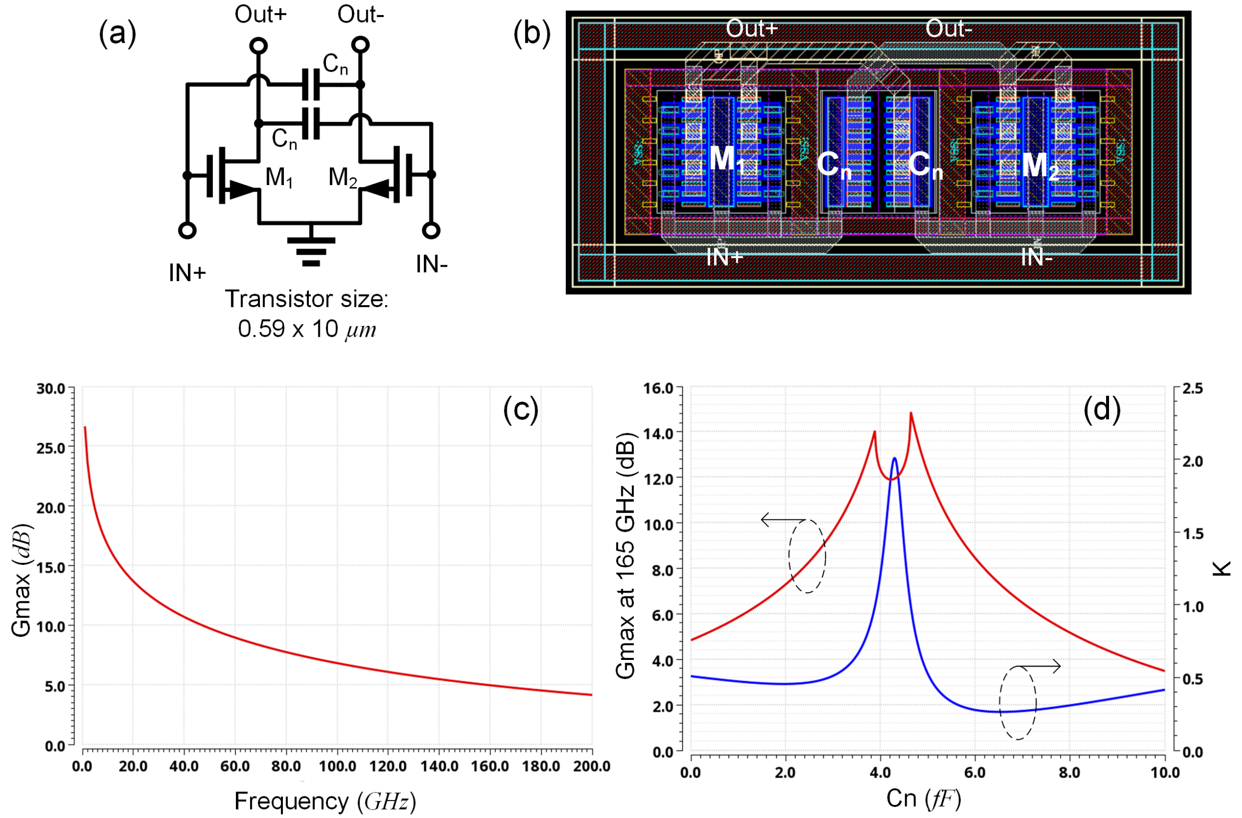


FIGURE 2.14. (a) Schematic and (b) layout of a capacitor neutralized transistor pair. G_{max} (c) before and after capacitor neutralization.

2.14, at 165 GHz, the G_{MAX} and K-factor are dramatically boosted to 12 dB and 2, respectively, when $C_n = 4 \sim 5\ fF$. K-factor is the Rollet's stability factor defined as Eqn. (2.25). tells you the two-port network is unconditionally stable when K-factor is greater than one. The initial G_{MAX} is plotted on the left bottom for comparison. The C_n could be MOS or MOM capacitor, because the Q is not so important in this situation.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \tag{2.25}$$

Transformer neutralization is also widely used in mm-wave and sub-THz/THz designs, especially suitable for common gate stages as shown in Figure 2.15. The typology is also named g_m-boosting common-gate [**31**] and its principle is compensating the input parasitic capacitance C_{GS} through a cross-coupled coils, resulting the improvement on noise and gain of an LNA. In the

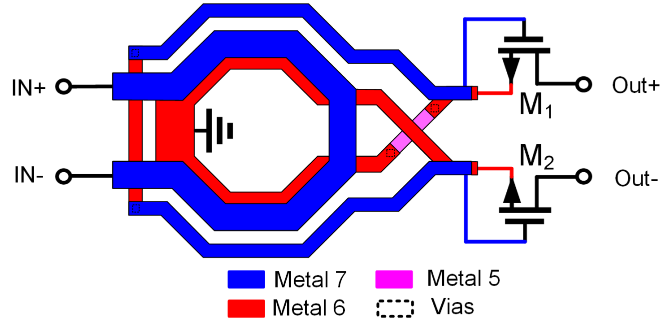


FIGURE 2.15. Example of transformer neutralization.

Chapter 5, an ultra-wide band LNA at sub-THz is successfully implemented with both transformer-neutralized common gate pair as the input stage and capacitor-neutralized common source pairs as the following stages. It achieves competitive bandwidth, gain and matching performance compared to the state-of-the-art, which proves that neutralization network is efficacious to improve the performance of transistors.

2.3. sub-THz/THz Detection and Key Blocks

In this section, sub-THz/THz detection is discussed by investigating the architecture and key building blocks. For all detecting system, such as imaging, sensing and communication system, SNR at the receiver front-end is critical for the signal quality acquired. This indicates that high performance receivers are equally important as high power transmitters for sub-THz/THz systems. To save the DC power burned and maximize the energy efficiency, link budget needs extremely attention and co-design of the transmitters and receivers is necessary. Firstly, the sub-THz/THz detection based on Si technologies is compared. Secondly, key blocks, such as envelope detector (ED), oscillator and quadrature VCO are designed at 165 GHz using standard 28 nm and 65 nm CMOS technologies.

2.3.1. Non-coherent and Coherent Detection.

There have been various detection approaches employed at sub-THz/THz. Si-based receivers can be divided into two types: direct (non-coherent) detection receiver and heterodyne (coherent) receiver. Figure 2.16 compares the recently reported noise equivalent power (NEP) obtained from Si-based (SiGe BiCMOS and Si CMOS) receivers at sub-THz/THz, together with other processes,

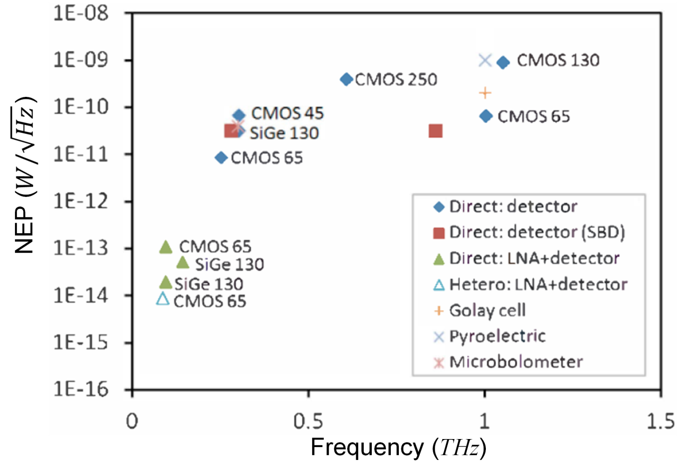


FIGURE 2.16. NEP comparison of Si-based receivers [D. Yoon et al., EuCAP, 2013]

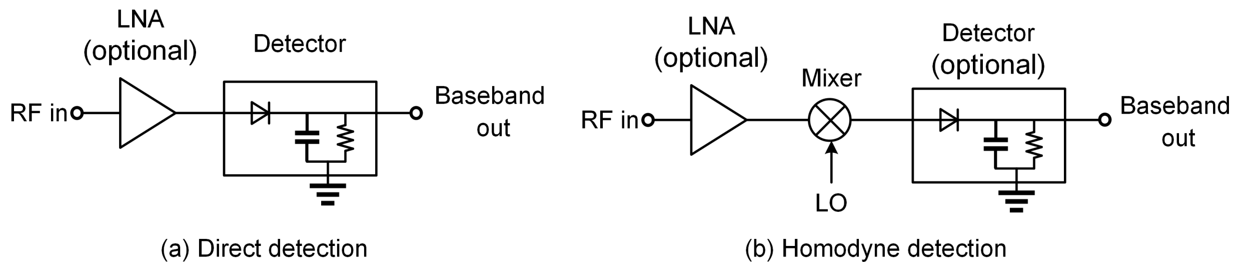


FIGURE 2.17. Diagrams of direct detection and homodyne detection

such as microbolometers [**32**]. The result shows that the Si-based receivers show comparable or better NEP performance than Golay cells, pyroelectric detectors and microbolometers. FET on CMOS and HBT on SiGe BiCMOS have similar performance. LNA in front of the detector reduces NEP by multiple orders of magnitude, but LNA is only implemented at sub-THz due to the limited gain and noise performance at THz, which is mentioned in the last section.

An example of direct (non-coherent) detection and heterodyne (coherent) receivers is shown in Figure 2.17. The most fundamental difference is whether a LO is required to demodulate the RF signal. Ideally, coherent receiver with a high-quality LO has better NEP leading to better SNR, and demodulation of quadrature modulation, such as QAM is possible, but it Requires expensive and complex LO generation or recovery circuits, such as phase locked loop (PLL). LNA is an option and the mixer can be operated in passive (no gain) and sub-harmonic mode for higher frequency applications.

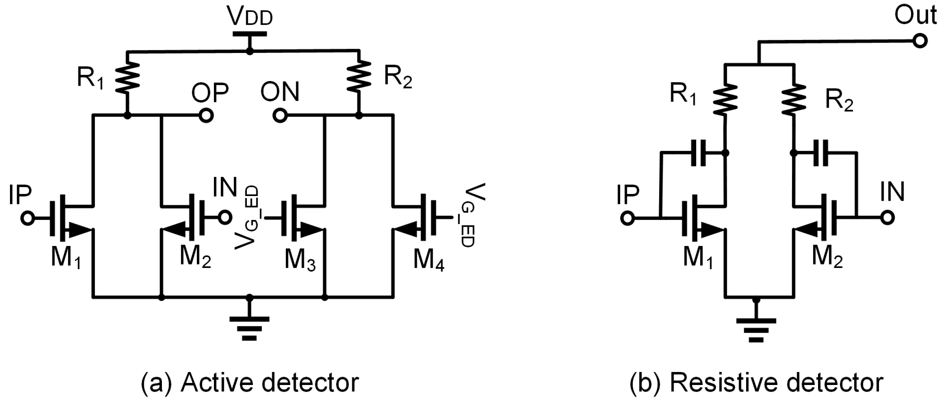


FIGURE 2.18. Active and resistive (passive) detectors.

In the direct detection case, detection is made at the frequency of incident signal. The detector is a key circuit block that converts the input signal power to baseband voltage. The direct detection is surfing from poor NEP and low responsivity (equivalent to conversion gain of a mixer) performance. LNA preceding the detector is a good idea to reduce NEP and provide sufficient gain at the operation frequency. On the other hand, the circuit complex and power consumption are increased. The link budget including signal bandwidth, transmitter power, channel loss and noise performance need to be considered before employing an LNA.

In the sub-THz interconnect systems, direct detection is the major approach employed to recover the baseband data, because an extremely low-loss channel and advanced multiplexer are designed, which relief the link budget. Square-law detectors, such as Schottky diodes, are dominantly employed exploiting their non-linearity. Transistors in standard CMOS technologies can be also used to implement detector circuits, as shown in Figure 2.18, and both active and passive transistor detectors can operate beyond the f_T as the gain could be below unit, because detector still has square-law function even it doesn't have any gain, unlike amplifiers or oscillators. The active detector is a differential pair with common drain node tied together and bias that forces the devices to operate in triode region with the strongest non-linearity. The current can be modeled with a Volterra Seriese $a_1V_{in} + a_2V_{in}^2 + a_3V_{in}^3...$ at the positive drain node, $-a_1V_{in} + a_2V_{in}^2 - a_3V_{in}^3...$ on the negative drain node. The square terms of the input signal resulting from the device non-linearity can be added and detected at the tied common node, while linear term and odd-order terms are

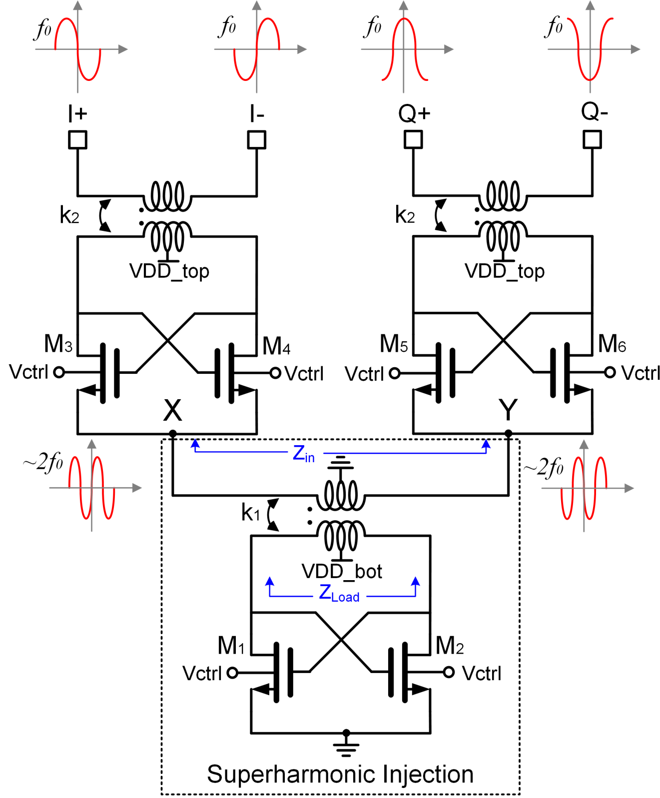


FIGURE 2.19. Schematic of the proposed superharmonic injection based quadrature VCO.

cancelled. The square term is proportional to the input power. A additional duplicated pair can be optionally inserted in symmetry to form a pseudo-differential output, thus eliminate the DC bias component and suppress the common-mode noise. In the resistive detector, the devices are operated in triode region without a duplicated pair. The input signal is self-mixed through the capacitors between the gate and drain, resulting in a baseband voltage proportional to the input power.

2.3.2. Quadrature VCO.

In a coherent detection system, quadrature LO as an essential component is widely used to enable high-order quadrature modulation with both amplitude and phase detection in the receivers.Quadrature signal generation in the mm-wave and sub-THz/THz frequency range is challenging through conventional techniques due to the introduced extra parasitic capacitance by the coupling devices. The method of using a tripler to generate 120 GHz quadrature LO from 40 GHz

quadrature inputs is a traditional way [**33**]. However, it introduces power-consuming components such as triplers and buffers. Another approach is to couple two oscillators using active or passive networks for quadrature generation. However, this structure has its own challenges. The passive coupling networks employ a phase shifter along the coupling path, and the phase accuracy is hard to guarantee due to its highly frequency dependent resonant networks [**34**] [**35**]. Active coupling by utilizing transistors adds more power consumption and noise and faces design trade-off between phase accuracy and phase noise (PN) performance in a quadrature oscillator [**36**]. Superharmonic coupling oscillation is an attractive technique [**37**]. It uses antiphase signals to lock the second harmonics of the two oscillators and enforcing fundamental frequency signals in quadrature phase relation without hurting PN, phase accuracy and tuning range. However, it is challenging to directly apply this idea to the frequency beyond one hundred GHz due to the difficulties of the generation and injection of second order harmonics.

A full-integrated superharmonic injection based G-band quadrature VCO is proposed in this section. The standalone quadrature VCO and I/Q signal test chips were fabricated in a 28 nm CMOS technology. Although the intrinsic device f_T is close to 300 GHz, the effective f_T and f_{max} are degraded significantly due to the parasitic effect, leading to lowering oscillation frequency and DC-to-RF efficiency. This work presents techniques in circuit structure, design ideas and layout strategies to overcome these challenges to guarantee the quadrature generation and boost the output power and efficiency. The quadrature VCO efficiently generates accurate I/Q signals from 149.3 to 152.4 GHz.

The quadrature VCO structure is illustrated in Figure 2.19. The top two oscillators generate differential outputs at fundamental frequency f_0. Their common-mode tail current source nodes are coupled through the bottom oscillator that resonates at frequency $2f_0$. The two tail current source nodes will present anti-phase signals at $2f_0$ if they are successfully injection locked by the bottom one. Because the injection signal is second harmonic of the top oscillation signal, the technique is named superharmonic injection. The critical factor for quadrature signal generation of this proposed structure is the successful superharmonic injection operation by the bottom oscillator at $2f_0$. To achieve that, the injection power needs to be strong enough and lock range needs to be sufficiently wide to cover the operating frequency.

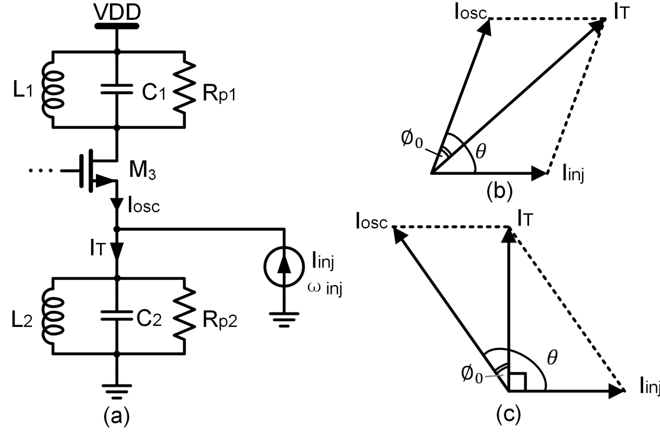


FIGURE 2.20. (a) The equivalent model, (b) phasor relationship, and (c) the maximum phase difference at the edge of injection lock.

Figure 2.20 (a) depicts the equivalent injection-lock analysis model. When an injection signal (I_{inj}, ω_{inj}) is added, it is required to satisfy the phasor relationship with I_{osc} and I_T, as shown in Figure 2.20 (b) [**38**]. The angle ϕ_0 between I_{osc} and resultant current I_T, and θ between I_{osc} and I_{inj} satisfy:

$$\sin\phi_0 = \frac{I_{inj}}{I_T}\sin\theta = \frac{I_{inj}\sin\theta}{\sqrt{I_{inj}^2 + I_{osc}^2 + 2I_{inj}I_{osc}\cos\theta}} \tag{2.26}$$

At the edge of the lock condition, as shown in Figure 2.20 (c), the phase should satisfy

$$\tan\phi_0 \approx \frac{2Q}{\omega_0}(\omega_r - \omega_{inj}) = \frac{I_{inj}}{I_T} \tag{2.27}$$

Where Q is the tank quality factor and ω_r is the resonant frequency of LC tank. Therefore, the lock range $\pm\omega_L$is determined as:

$$\omega_L = \omega_0 - \omega_{inj} = \frac{I_{inj}}{I_T}\frac{\omega_0}{2Q} \tag{2.28}$$

When $I_{inj} \ll I_{osc}$

$$\omega_L \approx \frac{I_{inj}}{I_{osc}}\frac{\omega_0}{2Q} \tag{2.29}$$

Lock range is inversely proportional to the Q, but lowering Q degrades the oscillation output power and efficiency, which is not a good trade-off in mm-wave and sub-THz/THz design. As a result, boost the injection signal strength is the natural way to increase the lock range. However,

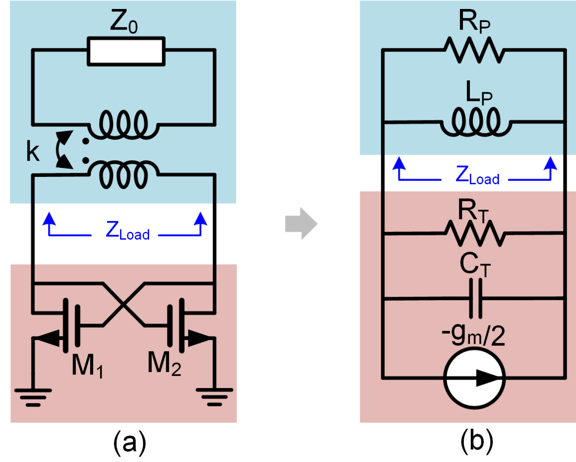


FIGURE 2.21. (a) Schematic of a cross-coupled oscillator and (b) its equivalent circuit

there are challenges even to start the oscillation at such high frequency, not even mention at the second harmonic. Firstly, the device transconductance g_m is extremely low at the frequency close to f_T. Second, the impedance looking into the common mode tail current nodes are relatively low, which drops the equivalent parallel resistance loading to the bottom oscillator to challenge the oscillation condition. To overcome the challenges, a transformer (k_1) is inserted between the top and bottom oscillators. First, it supports independent supply and bias of each oscillator to maximize the headroom and transistors' g_m so that it can satisfy the oscillation condition. Second, by adjusting the transformer parameters, including turn ratios and self-inductance etc., the optimum loading can be achieved to the bottom oscillator to increase the signal power and efficiency.

The top transformers (k_2) is designed to match to the optimum impedance faced by the core cross-coupled transistor pair. At high frequencies, transformer on the top metal is the best option due to its relatively high Q, which determines the oscillator signal power and efficiency. Besides, transformer-based impedance matching networks provide flexible structures for required impedance conversion ratio, differential interface suitable for cross-coupled transistor pair, and virtual ground in the centre readily for ground or DC connection.

Figure 2.21 depicts a cross-coupled oscillator and its equivalent circuit model, in which R_T is internal equivalent resistance, C_T is total node capacitance, R_P and L_P construct the load Z_L. According to the maximum power transfer theorem, when $R_P = R_T$, the maximum output power

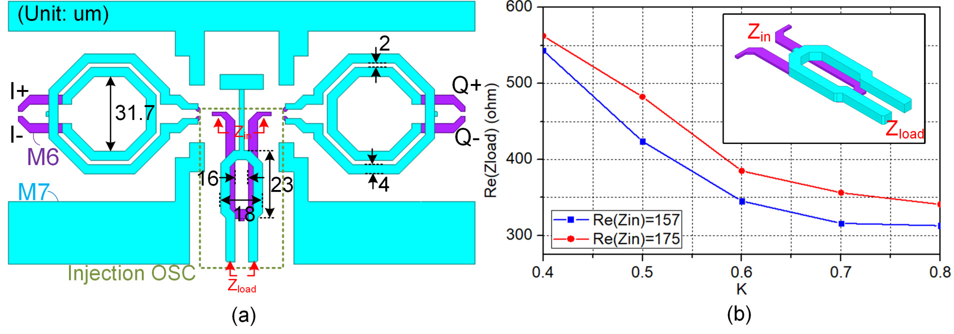


FIGURE 2.22. (a) Top view of the transformer in EM simulation. (b) Equivalent parallel resistance Z_{in} and boosted Z_{load} by tuning the coupling coefficient k of the transformer.

is delivered to the load. The other criteria that an oscillator must satisfy is oscillation condition, which is

$$-\frac{g_m}{2} + \frac{1}{R_T} + \frac{1}{R_P} < 0 \tag{2.30}$$

Therefore,

$$R_P > \frac{1}{\frac{g_m}{2} - \frac{2}{R_T}} \tag{2.31}$$

In the real case where the circuit is terminated with Z_0, a transformer is employed to realize the impedance matching. The transformer model with a series primary coil and a parallel second coil for analysis. Based on the parameters and definitions of the transformer, the input impedance can be calculated with Eqn. (2.19). The equivalent resistance R_p, parallel with the cross-coupled transistors at the resonant frequency ω_r is obtained:

$$R_P = \frac{\omega_r}{Re(Z_{in})} \tag{2.32}$$

Another key aspect of high-frequency LC oscillator is the design and layout of transformers, as shown in Figure 2.22 (a). Different transformers play different roles. As discussed in section II, the top transformer (k_2) is used to obtain maximum output power and DC-to-RF efficiency [**18**]. The transformers are drew as symmetric as possible to minimize common mode signal leakage to common source node to avoid disturbing the superharmonic signal injection operation. The bottom transformer is designed to push the oscillation frequency beyond 300 GHz and enlarge the

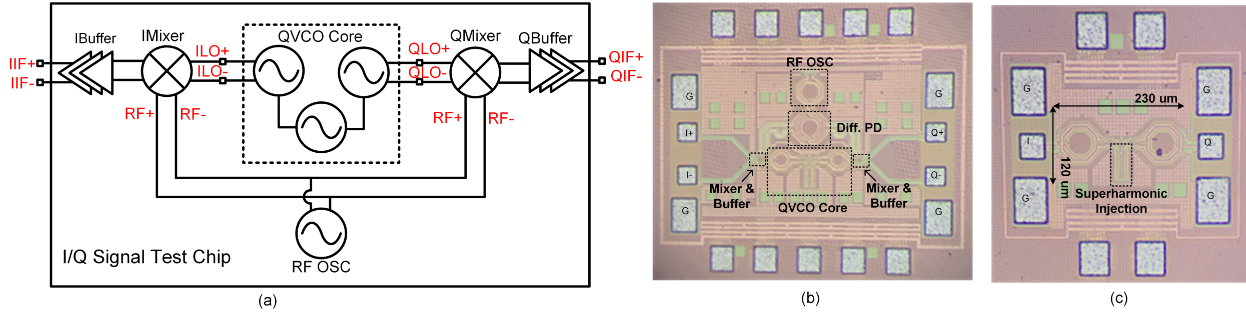


FIGURE 2.23. (a) Block diagram of I/Q signal test chip for phase and aptitude mismatch. Die micrographs of (b) the I/Q test chips and (c) standalone quadrature VCO.

injection signal level. As g_m is extremely small at high frequency, the priority is to satisfy the oscillation condition by boosting the parallel resistance presenting to the cross-coupled transistor pair without introducing extra inductance, which drops the operating frequency. Transformers at high frequencies are not easy to achieve large turn ratio due to the dimension constraint. The input impedance Z_{in} looking into the common-mode source nodes is obtained from simulation and listed in Figure 2.22 (b), and the equivalent parallel RC model is calculated as well. According to Eqn. (2.19) and (2.32), decreasing the coupling coefficient k is an effective way to boost R_p, as the curve shows in Figure 2.22 (b).

Due to the lack of ultra-wide band oscilloscope to measure I/Q signal in G-band, the on-chip down-convertors are implemented to convert to IF for I/Q signal measurements. Figure 2.23 (a) shows the block diagram with I/Q double-balanced mixers and buffers implemented on-chip. Besides, an additional differential signal is generated as the LO to mix down the G-band I/Q signals. The buffers are realized with pseudo-differential neutralized source follower amplifiers, providing high input-output isolation, driving the off-chip 50 Ω for IF I/Q measurements. Two chips, the I/Q signal test chip and standalone quadrature VCO, have been fabricated in TSMC 28 nm bulk CMOS technology, as shown in Figure 2.23 (b) and (c).

The measurement setup is illuminated in Figure 2.24. The output power, frequency and PN of the standalone quadrature VCO were tested with Keysight N9030A spectrum analyzer through the external G-band harmonic mixer OML M05HWD and GGB probes. The spectrum analyzer was calibrated and verified by an Erickson PM4 calorimeter. The standalone quadrature VCO occupies

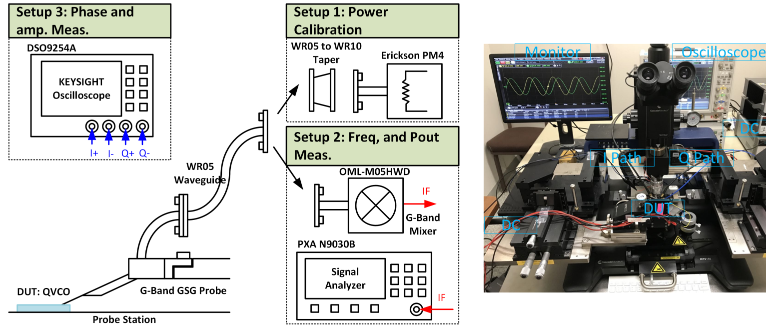


FIGURE 2.24. Measurement setups for output power, frequency at G-band, and phase and amplitude error at down-converted frequency.

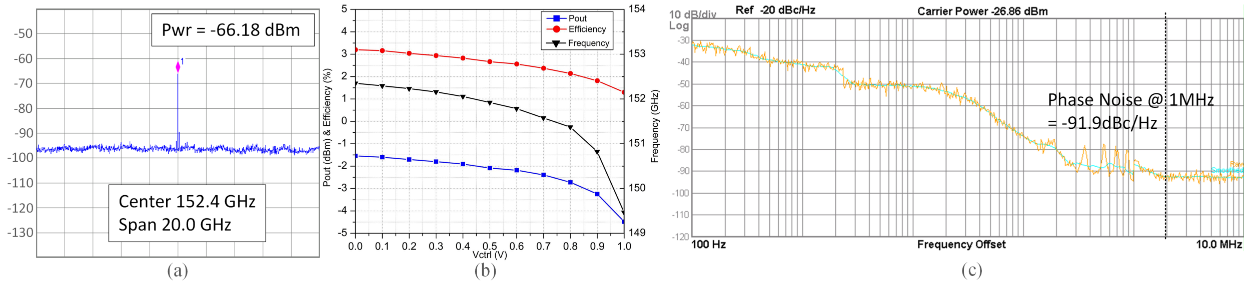


FIGURE 2.25. (a) Spectrum, (b) measured output power, DC-to-RF efficiency and oscillation versus the bulk control voltage, (c) phase noise at 152.4 GHz.

an active area of only 0.028 mm^2. It consumes 21.9 mA from a 1 V supply. Oscillation frequency covers from 149.3 to 152.4 GHz by tuning the body voltage from 0 to 1V. Figure 2.25 (a) shows the spectrum, measured output power and efficiency in the whole tuning range. In Figure 2.25 (b), it achieves the maximum power of -1.54 dBm with efficiency of 3.2% at 152.4 GHz. The measured PN is -91.9 dBc/Hz at 1 MHz offset for the 152.4 GHz output signal, as shown in Figure 2.25 (c). For the entire output frequency range, the PN is demonstrated is better than -90 dBc/Hz at 1 MHz offset.

The IF I/Q signal from the test chip were measured by a Keysight oscilloscope DSO9254A. The down-converted IF outputs at 3.7 GHz are shown in Figure 2.26. Measurements repeated over the entire tuning range and demonstrated a phase error of less than 1.5 degree and amplitude mismatch less than 0.33 dB. A comparison table with state of the art quadrature VCOs in silicon

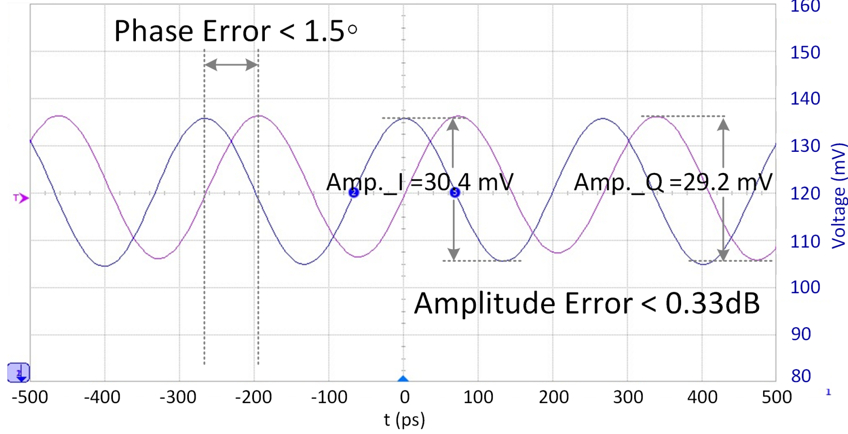


FIGURE 2.26. Measured quadrature signals down-converted to 3.7 GHz.

TABLE 2.3. Comparison with state-of-the-art QVCO at mm-wave/sub-THz in Si.

	TMTT'16 [35]	**TMTT'18 [39]**	**JSSC'15 [40]**	**JSSC'19 [41]**	**This Work**
Tech.	28nm CMOS	90nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS
Freq. (GHz)	71.4∼76.1/ 85.6∼90.7	49∼51.4	85∼127	37.5∼45	149.3∼152.4
Tunning range (%)	9.8	4.7	39.4	18.2	3.1
DC Power (mW)	35.6	75.4	45	8.4	21.9
Pout (dBm)	N/A	-10	-15	-65	-1.54
Efficiency (%)	N/A	0.13	0.07	∼0	3.2
PN @1MHz (dBc/Hz)	-114.2**/ -107**	-103.4	-105	-94.3	-91.9
Phase error (deg)	1.5/3.5	2.5	2	0.48	1.5
Amp. error (dB)	1	0.5	0.51	N/A	0.33
FOM_T* **(dBc/Hz)**	-165.6	-172.2	-180.9	-183	-168.3
Area (mm^2)	0.031	1.47	0.55	0.068	0.028

in the mm-wave/sub-THz band is shown in Table 2.3, where FOM_T is defined as

$$FOM_T = PN - 20\log\left(\frac{f_0}{\Delta f} \times \frac{Tuning\ Range}{10}\right) + 10\log\frac{P_{DC}}{1mW} \tag{2.33}$$

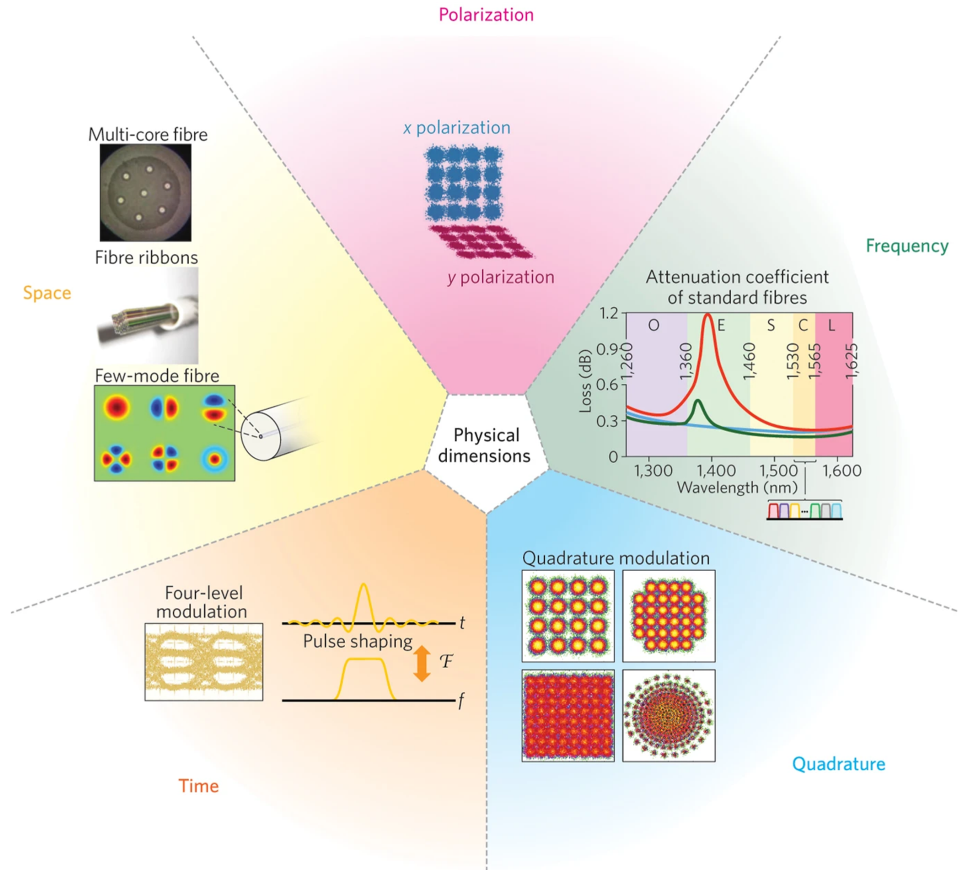


FIGURE 2.27. Spatial multiplexing schemes [P. Winzer, Nature Photonics, 2014]

and ** PN is at 10 MHz offset. Benefited by the superharmonic injection technique and the design optimization for both active and passive devices, this work achieves the best I/Q phase accuracy, highest power efficiency and good PN for the entire tuning range.

2.4. Multiplexing Schemes at sub-THz/THz

All the researchers acknowledge the Shannon Theorem that accurately defines the data capacity over a channel. There are two ways to improve it by broadening the bandwidth, increasing the modulation order or enhancing the SNR. Single-channel transmission had great development in the past decades, and is almost pushed to the physical limits of circuits and channels. Introducing more logical channels not only boosts manyfold the total data capability, but also provides data transportation possibility between nodes located at different spots. There are five dimensions of multiplexing: time, frequency, space, polarization, and quadrature [**42**], as shown in Figure 2.27.

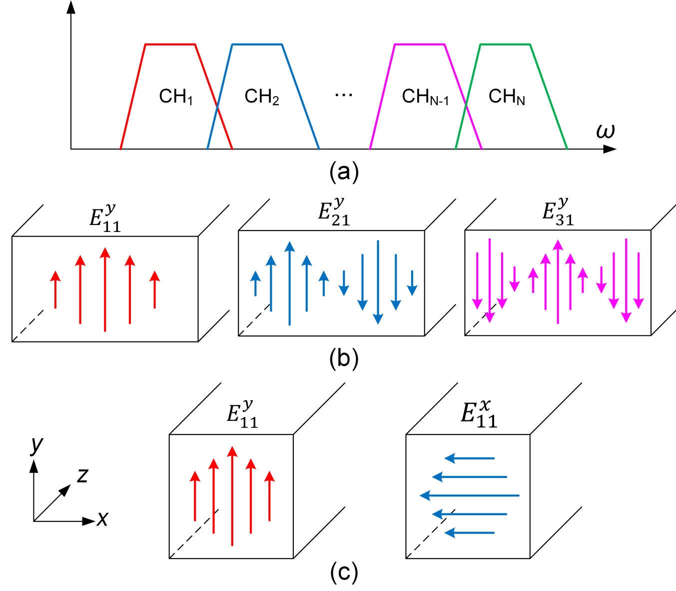


FIGURE 2.28. (a) Frequency division, (b) mode division, and (c) polarization multiplexing.

Time multiplexing does not increase the throughput. Quadrature multiplexing requires advanced signal processing and high order modulations, thus increasing performance requirements of system building blocks, such as PLL, analog to digital converter (ADC), digital to analog converter (DAC) and clock distribution. As a subsequence, it may not be very energy efficient and is not the focus of the sub-THz/THz interconnect. One of the challenges for sub-THz/THz interconnects lies in the realization of compact and low-loss multiplexers. Several multi-channel sub-THz/THz interconnects have been developed. In [**43**], a bi-directional plastic waveguide at E-band is implemented and achieves 13 dB insertion loss and lower than -55 dB crosstalk. However, the connector is difficult to be crowed into a package or device due to its large dimension. Another nonnegligible issue is interference when unshielded DWGs get closer, and coupling becomes considerable. Multiport interconnect consisted with dielectric waveguide Y-junctions is an option for multicasting and broadcasting in chip-to-chip communication [**44**], but it doesn't improve data rate and 3-dB signal loss is added theoretically if one more port is introduced. Frequency division multiplexing has emerged in waveguide [**45**] [**46**], on chip [**23**], and on substrate [**47**].

A Si DWG has been demonstrated 3-dB bandwidth of 59 GHz and transmission loss better than 4 dB [**48**]. To take fully advantage of the bandwidth, it is beneficial to adopt multiplexing

schemes to split one physical channel into several sub-channels logically, to relieve the system and active circuits specification requirements, such as the dispersion of the DWG and bandwidth of the transmitter and receiver, thus boost the total data rate. This section will introduce three multiplexers: frequency division multiplexing (FDM), polarization mode division multiplexing, and mode division multiplexing (MDM), that are designed for sub-THz/THz interconnects [**49**]. The detailed simulation, fabrication and measurement of frequency division multiplexing (FDM) and mode division multiplexing (MDM) multiplexers will be elaborated in Chapter 3 and Chapter 4, together with the sub-THz interconnect systems.

The circuit design and fabrication at sub-THz/THz are challenging because the smaller feature dimensions require high precision in modeling and fabrication. Three multiplexing mechanism of frequency division [**47**], mode division and polarization [**50**], is depicted in Figure 2.28 (a), (b) and (c), respectively. All of them achieve good transmission and isolation performance that can satisfy the high-speed chip-to-chip communications. The mode multiplexer can dramatically boost the data rate and bandwidth density of a sub-THz/THz interconnect, and are able to connect transceivers at different places, which works like a data bus. A smooth mode transition is a key factor to determine the overall performance of a mode multiplexing system.

2.4.1. frequency division multiplexing (FDM).

Frequency division multiplexing is combining and transmitting multiple communication signals in parallel at distinct carrier frequencies over the same transmission medium, as shown in Figure 2.28 (a). Each sub-channel is required to have enough bandwidth to support high data rate and sufficient out-of-band suppression to reduce crosstalk interference. Planar band-pass filter (BPF) is a good candidate of frequency division multiplexer. High Q substrate is preferred to realize the channel selection filter, which can minimize the transition loss and improve the suppression by cascading more stages.

To illustrate frequency division multiplexing, a dual-band sub-THz channel is designed, as shown in Figure 2.29 (a), which consists of Si DWG, microstrip line (MSL)-to-DWG transition and a pair of diplexers. MSL-to-DWG transition in Figure 2.29 (b) smoothly transfers quasi-TEM mode in MSL to E_{11}^{y} mode in DWG for a wide frequency band. The diplexer, as the only bandpass

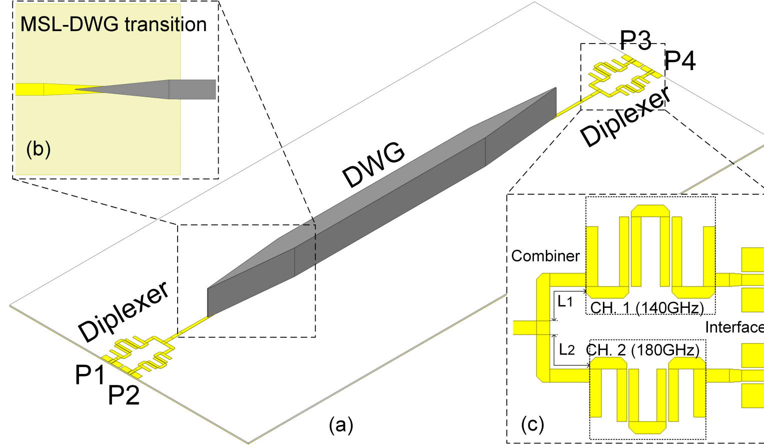


FIGURE 2.29. (a) Structure of the dual-band channel, (b) MSL-to-DWG transition, and (c) diplexer on BCB substrate.

component in the channel, determines the frequency selection performance and is synthesized on dielectric substrate of 20-μm BCB. Its $\varepsilon_r = 2.7$ and $\tan\delta = 0.03$ are calibrated at 165 GHz, which is necessary for frequency sensitive components above mm-Wave. The sub-THz diplexer, as illustrated in 2.29 (c), is constructed with BPFs, a combiner and GSG interface. Conventional hairpin BPF adopting edge-coupled resonators has the compact size due to folded $\lambda/2$ MSL approaches. The center frequencies of the BPFs in the diplexer are 140 GHz and 180 GHz, respectively, and the bandwidth is more than 20 GHz to support high data-rate communications. The simulated insertion loss is about 3 dB and suppression in the adjacent bands is more than 20 dB. When the two BPFs are combined, one BPF will be part of the loading to the other BPF. To minimize the loading effect, 50-Ω L_1 and L_2, which have minor effect in its passband but significant effect on the adjacent band (the passband of the other BPF), are tuned to present a high-impedance to the other BPF. The simulation, fabrication and measurement will be presented in Chapter 3.1.

2.4.2. Polarization (or Orthogonal mode) Multiplexing.

Polarization multiplexing also can realize simultaneous transmission of multiple information streams. The orthogonal modes, E_{11}^y and E_{11}^y in Figure 2.28 (c), are transferred by a polarization diplexer, which is a device combining or separating orthogonally polarized signals. The orthogonal modes are intrinsically isolated because of the polarization. Figure 2.30 (a) shows the ortho-mode

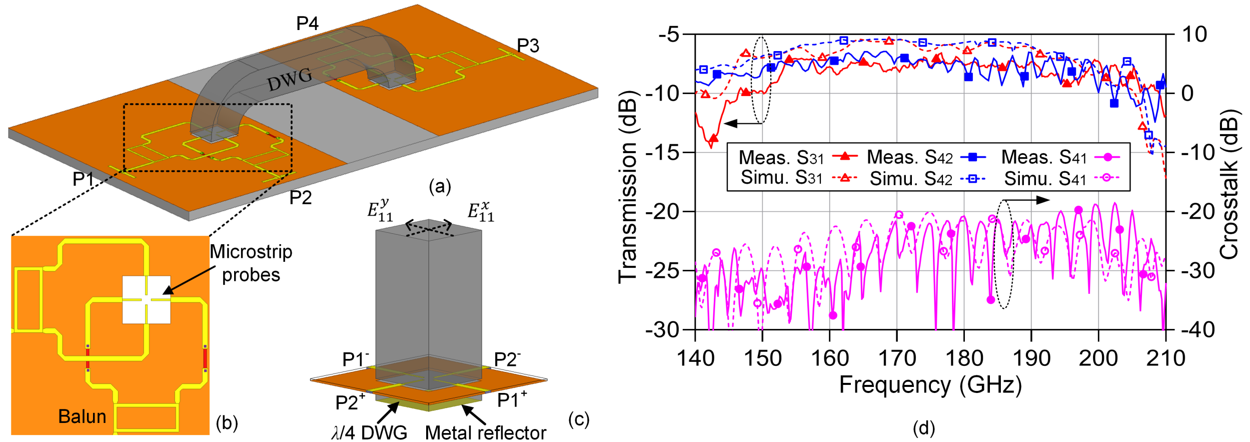


FIGURE 2.30. (a) Stucture of the ortho-mode channel, (b) single-ended to differential transition, (c) probe-based MSL-to-DWG transition. (d) Comparison of the simulated and measured S-parameters.

DWG channel. There are two orthogonal fundamental modes, E_{11}^{y} and E_{11}^{y}, supporting the signal propagations via the P1-to-P3 path (S_{31}) and the P2-to-P4 path (S_{42}), respectively. It consists of a pair of single-end to differential baluns in Figure 2.30 (b), probes-based MSL-to-DWG transition in Figure 2.30 (c) and an isotropic rectangular DWG. The differential probes-basedMSL-to-DWG transition is proposed to form a differential mode intrinsically to excite E_{11}^{y} or E_{11}^{y} mode in the DWG. The identical pair of microstrip probes are fed with differential EM waves, and a reflector is placed $\lambda/4$ away from the feeding position, provides out-of-phase signal cancellation and only allows the EM waves propagate along the up direction of the DWG. The balun was optimized and achieved less than 1.5 dB magnitude mismatch and 7 degree phase mismatch at the range of 140∼190 GHz. To implement a planar interconnect, the DWG is bended, but introduce the asymmetric bending issue and large ripples occurs for an ortho-mode DWG if the bending radius is less 1000 μm at 165 GHz. The transmission loss for E_{11}^{x} and the mode E_{11}^{y} are 6.6 dB from 151.1 to 171.4 GHz and 6.5 dB from 150.8 to 206 GHz, respectively. The crosstalk between orthogonal modes is better than -20 dB in the range of 140∼210 GHz.

2.4.3. mode division multiplexing (MDM).

At a given frequency, a wider Si DWG can support multiple modes existing simultaneously and different modes are naturally isolated from each other. Taking advantage of this feature

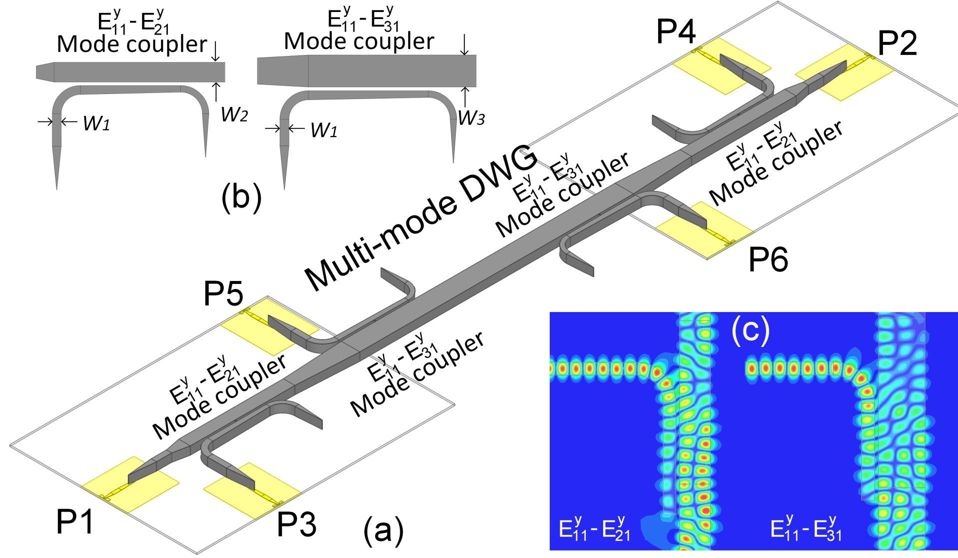


FIGURE 2.31. (a) Structure of the multi-drop channel, (b) mode coupler between $E_{11}^{y} - E_{21}^{y}$ and $E_{11}^{y} - E_{31}^{y}$, and (c) the E field distribution.

can build multiple channels in a physic link and transmit data simultaneously. Figure 2.28 (b) shows a multi-mode channel with three modes (E_{11}^{y}, E_{21}^{y} and E_{31}^{y} modes) and they have sufficient isolation to suppress the crosstalk. Mode converters transfer modes, combine and separate signal streams at each end, working as multiplexers. The challenge of this design lies in maximizing the coupling efficiency to a desired mode and avoiding stimulating other unwanted modes and crosstalk interference.

Figure 2.31 (a) illuminates a multi-drop channel that consists of a multi-mode Si DWG, MSL-to-DWG transition and mode couplers implementing mode conversion between E_{11}^{y} and E_{21}^{y}, E_{11}^{y} and E_{31}^{y}, respectively. The coupling always exists when the unshielded DWGs approach close, and it happens between the same modes (for example E_{11}^{y} and E_{11}^{y}) or different modes (such as E_{11}^{y} and E_{21}^{y}). The condition for mode coupling are field overlap and phase matching. Field overlap means DWGs are close enough and field in each waveguide is interacting. Phase matching requires that the propagation constant β, which is the wavenumber along propagation direction, are equal for those modes. By precisely controlling the width of DWG, the effective refractive index n_{eff} of a specific mode can be finely tuned, then it is possible to make two modes phase matched. As shown in Figure 2.31 (b), mode E_{11}^{y} is fed from the branch DWG with W_1=300 μm, which has the same

n_{eff} of E^y_{21} in a DWG with W_2=760 μm and E^y_{31} in a DWG with W_3=1200 μm, then coupling happens between E^y_{11} and E^y_{21}, E^y_{11} and E^y_{31}, as shown in Figure 2.31 (c). The theoretical analysis and demonstration of the multi-mode multi-drop Si waveguide will be presented in Chapter 4.

2.5. Conclusion

Various components, such as off-chip and on-chip passives, semiconductor technologies, actives in CMOS, schematic and layout optimization strategies, circuit typologies, receiver architectures, quadrature VCO and multiplexers, are presented in Chapter 2. This chapter analyzed the characteristics and behavior of such components at sub-THz frequencies, proposing design and optimization techniques. Most of those key blocks and techniques are employed in the sub-THz interconnects, playing the fundamental and vital role of the systems. The theoretical analysis and derivation are verified with simulations and demonstrations, which are clearly presented. Other potential techniques such as coherent detection and high-order modulation schemes are also discussed, because those techniques could be employed in the future demonstration to further boost the performance. From next chapter, the dissertation start to introduce the application of those components and techniques dual-band and multi-mode multi-drop sub-THz interconnects.

CHAPTER 3

Dual-band Sub-THz Interconnect

As discussed in the Chapter 2.4, advanced spatial multiplexing has potential to boost the total data rate significantly without complex transmitters, receivers and strict high-order modulations. The two key metrics for all interconnects are the energy efficiency, defined as pico-joules per bit, and the bandwidth density, defined as gigabits per second per square micrometer. Sub-THz/THz interconnect [**18**] [**51**] demonstrates high potential to address the long-standing challenge by leveraging the advantages of both electrical and optical interconnects due to the wide available spectrum.

Among the multiplexing schemes, FDM is the most popular one that has been implemented in both wireless and wireline communication standards. Carrier assigned to each frequency channel is generated by the corresponding oscillator or VCO. For coherent detection, carriers must have a steady oscillating waveform at a single frequency, and be much higher in frequency than the baseband signal. In direct detection system, the requirement in quality for the carrier is much lower. The carrier signal and the baseband signal are combined in a modulator circuit. In the modulator, baseband signal is at the sum $(f_C + f_B)$ and difference $(f_C - f_B)$ of the frequencies. The other baseband signals are used to modulate carriers at other frequencies, creating other channels of information. The carriers are spaced far enough apart in frequency to avoid overlapping of each sub-channel. High data rate baseband signal has relatively wide bandwidth, like the on-off keying (OOK) in sub-THz interconnect, the total bandwidth will be at least the sum of the sub-channels' bandwidth, normally much larger. Very luckily, we have designed a Si DWG based channel at sub-THz with 80 GHz flat bandwidth that can enable multiple sub-channels.

This chapter percents a full-duplex sub-THz interconnect system based on FDM scheme. The system consists of a dual-band transmitter, receiver, and DWG channel that provides low in-band insertion loss and high isolation in the two adjacent frequency bands. Full-duplex measurement was set up with pseudorandom binary sequence (PRBS) length of 2^{31}-1. With the bit error rate (BER) $< 1 \times 10^{-12}$, channel 1 (CH.1) at 140 GHz and channel 2 (CH.2) at 180 GHz achieve on-off

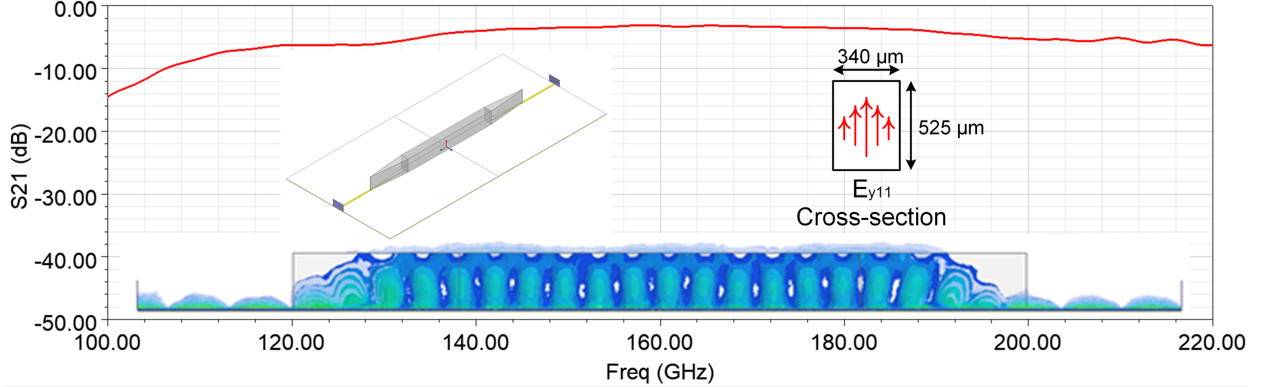


FIGURE 3.1. Si-based DWG, its E field distribution and S-parameters.

keying (OOK) modulated data rate of 12.3 Gb/s and 10.3 Gb/s, respectively. This full duplex interconnect system achieves the energy efficiency of 1.58 pJ/b and the record bandwidth density of 150.7 Gb/s/mm^2.

The innovation of this design is the implement of FDM and efficient direct detection in the dual-band sub-THz interconnect. Two broadband and low-loss transmission channels are built with high isolation, which are the foundation to combine signal streams and significantly boost the aggregate data rate. The passive and active analysis and co-design maximize the energy efficiency and guarantee the demonstration success. The other advantage of the architecture is that high-quality LO, off-chip LO synchronization or complex clock recovery are not required in the measurement.

3.1. FDM Implement: Dual-band Si DWG Channel

A dual-band sub-THz channel is required to have features of low insertion loss, high isolation, and good frequency selectivity. The channel consists of a Si DWG, a pair of diplexers and DWG and MSL-to-DWG transitions. To fully utilize the waveguide bandwidth, two sub-channels, at 140 GHz (CH.1) and 180 GHz (CH.2), are designed.

3.1.1. Si dielectric waveguide (DWG).

The Si DWG as core part of the dual-band channel at sub-THz covers an ultra-wide 3-dB bandwidth from 120 to 200 GHz, meanwhile the simulated minimum insertion loss is better than 3.5 dB. The structure, simulated S-parameters and E-field distribution in the Si DWG is depicted in Figure 3.1. High-permittivity and high-resistivity Si ($\varepsilon_r = 11.7,\ \tan\delta = 0.001$) serves as the low

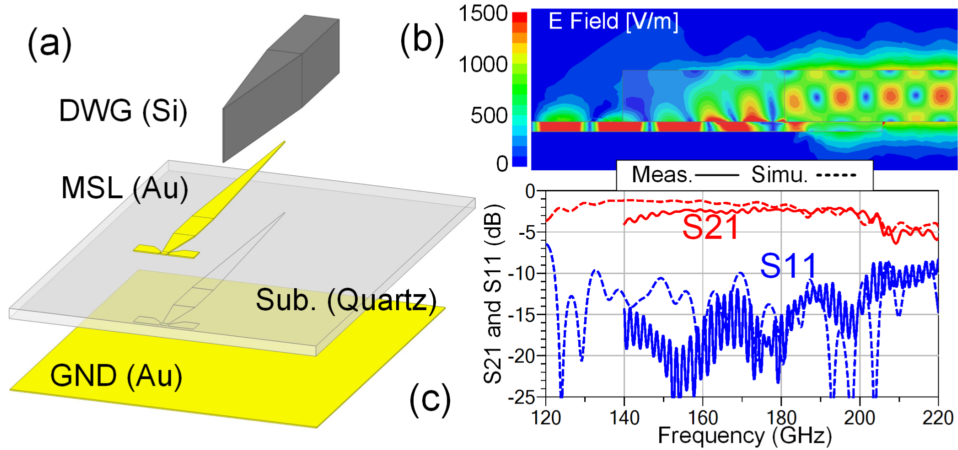


FIGURE 3.2. (a) Configuration, (b) E-field distribution and (c) S parameters of the MSL-to-DWG transition

loss and compact transmission medium due to its low material loss of 0.017∼0.034 dB/mm at THz and high dielectric constant. In the rectangular waveguide with a dimension of 340 $\mu m \times 525$ μm (W x H), E^y_{11} and E^x_{11} are the fundamental modes and polarized along y and x directions, respectively. Both modes have a low cut-off frequency (about 110 GHz) and high-pass frequency response, therefore, a wide pass band is formed. However, the bandwidth can not be infinitely wide, because at high frequency range, it is easy to excite higher-order mode conversion and introduce another type of loss. This mode conversion happens in metallic waveguide as well.

The other reason why Si DWG achieves wide bandwidth and low-transition loss is benefit from the low-loss near-field MSL-to-DWG transition. It consists of the overlapped taper-shaped DWG and taper-shaped MSL as illustrated in Figure 3.2 (a). It shows the mode is smoothly propagated from the MSL to the DWG. The cross-section view of the simulated E field distributions for the transition are illustrated in 3.2 (b). The mode is gradually transitioned from the quasi-TEM in the MSL to the hybrid mode, and then to the E^y_{11} mode in the DWG.

To measure the accurate calibrate and break down the insertion loss of each part, a straight Si DWG in 10 mm was designed, as shown in Figure 3.3 (a). The measured DWG transition loss is about 4.2 dB across the range of 150∼200 GHz, as shown in Figure 3.3 (b) The simulated straight Si DWG loss is about 0.04 dB/mm. Therefore, the transmission loss breakdown is: 0.4 dB from the straight Si DWG; 1.9 dB from an MSL-to-DWG transition. Compared with the simulated results

FIGURE 3.3. (a) A straight DWG and (b) its measured S-parameters

FIGURE 3.4. Structure of the BPF based diplexer

in Figure 3.2 (c), S21 is degraded by 0.4∼0.5 dB, which is probably caused by the misalignment and air gap between the MSL and DWG. The essential mechanism of the transition design is the phase match, with which the propagation constant in two medium are equal or close. The mechanism will be explained in the Chapter 4.

3.1.2. Filter-base diplexer.

The sub-THz diplexer, as illustrated in Figure 3.4 is constructed with BPF, a combiner and a GSG interface. Conventional hairpin BPF, adopted in the diplexer, has the small size with the length of hairpin resonator of around $\lambda/2$ using MSL approaches. The center frequencies of the BPFs in the diplexer are 140 GHz and 180 GHz, respectively, and the bandwidth is more than 20

Table 3.1. Dimensions of the diplexer (unit: μm).

CH. 1		**CH. 2**		**Interface**		**Combiner**	
LL1	194	LH1	144	LI1	10	LC1	340
LL2	90	LH2	65	LI2	100	LC2	325
LL3	290	LH3	220	LI3	50	WC1	56
LL4	80	LH4	75	LI4	60	WC2	56
WL1	50	WH1	50	LI5	100	**Substrate**	
WL2	50	WH2	50	WI1	48	TSub	20
WL3	40	WH3	40	WI2	150	TM1	0.3
WL4	50	WH4	50			TM2	2

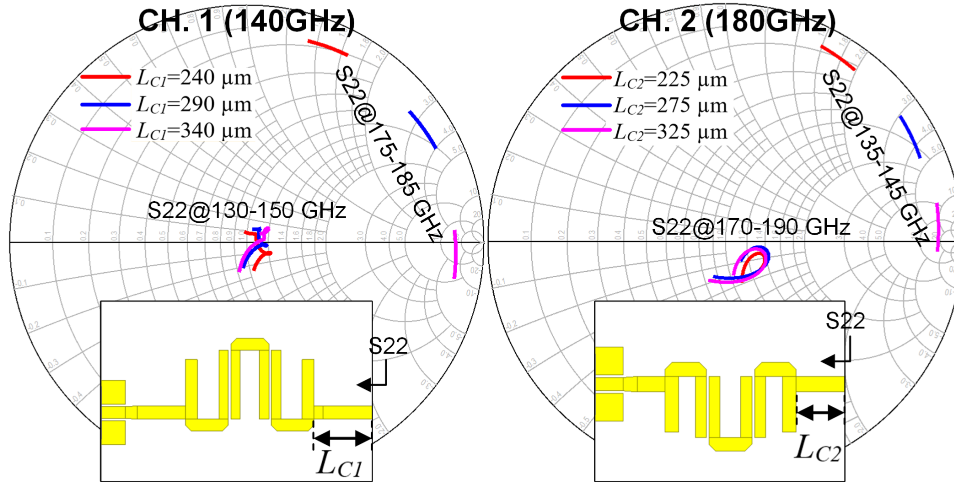


Figure 3.5. Input impedance of the BPFs.

GHz to support high data-rate communications. The simulated insertion loss is about 3 dB and suppression in the adjacent bands is more than 20 dB. When the two BPFs are combined, one BPF will be part of the loading to the other BPF.

To minimize the loading effect, L_{C1} and L_{C2} that have minor effect on the frequency response in its passband, are tuned to shift S22 at frequency of the other sub-channel to high-impedance region, as shown in Figure 3.5. For instance, L_{C1} in CH.1 is swept from 240 μm to 340 μm, and the normalized input impedance S22 at 175~185 GHz, which is the passband of CH.2, moves toward high impedance region in the Smith Chart. The dimensions of the diplexer, including the combiner and GSG interface, are summarised in Table 3.1.

The accurate high-frequency electrical properties of BCB ($\varepsilon_r = 2.65,\ \tan\delta = 0.015$ up to 20 GHz) is not provided by the datasheet. Therefore, a permittivity sensor is necessary to accurately

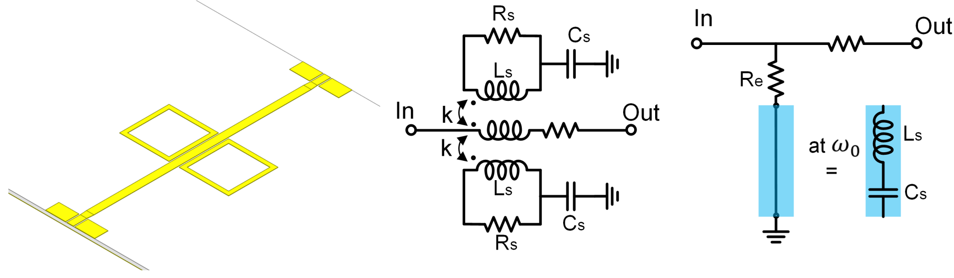


FIGURE 3.6. Resonator based dielectric sensor

measure the material parameters, which has significant impact to the diplexer design. A planar resonator-based sensor, as illustrated in Figure 3.6, is designed, and fabricated together with the dual-band channel. The equivalent lumped model and simplified circuit at the resonate frequency are demonstrated in Figure 3.6 as well. The key metrics for resonator-based sensors are resolution that affects the sensing accuracy, and loaded quality factor Q that determines how easily the resonate dip or peak will be detected [**52**]. The rectangular ring forms the inductor and the overlap between top and bottom metal layers forms the capacitor. The resonate frequency is expressed by

$$f_r = \frac{1}{2\pi\sqrt{L_s C_s}} = \frac{\sqrt{d}}{2\pi\sqrt{L_s \varepsilon_r \varepsilon S_{eff}}} \tag{3.1}$$

where d is the substrate thickness, L_S is the effective inductance of the ring resonator, ε_r is the relative permittivity of the substrate, ε_0 is the permittivity of free space, and S_{eff} is the effective area of plates. Once the dimension of the sensor is fixed, f_r shifts as the relative permittivity of the substrate changes. The resonance dip is majorly determined by the equivalent resistor R_e remained to the main path at resonate frequency, which is given by Eqn. (3.2).

$$R_e = \alpha \frac{R_s}{Q_L^2 k} \tag{3.2}$$

where α is the coefficient fitting the equation into different circuit models, R_s and Q_L are the series resistance and quality factor of the ring, and k is the coupling coefficient between the resonator and main path. Large Q_L and k will contribute to form resonance dip. Rectangular rings with larger k is better than circular rings in this situation. When a resonator element is introduced on both sides, the proposed design has slightly lower resonant frequency and deeper dip in the transmission

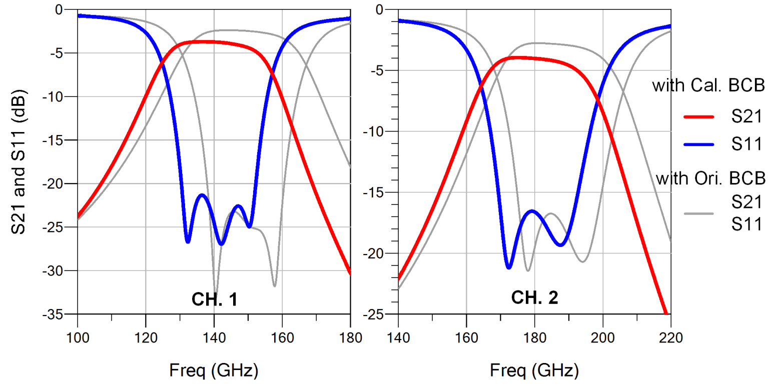


FIGURE 3.7. Simulated S-parameters of the BPFs

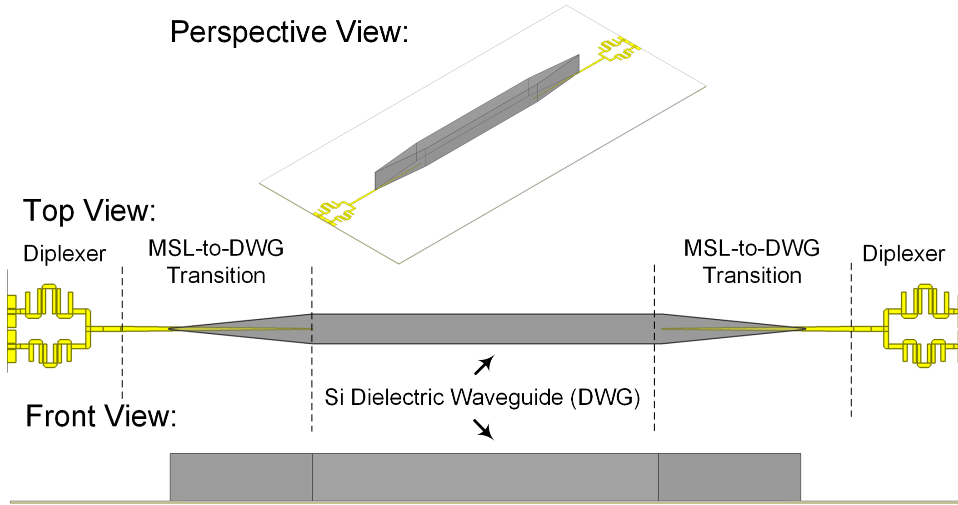


FIGURE 3.8. Structure of the dual-band Si DWG channel.

resonance. By comparing simulation and measurement results, the parameters of BCB provided on the datasheet ($\varepsilon_r = 2.9$ and $\tan\delta = 0.03$ at 160 GHz) are calibrated, which are utilized for the BPFs and dual-band channel design.

The simulated S-parameters of BPFs designed with the original and calibrated electrical properties of BCB are plotted in Figure 3.7. Both BPFs at CH.1 and CH.2 achieve the minimum insertion loss of 3.8 dB with the calibrated electrical properties of BCB. Compared with the performance based on the original electrical properties, the insertion loss degrades by 1.4 dB and center frequency shifts lower by 8 GHz approximately, but the results match better with the measurements.

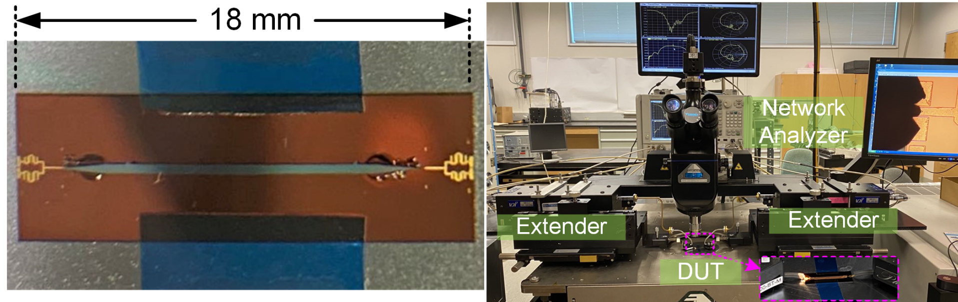


FIGURE 3.9. Photo and G-band S-parameter measurement setup.

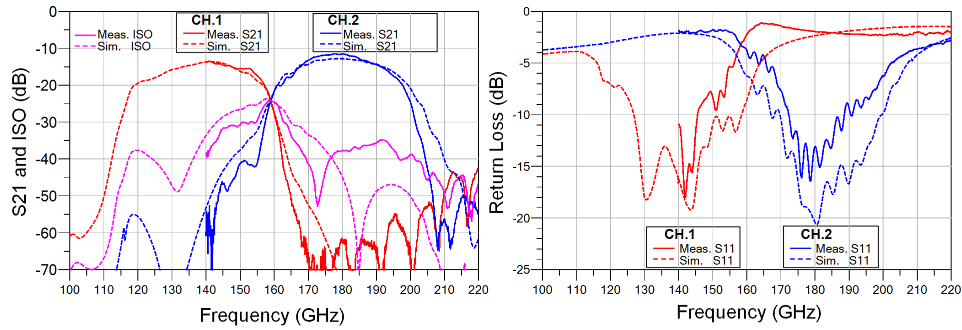


FIGURE 3.10. Measured S-parameter.

The entire structure, as shown in Figure 3.8, was modelled in full-wave simulator HFSS and measured on-wafer with G-band (140 to 220 GHz) S-parameters testbench. All parts are fabricated in-house with micro-manufacturing process. Si DWG is produced by deep reactive ion etching (DRIE). MSL-to-DWG transition and diplexer are fabricated using lithography on a thin-film substrate BCB and assembled with Si DWG by a flip-chip bonder to form the dual-band sub-THz channel. The fabrication processes of diplexer board are summarized as the followings. M1 (50 nm/300 nm Ti/Au) is deposited on the top of a 300-μm Si wafer. Then, A 20-μm BCB is spin coated with curing. After that, top metal layer M2 is deposited and thickened to 2-μm with electrical-plating process. At last, Si DWG is bonded to diplexer board with a flip chip bonder, as shown in Figure 3.9.

The simulated and measured S-parameters of the dual-band sub-THz channel are shown in Figure 3.10, and they agree well with each other. The minimum measured insertion loss is 13.2 dB for CH.1 (140 GHz) and 11.7 dB for CH.2 (180 GHz). Both bands have more than 25 GHz

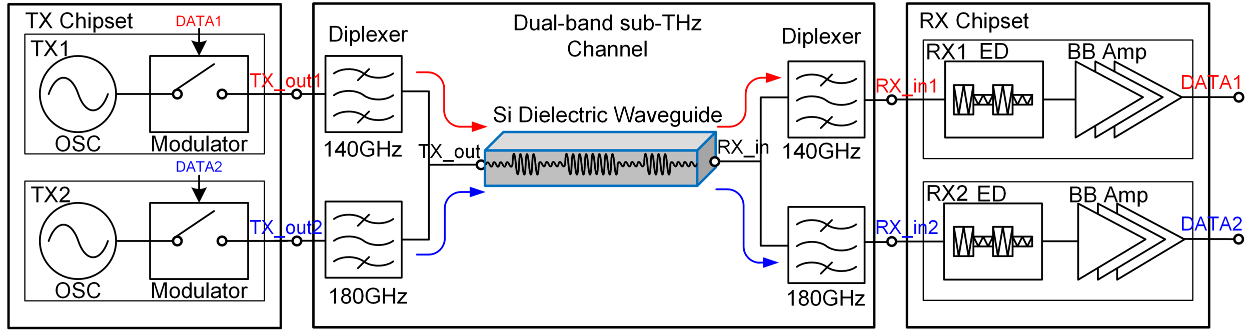


FIGURE 3.11. Architecture of the dual-band sub-THz interconnect.

3-dB bandwidth and in-band isolation is more than 30 dB. High out-of-band rejection of diplexer reduces the noise level on receiver side and relaxes its dynamic range requirement.

3.2. Dual-band sub-THz Interconnect system

The sub-THz interconnect system consists of two parts: the active and passive channel, including Si DWG, transitions, diplexers and interface between components. To minimize interference from each other, both sub-channels are required to have enough bandwidth and sufficient suppression in the other sub-channel frequency band. Two separate sub-channels, at 140 (CH.1) and 180 GHz (CH.2), are designed in the last section, achieving transition loss of 11∼13 dB within 3-dB bandwidth of 25 GHz. The more than 30 dB in-band isolation significantly eliminates the crosstalk interference. Benefit from the high-performance channel, non-coherent detection and low-power transmitter and receivers can be adopted to drive the data transmission When designing the sub-THz interconnect. Carriers at two different frequencies are generated by oscillators in the dual-band CMOS transmitter. Since a switch-based OOK modulator is employed, and it need a clear binary bits waveform and proper voltage swing to drive the switch on and off, so Nyquist pulse shaping can't not be applied in the baseband, which can save half of the bandwidth. Si Binary sequences are modulated as OOK signals by the carriers with the bandwidth at least twice of its data rate. On the receiver side, the two streams of RF signals modulated at different carriers ate separated by the diplexer and recovered by ED. Power-hungry components, such as PLL, PA and frequency multiplier, are avoided in the non-coherent transceivers, the system has competitive energy efficiency compared to the other reported designs.

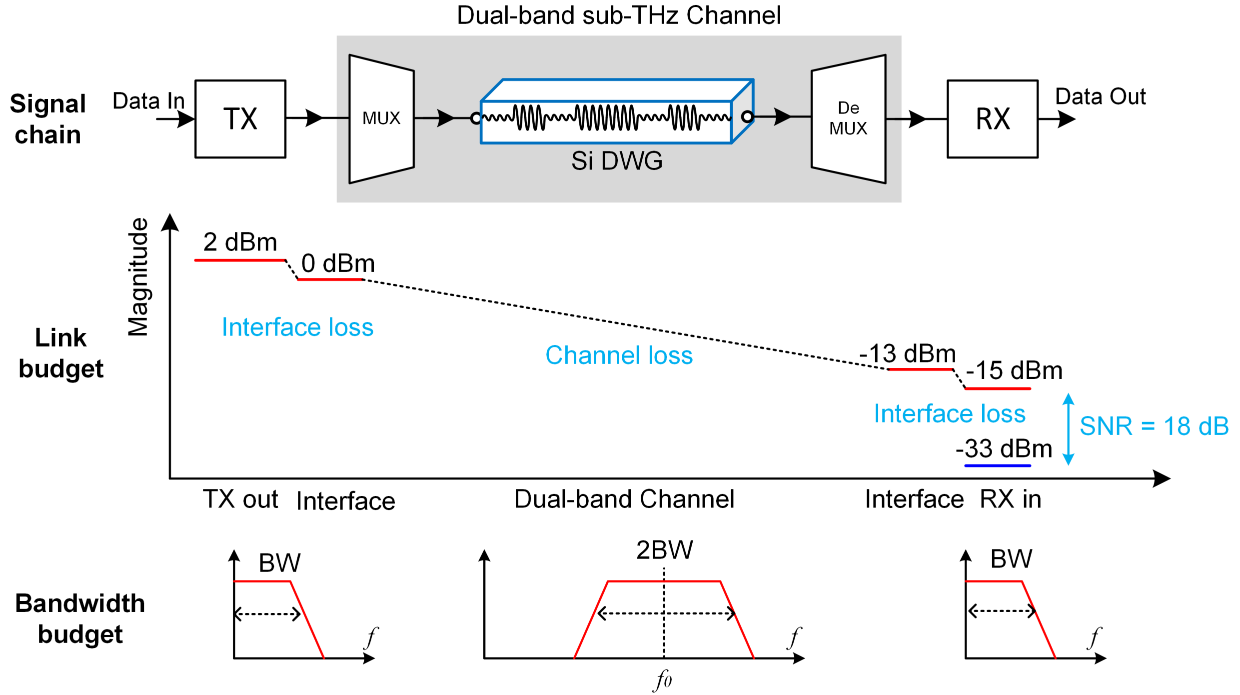


FIGURE 3.12. Link budget and bandwidth budget of the dual-band sub-THz interconnect.

On the other hand, since all the components in the signal chain are in low power condition, the link budget and bandwidth budget must be calculated carefully to establish a communication link successfully. the link budget analysis is provided in Figure 3.12. The target data rate for each subchannel is 12 Gb/s (totally 24 Gb/s). Based on the non-linear property of the ED in the receiver, the link budget analysis is different with the conventional mixer-based system. Voltage responsivity (R_v) and NEP, used to quantify the performance of the ED, which are similar to the gain and noise figure (NF) of an LNA, respectively, and they will be derived in section 3.4. The simulated NEP of an active ED is about 5 $pW/\sqrt{Hz}$ ($\approx -83\ dBm/\sqrt{Hz}$), and it is a reasonable value according to Figure 2.16. T To achieve 12 Gb/s data rate, at least 12 GHz bandwidth is required for the baseband and it contributes about 50 dB noise on top of the noise floor and raises the noise strength to -33 dBm. The minimum SNR requirement for OOK signal to maintain a BER below 1e-12 is 17 dBc, thus the minimum signal strength for receivers is -16 dBm. If the transmitter can generate 2 dBm power and there is about -15 dBm can be delivered to the receivers after deducting all the loss along the signal chain, which satisfies the link budget. However, the link budget is too tight and

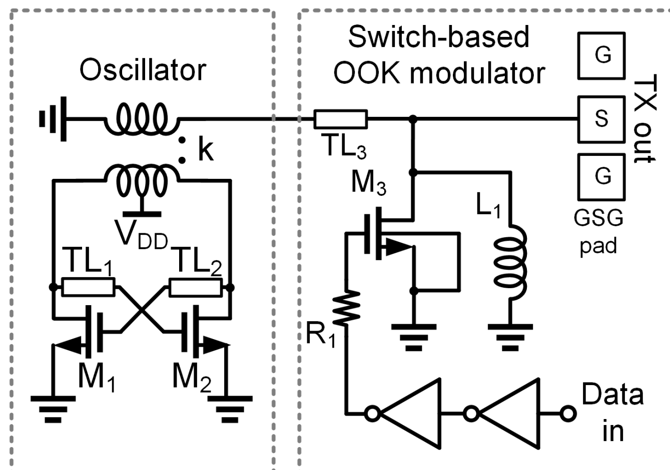


FIGURE 3.13. Schematic of the transmitter.

there is no margin for the extra loss or interference introduced in practice, so an improved version will be proposed in Chapter 5, achieving much better data rate and SNR.

For the channel, transmitter and receivers in this dual-band sub-THz interconnect, since the target maximum data rate is only 12 Gb/s, they have sufficient bandwidth to support the communication. The bandwidth budget is also illuminated in Figure 3.12. The required bandwidth in the baseband circuits and RF front-end are 12 GHz and 24 GHz, respectively. The estimated power consumption of each sub-channel is about 15 mW for the transmitter and 3 mw for the receiver except the on-chip baseband amplifier and buffer, which are employed to enhance the output voltage swing for measurement, but do not affect the SNR if their bandwidth is sufficient. The overall energy efficiency is about 1.7 pJ/b and bandwidth density is about 150 Gb/s/mm^2

3.3. Transmitter

Figure 3.13 shows the building blocks and schematic of the transmitter that consists of an oscillator as the carrier generator and switch as the OOK modulator. At sub-THz/THz, few CMOS PA or multiplier achieves decent energy efficiency, due to large influence of the parasitics and low gain. Oscillator and harmonic-mode oscillator have capability to generator signals close or even beyond the f_{MAX} with a higher energy efficiency. Shunt-NMOS switch has relatively low loss and broad bandwidth at sub-THz/THz, making it suitable to be the modulator in the interconnect system, but there is a trade-off between isolation and insertion loss, which directly determine the

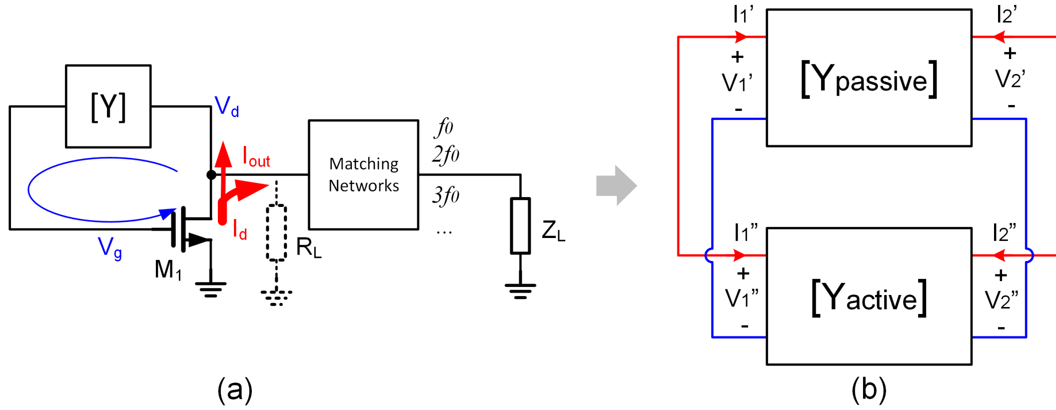


FIGURE 3.14. (a) Topology of an colpitts oscillator and (b) its equivalent two-port network model

signal on-off ratio. The other drawback of the switch-based modulator only support ASK and doesn't allow Nyquist shaping process. This section firstly introduces the oscillator design and its power maximization approach; secondly, discusses the switch modulator optimization.

3.3.1. Oscillator and Power Maximization.

Oscillator is the engine of the transceiver and takes a large fraction of the total power consumption. To boost the bandwidth density, the high carrier frequency is preferred. However, the operating frequency is limited by the transistor' f_{MAX}, which is around 280 GHz for a 65-nm bulk CMOS technology. Hence, the relatively low f_{MAX} makes the high-output-power and high-efficiency circuits much challenging. Chapter 2.3 has discussed the oscillation condition and transformer-based load matching of a transitional cross-coupled oscillator. The RF power (P_{out}) can is normally dilivered to 50-Ω terminals and energy efficiency is defined as

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{P_{out}}{V_{DC}I_{DC}} \tag{3.3}$$

To maximize the output power, we need to understand the RF power generation mechanism. As shown in Figure 3.14 (a), the basic oscillator topology is a positive feedback loop, which means gate voltage (V_g) experiences a phase shift and magnitude changing through the transistor and feedback network [Y], but still maintains a positive gain. An active transistor works as the engine, and it will generate RF power. When talking about the power or current flow, part of the power

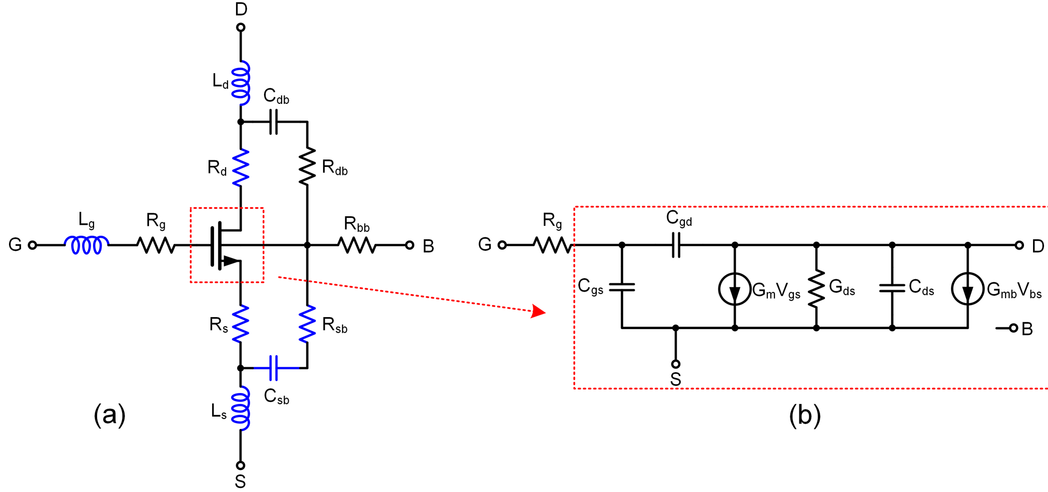


FIGURE 3.15. (a) Transistor with parasitic elements and (b) its large-signal model

is extracted by the matching networks that could match at f_0, $2f_0$ or $3f_0$ by tuning the networks, and part of the power goes to the feedback loop and maintain the oscillation. The task is to extract more power from the transistor to the load, which will maximize the output power.

Figure 3.14 (b) depicts the Y-parameter (admittance) matrix that is used to model the circuit. For the passive Y matrix, we suppose all components except R_p are lossless. R_p is the equivalent load looking into matching networks and it is considered the load of the circuit. In the active Y matrix, only the effective transconductance G_m is nonlinear. The transistor experiences three regions, triode, saturation and cutoff, so G_m is nonlinear, similar as PA. We define the port voltages and currents. The complex RF power generated by transistors is defined by

$$P = V_1^* I_1 + V_2^* I_2 \tag{3.4}$$

Then, using the Y-parameters of the passive network and port voltages to represent the current I_1 and I_2,

$$P = |V_1|^2 \left(Y_{11} + A^2 Y_{22} + Y_{12} \frac{V_1^* V_2}{|V_1|^2} e^{j\phi} Y_{21} \frac{V_1 V_2^*}{|V_1|^2} e^{-j\phi} \right) \tag{3.5}$$

where $A = \frac{|V_2|}{|V_1|}$ and $\phi = \angle \frac{|V_2|}{|V_1|}$ are the magnitude and phase the passive feedback network. The real power flowing out of the transistor is

$$P_{real} = |V_1|^2 \left\{ -G_{11} - A^2 G_{22} - A|Y_{12} + Y_{21}^*| \cdot \cos[\angle(Y_{12} + Y_{21}^*) + \phi] \right\} \tag{3.6}$$

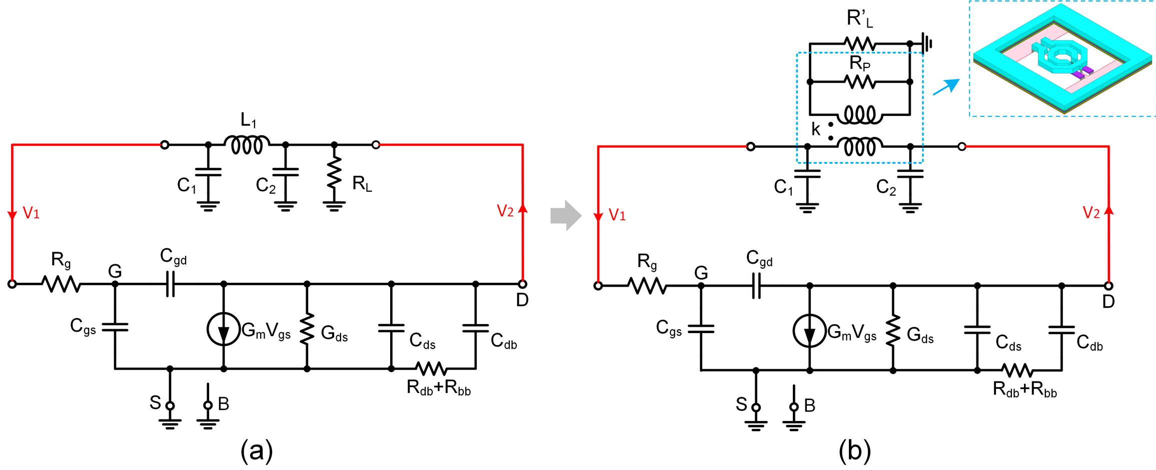


FIGURE 3.16. Transistor with (a) lumped element feedback network and (b) synthesized transformer model.

where G is the G-parameters.

Since the R_p is the only lossy component and transistor is the only active device in the circuit, according to the energy consecration principle, the power generated by the transistor should be equal to the power dissipated on R_p. Obviously, only the last term could be positive and P_{real} can be maximized by setting $\cos[\angle(Y_{12} + Y_{21}^*) + \phi] = -1$, which is the first condition to maximize power.

A real transistor has many parasitic element at gate, drain and source nodes, as shown in Figure 3.15 (a), and all those parasitic elements plays negligible effect on the current and voltage in a sub-THz/THz circuits. The large-signal model with a nonlinear G_m is illuminated in Figure 3.15 (b). With that large-signal model, a feedback loo can be built by inserting an LCR network that can be synthesized to a transmission line or a transformer easily, as shown in Figure 3.16. By analyzing the circuit, we can calculate the phase of the port gain ($A = \dfrac{V_2}{V_1}$) by $\pi-$ phase shift of the transistor,

$$\phi = \pi - \tan^{-1}\left\{\frac{\omega[G_m R_g(C_{gs} + C_{gd}) + C_{gd}] - \omega C_{gd}}{G_m - 2R_g C_{gd}(C_{gs} + C_{gd})\omega^2}\right\} \approx \pi - \tan^{-1}[\omega R_g(C_{gs} + C_{gd})] \tag{3.7}$$

The parasitic parameters of a transistor layout can be extracted accurately by Cadence Calibre and the calculated optimum ϕ is shown in Figure 3.17 (a). For the selected transistor is about 164° at 165 GHz.

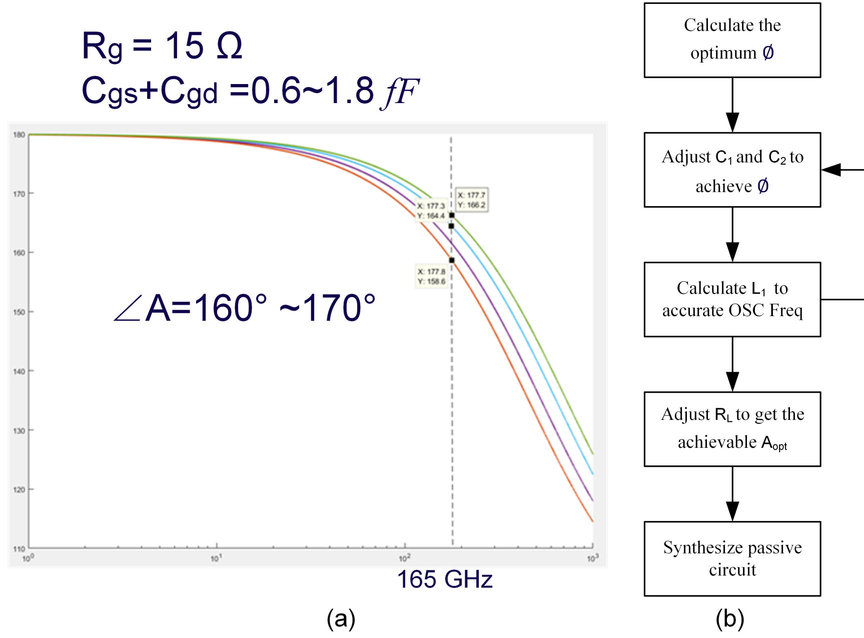


FIGURE 3.17. (a) Calculated optimum ϕ versus frequency. (b) Procedure of power maximization for an oscillator.

At a stead state of the oscillator,

$$\frac{V_2}{V_1} \approx -\frac{G_m + j\omega(C_1 + C_{gs})}{G_{Rp} + G_{ds} + j\omega(C_2 + C_{ds})} \tag{3.8}$$

Since $G_m \gg \omega(C_1 + C_{gs})$ and $G_{RL} + G_{ds} \gg \omega(C_2 + C_{ds})$, ϕ is majorly determined by C_1 and C_2, L_1 together with all the capacitors determines the oscillation frequency, so it also participates the phase tuning. The second condition to maximizing power is the optimum magnitude $|A|$ that is majorly determined by G_{Rp} according the Eqn. (3.8).

The design procedure to maximizing the output power is concluded in Figure 3.17 (b), and this approach has been verified with simulation and measurement. Tuning C_1 and C_2 effectively changes the phase shift, but the operation frequency, therefore, the series inductor L_1 is tuned correspondingly to make the LC tank resonate at the desired frequency. Several iteration is necessary to optimize the design. Back to the cross-coupled oscillator schematic in Figure 3.13, the transmission line TL_1 and TL_2 is employed to tuning the phase and the transformer is utilized to convert the load impedance to the optimum R_p.

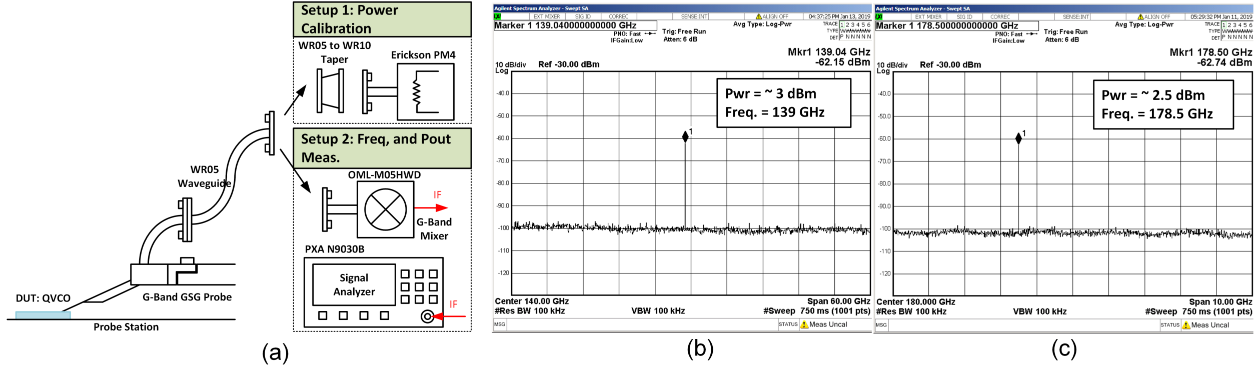


FIGURE 3.18. (a) Measurement setup for sub-THz oscillator. The measured spectrum at (b) 140 GHz and (c) 180 GHz.

The oscillator designed at 140 GHz and 180 GHz are measured individually. Figure 3.18 shows the testing setup. Same as the quadrature VCO, the output power were measured with power meter and spectrum analyzer. The measured results are 3 dBm at 140 GHz and 2.5 dBm at 180 GHz including the loss of a switch modulator, as shown in Figure 3.18 (b) and (c). The power efficiency is more that 13% with DC power consumption of 15 mW.

3.3.2. Switch-based OOK Modulator.

In the sub-THz transmitter, another crucial component is the high-speed modulator. In the sub-THz frequency range, switches are widely used for the OOK modulation [**53**] [**54**]. In this work, a single pole single throw (SPST) switch-based passive modulator is adopted to maximize the power efficiency as shown in Figure 3.13. The on-off transistors are turned off and operated as the shunt networks consisting of a capacitance C_{ds} and a large resistance R_{off} in the pass mode while they are turned on and operated as the shunt networks consisting of a capacitance C_{on} and a very small resistance R_{on} in the isolation mode. The equivalent models are drawn in Figure 3.19 for the pass and isolation modes, respectively. The baseband input data is sent into an input buffer and then pumped into transistors' gate terminals. Due to the parasitic capacitance C_{gd}, the input RF signal could be coupled to the gates which are biased by a constant voltage and then is reflected. Normally, R_g is preferred as large as possible to eliminate the reflection. However, a large R_g will affect the data rate due to a large RC constant. With the trade-off, 150-Ω resistor is used to minimize the insertion loss and maximize the data rate.

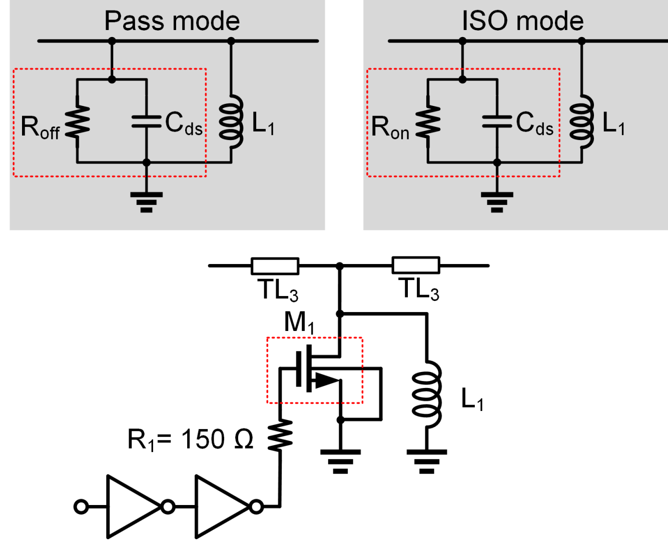


FIGURE 3.19. Shunt transistor SPST and its on-/off- circuit model.

3.4. Receiver

The son-coherent sub-THz receiver consists of a balun and an envelope detector (ED) based demodulator. To facilitate the measurement, a limiting amplifier (LA) based output buffer is employed. The entire architecture is shown in Figure 3.20 (a).

First of all, the OOK signal is received by the balun's input. Figure 3.20 (b) depicts the schematic of the demodulator. As discussed in Chapter 2.3, active EDs are based on the feature of the non-linearity of MOS transistors. To maximize the received input power of the ED, the interface of the ED input and 50-Ω source should be matched conjugately. ED is not a frequency sensitive component, but the input balun must align with carrier's frequency to reduce power reflection. Therefore, the transformer serves as both the single-ended to differential-outputs converter and the impedance converter. The imaginary part of the input matching network comes from the flux leakage of the transformer and resonates the parasitic capacitance of the transistor. The real part of the input matching network matches with the parasitic resistance R_g. The ED demodulates the input RF signal and extracts the baseband at zero frequency. Besides, the differential structure suppresses the odd-mode signals. A duplicated ED is employed to form the pseudo-differential outputs to improve the common-mode noise rejection. In addition, to suppress the undesired fundamental signal and its harmonics, a shunt Cd is added to form a low-pass filter (LPF). To

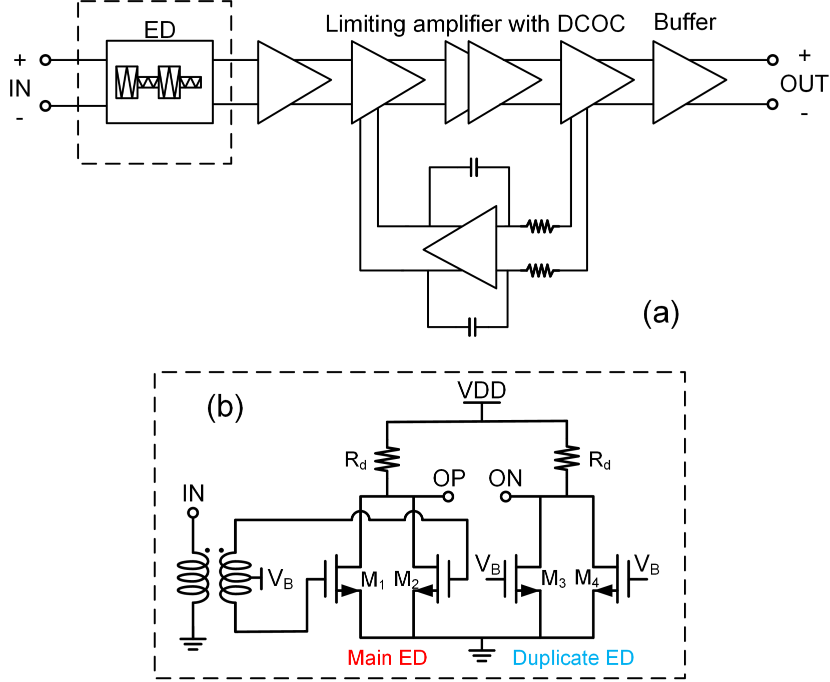


FIGURE 3.20. (a) Architecture of the receiver and (b) schematic of the ED

support a high data rate, a small RC product is necessary by reducing the load resistor R_d because the capacitance is usually from parasitic elements and it has been minimized when optimizing the transistor's layout. On the other hand, reducing R_d drops the responsitivity R_V defined as Eqn. (3.9), and then degrades the NEP performance, which directly decides the sensitivity of the receiver. By trading off the NEP and speed, the load resistance R_d = 700∼800 Ω is selected for the dual-band sub-THz interconnect, which achieves the target of 15 Gb/s data rate and guarantee about 5 dB margin for the sensitivity.

$$R_V = \frac{V_{out,pp}}{\Delta P_{in,RF}} = \frac{\partial^2 I_d}{\partial V_{in}^2} re\left\{Z_{in}\right\} R_d \tag{3.9}$$

where I_d is the drain current, v_in is the input voltage, $re\{Z_{in}\}$ is the real part input impedance and R_d is the load resistor of ED. The maximum R_V happens at the most nonlinear region of a transistor, thus, the bias is set close to V_T. After ED, baseband signals are magnified by amplifiers and buffers, then delivered to 50 Ω off-chip terminals for measurements.

Strong signal is always prefered in the measurement. To meet the minimum input requirement of the BERT, an LA is used to further amplify the output of the ED. One of a critical issue for

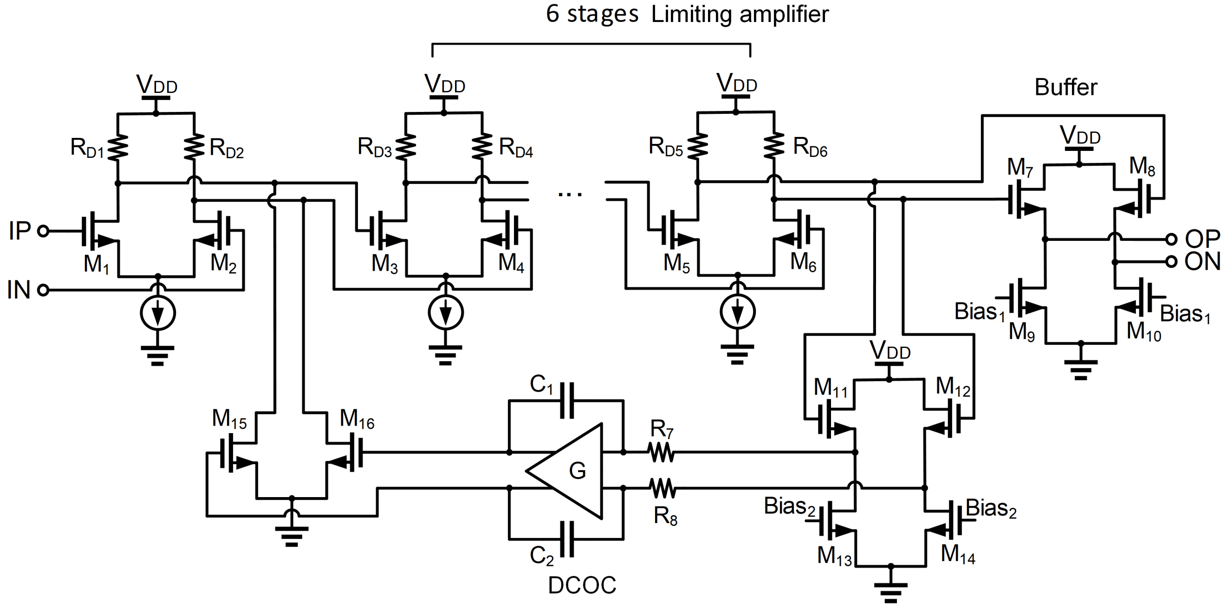


FIGURE 3.21. Baseband LA with DCOC loop.

the LA is dc offset. A tiny dc off-set will be amplified significantly after several stages and let the dc bias at incorrect level. The gain could be reduced dramatically. The DC offset cancellation (DCOC) techniques can eliminate this issue by using a high-pass filter (HPF), which has an infinite attenuation at dc. Generally, there are four types of DCOC techniques, including AC coupling, feed-forward, digital correction, and DC feedback. For the AC coupling, huge capacitors are required between each stage but it is area consuming. For the feed-forward, there are two identical parallel gain blocks are required. Actually, it is too hard to achieve due to process variations. For the digital correction, it simplifies the analog design but requires a DSP unit. For the dc feedback, it feeds the dc offset from the output to the input by a LPF and the dc offset is canceled. In this work, the dc feedback technique is employed. A broadband, low-noise, high energy-efficiency LA is prefered, therefore, the number of stages would like to be minimized as long as it satisfies the BERT sensitivity requirement. Normally, the minimum sensitivity of the Anritsu BERT is 10 mV V_{pp}. Both LA and DCOC have been explained clearly in the textbooks [**55**] [**56**], so they are not repeated in this dissertation.

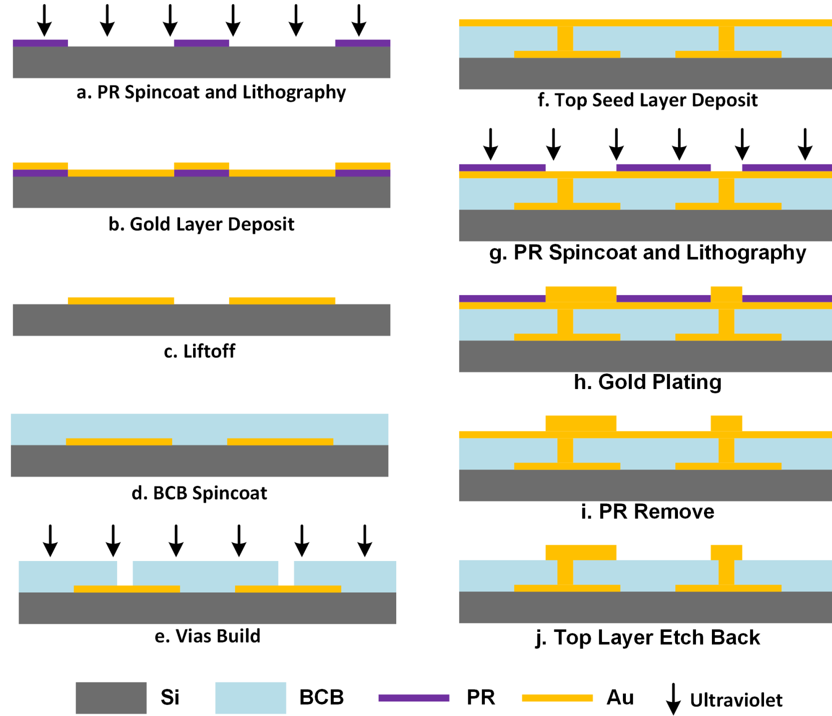


FIGURE 3.22. Diplexer board fabrication

3.5. Fabrication and System Packaging

The transmitter and receiver chipsets are implemented in a TSMC 65-nm CMOS technology. All other components are fabricated in-house with micro-manufacturing process and assembled with a flip-chip bonder. The device fabrication and packaging of the dual-band sub-THz/THz system is as important as the circuit design. Due to the short wave length at sub-THz/THz, any dimension inaccuracy or bonding misalignment will affect the performance significantly. Every step in the fabrication and packaging processes is worth to think about, analyze, co-design simulate and debug until the final success. After repeating for several times, the procedure of critical components and packaging will be presented in this section.

The diplexer board is fabricated on a 20-μm thick BCB substrate. The fabrication processes of the diplexer board and transition are summarized in Figure 3.22. Since the thin BCB substrate is soft and fragile, a 300-μm thick Si wafer having the same thickness as CMOS chips, is used to hold the entire diplexer board and assembled in the system. Commercial CMOS process is uses to fabricated the active chips, bonding wires will be employed to connect all the passive and active

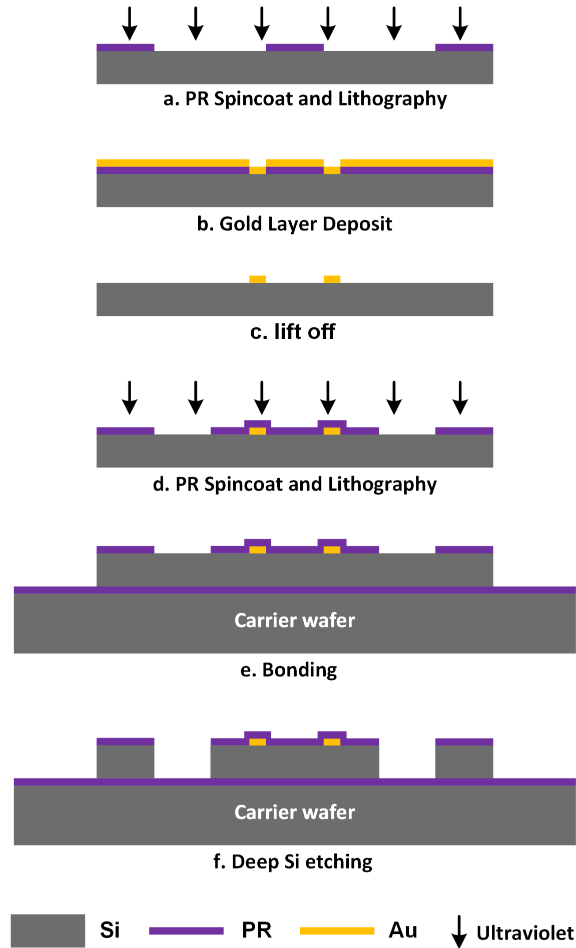


FIGURE 3.23. Si DWG fabrication

components. Bonding wire is extremely lossy at sub-THz/THz. therefore, making all components on the same altitude is helpful to reduce the length of bonding wires.

The first metal layers (50-nm Ti/300-nm Au) is deposited on the 300-μm thick Si wafer, then a thin-film layer is developed with BCB 4026-46. Then the second seed metal layer (50-nm Ti/300-nm Au) is deposited on top of the BCB layer. After that, diplexer and coupling structure (transition) are patterned with lithography process, Next step is electrical-plating to increase the thickness of the top golden layer. The pattern area is exposed and platted with 2-μm Au. At last, after etching back the seed layer and dicing the board, the diplexer boards are ready.

The Si DWG are fabricated with the deep reactive ion etching (DRIE) process, as shown in Figure 3.23. First a 4-inch Si wafer is patterned with a thick photoresist (AZ9260) layer. Since

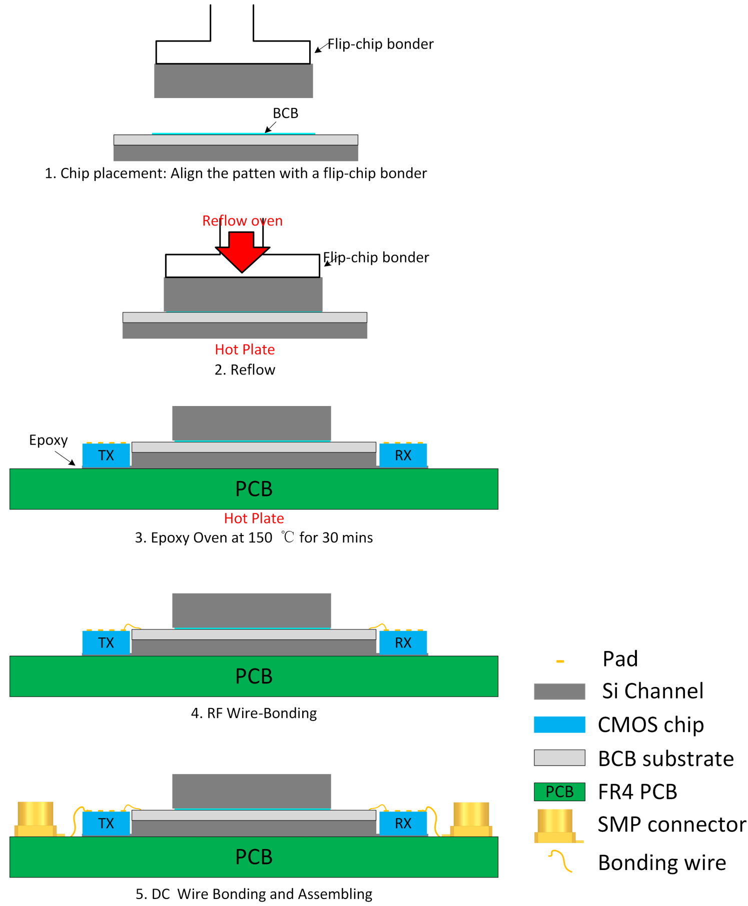


FIGURE 3.24. Dual-band sub-THz interconnect assembling

etching-through process is harmful to the chamber and not allowed in the DRIE machine, a 6-inch handle wafer is needed. Then, the 4-inch Si wafer is adhered on top of handle wafer (carrier wafer) that is also protected with thick AZ9260. The Si DWG can be saperated from wafer after deep Si etching process with an accurate shape patterned by the first step.

When all the components are ready, we can start to assemble the system. First step is bonding the channel to the diplexer board to form the dual-band channel. The alignment and bonding can be done very well with a pick-and-place tool (Finetech Fineplacer PICO A4). After this step, the dual-band channel can be tested individually. Next step is attaching the dual-band channel, transmitter and receiver to a mother PCB with epoxy and baking it at 150 $°C$ at least 30 minutes. After that is RF wire bonding that is the most critical and difficult step in the packaging process. Bonding wires are employed to connect signal at sub-THz, but they are extremely lossy at that frequency.

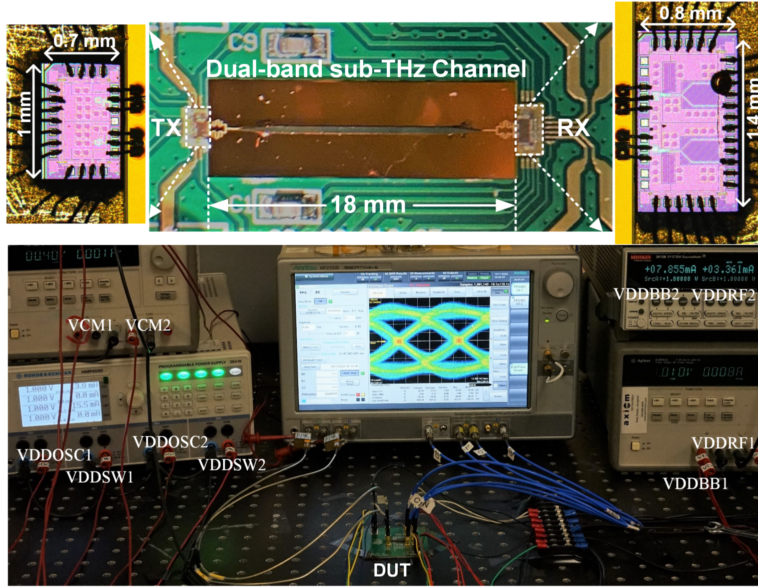


FIGURE 3.25. The photo of transmitter and receiver chipsets, system board and full-duplex measurement setup for the dual-band sub-THz interconnect

To minimize their effect, the bonding wires are kept as short as possible and the components heigh difference should be minimized. That is the reason why 300-μm thick Si wafer was used as a underneath carrier for the diplexer board, Furthermore, bonding wires are included in the package design to evaluate and compensate their effects. At last, the lumped elements components, such as capacitor, resistor, and SMP connector are assemble on the PCB. The dual-band sub-THz interconnect system photo is shown in Figure 3.25.

3.6. Measurement Results and Conclusion

3.6.1. Measurement setup and results.

The full-duplex testbench is setup to measure the dual-band sub-THz interconnect system, as shown in Figure 2.25. The carrier is generated by on-chip oscillator and non-coherent detection does not need phase synchronization. Therefore, the testbench for the proposed interconnect architecture is straightforward. DC supply, PRBS pattern generator and BERT/oscilloscope are sufficient to test the interconnect system. BER measurement is performed by Anritsu MP2011B. The $2^{31}-1$ PRBS pattern are generated as the test data, and data rate and eye diagrams are measured at the receivers' outputs. CH.1 and CH.2 are tested in full-duplex configuration and the maximum date

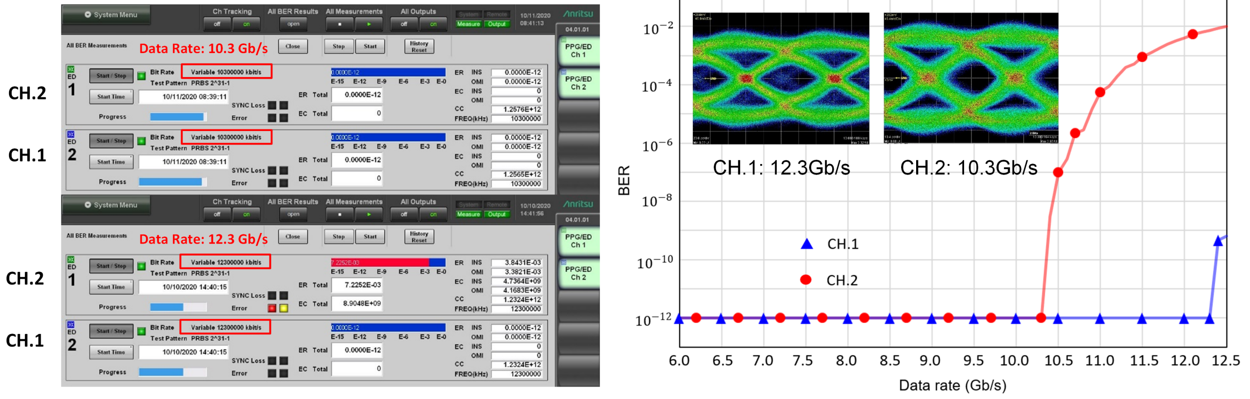


FIGURE 3.26. (a) Maximum error-free date rate and (b) the corresponding eye diagrams in full-duplex configuration

rate achieved with error free are up to 12.3 Gb/s and 10.3 Gb/s, respectively, as shown in Figure. The measured BER versus corresponding data rate with the inset eye diagrams at PRBS $2^{31} - 1$ and BER $< 1 \times 10^{-12}$ are plotted in Figure 3.26.

The power consumption at the maximum data rate are summarized as following: 15.5 mW for transmitter and 3.3 mW for receiver in CH.1, and 13.5 mW for transmitter and 3.2 mW for receiver in CH.2. The total power consumed by the proposed dual-band sub-THz interconnect system is 35.8 mW and the energy-efficiency is 1.58 pJ/b. Table 3.2 compares this work with the other state-of-the-art duplex sub-THz/THz interconnects.

3.6.2. Conclusion.

To boost interconnect data rate and bandwidth density, this paper demonstrates a full-duplex dual-band sub-THz interconnect, which is an implement of FDM scheme. A low-loss and wideband Si DWG coupled with a pair of diplexers is employed to support two highly isolated and low loss sub-channels simultaneously. The proposed sub-THz interconnect achieves the energy efficiency of 1.58 pJ/b with the aggregate data rate of 22.6 Gb/s and BER better than 1e-12. It demonstrates the record bandwidth density of 150.7 Gb/s/mm^2. Channelization provides a venue to boost the interconnect key metric of bandwidth density by taking full advantages of the abundant THz spectrum resource.

TABLE 3.2. Comparison of state-of-the-art duplex sub-THz/THz interconnect.

	JSSC'11 [45]	**JSSC'18 [57]**	**ICEIC'18 [19]**	**SPIE'19 [48]**	**This Work**
Tech.	40-nm CMOS	40-nm CMOS	40-nm CMOS	65-nm CMOS	65-nm CMOS
Concept	Full-Duplex	Half-Duplex	Signal-mode	Ortho-mode	Full-Duplex
Freq. (GHz)	57 & 80	120	73	165	140 & 180
Modulation	ASK	CP-FSK	ASK	OOK	OOK
CH. size (mm^2)	2	12.56	8	0.25	0.15
Distance (mm)	120	1000	1200	18.7	18
Data Rate (Gb/s)	25	6.2	14.3	15	22.6
Power (mW)	143	72.97	69	21.2	35.8
Energy effi. (pJ/b)	5.7	11.77	4.92	1.41	1.58
BW density (Gb/s/mm^2)	12.5	0.49	1.79	60	150.7
BER	1e-12	1e-12	1e-12	1e-12	1e-12
*** FOM1**	2.2	0.04	0.36	42.6	95.4
**** FOM2**	26.4	0.48	4.73	511.2	1144.8

CHAPTER 4

Theoretical Analysis and Demonstration of Multi-drop DWG

Chapter 2.4 presents three types of spatial multiplexers that we have investigated and demonstrated. Similar to FDM and polarization multiplexing, mode division multiplexing (MDM) has the same ptential to boost the total data rate and bandwidth density by creating more logical channels for the data transmission. Besides that, MDM has great scalability for larger port numbers and multi-dimensions that enables a data bus matrix at sub-THz/THz.

The mode-coupler based multi-drop Si DWG has been designed and Figure 2.31 depicts the detailed structure including MSL-to-DWG transitions on quartz boards. In this chapter, 4.1 drives the eigen modes in rectangular dielectric waveguides; 4.2 analyzes the waveguide mode directional coupler design, including mode coupling condition, coupling coefficient extraction, coupling efficiency maximization and verification. 4.3 introduce all the detailed building structures and the mechanism behind them. 4.4 shows the fabrication and measurement results.

The innovation of this chapter lies in the DWG mode coupler theoretical analysis and theory guided design of the multi-mode multi-drop channel. It is the first time to analyze the bandwidth and crosstalk for DWG mode couplers and qualitatively conclude the factors that impact bandwidth performance. The proposed tapered structures prove the theory and design approach correct and effective.

4.1. Mode in Rectangular DWGs

The multi-drop Si DWG uses a lot of rectangular, tapered, tip-shape and bended waveguides. To fully understand design logic and the mechanism, it is very necessary to drive the theory of the rectangular DWG. Metallic waveguides have strict boundary conditions that the E field on the conductor boundary must be zero, which makes the field distribution looks more regular. Unlike metallic waveguide, E and H field has more flexibility in DWGs and they are also distributed out of the waveguide with a decay ratio. That could be a two-edged sword: DWG is more sensitive

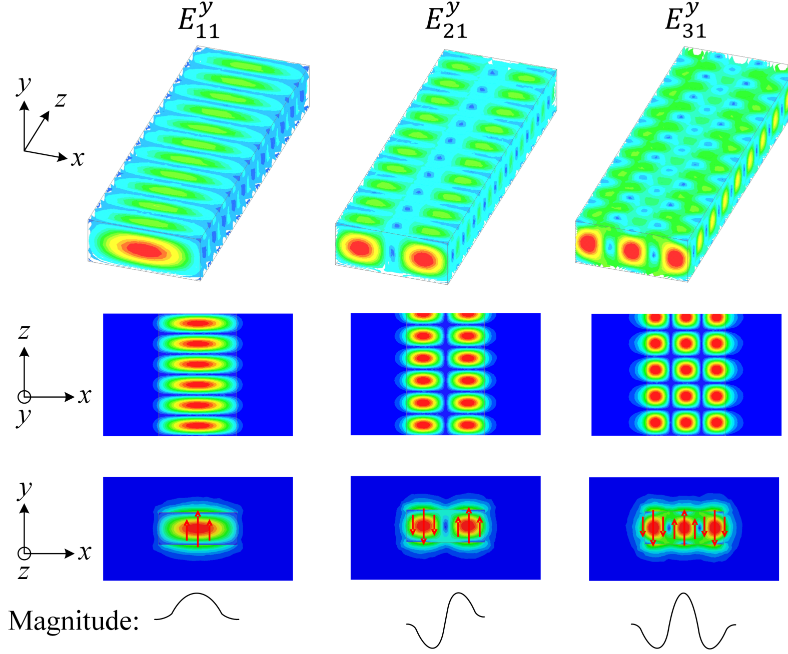


FIGURE 4.1. A multi-mode dielectric waveguide and its E field distribution and magnitude for E_{11}^{y}, E_{21}^{y} and E_{31}^{y} modes.

to the surroundings due to non-shielding and has a more complex eigen mode map; on the other hand, it allow coupling between different waveguides, components and modes. Figure 4.1 shows a multi-mode rectangular DWG and the E field distribution of three of the eigen modes (E_{11}^{y}, E_{21}^{y} and E_{31}^{y}) are plotted as well. For a given frequency,how many orders of mode could propagate in the waveguide is depended on the dimensions and effective refractive index difference between the core and cladding. Normally, larger dimensions allow higher order mode existing.

All the E and H field should follow the Maxwell's equations [**58**]

$$\begin{cases} \nabla \times \overrightarrow{\mathbf{E}} = -\mu_0 \dfrac{\partial \overrightarrow{\mathbf{H}}}{\partial t} \\ \nabla \times \overrightarrow{\mathbf{H}} = \varepsilon_0 \varepsilon_r \dfrac{\partial \overrightarrow{\mathbf{E}}}{\partial t} = \varepsilon_0 N^2 \dfrac{\partial \overrightarrow{\mathbf{E}}}{\partial t} \end{cases} \tag{4.1}$$

where $N^2 = \varepsilon_r$ is the refractive index distribution on the cross-section. Plane-wave propagation form is expressed as

$$\begin{cases} \overrightarrow{\mathbf{E}} = \mathbf{E}(x, y) e^{j(\omega t - \beta z)} \\ \overrightarrow{\mathbf{H}} = \mathbf{H}(x, y) e^{j(\omega t - \beta z)} \end{cases} \tag{4.2}$$

where $\mathbf{E}(x, y)$ and $\mathbf{H}(x, y)$ are the E field and H field profile in the cross-section. Substituting Eqn. (4.2) into Eqn. (4.1). The electromagnetic (E and H) field components can be obtained:

$$\begin{cases} \dfrac{\partial E_z}{\partial y} + j\beta E_y = -j\omega\mu_0 H_x \\ -j\beta E_x - \dfrac{\partial E_z}{\partial x} = -j\omega\mu_0 H_y \\ \dfrac{\partial E_y}{\partial x} - \dfrac{\partial E_x}{\partial y} = -j\omega\mu_0 H_z \end{cases} \tag{4.3}$$

$$\begin{cases} \dfrac{\partial H_z}{\partial y} + j\beta H_y = j\omega\varepsilon_0 N^2 E_x \\ -j\beta H_x - \dfrac{\partial H_z}{\partial x} = j\omega\varepsilon_0 N^2 E_y \\ \dfrac{\partial H_y}{\partial x} - \dfrac{\partial H_x}{\partial y} = j\omega\varepsilon_0 N^2 E_z \end{cases} \tag{4.4}$$

We care more about the electromagnetic modes E_y in which E_y and H_x are predominant. (Similarly, E_x and H_y are predominant in E_x). Using the Marcatili's method approximate [**59**] $H_y = 0$ in Eqn. (4.3) and Eqn. (4.4), the equations can be simplified as:

$$\begin{cases} \dfrac{\partial E_z}{\partial y} + j\beta E_y = -j\omega\mu_0 H_x \\ -j\beta E_x - \dfrac{\partial E_z}{\partial x} = 0 \\ \dfrac{\partial E_y}{\partial x} - \dfrac{\partial E_x}{\partial y} = -j\omega\mu_0 H_z \end{cases} \tag{4.5}$$

$$\begin{cases} \dfrac{\partial H_z}{\partial y} = j\omega\varepsilon_0 N^2 E_x \\ -j\beta H_x - \dfrac{\partial H_z}{\partial x} = j\omega\varepsilon_0 N^2 E_y \\ -\dfrac{\partial H_x}{\partial y} = j\omega\varepsilon_0 N^2 E_z \end{cases} \tag{4.6}$$

From Eqn. (4.6), E field components are

$$\begin{cases} E_x = \dfrac{1}{j\omega\varepsilon_0 N^2}\dfrac{\partial H_z}{\partial y} \\ E_y = \dfrac{1}{j\omega\varepsilon_0 N^2}\left(-j\beta H_x - \dfrac{\partial H_z}{\partial x}\right) \\ E_z = -\dfrac{1}{j\omega\varepsilon_0 N^2}\dfrac{\partial H_x}{\partial y} \end{cases} \tag{4.7}$$

Plugging Eqn. (4.7) into Eqn. (4.5), the H field components are

$$\begin{cases} -\dfrac{\partial^2 H_x}{\partial y^2} + \beta^2 H_x - j\beta \dfrac{\partial H_z}{\partial x} = \omega^2 \varepsilon_0 \mu_0 N^2 H_x = k_0^2 N^2 H_x \\ -j\beta \dfrac{\partial H_z}{\partial x} - \dfrac{\partial^2 H_x}{\partial x^2} = 0 \\ -j\beta \dfrac{\partial H_x}{\partial x} - \dfrac{\partial^2 H_z}{\partial x^2} - \dfrac{\partial^2 H_z}{\partial y^2} = \omega^2 \varepsilon_0 \mu_0 N^2 H_z = k_0^2 N^2 H_z \end{cases} \tag{4.8}$$

By arranging the first and second equations in Eqn. (4.8), a second-order partial differential in term of H_x is obtained:

$$\frac{\partial^2 H_x}{\partial x^2} + \frac{\partial^2 H_x}{\partial y^2} + (k_0^2 N^2 - \beta^2) H_x = 0, \ (\beta = k_z) \tag{4.9}$$

All other E and H field components are calculated in respect to H_x. From Eqn. (4.7.3)

$$E_z = -\frac{1}{j\omega\varepsilon_0 N^2} \frac{\partial H_x}{\partial y} \tag{4.10}$$

From Eqn. (4.5.2)

$$E_x = -\frac{1}{j\beta} \frac{\partial E_z}{\partial x} = -\frac{1}{\omega\varepsilon_0 N^2 \beta} \frac{\partial^2 H_x}{\partial x \partial y} \tag{4.11}$$

From Eqn. (4.5.1)

$$E_y = -\frac{\omega\mu_0}{\beta} H_x - \frac{1}{j\beta} \frac{\partial E_z}{\partial y} = -\frac{\omega\mu_0}{\beta} H_x - \frac{1}{\omega\varepsilon_0 N^2 \beta} \frac{\partial^2 H_x}{\partial y^2} \tag{4.12}$$

From Eqn. (4.5.3)

$$\begin{aligned} H_z &= -\frac{1}{j\omega\mu_0} \left(\frac{\partial E_y}{\partial x} - \frac{\partial E_x}{\partial y} \right) \\ &= -\frac{1}{j\omega\mu_0} \left(-\frac{\omega\mu_0}{\beta} \frac{\partial H_x}{\partial x} - \frac{1}{\omega\varepsilon_0 N^2 \beta} \frac{\partial^3 H_x}{\partial x \partial y^2} + \frac{1}{\omega\varepsilon_0 N^2 \beta} \frac{\partial^3 H_x}{\partial x \partial y^2} \right) \\ &= -\frac{j}{\beta} \frac{\partial H_x}{\partial x} \end{aligned} \tag{4.13}$$

The wave equation of H_x and E and H field components representation are given by

$$\frac{\partial^2 H_x}{\partial x^2} + \frac{\partial^2 H_x}{\partial y^2} + (k_0^2 N^2 - \beta^2) H_x = 0, \ (\beta = k_z) \tag{4.14}$$

$$\begin{cases} H_y = 0 \\ H_z = -\dfrac{j}{\beta}\dfrac{\partial H_x}{\partial x} \\ E_x = -\dfrac{1}{\omega\varepsilon_0 N^2\beta}\dfrac{\partial^2 H_x}{\partial x \partial y} \\ E_y = -\dfrac{\omega\mu_0}{\beta}H_x - \dfrac{1}{\omega\varepsilon_0 N^2\beta}\dfrac{\partial^2 H_x}{\partial y^2} \\ E_z = -\dfrac{j}{\omega\varepsilon_0 N^2}\dfrac{\partial H_x}{\partial y} \end{cases} \tag{4.15}$$

Then, we need to solve the second-order partial differential equations (PDE) of H_x and calculate all other EM filed components in a rectangular DWG. The H_x equation is not a transitional Laplace equitation. Second-order PDEs solving is very difficult and there are multiple solutions. We can start with a simple second-order derivative equation as an example.

$$y(x)^{"} + ay(x) = 0 \tag{4.16}$$

When $a > 0$

$$y = C_1 \cos(\sqrt{a}x) + C_2 \sin(\sqrt{a}x) \tag{4.17}$$

When $a < 0$

$$y = C_1 e^{\sqrt{-a}x} + C_2 e^{-\sqrt{-a}x} \tag{4.18}$$

The second-order PDE of H_x can be separated into two second-order PDEs by arranging the linear term, as shown in Eqn. (4.19). The solution of H_x can be the product of the solutions to the separated second-order PDEs. In a propagating waveguide, $k_0 n_1 > \beta$, and out of the waveguide $k_0 n_0 < \beta$, the wavenumber relation is shown in Figure 4.3, which is $k_0^2 n_1^2 - \beta^2 = k_c^2 = k_x^2 + k_y^2$. Since region 2 and region 3 have two identical symmetric area, we only calculate the right an upper ones and extend the solutions to the whole crosssection.

$$\frac{\partial^2 H_x}{\partial x^2} + \frac{\partial^2 H_x}{\partial y^2} + (k_0^2 N^2 - \beta^2) H_x = 0 \tag{4.19}$$

(1) Therefore, inside the waveguide (region 1 in Figure 4.2): $k_0 n_1 > \beta$

$$\frac{\partial^2 H_x}{\partial x^2} + k_x^2 H_x + \frac{\partial^2 H_x}{\partial y^2} + k_y^2 H_x = 0 \tag{4.20}$$

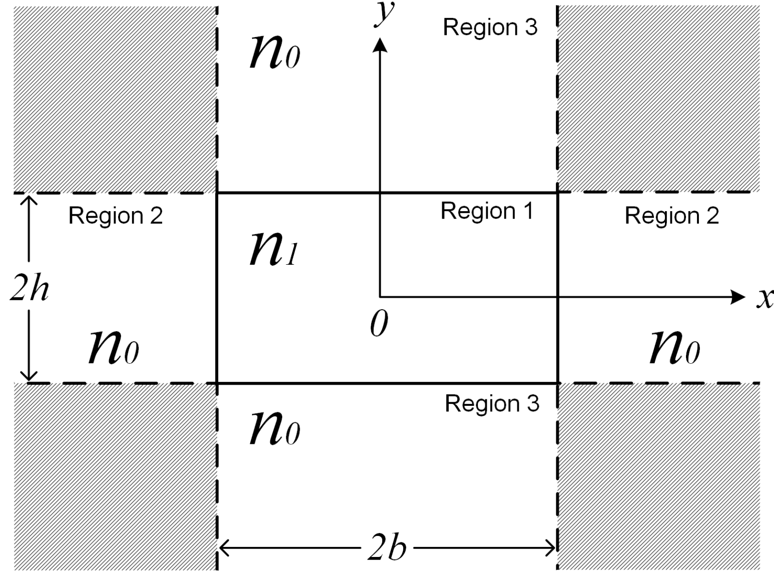


FIGURE 4.2. Cross-section and dimensions of a rectangular DWG

The general solution of H_x in region 1 is

$$H_x = [C_1 \cos(k_x x) + C_2 \sin(k_x x)] [C_3 \cos(k_y y) + C_4 \sin(k_y y)] \tag{4.21}$$

where $C_1, C_2, ...$ can be any real numbers.

(2) Out of the waveguide (region 2 and 3 in Figure 4.2): $k_0 n_0 < \beta$

We define a new variable α that can be calculated with $k_0^2 n_0^2 - \beta^2 = -\alpha_x^2 + k_y^2$ in region 2 and $k_0^2 n_0^2 - \beta^2 = -\alpha_y^2 + k_x^2$, respectively. $j\alpha$, k_x and k_y are regarded as wavenumbers.

The general solution of H_x in region 2 is

$$H_x = [C_1 \cos(k_y y) + C_2 \sin(k_y y)] \left[C_3 e^{\alpha_x(|x|-b)} + C_4 e^{-\alpha_x(|x|-b)}\right] \tag{4.22}$$

and the general solution of H_x in region 3 is

$$H_x = [C_1 \cos(k_x x) + C_2 \sin(k_x x)] \left[C_3 e^{\alpha_y(|y|-h)} + C_4 e^{-\alpha_y(|y|-h)}\right] \tag{4.23}$$

where $C_1, C_2, ...$ can be any real numbers.

However, not all the solutions solved from the derivative equations can satisfy the waveguide mode characteristics in a rectangular DWG. The choice of the standing-wave solutions $\cos(kx + \Phi)$

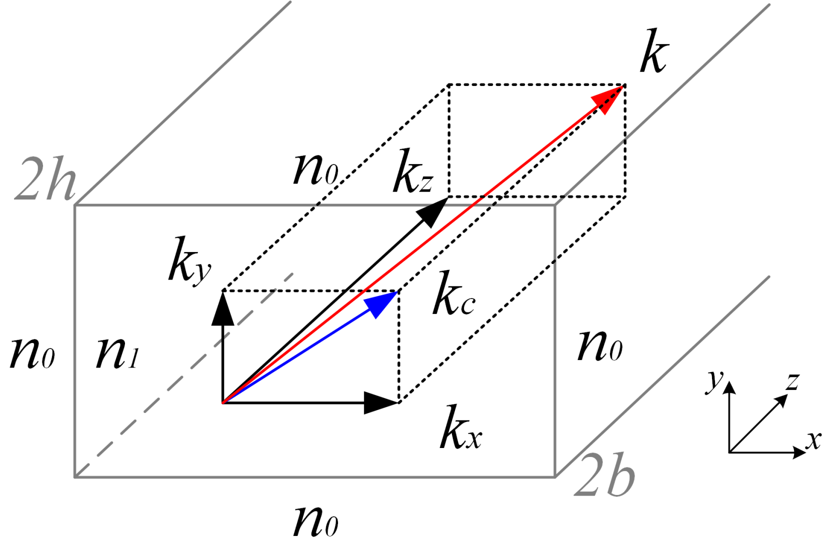


FIGURE 4.3. Wavenumber Relation in a Rectangular Waveguide

inside the waveguide and decaying solutions out of the waveguide is made. Therefore,

$$H_x = \begin{cases} A_1 \cos(k_x x - \Phi_x)\cos(k_y y - \Phi_y), & region\ 1\ (|x| < b,\ |y| < h) \\ A_2 \cos(k_y y - \Phi_y) e^{-\alpha_x(|x|-b)}, & region\ 2\ (|x| > b,\ |y| < h) \\ A_3 \cos(k_x x - \Phi_x) e^{-\alpha_y(|y|-h)}, & region\ 3\ (|x| < b,\ |y| > h) \end{cases} \tag{4.24}$$

$$where, \begin{cases} \Phi_x = (p-1)\dfrac{\pi}{2}, & p = 1, 2, ..., \infty \\ \Phi_y = (q-1)\dfrac{\pi}{2}, & q = 1, 2, ..., \infty \end{cases} \tag{4.25}$$

Because both sin and cos can satisfy the mode solutions, the solutions contain Φ_x and Φ_y in phase of multiple $\frac{\pi}{2}$ to make the solution comprehensive. H_x is continuous at the boundary:

(1) When x=b,

$$A_1 \cos(k_x b - \Phi_x)\cos(k_y y - \Phi_y) = A_2 \cos(k_y y - \Phi_y) e^{-\alpha_x(|b|-b)} \tag{4.26}$$

So, $A_1 \cos(k_x b - \Phi_x) = A_2$.

(2) When y=h,

$$A_1 \cos(k_x x - \Phi_x)\cos(k_y h - \Phi_y) = A_3 \cos(k_x x - \Phi_x) e^{-\alpha_y(|h|-h)} \tag{4.27}$$

So, $A_1 \cos(k_y h - \Phi_y) = A_3$.

Therefore, we can conclude the dispersion equations (or Eigenvalue Equation) for E^y_{pq} as,

$$H_x = \begin{cases} A\cos(k_x x - \Phi_x)\cos(k_y y - \Phi_y), & region\ 1\ (|x| < b,\ |y| < h) \\ A\cos(k_x b - \Phi_x)e^{-\alpha_x(|x|-b)}\cos(k_y y - \Phi_y), & region\ 2\ (|x| > b,\ |y| < h) \\ A\cos(k_x x - \Phi_x)e^{-\alpha_y(|y|-h)}\cos(k_y h - \Phi_y), & region\ 3\ (|x| < b,\ |y| > h) \end{cases} \tag{4.28}$$

The transverse wavenumber in region 1,2 and 3 are safisfying

$$\begin{cases} -k_x^2 - k_y^2 - \beta_z^2 + k_0^2 n_1^2 = 0, & region\ 1\ (|x| < b,\ |y| < h) \\ \alpha_x^2 - k_y^2 - \beta_z^2 + k_0^2 n_0^2 = 0, & region\ 2\ (|x| > b,\ |y| < h) \\ -k_x^2 + \alpha_y^2 - \beta_z^2 + k_0^2 n_0^2 = 0, & region\ 3\ (|x| < b,\ |y| > h) \end{cases} \tag{4.29}$$

$$where,\ \begin{cases} \Phi_x = (p-1)\frac{\pi}{2}, & p = 1, 2, ..., \infty \\ \Phi_y = (q-1)\frac{\pi}{2}, & q = 1, 2, ..., \infty \end{cases} \tag{4.30}$$

Then all the field can be calculated based on the solved H_x

$$\begin{aligned} H_z &= -\frac{j}{\beta}\frac{\partial H_x}{\partial x} \\ &= \begin{cases} \frac{jAk_x}{\beta}\sin(k_x x - \Phi_x)\cos(k_y y - \Phi_y), & region\ 1\ (|x| < b,\ |y| < h) \\ \frac{jA\alpha_x}{\beta}\cos(k_x b - \Phi_x)\cos(k_y y - \Phi_y)e^{-\alpha_x(|x|-b)}, & region\ 2\ (|x| > b,\ |y| < h) \\ \frac{jAk_x}{\beta}\sin(k_x x - \Phi_x)\cos(k_y h - \Phi_y)e^{-\alpha_y(|y|-h)}, & region\ 3\ (|x| < b,\ |y| > h) \end{cases} \end{aligned} \tag{4.31}$$

$$\begin{aligned} E_x &= -\frac{1}{\omega\varepsilon_0 N^2 \beta}\frac{\partial^2 H_x}{\partial x \partial y} \\ &= \begin{cases} -\frac{Ak_x k_y}{\omega\varepsilon_0 N^2\beta}\sin(k_x x - \Phi_x)\sin(k_y y - \Phi_y), & region\ 1\ (|x| < b,\ |y| < h) \\ -\frac{A\alpha_x k_y}{\omega\varepsilon_0 N^2\beta}\cos(k_x b - \Phi_x)\sin(k_y y - \Phi_y)e^{-\alpha_x(|x|-b)}, & region\ 2\ (|x| > b,\ |y| < h) \\ \frac{Ak_x\alpha_y}{\omega\varepsilon_0 N^2\beta}\sin(k_x x - \Phi_x)\cos(k_y h - \Phi_y)e^{-\alpha_y(|y|-h)}, & region\ 3\ (|x| < b,\ |y| > h) \end{cases} \end{aligned} \tag{4.32}$$

$$E_y = -\frac{\omega\mu_0}{\beta}H_x - \frac{1}{\omega\varepsilon_0 N^2\beta}\frac{\partial^2 H_x}{\partial y^2} \approx -\frac{\omega\mu_0}{\beta}H_x$$

$$= \begin{cases} -\dfrac{A\omega\mu_0}{\beta}\cos(k_x x - \Phi_x)\cos(k_y y - \Phi_y), & \textit{region } 1\ (|x| < b,\ |y| < h) \\ -\dfrac{A\omega\mu_0}{\beta}\cos(k_x b - \Phi_x)e^{-\alpha_x(|x|-b)}\cos(k_y y - \Phi_y), & \textit{region } 2\ (|x| > b,\ |y| < h) \\ -\dfrac{A\omega\mu_0}{\beta}\cos(k_x x - \Phi_x)e^{-\alpha_y(|y|-h)}\cos(k_y h - \Phi_y), & \textit{region } 3\ (|x| < b,\ |y| > h) \end{cases} \tag{4.33}$$

$$E_z = -\frac{j}{\omega\varepsilon_0 N^2}\frac{\partial H_x}{\partial y}$$

$$= \begin{cases} \dfrac{jAk_y}{\omega\varepsilon_0 N^2}\cos(k_x x - \Phi_x)\sin(k_y y - \Phi_y), & \textit{region } 1\ (|x| < b,\ |y| < h) \\ \dfrac{jAk_y}{\omega\varepsilon_0 N^2}\cos(k_x b - \Phi_x)\sin(k_y y - \Phi_y)e^{-\alpha_x(|x|-b)}, & \textit{region } 2\ (|x| > b,\ |y| < h) \\ \dfrac{jA\alpha_y}{\omega\varepsilon_0 N^2}\cos(k_x x - \Phi_x)\cos(k_y h - \Phi_y)e^{-\alpha_y(|y|-h)}, & \textit{region } 3\ (|x| < b,\ |y| > h) \end{cases} \tag{4.34}$$

The boundary conditions that the magnetic field H_z should be continuous at $|x| = b$ and the electric field E_z should be continuous $|y| = h$.

(1) At the boundary of region 1 and 2 ($|x| = b$), H_z should be continuous.

$$\frac{jAk_x}{\beta}\sin(k_x b - \Phi_x)\cos(k_y y - \Phi_y) = \frac{jA\alpha_x}{\beta}\cos(k_x b - \Phi_x)\cos(k_y y - \Phi_y)e^{-\alpha_x(|b|-b)} \tag{4.35}$$

$$\tan(k_x b - \Phi_x) = \frac{\alpha_x}{k_x} \tag{4.36}$$

$$k_x b = (p-1)\frac{\pi}{2} + \tan^{-1}\frac{\alpha_x}{k_x} \tag{4.37}$$

(2) At the boundary of region 1 and 3 ($|y| = h$), E_z should be continuous.

$$\frac{jAk_y}{\omega\varepsilon_0 n_1^2}\cos(k_x x - \Phi_x)\sin(k_y h - \Phi_y) = \frac{jA\alpha_y}{\omega\varepsilon_0 n_0^2}\cos(k_x x - \Phi_x)\cos(k_y h - \Phi_y)e^{-\alpha_y(|h|-h)} \tag{4.38}$$

$$\tan(k_y h - \Phi_y) = \frac{n_1^2\alpha_y}{n_0^2 k_y} \tag{4.39}$$

$$k_y h = (q-1)\frac{\pi}{2} + \tan^{-1}\frac{n_1^2\alpha_y}{n_0^2 k_y} \tag{4.40}$$

The phase condition for E^y_{pq} mode in a rectangular DWG:

$$\begin{cases} k_x b = (p-1)\dfrac{\pi}{2} + \tan^{-1}\left(\dfrac{\alpha_x}{k_x}\right) \\ k_y h = (q-1)\dfrac{\pi}{2} + \tan^{-1}\left(\dfrac{n_1^2 \alpha_y}{n_0^2 k_y}\right) \end{cases} \tag{4.41}$$

Different books may derive slightly different solutions of the EM filed and mode condition, because the calculations are based on different assumptions and approximations. The derivation in this section makes approximations as well, for example, the higher-order derivatives in E_x and E_y in Eqn. (4.15) are ignored.

4.2. Directional Mode Coupler

The EM wave field and E^y_{pq} mode condition have been discussed in section 4.1. This section continues to investigate DWG directional mode couplers. For a mode coupler, the most critical metrics are the coupling coefficient and coupling efficiency. Building the link between metrics and design parameters can efficiently guide the design and optimization.

4.2.1. Mode Coupling Condition.

For the construction of practical optical devices, it is very important to utilize the mutual lightwave interaction between the two copropagating light beams in the adja- cent waveguides or interaction between the contrapropagating two beams in the corrugated optical waveguides. Coupled mode theory deals with the mutual light- wave interactions between the two propagation modes. In this chapter derivation of coupled mode equations based on perturbation theory is first presented and then concrete methods calculating the coupling coefficients for several prac- tically important devices are explained in detail. Finally, several waveguide devices using directional couplers such as Mach–Zehnder interferometers, ring resonators, and bistable devices are described.

The wave coupling can happen when the unshielded DWGs are close-by. Figure 4.4 also describes the coupling mechanism between the same or different modes. The requirements for mode coupling include field overlap and phase matching. Field overlap means DWGs are close enough so that the EM field of each waveguide is interacting. Phase matching requires that the propagation constant β, which is the wavenumber along propagation direction, are equal for the coupling modes.

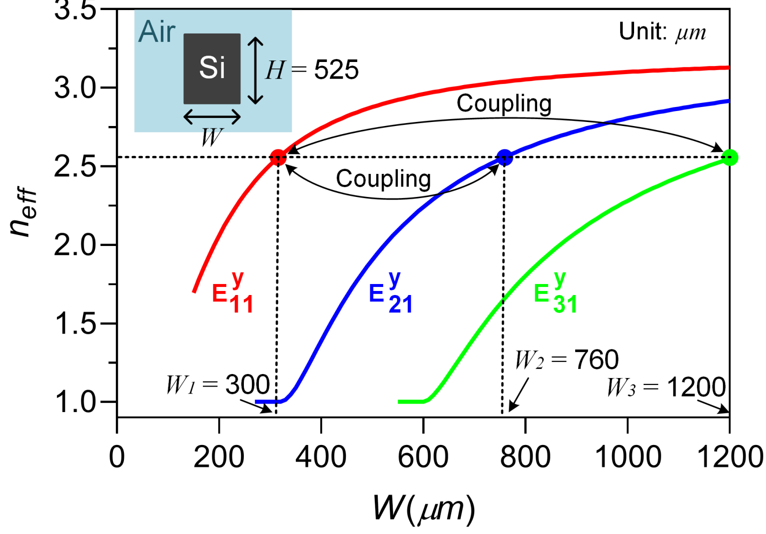


FIGURE 4.4. Simulated effective refractive index n_{eff} for the three modes (E^y_{11}, E^y_{21} and E^y_{31}) in Si DWG versus waveguide width at 165 GHz

By precisely controlling the width of DWG, the n_{eff} of a specific mode can be finely tuned, then it is possible to make two modes phase matched according to the Eqn. (4.42).

$$\beta = k_z = n_{eff}\frac{\omega}{c} \tag{4.42}$$

4.2.2. Mode Coupling Coefficient.

In a waveguide mode coupler, the coupling coefficient is the first parameter need to calculate, because it directly determines the optimum coupler length and maximum coupling efficiency. Besides that, the mathematical expression of coupling coefficient is the guideline to optimize the coupler dimensions, such as the waveguide width and gap. A critical assumption based on perturbation theory [**60**] is made: the total E and H field is the sum of the field in each individual waveguide, as described in Eqn. (4.43). This is the most important assumption for the derivation of coupling coefficient.

$$\begin{cases} \overrightarrow{\mathbf{E}} = A(z)\overrightarrow{\mathbf{E}}_1 + B(z)\overrightarrow{\mathbf{E}}_2 \\ \overrightarrow{\mathbf{H}} = A(z)\overrightarrow{\mathbf{H}}_1 + B(z)\overrightarrow{\mathbf{H}}_2 \end{cases} \tag{4.43}$$

Both the total EH filed ($\overrightarrow{\mathbf{E}}$ and $\overrightarrow{\mathbf{H}}$) and individual EH field ($\overrightarrow{\mathbf{E}}_1$, $\overrightarrow{\mathbf{E}}_2$, $\overrightarrow{\mathbf{H}}_1$, and $\overrightarrow{\mathbf{H}}_2$) should have the same coefficient and satisfy the Maxwell's Equations (4.1) and the vector formula below.

$$\begin{aligned}\nabla \times [A(z)\overrightarrow{\mathbf{E}}] &= A(z)\nabla \times \overrightarrow{\mathbf{E}} + \nabla \times A(z)\overrightarrow{\mathbf{E}} \\ &= A(z)\nabla \times \overrightarrow{\mathbf{E}} + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{E}}\end{aligned} \tag{4.44}$$

(1) Substituting the E field expression in Eqn. (4.43) into Eqn. (4.44).

$$\begin{aligned}\nabla \times \overrightarrow{\mathbf{E}} &= \nabla \times [A(z)\overrightarrow{\mathbf{E}}_1] + \nabla \times [B(z)\overrightarrow{\mathbf{E}}_2] \\ &= A(z)\nabla \times \overrightarrow{\mathbf{E}}_1 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{E}}_1 + B(z)\nabla \times \overrightarrow{\mathbf{E}}_2 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{E}}_2 \\ &= -j\omega\mu_0 A(z)\overrightarrow{\mathbf{H}}_1 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{E}}_1 - j\omega\mu_0 B(z)\overrightarrow{\mathbf{H}}_2 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{E}}_2\end{aligned} \tag{4.45}$$

And, $\nabla \times \overrightarrow{\mathbf{E}}$ also equals to

$$\begin{aligned}\nabla \times \overrightarrow{\mathbf{E}} &= -j\omega\mu_0\overrightarrow{\mathbf{H}} \\ &= -j\omega\mu_0 A(z)\overrightarrow{\mathbf{H}}_1 - j\omega\mu_0 B(z)\overrightarrow{\mathbf{H}}_2\end{aligned} \tag{4.46}$$

From Eqn. (4.45) and Eqn. (4.46)

$$\frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{E}}_1 + \frac{dB(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{E}}_2 = 0 \tag{4.47}$$

(2) Substituting the H field expression in Eqn. (4.43) into Eqn. (4.44).

$$\begin{aligned}\nabla \times \overrightarrow{\mathbf{H}} &= \nabla \times [A(z)\overrightarrow{\mathbf{H}}_1] + \nabla \times [B(z)\overrightarrow{\mathbf{H}}_2] \\ &= A(z)\nabla \times \overrightarrow{\mathbf{H}}_1 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{H}}_1 + B(z)\nabla \times \overrightarrow{\mathbf{H}}_2 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{H}}_2 \\ &= j\omega\varepsilon_0 N_1^2 A(z)\overrightarrow{\mathbf{E}}_1 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{H}}_1 + j\omega\varepsilon_0 N_2^2 B(z)\overrightarrow{\mathbf{E}}_2 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{H}}_2\end{aligned} \tag{4.48}$$

And, $\nabla \times \overrightarrow{\mathbf{H}}$ also equals to

$$\begin{aligned}\nabla \times \overrightarrow{\mathbf{H}} &= j\omega\varepsilon_0 N^2\overrightarrow{\mathbf{E}} \\ &= j\omega\varepsilon_0 N^2 A(z)\overrightarrow{\mathbf{E}}_1 + j\omega\varepsilon_0 N^2 B(z)\overrightarrow{\mathbf{E}}_2\end{aligned} \tag{4.49}$$

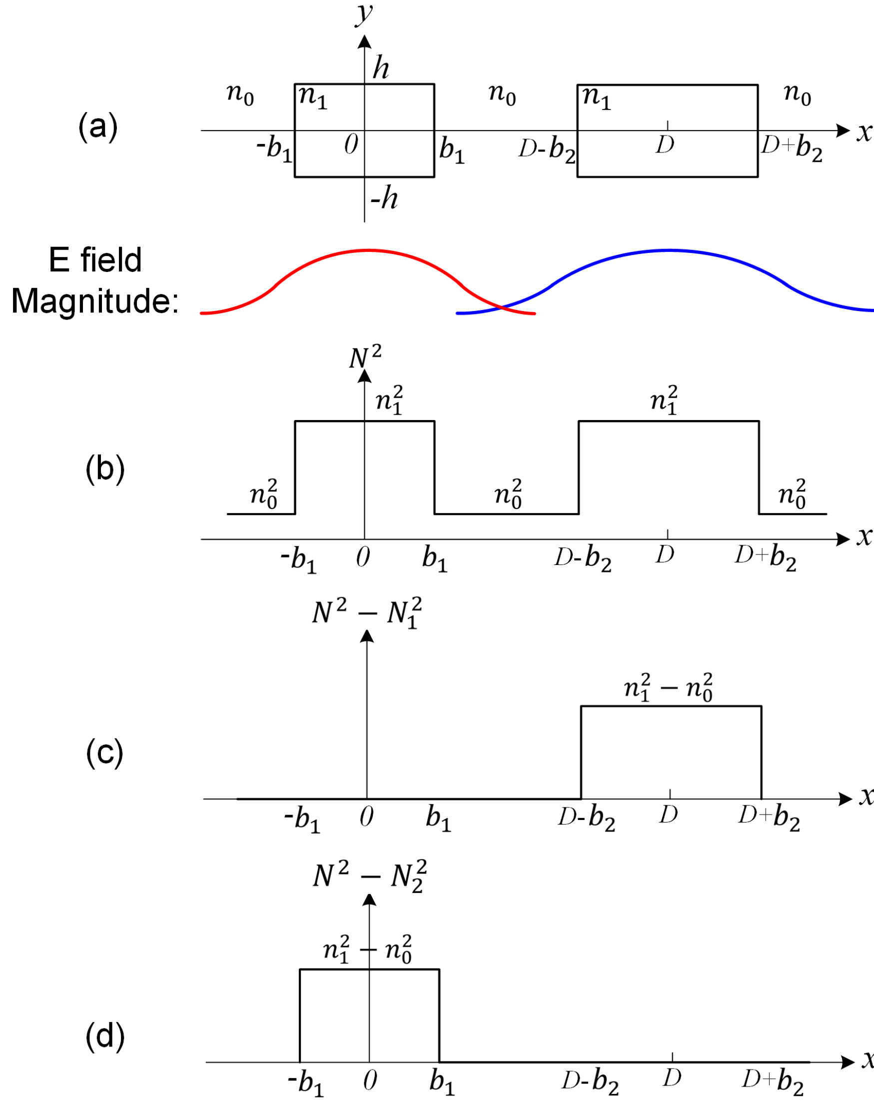


FIGURE 4.5. (a) Cross-section and E field profiles of a rectangular DWG coupler. (b) Refractive index distribution N^2, (c) $N^2 - N_1^2$ and (d) $N^2 - N_2^2$

From Eqn. (4.48) and (4.49)

$$
\begin{aligned}
&- j\omega\varepsilon_0(N^2 - N_1^2)A(z)\overrightarrow{\mathbf{E}}_1 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{H}}_1 \\
&- j\omega\varepsilon_0(N^2 - N_2^2)B(z)\overrightarrow{\mathbf{E}}_2 + \frac{dA(z)}{dz}\mathbf{u}_z \times \overrightarrow{\mathbf{H}}_2 = 0
\end{aligned}
\tag{4.50}
$$

$N^2(x, y)$ is the refractive-index distribution in the entire coupled waveguide, as shown in Figure 4.5. The coupling is majorly along x axis. To simplify the calculation, the refractive-index is set

constant in term of y. Substituting Eqn. (4.47) and (4.50) into the following integral equations.

$$\begin{cases} \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\left[\overrightarrow{\mathbf{E}}_1^*\cdot(4.50)-\overrightarrow{\mathbf{H}}_1^*\cdot(4.47)\right]=0 \\ \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\left[\overrightarrow{\mathbf{E}}_2^*\cdot(4.50)-\overrightarrow{\mathbf{H}}_2^*\cdot(4.47)\right]=0 \end{cases} \tag{4.51}$$

The reason we employ $\overrightarrow{\mathbf{E}}_1^*\cdot(4.50)-\overrightarrow{\mathbf{H}}_1^*\cdot(4.47)=0$ is to form special items, such as the Poynting Vector $\overrightarrow{\mathbf{E}}\times\overrightarrow{\mathbf{H}}^*$ and E field interacting term $\overrightarrow{\mathbf{E}}_1\cdot\overrightarrow{\mathbf{E}}_2^*$, and build relation between those items.

Substituting (4.47) and (4.50) into the integral equations (4.51)

$$\begin{aligned} I_1=\overrightarrow{\mathbf{E}}_1^*\cdot(4.50)-\overrightarrow{\mathbf{H}}_1^*\cdot(4.47)=&\frac{dA(z)}{dz}\left[\overrightarrow{\mathbf{E}}_1^*\cdot(\mathbf{u}_z\times\overrightarrow{\mathbf{H}}_1)-\overrightarrow{\mathbf{H}}_1^*\cdot\mathbf{u}_z\times(\overrightarrow{\mathbf{E}}_1)\right] \\ &+\frac{dB(z)}{dz}\left[\overrightarrow{\mathbf{E}}_1^*\cdot(\mathbf{u}_z\times\overrightarrow{\mathbf{H}}_2)-\overrightarrow{\mathbf{H}}_1^*\cdot\mathbf{u}_z\times(\overrightarrow{\mathbf{E}}_2)\right] \\ -j\omega\varepsilon_0A(z)((N^2-N_1^2))\overrightarrow{\mathbf{E}}_1^*\cdot\overrightarrow{\mathbf{E}}_1&-j\omega\varepsilon_0B(z)((N^2-N_2^2))\overrightarrow{\mathbf{E}}_1^*\cdot\overrightarrow{\mathbf{E}}_2 \end{aligned} \tag{4.52}$$

We use the following vector formulas to arrange the Eqn (4.52):

$$\begin{cases} \overrightarrow{\mathbf{E}}_1^*\cdot(\mathbf{u}_z\times\overrightarrow{\mathbf{H}}_1)=-\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_1^*\times\overrightarrow{\mathbf{H}}_1) \\ \overrightarrow{\mathbf{H}}_1^*\cdot(\mathbf{u}_z\times\overrightarrow{\mathbf{E}}_1)=\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_1^*\times\overrightarrow{\mathbf{H}}_1) \end{cases} \tag{4.53}$$

$$\begin{aligned} I_1=&-\frac{dA(z)}{dz}\mathbf{u}_z\cdot\left[\overrightarrow{\mathbf{E}}_1^*\times\overrightarrow{\mathbf{H}}_1-\overrightarrow{\mathbf{E}}_1\times\overrightarrow{\mathbf{H}}_1^*\right]-\frac{dB(z)}{dz}\mathbf{u}_z\cdot\left[\overrightarrow{\mathbf{E}}_1^*\times\overrightarrow{\mathbf{H}}_2-\overrightarrow{\mathbf{E}}_2\times\overrightarrow{\mathbf{H}}_1^*\right] \\ &-j\omega\varepsilon_0A(z)((N^2-N_1^2))\overrightarrow{\mathbf{E}}_1^*\cdot\overrightarrow{\mathbf{E}}_1-j\omega\varepsilon_0B(z)((N^2-N_2^2))\overrightarrow{\mathbf{E}}_1^*\cdot\overrightarrow{\mathbf{E}}_2 \end{aligned} \tag{4.54}$$

Similarly, the other integral equation can be calculated as well.

$$\begin{aligned} I_2=\overrightarrow{\mathbf{E}}_2^*\cdot(4.50)-\overrightarrow{\mathbf{H}}_2^*\cdot(4.47)=&\frac{dA(z)}{dz}\left[\overrightarrow{\mathbf{E}}_2^*\cdot(\mathbf{u}_z\times\overrightarrow{\mathbf{H}}_1)-\overrightarrow{\mathbf{H}}_2^*\cdot\mathbf{u}_z\times(\overrightarrow{\mathbf{E}}_1)\right] \\ &+\frac{dB(z)}{dz}\left[\overrightarrow{\mathbf{E}}_2^*\cdot(\mathbf{u}_z\times\overrightarrow{\mathbf{H}}_2)-\overrightarrow{\mathbf{H}}_2^*\cdot\mathbf{u}_z\times(\overrightarrow{\mathbf{E}}_2)\right] \\ -j\omega\varepsilon_0A(z)((N^2-N_1^2))\overrightarrow{\mathbf{E}}_2^*\cdot\overrightarrow{\mathbf{E}}_1&-j\omega\varepsilon_0B(z)((N^2-N_2^2))\overrightarrow{\mathbf{E}}_2^*\cdot\overrightarrow{\mathbf{E}}_2 \end{aligned} \tag{4.55}$$

Then arranging (4.55) with vector formulas (4.53)

$$\begin{aligned} I_2=&-\frac{dA(z)}{dz}\mathbf{u}_z\cdot\left[\overrightarrow{\mathbf{E}}_2^*\times\overrightarrow{\mathbf{H}}_1+\overrightarrow{\mathbf{E}}_1\times\overrightarrow{\mathbf{H}}_2^*\right]-\frac{dB(z)}{dz}\mathbf{u}_z\cdot\left[\overrightarrow{\mathbf{E}}_2^*\times\overrightarrow{\mathbf{H}}_2+\overrightarrow{\mathbf{E}}_2\times\overrightarrow{\mathbf{H}}_2^*\right] \\ &-j\omega\varepsilon_0A(z)((N^2-N_1^2))\overrightarrow{\mathbf{E}}_2^*\cdot\overrightarrow{\mathbf{E}}_1-j\omega\varepsilon_0B(z)((N^2-N_2^2))\overrightarrow{\mathbf{E}}_2^*\cdot\overrightarrow{\mathbf{E}}_2 \end{aligned} \tag{4.56}$$

Plugging (4.54) and (4.56) into (4.51), two expressions describing the changing rate of the field magnitude along the propagation direction (z axis), and the magnitude changing is caused by the coupling between waveguides.

$$
\begin{aligned}
\frac{dA(z)}{dz} + \frac{dB(z)}{dz}\frac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_1^*\times\overrightarrow{\mathbf{H}}_2+\overrightarrow{\mathbf{E}}_2\times\overrightarrow{\mathbf{H}}_1^*)dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_1^*\times\overrightarrow{\mathbf{H}}_1+\overrightarrow{\mathbf{E}}_1\times\overrightarrow{\mathbf{H}}_1^*)dxdy} \\
+jA(z)\frac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_1^2)\overrightarrow{\mathbf{E}}_1^*\cdot\overrightarrow{\mathbf{E}}_1dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_1^*\times\overrightarrow{\mathbf{H}}_1+\overrightarrow{\mathbf{E}}_1\times\overrightarrow{\mathbf{H}}_1^*)dxdy} \\
+jB(z)\frac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_2^2)\overrightarrow{\mathbf{E}}_1^*\cdot\overrightarrow{\mathbf{E}}_2dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_1^*\times\overrightarrow{\mathbf{H}}_1+\overrightarrow{\mathbf{E}}_1\times\overrightarrow{\mathbf{H}}_1^*)dxdy} = 0
\end{aligned}
\tag{4.57}
$$

$$
\begin{aligned}
\frac{dB(z)}{dz} + \frac{dA(z)}{dz}\frac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_2^*\times\overrightarrow{\mathbf{H}}_1+\overrightarrow{\mathbf{E}}_1\times\overrightarrow{\mathbf{H}}_2^*)dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_2^*\times\overrightarrow{\mathbf{H}}_2+\overrightarrow{\mathbf{E}}_2\times\overrightarrow{\mathbf{H}}_2^*)dxdy} \\
+jA(z)\frac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_1^2)\overrightarrow{\mathbf{E}}_2^*\cdot\overrightarrow{\mathbf{E}}_1dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_2^*\times\overrightarrow{\mathbf{H}}_2+\overrightarrow{\mathbf{E}}_2\times\overrightarrow{\mathbf{H}}_2^*)dxdy} \\
+jB(z)\frac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_2^2)\overrightarrow{\mathbf{E}}_2^*\cdot\overrightarrow{\mathbf{E}}_2dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\overrightarrow{\mathbf{E}}_2^*\times\overrightarrow{\mathbf{H}}_2+\overrightarrow{\mathbf{E}}_2\times\overrightarrow{\mathbf{H}}_2^*)dxdy} = 0
\end{aligned}
\tag{4.58}
$$

Let's define three types of coupling coefficient κ_{12}, c_{12} and χ_1 as below.

$$
\begin{cases}
\kappa_{12} = \dfrac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_2^2)\mathbf{E}_1^*\cdot\mathbf{E}_2dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\mathbf{E}_1^*\times\mathbf{H}_1+\mathbf{E}_1\times\mathbf{H}_1^*)dxdy} \\
c_{12} = \dfrac{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\mathbf{E}_1^*\times\mathbf{H}_2+\mathbf{E}_2\times\mathbf{H}_1^*)dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\mathbf{E}_1^*\times\mathbf{H}_1+\mathbf{E}_1\times\mathbf{H}_1^*)dxdy} \\
\chi_1 = \dfrac{\omega\varepsilon_0\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2-N_1^2)\mathbf{E}_1^*\cdot\mathbf{E}_1dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z\cdot(\mathbf{E}_1^*\times\mathbf{H}_1+\mathbf{E}_1\times\mathbf{H}_1^*)dxdy}
\end{cases}
\tag{4.59}
$$

Then, Substituting the propagation expression Eqn. (4.2) into Eqn. (4.57) and Eqn. (4.58), we can simplify Eqn. (4.57) and (4.58) into

$$
\begin{cases}
\dfrac{dA(z)}{dz} + c_{12}\dfrac{dB(z)}{dz}e^{[-j(\beta_2-\beta_1)z]} + j\chi_1A(z) + j\kappa_{12}B(z)e^{[-j(\beta_2-\beta_1)z]} = 0 \\
\dfrac{dB(z)}{dz} + c_{21}\dfrac{dA(z)}{dz}e^{[j(\beta_2-\beta_1)z]} + j\chi_2B(z) + j\kappa_{21}A(z)e^{[j(\beta_2-\beta_1)z]} = 0
\end{cases}
\tag{4.60}
$$

The denominators of Eqn. (4.59) are the Poynting Vectors respecting the total power carried by eigen mode in Waveguide 1 and Waveguide 2, respectively. Since ($\mathbf{E}_1$, $\mathbf{H}_1$) and ($\mathbf{E}_2$, $\mathbf{H}_2$) are the

field with an individual Waveguide 1 or Waveguide 2, we assume that the power in both waveguides are normalized to 1.

$$\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \mathbf{u}_z \cdot (\mathbf{E}_1^* \times \mathbf{H}_1 + \mathbf{E}_1 \times \mathbf{H}_1^*)dxdy = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} \mathbf{u}_z \cdot (\mathbf{E}_2^* \times \mathbf{H}_2 + \mathbf{E}_2 \times \mathbf{H}_2^*)dxdy = 1 \quad (4.61)$$

From the coupling coefficient in Eqn. (4.59) c_{12} and χ_1, we can easily find out that $c_{12} = c_{21}$ and $\chi_1 = \chi_2$.

In the theoretical analysis of this dissertation, c_{12} and χ_1 are negligible, because both c_{12} and χ_1 are much smaller than κ_{12}. Let's compare c_{12} and χ_1 with κ_{12}. Eqn. (4.60) describes the field strength change of $\frac{dA(z)}{dz}$ in Waveguide 1, $\frac{dB(z)}{dz}$ in Waveguide 2, respectively, with the coupling from the other waveguide. κ_{12} and κ_{21} are a mode coupling coefficient of the directional coupler. Compare the magnitude of κ_{12} and χ_1, when EM power is coupling from Waveguide 2 to Waveguide 1. As shown in Figure (4.4), the actual value of $N^2 - N_2^2$ in waveguide 1 equals $(n_1^2 - n_0^2)$ and takes zero in all other regions. Then κ_{12} is the integral of $\mathbf{E}_1^* \cdot \mathbf{E}_2$ that is carried out only inside the core region of Waveguide 1. The magnitude of κ_{12} is about $(n_1^2 - n_0^2)|\mathbf{E}_1||\mathbf{E}_2|e^{-\alpha_x(D-b_1-b_2)}$, where $(D-b_1-b_2)$ is the gap between waveguides. The value of $N^2-N_1^2$ in waveguide 2 equals $(n_1^2-n_0^2)$ and takes zero in all other regions, which means χ_1 in the numerator of $\mathbf{E}_1^* \cdot \mathbf{E}_1$ takes the integral inside the core region of Waveguide 2, and the value is approximately equals to $(n_1^2 - n_0^2)|\mathbf{E}_1|^2 e^{-2\alpha_x(D-b_1-b_2)}$ that is quite small when compared with κ_{12} when the waveguides are sufficiently separated. κ_{21} and χ_2 have the same relationship.

Then compare c_{12} with κ_{12}. The dominant field in the rectangular waveguide that we are discussing in this design are E_y and H_x, and they are almost perpendicular. The numerator of c_{12} can be calculated as

$$\mathbf{u}_z \cdot (\mathbf{E}_1^* \times \mathbf{H}_2 + \mathbf{E}_2 \times \mathbf{H}_1^*) \approx 2|\mathbf{E}_1||\mathbf{H}_2|e^{-\alpha_x(D-b_1-b_2)} \quad (4.62)$$

Substituting Eqn. (4.33) into Eqn. (4.62),

$$\begin{aligned} |\mathbf{E}_1||\mathbf{H}_2|e^{-\alpha_x(D-b_1-b_2)} &\approx \frac{\beta}{\omega\mu_0}|\mathbf{E}_1||\mathbf{E}_2|e^{-\alpha_x(D-b_1-b_2)} \\ &\approx \sqrt{\frac{\varepsilon_0}{\mu_0}}|\mathbf{E}_1||\mathbf{E}_2|e^{-\alpha_x(D-b_1-b_2)} \ll |\mathbf{E}_1||\mathbf{E}_2|e^{-\alpha_x(D-b_1-b_2)} \end{aligned} \quad (4.63)$$

where $\varepsilon_0 \approx 8.85 \times 10^{-12}\ F/m$ and $\mu_0 \approx 1.26 \times 10^{-6}\ N \cdot A^{-2}$. Therefore, $c_{12} \ll \kappa_{12}$.

The meaning of c_{12} described as follows. Let us consider waveguide configurations, where Waveguide 1 exists only in the region $z < 0$ and Waveguide 2 in $z > 0$. When the eigen mode $(\mathbf{E}_1, \mathbf{H}_1)$ of waveguide 1 propagates from the eigen mode $(\mathbf{E}_2, \mathbf{H}_2)$ at the point $z = 0$. This excitation efficiency is considered negative z-direction to z=0, the electromagnetic field in the cladding excites the to be c_{12}. Therefore, c_{12} represents the butt coupling coefficient between the two waveguides [**61**] [**62**].

The analyses of the directional couplers in this article, c_{12} and χ_1 were neglected and they are assumed to be $c_{12} = \chi_1 = 0$. However, both c_{12} and χ_1 should be taken into account in order to analyze the mode coupling effect strictly.

In most of the directional couplers, κ_{pq} is real and reciprocal.

$$\kappa = \kappa_{12} = \kappa_{21} = \frac{\omega\varepsilon_0 \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}(N^2 - N_2^2)\mathbf{E}_1^* \cdot \mathbf{E}_2 dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z \cdot (\mathbf{E}_1^* \times \mathbf{H}_1 + \mathbf{E}_1 \times \mathbf{H}_1^*)dxdy} \tag{4.64}$$

$$\kappa_{12} = \frac{\omega\varepsilon_0(n_1^2 - n_0^2)\int_{-b_1}^{b_1}\int_{-h}^{h}\mathbf{E}_1^* \cdot \mathbf{E}_2 dxdy}{\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\mathbf{u}_z \cdot (\mathbf{E}_1^* \times \mathbf{H}_1 + \mathbf{E}_1 \times \mathbf{H}_1^*)dxdy} \tag{4.65}$$

Since the expression of coupling coefficient has been derived, next step is to calculate the coupling coefficient in a rectangular waveguide. For a directional coupler consisting of three-dimensional rectangular waveguides, the electromagnetic field components of the E_{pq}^y mode are expressed in terms of H_x from Eqn. (4.32), (4.33) and (4.28).

$$\begin{cases} E_x = -\dfrac{1}{\omega\varepsilon_0 N^2\beta}\dfrac{\partial^2 H_x}{\partial x \partial y} \ll E_y \\ E_y - \dfrac{\omega\mu_0}{\beta}H_x - \dfrac{1}{\omega\varepsilon_0 N^2\beta}\dfrac{\partial^2 H_x}{\partial y^2} \approx -\dfrac{\omega\mu_0}{\beta}H_x \\ H_y = 0 \end{cases} \tag{4.66}$$

The denominator of Eqn. (4.65)

$$\mathbf{u}_z \cdot (\mathbf{E}_1^* \times \mathbf{H}_1 + \mathbf{E}_1 \times \mathbf{H}_1^*) = 2E_{1y}^* \cdot H_{1x} = \frac{2\omega\mu_0}{\beta}\left|H_{1x}\right|^2 \tag{4.67}$$

Then,

$$
\begin{aligned}
&2\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} E_{1y}^{*}\cdot H_{1x}dxdy \\
&= \frac{2\omega\mu_0}{\beta}\left(\iint_{Region1}|H_{1x}|^2\,dxdy + \iint_{Region2}|H_{1x}|^2\,dxdy + \iint_{Region3}|H_{1x}|^2\,dxdy\right)
\end{aligned}
\tag{4.68}
$$

$$
\begin{aligned}
\iint_{Region1}|H_{1x}|^2\,dxdy &= \frac{2\omega\mu_0}{\beta}\int_{-h}^{h}\int_{-b_1}^{b_1}|A|^2\cos^2(k_x x-\Phi_x)\cos^2(k_y y-\Phi_y)dxdy \\
&\approx \frac{2\omega\mu_0}{\beta}|A|^2 b_1 h
\end{aligned}
\tag{4.69}
$$

$$
\begin{aligned}
\iint_{Region2}|H_{1x}|^2\,dxdy &= \frac{4\omega\mu_0}{\beta}\int_{-h}^{h}\int_{b_1}^{\infty}|A|^2\cos^2(k_x b-\Phi_x)e^{-2\alpha_x(x-b_1)}\cos^2(k_y y-\Phi_y)dxdy \\
&\approx \frac{2\omega\mu_0}{\beta}|A|^2\frac{h}{\alpha_x}
\end{aligned}
\tag{4.70}
$$

$$
\begin{aligned}
\iint_{Region3}|H_{1x}|^2\,dxdy &= \frac{4\omega\mu_0}{\beta}\int_{h}^{\infty}\int_{-b_1}^{b_1}|A|^2\cos^2(k_x x-\Phi_x)e^{-2\alpha_y(y-h)}\cos^2(k_y h-\Phi_y)dxdy \\
&\approx \frac{2\omega\mu_0}{\beta}|A|^2\frac{b_1}{\alpha_y}
\end{aligned}
\tag{4.71}
$$

Therefore,

$$
\begin{aligned}
2\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} E_{1y}^{*}\cdot H_{1x}dxdy &\approx \frac{2\omega\mu_0}{\beta}|A|^2\left(b_1 h+\frac{h}{\alpha_x}+\frac{b_1}{\alpha_y}\right) \\
&\approx \frac{2\omega\mu_0}{\beta}|A|^2\left(b_1+\frac{1}{\alpha_x}\right)\left(h+\frac{1}{\alpha_y}\right)
\end{aligned}
\tag{4.72}
$$

The numerator of Eqn. (4.65)

$$
\mathbf{E}_1^{*}\cdot\mathbf{E}_2 = E_{1y}^{*}\cdot E_{2y} = |E_{1y}|^2\,e^{-\alpha_x(x-b_1-b_2)}
\tag{4.73}
$$

Substituting $E_{1y}=\dfrac{\omega\mu_0}{\beta}H_{1y}$ into Eqn. (4.73), then we can calculate the nominator of κ

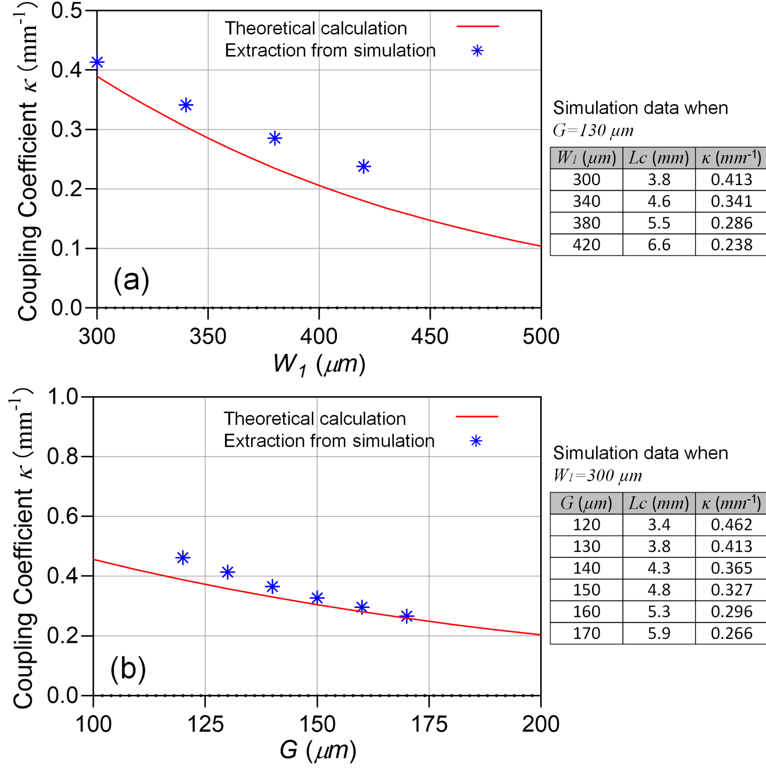
$$
\begin{aligned}
&\omega\varepsilon_0(n_1^2-n_0^2)\int_{-b_1}^{b_1}\int_{-h}^{h} E_{1y}^{*}\cdot E_{2y}dxdy \\
&=\omega\varepsilon_0(n_1^2-n_0^2)\int_{-b_1}^{b_1}\int_{-h}^{h} \left|E_{1y}\right|^2 e^{-\alpha_x(x-b_1-b_2)}dxdy \\
&=\omega\varepsilon_0(n_1^2-n_0^2)\frac{(\omega\mu_0)^2}{\beta^2}\int_{-b_1}^{b_1}\int_{-h}^{h} \left|H_{1x}\right|^2 e^{-\alpha_x(x-b_1-b_2)}dxdy \\
&\approx \frac{\omega^3\mu_0^2\varepsilon_0}{\beta^2}|A|^2\left(h+\frac{1}{\alpha_y}\right)\frac{(n_1^2-n_0^2)}{k_x^2\alpha_x}e^{[-\alpha_x(D-b_1-b_2)]}
\end{aligned}
\tag{4.74}
$$

Plugging Eqn. (4.72) and (4.74) into (4.65), we can obtain the coupling coefficient κ_{12},

$$
\begin{aligned}
\kappa &= \frac{\omega^2\mu_0\varepsilon_0}{2\beta}\frac{k_x^2\alpha_x^2}{(b_1\alpha_x+1)\,(n_1^2-n_0^2)}e^{[-\alpha_x(D-b_1-b_2)]} \\
&= \frac{k_0^2k_x^2\alpha_x^2}{2\beta\,(b_1\alpha_x+1)\,(n_1^2-n_0^2)}e^{[-\alpha_x(D-b_1-b_2)]} \\
&= \frac{\sqrt{2\Delta}}{b_1}\frac{(k_xb_1)^2(\alpha_xb_1)^2}{b_1(1+\alpha_xb_1)v^3}e^{[-\alpha_x(D-b_1-b_2)]}
\end{aligned}
\tag{4.75}
$$

where the relative refractive-index difference between n_1 and n_0 is defined as $\Delta=\sqrt{(n_1^2-n_0^2)/2n_1^2}$, and the normalized frequency is $v=k_0n_1b_1\sqrt{2\Delta}$. For a given waveguide coupler and mode, the most efficient way to adjust coupling coefficient is tuning the gap $(D-b_1-b_2)$ between waveguides.

To verify the theoretical analysis, HFSS simulations were conducted on a rectangular Si DWG coupler with the height of $H=525\ \mu m$ at 165 GHz. The coupling coefficient cannot be extracted directly from the EM solver, but it is inversely proportional to the optimum coupler length L_C, which will be discussed in the next subsection. In Figure. 4.6 (a), the coupling coefficient is simulated and calculated versus the DWG width W with a fixed gap of $G=130\ \mu m$. In Figure 4.6 (b) the coupling coefficient is plotted when sweeping the gap G of a DWG coupler with a width of $W_1=300\ \mu m$. The simulation results match the calculation curves very well when the gap is relatively large (compared to the width). With the gap decreasing, the field superposition assumption in Eqn. (4.43) is no longer accurate due to the strong interaction between EM field in waveguidess, thus causing result discrepancy between analytical and simulation results. Considering



W_1 (μm)	Lc (mm)	κ (mm^{-1})
300	3.8	0.413
340	4.6	0.341
380	5.5	0.286
420	6.6	0.238

G (μm)	Lc (mm)	κ (mm^{-1})
120	3.4	0.462
130	3.8	0.413
140	4.3	0.365
150	4.8	0.327
160	5.3	0.296
170	5.9	0.266

FIGURE 4.6. Calculated and simulated coupling coefficient versus the waveguides' (a) width of W and (b) gap of G.

higher-order mode conversion and fabrication capabilities, small gaps are also avoided in the design and the typical value is in the range of 120 to 170 μm.

4.2.3. Mode Coupling Efficiency.

Coupling efficiency quantifies the power percentage coupled from waveguide 1 to waveguide 2, and determines the insertion loss of the mode coupler. As we know, the coupling coefficient affects the EM field magnitude changing, therefore the expressions below can establish the relation between coupling coefficient κ and EM field magnitude $A(z)$ and $B(z)$ [**58**]. Since c_{12} and $\chi_1 \ll \kappa$, we assume that $c_{12} = \chi_1 = 0$, and the Eqn. (4.60) can be rewritten as

$$\begin{cases} \dfrac{dA(z)}{dz} = -j\kappa_{12}B(z)e^{-j(\beta_2-\beta_1)z} \\ \dfrac{dB(z)}{dz} = -j\kappa_{21}A(z)e^{j(\beta_2-\beta_1)z} \end{cases} \tag{4.76}$$

Solve the differential Eqn. (4.76)

$$\begin{cases} A(z) = \left[a_1 e^{jqz} + a_2 e^{-jqz}\right] e^{-j(\beta_2-\beta_1)z} \\ \\ B(z) = \left[b_1 e^{jqz} + b_2 e^{-jqz}\right] e^{j(\beta_2-\beta_1)z} \end{cases} \tag{4.77}$$

From Eqn. (4.76) and (4.80), one solution of magnitude $A(z)$ in waveguide 1 and $B(z)$ in waveguide 2 that satisfy the physical characteristics is given by:

$$\begin{aligned} A(z) = \Bigg\{ & [\cos(\sqrt{\kappa^2+\delta_\beta^2}z) + j\frac{\delta}{\sqrt{\kappa^2+\delta_\beta^2}}\sin(\sqrt{\kappa^2+\delta_\beta^2}z)]A(0) \\ & -j\frac{\kappa}{\sqrt{\kappa^2+\delta_\beta^2}}\sin(\sqrt{\kappa^2+\delta_\beta^2}z)B(0)\Bigg\} e^{-j\delta_\beta z} \end{aligned} \tag{4.78}$$

$$\begin{aligned} B(z) = \Bigg\{ & -j\frac{\kappa}{q}\sin(\sqrt{\kappa^2+\delta_\beta^2}z)A(0) + [\cos(\sqrt{\kappa^2+\delta_\beta^2}z) \\ & -j\frac{\delta_\beta}{\sqrt{\kappa^2+\delta_\beta^2}}\sin(\sqrt{\kappa^2+\delta_\beta^2}z)]B(0)\Bigg\} e^{-j\delta_\beta z} \end{aligned} \tag{4.79}$$

where $\delta_\beta = (\beta_1 - \beta_2)/2$ is the propagation constant difference.

If the DWGs start to overlap at $z = 0$ with a normalized magnitude of one, an initial condition is concluded in Eqn. (4.80).

$$\begin{cases} A(0) = 1, \quad z = 0 \\ \\ B(0) = 0, \quad z = 0 \end{cases} \tag{4.80}$$

Then, one solution of magnitude $A(z)$ in waveguide 1 and $B(z)$ in waveguide 2 that satisfy the physical characteristics is given by:

$$A(z) = [\cos(\sqrt{\kappa^2+\delta_\beta^2}z) + j\frac{\delta_\beta}{\sqrt{\kappa^2+\delta_\beta^2}}\sin(\sqrt{\kappa^2+\delta_\beta^2}z)]e^{-j\delta_\beta z} \tag{4.81}$$

$$B(z) = -j\frac{\kappa}{\sqrt{\kappa^2+\delta_\beta^2}}\sin(\sqrt{\kappa^2+\delta_\beta^2}z)e^{-j\delta_\beta z} \tag{4.82}$$

Power percentage left in waveguide 1

$$P_1(z) = \frac{|A(z)|^2}{|A(0)|^2} = \cos^2(\sqrt{\kappa^2 + \delta_\beta^2} z) + \frac{\delta_\beta^2}{\kappa^2 + \delta_\beta^2} \sin^2(\sqrt{\kappa^2 + \delta_\beta^2} z) \tag{4.83}$$

Power percentage coupled to waveguide 2, also defined as the coupling efficiency η

$$\eta = P_2(z) = \frac{|B(z)|^2}{|A(0)|^2} = \frac{\kappa^2}{\kappa^2 + \delta_\beta^2} \sin^2(\sqrt{\kappa^2 + \delta_\beta^2} z) \tag{4.84}$$

However, there is an attenuation constant α existing in practice and the total power dissipates along the DWG and coupler, as shown in Figure 4.7 (d). The attenuation constant can be calculated with the loss tangent ($\tan\delta$) of the dielectric material by [**24**]:

$$\alpha = \frac{\omega}{c}\sqrt{\frac{\varepsilon_r'}{2}\left(1 + \tan^2\delta\right) - 1} \tag{4.85}$$

where ε_r' is the real part of the relative dielectric constant. The coupling efficiency is expressed as Eqn. (4.86) if considering the material attenuation constant.

$$\eta = \frac{\kappa^2}{\kappa^2 + \delta_\beta^2} \sin^2(\sqrt{\kappa^2 + \delta_\beta^2} z) e^{-\alpha z} \tag{4.86}$$

z is the coupler length variable by assuming the DWGs start to overlap at $z = 0$. The maximum η occurs when

$$z = L_C = \frac{\pi}{\sqrt{\delta_\beta^2 + \kappa^2}}(m + \frac{1}{2}), \quad m = 0, 1, ..., \infty \tag{4.87}$$

Then the coupling efficiency η reaches

$$\eta_{max} = \frac{1}{1 + (\delta_\beta/\kappa)^2} e^{\left[-\alpha\pi/\left(2\sqrt{\delta_\beta^2+\kappa^2}\right)\right]} \tag{4.88}$$

where F denotes the maximum power-coupling efficiency, defined by $\frac{\kappa^2}{\kappa^2 + \delta_\beta^2}$.

In actual design, the first step is to minimize the propagation constant difference δ by tuning the width of DWG, then select the optimum coupler length L_C. To reduce channel loss and reduce coupler size, the first peak point when $m = 0$ is preferred. The simulated η along the propagation direction z is plotted in Figure. 4.7 (c). $L_C = 3.8\,mm$ for E_{11}^y to E_{21}^y coupler and $L_C = 4.5\,mm$ for E_{11}^y to E_{31}^y coupler are selected.

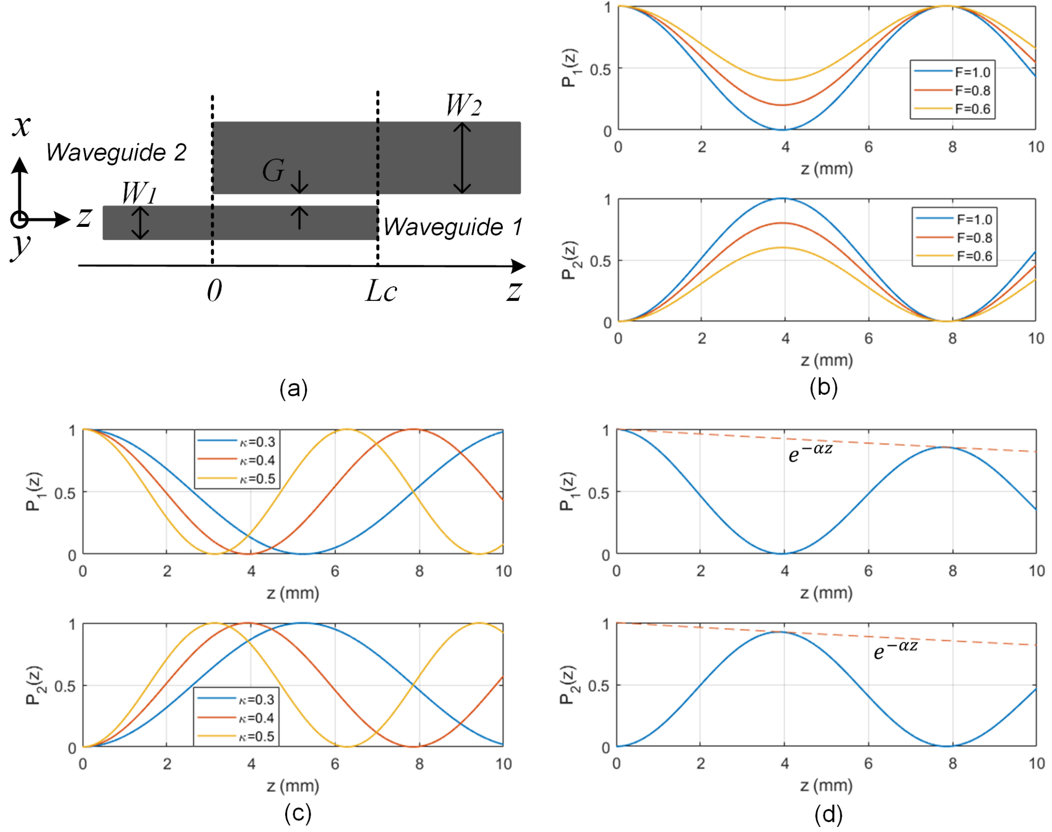


FIGURE 4.7. (a) Geometry illustration of a DWG coupler. Calculated power intensity $P_1(z)$ in waveguide 1 and $P_2(z)$ in waveguide 2 along z-direction with different coupling efficiency factor F, coupling coefficient κ and attenuation constant α: (b) $\kappa = 0.4$, $\alpha = 0$ and $F = 0.6, 0.8, 1$; (c) $F = 1$ (δ_β=0), $\alpha = 0$ and $\kappa = 0.3, 0.4, 0.5$; (d) $F = 1$ ($\delta_\beta = 0$), $\kappa = 0.4$ and $\alpha = 0.02$.

4.2.4. Mode Coupling Bandwidth.

The broad-band channel is desired in a communication system, because it directly determines the maximum data capability. In optics field, fiber's bandwidth is rarely discussed and it never becomes the bottleneck of the link, which is benefited from the high carrier frequency. Typically multi-mode glass fibers use light at 850 nm (186 THz) to 1300 nm (230 THz), referred to as short wavelength and single-mode fiber operates at 1310 nm (229 THz), or 1550 nm (193 THz), called long wavelength. The reported optic mode couplers [**50**] achieve 90 nm wavelength band that approximately equals to a bandwidth of 10 THz at 1550 nm, and it is hundred times wider than the bandwidth occupied by the latest high-speed communication link with 100 Gb/s data rate.

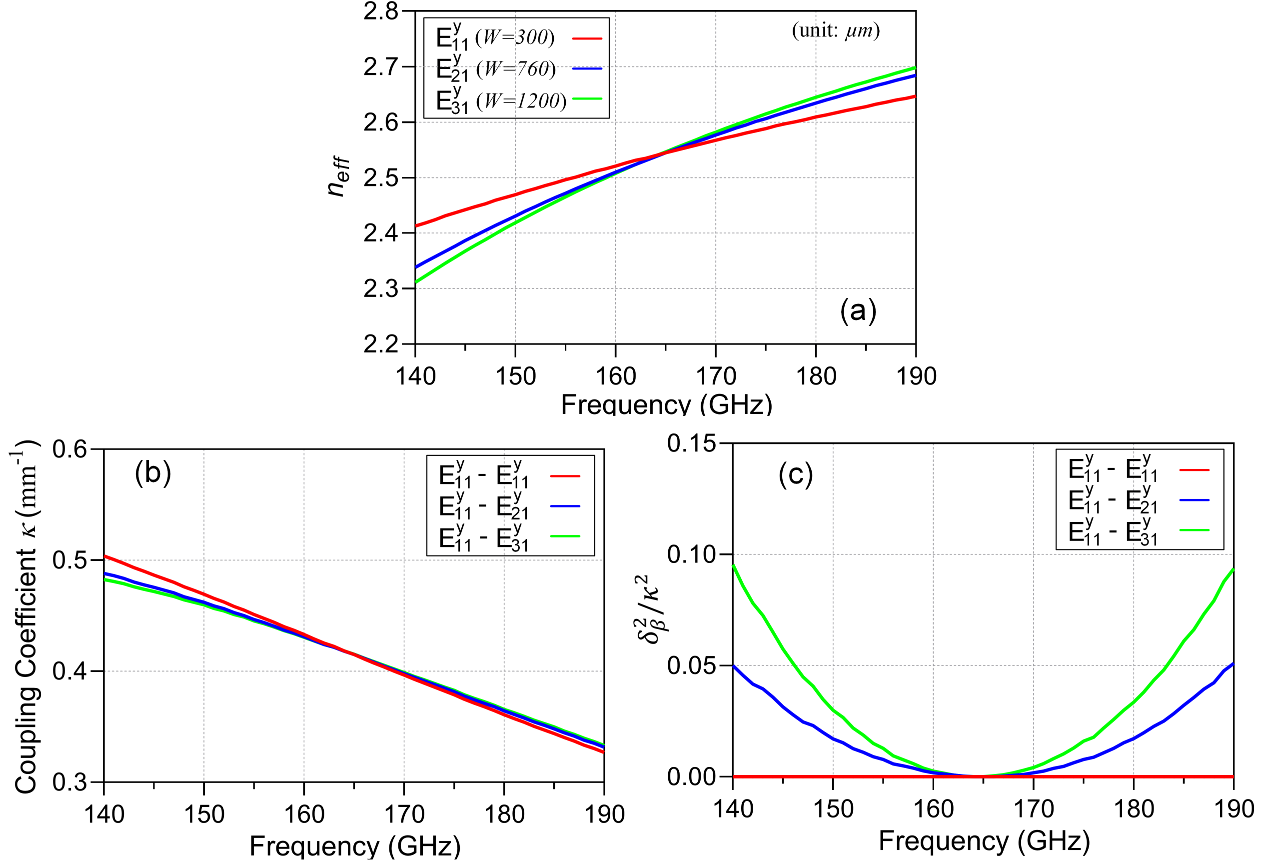


FIGURE 4.8. Frequency-dependent parameters of the DWG and mode coupler for the three different modes with different DWG widths: (a) effective refractive index n_{eff}, (b) coupling coefficient κ and (c) δ_β^2/κ^2 which is the only determining variable in the coupling efficiency factor F theoretical representation.

However, when the DWG mode coupler shifts down to sub-THz/THz and keeps similar fractional bandwidth, which may be insufficient for high data rate communications, especially in a non-coherent detection that requires double-side band RF signal. It is necessary to analyze the bandwidth constrains of mode couplers and researcher could try to conquer those bottlenecks.

From the coupling efficiency analysis in Eqn. (4.86), the major factors that constrains the bandwidth are δ_β (propagation constant difference), κ (coupling coefficient) and L_C (coupler length). All of those parameters are frequency depend, even higher-order related to the frequency. Figure. 4.8 shows a rectangular DWG mode coupler's frequency-dependent parameters, such as the effective refractive index n_{eff} in Figure 4.8 (a), coupling coefficient in Figure 4.8 (b), and δ_β^2/κ^2 ratio in Figure 4.8 (c) that determines the coupling efficiency factor F. All of the parameters together

determine the coupling efficiency at different frequencies, therefore the bandwidth. The effective refractive index n_{eff} dependency on frequency makes the propagation constant $\beta = n_{eff} \cdot \omega/c$ have a higher-order relation to the frequency. β describes the propagation characteristics and has influence on all the other parameters, among which the coupling coefficient κ and propagation constant difference δ_β are the most significant factors that affect the mode coupling bandwidth.

(1) Propagation constant difference δ_β

The first ting we have to consider is the phase matching condition that is the prerequisite for mode coupling. When the phase is matched or propagation constant along the propagation direction is equal or close, then it is possible to couple EM power between waveguides.Talking about E^y_{11}-to-E^y_{21} and E^y_{11}-to-E^y_{31} couplers, the phase is matched at the center frequency (165 GHz), but k_z starts to deviate when frequency is off from 165 GHz. δ^2_β increases rapidly as the frequency offset increases and E^y_{11}-to-E^y_{31} coupler has more serious issues than E^y_{11}-to-E^y_{21} coupler.

(2) Coupling coefficient κ

According to Eqn. (4.75), the coupling coefficient is a function of wavenumbers along z and x axis in this case (k_z and k_x). As we know, the wavenumbers' value can be calculated by the effective refractive index n_{eff} by the Eqn. (4.89) and (4.90)

$$\beta = k_z = n_{neff}\frac{\omega}{c} \tag{4.89}$$

$$k_x = \frac{\sqrt{n_1^2 - n_{neff}^2}}{n_1}\frac{\omega}{c} \tag{4.90}$$

The effective refractive index n_{eff} for a specific mode in a given waveguide can be extracted by simulators (by Rsoft or HFSS), as shown in Figure 4.9. It is obvious that the n_{eff} is a frequency-dependent variable, and the higher order modes have stronger dependency on frequency by checking the slope of the curves.

(3) The optimum coupler length L_C.

The optimum coupler length can be calculated with Eqn. (4.87), in which it is determined by the δ_β and κ. δ^2_β and κ^2 don't have opposite tendency in term of frequency and they could deffer in value by orders, so the frequency dependency can't be cancelled out in the L_C calculation, which makes L_C a function independent from frequency. The simulation results plotted in Figure 4.10 can

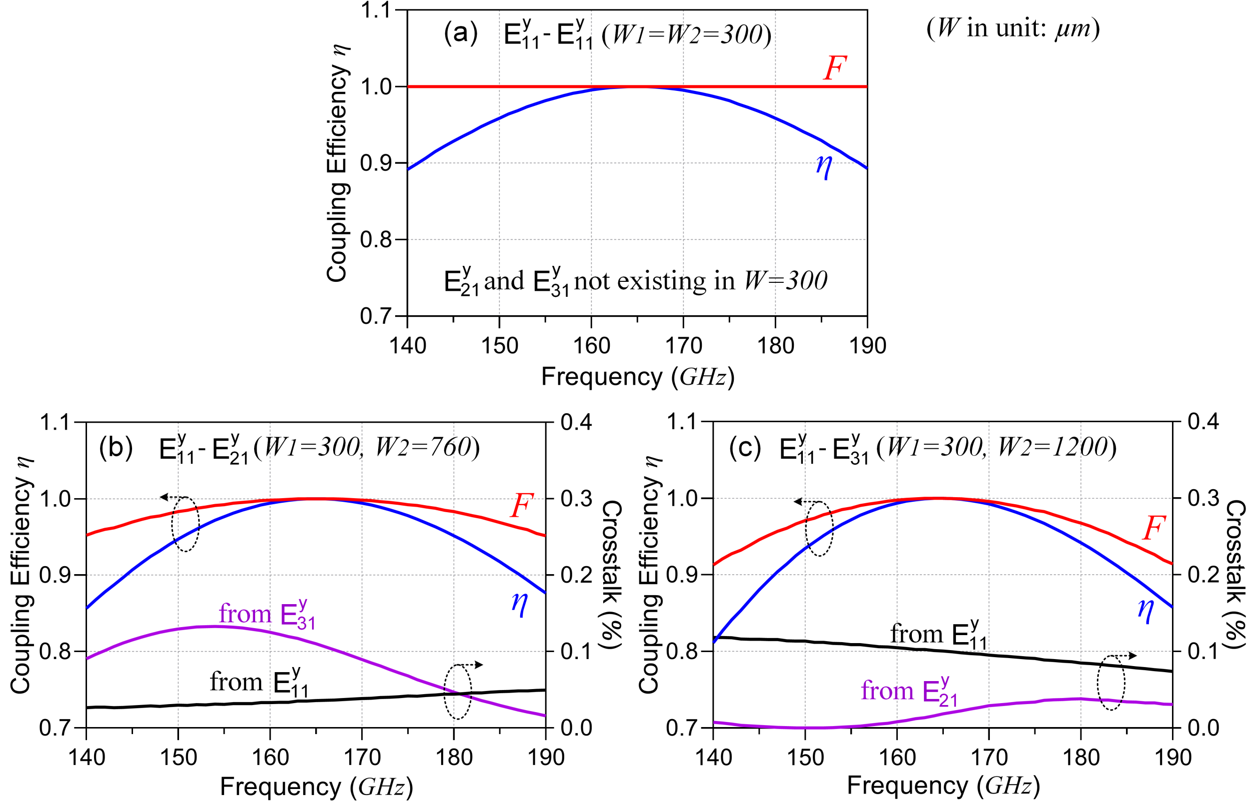


FIGURE 4.9. Calculated coupling efficiency η, coupling efficiency factor F and mode crosstalk for (a) E^y_{11}-E^y_{11}, (b) E^y_{11}-E^y_{21} and (c) E^y_{11}-E^y_{31} mode couplers

prove this hypothesis, in which the coupling efficiency for E^y_{11}-to-E^y_{11}, E^y_{11}-to-E^y_{21} and E^y_{11}-to-E^y_{31}. The optimum coupler length varies as the frequency changes and this characteristic is a factor constraining the bandwidth.

In summary, the three factors discussed above dictate the waveguide coupler a relatively narrow-band component in nature. That constrains the application in sub-THz/THz interconnects that requires wide bandwidth. The calculation of coupling efficiency and crosstalk are plotted in Figure 4.9.

For E^y_{11}-E^y_{11} mode coupler, the modes and dimensions of the waveguides are identical, thus δ_β is always zero and the coupling efficiency factor F is always one at any frequency, as shown in Figure 4.9 (a). However, L_C varies with frequency, because κ is a frequency-dependent variable and the corresponding optimum coupler length varies from 3.1 to 4.8 mm in the frequency band of 140∼190

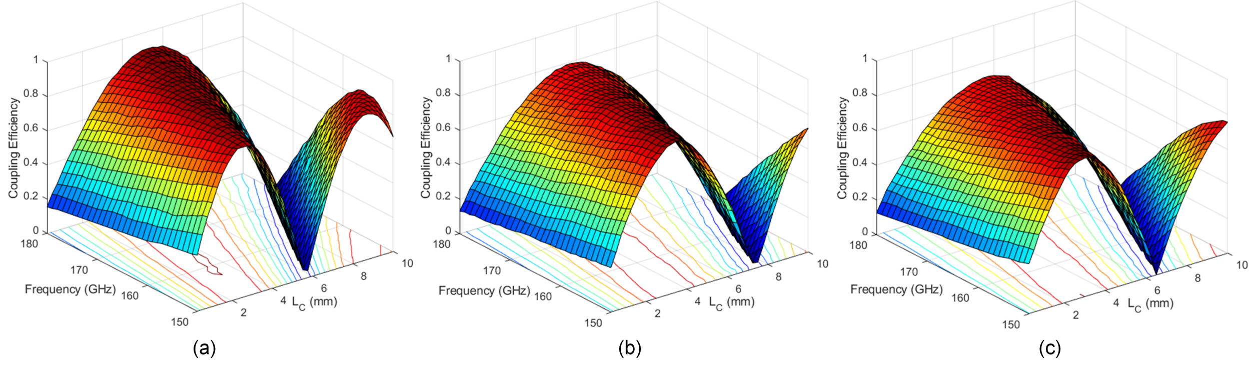


FIGURE 4.10. Simulated coupling efficiency for (a) E^y_{11}-to-E^y_{11}, (b)E^y_{11}-to-E^y_{21} and (c) E^y_{11}-to-E^y_{31} mode couplers versus the frequency and coupler length L_C.

GHz. If the optimum coupler length L_C at the center frequency of 165 GHz is picked, the coupling efficiency at the edges of band (140 and 190 GHz) drops to about 89%.

For E^y_{11}-E^y_{21} and E^y_{11}-E^y_{31} mode couplers, ideal phase matching condition can only be satisfied at the center frequency, as shown in Figure 4.9 (c). The increasing δ_β not only reduces the achievable maximum coupling efficiency F, but also makes the optimum coupler length L_C be a stronger frequency-dependent variable, thus leading to a smaller bandwidth. Figure 4.9 (b) and (c) clearly dictate the bandwidth degradation in the E^y_{11}-E^y_{21} and E^y_{11}-E^y_{31} mode couplers. At the edges of the frequency band (140 and 190 GHz), F drops to 0.95 and 0.91 due to non-zero δ_β, then η is further reduced to 0.85 and 0.81 because of the unmatched coupler length L_C. The bandwidth issue caused by β mismatch is more significant in the coupling between modes with larger order difference, such as E^y_{11} and E^y_{31}.

The mode crosstalk is evaluated in the DWG coupler as well. For the E^y_{11}-E^y_{11} coupler with width of $W_1 = W_2 = 300$ μm, only the fundamental mode exists in the DWGs, thus the crosstalk from higher-order modes is negligible, as shown in Figure. 4.9 (a). For bigger width, i.e. $W_2 = 760$ μm and 1200 μm, multiple modes, i.e. E^y_{11}, E^y_{21} and E^y_{31}, can co-exist together in the DWGs. Therefore, the crosstalk between undesired mode coupling occurs and can be qualified with Eqn. (4.84). Since the δ_β between undesired modes are large, the in-band crosstalk from all other mode is less than 0.14% (-28.5 dB), as shown in Figure 4.9 (b) and (c).

In actual design, the first step is to minimize the propagation constant difference δ_β at the center frequency by tuning the width of DWGs, then select the optimum coupler length L_C. To

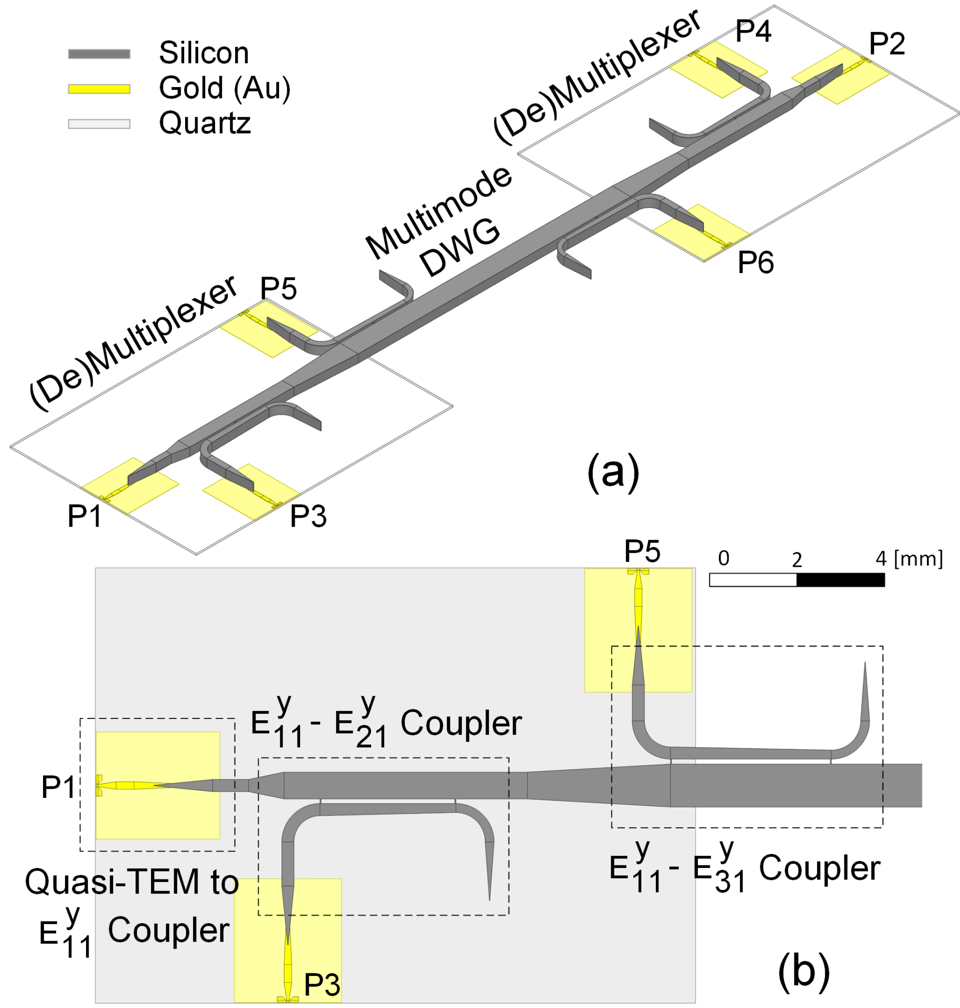


FIGURE 4.11. (a) 3-D view of the new mode-coupler-based multimode Si dielectric waveguide, and (b) the top view of mode couplers.

reduce the channel loss and coupler size, the first peak at $m = 0$ is usually preferred. Besides the frequency-dependent parameters in mode couplers, the waveguide cut-off frequency, undesired mode conversion at high frequency, and reflection also constrain the overall bandwidth. Therefore, the bandwidth in practice will be smaller than the theoretical calculation.

4.3. Multi-Drop Si DWG Channel Design

This section start to present a novel MDM (de)multiplexer based multi-drop DWG at sub-THz (with the center frequency at 165 GHz. The quasi-TEM to E^y_{11}, E^y_{11}-to-E^y_{11}, E^y_{11}-to-E^y_{21} and

E_{11}^y-to-E_{31}^y couplers are elaborated respectively. To evaluate the idea, couplers are cascaded with bending and tapers and form the compact multiplexer, which allows three modes transmitting in the multi-mode Si DWG with less than -26 dB crosstalk for multi-drop sub-THz/THz Interconnect. It is fabricated in-house with nano-manufacturing processes, so all the fabrication capability and tolerance need to be considered. For example, since the Si DWG is etched through from a Si wafer in a DRIE machine, the minimum gap between waveguides could be etched through is about 100 μm.

The sub-THz mode-coupler-based multi-mode Si DWG is shown in Figure 4.11 (a), which is built with a multiplexer, multimode Si DWG and demultiplexer on the other side. The bidirectional structure has 6 ports to excite and demultiplex E_{11}^y (P1 and P2), E_{21}^y (P3 and P4) and E_{31}^y (P5 and P6), respectively and independently. Three types of mode couplers construct the (de)multiplexer, as shown in Figure 4.11 (b). Quasi-TEM to E_{11}^y mode coupler working as a MSL-to-DWG transition is fabricated on a 100-μm quartz substrate. It generates and feeds E_{11}^y mode to all the ports of Si DWG. E_{11}^y to E_{21}^y and E_{11}^y to E_{31}^y mode couplers convert E_{11}^y to higher-order modes at P3 and P5, then three modes are generated, combined, and transmitted in the shared common waveguide in the center.

4.3.1. Multimode Si DWG Bus.

The common section of the Si DWG channel should support multiple modes simultaneously. If only considering y-polarized modes, such as E_{11}^y, E_{21}^y and E_{31}^y, the waveguide width does matter for multi-mode configuration. E-filed profiles shown in Figure 4.1, can exist together when the width of DWG is larger than 620 μm, which is determined by the effective refractive index n_{eff} in Figure 4.4. In other words, the higher-order modes, such as E_{21}^y and E_{31}^y, will be rejected or allowed in a DWG by simply reducing or increasing the waveguide width. This is similar as the operation principle of fiber mode filters to filter out undesired higher-order modes [**63**]. For a rectangular Si core (refractive index n_1=3.45, cross-section area: $H \times W$ μm^2) with air cladding (refractive index $n_0 = 1$), the n_{eff} and E-filed profiles of all the eigen modes are determined and solved by the graphic approach [**64**] at a given frequency. The highest-order mode determines the maximum number of modes that are supported by this DWG. The cross-section dimension of the multi-mode Si DWG in this design is $H \times W = 525 \times 1200$ μm^2.

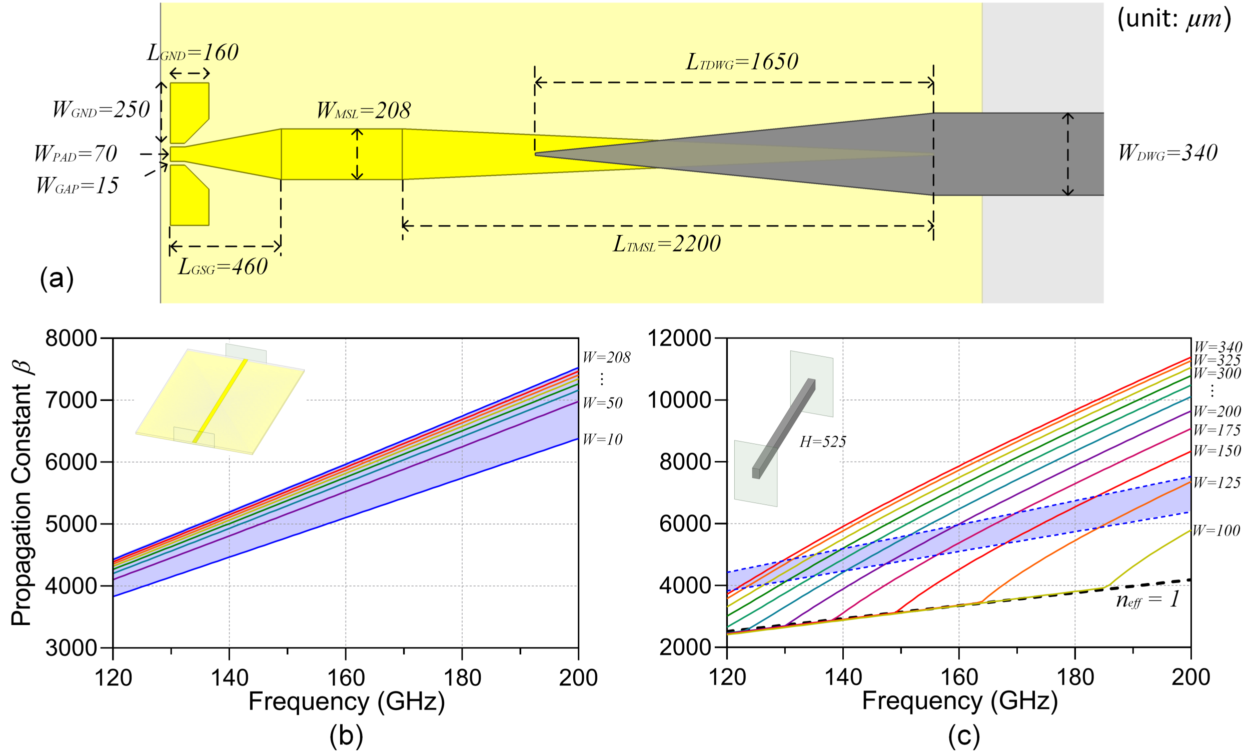


FIGURE 4.12. (a) Dimensions of the acrshortmsl-to-acrshortdwg transition. Simulated propagation constant comparison between (b) TEM mode in MSLs of width of 10 ∼ 200 μm and (c) E_{11}^{y} mode in DWGs of width of 50 ∼ 300 μm.

4.3.2. MSL-to-DWG transition (TEM-to-E_{11}^{y} Mode Coupler).

The MSL-to-DWG transition (or TEM-to-E_{11}^{y} Mode Coupler) has been introduced in the previous chapters and adopted in the dual-band sub-THz interconnect. The configuration of the Quasi-TEM to E_{11}^{y} coupler is shown in Figure 3.2. It consists of a CPWinterface with AC ground for GSG probe, oppositely tapered MSL and DWG to transit the electromagnetic wave smoothly. The quasi-TEM mode in MSL is gradually converted to E_{11}^{y} in DWG. The structure is fabricated on a 100 μm quartz ($\varepsilon_r = 3.78, \tan\delta = 0.0001$) substrate. The simulated S-parameters depicts great transition performance. It achieves the minimum insertion loss of 1.8 dB within a 2.5 dB bandwidth from 120 to 200 GHz.

In circuit or RFIC fields, impedance matching is the most common method to analyze this component, but it doesn't follow impedance matching mechanism if comparing the complex impedance of the MSL and DWG. However, this can be explained with mode coupling theory with phase

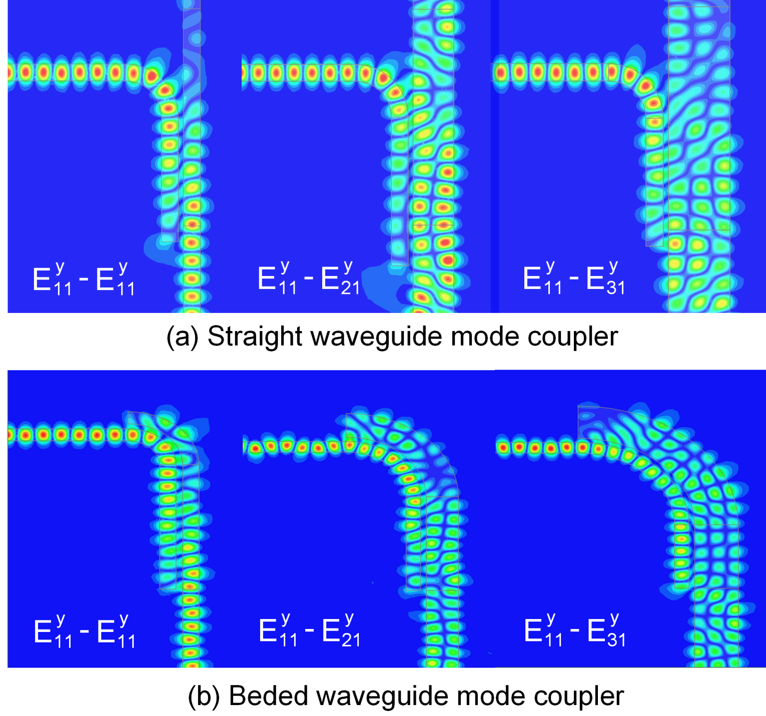


FIGURE 4.13. E field distribution in (a) straight DWG mode couplers, and (b) bended DWG mode couplers.

matching. Figure 4.12 compares the simulated propagation constant of TEM mode in MSLs of width of 10 $\sim$ 200 μm and E^y_{11} mode in DWGs of width of 50 $\sim$ 300 μm in a frequency range of 120$\sim$200 GHz. Tapped structure of MSL and DWG makes their propagation constant matched for a wide frequency band.In the practical design, the length and position of overlapping between the tapered MSL DWG must be optimized to achieve the best phase matching for the desire frequency bands.

4.3.3. E^y_{11}-to-E^y_{11}, E^y_{11}-to-E^y_{21} and E^y_{11}-to-E^y_{31} DWG Mode Couplers.

The theory of mode coupling between DWGs has been explained and derived in section 4.2. As mentioned before, the phase matching condition is the first requirement must satisfy. Phase matching requires that the propagation constant β or , which is the wavenumber along propagation direction, are equal for the coupling modes. By precisely controlling the width of DWG, the n_{eff} of a specific mode can be finely tuned, then it is possible to make two modes phase matched according to Eqn. (4.89). At 165 GHz, the n_{eff} of mode E^y_{11} in a DWG with W_1=300 μm is 2.55, which

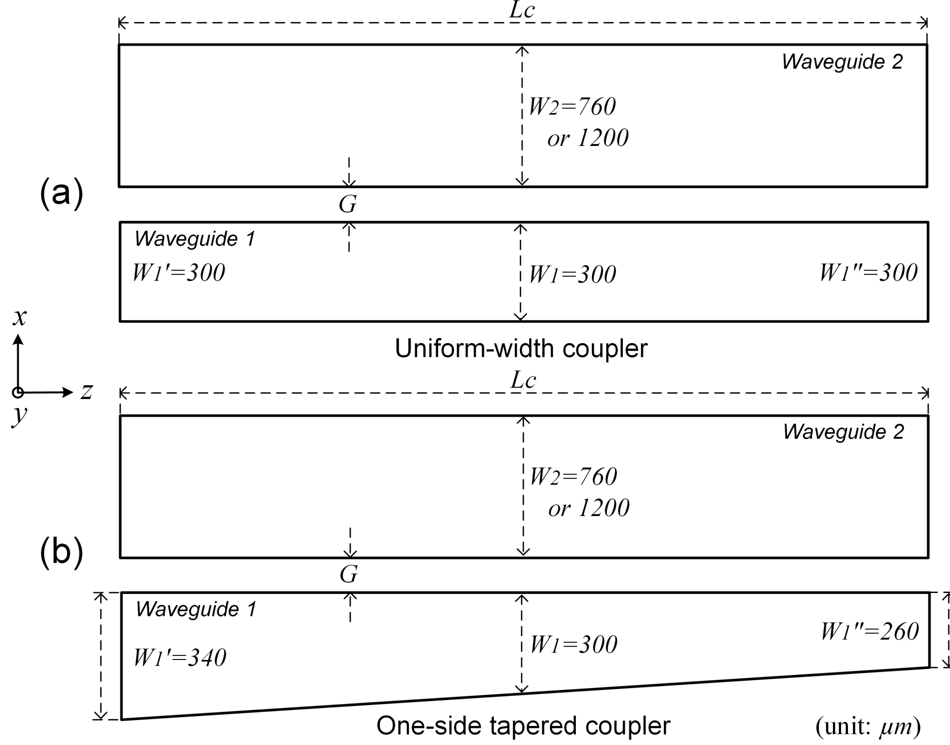


FIGURE 4.14. (a) Top view of the DWG mode coupler, and (b) E field distribution.

equals to the n_{eff} of E^y_{21} in a DWG with W_2=760 μm and E^y_{21} in a DWG with W_3=1200 μm, which is illuminated in Figure 4.13 (a). The mode coupler is also possible to design in a bended DWG, as shown in 4.13 (b), but the width need to finely tuned again, because the effective width and refractive index n_{eff} have changed, which could increase the propagation constant difference δ_β then degrade the coupling efficiency. Another concern in bended DWG is the higher-order mode conversion in bended waveguide, which will be discussed in the next subsection. To avoid mode conversion, a smoothly bended DWG with a large radius is prefered.

Talking about the DWG mode coupler design, the extract structure is depicted in Figure 4.16 (a). It consists of two parallel DWGs in identical width or different width, which is decided by the mode, refractive index of core and cladding, and operation frequency. The coupler arm is in one-side tapered shape and terminated with a tip-end, and smooth bended DWGs are used to connect all the sections. If the EM signal in E^y_{11} mode injected from bottom port as shown in the figure, it is guided to coupler smoothly. Then the one-side tapered structure helps the mode coupling happen

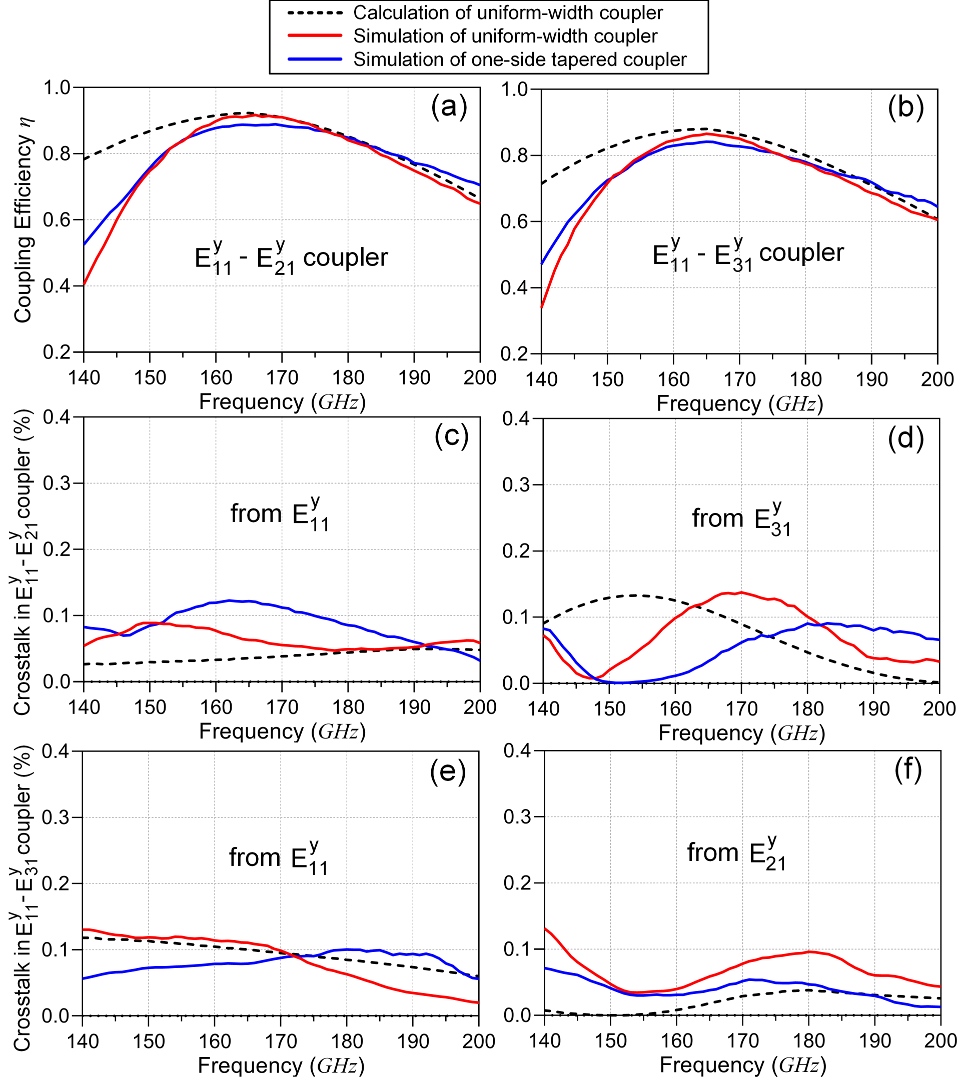


FIGURE 4.15. Calculated and simulated performance of uniform-width and one-side tapered mode couplers: Coupling efficiency of (a) E^y_{11}-E^y_{21} and (b) E^y_{11}-E^y_{31}; Crosstalk from (c) E^y_{11} and (d) E^y_{31} modes in E^y_{11}-E^y_{21} coupler; Crosstalk from (e) E^y_{11} and (f) E^y_{21} modes in E^y_{11}-E^y_{31} coupler.

and convert it to E^y_{21} (or the other modes) with high coupling efficiency. The energy remained in the coupler arm is guided to the tip-end terminal by a bending then radiate out, otherwise strong reflection at the coupler end will cause higher-order mode conversion and interference issues.

The one-side tapered structure sweeps the propagation constant in the coupler arm in a certain range, which could match the propagation constant for wider frequency, similar as the MSL-to-DWG transition discussed in last subsection. Secondly, the one-side tapered structure push the

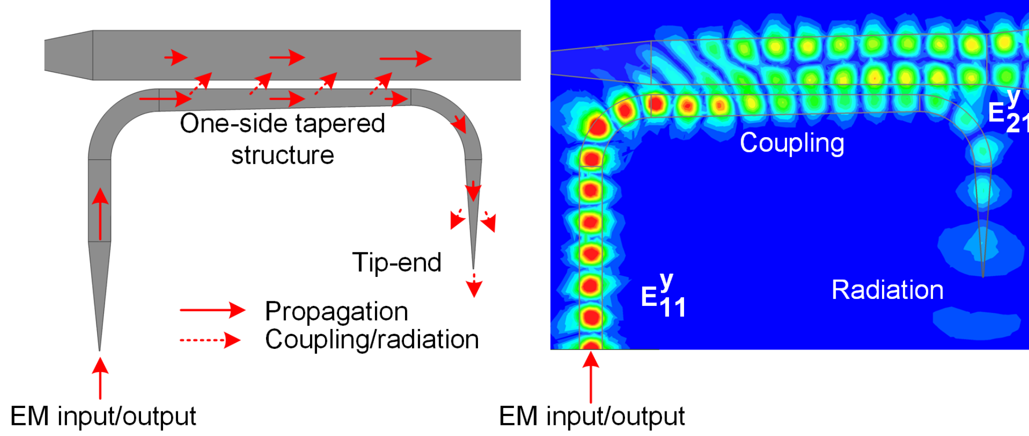


FIGURE 4.16. (a) Top view of the DWG mode coupler, and (b) E field distribution.

EM wave in all frequency range leak to the coupled DWG. Therefore, the one-side tapered structure is adopted to improve the coupling efficiency and bandwidth. Figure 4.16 (b) shows a smooth mode coupling between E^y_{11} and E^y_{21} and the coupler is reciprocal.

There are many types of tapered structures, such as one-side tapered coupler, tip-end terminal and taper transition between sections, employed in the multi-drop Si DWG. The analysis can be done by advanced simulators (Rsoft, Ansys HFSS Lumerical), but the finite element analysis (FEM) and finite-difference time-domain (FDTD) methods don't give a straightforward insight on the structures, especially when an urgent optimization is needed. The light ray tracing method will be introduced to explain the function of basic structures. The light ray tracing method has been introduced to do guided mode solving in textbooks, [**64**] [**24**] [**58**], and it is also a effective approach to analyze the effect on EM waves from the structure. In Figure 4.17, the straight DWG can be divided into three groups: rectangular DWG, one-side taper and symmetric taper DWG. For a guided wave in the rectangular waveguide, the The refractive index of the core n_1 is higher than that of the cladding n_0. Therefore the light ray is confined in the core by total internal reflection with a condition as

$$\varphi < (\pi/2 - \theta_c) \tag{4.91}$$

where φ is the angle between light ray and the baundary of a DWG, and θ_c is the critical angle for total internal reflection $\theta_c = \arcsin(n_0/n_1)$.

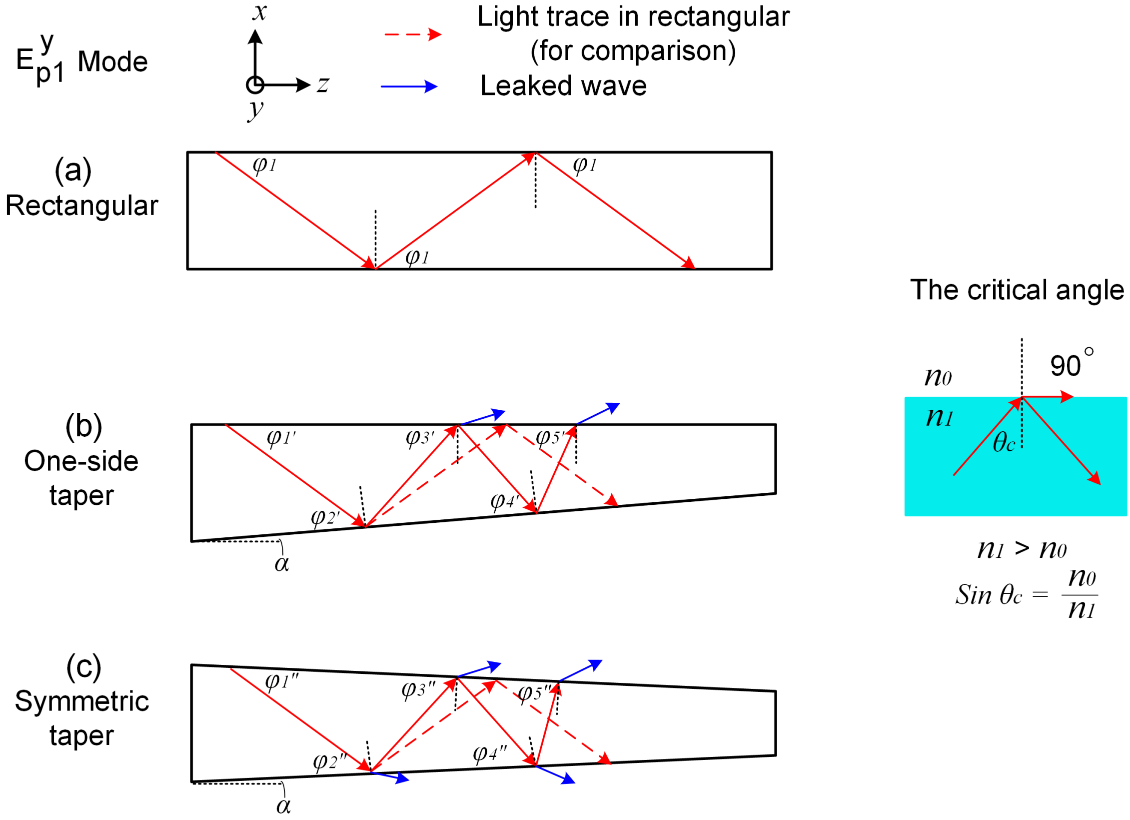


FIGURE 4.17. Light ray trace inside (a) rectangular, (b) one-side tapered and (c) symmetric tapered DWG.

In a given DWG, φ is associate with mode, because it is calculated by Eqn. (4.92). Once the φ is nailed down, the magnitude of the transverse wavenumber is determined. for a pure plane wave, the mode in the given DWG (with known dimension of the cross-section) is also determined. Fortunately, all the modes (E^y_{11}, E^y_{21} and E^y_{31}) in this design are plane waves and they are associate with a φ, and higher order mode has a larger φ. When φ exceeds the condition in Eqn. (4.91), this mode can not exist in this waveguide.

$$\cos(\varphi) = \frac{k_z}{k} = \frac{n_{neff}}{n_1} \tag{4.92}$$

Back to the taper structures in Figure 4.17 (b) and (c): (1) For the one-side taper, φ is always increased at the bottom inclined plane by 2α compared with the last cycle. We take the angle $= \varphi$ a rectangular DWG. Therefore, the angle φ can be calculated as following, $\varphi_1' = \varphi_1$, $\varphi_2' = \varphi_1 - \alpha$,

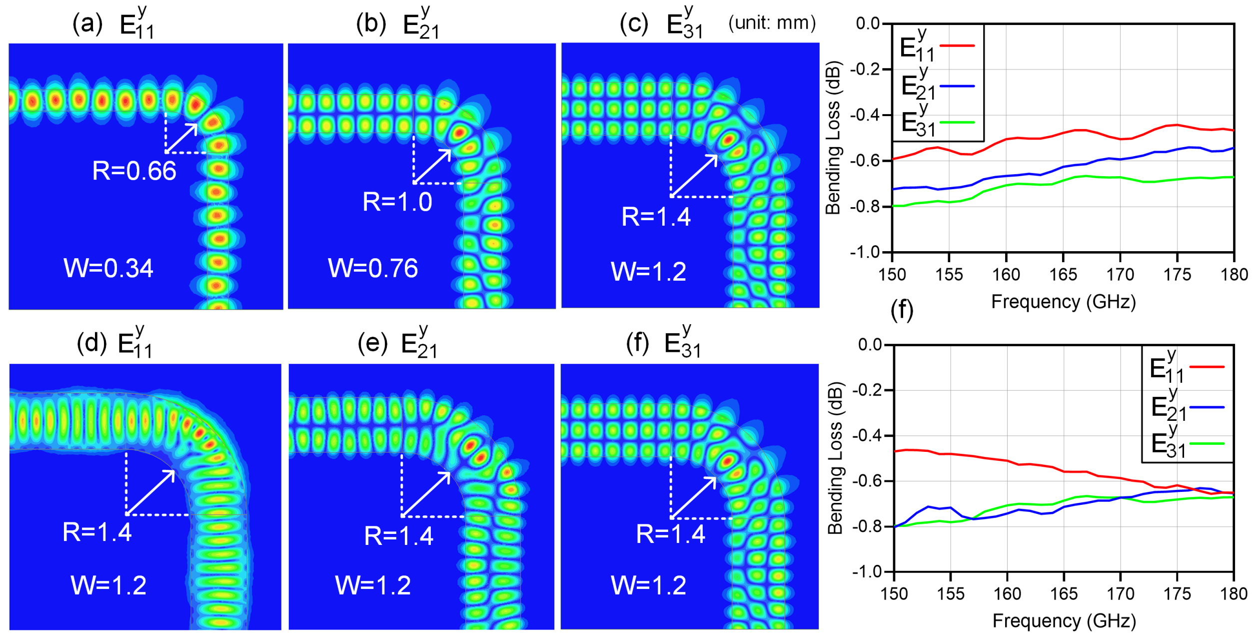


FIGURE 4.18. Bending loss analysis: E field distribution of (a) E^y_{11} in $W = 0.34\ mm$ and $R = 0.66\ mm$, (b) E^y_{21} in $W = 0.76\ mm$ and $R = 1.0\ mm$, (c) E^y_{31} in $W = 1.2\ mm$ and $R = 1.4\ mm$, (d) E^y_{11} in $W = 1.2\ mm$ and $R = 1.4\ mm$, (e) E^y_{21} in $W = 1.2\ mm$ and $R = 1.4\ mm$, (f) E^y_{31} in $W = 1.2\ mm$ and $R = 1.4\ mm$ and (g) their S parameters

$\varphi_3' = \varphi_1 + \alpha$, $\varphi_4' = \varphi_1$, $\varphi_5' = \varphi_1 + 3\alpha$, ... The angle on the top plane exceed the total internal reflection faster than the one on the bottom plane. Therefore, EM waves tend to leak from the top plane in the one-side taper .

In a symmetric taper, the angle φ is increasing more evenly and quickly. Then the EM waves will exceed $(\pi/2 - \theta_c)$ very quick and start to radiate in a sharp tapered structure, such as the tipped terminal.The angle changes as $\varphi_1" = \varphi_1 - \alpha$, $\varphi_2" = \varphi_1 + \alpha$, $\varphi_3" = \varphi_1 + 3\alpha$, $\varphi_4" = \varphi_1 + 5\alpha$, $\varphi_5" = \varphi_1 + 7\alpha$, ... For the tapered transitions, normally a gentle-slope is prefered to avoid undesired mode conversions. If multiple modes are imported form the wider side, the taper can work as mode filters to filter out the higher-order modes when the slope and length of the taper are designed properly. Therefore, when adopting a structure in DWG, we can first analysis it with this method. The situation and function could deffer from scenarios.

Bended DWGs are also used in the proposed multi-mode multi-drop Si DWG, as shown in Figure 4.18. Mode conversion (or coupling) and radiation leakage, causing extra loss, are very common

in a bending dielectric waveguide. According to the mechanism in [**58**], they are related to the wavelength (frequency), bending radius, waveguide width and difference in the index of refraction between the waveguide and cladding. Compared to radiation, mode conversion in a bended triple-mode waveguide is significant, because mode couplers at the end of the triple-mode waveguide will be affected, which leads to degradation in coupling efficiency and crosstalk performance. For a given mode, wavelength and DWG, both radiation and mode conversion are related to the bending radius. That is, the total loss drops with increasing bending radius. The bottom three figures in Figure 4.18 shows the total bending loss, including radiation and mode conversion, for different scenarios: R=0.66 mm for E^y_{11} in a DWG with $W = 0.34$ mm, R=1.0 mm for E^y_{21} in a DWG with W=0.76 mm, and R=1.4 mm for E^y_{31} in a DWG W=1.2 mm. The total bending loss is less than 0.8 dB (17%) for all the cases. Smoothly bended DWG with a large bending radius is preferred to the performance, but it is inflexible to integrate especially if device needs to be compact. Therefore, a design trade-off is necessary when a bending waveguide is adopted in the design.

4.4. Demonstration and Measurement

Besides theoretical analysis, high frequency device strongly demands the help of powerful EM simulators, because every tiny deviation may course significant performance degradation. The multi-mode multi-drop Si DWG was designed and modeled in the full-wave simulator HFSS and measured on-wafer with G-band (140 to 220 GHz) S-parameters testbench. There are two separated parts for the multi-drop channel: Si DWG and transitions on quartz boards.

4.4.1. Fabrication and Assembling.

All parts are fabricated piece by piece in-house with nano-manufacturing process, and then assembled together. Since the multi-drop Si DWG has a relative large dimension (about 50 $mm \times$ 12 mm), it is difficult to fabricate the transition on a comparable size quartz, because 100 μm thick quartz wafer is fragile especially with large size. Therefore, the transition is fabricated on two quartz substrates, as shown in Figure 4.11, but the assembling procedure must be modified accordingly. The fabrication process is similar as the ones discussed in Chapter 3.5, Figure 3.22 and 3.23. The multi-drop Si DWG together with couplers are produced in one piece by DRIE process.

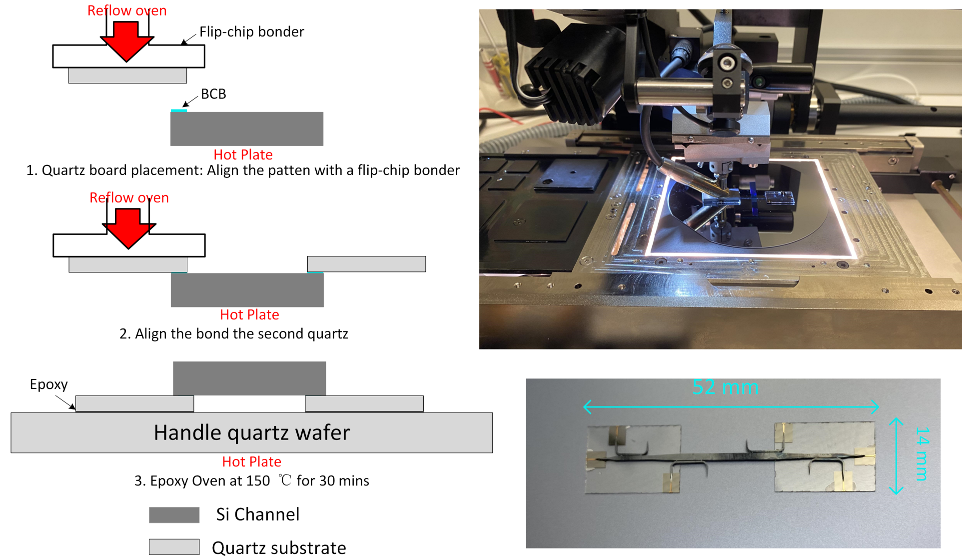


FIGURE 4.19. Assembling process with a flip-chip bonder and photo of the DWG.

Quasi-TEM to E_{11}^{y} coupler with GSG interface is fabricated on a 100-μm quartz substrate using lithography and metal deposition processes.

The assembling procedure is illuminated in Figure 4.19. Different from the SiDWG bonding in Chapter 3, the Si DWG in a larger dimension was put on the vacuum plate and quartz boards are bonded to the DWG, because bondind a small piece component to a larger one is more stable and reliable than bonding them oppositely, as shown in the top right photo in Figure 4.19. The final dimension of the multi-mode multi-drop Si DWG is about about 52 $mm \times 14$ mm.

4.4.2. Measurement Setup and Results.

Two testbenches were setup for the transition and crosstalk measurements. The fist measurement setup includes an Agilent network analyzer (PNA-X N5247A), a pair of Virginia Diodes frequency extension modules (VDI WR5.1-VNAX), WR-5 (140-220 GHz) S-bend waveguides, and a pair of WR-5 probes. The SOLT (Short, Open, Load, Thru) calibration method is employed to set the reference plane at the probe tip. Figure 4.20 shows the G-band S-parameters on-wafer testbench, the ports' return loss (S_{11} and S_{22}), transition loss and partial crosstalk with port on the oppsite sides were tested on this tescbench. However, since the frequency extender station has limitations on rotating probes, another testbench in Figure 4.21 were set to test all the transition

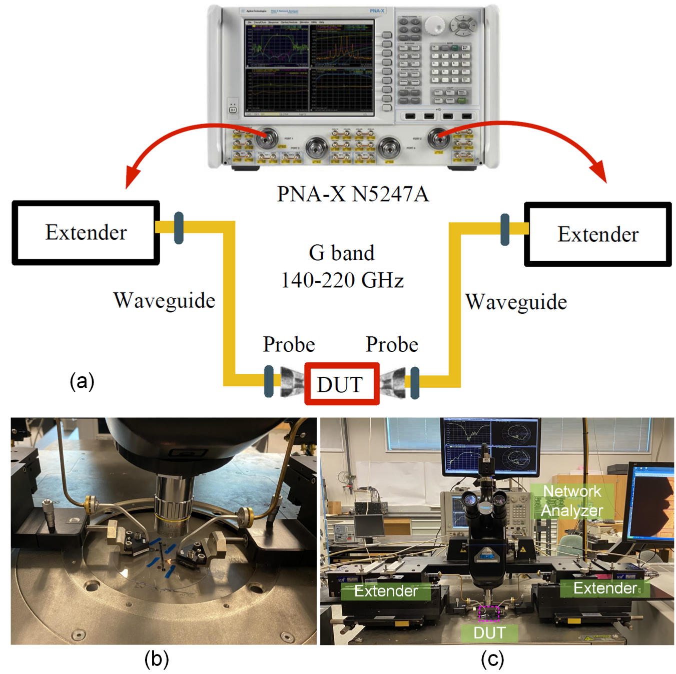


FIGURE 4.20. (a) Measurement setup with network analyzer and frequency extender. Photos of the (b) sample and (c) testbench

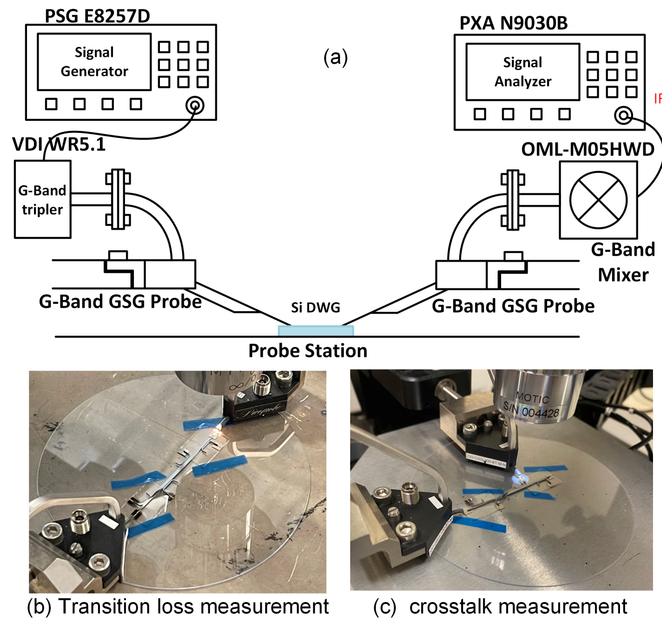


FIGURE 4.21. (a) Measurement setup with tripler and down-convert mixer. (b) Through and (c) crosstalk tests

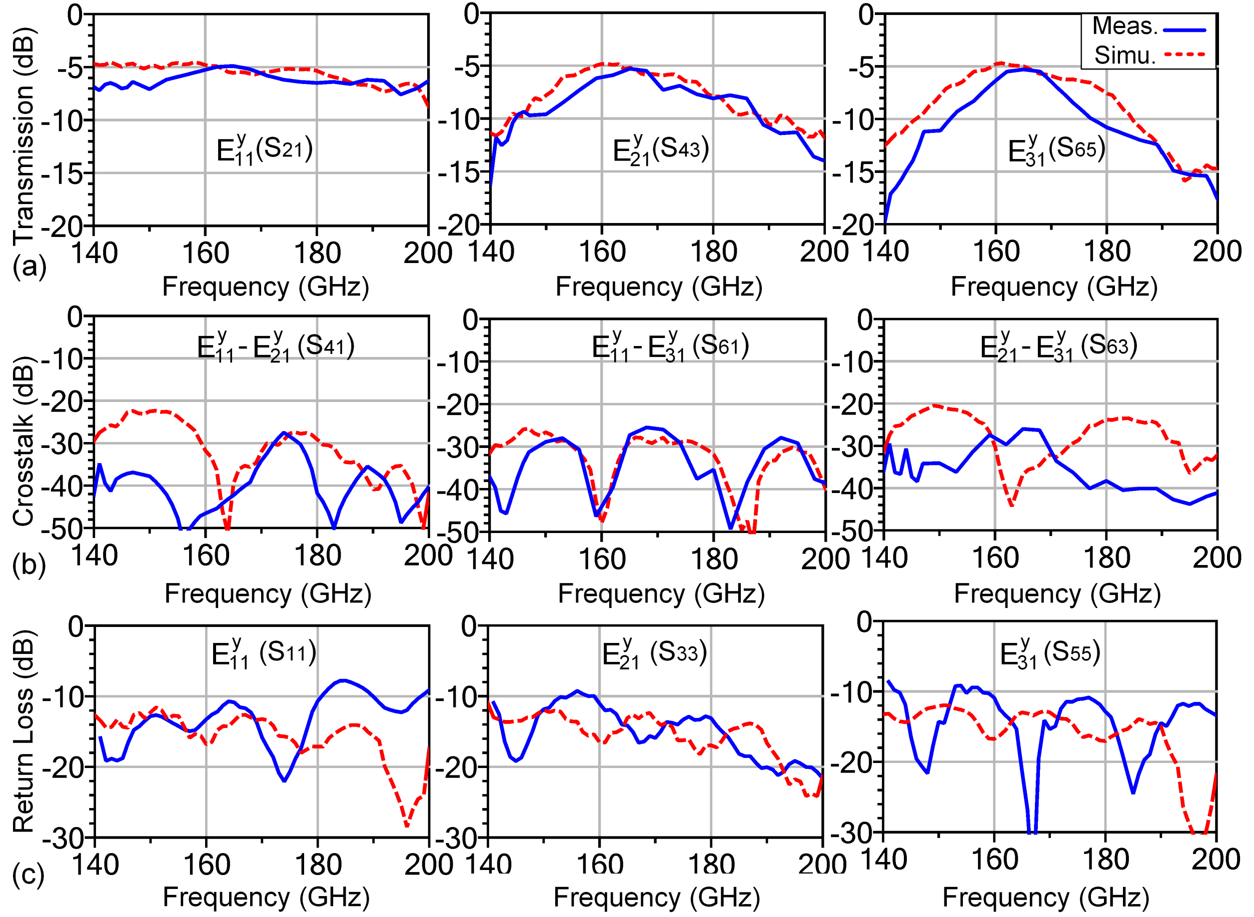


FIGURE 4.22. Simulated and measured S-parameters of the multimode Si dielectric waveguide.

and crosstalk performance. To measure the transition loss from Port 1 to Port 2 accurately, the station was first calibrated with a through, and the received power was recorded. Then the Si DWG replaced the through and tested the received power with the extract same configuration. By comparing the two transition loss, the "S_{21}" were measured.

The simulated and measured S-parameters of the multimode DWG are plotted in Figure 4.22 and results are compared with state-of-the-arts multi-channel transmission over 100 GHz carriers in Table 4.1. The minimum loss is about 5 dB within the 3-dB bandwidth of 143-200 GHz, 151-185 GHz and 155-174 GHz, respectively for the three modes. The measured crosstalk between modes is less than -26 dB. The comparison with SOAs above 100 GHz reveals that the proposed approach achieves competitive loss and bandwidth performances.

Table 4.1. Comparison with the state-of-the-art multi-channel transmission above 100 GHz.

Ref.	**TMTT'18 [22]**	**TMTT'20 [46]**	**IRMMW-THz'21 [47]**	**This Work**
3-dB BW. (GHz)	150.8∼206 151∼171.4	225∼250* 262∼285* 302∼322*	127.7-152.3 168.3-191	143∼200 151∼185 155∼174
Scheme	MDM	FDM	FDM	MDM
Tech.	DWG	Ridged SIW	MSL	DWG
NO. CHNL.	2	3	2	3
Min. Loss (dB)	6.4/6.6	6/8/10**	11.6/13.2	5/5.1/5.3
Crosstalk (dB)	-20	-35	-30	-26

* Read from the figure; ** the total loss of a multiplexer and demultiplexer.

4.5. Conclusion

A sub-THz mode-coupler-based multi-mode multi-drop Si DWG is presented with the theory, analysis, design and demonstration elaborated. This is the first time three-mode division multiplexing based channelization demonstrated on a dielectric waveguide. The design method can be extended to more modes and opens a new direction to more efficiently utilize the extremely broad bandwidth of DWG to materialize high bandwidth density and high energy efficiency multi-drop sub-THz/THz Interconnect to meet the ever-increasing interconnect demands.

CHAPTER 5

Multi-mode and Multi-drop Sub-THz Interconnect

Ever-increasing data generation and transmission demands have been driving great advancements in wireline communications from both electrical and optical approaches for short- and long-distance scenarios, respectively. In the meter range scenario, both electrical and optical approaches face great challenges. That is, the lossy and bandwidth limited channels are the bottlenecks of electrical interconnect. For optical interconnect, the features, such as the required complex fabrication and the high environment sensitivity, increase the power and cost budgets significantly, making it uneconomical for short-distance communications. To mitigate these issues, low loss dielectric channel-based interconnects have been investigated and demonstrated [**65**] [**17**] [**20**] [**23**] [**43**].

However, they are all for point-to-point configurations, not suitable for multi-drop distributed architectures as shown in Figure 5.1. A bunch of nodes integrating transmitters and receivers are connected with multi-drop channels, and each node has individual logical channel to communicate. In optical FDM networks, the add-drop multiplexing is usually realized by the combination of mature optical elements such as ring resonator, phase-shifted grating, Bragg grating, arrayed waveguide grating, circulator, and coupler on the platform of silica-based planar lightwave circuits and fiber array [**66**] [**67**]. Using the directional coupling between two adjacent wave-guides or the leaky wave of a single deformed waveguide. THz add-drop multiplexer have been proposed based on parallel-plate waveguides and Si substrates. A waveguide bragg grating based add-drop multiplexer for several THz carrier waves in the vicinity of 140 GHz modulated up to 6 Gb/s are demonstrated experimentally [**68**].

This chapter presents an mode division multiplexing (MDM) based multi-drop sub-THz interconnect prototype with three modes specifically, i.e. E_{11}^{y}, E_{21}^{y} and E_{31}^{y} through a single high resistivity Si DWG. The multi-mode multi-drop Si DWG channel has been fully discussed in the Chapter 4, so the channel design will not repeat in Chapter 5. Section 5.1 introduces the system architecture, analyze the link budget and bandwidth budget aiming at a data rate of 25 Gb/s for

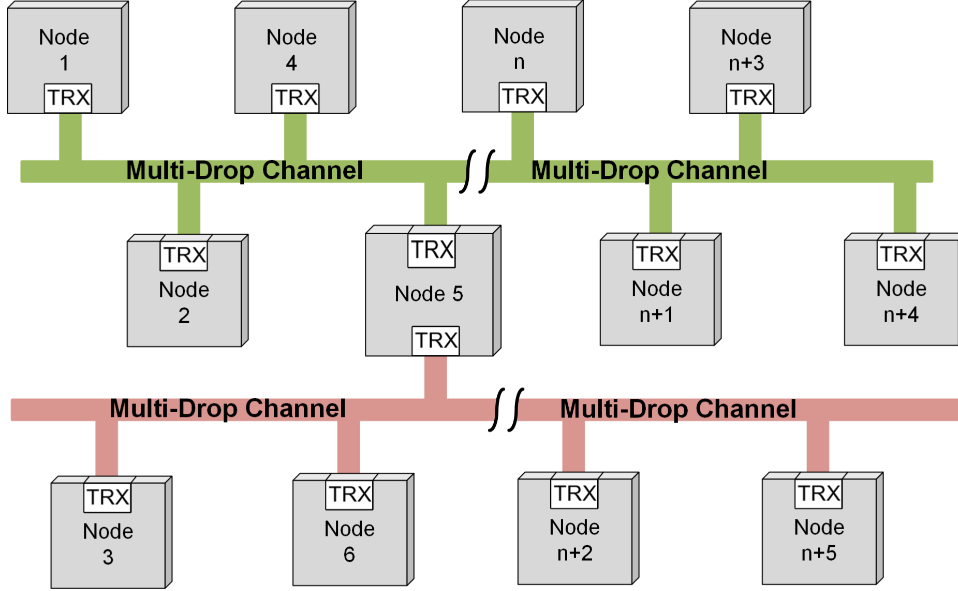


FIGURE 5.1. A communication networks with multi-drop channels.

each channel. Section 5.2 and Section 5.3 propose a improved transmitter and receiver. Section 5.4 focuses on the fabrication and package design. In section 5.5, the multi-mode multi-drop sub-THz interconnect is measured and achieves data rates of 24 Gb/s, 22 Gb/s and 19 Gb/s for E^y_{11}, E^y_{21} and E^y_{31} modes, respectively with the BER better than 10^{-12}. The demonstrated aggregate data rate of the three channels is 65 Gb/s with the energy efficiency of 1.6 pJ/b.

The innovation of this chapter is the brand new sub-THz interconnect architecture. To the authors' knowledge, this is the first time to demonstrate multi-mode multi-drop DWG based interconnect. The interconnect system takes advantages of multiple modes supported by the Si DWG and builds three individual channels for data transmissions for multiple nodes at different locations. The demonstrated multi-mode multi-drop sub-THz interconnect systems also open a new path and can scale to more modes to support more logic channels per physical link and can be extended to multi-dimension, two-/three- dimension, interconnect systems.

5.1. MDM Implement: Multi-mode and Multi-drop sub-THz Interconnect

The system diagram of the multi-drop sub-THz interconnect is illuminated in Figure 5.2. Similar as the dual-band sub-THz interconnect system, the proposed multi-drop sub-THz interconnect consists of two parts: the active transceivers and passive multi-drop channel. The multi-drop Si

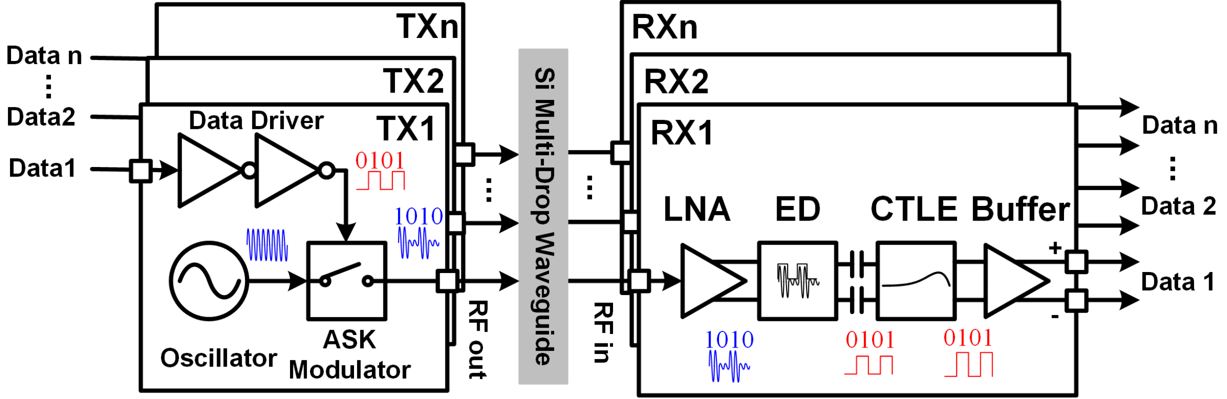


FIGURE 5.2. Multi-drop system diagram.

DWG channel builds multiple individual channelization for transmitters and receivers, and enables full-duplex communication simultaneously within one physical link.

Several key features contribute its high energy efficiency. First, the high-efficient and broadband mode coupler and MSL-to-DWG transitions, as well as the low loss channel relax the link budget, thus eliminating PA. Second, the high isolation between different modes introduces minimum interference, thus allowing non-coherent detection at the receiver by removing power hungry clock generation and synthesizing. Third, ultra-wide bandwidth of DWG enables ultra-high speed data transmission which not only boosts bandwidth density but also allows using simple and power efficient modulation scheme, such as OOK. Therefore, as shown Figure 5.2, each transmitter/receiver set adopts energy efficient architecture. Digital data is shaped by inverter driver in the transmitter and up-converted to 165 GHz by the switch based OOK modulator. At the receiver, the RF signal is boosted by an integrated LNA before feeding an ED to recover the data.

All the OOK signals are modulated at 165 GHz with the transmitters. The Si multi-drop channel has integrated mode coupler based multiplexers, with which RF signal from different transmitters are transferred into different modes and combined together in the common waveguide. On the receiver side, RF signals in different modes are extracted by the corresponding DWG mode couplers (multiplexer). To support a higher date rate of 25 Gb/s, the receiver was improved according the new specifications. A broadband LNA is employed in receivers to improve the noise and gain performance, then improve the sensitivity significantly, which is the foundation to transmit wider bandwidth RF signals. ED is still used to recover the OOK signal. Since the responsivity R_v and

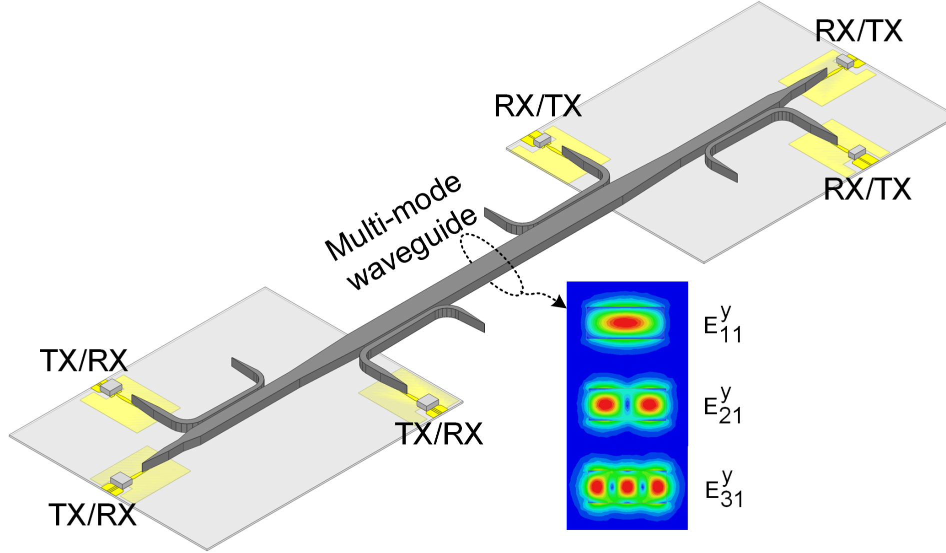


FIGURE 5.3. Si multi-drop waveguide and package.

NEP has improved by the LNA, ED can use smaller *RC* loading to support faster speed. The baseband bandwidth is also increased by the continuous time linear equalization (CTLE) for higher date rate transmission.

Both transmitter and receiver are fabricated in standard 65-nm CMOS technology with bump pads, which dramatically improves the packaging flexibility and reduces the loss from interfaces, because narrow-band and lossy bonding wires can be removed from the RF signal chain. furthermore, chipset can move closer to the DWG channel. The simplified package structure is illuminated in Figure 5.3. Two quartz boards are employed to hold the multi-drop channel and CMOS chipsets. MSL-to-DWG transitions are fabricated on a quartz board convert the quasi-TEM RF signal on the transmission line to the fundamental E^{y}_{11} mode signal in Si waveguide. After that, the fundamental E^{y}_{11} signal can be further converted to higher-order modes E^{y}_{21} or E^{y}_{31} by mode couplers. Signals in the three modes (i.e. E^{y}_{11}, E^{y}_{21} and E^{y}_{31}) in the common waveguide are isolated from each other in principle, therefore can propagate together along the common waveguide. On the receiver side, RF signals in different modes are extracted by the corresponding DWG mode couplers and recovered by ED. In reality, crosstalk exists in the multi-drop channel due to the non-perfect mode coupler and mode conversions. However, the crosstalk could be lower than -26 dB that significantly reduce the

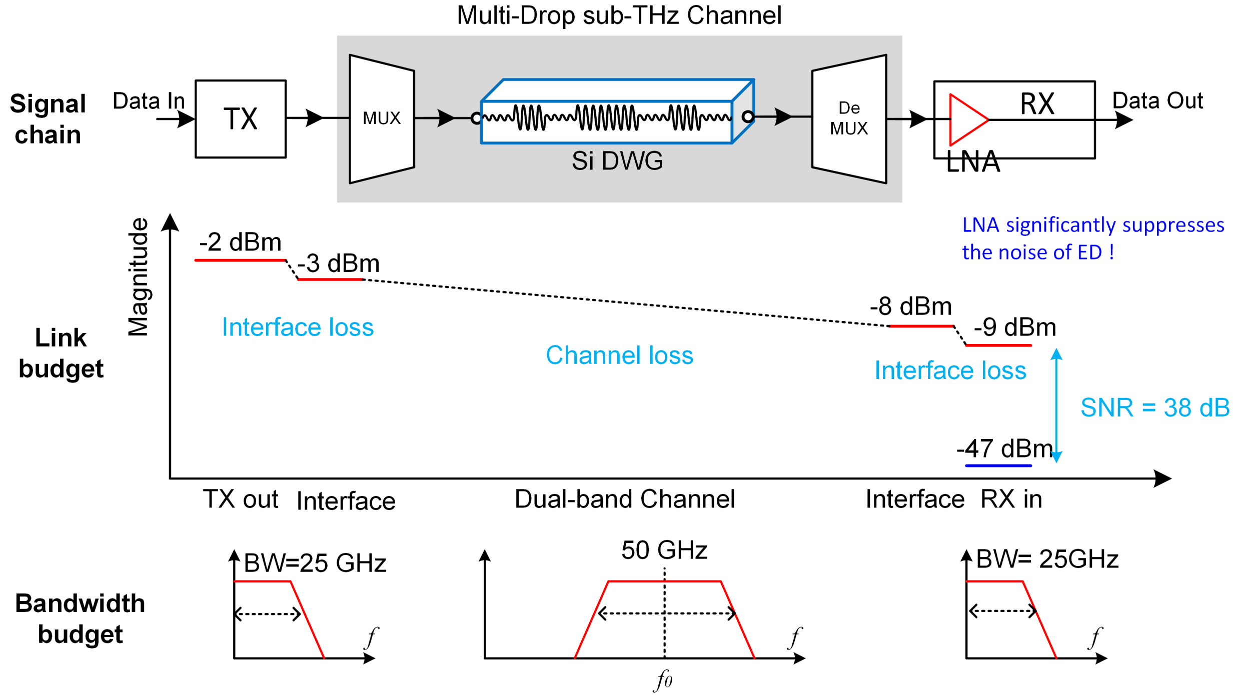


FIGURE 5.4. Link budget and bandwidth budget of the multi-drop sub-THz interconnect.

interference form the other sub-channels, and it can meet the SNR requirement for OOK signals, which is about 17 dB.

Again, the the link budget and bandwidth budget must be calculated carefully to establish a successful communication link, as shown in Figure 5.4. The target data rate for each sub-channel is 25 Gb/s (totally 75 Gb/s). To support higher data rate and relax the link budget an LNA with about 26-dB voltage gain is adopted as the RF front end in the receiver. The noise figure of the LNA is about 7 dB with a 3-dB bandwidth from 140 GHz to 190 GHz. The NEP of ED is suppressed significantly from 15 $pW/\sqrt{Hz}$ ($\approx -83\ dBm/\sqrt{Hz}$) to 100 $fW/\sqrt{Hz}$ ($\approx -100\ dBm/\sqrt{Hz}$). The calculation and simulation of NEP will be discussed in the receiver section. The noise contribution from bandwidth (25 GHz) is about 53 dB, therefore, the sensitivity of the receiver is about -47 dBm, to maintain the 17 dB SNR and 10 dB margin, the minimum RF power of -20 dBm is required at the input of the receiver, which is relatively easy to achieve in this multi-drop Si channel, because its typical transition loss is 6∼7 dB. The bump pad interface also has excellent loss of about 1 dB

at sub-THz. As a result, the only -11 dBm of RF power is required at the transmitter output, so the afford is paid more on the bandwidth budget.

For 25 Gb/s OOK signal, a 25 GHz bandwidth for baseband and 50 GHz bandwidth for RF components are required. The measured 3-dB bandwidth of channel are 57 GHz, 36 GHz and 28 GHz for E_{11}^{y}, E_{21}^{y} and E_{31}^{y}, respectively, So the bandwidth is a little tight for the E_{21}^{y} and E_{31}^{y} modes. The switch-based modulator in the transmitter, LNA and ED in the receiver has a sufficient bandwidth or equivalent speed. An other bandwidth constrain lies in baseband circuits, such as the inverter-based data driver in the transmitter and baseband amplifier in the receiver. It is difficult to achieve an absolute bandwidth of 25 GHz in 65-nm CMOS process. The conquer this issue, a CTLE is employed to compensate the gain drop at high frequency. In the final demonstrated system, the degradation of data rate performance is majorly caused by the bandwidth limitation.

5.2. Transmitter

Figure 5.5 (a) shows the building blocks and schematic of the transmitter that consists of a cross-coupled oscillator as the carrier generator and switch as the OOK modulator. Same as the oscillator discussed in Chapter 3.3. The oscillator was designed with power maximization approach as well. TL_1 and TL_2 are utilized to adjust the loop gain phase and the transformer is to match the optimum loading.

A high-speed OOK modulator needs a bandwidth as wide as the RF signals of 50 GHz, so the multi-stage shunt single pole single throw (SPST) architecture is adopted in this design. Shunt inductors (i.e. L_3, L_4 or L_5) are used to resonate the parasitic capacitance C_{ds} and reduce the loss. Each stage resonates at different frequencies, making the three-stage switch achieve much wider bandwidth. Besides that, large inductors R_6, R_7 and R_8 ($> 1\ k\Omega$) are employed to block the body capacitance to the substrate, which makes the transistor as a NMOS in SOI technology, then significantly improve its speed and insertion loss performance. The major advantage of building the device over the SOI wafers are: The operating speed increases by 20–30% in comparison to the devices on bulk silicon. The devices fabricated over the bulk silicon operate at relatively low switching speed because of the presence of the large volume of semiconductor material underlying the devices and hence more charge is needed to turn on and off; Higher device packing density

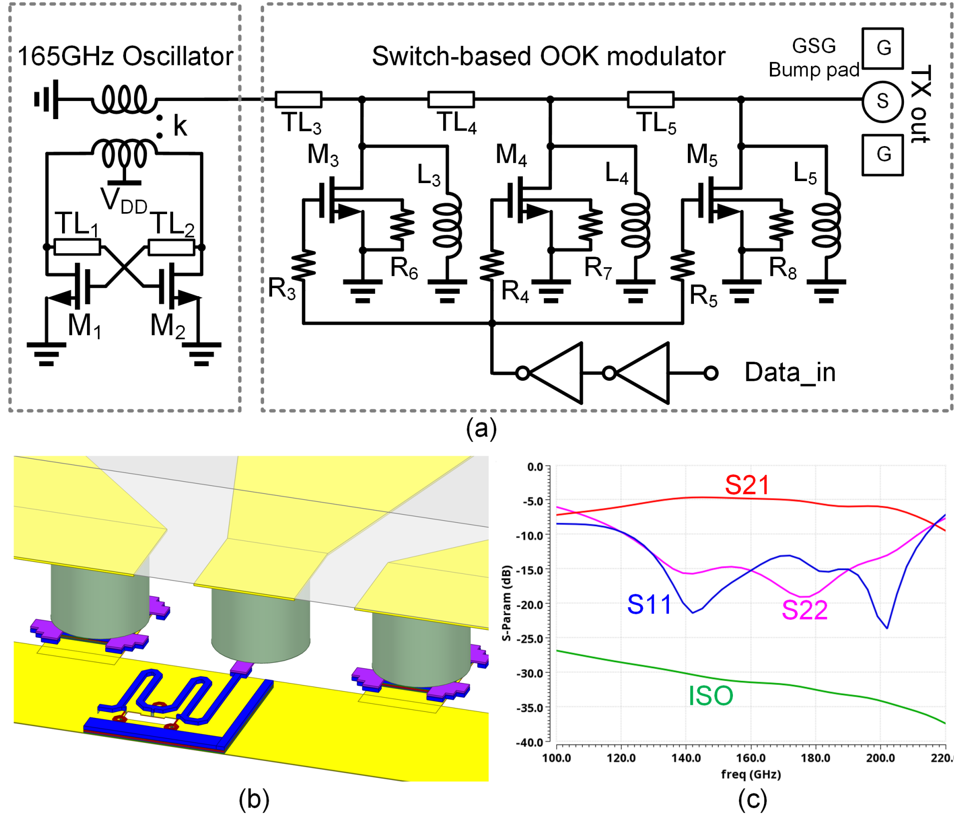


FIGURE 5.5. (a) Schematic of the transmitter. (b) EM modeling and (c) simulated S parameter of the switch modulator.

can be achieved; Minimizes the current leakage; Lower the power consumption.Those advantages benefit the on-chip passive circuits, but are not suitable for active components. layout of the switch is modeled with bump pads and interfaces, as shown in Figure 5.5 (b). The simulated S-parameters are shown in Figure 5.5 (c). The 3-dB bandwidth is more than 80 GHz with a typical insertion loss of 5 dB. The isolation is increased as well by multiple stages.Normally, R_g is preferred as large as possible to eliminate the reflection. However, a large R_g will affect the data rate due to a large RC constant. With the trade-off, 150-Ω resistor is used to minimize the insertion loss and maximize the data rate.

The transmitter was tested individually, as shown in Figure 5.6. The RF power and spectrum are measured with a down-convert mixer and spectrum analyzer. Figure 5.6 (c) shows that the transmitter deliveries a output power of -3.2dBm with the DC power consumption of 13.2mW at 166.344 GHz.

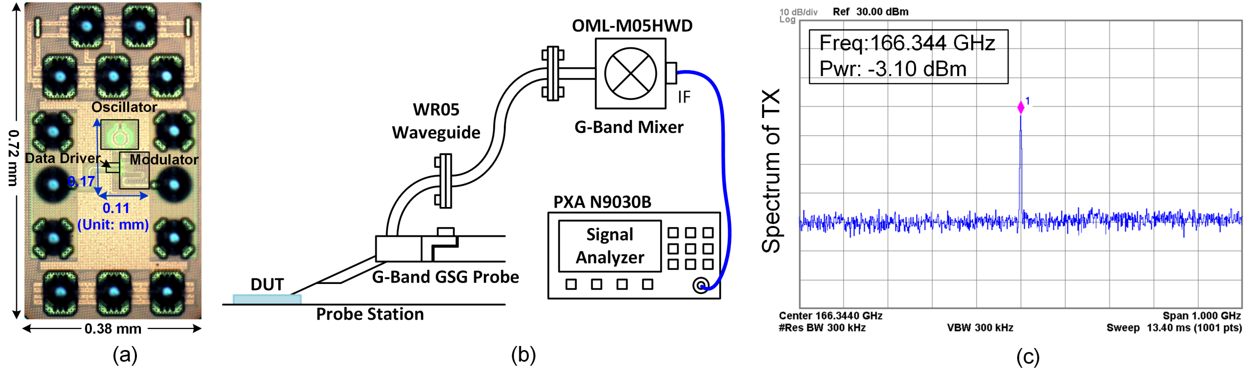


FIGURE 5.6. (a) Die photo of the transmitter, (b) measurement setup and (c) measured power and spectrum

5.3. Receiver

The receiver plays a more important role in this system. As discussed in the link and bandwidth budget analysis, a bandwidth of 50 GHz and high sensitivity receiver is needed to achieve the 25 Gb/s data rate, which is extremely challenging at sub-THz, So as the broadband baseband circuit. As shown in Figure 5.7, the receiver consists of a LNA, ED, CTLE and buffer. Frequency-insensitive direct detection requires wide bandwidth of signal chain and suffers from poor noise performance. To deal with this issue, a 3-stage LNA is employed to suppress the noise and enhance the sensitivity. A three-coil neutralization transformer is proposed for the first common-gate stage that aims at low noise figure (NF) and broad bandwidth at sub-THz. The following two common-source stages are neutralized by capacitors. It provides 24 dB voltage gain with 7dB NF over 140 180 GHz. The input-referred NEP is improved from 15 $pW/\sqrt{Hz}$ ($\approx -83\ dBm/\sqrt{Hz}$) to 100 $fW/\sqrt{Hz}$ ($\approx -100\ dBm/\sqrt{Hz}$). The LNA consumes 15.9 mW with a supply voltage of 1 V. CTLE is design to compensate the voltage gain drop at high frequency. The bandwidth of baseband is increased from 14.9 GHz to 33.6 GHz. The receiver is implemented within a small area and low power consumption, which allows them to be integrated conveniently.

Talking about the receiver, the most critical metric is the NF in linear components and NEP in non-linear components, because they that indicate degradation of the SNR that is caused by components in a signal chain then directly determine the sensitivity of the receiver. In a cascaded

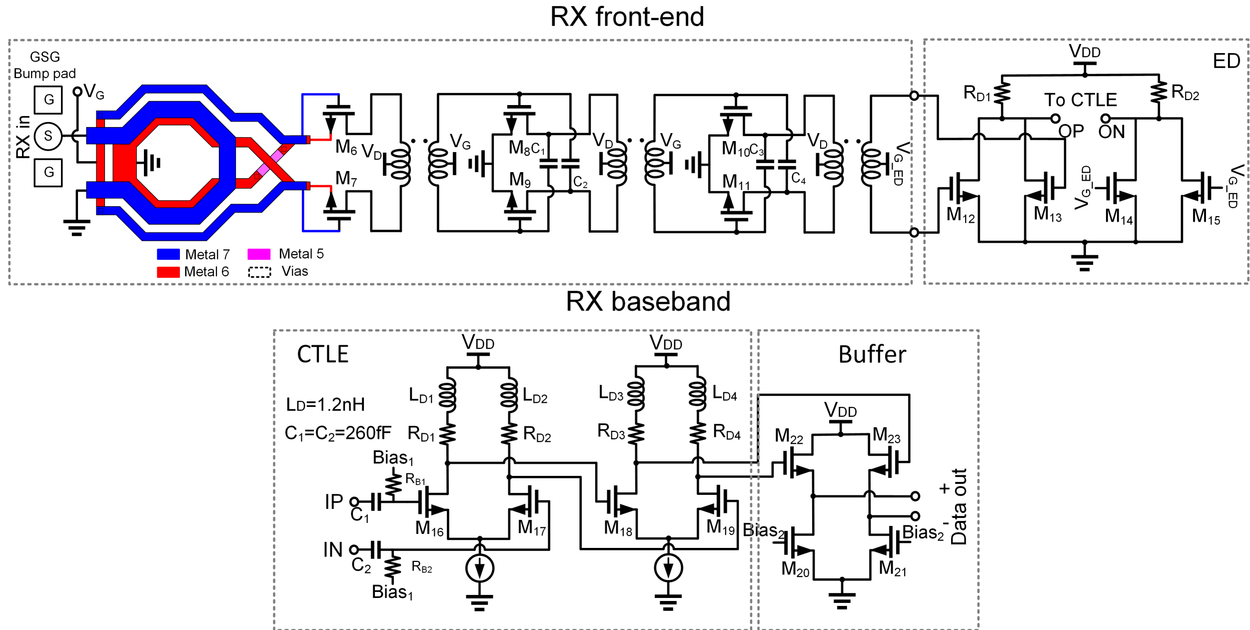


FIGURE 5.7. Schematic of the receiver.

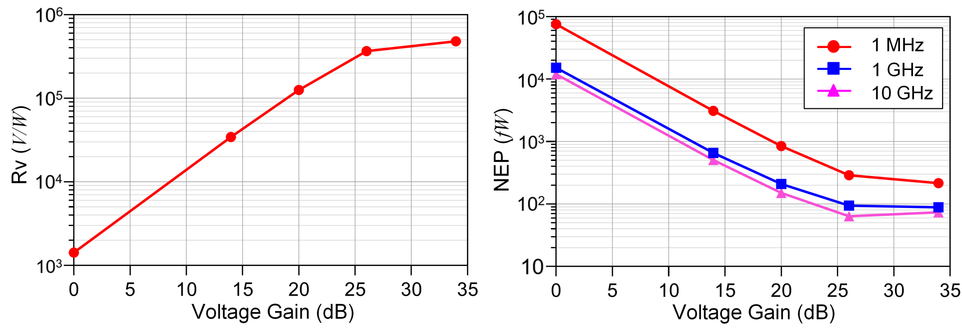


FIGURE 5.8. Simulated R_v and NEP versus LNA's volatage gain.

device, the overall NF is

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... \tag{5.1}$$

where F represents the NF of the cascade, F_1 is the noise figure of the first and F_2 is the noise figure of the second component; G_1 the power gain of the first component and G_2 the power gain of the second component.

Similar in non-linear direct detection receivers, the noise from following stages, i.e. ED, is suppressed by the voltage gain of LNA and LNA itself contributes much lower noise. The principle

can be verified with simulations, as shown in Figure 5.8. If a variable-gain LNA is inserted in front of the ED, both the responsivity R_v and input-referred NEP will be improved. When the voltage gain exceed reach about 26 dB, the responsivity R_v starts to saturate and the overall NEP is determined by the LNA. The noise at 1 MHz is a litter higher than the one at 1 GHz and 10 GHz because of the low-frequency flicker noise.

5.3.1. RF Front-end (LNA and ED).

As discussed previously, the noise and sensitivity performance is majorly determined by the RF Front-end in the receiver. A wide-band LNA is proposed in this section with novel neutralization matching networks to compensate the parasitic capacitance (C_{GS} and C_{GD} at gate node that drops the gain significantly.

Common gate structure draws more interest than common source amplifier due to the wide-band matching performance, which is realized as $1/g_m$ of the input transistor. However, the noise performance of the the common-gate stage is limited due to the low gain of $1/g_m$.

$$F \approx 1 + \frac{\gamma g_{d0}}{g_m^2 R_S} = 1 + \frac{\gamma}{\alpha}|_{g_m R_S = 1} \tag{5.2}$$

where γ represents the process dependent parameter,$\alpha = g_m/g_{d0}$, g_{d0} is the drain admittance when $V_{DS} = 0$, and R_S is the source impedance which is 50 Ω. The NF is constrained by the input condition of $g_m R_S = 1$, which limits the arbitrarily increasing of g_m while maintaining g_{d0}. Thus a decoupling mechanism between input matching and NF characteristics is proposed to address this problem. Inserting an inverting gain, A, between gate and source terminal. There are several ways to implement inverting gain including the active method and the passive method, but passive realization is more attractive in high-frequency design for the consideration of extra noise introduced by active transistors. For the passive method, capacitor crosscoupled technique and transformer coupled technique has been proposed to realize g_m boosting.

In Figure 5.9 (a), a new method based on the 3-coil transformer for mm-wave LNA design. This transformer used for input matching contains 3 inductors, which is different from the conventional 2-coil transformer. The inductor L_1 connects to the input, inductor L_2 connects to the source of the transistor with cross-coupled structure, and inductor L_3, connects to the gate of the transistor, and this transformer has 3 coupling coefficients, coupling coefficient of L_1 and L_2, L_1 and L_3, L_2

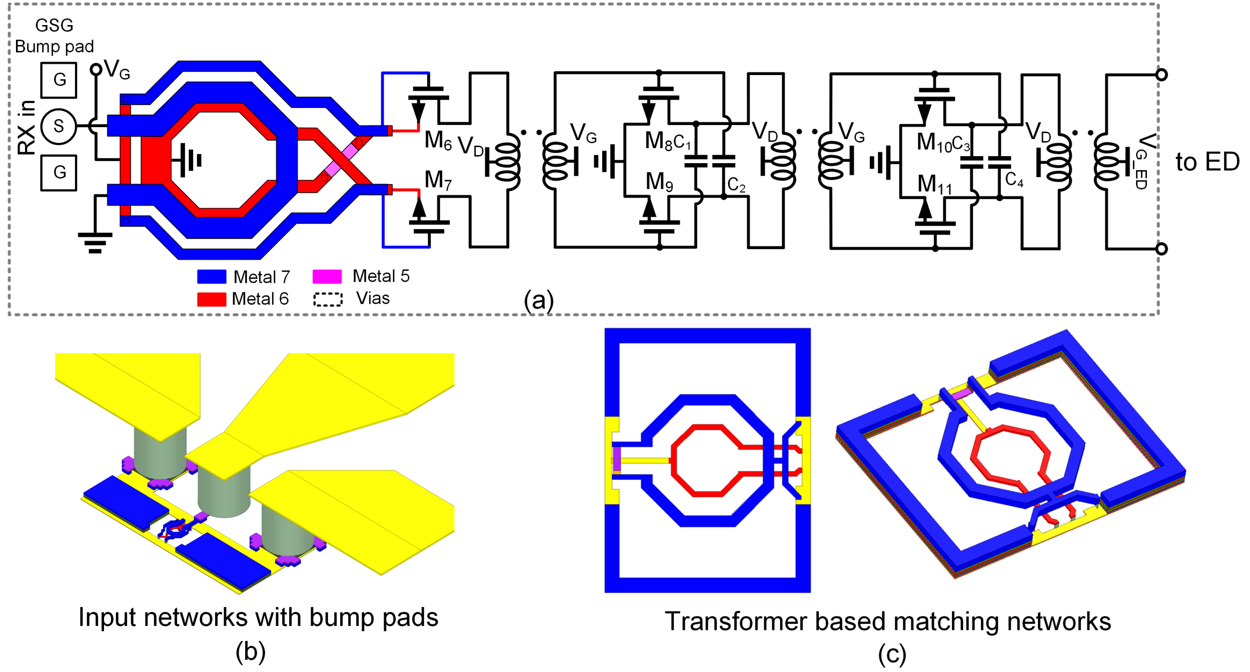


FIGURE 5.9. (a) Schematic of LNA. EM modeling of the (b) input matching and (c) transformers.

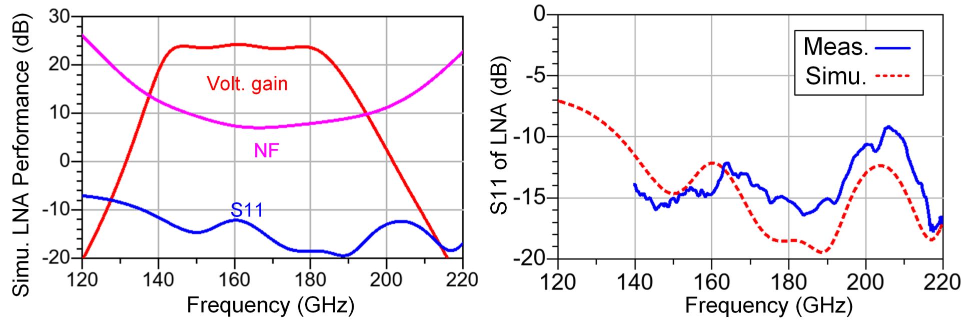


FIGURE 5.10. Simulated S parameters of the LNA.

and L_3, are k_{21}, k_{21} and k_{32}, respectively. The transformer transfers the signal from input to the gate and source terminals with a cross-coupled structure to compensate the loss due to C_{GS}, thus increasing the Δ_{GS} and improving the noise performance.

capacitor neutralization is alos utilized in this LNA. Capacitors C_n connected between gates and drains of the opposing transistors in the differential pair behave as negative capacitances in the differential operating mode, acting against C_{GD} capacitances of the transistors themselves.

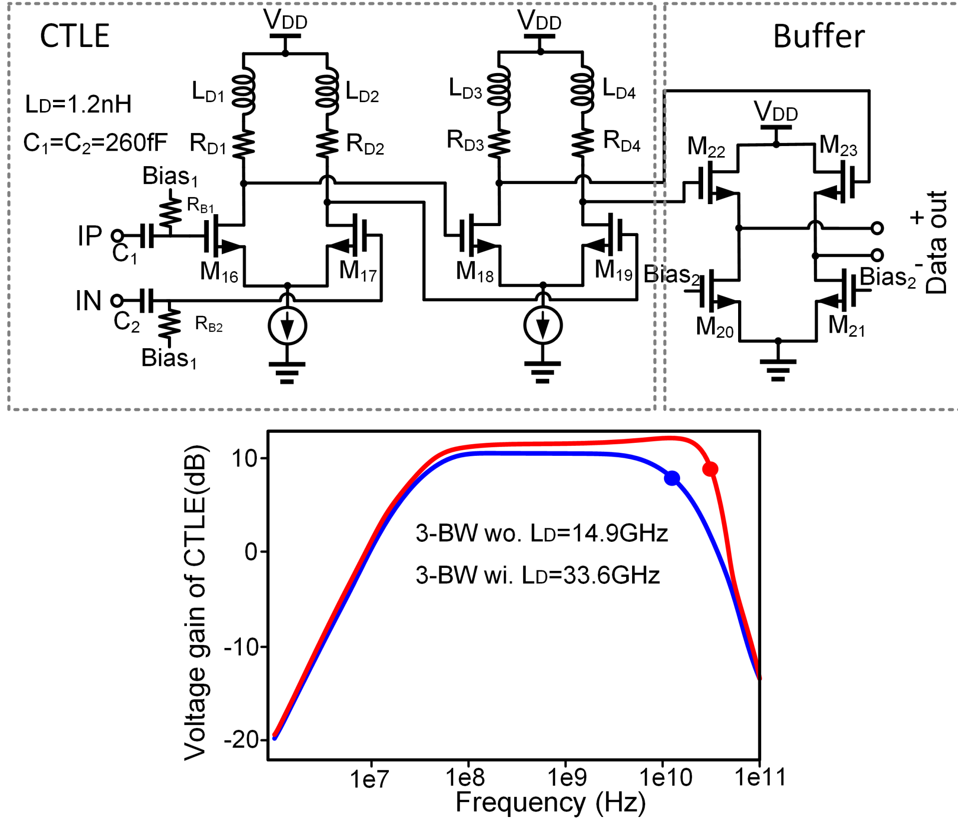


FIGURE 5.11. Schematic and simulated voltage gain of the CTLE.

Theoretically, if those capacitors are equal to C_{GD} and connected at the same node as C_{GD}, the gate-drain capacitances are completely canceled, resulting in an unconditionally stable stage. An additional advantage of this structure is an operation in the differential mode, leading to a closed signal current loop inside the differential pair and facilitating the circuit operation modeling. Due the extra parasitic at the nodes, it is better to tune optimize C_n and get the highest G_{MAX} at the given frequency. The boosted gain at 165 GHz is plotted in Figure 2.14, and the G_{MAX} and K-factor are dramatically boosted to 12 dB and 2, respectively.

The EM modeling of the matching networks are depicted in Figure 5.9 (b) including the GSG bump pads. The simulated and measured S_{11} are plotted in Figure 5.10. The simulated voltage gain is 23 dB with a 3-dB bandwidth of 140 to 188 GHz, and typical NF is 7 dB. Since the LNA is cascaded with the ED, only S_{11} is able to test. The measured S_{11} agrees the simulation very well.

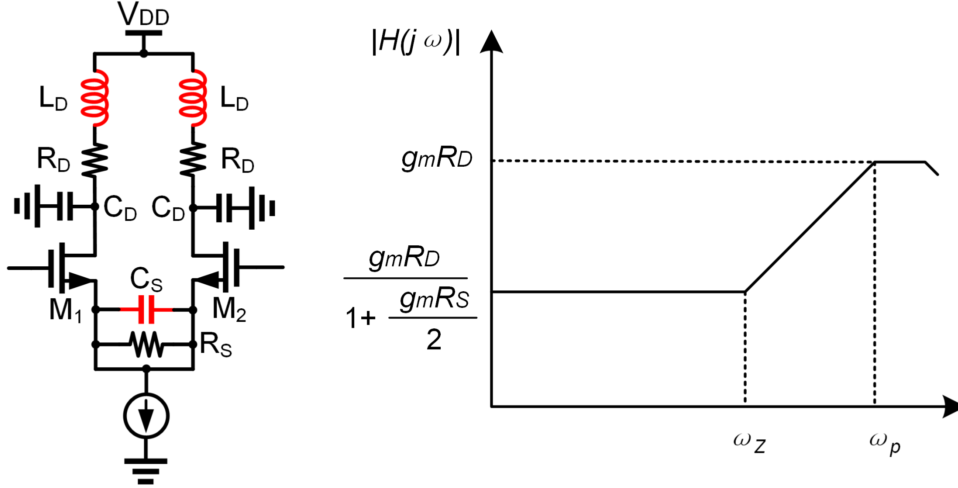


FIGURE 5.12. Schematic CTLE unit and its frequency response.

5.3.2. Baseband CTLE and Buffer.

The limitation of the bandwidth of baseband circuits is another constrain of the data rate. There is a trade-off between the voltage gain and bandwidth. Normally, large load resistor R_d brings in larger voltage gain, but reduce the speed by increasing RC time constant. A normal common gain stage that achieves 10 dB gain has a 3-dB width up to 14.9 GHz in 65-nm CMOS, as shown in Figure 5.11.

continuous time linear equalization (CTLE), as shown in Figure 5.12 are widely used in broadband wireline systems. The most common approach to creating a boost at high frequencies incorporates resistive and capacitive degeneration in a differential pair, as shown in Figure 5.12. It can be readily proved that the circuit's transfer function,

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{-g_m(R_D + L_D s)(R_S C_S s + 1)}{R_S C_S s + 1 + g_m R_S/2} \tag{5.3}$$

where g_m denotes the transconductance of M1 and M2 and channel-length modulation is neglected. The stage exhibits a zero and a pole, respectively:

$$\begin{cases} \omega_{z1} = \dfrac{1}{R_S C_S} \\ \omega_{z2} = \dfrac{R_D}{L_D} \end{cases} \tag{5.4}$$

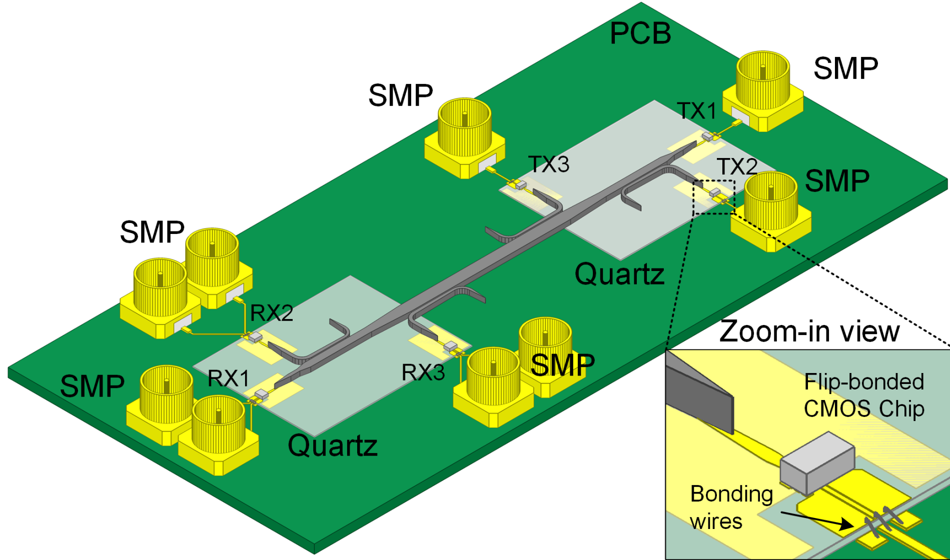


FIGURE 5.13. Package design of the multi-drop sub-THz interconnect

$$\omega_p = \frac{1 + g_m R_S/2}{R_S C_S} \tag{5.5}$$

and the magnitude of its response varies from $g_m R_D/(1 + g_m R_S/2)$ at low frequencies to $g_m R_D$ at high frequencies as shown in Figure 5.12. In this design, only L_D is adopted to boost the high-frequency gain and 3-dB bandwidth to 33.6 GHz, as shown in Figure 5.11.

5.4. Fabrication and Packaging

The transmitters and receivers chips are fabricated in a 65nm CMOS technology with the size of $0.38 \times 0.72\ mm^2$ and $0.65 \times 0.77\ mm^2$, as shown in Figure 5.13. The process has 70-μm diameter bump pads that enable short interconnection to the transition and reduce the mismatch and insertion loss. The passives including waveguide and transition board are fabricated in-house. The multi-drop waveguide is etched from 4-inch Si wafer in a piece. The waveguide is in a length of 5.2 cm, which is limited by the available wafer size for the deep Si etch machine, but it can extend to meter range due to the low-loss Si material. The detailed fabrication processes of transition board and DWG are exactly same with the ones introduced in Chapter 3.5.

For the sub-THz interconnect, the package design is extremely challenging and critical to the performance. The entire package configuration on a PCB mother board is shown in Figure 5.13.

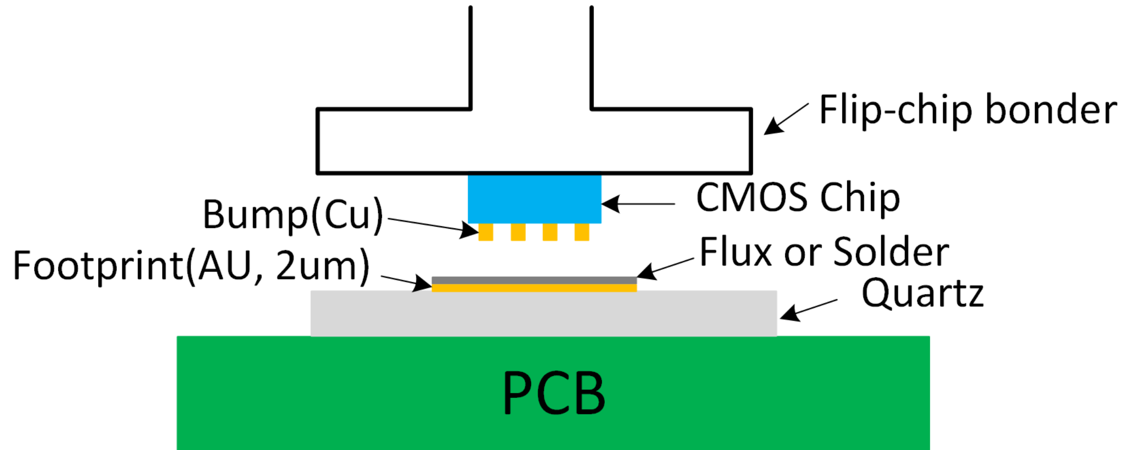


FIGURE 5.14. Flip-chip bonding process for CMOS dies

Since there are multiple elements need to assemble and form the system, the assembling procedure requires significant consideration. Six transmitters and receiver chips bonded precisely to a quartz board together with the Si DWG channel by a flip-chip bonder. Then the interconnect board is attached on a PCB mother to feed the DC supplies and baseband OOK signals. The sub-THz signal only communicates in the waveguide channel and thin quartz board. The baseband signal (up to 25 GHz) travels through PCB, bonding wires and quartz board, and connect to testing instruments with SMP connectors. The packaging procedure is design according to the components dimensions, reflowing temperature and distance to other component.

The CMOS chips has thinner thickness (300 μm) than Si DWG in 525 μm, which will not block other components bonding to the quartz board. Therefore, the CMOS chips are flip bonded to quartz board in the first step. Since quartz board with 2-μm Au metal on the top, which is not a commercial materials used in the industry. The recipe for flip-chip bonding needs to debugged by tuning the reflowing temperature (200∼210 $°C$) and time (10∼15 seconds). The materials and instrument (Finetech Fineplacer PICO A4) used for chip bonding shown in Figure 5.14.

The detailed packaging process is introduced in Figure 5.15. First step is bonding the chips to the quartz boards one by one. The alignment and bonding can be done very accurately (< 5 μm) with a pick-and-place flip-chip bonder. Then, two quartz boards with chips are bonded to Si DWG channel on each side. After this step, the core of the multi-drop sub-THz are formed. In order to test the performance, the core device is mounded on and PCB and connect the baseband and DC

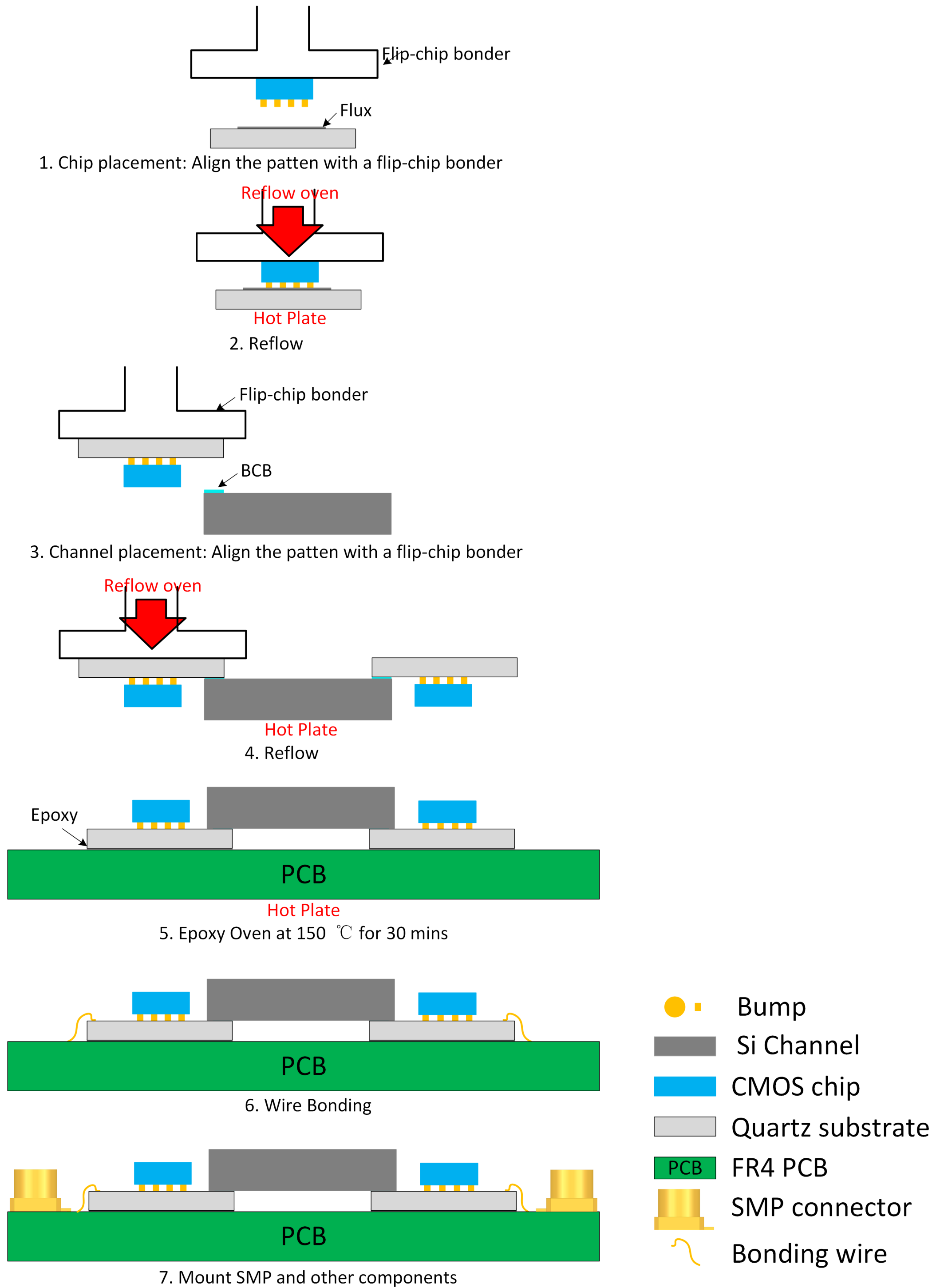


FIGURE 5.15. System packaging process

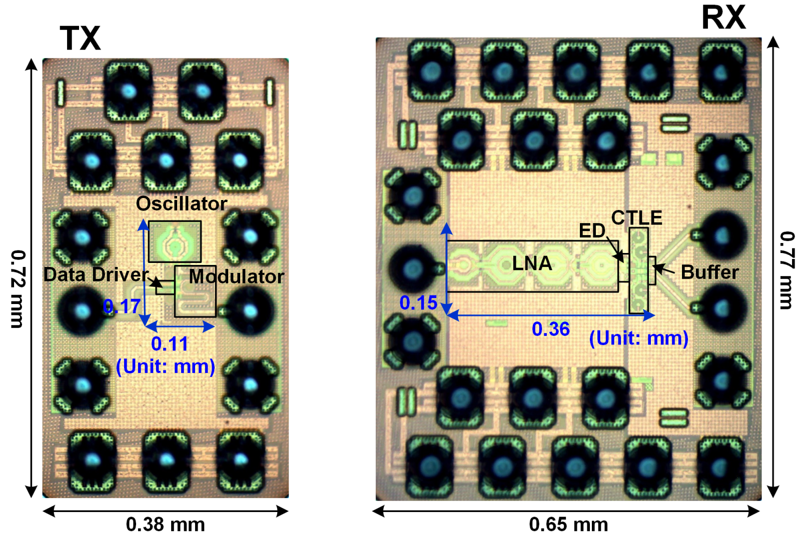


FIGURE 5.16. Die photos of the transmitter and receiver

traces with bonding wires. At last, the lumped elements components, such as capacitor, resistor, and SMP connector are assemble on the PCB for measurement.

5.5. Measurement Results and Conclusion

In a complex high-frequency system, all the components in the signal chain require performance evaluation before they are assembled together. That is the reason why all the components are designed with GSG-type interfaces to enable their capability to be tested individually. The components' measurements are conducted on the probe station to obtain their port matching and transferring performance. The results have discussed along with the components in the previous sections. For the multi-drop sub-THz system, there is one more step, which is the single-link measurement, to test the data rate capability of the transmitter and receiver, whose die photos are shown in Figure 5.16. Then, the system measurement is presented and the aggregate data rate of the multi-drop sub-THz interconnect is obtained with the interference from the other channels and environment.

A PRBS patterns of $2^{15}-1$, $2^{21}-1$ and $2^{31}-1$ are generated by a multi-channel arbitrary waveform generators (AWG) as the testing signals, and eye diagrams of the output baseband data are plotted by a broadband multi-channel oscilloscopes to evaluate the SNR. Since the OOK

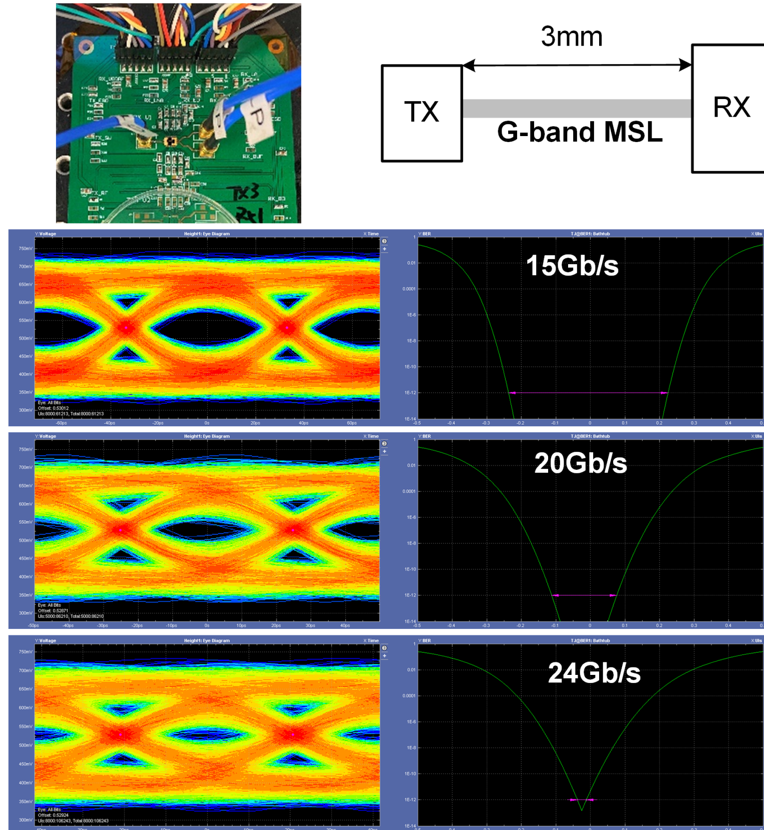


FIGURE 5.17. Single link measurement

transmitter is integrated with carrier oscillator and direct-detection receiver does not need off-chip LO and extra phase synchronization, the measurements are really straightforward and convenient, even for multiple channels simultaneously.

5.5.1. Signal Link Measurement.

The single-link test configuration is shown in Figure 5.17. In order to test the maximum data rate of theCMOS transmitter and receiver, they are connected with a 3-mm microstrip line that has less than 1-dB insertion loss and more than 60 GHz 3-dB bandwidth, then the interconnection does not constrain the speed of the link. In this testbench, the bias and DC supplies are tuned to search the optimum condition to achieve the best data rate and energy efficiency. Figure 5.17 also shows the eye diagrams and bathtub curves at 15 Gb/s, 20 Gb/s and 24 Gb/s. The maximum data rates of 24 Gb/s with the BER better than 10^{-12} is obtained.

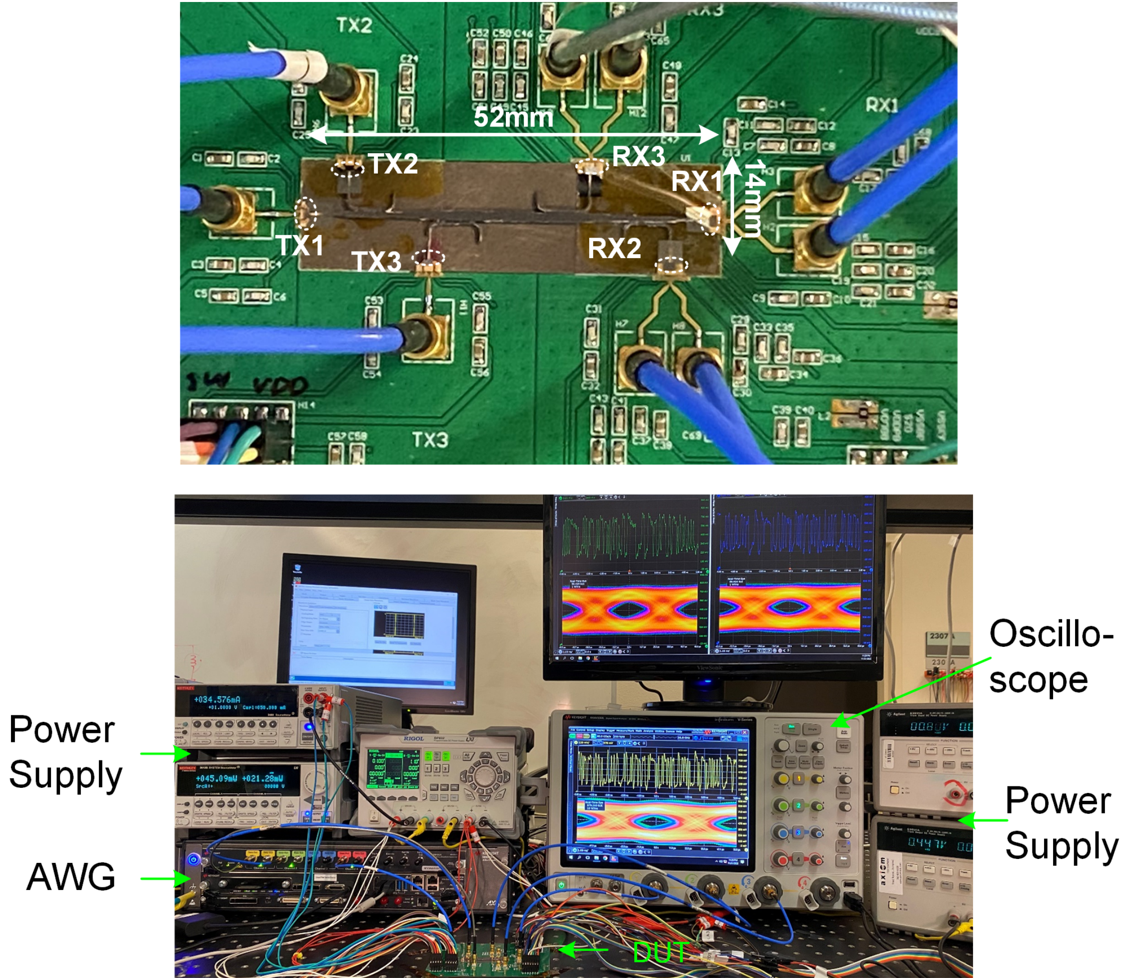


FIGURE 5.18. Photos of the multi-drop sub-THz interconnect system and measurement setup

5.5.2. Multi-drop sub-THz Interconnect Measurement.

The multi-mode multi-drop sub-THz interconnect system was assembled and tested with three modes configurations. Figure 5.18 depicts the demonstration board and testbench for multi-mode configuration. As usual PRBS patterns of $2^{21}-1$ was generated to test the three modes (E^y_{11}, E^y_{21} and E^y_{31}) of the multi-drop interconnect system simultaneously. As mentioned before, the proposed interconnect systems do not require any off-chip high-frequency signals, such as LO and synchronization signal, to assist the modulation and demodulation. The testbench are still straightforward for three-channel measurements. The AWG is able to generate four PRBSs up to 65 Gbaud/s and the wide-band oscilloscope can test four channels at the same time.

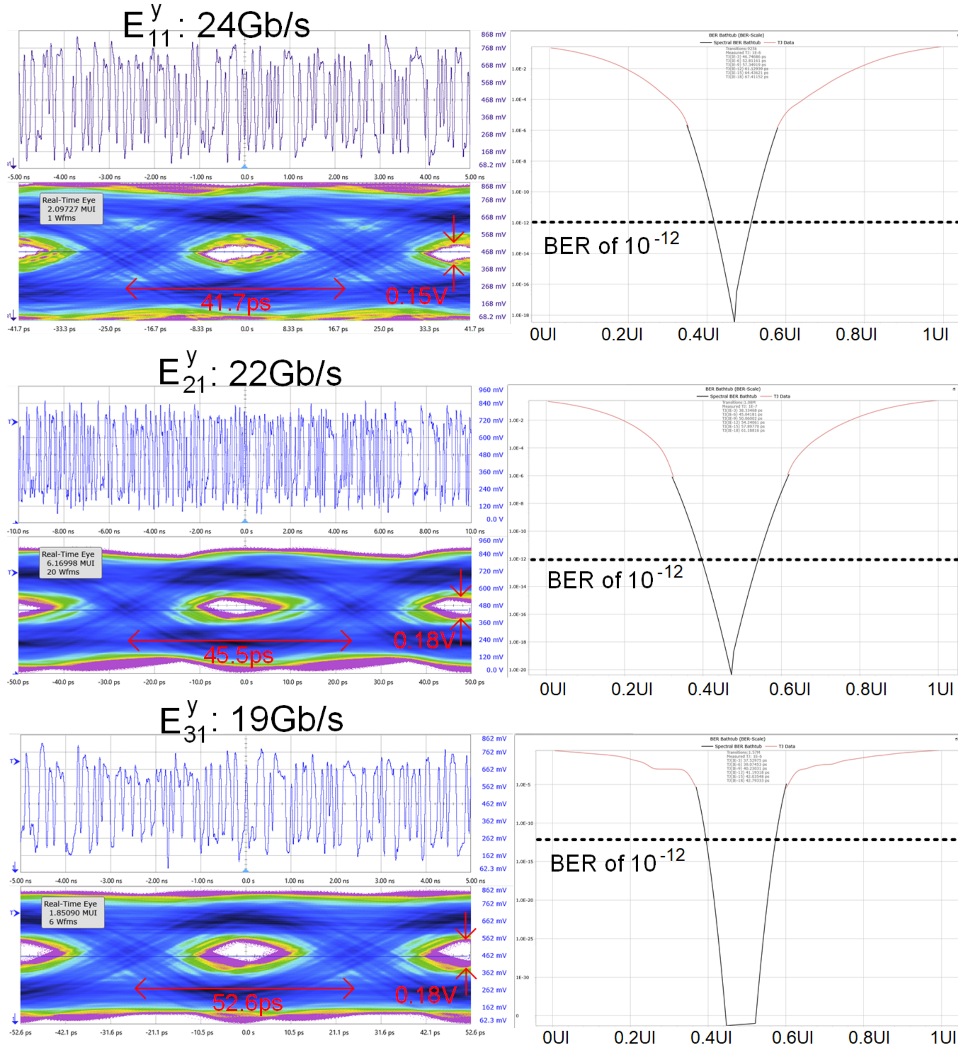


FIGURE 5.19. Measured waveforms, eye diagrams and bathtub curves at multi-mode configuration.

Benefit from the low crosstalk of the multi-drop channel, the interference from the other modes is negligible to the OOK signal that requires about 17 dB SNR. The maximum data rate can reach 24 Gb/s when the channel bandwidth is sufficient, such as E^y_{11} channel. Figure 5.19 shows the maximum measured data rates are 24 Gb/s, 22 Gb/s and 19 Gb/s for E^y_{11}, E^y_{21} and E^y_{31} modes, respectively, with a BER better than 10^{-12}. The waveforms, eye diagrams and bathtub curves at the maximum data rate are plotted in Figure 5.19 as well, which prove the success of the high-speed data transmission in the multi-drop sub-THz interconnect.

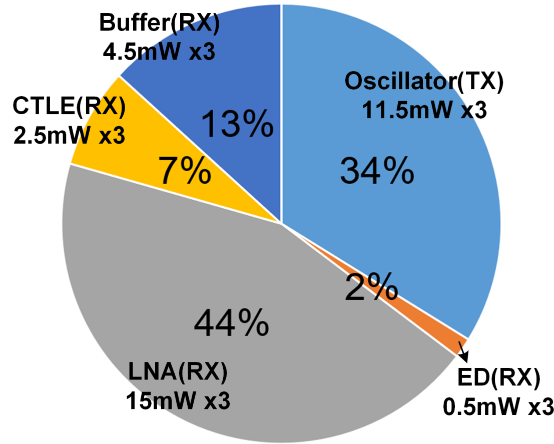


FIGURE 5.20. Power consumption breakdown.

Besides data related performance, the power consumption is another critical criteria. The total and breakdown power consumption is shown in Figure 5.20. Both transmitter and receive work at low-power consumption. The most power was burn in the oscillator in the transmitter and LNA in the receiver. The demonstrated aggregate data rate of the three channels is 65 Gb/s with the energy efficiency of 1.6 pJ/b. Table 5.1 compares with state-of-the-art dielectric waveguide based interconnect systems with our approach achieving the best energy efficiency with the capability to support multi-drop and scalability.

5.5.3. Conclusion.

This is the first time, to the authors' knowledge, to demonstrate multi-mode multi-drop DWG based interconnect. One note to make is that although the demonstration channel length is 5.2 cm, this is due to the size constraint of the wafer used to fabricate the channel. This interconnect system can be readily extended to the meter range due to the channel ultra-low loss feature. Furthermore, it can also scale to more modes to support more logic channels per physical link and can be extended to multi-dimension, two-/three- dimension, interconnect systems. Besides, with more advanced semiconductor technologies for active circuits, the data rate per channel will be further increased. Therefore, we believe that demonstrated multi-mode multi-drop sub-THz interconnect systems open a new path with high potentials to complement the existing electrical and optical interconnect to address the challenging meter range wireline communication scenarios.

TABLE 5.1. Comparison of state-of-the-art sub-THz/THz interconnect.

	JSSC'19 [20]	**ISSCC'21 [23]**	**ISSCC'22 [43]**	**This work**
Technology	28nm CMOS	130nm BiCMOS	28nm CMOS	65nm CMOS
Waveguide	PTFE+ePTFE	Rogers R3006	PTFE	High-resistivity Si
DWG size (WxH, mm^2)	1.9x1.0	0.4x0.25	3.5x0.8	1.2x0.525
Carrier freq. (GHz)	140	220, 260, 300	70	165
Channelization	-	FDM	Bi-directional	MDM
NO. of CHNLs	1	3	2	3
Simultaneous CHNLs	1	2	1	3
Off-chip LO required	No	Yes	Yes	No
Off-chip LO phase sync.	No	Yes	No	No
Aggregate data rate (Gb/s)	7	30 x 2	25	24+22+19
BER	1e-12	1e-12	1e-12	1e-12
Modulation	FSK	ASK	BPSK	ASK(OOK)
Power (mW)	230	256(TX), 73x3(RX)*	95(TX), 117(RX)*	34.5(TX), 67.5(RX)
Energy effi. (pJ/b)	32.9	5.3	8.5	1.6
Multi-drop capability	No	No	No	Yes
Scalability	No	No	No	Yes
Chip area (mm^2)	1.5(TX), 0.81(RX)	9.36(TX), 0.81(RX)	6.72(TRX)	0.27(TX), 0.5(RX)

* not including the off-chip LO power.

CHAPTER 6

Conclusions

6.1. Summary

The sub-THz/THz frequency band draws more and more attention because of the primarily large available bandwidth and small wavelength, have motivated extensive research in this field. Those advantages make the THz band ideal for numerous applications, where the most common applications are high-speed communications, imaging and sensing, and spectroscopy.

In sub-THz/THz interconnect field, belonging to high-speed wireline communication, the most important metrics is data rate, energy efficiency and bandwidth density. Transitional electrical and optical approaches for short- and long-distance scenarios have significant constrains in the meter range scenario. That is, the lossy and bandwidth limited channels are the bottlenecks of electrical interconnect; For optical interconnect, the features, such as the required complex fabrication and the high environment sensitivity, increase the power and cost budgets significantly, making it uneconomical for short-distance communications. Low loss dielectric channel-based interconnects have been investigated and demonstrated and researchers are designing very complex transmitter and receiver architecture in CMOS technologies to boost the date rate but paying more power and cost. This dissertation focus on the advanced spatial multiplexing schemes, improve the total data rate performance by creating more logical channels. Due to the high performance channel, non-coherent detection are adopted, which save much power, chip area and extra afford for measurement, such as clock recovery and synchronization. The sub-THz interconnects proposed in this dissertation achieve one of the best data rate and energy efficiency performance, meanwhile, is able scale to more modes to support more logic channels per physical link and can be extended to multi-dimension, two-/three- dimension, which is not supported by other solutions.

Chapter 2 portrays the passive and active most commonly used in the sub-THz/THz CMOS design. Section 2.1 presents on-chip and off-chip passives in a frequency range from baseband to sub-THz. Section 2.2 introduces actives in CMOS including transistor modeling, layout optimization and neutralization. Section 2.3 of this chapter presents the coherent and non-coherent detection in commercial communication systems. The elements in both directions are proposed and several design techniques are introduced to optimize sub-THz/THz blocks in standard CMOS technologies. Section 2.4 introduces multiplexing schemes, besides the traditional FDM, TDM and quadrature division multiplexing, more advanced spatial multiplexers are designed.

Chapter 3 percents a full-duplex sub-THz interconnect system based on FDM scheme. The system consists of a dual-band transmitter, receiver, and DWG channel that provides low in-band insertion loss and high isolation in the two adjacent frequency bands. Full-duplex measurement was set up with pseudorandom binary sequence (PRBS) length of 2^{31}-1. With the bit error rate (BER) $< 1 \times 10^{-12}$, channel 1 (CH.1) at 140 GHz and channel 2 (CH.2) at 180 GHz achieve on-off keying (OOK) modulated data rate of 12.3 Gb/s and 10.3 Gb/s, respectively. This full duplex interconnect system achieves the energy efficiency of 1.58 pJ/b and the record bandwidth density of 150.7 Gb/s/mm^2.

Chapter 4 proposes a mode-coupler based multi-drop Si DWG with MSL-to-DWG transitions on quartz boards, and theoretical analyzes and explains the design DWG mode coupler. Many analysis methods and solutions, such as bandwidth analysis and taper analysis with light ray tracing method, are firstly proposed. Section 4.1 drives the eigen modes in rectangular dielectric waveguides; Section 4.2 analyzes the waveguide mode directional coupler design, including mode coupling condition, coupling coefficient extraction, coupling efficiency maximization and verification. Section 4.3 introduce all the detailed building structures and the mechanism behind them. Section 4.4 shows the fabrication and measurement results.

Chapter 5 introduces a multi-drop sub-THz interconnect system based on the multi-drop Si DWG channel designed in the Chapter 4. the system aims to achieve more than 60 Gb/s data rate (20 Gb/s per channel). Therefore, the system architecture is investigated again and modified to improve the bandwidth and sensitivity of the receiver. Section 5.2 and 5.3 improve the transmitter and receiver by adopting broadband modulator, LNA and CTLE. Section 5.4 presents the package

design and fabrication and replace all bonding wires with flip-chip bumps in RF signal chain. In section 5.5, the multi-drop data rates are 24 Gb/s, 22 Gb/s and 19 Gb/s for E^y_{11}, E^y_{21} and E^y_{21} modes, respectively with the BER better than 10-12. The demonstrated aggregate data rate of the three channels is 65 Gb/s with the energy efficiency of 1.6 pJ/b.

6.2. Future Directions

The demonstrations of DWG sub-THz/THz interconnects reveal high potential data rate, energy efficiency and bandwidth density in the interconnect field. The SOA data rate has exceeded 50 Gb/s and energy efficiency is lower than 2 pJ/b. It is believed that the data rate of sub-THz/THz interconnect system will quickly approach 100∼200 Gb/s and maintain an energy efficiency below 5 pJ/b in a few years. The best solution for interconnects will be the co-design of passive channel and active transceiver according to the comprehensive analysis, then combine the optimum techniques into a system. In such a broad area, there is plenty of room for further research and systems development. The suggestions are proposed for Si DWG channel, multiplexer and active transceiver.

(1) Si DWG channel

An essential weakness of the proposed Si DWG based sub-THz/THz interconnects is the length of channel. The high-resistivity Si has very low low and dispersion, and is suitable for meter-range scenario. The Si channels are etched from 4-inch Si wafers with DRIE, thus they are too short to realized in the practical applications. As the improvement of fabrication and packaging approaches, a hybrid Si/SiO_2 DWG channel is possible to fabricate by cascading multiple Si/SiO_2 waveguides with precise bonders.

(2) Multiplexer

The FDM and MDM multiplexers introduced in this dissertation indicate a clear directions for sub-THz/THz interconnects. By employing advanced spatial multiplexing schemes, multiple channels is built in a physical link, which not only multiplies the aggregate data rate by times, but also extends the links to multi-dimension, interconnect systems. The advance multiplexer can significantly relief the burden on active transceivers. Among the multiplexing schemes, MDM has the

highest potential to be scaled to more channels and multi-dimension, because it is straightforward to bring in more modes by employing more mode couplers or swapping the polarization direction.

(3) Active transceiver

Moore's Law predicts the development of semiconductor technologies. The increasing f_T and f_{max} of the transistors enable higher operating frequency and lower power consumption, which is benefit to both bandwidth and energy efficiency of active devices.

Another strategy lying active transceiver is the high-order modulation, such as QPSK or QAM. High-order modulation improves the spectral efficiency and frequency spectrum at sub-THz/THz will be bounteous for those signals. On the other hand, high-order modulation certainly increase the complexity of the circuits and quality of the signal at the cost of power consumption. The individual transceiver has achieved more than 200 Gb/s data rate. To implement the transceiver in sub-THz/THz interconnects and boost the system speed, a high-efficient modulator is the crucial component, which must meet the high requirement of phase and amplitude accuracy with a low power consumption.

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