UC Santa Barbara
UC Santa Barbara Electronic Theses and Dissertations

Title
Development of III-Nitride Tunnel Junctions and p-n Diodes by Ammonia-Assisted Molecular Beam Epitaxy

Permalink
https://escholarship.org/uc/item/9px1s8b0

Author
Wang, Jianfeng

Publication Date
2020

Peer reviewed|Thesis/dissertation

eScholarship.org Powered by the California Digital Library
University of California

UNIVERSITY OF CALIFORNIA

Santa Barbara

Development of III-Nitride Tunnel Junctions and p-n Diodes by Ammonia-Assisted Molecular Beam Epitaxy

A dissertation submitted in partial satisfaction of the

requirements for the degree Doctor of Philosophy

in Materials

by

Jianfeng Wang

Committee in charge:

Professor James Speck, Chair

Professor Claude Weisbuch

Professor Steven DenBaars

Professor Umesh Mishra

September 2020

The dissertation of Jianfeng Wang is approved.

Claude Weisbuch

Steven DenBaars

Umesh Mishra

James Speck, Committee Chair

September 2020

[This page is optional]

Development of III-Nitride Tunnel Junctions and p-n Diodes by Ammonia-Assisted Molecular Beam Epitaxy

Copyright © 2020

by

Jianfeng Wang

ACKNOWLEDGEMENTS

There are many people I'd like to thank for helping me throughout this journey. I'd like to thank my parents for their dedication in my education which bring me to graduate school. In Penn State, my undergraduate advisor Professor Clive Randall offered me the first key to the door of research. My co-advisor Dr. Ramakrishna Rajagopalan showed me research can be fun and enjoyable. He also helped me with every detail about graduate school applications.

The life at UCSB has been a great journey. I would like to thank my advisor Professor James Speck for giving me the great opportunity, for sharing his passion for science, and for all the guidance along the way. I would like to thank my committee members, Professor Claude Weisbuch, Professor Steve Denbaars, and Professor Umesh Mishra for the great classes they teach, their kind suggestions and helping me with the academic checkpoints.

I was lucky to have many great mentors in graduate school. Dr. Erin Young showed me how to use MBE and gave us the opportunity to take care of the 930 she treasured so much after she left. Dr. Elaheh Ahamed gave us great research suggestions, cared for our experience, and helped me a lot with job search. Dr. Asad Mughal showed me how to use cleanroom and gave me a lot of career advises. Dr. Burhan SaifAddin helped me with research. We also had many inspiring conversations. I want to thank all my mentors for showing me how to do research and answering all my questions.

None of my research would be possible without the MBE lab managers, Kurt Olsson and John English. Kurt work tirelessly and takes good care of all the MBE system - a seemingly impossible job. Part of my joy for working in the MBE lab come from working with John, watching him came up with genius ideas for every problem, and reading his fun notes on toolboxes. I would also like to thank the Nanofab staff and the CNSI lab managers. Including

Dr. Youli Li, Aiden Hopkins, Brian Lingg. Special thanks to Dr. Tom Mates for the many SIMS hours. I also want to thank the SSLEEC and Materials department staff for their help and support.

I would like to thank my wonderful teammates that collaborated with me and helped me with my research. First, I would like to thank my fellow nitride MBE lab mates, Dr. Kelsey Jorgensen, Kai Shek Qwah, Dr. Christian Robertson, Dr. Richard Cramer, Dr. Erin Young, Dr. Micha Fireman, Christian Wurm, Zachary Biegler, and Dr. Morteza Monavarian. We went through the exhausting openings together, survived the difficult times by encouraging each other, and shares great time outside of work. Many of them are also dear friends to me. I want to thank the diode team for achieving such great result in a very short time frame thanks to everyone's kind collaboration. The team members include Dr. Esmat Farzana, Dr. Kelsey Jorgensen, Kai Shek Qwah, Zachary Biegler, Dr. Morteza Mornavarian, Dr. Yuewer Zhang, and Dr. Christian Robertson. I also want to thank the UV team. Thanks to Dr. Burhan SaifAddin for his mentorship, Chris Zollner for the AlN on SiC templates I used for Chapter 3's work, Dr. Abdullah Almogbel for the discussions on n-AlGaN, Michael Iza for leading the meetings, Yifan Yao for help with processing, Micheal Wang and Vincent Rienzi for the fruitful discussions. I am thankful for the Speck group members. Thanks to Wan Ying Ho for teaching me how to process LEDs, Yi Chao Chow for his suggestions and help with processing, Dr. Bastien Bonef for the APT measurements, Dr. Yuewei Zhang for his great suggestions, Akhil Mauze for the great chats, Cheyenne Lynsky for the suggestions about p-GaN studies, Dr. Daniel Myers and Dr. Andrew Espenlaub for helping me as senior group members. I would like to thank my office mate Cheyenne Lynsky and Dr. Matthew Wong for the great discussions about science and life. I am also thankful for all the SSLEEC and MBE lab

colleagues. It is my great privilege to work in an inspiring research environment built by their shared effort. I am also thankful for the women community in SSLEEC, Materials, ECE, and STEM in general.

Outside of the UCSB campus I would like to thank my friends, both those in Santa Barbara and those live elsewhere, for helping me to stay happy and showing me there's infinite possibility in life beyond success in work. I would like to thank my cat Sadie for allowing me to pet her and brush her so that I can stay sane. Fortunately, she has more hair than average PhD student. Last but not the least, I want to thank my families, especially my grandmother for caring for me and supporting me to get to where I am today.

I'm really fortunate to have all the people helping me to get here. I'm grateful for everyone and every moment, mentioned here or not, on this journey.

VITA OF JIANFENG WANG

September 2020

Engineering Science Building Rm 3215C, University of California, Santa Barbara, CA, USA, 93106
Email: lisa.wjf@gmail.com
Tel: +1-(814)-206-6862
Linkedin: www.linkedin.com/in/jianfeng-wang-ucsb

SUMMARY OF SKILLS

- Conducted research for > 6 years, focusing on epitaxial growth, characterization, processing, and testing of III-Nitride semiconductor, (UV) LEDs, p-n diodes, tunnel junctions, optical/power devices and supercapacitors
- Operated, maintained, and trained junior students on sophisticated instruments such as NH_3-assisted Molecular Beam Epitaxy (MBE) system and temp-controlled Hall setup
- Wrote 2 first-author journal articles, a patent, presented at 2 international conferences and 3 reviews
- Experienced team player by collaborating in > 5 research groups and communicating across cultures

EDUCATION

1. University of California Santa Barbara (UCSB) — Aug 2015 – Sep 2020 (Expected)
   Ph.D. in Materials, Electronic/Photonic Materials course track, GPA 3.78
   Thesis Advisor: James Speck (email: speck@ucsb.edu)
   Committee: James Speck, Umesh Mishra, Steven Denbaars, Claude Weisbuch
2. Pennsylvania State University, University Park (Penn State) — Aug 2013 – May 2015
   B. S. in Materials Science and Engineering, Minor in Economics, graduated with distinction
   Thesis Advisor: Clive Randall (email: car4@psu.edu) Ramakrishnan Rajagopalan (email: rur12@psu.edu)
3. Harbin Institute of Technology (HIT) — Aug 2011 – Jun 2013
   B. E. in Welding, Honor School

RESEARCH SKILLS

- **Instruments:** NH_3**-MBE** (UHV epitaxy system, including cryo panels, pumps, gauges, pressure control, mass flow controller, respirator), plasma-assisted MBE (PA-MBE), cleanroom, glovebox, MOCVD
- **Materials Fabrication:** e-beam evaporation, photolithography, reactive-ion etching, dicing saw, atomic layer deposition, plasma-enhanced CVD, inductive coupled plasma etching, chemical-mechanical polishing, flip-chip bonding, contact aligner, wire bonder, polisher
- **Characterization:** X-ray diffraction, reflection high-energy electron diffraction (RHEED), atomic force microscopy, secondary-ion mass spectrometry, (temp-controlled) Hall, capacitance-voltage measurements, scanning electron microscopy, photoluminescence, electroluminescence, 4-pt probe, LIV characterization, integrating sphere, oscilloscope, optical microscopy, electrochemical impedance analyzer, potentiostat, galvanostat
- **Data Processing & Analysis:** MATLAB, Origin, Microsoft Excel, Mathematica
- **Modeling:** SiLENSe, ddcc (1D, 2D), BandEng, Material Studio
- **Other Software:** L-edit, Klayout, LabVIEW, Crystal Maker, Autodesk 3D, C/C++
- **Languages:** English (Full Professional Proficiency), Mandarin (Native)

RESEARCH PROJECTS

1. **Low leakage and high reverse breakdown GaN p-n diodes for power electronic applications** (ARPA-E PNDIODES program) — Aug 2019 – Present
   - Established growth condition for top-quality III-nitride material with low impurity level ($3\times10^{15}/cm^3$)
   - Characterized morphology and impurity level of the drift region material
   - Measured diode IV behavior using high voltage setup (up to 2000 V)

- Developed low-leakage ($I_{on}/I_{off}>10^{10}$) high breakdown voltage (> 1000 V) GaN on GaN vertical p-n diodes with low ideality factor (n=1.3) and low ON resistance (R_{ON_sp}= 0.28 mΩ·cm^2)

2. **Low voltage penalty hybrid tunnel junctions for visible applications**
   (Solid State Lighting & Energy Electronics Center at UCSB) Aug 2016 – Present
   - Grew GaN and InGaN-based hybrid and all MBE tunnel junctions on MOCVD grown LEDs
   - Fabricated record-low voltage penalty (0.23 V) blue tunnel junction LEDs
   - Analyzed high-volume industrial testing results using statistical methods
   - Wrote patent for improved light extraction structure for tunnel junction LEDs
3. **High conductivity Si-doped AlGaN for UV emitters** Oct 2017 – July 2019
   (Solid State Lighting & Energy Electronics Center at UCSB)
   - Grew high doping level (4×10^{19}/cm^3) low resistivity (3 mΩ·cm) n-$Al_{0.6}Ga_{0.4}N$ on AlN/SiC templates
   - Characterized the dislocation density, alloy composition, relaxation ratio, dopant level, and electrical properties of the AlGaN thin film
   - Fabricated thin film flip chip UVC tunnel junction LEDs with doubled light extraction efficiency
   - Measured the electrical and optical performance of the UV emitter
   - Simulated the band structure to improve epi design
4. **Mg-doped GaN with controllable doping by valved Mg cell** Aug 2015 – Aug 2017
   - Maintained valved Mg cell on MBE and temperature-controlled Hall setup
   - Grew Mg doped GaN with low resistivity, high quality, and highly controllable doping up to 3×10^{20}/cm^3
5. **Lithium-ion supercapacitors with pre-lithiated graphite anode** Apr 2014- May 2015
   (Project founded by NSF ERC Advanced Self-Powered Systems of Integrated Sensors and Technologies (ASSIST))
   - Developed Li-ion capacitors with high energy density and cyclability, large voltage range, as well as ultra-low self-discharge
   - Characterized coin cell performance such as cyclic voltammetry, constant charge discharge by electrochemical measurements
   - Assembled capacitor and electrical double layer capacitor (EDLC) coin cells in glove box
   - Fabricated pre-lithiated graphite anode with controlled degree of lithiation
   - Synthesized electrode using powder materials
   - Fabricated PVDF membranes by phase inversion process to be used as separators for Li-ion capacitors

EXPERIENCE

1. **Graduate Student Researcher, MBE growth of III-Nitride materials and devices**
   Aug 2015 – Present
   Advised by Dr. James S. Speck, the Solid State Lighting & Energy Electronics Center (SSLEEC), UCSB
   - Led a group of 3 to maintain, trouble-shoot, and modify cryogenic and ultra-high vacuum MBE systems
   - Became a subject matter expert in growing top-quality III-nitride materials and devices using NH_3-MBE
   - Managed the training on multiple sophisticated instruments and coordinated system upgrade, part ordering, and maintenance with lab managers and vendors
   - Coordinated collaborations with other groups and industry collaborators using multiple languages
2. **Graduate Student Teaching Assistant** Apr 2017 – Jun 2017
   Materials department, UCSB, with Prof. Van der Ven
   - Managed a class of 30+ graduate students, coordinate time and locations for TA sessions
   - Explained complex scientific concepts in basic terms and answer questions during the sessions
3. **Undergraduate Student Researcher** Apr 2014 – May 2015

Advised by Dr. Clive A. Randall and Dr. Ramakrishnan Rajagopalan, Penn State

3. **Summer Student Researcher Intern** Jun 2014 – Aug 2014
   Materials Research Institute, Penn State

REFEREED PUBLICATIONS

Journal Articles

1. **Wang, J.,** Young, E. C., Ho, W., Bonef, B., Fireman, M., Margalith, T., & Speck, J. S. "III-Nitride Blue Light-emitting Diodes Utilizing Hybrid Tunnel Junction with Low Excess Voltage. Manuscript submitted (Aug 2020)
2. **Wang, J.,** SaifAddin, B. K., Zollner, C. J., Bonef, B., Alomogbel, A. S., Yao, Y., Iza, M., Zhang, Y., Fireman, M. N., Young, E. C., Nakamura, S., & Speck, J. S. "Optimization of n-type conductivity of Si-doped $Al_{0.6}Ga_{0.4}N$ by ammonia-assisted molecular beam epitaxy for UV emitters," Manuscript in preparation (Sep 2020)
3. Farzana, E., **Wang, J.,** Monavarian, M., Itoh, T., Qwah, K. S., Biegler, Z. J., Jorgensen, K. F., & Speck, J. S. "Over 1 kV vertical GaN-on-GaN p-n diodes with low on resistance using molecular beam epitaxy," Manuscript in preparation (Sep 2020)
4. Qwah, K. S., Monavarian, M., Lheureux, G., **Wang, J.,** Wu, Y.-R., & Speck, J. S. "Theoretical and experimental investigations of vertical hole transport through unipolar AlGaN structures: Impacts of random alloy disorder," *Appl. Phys. Lett.* 117, 022107 (2020)

Conference Presentations

1. **Wang, J.,** Young, E. C., SaifAddin, B., Zollner, C., Almogbel, A., Fireman, M. N., Iza, M., Nakamura, S., Denbaars, S. P., & Speck, J. S. "Hybrid III-Nitride Tunnel Junctions for Low Excess Voltage Blue LEDs and UVC LEDs," 2019 Compound Semiconductor Week (CSW), Nara, Japan, 2019, pp. 1-1, doi: 10.1109/ICIPRM.2019.8819252.
2. **Wang, J.,** Young, E. C., SaifAddin, B., Zollner, C., Almogbel, A., Fireman, M. N., Iza, M., Nakamura, S., Denbaars, S. P., & Speck, J. S. "Hybrid MOCVD/MBE Tunnel Junctions for III-Nitride UVC LEDs and Low Voltage Penalty Blue LEDs," 13th International Conference on Nitride Semiconductors 2019 (ICNS-13), Bellevue, Washington, 2019.
3. **Wang, J.,** Ma, D., Rajagopalan, R., Randall, C., "Fabrication of Low Leakage Electrochemical Capacitors", ASSIST Webinar, Apr. 2015
4. **Wang, J.,** Ma, D., Rajagopalan, R., Randall, C., "Lithium-ion Capacitors using Pre-lithiated Graphite Anode", Z3.18, MRS 2014 Fall Meeting, Dec. 2014, Boston. (Poster).
5. Ma, D., **Wang, J.,** Wang, Y., Rajagopalan, R., Randall, C., "Lithium-ion Capacitors using Pre-lithiated Graphite Anode", Materials Day 2014 Meeting, Oct. 2014, State College. (Poster).
6. Berbano, S., Ma, D., **Wang, J.,** Wang, Y., Lanagan, M., Rajagopalan, R., Randall, C., "Supercapacitor Materials & Devices for a Self-Powered and Adaptive Sensing Platform", NSF ASSIST Site Visit Raleigh, NC, May 19, 2015. (Poster).

LEADERSHIP/EXTRACURRICULAR

1. Volunteer of Nittany Greyhounds (organization for re-homing ex-racing dogs) Nov 2014 – May 2015
2. Member of CSSA (Chinese Students and Scholars Association) Academic Department
   Dec 2013 – May 2015
3. Head of Business Department of Enactus (Entrepreneurship Action US), HIT Chapter
   May 2012 – Mar 2013
   - Lead the department to cooperate with Walmart, providing female students with vocational training
   - Participated in improving the operation mode of Sunshine Baby Autistic Children Training Center
4. Volunteer of Aiesec (international student organization for leadership development)
   Jun 2012 – Aug 2012
   - Cooperated with volunteers from Britain, Swiss, and Italy

Provided elementary school students from underdeveloped areas in China with classes about English and foreign culture

ABSTRACT

Development of III-Nitride Tunnel Junctions and p-n Diodes by Ammonia-Assisted Molecular Beam Epitaxy

by

Jianfeng Wang

Tunnel junctions (TJs) offer alternative designs and promise in some cases improved performances for nitride-based light-emitting diode (LEDs) and laser diodes (LDs). To achieve the high p-type doping in the TJ, Mg-doped GaN with controllable doping was desired. For visible wavelength range applications, two TJ techniques, hybrid TJ and all MBE TJ, were investigated. The study targeted a low voltage penalty compared to the conventional ITO contact. For ultraviolet (UV) applications, a hybrid UV TJ was enabled by the development of low resistivity n-AlGaN. In recent years, GaN-based power electronics have attracted great interests due to the attractive physical properties of the III-N material system. Vertical GaN p-n diodes with low leakage and high breakdown field was demonstrated.

With a valved Mg source and indium as surfactant, high quality p-GaN with controllable and reproducible doping levels are grown by NH_3 MBE. The high doping levels achievable enables TJ applications. Details of doing Hall measurements on p-GaN were also discussed.

The voltage penalty of the TJ LEDs and LDs, in comparison with standard contact technologies, has been a major concern especially for commercial applications. In this study, methods to achieve low excess voltage were investigated. Using NH_3 MBE, hybrid GaN TJs were grown on commercial metalorganic chemical vapor deposition (MOCVD) grown blue LED wafers. Atom probe tomography (APT) and secondary ion mass spectrometry (SIMS) indicate 1 min buffered HF (BHF) clean of the regrowth interface reduced Mg and impurity

incorporation into the n++ regrown TJ layers. The wafers were processed and measured in parallel to reference wafers using both university and industry cleanroom and measurement setups. At 20 $A \cdot cm^{-2}$, TJ LEDs grown with Si δ-doping at the junction interface processed in the university cleanroom had a forward voltage of 3.10 V in comparison to 2.87 V for LEDs processed with a standard ITO contact. Unencapsulated TJ LEDs processed by industrial process without indium tin oxide (ITO) or current blocking layer (CBL) had about 0.3 V excess voltage compared to reference LEDs. The TJ LEDs also had more uniform light emission profile. The low excess voltage and consistent results acquired in both settings suggest that tunnel junction can be scaled for industrial processes. Similar studies were done to for all MBE TJs. Systematic studies examined the effect of InGaN interlayers.

Highly doped n-$Al_{0.6}Ga_{0.4}N$ can be used to form tunnel junctions (TJs) on deep ultraviolet (UVC) LEDs and potentially double the light extraction efficiency (LEE) compared to the use of p-GaN/p-AlGaN. High quality $Al_{0.6}Ga_{0.4}N$ was grown by NH_3-assisted molecular beam epitaxy (NH_3 MBE) on top of AlN on SiC substrate. The film is crack free under scanning electron microscope (SEM) for the thickness investigated (up to 1 µm). X-ray diffraction reciprocal space map scan was used to determine the Al composition and the result is in close agreement with APT measurement result. By varying the growth parameters including growth rate, and Si cell temperature, n-$Al_{0.6}Ga_{0.4}N$ with a doping level of 4×10^{19} $/cm^3$ and a resistivity of 3 $m\Omega \cdot cm$ was achieved. SIMS measurement shows that a high Si doping level up to 2×10^{20} $/cm^3$. Using a vanadium-based annealed contact, ohmic contact with a specific resistance of 10^{-6} $\Omega \cdot cm^2$ as determined by circular transmission line measurement (CTLM) was achieved. Finally, the n-AlGaN regrowth was done on MOCVD grown UVC LEDs to form UVC TJ

LED. The sample was processed into thin film flip chip (TFFC) configuration. The emission wavelength is around 278 nm and the excess voltage of processed UV LED is around 4.1 V.

In the last part of the study, growth development of low leakage, high reverse breakdown field GaN p-n diodes was shown. Efforts were made to optimize morphology and achieve low impurity un-intentionally doped (UID) GaN in the drift region. Secondary ion mass spectrometry (SIMS) and capacitance-voltage (CV) measurements showed oxygen and carbon concentrations in the low 10^{16} cm^{-3} and N_D-N_A level of 3×10^{15} cm^{-3}. This was combined with the use of high-quality p-GaN to make GaN p-n diodes with on/off ratio>10^{10}, ideality factor of 1.33, and a minimum specific on resistance of 0.29 m$\Omega\cdot$cm^2.

TABLE OF CONTENTS

Chapter 1 p-type doping of GaN by valved Mg cell for tunnel junction applications...... 1

1.1 Introduction 1

1.1.1 III-Nitride MBE 1

1.1.2 Valved Mg Cell 2

1.1.3 Mg-doping of III-Nitride Materials 6

1.1.4 Hall calibration sample epi structures 7

1.1.5 Temperature Controlled Hall Measurement 10

1.2 Impurity reduction in p-GaN 11

1.3 Range of Mg doping level achieved 15

1.4 H_2 diffusion in MBE p-GaN grown with high NH_3 flux 16

References 19

Chapter 2 Hybrid Tunnel Junctions for Visible Applications 22

2.1 III-nitride blue light-emitting diodes utilizing hybrid tunnel junction with low excess voltage 22

2.1.1 Introduction 22

2.1.2 Experimental 25

2.1.3 Results 29

2.1.4 Discussion 40

2.4.5 Conclusion 43

2.2. Hybrid growth technique of tunnel junction on c-plane and m-plane 44

2.2.3 p-GaN activation 44

2.2.4 Sample cleaning 45

2.2.5 NH_3 annealing before growth 45

2.2.6 n-TJ regrowth by MBE 45

References 48

Chapter 3 Highly doped n-AlGaN with low resistivity for UV TJ LEDs 56

3.1 Introduction 56

3.2 Experimental 58

3.3 Results 61

3.3.1 Epitaxial growth of AlGaN 61

3.3.2 Doping optimization for Si-doped AlGaN 67

4.3.3 UVC TJ LEDs 71

3.4 Conclusion ... 73
3.5 Future work ... 74
References ... 77
Chapter 4 Growth development for low leakage high reverse breakdown GaN p-n diodes ... 86
4.1 Introduction ... 86
4.2 Unintentionally doped GaN with low impurity concentration for n^- drift region ... 90
4.2.1 C/H/O levels vs growth rate by SIMS ... 90
4.2.2 N_{net} vs growth rate by CV measurements ... 91
4.2.3 Morphology vs growth temperature by AFM ... 93
4.3 GaN p-n diode batch 1 ... 94
4.4 GaN p-n diode batch 2 ... 101
4.5 SIMS and CV analysis of batch 1 and 2 diodes ... 106
4.2 Conclusion ... 107
References ... 109
Chapter 5 Summary and future work ... 110
5.1 All MBE tunnel junctions for visible applications (on-going work) ... 110
5.1.1 Introduction ... 110
5.1.2 Growth of InGaN by NH_3 MBE as interlayers ... 111
5.1.3 Experimental details for developing all MBE tunnel junction blue LEDs ... 112
5.1.4 Initial Results ... 116
5.2 Summary and future work ... 117
References ... 119
Appendices ... 120
Appendix A. Examples of ammonia MBE growth recipes ... 120
A.1 SIMS stack for Si doping ... 120
A.2 All MBE tunnel junctions with InGaN interlayer ... 120
A.3 Continuous vertical diode ... 122
Appendix B. Calibrations for NH_3 MBE growths ... 123
B.1 Emissivity calibrations ... 123
B.2 Growth rate and composition calibrations for AlGaN ... 124
Appendix C. Hall measurements ... 127
C.1 Room temperature Hall measurements ... 127
C.2 Temperature-controlled Hall measurements ... 127

Appendix D. SIMS measurements 129
Appendix E. Process travelers 130
E.1 Pd/Au vs TJ LED 130
E.2 ITO vs TJ LED 132
E.3 Miscellaneous for LED processing 134
E.4 Diode_v1 137
E.5 Diode_v2 139
E.6 CV for UID on STN 142
References 144

LIST OF FIGURES

Figure 1.1 A typical design of an effusion cell. The charge is exposed to the growth environment. 3
Figure 1.2 Valved Mg cell used for this work. (a) Picture of a valved corrosive source model vcor 110 manufactured by Riber. (b) The valve opening is controlled by the vertical movement of parts (blue area in image). 4
Figure 1.3 The doping level as a function of the week the Mg-doped samples are grown. The red and brown dots correspond to 10% and 15% valve opening respectively. The doping levels from 5 weeks' time fluctuates within $1\times 10^{18}/cm^3$ range, showing great reproducibility. Figure courtesy Prof. Nicholas Grandjean. 4
Figure 1.4 The Mg flux is controlled by both the cell temperature and valve opening. (a) The doping level increase exponentially as a function of cell temperature by CV measurements. The deviation on the start of trend is due to strong compensation effect. (b) Relative flux as a function of valve opening. The flux is highly controllable. Figure courtesy Prof. Nicholas Grandjean. 5
Figure 1.5 Schematic of epi structures for (a) quick p-GaN Hall calibrations and (b) accurate p-GaN Hall calibrations. 8
Figure 1.6 AFM images of GaN:C layer showing pits on the surface. The RMS roughness was 0.75 nm. 8
Figure 1.7 SIMS measurements for GaN:C SIMS stack. The CBr_4 flow used was 30, 20, 10 sccm for the GaN:C layers from left to right. 9
Figure 1.8 Typical AFM image of p-GaN grown with indium surfactant. 12
Figure 1.9 Schematic of the epi structure for p-GaN Hall sample with and without 10 periods of low temperature/high temperature impurity reduction super lattice. 12
Figure 1.10 Secondary-ion mass spectrometry (SIMS) measurements of p-GaN sample grown with and without superlattice. 14
Figure 1.11 SIMS of Mg, H, C, H, and O level in Mg SIMS stack sample. 16
Figure 1.12 SIMS measurement for Mg-doped GaN grown at 1000 sccm before and after annealing. 16
Figure 1.13 The hydrogen diffusion in Mg-doped GaN follows Fick's law. (a) Initial concentration profile (b) concentration profile during the diffusion process as calculated by Mathematica. 17
Figure 2.1 Schematic of the tunnel junction (TJ) LED epitaxial structure. The commercial MOCVD blue LED wafer has p-InGaN (type I wafer) or p-GaN (type II wafer) cap on top as part of the p-side tunnel junction. The MBE regrowth was carried out on the commercial wafer to form the tunnel junction n-side and n-GaN current spreading layers. A Si δ-doped layer was grown on one of the samples (sample 1). 28
Figure 2.2 (a). Image of a LED processed by an industrial LED process. The chip size is 584 μm ×1143 μm. (b-d) Schematic of processed LED structure. (b). The reference sample R2 is processed with current blocking layer (CBL) and ITO. (c). Sample A has TJ and is processed without CBL or ITO. (d). Sample B has TJ and is processed with CBL and ITO. 29
Figure 2.3 Atom probe tomography (APT) concentration profiles for magnesium, aluminum, oxygen, and gallium near the TJ interface. (a). Spatial distribution of Mg, Al, O, and Ga (from surface to bottom: n-side TJ || regrowth interface || MOCVD grown blue LED). (b). Concentration profiles for Mg, O, and In near the regrowth interface (from left to right: n-

side TJ || regrowth interface || MOCVD grown blue LED). Data courtesy of Dr. Bastien Bonef. 31
Figure 2.4 SIMS concentration profiles for silicon, magnesium, and indium near the tunnel junction region (no Si δ-doping). Data courtesy Dr. Tom Mates. 32
Figure 2.5 SIMS concentration profiles for silicon, magnesium, carbon, hydrogen, and oxygen near the tunnel junction region for (a). samples treated by BFH dip (sample 3); and (b). sample treated by solvent clean before regrowth (sample 4). The sample cleaned by BHF has sharper Mg profile at the junction. The level of C, H, and O impurities were also lower. (Type II MOCVD wafer were used in this experiment). Data courtesy Dr. Tom Mates. 33
Figure 2.6 SIMS concentration profiles for silicon and magnesium for TJ samples with and without δ [Si] doping at the junction interface. The solid lines represent the sample with δ [Si] (sample 1). The dotdash lines represent the sample without δ [Si] (sample 2). The peak Si level near the samples' junction are 7.1×10^{20} cm^{-3} and 5.4×10^{20} cm^{-3} respectively. Data courtesy Dr. Tom Mates. 34
Figure 2.7 I-V characteristics of standard (sample R1) and TJ LEDs with (sample 1) and without (sample 2) Si δ-doping at the junction interface. At 20 $A\cdot cm^{-2}$, the voltage for sample R1, sample 1, and sample 2 were 2.87, 3.10, and 3.27 V respectively. The voltage penalty of sample 1 is only 0.23 V as compared to sample R1. 36
Figure 2.8 Charge coupled device (CCD) images of a LED from the three wafers at various current density. The white lines show the light intensity as a function of lateral or vertical position. The tunnel junction LEDs have more uniform light output than reference LEDs. (The same scale was used for all images.) 40
Figure 2.9 Examples of proposed light extraction structure for TJ LEDs. (a). The conductive layer (ITO) is between metal contact and CBL. (b). The conductive layer (ITO) is above the metal contact. 42
Figure 2.10 Examples of samples with and without titanium backside coating grown with indium bonding. The indium and titanium on the sample backside partially evaporated during growth. 46
Figure 2.11 LED samples showing emission under RHEED at the initial stage of growth. The blue samples were LEDs. The yellow sample was GaN on sapphire template. 47
Figure 2.12 AFM image of TJ sample grown on m-plane. The rms roughness is 3 nm. 47
Figure 3.1 (a). MBE n-AlGaN regrowth was done on the on top of the p-GaN and n-AlGaN region of the MOCVD grown UVC LED sample to form hybrid TJ UVC LED. Figure courtesy Dr. Burhan SaifAddin. (b). Schematic of the UVC tunnel junction (TJ) LED epitaxial structure. 60
Figure 3.2 (a) Front view and (b) side view of an Al cell crucible. 61
Figure 3.3 SIMS measurements of Al cell shutter leak check. 62
Figure 3.4 (a) SEM image of a crack-free AlGaN layer (110 nm), Al=55.5%, and a growth rate of 218 nm/hr. (b) Optical microscope image of a crack-free $Al_{0.59}Ga_{0.61}N$ layer (1 µm) grown at 210 nm/hr showing no cracks. (c) AFM image of the AlN on SiC template, which shows step flow growth. The rms roughness is 0.3 nm (d) AFM image of 100 nm AlGaN layer grown by MBE on the template with Al%=65.5% and a growth rate of 216 nm/hr. The surface was smooth and rms roughness is 0.48 nm. 63
Figure 3.5 (a) ω-2θ scan of 100 nm $Al_{0.60}Ga_{0.40}N$ film grown at 218 nm/hr with clear thickness fringes. The spacings between the fringes were used to calculate the film thickness and growth rate. From left to right, the peaks are: AlGaN, SiC, and AlN peaks. (b) RSM scan

of 400 nm fully strained $Al_{0.60}Ga_{0.40}N$ film grown at the same condition as in 3 (a). The separation between the SiC (in the middle) and the AlGaN peak (bottom) was used to calculate the Al% composition and relaxation ratio. The same Q_x between the AlN (top) and AlGaN peak shows that the AlGaN film is fully strained. 64
Figure 3.6 Alloy composition and growth rate dependence with the growth temperature..... 65
Figure 3.7 3D APT reconstruction of 60 nm of $Al_{0.59}Ga_{0.41}N$ showing Al and Ga atoms. (b) 2D distribution of the Aluminum fraction measured from the dashed rectangle shown in (a). APT data courtesy Dr. Batien Bonef. 67
Figure 3.8 Doping optimization for n-AlGaN by varying the Si cell temperature using a growth rate of (a) 109 nm/hr at Al%=61.6% (series 1) and (b) 210 nm/hr at Al%=59.4% (series 2). The n-AlGaN grown at 109 nm/hr with the Si cell at 1450 °C was resistive and thus not shown in (a). The star shape denotes the optimum growth condition for the 210 nm/hr growth rate.. 69
Figure 3.9 AFM image of the optimum n-AlGaN growth condition (star sign in Figure 6). The RMS roughness is 0.6 nm. There were no pits on the surface.. 69
Figure 3.10 Si, C, H, and O concentration in n-AlGaN series 2 samples measured by secondary ion mass microscopy (SIMS). The n-type carrier concentration is included for comparison. The star shape denotes the optimum doping condition..................................... 70
Figure 3.11 IV curve for CTLM pattern with 10 nm gap on n-AlGaN with vanadium-based contact before and after annealing in N_2 gas at 720 °C for 30 s. 70
Figure 3.12 AFM images of the n-AlGaN regrown area on the UVC TJ LED..................... 71
Figure 3.13 (a) Electroluminescence spectra of the UVC LED with TJ. (b) I-V characteristics for the processed TJ LED, an LED with the same MOCVD structure but without the TJ regrowth, and an identical LED without regrowth but with 5 nm of p-GaN on top of the MOCVD structure. Figure courtesy Dr. Burhan SaifAddin. 73
Figure 3.14 The hole concentration and band diagram for UV LEDs with and without Al% grading. (a) Schematic of UV LED. (b) Schematic of UV LED with Al% grading of 85-55% in Mg:AlGaN layer. (c) At a Mg concentration of 1×10^{19}, hole concentration, h, is ~10^{16}. (d) with grading, h is ~ 10^{18}. (e-f) Valence band is closer to Fermi level with grading.............. 75
Figure 3.15 Images of samples after the regrowth. Indium-crept on the sample surface for UV LED wafers with SiO_2 hard mask. No such effect was observed for blank regrowth (for example, the sample on the top right)... 76
Figure 4.1 Charge and field profile for GaN p-n diode with lightly-doped drift region. Figure courtesy Dr. Yuewei Zhang. 88
Figure 4.2 Maximum breakdown voltage as a function of the net charge concentration in the drift region for p-n diode grown using different materials. Figure courtesy Dr. Yuewei Zhang. 89
Figure 4.3 SIMS measurements for O, C, and H level in UID GaN layers grown using growth rate of 0.6, 1.0, 1.5, and 1.7 µm/hr from right to left... 90
Figure 4.4 Schematics of processed sample used for CV measurements. Metal-insulator-semiconductor (MIS) structure was formed using ALD SiO_2 and Pt/Au.............................. 92
Figure 4.5 CV measurements of UID GaN grown at different growth rates. (a) Capacitance as a function of voltage. (b) Doping levels for different growth rate. Figure courtesy Dr. Esmat Farzana.. 93

Figure 4.6 AFM of 1 µm of UID GaN grown on the MCC substrate at 0.6 µm/hr and at growth temperature of 800, 820, and 840 °C, respectively. Figure courtesy Kai Shek Qwah. 94
Figure 4.7 Schematic of the diode epi structure. The drift region was 4 µm thick. (a) Continuously grown diode. (b) Interrupted diode with ambient exposure at the p-n junction interface........ 95
Figure 4.8 AFM image for typical continuously grown diode. The surface was smooth with no pits observed. Figure courtesy Kai Shek Qwah. 96
Figure 4.9 Processed diode. (a) Schematics of the processed vertical GaN p-n diode. (b) Optical microscope image of the processed diode. 97
Figure 4.10 Typical forward J-V characteristics of batch 1 diodes in (a) linear and (b) log scale. (c) Ideality factor of the diode. Figure courtesy Dr. Esmat Farzana, Dr. Morteza Monavarian. 98
Figure 4.11 Reverse J-V characteristics of the diode. The reverse breakdown voltage was 125 V. Figure courtesy Dr. Esmat Farzana, Dr. Morteza Monavarian. 99
Figure 4.12 Histogram of reverse voltage (V_{r_10}) of the diodes when a reverse current of 10 µA was reached. 100
Figure 4.13 Comparison of V_{r_10} for (a) continuous and (b) interrupted diode. 101
Figure 4.14 Samples grown without the improved cleaning procedure showed dust and crater-like defect after growth. Figure courtesy Dr. Morteza Monavarian. 102
Figure 4.15 Schematics of batch 2 diodes after processing. 103
Figure 4.16 Batch 2 diode performance in forward bias. (a) J-V characteristics in log scale. (b) Specific on-resistance. (c) Ideality factor. Figure courtesy Dr. Esmat Farzana, Dr. Morteza Monavarian. 104
Figure 4.17 Batch 2 diode performance in reverse bias. The leakage current was found to be dominated tool-related leakage. Both samples showed breakdown voltage over 1000 V (highest voltage of the instrument used for testing). Figure courtesy Dr. Esmat Farzana, Dr. Morteza Monavarian. 105
Figure 4.18 Comparison of the diode performance achieved in this study and reported in literature. Note the diode in this study had thinner (4 µm) drift region and didn't reach breakdown. Figure courtesy Dr. Esmat Farzana. 106
Figure 5.1 ω-2θ scan for InGaN sample coloaded by indium-bonding during growth. The sample with backside coating had In%=6.0% while the one without backside coating had In%=6.4%. In growth rate for the two samples were 106 and 107 nm/hr, respectively. 112
Figure 5.2 Schematic of the regrowth LEDs' epitaxial structure. 114

Chapter 1 p-type doping of GaN by valved Mg cell for tunnel junction applications

1.1 Introduction

1.1.1 III-Nitride MBE

Molecular Beam Epitaxy is a growth technique used to acquire high crystal quality semiconductors. An MBE system is usually under ultra-high vacuum (UHV) during operation [1]. The cryo panels helps maintain high vacuum in the growth chamber. During growth, sample is heated on the CAR (Continuous Azimuthal Rotation). The CAR is rotated so that the growth is uniform. When cells are heated, precursors have a longer mean-free-path than the distance from cell to substrate due to high vacuum. Gases and materials from cells react at the substrate. A pyrometer is used to monitor the substrate temperature as grown. The RHEED (Reflection High Energy Electron Diffraction) monitors the surface morphology.

III-Nitride materials can be grown by both N_2 plasma and NH_3 MBE. The former one's optimum growth regime is metal rich. Metal form ad-layers on substrate surface and is later dissolved to avoid metal island forming. [2] The defects in the material can form leakage path and affect the device performance. The growth temperature of plasma MBE is not limited. The

low temperature required for In incorporation can be met well still keeping good morphology. Any 0-100% In incorporation (GaN-InN) can be achieved with plasma MBE. [1]

High V-III ratio is optimum for NH_3 MBE growth. [3] The growth temperature of NH_3 MBE is limited by the pyrolyzing temperature of NH_3. At below 600°C, NH_3 pyrolyzing rate at the substrate surface reduces to zero. Thus, the low temperature necessary for In incorporation > 30% will lead to poor morphology. The NH_3 gas condenses on the cryo panel during growth. As more growth is done, green NH_3 ice accumulate on the panel. If cryo panel fails, the NH3 ice will vaporize and over pressure the main chamber. Thus, a recovery is run after every two weeks of growth.

MBE is mainly used for research purpose and sometimes used in industry to fabricate electronics. LEDs and Lasers fabricated by MBE is generally inferior to equivalent devices produced by MOCVD. However, MBE provides a high vacuum environment (base pressure ~1×10^{-9} torr) for crystal growth as opposed to MOCVD (15-750 Torr) [4]. Pyrometers and RHEED monitors the growth in real time. Thus, MBE's growth environment is easier to control, and the growth mechanism is better understood. It offers great research opportunities. Besides, the Mg-doped materials grown by MBE is active as grown [5] and allows device design with buried p-regions such as tunnel junctions. [6–10]

1.1.2 Valved Mg Cell

Traditionally, an effusion cell design as shown in Figure 1.1 is used for Mg doping. [11] In both plasma and NH_3 MBE, the Mg charge in such cell tends to be nitrided. The nitride layer forms a crust outside the Mg metal. It is then hard to get sufficient Mg flux out of the cell. The Mg-doping level is also unreproducible because the flux is not only depended on the cell

temperature but also affected by the nitride layer. One available solution is to run low temperature-high temperature cycles to crack the nitride layer and expose the inside charge. The steps are listed below:

<Raise up cell temperature to 450 °C – wait 60min>

<Cool down the cell to 100 °C – wait 30min>

<Repeat the cycle untill getting sufficient Mg flux>

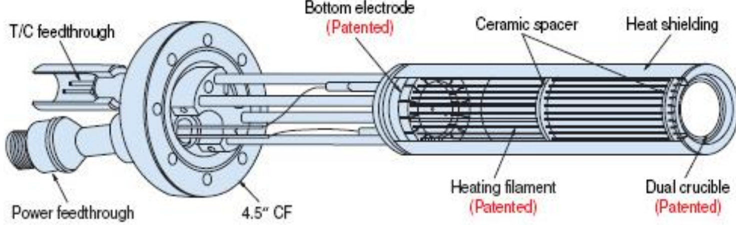
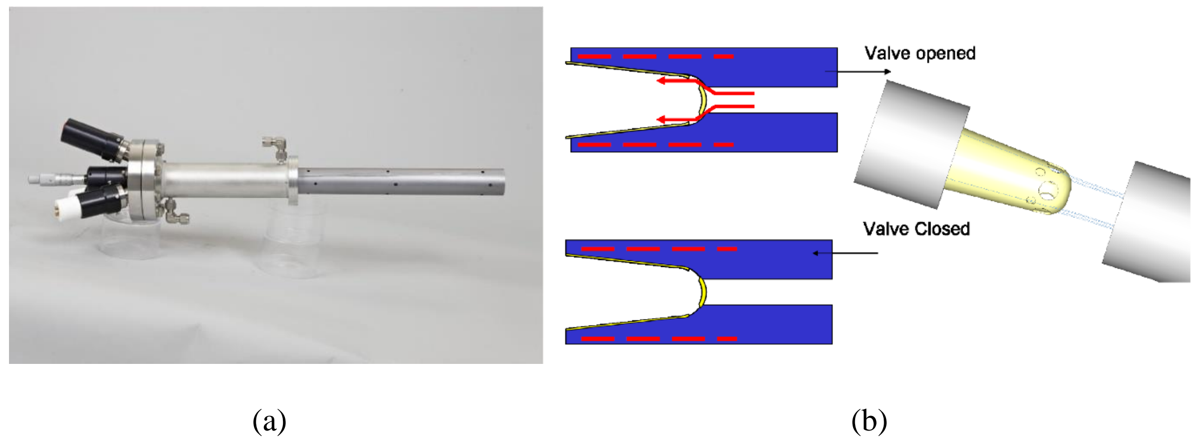


Figure 1.1 A typical design of an effusion cell. The charge is exposed to the growth environment.

Another option, which is adopted by this work, is using a valved Mg cell. Figure 1.2 shows an valved Mg cell [12]. In this design, the Mg flux is controlled by both the valve opening and cell temperature. At idle state, the valve is close, separating Mg charge from the growth environment. While operating, the valve opens, and certain Mg flux is realized. After operation, the valve is kept open until the growth is done and system pumps down to low pressure. This way, negligible amount of active gas is trapped inside the cell. The exposure of Mg charge to the active gas is minimized.



(a) (b)

Figure 1.2 Valved Mg cell used for this work. (a) Picture of a valved corrosive source model vcor 110 manufactured by Riber. (b) The valve opening is controlled by the vertical movement of parts (blue area in image).

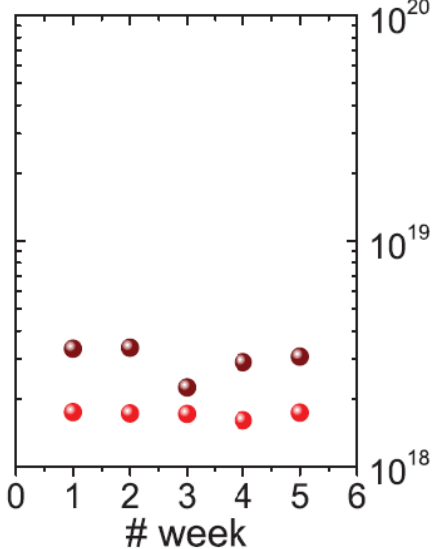


Figure 1.3 The doping level as a function of the week the Mg-doped samples are grown. The red and brown dots correspond to 10% and 15% valve opening respectively. The doping levels from 5 weeks' time fluctuates within $1\times 10^{18}/cm^3$ range, showing great reproducibility. Figure courtesy Prof. Nicholas Grandjean.

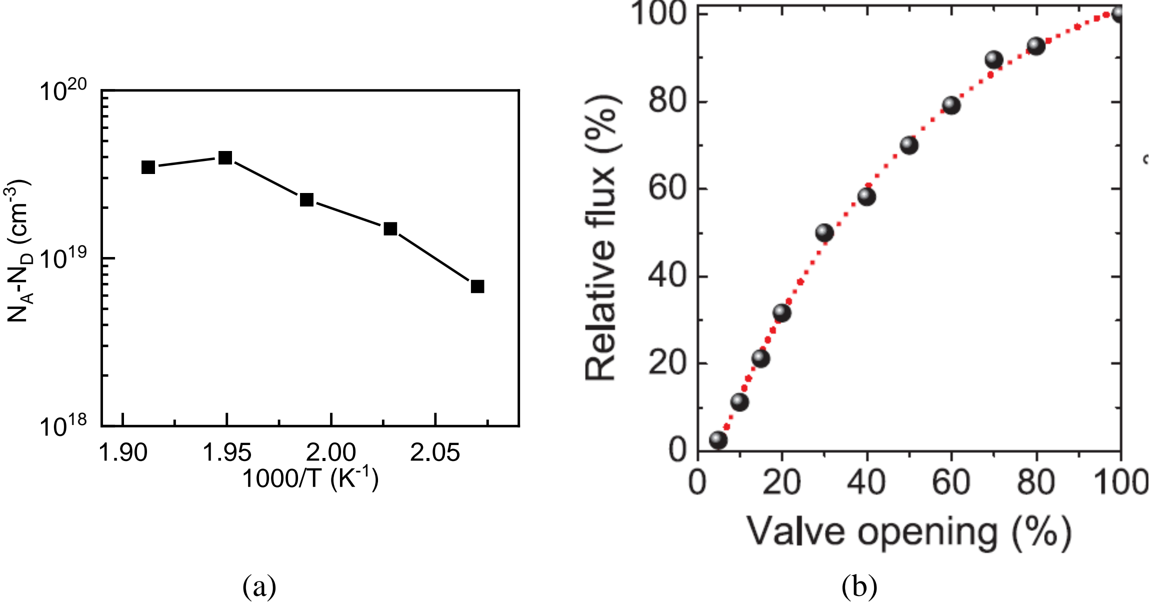


Figure 1.4 The Mg flux is controlled by both the cell temperature and valve opening. (a) The doping level increase exponentially as a function of cell temperature by CV measurements. The deviation on the start of trend is due to strong compensation effect. (b) Relative flux as a function of valve opening. The flux is highly controllable. Figure courtesy Prof. Nicholas Grandjean.

Figure 1.3 (provided by Prof. Nicholas Grandjean (EPFL)) shows the doping levels of p-GaN grown with the valved Mg cell. The samples are grown in a 5 weeks' time span. Figure 1.4 (provided by N. Grandjean 2016) shows the doping level as a function of cell temperature and valve opening. The Mg doping acquired is highly reproducible and controllable.

This valved Mg magnesium cell offers great opportunity. M. Malinverni, et al. has shown that low temperature MBE p-doped Al(Ga)N can be grown with this cell design by CV measurements. [13] Previously, with the traditional effusion Mg cell, one of the biggest obstacles to developing tunnel junctions and LEDs with the Veeco Nitride 930 MBE used in this work is the inability to grow p-layer with high while stable doping level. It is expected that with this valved Mg cell, structures such as all MBE tunnel junctions will be possible.

1.1.3 Mg-doping of III-Nitride Materials

When III-nitrides were first studied, the development of GaN-based devices is hindered because the highly resistive p-layer. Later in 1989, Amano et al. discovered the method of activating MOCVD p-GaN by postgrowth exposure to a low energy electron beam irradiation. [14] In 1992, Nakamura et al. showed that a thermal annealing in N_2 would activate MOCVD p-GaN by the eliminating the Mg-H complexes.[15,16] These works allow efficient MOCVD grown GaN-based LEDs.

In the hydrogen-rich MOCVD growth environment, magnesium is passivated by hydrogen, forming Mg-H complexes. [17,18] The p-layer layer can be activated by annealing in air or N_2. For the hydrogen to escape, the layer must be exposed since n-type GaN has high energy barrier for hydrogen. [19] This limit the device design to be p-side up only. MOCVD p-GaN also suffers from memory effect. [20,21]

The ultra-high vacuum(UHV) growth environment of MBE allows p-GaN to be active as grown. The hydrogen partial pressure inside MBE chamber ($<10^{-5}$ torr) is several orders of magnitude less than in MOCVD growths (~400 torr), limiting the formation of Mg-H complexes. Due to the same reason, MBE p-GaN has minor memory effect than MOCVD p-GaN. However, Mg acceptors gets compensated more in MBE p-type materials. The compensating donor is believed to be nitrogen vacancies. [22–24] Using Indium as a surfactant has been shown to reduce the compensation ratio of NH_3 MBE p-GaN by one to two orders of magnitudes and improve the morphology. [5] Low temperature NH_3 MBE p-(Al)GaN has been studied by CV measurements with a valved Mg-cell. [13]

In MOCVD material, Mg is compensated nearly 100% by the hydrogen. The nitrogen vacancy level is magnitudes lower than that of Mg. Thus, after eliminating the Mg-H

complexes by annealing, the material becomes p-type. In MBE material, hydrogen level is much lower compared to Mg level. However, the nitrogen vacancy is only slightly lower than that of Mg at high temperature. This explains why the optimum temperature for growing MBE p-GaN is around 740 °C. [5,25]

Another challenge for acquiring good p-type materials is the high activation energy of Mg in III-Nitrides. Magnesium has the lowest activation energy (~200 meV) as an acceptor species in GaN. However, it is still a deep acceptor. The hole concentration in p-GaN is usually several percentages of the Mg concentration. The activation energy is found to increase with band gap energy. [26] Ohmic contact to p-GaN can potentially be achieved with p-type InGaN.

1.1.4 Hall calibration sample epi structures

For p-type doping, a Mg level of > high 10^{18} is needed to achieve detectable hole concentration and ohmic contact. Hall measurements are also limited by detection limit of the setup for low mobility. Mobility below 10 $cm^2V^{-1}s^{-1}$ cannot be accurately measured by the conventional Hall setup such as the one used for this study.

The structure of p-GaN Hall calibration samples is used as an example to explain the epi structure to use for Hall measurement. For quick calibrations, 300 nm p-GaN on semi-insulating GaN:Fe on sapphire sample is usually used. To acquire a better Ohmic contact, 15 nm of p++ contact layer is grown on top. The equations for analyzing bi-layer Hall structures can be found at citation [27] and [28]. It is necessary to confirm that if the contact layer will not affect the measurement results before each Hall measurements done using contact layers.

Parasitic conducting channels at the regrowth interface can also affect the measurement. Carbon-doped GaN grown by PAMBE is insulating and used in high-electron-mobility

transistors (HEMT) [29]. By using 100 nm GaN:C at the regrowth interface, the impurities can be depleted. A 100 nm UID GaN layer can re-establish the growth morphology to be pit-free. Figure 1.5 shows the schematic epi structures for quick p-GaN Hall calibrations and more advanced structure for accurate Hall measurements.

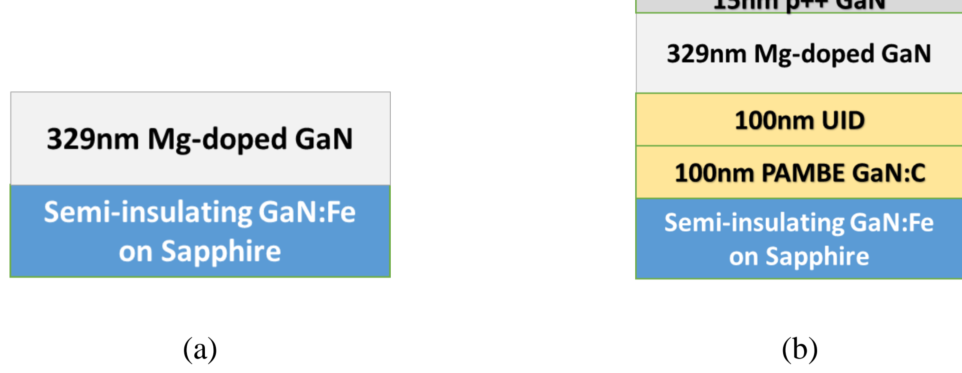


Figure 1.5 Schematic of epi structures for (a) quick p-GaN Hall calibrations and (b) accurate p-GaN Hall calibrations.

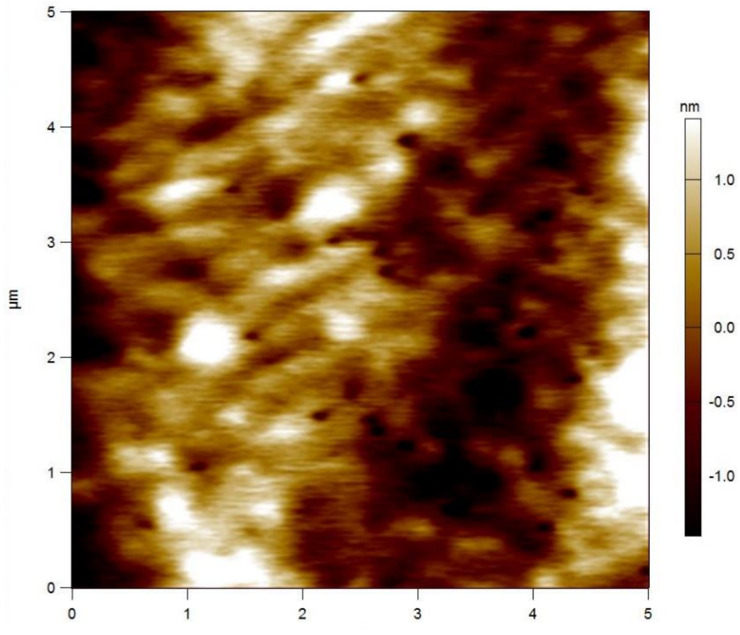


Figure 1.6 AFM images of GaN:C layer showing pits on the surface. The RMS roughness was 0.75 nm.

The growth of GaN:C was done using CBr_4 as the C source and N_2 plasma as the group V source. This requires a switch of growth mode if the later layers are grown using NH_3 MBE. The relationship between the CBr_4 flow and the C concentration was measured to be linear by SIMS measurements as shown in Figure 1.7. The GaN:C layers were grown using a N_2 flux of 1.1 sccm, a plasma power of 250 W, and a Ga flux of 1.8×10^{-7} torr. The growth temperature was kept around 790-740 °C to achieve optimum III-V ratio and thus optimum growth regime [2]. The growth rate was 258 nm/hr and the CBr_4 flux were 10, 20, and 30 sccm from bottom to top GaN:C layers.

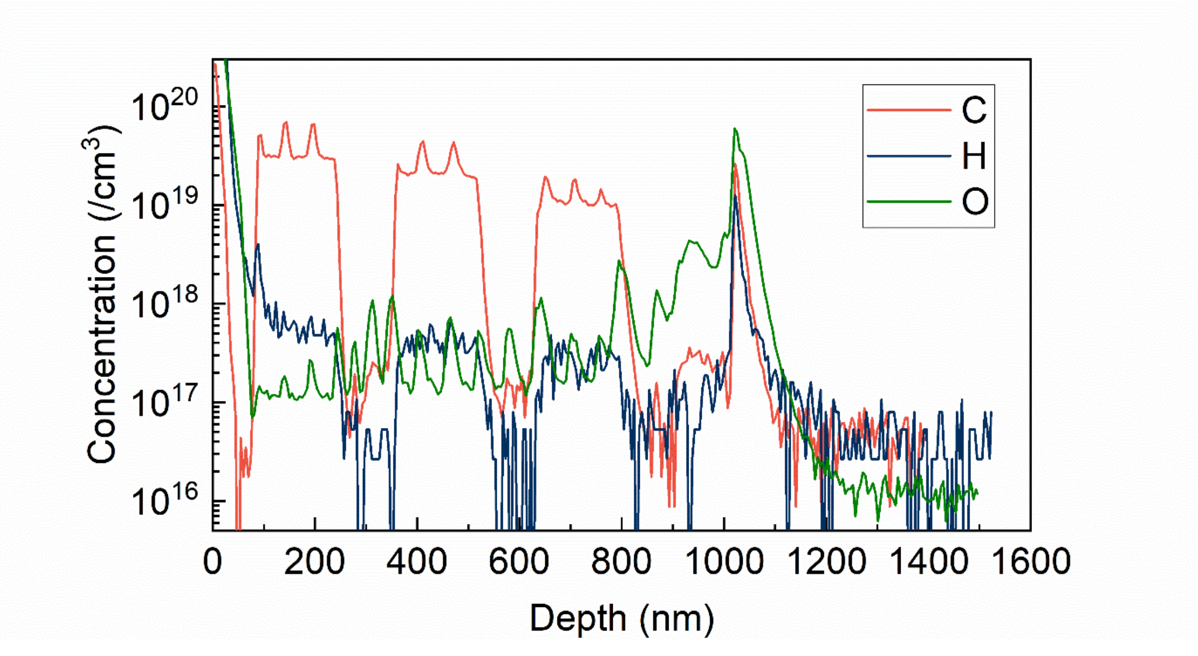


Figure 1.7 SIMS measurements for GaN:C SIMS stack. The CBr_4 flow used was 30, 20, 10 sccm for the GaN:C layers from left to right.

The H concentration for C doped layers were higher than the un-intentionally doped layers. The oxygen profile had huge peak at the growth interface showed incorporation in later layers. The O concentration eventually stabilized around 1×10^{17} /cm^3.

1.1.5 Temperature Controlled Hall Measurement

Room temperature Hall measurements can be used to determine the carrier concentration, mobility, and sheet resistance. Temperature controlled Hall measurements can be used to determine the acceptor concentration, compensating donor concentration, and activation energy.

In a non-degenerate p-type semiconductor, charge neutrality gives the following equation [30]:

$$\frac{p(p+N_D)}{(N_A-N_D-p)} = \frac{N_V}{g}\exp\left(\frac{-E_a}{k_BT}\right)$$

where p is the hole concentration, N_D is the donor concentration, N_A is the acceptor concentration, N_V is the effective density of states in the valence band ($N_V = \frac{2(2\pi m_h{}^* k_BT)^{\frac{3}{2}}}{h^3}$), h is Plank's constant, $m_h{}^*$ is the effective hole mass in GaN, ($m_h{}^* = 1.25m_0$ [31]), g is the acceptor degeneracy ($g = 4$), E_a is the ionization energy of a hole, k_B is the Boltzmann constant.

The ionization energy is observed to decreases with increasing ionized acceptor concentration in Mg-doped GaN. [32,33] Thus, it is important to account for the reduction in ionization energy from the Columbic potential between ionized acceptors and holes. The following equation was adapted for p-type GaN [33]:

$$E_a(N_A{}^-) = E_{a0} - f\frac{q^2}{4\pi\epsilon}(N_A{}^-)^{1/3}$$

where $N_A{}^-$ can be assumed to follow $N_A{}^- = p + N_D{}^+, N_D{}^+ = N_D$ (shallow donor). E_{a0} is the acceptor ionization energy. It can be assumed to be the same for p-GaN samples with Indium concentration less than 1×10^{20} cm^{-3} [5]. f is the geometric factor $(4\pi)^{\frac{1}{3}}\Gamma\left(\frac{2}{3}\right)$. [33]

Γ (x)is the gamma function. q is the charge of an electron or hole. ϵ is the dielectric constant (assumed to be $9.5\epsilon_0$).

By fitting the hole concentration and temperature relationship to the above equations, acceptor concentration, compensating donor concentration, and activation energy can be determined.

1.2 Impurity reduction in p-GaN

Mg-doped GaN are grown with a Veeco Gen 930 MBE system with conventional effusion cells for Ga, In, Al, Si, and valved Mg cell corrosive source model vcor 110 manufactured by Riber Inc. Purified NH_3 feed though an unheated showerhead injector. GaN:Mg Hall samples were grown on top of semi-insulating GaN:Fe on sapphire template manufactured by Lumilog Inc. Growths are done in a NH_3-rich growth regime. The Mg source was kept at 250 °C and the opening was varied to achieve the desired amount of Mg incorporation.

Figure 1.8 shows the atomic force microscopy (AFM) image of a p-GaN sample grown at typical growth condition. 329 nm of Mg-doped GaN was grown with a growth rate of 281 nm/hr at a growth temperature of 760 °C. Indium with a flux of 1×10^{-8} torr was used. The NH_3 flow rate was 200 sccm. The Mg valve was at 25% opening. The 1×1 μm^2 AFM image shows no pits on the surface. The root mean square (rms) roughness is 0.701 nm.

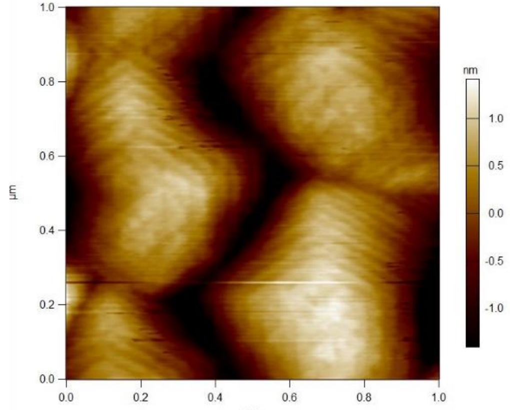


Figure 1.8 Typical AFM image of p-GaN grown with indium surfactant.

Hall measurements showed that the hole concentration is 4.56×10^{17} cm^{-3}, with a resistivity of 0.95 Ω·cm, and a mobility of 13 $cm^2 \cdot V^{-1} \cdot s^{-1}$.

A 10 period of 5 nm low temperature InGaN/19 nm high temperature GaN superlattice [34] was grown under the p-GaN to test its effect in terms of impurity reduction. The p-GaN growth condition was kept the same as the sample described above. Schematic of the p-GaN structure with and without the superlattice is shown in Figure 1.9.

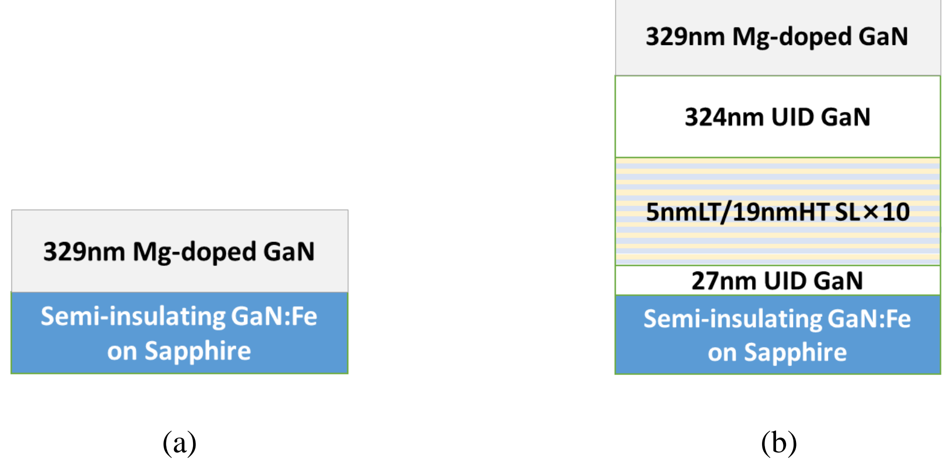
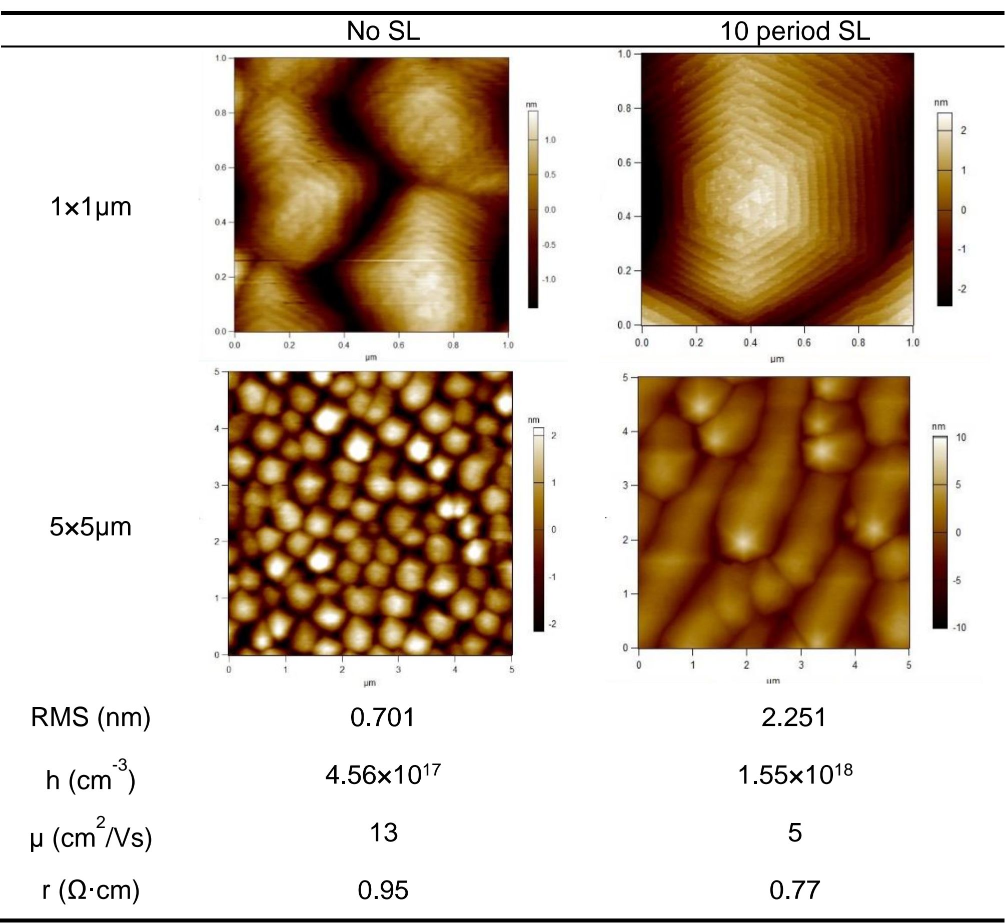


Figure 1.9 Schematic of the epi structure for p-GaN Hall sample with and without 10 periods of low temperature/high temperature impurity reduction super lattice.

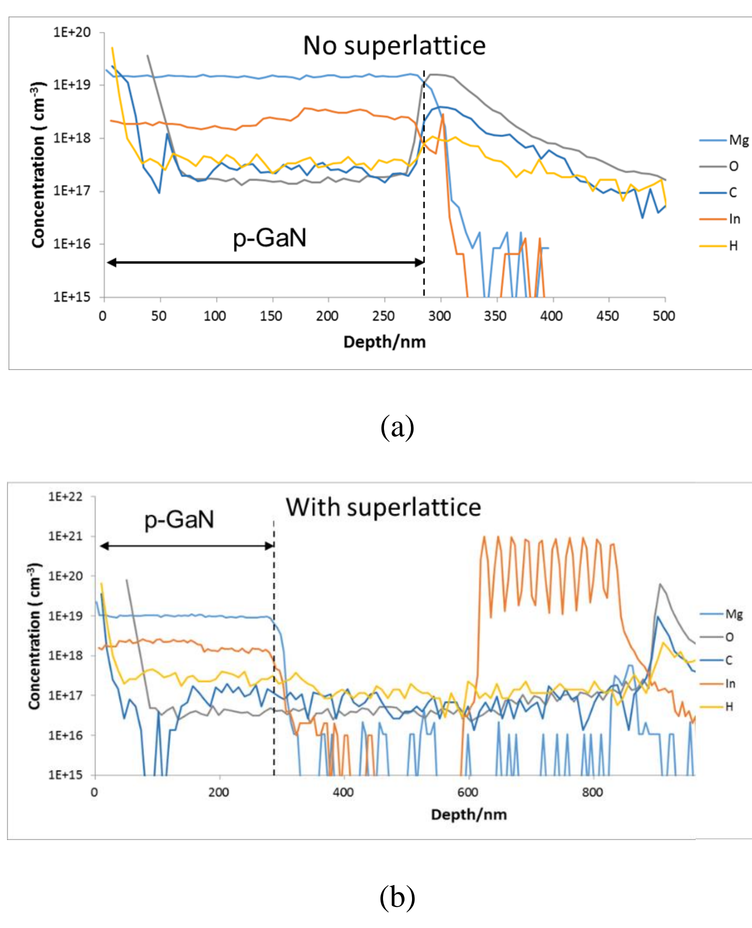
Table 1.1 compares the AFM and Hall measurement result for the two samples. The superlattice reduced the resistivity of the p-GaN without degrading the morphology.

Table 1.1 AFM images and Hall measurements for p-GaN grown at the same condition with and without impurity reduction super lattice.



	No SL	10 period SL
1×1μm		
5×5μm		
RMS (nm)	0.701	2.251
h (cm^{-3})	4.56×10^{17}	1.55×10^{18}
μ (cm^2/Vs)	13	5
r (Ω·cm)	0.95	0.77

To investigate the impurity concentration change from the use of superlattice, Secondary-ion mass spectrometry (SIMS) measurements were done for the two sample. Figure 1.10 shows the Mg, In, C, H, and O concentrations in the samples. The result is summarized in Table 1.2.



(a)

(b)

Figure 1.10 Secondary-ion mass spectrometry (SIMS) measurements of p-GaN sample grown with and without superlattice.

Table 1.2 Summary of SIMS measurement for p-GaN grown with and without the superlattice.

atom·cm^{-3}	No SL	SL
[Mg]	1.49×10^{19}	9.89×10^{18}
[In]	2.33×10^{18}	1.91×10^{18}
[O]	1.93×10^{17}	3.77×10^{16}
[C]	2.51×10^{17}	$<1.26\times10^{17}$
[H]	3.61×10^{17}	2.95×10^{17}

The O and C concentration was greatly reduced while the H level was almost the same. We suspect that the hydrogen was from the NH_3 used during growth and thus its incorporation wasn't reduced by the use of superlattice.

1.3 Range of Mg doping level achieved

The Mg doping level is controlled by either the Mg valve opening or the growth rate while fixing the Mg cell temperature at 250 °C. To map out the Mg level achievable, a SIMS stack with various growth condition (Table 1.3) was grown. The growth was done with a NH_3 flow of 200 sccm, an indium flux of 5×10^{-8} torr, at 750 °C. The result is shown in Table 1.3 and Figure 1.11. The maximum Mg level achieved was around 3×10^{20} cm^{-3}, using a growth rate of 50 nm/hr and a Mg valve opening of 100%. This high doping level is beneficial for TJ applications where the Mg level in the p^{++} layer is high. A typical Mg concentration for high quality p-GaN is around mid 10^{19} cm^{-3}, and is achieved using a growth rate of 300 nm·hr^{-1}.

Table 1.3 Growth conditions for the Mg SIMS stack

Mg%	*%*	*UID*	*80*	*80, In*	*80*	*65*	*50*	*UID*	*Template*
Growth rate	nm/hr	300	100	100	300				N/A
Mg	/cm^3	1.5 $\times10^{18}$	1.7 $\times10^{20}$	1.9 $\times10^{20}$	7 $\times10^{19}$	5.7 $\times10^{19}$	3.5 $\times10^{19}$	5 $\times10^{16}$	1.2 $\times10^{16}$
H	/cm^3		2.7 $\times10^{19}$	2.3$\times10^{19}$	1.2 $\times10^{19}$	1.4 $\times10^{19}$	1.3 $\times10^{19}$		

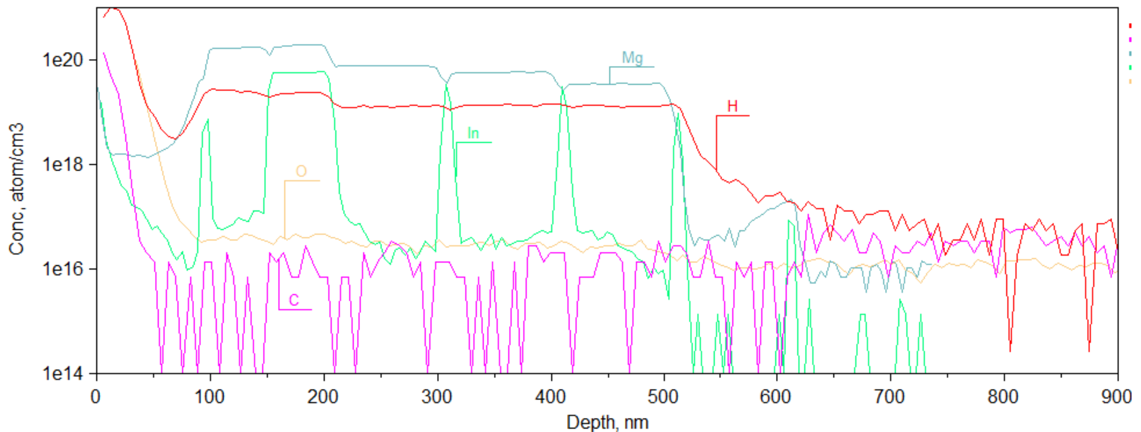


Figure 1.11 SIMS of Mg, H, C, H, and O level in Mg SIMS stack sample.

1.4 H_2 diffusion in MBE p-GaN grown with high NH_3 flux

The H-Mg complex formed during p-GaN growth by MOCVD lower the formation energy of compensating defects [17]. Effort was made to see if passivation of MBE grown p-GaN can be realized by growing at high NH_3 flux of 1000 sccm. Figure 1.12 shows the SIMS profile for Mg and H level in as grown MBE p-GaN and the same sample after annealing in air at elevated temperature.

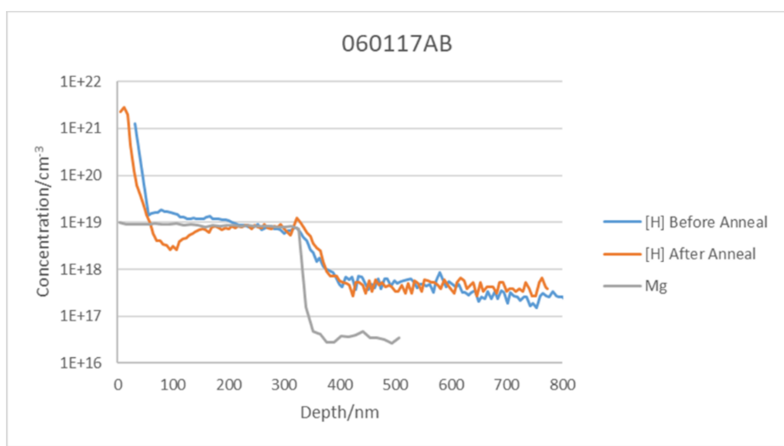
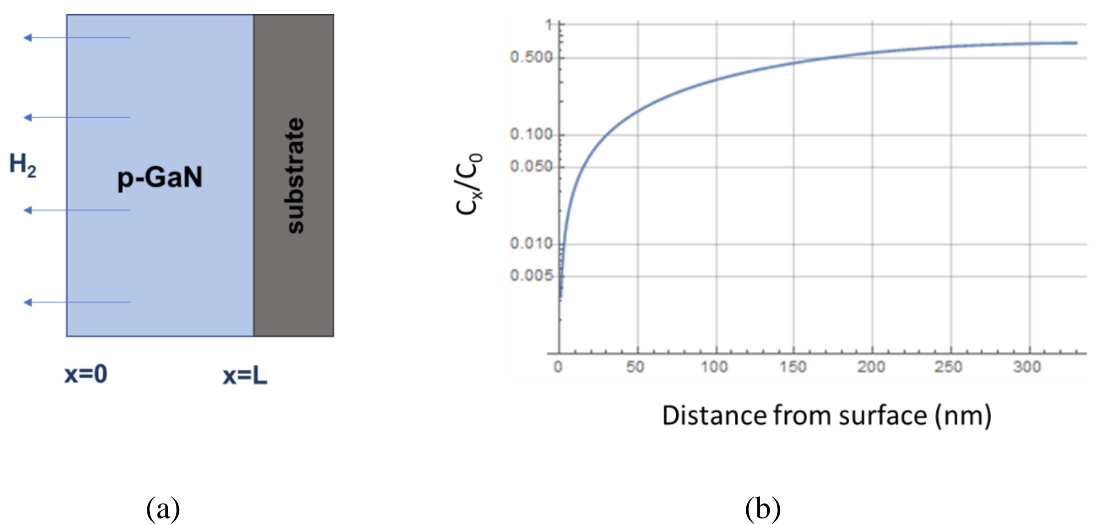


Figure 1.12 SIMS measurement for Mg-doped GaN grown at 1000 sccm before and after annealing.

The hydrogen profile shows partial diffusion from the sample surface. The diffusion process can be simplified as single-side diffusion model with surface sink and an initial H_2 concentration C_0 across the sample thickness L as shown in Figure 1.13. The boundary conditions include: 1. H_2 flux=0 at x=L (the growth interface between p-GaN and substrate). 2. The H_2 concentration for the sample surface (x=0) is zero. The concentration changes with time based on the solution to Fick's law [35]:

$$c(x,t) = \sum_{n=0}^{\infty} \frac{4C_0}{(2n+1)\pi} \sin\left(\frac{(2n+1)\pi}{2L}x\right) \exp\left(-\left(\frac{(2n+1)\pi}{2L}\right)^2 Dt\right)$$

Where n is natural integral, and D is the diffusivity.



(a) (b)

Figure 1.13 The hydrogen diffusion in Mg-doped GaN follows Fick's law. (a) Initial concentration profile (b) concentration profile during the diffusion process as calculated by Mathematica.

Table 1.4 shows SIMS profile for a GaN:Mg sample grown at 800 °C with a NH_3 flux of 1000 sccm, a growth rate of 200 nm/hr and a Mg valve opening of 50%. Before annealing, the H:Mg ratio is 37%. The hole concentration was 1×10^{17} cm^{-3}, the mobility was 8.5 cm$^{2}\cdot$V$^{-1}\cdot$s^{-1}, the resistivity was 7.4 Ω·cm. After annealing in air at 700 °C for 15 min, the Mg is fully

activated. With H:Mg = 5.7%, a hole concentration of 1.7×10^{17} cm^{-3}, a mobility of 6 $cm^{2}\cdot V^{-1}\cdot s^{-1}$, and a resistivity of 5.6 Ω·cm. The resistivity of the sample decreased by the annealing process but is still high probably due to the high growth temperature. More studies need to be done to understand how to apply this to more standard p-GaN condition.

Table 1.4 SIMS of p-GaN grown with high NH_3 flux before and after annealing.

	Mg	H	O
Before annealing	4.5×10^{19}	1.7×10^{19}	5.9×10^{17}
After annealing	4.4×10^{19}	2.5×10^{18}	1.0×10^{18}

References

1. E. C. H. Kyle, PhD thesis, University of California, Santa Barbara, Materials, *Growth Development of III-Nitrides for Electronic Devices by Molecular Beam Epitaxy* (2016).
2. B. M. McSkimming, F. Wu, T. Huault, C. Chaix, and J. S. Speck, "Plasma assisted molecular beam epitaxy of GaN with growth rates >2.6µm/h," Journal of Crystal Growth **386**, 168–174 (2014).
3. T. Kuech, *Handbook of Crystal Growth: Thin Films and Epitaxy* (Elsevier, 2014).
4. R. Pelzel, "A Comparison of MOVPE and MBE Growth Technologies for III-V Epitaxial Structures," CS MANTECH Conference, May 13th - 16th, 2013, New Orleans, Louisiana, USA (2013).
5. E. C. H. Kyle, S. W. Kaun, E. C. Young, and J. S. Speck, "Increased p-type conductivity through use of an indium surfactant in the growth of Mg-doped GaN," Appl. Phys. Lett. **106**, 222103 (2015).
6. J. T. Leonard, E. C. Young, B. P. Yonkee, D. A. Cohen, C. Shen, T. Margalith, T. K. Ng, S. P. DenBaars, B. S. Ooi, J. S. Speck, and S. Nakamura, "Comparison of nonpolar III-nitride vertical-cavity surface-emitting lasers with tunnel junction and ITO intracavity contacts," in (International Society for Optics and Photonics, 2016), Vol. 9748, p. 97481B.
7. J. Leonard, E. Young, B. P. Yonkee, D. A. Cohen, T. Margalith, S. Denbaars, J. Speck, and S. Nakamura, "Demonstration of a III-nitride vertical-cavity surface-emitting laser with a III-nitride tunnel junction intracavity contact," Applied Physics Letters **107**, 091105 (2015).
8. T.-Y. Seong, J. Han, H. Amano, and H. Morkoç, *III-Nitride Based Light Emitting Diodes and Applications* (Springer, 2017).
9. C. A. Forman, J. T. Leonard, E. C. Young, S. Lee, D. A. Cohen, B. P. Yonkee, R. M. Farrell, T. Margalith, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Nonpolar GaN-based vertical-cavity surface-emitting lasers," in *2016 International Semiconductor Laser Conference (ISLC)* (2016), pp. 1–2.
10. Y. Zhang, S. Krishnamoorthy, F. Akyol, S. Bajaj, A. A. Allerman, M. W. Moseley, A. M. Armstrong, and S. Rajan, "Tunnel-injected sub-260 nm ultraviolet light emitting diodes," Applied Physics Letters **110**, 201102 (2017).
11. "Effusion Cell & Controller(id:408742) Product details - View Effusion Cell & Controller from AlphaPlus Co., Ltd. - EC21," https://alphaplus.en.ec21.com/Effusion_Cell_Controller--408646_408742.html.
12. "CORROSIVE MATERIALS (eg. Sb) VALVED SOURCE - Riber," https://www.riber.com/en/products/mbe-components-sources/21-effusion-sources/213-valved-sources/2133-vcor-series-all-pbn-valved-source.html.
13. M. Malinverni, J.-M. Lamy, D. Martin, E. Feltin, J. Dorsaz, A. Castiglia, M. Rossetti, M. Duelk, C. Vélez, and N. Grandjean, "Low temperature p-type doping of (Al)GaN layers using ammonia molecular beam epitaxy for InGaN laser diodes," Appl. Phys. Lett. **105**, 241103 (2014).
14. H. Amano, M. Kito, K. Hiramatsu, and I. Akasaki, "P-Type Conduction in Mg-Doped GaN Treated with Low-Energy Electron Beam Irradiation (LEEBI)," Jpn. J. Appl. Phys. **28**, L2112 (1989).

15. S. Nakamura, N. Iwasa, M. Senoh, and T. Mukai, "Hole Compensation Mechanism of P-Type GaN Films," Jpn. J. Appl. Phys. **31**, 1258 (1992).
16. S. Nakamura, T. Mukai, M. Senoh, and N. Iwasa, "Thermal Annealing Effects on P-Type Mg-Doped GaN Films," Jpn. J. Appl. Phys. **31**, L139 (1992).
17. C. G. Van de Walle and J. Neugebauer, "First-principles calculations for defects and impurities: Applications to III-nitrides," Journal of Applied Physics **95**, 3851–3879 (2004).
18. J. Neugebauer and C. G. Van de Walle, "Hydrogen in GaN: Novel Aspects of a Common Impurity," Phys. Rev. Lett. **75**, 4452–4455 (1995).
19. J. Neugebauer and C. G. Van de Walle, "Role of hydrogen in doping of GaN," Appl. Phys. Lett. **68**, 1829–1831 (1996).
20. Y. Ohba and A. Hatano, "A study on strong memory effects for Mg doping in GaN metalorganic chemical vapor deposition," Journal of Crystal Growth **145**, 214–218 (1994).
21. H. Xing, D. S. Green, H. Yu, T. Mates, P. Kozodoy, S. Keller, S. P. DenBaars, and U. K. Mishra, "Memory Effect and Redistribution of Mg into Sequentially Regrown GaN Layer by Metalorganic Chemical Vapor Deposition," Jpn. J. Appl. Phys. **42**, 50 (2003).
22. J. Neugebauer and C. G. V. de Walle, "Native defects and impurities in GaN," in *Advances in Solid State Physics 35*, Advances in Solid State Physics (Springer, Berlin, Heidelberg, 1996), pp. 25–44.
23. U. Kaufmann, M. Kunzer, M. Maier, H. Obloh, A. Ramakrishnan, B. Santic, and P. Schlotter, "Nature of the 2.8 eV photoluminescence band in Mg doped GaN," Appl. Phys. Lett. **72**, 1326–1328 (1998).
24. P. Kozodoy, S. Keller, S. P. DenBaars, and U. K. Mishra, "MOVPE growth and characterization of Mg-doped GaN," Journal of Crystal Growth **195**, 265–269 (1998).
25. M. Malinverni, J.-M. Lamy, D. Martin, E. Feltin, J. Dorsaz, A. Castiglia, M. Rossetti, M. Duelk, C. Velez, and N. Grandjean, "Low temperature p-type doping of (Al)GaN layers using ammonia molecular beam epitaxy for InGaN laser diodes," Applied Physics Letters **105**, (2014).
26. K. Kumakura, T. Makimoto, and N. Kobayashi, "Activation Energy and Electrical Activity of Mg in Mg-Doped InxGa1-xN (x<0.2)," Jpn. J. Appl. Phys. **39**, L337 (2000).
27. S. H. Jain, P. B. Griffin, and J. D. Plummer, "Hall measurements of bilayer structures," Journal of Applied Physics **93**, 1060–1063 (2002).
28. "Mobility," in *Semiconductor Material and Device Characterization* (John Wiley & Sons, Ltd, 2005), pp. 465–522.
29. G. Koblmüller, R. M. Chu, A. Raman, U. K. Mishra, and J. S. Speck, "High-temperature molecular beam epitaxial growth of AlGaN/GaN on GaN templates with reduced interface impurity levels," Journal of Applied Physics **107**, 043527 (2010).
30. *Semiconductor Physics - An Introduction | Karlheinz Seeger | Springer* (n.d.).
31. B. Santic, "On the hole effective mass and the free hole statistics in wurtzite GaN," Semicond. Sci. Technol. **18**, 219 (2003).
32. P. Kozodoy, H. Xing, S. P. DenBaars, U. K. Mishra, A. Saxler, R. Perrin, S. Elhamri, and W. C. Mitchel, "Heavy doping effects in Mg-doped GaN," Journal of Applied Physics **87**, 1832–1835 (2000).

33. W. Götz, R. S. Kern, C. H. Chen, H. Liu, D. A. Steigerwald, and R. M. Fletcher, "Hall-effect characterization of III–V nitride semiconductors for high efficiency light emitting diodes," Materials Science and Engineering: B **59**, 211–217 (1999).
34. E. C. Young, N. Grandjean, T. E. Mates, and J. S. Speck, "Calcium impurity as a source of non-radiative recombination in (In,Ga)N layers grown by molecular beam epitaxy," Appl. Phys. Lett. **109**, 212103 (2016).
35. "Solutions to the Diffusion Equation," in *Kinetics of Materials* (John Wiley & Sons, Ltd, 2005), pp. 99–129.

Chapter 2 Hybrid Tunnel Junctions for Visible Applications

2.1 III-nitride blue light-emitting diodes utilizing hybrid tunnel junction with low excess voltage

2.1.1 Introduction

Tunnel junction (TJ) diodes have attracted great interest since they were first demonstrated by Esaki in 1958 [1]. They provide a means of carrier conversion between p-type and n-type materials and have shown great potential for III-nitride based optical and power electronic devices. Due to the poor conductivity of p-type GaN and the difficulty to achieve ohmic p-contacts, conventional III-nitride optical devices such as LEDs and LDs use transparent conductive oxides (TCOs), such as n-type Sn-doped In_2O_3 (ITO), as the p-side current spreading layer [2]. However, ITO suffers from high optical absorption, especially in the case of UV wavelength devices and LDs [3]. TJs eliminate the need for ITO by providing current spreading in the n-GaN layer [4–8]. Similarly, conventional flip-chip (FC) devices use absorptive silver-based mirrors which have adhesion and tarnishing issues. TJs allows the use

of dielectric-based omnidirectional reflectors (ODRs), thus avoiding any silver metallization for visible FC LEDs [9] and improve light extraction efficiency in UV LEDs [10]. Other benefits of using TJ includes facilitating hole injection [5,11–17], allowing for multiple active region epi design [18–27], allowing for p-down device design [28–31], and providing current confinement especially in LDs [4,32–38].

Despite the advantages, there are challenges for using TJs in III-nitride devices, one of which is the penalty in operating voltage. Due to the wide bandgap of III-nitride materials, a reverse bias voltage is needed to achieve appreciable tunneling currents. Typically, the excess voltage for MOCVD grown TJ devices, compared to ITO/p-GaN contacts, is $\Delta V_F \approx 1$ V. This might be insignificant for some research-purpose devices but not for well-developed commercial devices such as blue LEDs or lasers due to the strict efficiency requirements. Several epi design strategies have been demonstrated to reduce the voltage penalty. The most fundamental approach is to increase the doping density on each side of the junction [4,6,39–41]. Another approach is to use InGaN [5,12,42–45] or AlN [46–49] as an interlayer or part of the GaN TJ, or in the case of UV LEDs, to use (In)GaN in the AlGaN TJ [14–17,41,50,51]. This takes advantage of the intrinsic spontaneous and piezoelectric polarization properties for III-nitride materials and the narrower band gap of the interlayers. The limitations of this approach include potential optical absorption by the narrow bandgap layer and the high voltage from the use of AlN. It has also been demonstrated that by introducing mid-gap states, such as the use of GdN nanoparticles [52], the tunneling distance can be reduced - however, the diode resistance was high.

The voltage penalty also arises from incomplete activation of buried p-layers in the TJ. While many TJ devices are successfully demonstrated by molecular beam epitaxy (MBE), the

industry standard technique for growing III-nitride optical devices is by MOCVD. The hydrogen used in the carrier gas during MOCVD growth forms neutral complexes with the magnesium acceptor [53,54]. Thus GaN:Mg layers require post-growth activation by thermal annealing in vacuum or air [55]. However, this approach only works for exposed p-layer due to the high energy barrier for hydrogen diffusion in n-GaN . Regrowth on top of p-GaN layer can also re-passivate previously activated Mg [8]. One way to avoid hydrogen re-passivation in MOCVD TJ regrowth is to use a low growth temperature [56,57]. This method was combined with use of interlayer [57] and a rough n-GaN surface which will facilitates light extraction [56]. Attempts have been made to activate MOCVD TJ devices through the mesa sidewalls [8,39,58–60] or via in-situ annealing [37]. However, the operating voltage was still high [59] and nonuniform light output were observed in the LEDs [8], suggesting partial activation of p-GaN. Vertical p-GaN activation has been recently demonstrated for large-area and micro MOCVD TJ LEDs by exposing part of p-GaN using selective area growth (SAG) [61,62]. To circumvent the p-GaN passivation issue, a hybrid growth approach has been first demonstrated by Malinverni et al. [4]. The active region was grown by MOCVD while part of the p-side region and the tunnel junction were grown by MBE. This approach utilizes both the high material quality of MOCVD and the active as-grown p-type GaN in MBE due to the low hydrogen partial pressure in the MBE growth environment. MBE also has weaker Mg memory effect [63]. Our group has shown similar hybrid growth approach for TJ devices where the active region and p-side of the TJ was grown by MOCVD and the n-side of the TJ was grown by ammonia MBE [6,9,32]. This hybrid growth technique has been successfully demonstrated on blue LEDs [6,45,64], silver-free flip chip blue LEDs [9], green LEDs [65], cascaded LEDs [22] [19], edge-emitting lasers [3,66], and vertical-cavity surface-emitting

lasers (VCSELs) [32,33,36], all in university settings. It would be interesting to see how the TJ technique can be applied in commercial devices that have strict voltage requirements.

In this work, we demonstrate low voltage penalty tunnel junction blue LEDs. To achieve low voltage penalty, hybrid TJ was formed by growing n-side of the TJ using MBE on MOCVD blue LED wafers. We studied the effect of regrowth interface cleaning procedures and the dopant level in the n-side of the TJ. To test the viability of using this technique in commercial applications, the study was carried out in both university and industry settings. Commercial MOCVD blue LED wafers were used in the study since their production is standardized in the industry. Besides, their electrical performance is relatively simple and better understood compared to more advanced devices, thus providing us an easy and robust way of evaluating the voltage penalty of TJ Although the use of MBE is limited in industry, remote plasma chemical vapor deposition (RPCVD) and sputtering deposition are highly feasible in the mass-production of III-nitride optical devices and share MBE's advantage of producing active as-grown p-layers [67,68]. In this Chapter, MBE was used due to its availability in research environment. We expect that similar results can be achieved using RPCVD and sputtering deposition if the same doping and surface cleaning methods are used.

2.1.2 Experimental

Industry blue LED epitaxial wafers were used for this study. The 4-inch blue LED wafers used for most of this study were from the same MOCVD run and had p-InGaN layer on top (type I in table 2.1). The wafers were activated in-situ in the MOCVD reactor after growth. Similar commercial wafers with p-GaN on top were used for studying the effect of regrowth surface treatment (type II). Experimental wafers were prepared for MBE growth to form the tunnel

junctions. Wafers to be processed in university cleanroom were diced into 1 cm × 1 cm squares while the ones to be processed by industry were diced into quarters of the 4-inch LED wafer to fit them into the 3-inch MBE sample carrier. Before regrowth the samples were cleaned by a (~1 min) dip in buffered HF solution except one sample were cleaned using acetone, isopropanol and de-ionized water to be used for comparison. The samples were vacuum sealed and taken out of the vacuum package immediately prior to indium-bonding on to silicon wafers and transferring into the MBE. The samples were baked at 400 °C for 1 hour in vacuum in the MBE before growth.

Table 2.2.1 Summary of parameters for each sample discussed in this study.

Processed by/in	*Sample ID*	*MOCVD wafer used*	*Tunnel junction growth*	*Regrowth surface treatment*	*Delta (Si) doping*	*p-side contact*	*n-side contact*
University cleanroom	R1	Type I				ITO + Cr/Ni/Au	Ti/Au
	1	Type I	✓	BHF	✓	Ti/Au	Ti/Au
	2	Type I	✓	BHF		Ti/Au	Ti/Au
	3	Type II	✓	BHF			
	4	Type II	✓	Solvent clean			
Industry	R2	Type I				CBL + ITO + Cr/Al/Ti/Pt/Au	Cr/Al/Ti/Pt/Au
	A	Type I	✓	BHF		Cr/Al/Ti/Pt/Au	Cr/Al/Ti/Pt/Au
	B	Type I	✓	BHF		CBL + ITO + Cr/Al/Ti/Pt/Au	Cr/Al/Ti/Pt/Au

The regrowth was done in a Veeco 930 MBE with NH_3 as the nitrogen source and solid effusion cells for Ga and Si. Reflection high-energy electron diffraction (RHEED) was used to monitor the sample surface morphology in real time. The growth temperature was monitored by a calibrated pyrometer and was adjusted between 700 °C and 760 °C to maintain a streaky RHEED pattern. A 200 sccm NH_3 flow was used during growth. The NH_3 overpressure

($\sim 4\times 10^{-6}$ Torr) was low enough to prevent hydrogen re-passivation of the p-type layers. The n-GaN growth rates were calibrated using high-resolution x-ray diffraction. The doping densities were calibrated using Hall measurements or secondary ion mass spectrometry (SIMS). Figure 2.1 shows the schematic of the TJ LED epitaxial structure. For one of the samples (sample 1 in table 2.1), a delta Si-doped layer were first grown targeting a surface concentration of $\sim 1.5\times 10^{14}$ cm^{-2} , or approximately 37.5% of a monolayer. The growth was done by keeping the Si shutter open and the Ga shutter closed, during which the NH_3 flow was kept at 200 sccm. For all TJ samples, a 20 nm n++ GaN layer with a doping density of [Si] $\approx 10^{20}$ cm^{-3} was grown to form the n-side of the tunnel junction. A slow growth rate of 80 to 200 nm/hr and a Si cell temperature of 1435 to 1450 °C were used to achieve high doping level and mobility. A 400 nm n-GaN layer ([Si]: $\sim 10^{19}$ cm^{-3}) was then grown to act as current spreading layer followed by 5 nm of n++ GaN ([Si]: $\sim 10^{20}$ cm^{-3}) as the contact layer. The two upper layers were grown at a growth rate of ~400 nm·hr^{-1}. The Si cell temperature for the n-GaN and upper n++ layers were 1425 °C and 1435-1450 °C respectively.

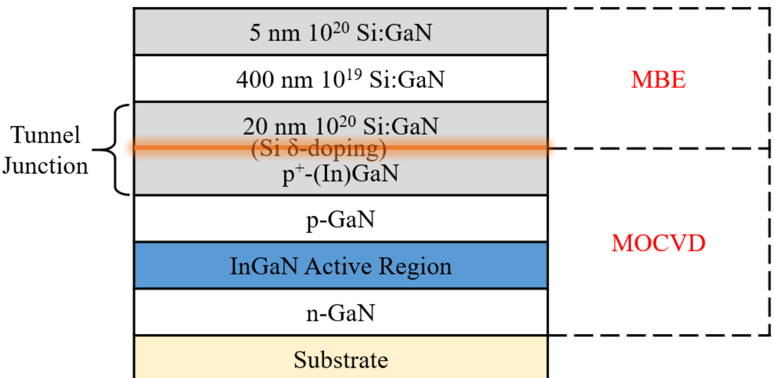


Figure 2.1 Schematic of the tunnel junction (TJ) LED epitaxial structure. The commercial MOCVD blue LED wafer has p-InGaN (type I wafer) or p-GaN (type II wafer) cap on top as part of the p-side tunnel junction. The MBE regrowth was carried out on the commercial wafer to form the tunnel junction n-side and n-GaN current spreading layers. A Si δ-doped layer was grown on one of the samples (sample 1).

Reference sample R1, TJ sample 1 and 2 were processed in parallel in the university cleanroom. 0.1 mm^2 circular devices were formed with p-side contact covering most area of the mesa surfaces to achieve accurate voltage measurements. A 110 nm ITO layer plus 25/20/500 nm of Cr/Ni/Au metal stack were deposited by electron beam evaporation to form the p-contact for sample R1. The n-contact for sample R1, as well as both n and p-side contacts for sample 1 and 2 were formed using 30/300 nm of Ti/Au metal stack. The reference sample R2 and the two experimental samples A and B were processed in parallel to each other by an industrial LED process. The final unencapsulated LED chip size was 584 μm × 1143 μm with a junction area of 0.6 mm^2 (Figure 2.2 (a)). A Cr/Al/Ti/Pt/Au metal stack was used for both the anode and cathode contacts. As shown in Figure 2.2 (b) and (d), the reference sample R2 and sample B were processed with ITO as the current spreading layer. A current blocking layer (CBL) was placed between the ITO and LED epi-surface under contact metal to avoid light absorption by the metal contact. Sample A was processed without the ITO and CBL layer as shown in Figure 2 (c). The LEDs were measured by industry testing techniques.

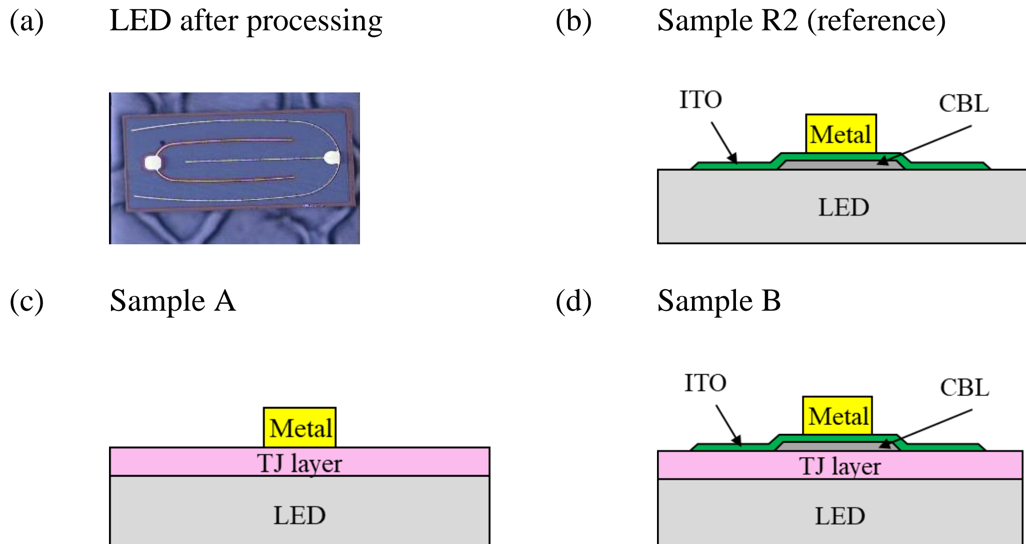


Figure 2.2 (a). Image of a LED processed by an industrial LED process. The chip size is 584 µm ×1143 µm. (b-d) Schematic of processed LED structure. (b). The reference sample R2 is processed with current blocking layer (CBL) and ITO. (c). Sample A has TJ and is processed without CBL or ITO. (d). Sample B has TJ and is processed with CBL and ITO.

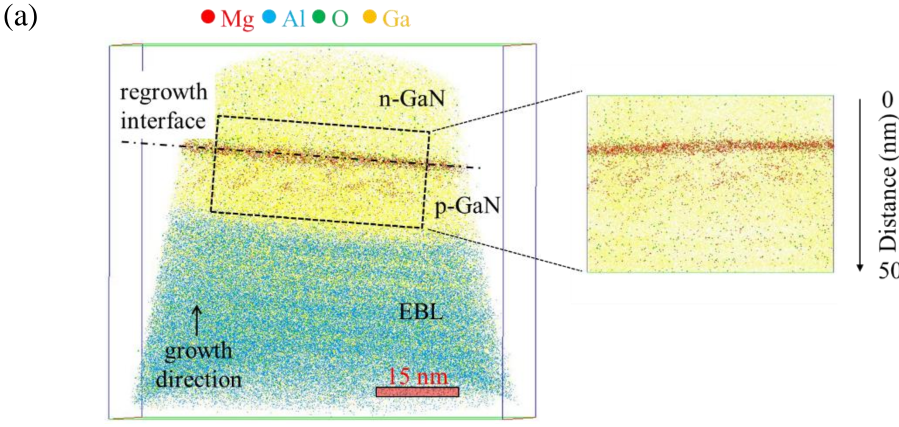
The TJ devices were also characterized using Atom probe tomography (APT) by Dr.Bastien Bonef with a Cameca local electrode atom probe (LEAP) 3000X HR. The high depth resolution of APT showed the three-dimensional (3D) distribution of dopants and impurities in the devices [69]. The Cameca IMS 7f Auto SIMS was used to measure the doping profile and impurities levels at the junction.

2.1.3 Results

Figure 2.3 shows the APT measurement for a TJ sample without delta Si doping grown on type I MOCVD LED wafer. The Mg level dropped sharply at the regrowth interface. This facilitates the formation of a sharp junction interface and prevents Mg from compensating donors on the n-side of the junction. The oxygen level (peak ~10^{19} cm^{-3}) is relatively low and barely visible

in APT resolution, suggesting that the surface cleaning of 1min BHF was effective. SIMS measurement of Si, Mg, and In levels near the regrowth interface are shown in Figure 2.4. It can be seen that Si and Mg doping form a relatively sharp junction at the regrowth interface. The [In] level was low (peak $< 1\times10^{20}$ cm^{-3}) possibly due to low In composition in the p-InGaN capping layer or the desorption of In during the initial temperature ramp up stage of MBE growth. With the p-InGaN layer having negligible In alloy composition, the tunnel junctions can be considered as GaN homo junctions. The concentration for atmospheric impurities (C, H, and O) at the junction were also measured (not shown in Figure 2.4). The peak values were all around 1×10^{19} cm^{-3}.

(a)



(b)

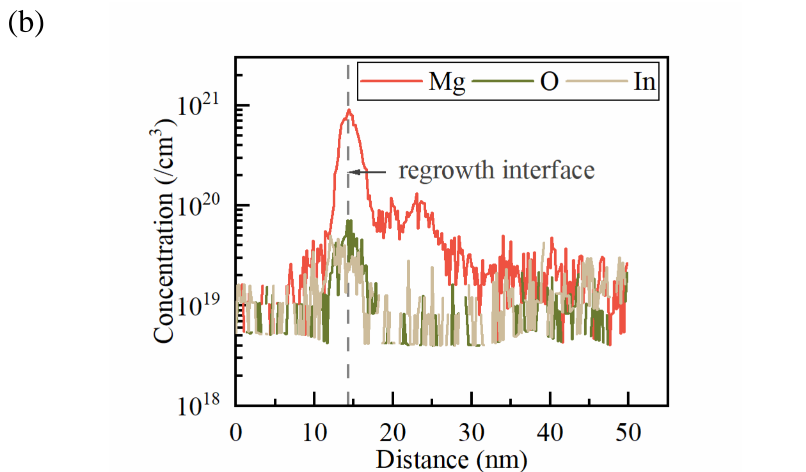


Figure 2.3 Atom probe tomography (APT) concentration profiles for magnesium, aluminum, oxygen, and gallium near the TJ interface. (a). Spatial distribution of Mg, Al, O, and Ga (from surface to bottom: n-side TJ || regrowth interface || MOCVD grown blue LED). (b). Concentration profiles for Mg, O, and In near the regrowth interface (from left to right: n-side TJ || regrowth interface || MOCVD grown blue LED). Data courtesy of Dr. Bastien Bonef.

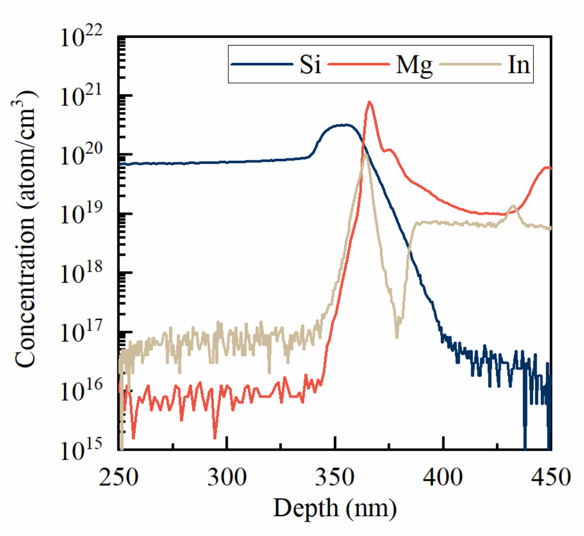


Figure 2.4 SIMS concentration profiles for silicon, magnesium, and indium near the tunnel junction region (no Si δ-doping). Data courtesy Dr. Tom Mates.

To investigate the effect of regrowth interface treatments, tunnel junctions were grown on similar commercial LED wafers (type II in table 2.1) using different regrowth surface treatment techniques. Sample 3 was dipped in BHF for 1 min before regrowth while sample 4 was only solvent cleaned. The two samples were co-loaded into MBE to grow the n-side TJ structure on top of them. The SIMS concentration profiles of dopants and impurities levels near the regrowth interface are shown in Figure 2.5. While the silicon profile and the peak dopant levels were almost identical for the two samples, the Mg profile for the sample treated with BHF had a more abrupt drop at the junction compared to solvent cleaned sample. The Mg level for BHF treated sample dropped to 2×10^{19} cm^{-3} at 10nm away from the profile peak, towards the n++ side. For solvent cleaned sample, this value is 9×10^{19} cm^{-3}. The concentration of C, H, O at the regrowth interface for BHF cleaned sample were 1×10^{17} cm^{-3}, 3×10^{18} cm^{-3}, and 6×10^{17} cm^{-3} respectively. For solvent cleaned sample, the C, H, O concentration were much higher: 1×10^{19} cm^{-3}, 1×10^{19} cm^{3}, and 4×10^{18} cm^{-3}, respectively. This suggests that the BHF dip effectively

removed the excess Mg at the MOCVD wafer surface and prevented its further incorporation into the n-side TJ. It also reduced the amount of C, H and O impurity incorporated into the TJ structure. This effect is especially strong for C and O, whose incorporation levels were reduced by 2 and 1 orders of magnitude, respectively, resulting in very small concentration peaks at the regrowth interface. There were differences in C, H, O incorporation levels between TJ LED grown on type I and type II wafers under the same BHF treatment. This could be a result of the different MOCVD wafer used. The storage time and conditions for the two type of MOCVD LED wafers may have also affected the result. The effect of different surface treatment on the electrical performance of TJ LEDs were demonstrated in our previous work and can be found elsewhere (Figure 2(a) in Ref. [9]). In that study, higher voltage penalty was observed in TJ samples without treatment compared to the one treated with 49% HF.

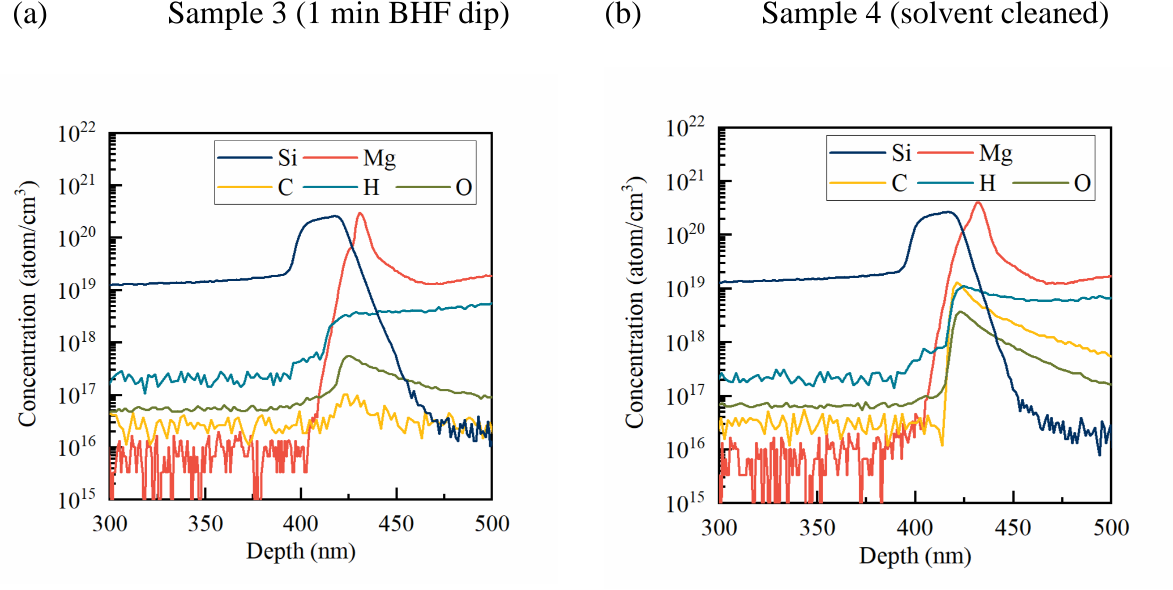


Figure 2.5 SIMS concentration profiles for silicon, magnesium, carbon, hydrogen, and oxygen near the tunnel junction region for (a). samples treated by BFH dip (sample 3); and (b). sample treated by solvent clean before regrowth (sample 4). The sample cleaned by BHF has sharper Mg profile at the junction. The level of C, H, and O impurities were also lower. (Type II MOCVD wafer were used in this experiment). Data courtesy Dr. Tom Mates.

The effect of silicon doping levels in the TJs were also investigated. In addition to the regular TJ structure, another sample was grown with delta silicon doping at the interface (sample 1). Silicon is known as an anti-surfactant in GaN growth. The amount of Si incorporated before degrading the epi quality is thus limited. During the growth of sample 1, the RHEED pattern turned a bit spotty for a few seconds when the lower n++ layer growth started, indicating partial 3D growth mode. As the growth continued, the RHEED pattern recovered and turned streaky. This suggest that even though the high delta Si doping roughens the morphology, it can be easily recovered by the subsequent growth. Figure 2.6 shows the doping levels for TJ sample with and without delta Si doping. Sample 1 had higher peak Si level of 7.1×10^{20} cm^{-3} compared to 5.4×10^{20} cm^{-3} for the sample without delta doping (sample 2). The extra Si continued to incorporate beyond the regrowth interface into the n++ layer. There was no significant difference in the Mg profile.

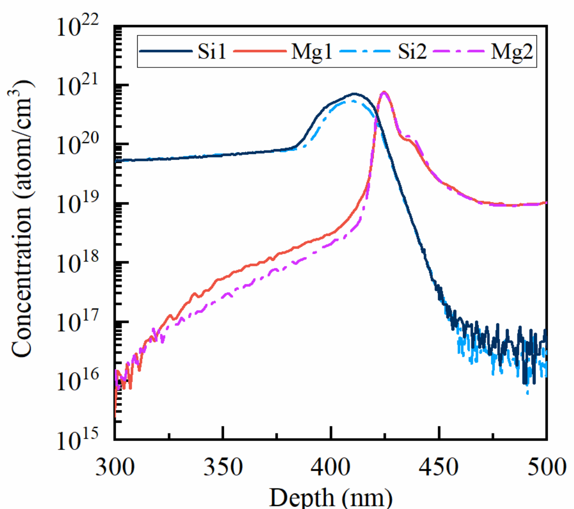


Figure 2.6 SIMS concentration profiles for silicon and magnesium for TJ samples with and without δ [Si] doping at the junction interface. The solid lines represent the sample with δ [Si] (sample 1). The dotdash lines represent the sample without δ [Si] (sample 2). The peak Si level near the samples' junction are 7.1×10^{20} cm^{-3} and 5.4×10^{20} cm^{-3} respectively. Data courtesy Dr. Tom Mates.

Sample 1 and 2 were processed in university cleanroom with the reference sample (sample R1). Metal contacts were formed on the n-side and p-side of the TJ samples using Ti/Au metal stack in the same lithography step. The reference sample had an ITO layer along with a Cr/Ni/Au metal stack deposited on the p-GaN. Circular transmission line measurement (CTLM) showed that the specific contact resistance r_c for the n-GaN contacts and the ITO to metal contacts were $1.5\text{-}4.6 \times 10^{-5}\ \Omega\cdot cm^2$ and $1.5\times10^{-5}\ \Omega\cdot cm^2$, respectively. For the contacts between p-GaN and ITO, no valid r_c were measured due to the plasma damage to the p-GaN material during ITO dry etching. Developments of ITO wet etching technique are underway to solve this issue. Figure 2.7 summarize the *I-V* performance for the three samples. A representative IV curve was shown for the devices tested on each sample. At 20 $A\cdot cm^{-2}$, the voltage for reference sample processed with ITO (sample R1), TJ sample with δ [Si] doping (sample 1), and TJ sample without δ [Si] (sample 2) were 2.87, 3.10, and 3.27 V. The voltage penalty of the TJ in sample 1 was only 0.23 V. The specific differential resistance of the samples at 20 $A\cdot cm^{-2}$ were 8.8×10^{-3}, 1.15×10^{-2}, and $1.51\times10^{-2}\ \Omega\cdot cm^2$ respectively. It can be concluded that a higher Si level at the junction interface can lower the forward voltage penalty and the dynamic resistance of the TJ. This is limited by the amount of Si that can incorporate into the material without degrading the crystal quality as stated above.

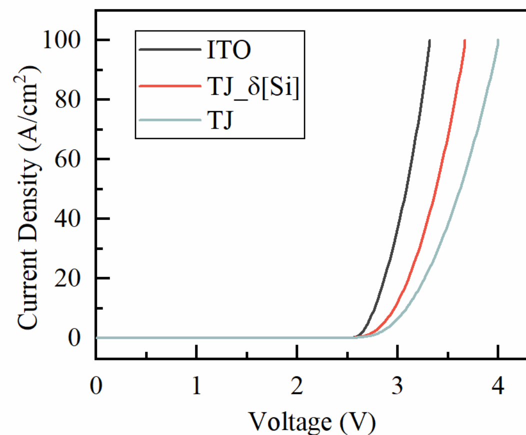


Figure 2.7 I-V characteristics of standard (sample R1) and TJ LEDs with (sample 1) and without (sample 2) Si δ-doping at the junction interface. At 20 A·cm^{-2}, the voltage for sample R1, sample 1, and sample 2 were 2.87, 3.10, and 3.27 V respectively. The voltage penalty of sample 1 is only 0.23 V as compared to sample R1.

In addition to process and measure LED performance using university cleanroom and testing instruments, wafers were processed using industry LED processes as shown in Figure 2.2. and table 2.2. After chip dicing, more than 9,000 unencapsulated LEDs were obtained using reference wafer (sample R2). More than 1,500 unencapsulated LEDs were obtained using either of the experimental quarter wafers (sample A&B). The LEDs were tested by industry measurement setups and the measured on chip before encapsulation. The average parameters are shown in Table 2.2.

Table 2.2.2 Average measured values for LEDs from the three wafers before encapsulation. The forward voltage V_F, light output power P_{out}, dominant wavelength W_d, and peak wavelength W_p were measured at 120 mA (20 A·cm^{-2}).

	V_{fin} *(V)*	V_F *(V)*	*R* (Ω·cm^2)	P_{out} *(mW)*	W_d *(nm)*	W_p *(nm)*	V_r *(V)*	I_r *(μA·cm^{-2})*
	Voltage @ 1 μA	Forward voltage	Specific differential resistance	Light output power	Dominant wavelength	Peak wavelength	Breakdown voltage	Current density @ -7 V
Sample R2 (reference, CBL + ITO)	2.37	**3.20**	1.5×10^{-2}	**238.76**	449.52	444.66	16.08	12.2
Sample A (TJ + no CBL or ITO)	2.39	**3.33**	2.4×10^{-2}	228.55	450.55	445.94	16.06	0.42
Sample B (TJ + CBL + ITO)	2.39	3.56	1.9×10^{-2}	**231.96**	449.14	444.46	16.07	0.48

Table 2.3 shows the statistical analysis for the LED forward voltage V_F at 120 mA (20 A/cm^2). The data used for this analysis had a margin error of 0.25 V. Since some of the LEDs processed from the central region of sample R2 were resistive, the mode value of R2's V_F (2.95 V) is more representative of the sample's electrical performance compared to the mean (average) value (3.20 V). This mode value is used for the comparison between samples later. When leaving out LEDs on R2 with V_F>3.6 V, the standard deviation for R2's V_F reduces to 0.10 V.

Table 2.2.3 Statistical analysis of the LED forward voltage V_F at 120 nm (20 A/cm^2). Some LEDs on sample R2 is resistive (V_F>3.4 V at 20 A/cm^2). By leaving them out, an improved representation of the sample electrical performance is shown in the table.

Sample	number of LEDs tested	mean	mode	median	standard deviation
Sample R2	9303	3.20	**2.95**	3.05	0.27
R2, leaving out the resistive samples	7698	3.07	**2.95**	2.95	0.10
Sample A	2185	3.33	**3.25**	3.25	0.12
Sample B	1528	3.56	**3.55**	3.55	0.37

The required forward voltages to get a current of 1 μA were similar for the three groups of LEDs (~2.4 V). The forward voltage measured at 120 mA (20 A·cm^{-2}) for sample A LEDs was 0.30 V higher than that of the reference LEDs. Since a tunnel junction LED has an n-GaN current spreading layer, ITO was unnecessary. The comparison of V_F between reference LEDs and sample A LEDs showed that the average voltage penalty for using TJ was 0.30 V. This value is similar to what we achieved in university settings (0.23-0.40 V) and can be further brought down by the use of Si delta doping. This indicated that when using tunnel junction in commercial devices, the resulting potential increase in forward voltage could be insignificant. The forward voltage of sample B LEDs was 0.60 V higher than that of the reference LEDs. We speculate that the excess voltage was caused by an unoptimized contact between ITO and n-GaN [70] since the process used was optimized for standard ITO devices design with ITO and p-GaN in contact. This issue could be solved by contact optimization [71].

The light output power for reference LEDs and sample B LEDs were similar. Reference A LEDs had slightly lower light output than the reference LEDs. The difference in power output between the TJ samples was presumably due to the use or absence of a CBL. The CBL inserted

below the metal can suppress current injection and light generation beneath the metal pad and thus reduce pad-related light absorption.

The dominant wavelength (~450 nm), peak wavelength (~445 nm), and the breakdown voltage (-16.07 V) were similar for the three groups of LEDs. At a reverse bias of -7 V, the two groups of tunnel junction LEDs had reverse currents of 0.42 $\mu A \cdot cm^{-2}$ and 0.48 $\mu A \cdot cm^{-2}$ respectively. This value was lower than that of ITO LEDs, which was 12.2 $\mu A \cdot cm^{-2}$.

Images recorded on a charge coupled device (CCD) camera of the unencapsulated LEDs at various current density are shown in Figure 2.8. The integrated intensity for a lateral or vertical position was shown by the fine white lines with arbitrary unit. The tunnel junction LEDs had more uniform light intensity than the reference LED, especially at higher current. This was possibly due to the more effective current spreading of n-GaN compared to the ITO layer. This shows the benefit of using tunnel junction especially in high power devices or when the light uniformity is of importance. After encapsulation, the light pattern and luminous angle for reference and tunnel junction LEDS were similar to each other.

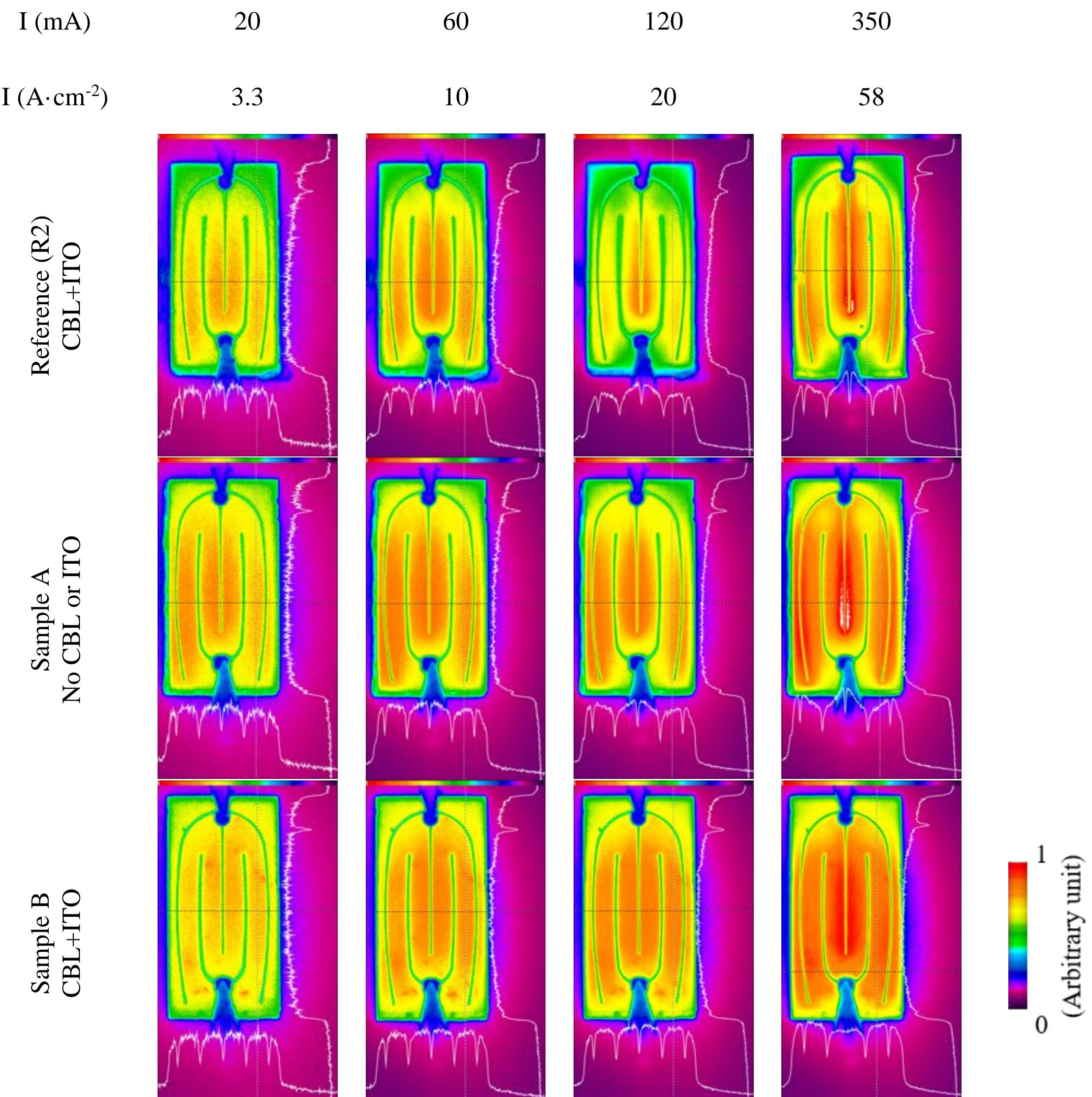


Figure 2.8 Charge coupled device (CCD) images of a LED from the three wafers at various current density. The white lines show the light intensity as a function of lateral or vertical position. The tunnel junction LEDs have more uniform light output than reference LEDs. (The same scale was used for all images.)

2.1.4 Discussion

The low excess voltage of 0.23-0.30 V achieved in this study is essential since it shows that using TJ doesn't necessarily compromise the efficiency. The fact that similar low ΔVF can be

achieved in both university and industry settings suggest TJ technique is transferable and can be used for both research and commercial devices. Although the use of MBE is limited in III-nitride device industrial production, RPCVD and sputtering deposition, which are suitable for large-scale production, has been shown to achieve active buried p-type layers as well [67,68]. We speculate that similar results can be achieved using these techniques if proper doping profile and surface cleaning procedure were used.

The TJ LEDs processed by industry procedures had a slightly higher excess voltage. We speculate that this can be improved by the use of Si delta doping. In this study, the voltage penalty reduction is associated with sharp doping profiles at the junction interface, high doping levels in n++ region, and surface cleaning procedure used before regrowth. Other works have shown that the use of InGaN in the GaN tunnel junction can also reduce voltage penalty [5,12,42–45].

The resistivity and voltage characteristics achieved for this study (the forward voltage V_F = 3.10 V for TJ LEDs, with the excess voltage ΔV_F = 0.23-0.30 V at 20 A/cm^2, ΔV_F = 0.35 V at 100 A/cm^2) was compared to the results in literature. Some of the lowest forward voltage achieved for GaN tunnel homojunction are: ΔV_F = 0.2-0.3 V at 20 A/cm^2 for micro-LEDs grown by MOCVD utilizing SAG [62]; V_F = 3.08 V at 20 A/cm^2 for blue TJ LED grown by similar hybrid growth approach [9]. For InGaN-containing tunnel junction, some of the lowest forward voltage reported are: V_F = 3.775 V for hybrid TJ LED using $In_{0.23}Ga_{0.77}N$ interlayer compared to 3.9 V for ITO LED [5]; V_F = 3.12 V for hybrid TJ LED using $In_{0.12}Ga_{0.88}N$ interlayer compared to 3.37 V for ITO LED [45]. Thus, we consider the results in this study is comparable to the lowest resistivity and voltage characteristics reported for both GaN and InGaN-containing tunnel junctions LEDs.

The light output power of TJ samples processed with CBL and ITO (sample B) is higher than the one processed without them (sample A). This suggest that a proper light extraction design for TJ LEDs would include a CBL below the metal contact to avoid optical absorption by the contact pad. ITO or other transparent conducting materials can be used to assist the contact between the top n-GaN and metal contact in the presence of the CBL as in sample B. However, having the ITO layer covering most of the surface is unnecessary because the n-GaN layer in TJ can already spread current and is more transparent than ITO [72]. Thus, the conductive layer only needs to cover the area around the metal contacts. Example of this proposed light extraction structure is shown in Figure 2.9. The contact stack should be properly optimized to ensure low resistivity and avoid extra voltage loss.

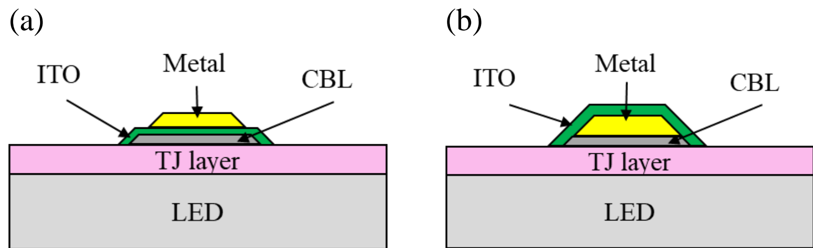


Figure 2.9 Examples of proposed light extraction structure for TJ LEDs. (a). The conductive layer (ITO) is between metal contact and CBL. (b). The conductive layer (ITO) is above the metal contact.

The use of tunnel junctions allows for common contact metallization. This reduces the number of processing steps and manufacturing cost. In flip chip LEDs, TJ also allows for the replacement of the Ag-based mirror with a higher reflectivity omnidirectional dielectric reflector [9]. This increases the LED efficiency and improves the yield by helping to circumvent the adhesion and tarnishing issues associated with Ag-based mirrors [9]. Blue LEDs was used in this study to achieve a robust evaluation of the TJ's excess voltage. However, the benefits of using TJ is more significant in more complicated devices such as flip-chip LEDs,

laser diodes, UV devices, and cascade LEDs where the improvements in devices performance by using TJs outweighs the cost of making TJs and the effect of having excess voltage. With both low voltage penalty and improved light extraction structure, TJ devices have huge potential in both academic and commercial applications.

2.4.5 Conclusion

We have demonstrated low excess voltage GaN tunnel junction LEDs using both academic and industrial processing and testing techinques. Hybrid tunnel junctions were grown on commercial MOCVD blue LED wafers by NH_3-assisted MBE. Using an academic process, the voltage penalty at 20 $A \cdot cm^{-2}$ was as low as 0.23 V. δ-doping of silicon at the junction interface was shown to reduce the voltage penalty. APT and SIMS measurements indicate that a BHF clean at the regrowth interface can reduce Mg diffusion into the n++ layer and reduce the amount of C, H, and O incorporation at the regrowth interface. Using industrial process, for tunnel junction LED processed without ITO or CBL, the excess voltage is as low as 0.3V. Tunnel junction LEDs processed with ITO and CBL have similar light output compared to conventional ITO LEDs. Tunnel junction LEDs also have more uniform intensity than ITO LEDs. With improved light extraction structure, TJ LEDs could have similar efficiency compared to ITO LEDs. RPCVD and sputtering deposition are techniques widely available in industry production of III-nitride devices [67,68]. If similar approach is followed, they are expected to achieve similar result as the MBE used in this study. The results presented here respond to the concern about using TJs in commercial devices by showing that TJs don't necessarily compromise the device efficiency. Although further optimization may be required, with the other benefits such as simplicity of manufacturing and allowing for the replacement

of Ag mirror in flip-chip devices [9], TJ LEDs and laser devices are viable for commercialization.

2.2. Hybrid growth technique of tunnel junction on c-plane and m-plane

2.2.3 p-GaN activation

The energy barrier for hydrogen diffusion in n-GaN is high [73], preventing the dissociation of Mg-H complexes when the p-GaN layer is buried. Thus, when doing MBE n-type TJ regrowth on MOCVD grown devices with p-GaN layers, it is important to activate the p-GaN before the n++GaN growth start.

This can be done in two ways: 1. Activate the sample in air, N_2, or in situ in the MOCVD reactor. The same approach the LED is usually activated without TJ regrowth experiment; 2. Activate the sample in MBE. Baking the sample at an elevated temperature in the main chamber without ammonia flow can activate the sample. This is equivalent to activating a sample in vacuum. Even without doing an intentional activation step, the 1 hr 400 °C bake in vacuum plus the ~15 min temperature ramp up step in the main chamber will partially activate the sample. Although some NH_3 (≤200 sccm in most cases) is flowing during the ramp up stage, the equivalent pressure is low enough to prevent re-passivation of the p-GaN and allow the Mg-H complex to dissociate.

2.2.4 Sample cleaning

The optimal sample cleaning procedure is based on the crystal orientation. For c-plane devices, ample cleaning, including 49% HF dip, BHF dip, 15 min HCl dip, and aqua regia cleaning reduces the forward voltage [9]. The samples were vacuum sealed using vacuum level of 99%, gas flow of 1.0, a sealing factor of 2.5. Samples were taken out from the bag right before transferring into the MBE. For semi-polar devices, such cleaning can potentially increase the voltage [6]. A solvent clean is usually chosen to clean the sample.

2.2.5 NH_3 annealing before growth

An NH_3 annealing step usually act as an approach for surface cleaning. However, this step has opposite effect on the forward voltage of samples grown on different orientations. It was shown that for semi-polar devices, NH_3 annealing increases the forward voltage [6]. Thus, during the temperature ramp up step for TJ regrowth on semi-polar device, a NH_3 flow of 100 sccm or 50 sccm is usually used compared to 200 sccm which is the standard NH_3 flow rate during temperature ramp up from 400 °C to the target temperature. The growth was also start quickly to minimize the NH_3 exposure. For c-plane devices, NH_3 anneal help reduce the voltage within a limited range.

2.2.6 n-TJ regrowth by MBE

To do regrowth on multiple samples at the sample time, indium bonding is often used to co-load samples on to the same Si wafer. The indium also facilitates the temperature reading and the heat spreading on the backside of the sample. Usually, we can assume the co-bonded samples are at the same temperature.

The indium bonding evaporates at elevated temperature. Thus, the growth temperature and growth time is limited. Increased NH_3 (for example, during InGaN growth) also etches away the indium metal. Titanium coating on sample backside will alleviate this issue but not solve it entirely. An example for a growth with indium bonding is at 750 °C, with a NH_3 flow rate of 200 sccm or 500 sccm for a short period of time, and the growth time is < 1.5 hr.

Figure 2.10 Examples of samples with and without titanium backside coating grown with indium bonding. The indium and titanium on the sample backside partially evaporated during growth.

At the initial stage of growth, the RHEED electrons will cause electroluminescence to happen on the LEDs as shown in Figure 11.

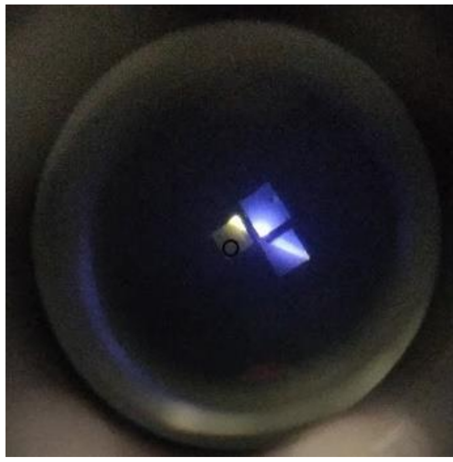


Figure 2.11 LED samples showing emission under RHEED at the initial stage of growth. The blue samples were LEDs. The yellow sample was GaN on sapphire template.

The high doping levels in n++ layer (doped with Si) usually causes pits on the sample surface. The morphology is also dependent on the crystal orientation. Figure 2.12 shows AFM image for a m-plan TJ sample. Note the morphology is streaky rather than mound-like as in typical c-plane regrowth.

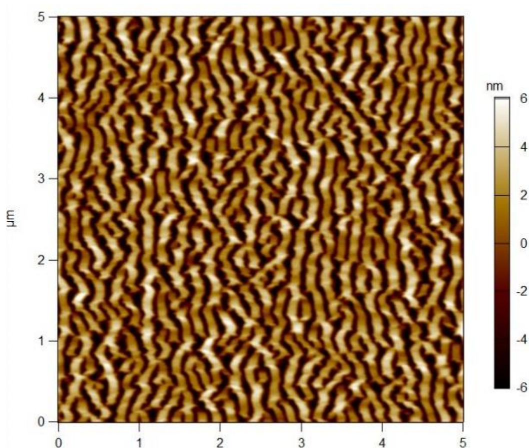


Figure 2.12 AFM image of TJ sample grown on m-plane. The rms roughness is 3 nm.

References

1. L. Esaki, "New Phenomenon in Narrow Germanium p-n Junctions," Physical Review **109**, 603–604 (1958).
2. T. Margalith, O. Buchinsky, D. A. Cohen, A. C. Abare, M. Hansen, S. P. DenBaars, and L. A. Coldren, "Indium tin oxide contacts to gallium nitride optoelectronic devices," Appl. Phys. Lett. **74**, 3930–3932 (1999).
3. B. P. Yonkee, E. C. Young, C. Lee, J. T. Leonard, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Demonstration of a III-nitride edge-emitting laser diode utilizing a GaN tunnel junction contact," Opt. Express, OE **24**, 7816–7822 (2016).
4. M. Malinverni, D. Martin, and N. Grandjean, "InGaN based micro light emitting diodes featuring a buried GaN tunnel junction," Appl. Phys. Lett. **107**, 051107 (2015).
5. S. Krishnamoorthy, F. Akyol, and S. Rajan, "InGaN/GaN tunnel junctions for hole injection in GaN light emitting diodes," Appl. Phys. Lett. **105**, 141104 (2014).
6. E. C. Young, B. P. Yonkee, F. Wu, S. H. Oh, S. P. DenBaars, S. Nakamura, and J. S. Speck, "Hybrid tunnel junction contacts to III–nitride light-emitting diodes," Appl. Phys. Express **9**, 022102 (2016).
7. S.-R. Jeon, Y.-H. Song, H.-J. Jang, G. M. Yang, S. W. Hwang, and S. J. Son, "Lateral current spreading in GaN-based light-emitting diodes utilizing tunnel contact junctions," Appl. Phys. Lett. **78**, 3265–3267 (2001).
8. Y. Kuwano, M. Kaga, T. Morita, K. Yamashita, K. Yagi, M. Iwaya, T. Takeuchi, S. Kamiyama, and I. Akasaki, "Lateral Hydrogen Diffusion at p-GaN Layers in Nitride-Based Light Emitting Diodes with Tunnel Junctions," Jpn. J. Appl. Phys. **52**, 08JK12 (2013).
9. B. P. Yonkee, E. C. Young, S. P. DenBaars, S. Nakamura, and J. S. Speck, "Silver free III-nitride flip chip light-emitting-diode with wall plug efficiency over 70% utilizing a GaN tunnel junction," Appl. Phys. Lett. **109**, 191104 (2016).
10. B. Saifaddin, A. Almogbel, M. Iza, A. Albadri, A. Al Yamani, S. Nakamura, C. J. Zollner, H. M. Foronda, F. Wu, J. S. Speck, and S. P. DenBaars, "Developments in AlGaN and UV-C LEDs grown on SiC," in *Light-Emitting Diodes: Materials, Devices,*

and Applications for Solid State Lighting XXII, L.-W. Tu, M. Strassburg, J. K. Kim, and M. R. Krames, eds. (SPIE, 2018), p. 64.

11. T. Takeuchi, G. Hasnain, S. Corzine, M. Hueschen, J. Richard P. Schneider, C. Kocot, M. Blomqvist, Y. Chang, D. Lefforge, M. R. Krames, L. W. Cook, and S. A. Stockman, "GaN-Based Light Emitting Diodes with Tunnel Junctions," Jpn. J. Appl. Phys. **40**, L861 (2001).
12. S. Krishnamoorthy, F. Akyol, P. S. Park, and S. Rajan, "Low resistance GaN/InGaN/GaN tunnel junctions," Appl. Phys. Lett. **102**, 113503 (2013).
13. Z.-H. Zhang, S. Tiam Tan, Z. Kyaw, Y. Ji, W. Liu, Z. Ju, N. Hasanov, X. Wei Sun, and H. Volkan Demir, "InGaN/GaN light-emitting diode with a polarization tunnel junction," Appl. Phys. Lett. **102**, 193508 (2013).
14. Y. Zhang, S. Krishnamoorthy, F. Akyol, S. Bajaj, A. A. Allerman, M. W. Moseley, A. M. Armstrong, and S. Rajan, "Tunnel-injected sub-260 nm ultraviolet light emitting diodes," Applied Physics Letters **110**, 201102 (2017).
15. Y. Zhang, Z. Jamal-Eddine, F. Akyol, S. Bajaj, J. M. Johnson, G. Calderon, A. A. Allerman, M. W. Moseley, A. M. Armstrong, J. Hwang, and S. Rajan, "Tunnel-injected sub 290 nm ultra-violet light emitting diodes with 2.8% external quantum efficiency," Appl. Phys. Lett. **112**, 071107 (2018).
16. Y. Zhang, S. Krishnamoorthy, F. Akyol, A. A. Allerman, M. W. Moseley, A. M. Armstrong, and S. Rajan, "Design and demonstration of ultra-wide bandgap AlGaN tunnel junctions," Appl. Phys. Lett. **109**, 121102 (2016).
17. Y. Zhang, S. Krishnamoorthy, F. Akyol, S. Khandaker, A. Allerman, M. W. Moseley, A. Armstrong, and S. Rajan, "Sub 300 nm wavelength III-Nitride tunnel-injected ultraviolet LEDs," in *2015 73rd Annual Device Research Conference (DRC)* (2015), pp. 69–70.
18. J. Piprek, "Origin of InGaN/GaN light-emitting diode efficiency improvements using tunnel-junction-cascaded active regions," Appl. Phys. Lett. **104**, 051118 (2014).
19. S.-J. Chang, W.-H. Lin, and C.-T. Yu, "GaN-Based Multiquantum Well Light-Emitting Diodes with Tunnel-Junction-Cascaded Active Regions," IEEE Electron Device Letters **36**, 366–368 (2015).

20. F. Akyol, S. Krishnamoorthy, and S. Rajan, "Tunneling-based carrier regeneration in cascaded GaN light emitting diodes to overcome efficiency droop," Appl. Phys. Lett. **103**, 081107 (2013).
21. F. Akyol, S. Krishnamoorthy, Y. Zhang, and S. Rajan, "GaN-based three-junction cascaded light-emitting diode with low-resistance InGaN tunnel junctions," Appl. Phys. Express **8**, 082103 (2015).
22. S. J. Kowsz, E. C. Young, B. P. Yonkee, C. D. Pynn, R. M. Farrell, J. S. Speck, S. P. DenBaars, and S. Nakamura, "Using tunnel junctions to grow monolithically integrated optically pumped semipolar III-nitride yellow quantum wells on top of electrically injected blue quantum wells," Opt. Express, OE **25**, 3841–3849 (2017).
23. S. M. Sadaf, Y.-H. Ra, H. P. T. Nguyen, M. Djavid, and Z. Mi, "Alternating-Current InGaN/GaN Tunnel Junction Nanowire White-Light Emitting Diodes," https://pubs.acs.org/doi/abs/10.1021/acs.nanolett.5b02515.
24. M. Siekacz, G. Muziol, M. Hajdel, M. Żak, K. Nowakowski-Szkudlarek, H. Turski, M. Sawicka, P. Wolny, A. Feduniewicz-Żmuda, S. Stanczyk, J. Moneta, and C. Skierbiszewski, "Stack of two III-nitride laser diodes interconnected by a tunnel junction," Opt. Express, OE **27**, 5784–5791 (2019).
25. H. Kurokawa, M. Kaga, T. Goda, M. Iwaya, T. Takeuchi, S. Kamiyama, I. Akasaki, and H. Amano, "Multijunction GaInN-based solar cells using a tunnel junction," Appl. Phys. Express **7**, 034104 (2014).
26. X. Guo, G. D. Shen, B. L. Guan, X. L. Gu, D. Wu, and Y. B. Li, "Cascade single-chip phosphor-free white light-emitting diodes," Appl. Phys. Lett. **92**, 013507 (2008).
27. I. Ozden, E. Makarona, A. V. Nurmikko, T. Takeuchi, and M. Krames, "A dual-wavelength indium gallium nitride quantum well light emitting diode," Appl. Phys. Lett. **79**, 2532–2534 (2001).
28. M. L. Reed, E. D. Readinger, H. Shen, M. Wraback, A. Syrkin, A. Usikov, O. V. Kovalenkov, and V. A. Dmitriev, "n-InGaN∕p-GaN single heterostructure light emitting diode with p-side down," Appl. Phys. Lett. **93**, 133505 (2008).
29. S. Newman, C. Gallinat, J. Wright, R. Enck, A. Sampath, H. Shen, M. Reed, and M. Wraback, "Wavelength stable, p-side-down green light emitting diodes grown by

molecular beam epitaxy," Journal of Vacuum Science & Technology B **31**, 010601 (2012).

30. H. Turski, S. Bharadwaj, M. Siekacz, G. Muziol, M. Chlipala, M. Zak, M. Hajdel, K. Nowakowski-Szkudlarek, S. Stanczyk, H. Xing, D. Jena, and C. Skierbiszewski, "Monolithically p-down nitride laser diodes and LEDs obtained by MBE using buried tunnel junction design," in *Gallium Nitride Materials and Devices XV* (International Society for Optics and Photonics, 2020), Vol. 11280, p. 1128010.
31. S. Bharadwaj, S. Bharadwaj, J. Miller, K. Lee, J. Lederman, M. Siekacz, H. (Grace) Xing, H. (Grace) Xing, H. (Grace) Xing, D. Jena, D. Jena, D. Jena, C. Skierbiszewski, and H. Turski, "Enhanced injection efficiency and light output in bottom tunnel-junction light-emitting diodes," Opt. Express, OE **28**, 4489–4500 (2020).
32. J. T. Leonard, E. C. Young, B. P. Yonkee, D. A. Cohen, T. Margalith, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Demonstration of a III-nitride vertical-cavity surface-emitting laser with a III-nitride tunnel junction intracavity contact," Appl. Phys. Lett. **107**, 091105 (2015).
33. J. T. Leonard, E. C. Young, B. P. Yonkee, D. A. Cohen, C. Shen, T. Margalith, T. K. Ng, S. P. DenBaars, B. S. Ooi, J. S. Speck, and S. Nakamura, "Comparison of nonpolar III-nitride vertical-cavity surface-emitting lasers with tunnel junction and ITO intracavity contacts," in (International Society for Optics and Photonics, 2016), Vol. 9748, p. 97481B.
34. C. A. Forman, J. T. Leonard, E. C. Young, S. Lee, D. A. Cohen, B. P. Yonkee, R. M. Farrell, T. Margalith, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Nonpolar GaN-based vertical-cavity surface-emitting lasers," in *2016 International Semiconductor Laser Conference (ISLC)* (2016), pp. 1–2.
35. C. A. Forman, S. Lee, E. C. Young, J. A. Kearns, D. A. Cohen, J. T. Leonard, T. Margalith, S. P. DenBaars, and S. Nakamura, "Continuous-wave operation of nonpolar GaN-based vertical-cavity surface-emitting lasers," in *Gallium Nitride Materials and Devices XIII* (International Society for Optics and Photonics, 2018), Vol. 10532, p. 105321C.
36. C. A. Forman, S. Lee, E. C. Young, J. A. Kearns, D. A. Cohen, J. T. Leonard, T. Margalith, S. P. DenBaars, and S. Nakamura, "Continuous-wave operation of m-plane

GaN-based vertical-cavity surface-emitting lasers with a tunnel junction intracavity contact," Appl. Phys. Lett. **112**, 111106 (2018).

37. S. Lee, C. A. Forman, C. Lee, J. Kearns, E. C. Young, J. T. Leonard, D. A. Cohen, J. S. Speck, S. Nakamura, and S. P. DenBaars, "GaN-based vertical-cavity surface-emitting lasers with tunnel junction contacts grown by metal-organic chemical vapor deposition," Appl. Phys. Express **11**, 062703 (2018).
38. S.-R. Jeon, C. S. Oh, J.-W. Yang, G. M. Yang, and B.-S. Yoo, "GaN tunnel junction as a current aperture in a blue surface-emitting light-emitting diode," Appl. Phys. Lett. **80**, 1933–1935 (2002).
39. M. Kaga, T. Morita, Y. Kuwano, K. Yamashita, K. Yagi, M. Iwaya, T. Takeuchi, S. Kamiyama, and I. Akasaki, "GaInN-Based Tunnel Junctions in n–p–n Light Emitting Diodes," Jpn. J. Appl. Phys. **52**, 08JH06 (2013).
40. F. Akyol, S. Krishnamoorthy, Y. Zhang, J. Johnson, J. Hwang, and S. Rajan, "Low-resistance GaN tunnel homojunctions with 150 kA/cm2 current and repeatable negative differential resistance," Appl. Phys. Lett. **108**, 131103 (2016).
41. J. Verma, S. M. Islam, V. Protasenko, P. Kumar Kandaswamy, H. (Grace) Xing, and D. Jena, "Tunnel-injection quantum dot deep-ultraviolet light-emitting diodes with polarization-induced doping in III-nitride heterostructures," Appl. Phys. Lett. **104**, 021105 (2014).
42. S. Krishnamoorthy, P. S. Park, and S. Rajan, "Demonstration of forward inter-band tunneling in GaN by polarization engineering," Appl. Phys. Lett. **99**, 233504 (2011).
43. X. Yan, W. Li, S. M. Islam, K. Pourang, H. (Grace) Xing, P. Fay, and D. Jena, "Polarization-induced Zener tunnel diodes in GaN/InGaN/GaN heterojunctions," Appl. Phys. Lett. **107**, 163504 (2015).
44. S. Krishnamoorthy, D. N. Nath, F. Akyol, P. S. Park, M. Esposto, and S. Rajan, "Polarization-engineered GaN/InGaN/GaN tunnel diodes," Appl. Phys. Lett. **97**, 203502 (2010).
45. A. J. Mughal, E. C. Young, A. I. Alhassan, J. Back, S. Nakamura, J. S. Speck, and S. P. DenBaars, "Polarization-enhanced InGaN/GaN-based hybrid tunnel junction contacts to GaN p–n diodes and InGaN LEDs," Appl. Phys. Express **10**, 121006 (2017).

46. M. Singh, Y. Zhang, J. Singh, and U. Mishra, "Examination of tunnel junctions in the AlGaN/GaN system: Consequences of polarization charge," Appl. Phys. Lett. **77**, 1867–1869 (2000).
47. M. J. Grundmann and U. K. Mishra, "Multi-color light emitting diode using polarization-induced tunnel junctions," physica status solidi c **4**, 2830–2833 (2007).
48. J. Simon, Z. Zhang, K. Goodman, T. Kosel, P. Fay, and D. Jena, "Polarization-induced zener tunnel junctions in wide-bandgap heterostructures," in *2009 Device Research Conference* (2009), pp. 101–102.
49. M. F. Schubert, "Interband tunnel junctions for wurtzite III-nitride semiconductors based on heterointerface polarization charges," Phys. Rev. B **81**, 035303 (2010).
50. C. Kuhn, L. Sulmoni, M. Guttmann, J. Glaab, N. Susilo, T. Wernicke, M. Weyers, and M. Kneissl, "MOVPE-grown AlGaN-based tunnel heterojunctions enabling fully transparent UVC LEDs," Photon. Res., PRJ **7**, B7–B11 (2019).
51. A. Pandey, W. J. Shin, J. Gim, R. Hovden, and Z. Mi, "High-efficiency AlGaN/GaN/AlGaN tunnel junction ultraviolet light-emitting diodes," Photon. Res., PRJ **8**, 331–337 (2020).
52. S. Krishnamoorthy, T. F. Kent, J. Yang, P. S. Park, R. C. Myers, and S. Rajan, "GdN Nanoisland-Based GaN Tunnel Junctions," Nano Lett. **13**, 2570–2575 (2013).
53. J. Neugebauer and C. G. Van de Walle, "Role of hydrogen in doping of GaN," Appl. Phys. Lett. **68**, 1829–1831 (1996).
54. J. Neugebauer and C. G. Van de Walle, "Hydrogen in GaN: Novel Aspects of a Common Impurity," Phys. Rev. Lett. **75**, 4452–4455 (1995).
55. S. Nakamura, T. Mukai, M. Senoh, and N. Iwasa, "Thermal Annealing Effects on P-Type Mg-Doped GaN Films," Jpn. J. Appl. Phys. **31**, L139 (1992).
56. V. Fan Arcara, B. Damilano, G. Feuillet, A. Courville, S. Chenot, and J.-Y. Duboz, "(Ga,In)N/GaN light emitting diodes with a tunnel junction and a rough n-contact layer grown by metalorganic chemical vapor deposition," AIP Advances **9**, 055101 (2019).
57. P. Sohi, M. Mosca, Y. Chen, J.-F. Carlin, and N. Grandjean, "Low-temperature growth of n $\mathplus$$\mathplus$-GaN by metalorganic chemical vapor deposition to achieve low-resistivity tunnel junctions on blue light emitting diodes," Semicond. Sci. Technol. **34**, 015002 (2018).

58. D. Minamikawa, M. Ino, S. Kawai, T. Takeuchi, S. Kamiyama, M. Iwaya, and I. Akasaki, "GaInN-based tunnel junctions with high InN mole fractions grown by MOVPE," physica status solidi (b) **252**, 1127–1131 (2015).
59. D. Hwang, A. J. Mughal, M. S. Wong, A. I. Alhassan, S. Nakamura, and S. P. DenBaars, "Micro-light-emitting diodes with III–nitride tunnel junction contacts grown by metalorganic chemical vapor deposition," Appl. Phys. Express **11**, 012102 (2017).
60. W. Li, K. Nomoto, K. Lee, S. M. Islam, Z. Hu, M. Zhu, X. Gao, J. Xie, M. Pilla, D. Jena, and H. G. Xing, "Activation of buried p-GaN in MOCVD-regrown vertical structures," Appl. Phys. Lett. **113**, 062105 (2018).
61. A.I. Alhassan, C. Lynsky, A. Alyamani, S. Nakamura, and S.P. Denbaars, "Realization of MOCVD GaN Tunnel Junction Contacts in Large Area LEDs" in Proceedings of 2018 Compd. Semicond. Week CSW Incl. 30th Int. Conf. Indium Phosphide Relat. Mater. IPRM 45rd Int. Symp. Compd. Semicond. ISCS (2016), pp. 102-103.62.
62. P. Li, H. Zhang, H. Li, M. Iza, Y. Yao, M. S. Wong, N. Palmquist, J. S. Speck, S. Nakamura, S. Nakamura, S. P. DenBaars, and S. P. DenBaars, "Size-independent low voltage of InGaN micro-light-emitting diodes with epitaxial tunnel junctions using selective area growth by metalorganic chemical vapor deposition," Opt. Express, OE **28**, 18707–18712 (2020).62.
63. I. P. Smorchkova, E. Haus, B. Heying, P. Kozodoy, P. Fini, J. P. Ibbetson, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Mg doping of GaN layers grown by plasma-assisted molecular-beam epitaxy," Appl. Phys. Lett. **76**, 718–720 (2000).
64. B. P. Yonkee, E. C. Young, J. T. Leonard, C. Lee, S. H. Oh, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Hybrid MOCVD/MBE GaN tunnel junction LEDs with greater than 70% wall plug efficiency," in *2016 Compound Semiconductor Week (CSW) [Includes 28th International Conference on Indium Phosphide Related Materials (IPRM) 43rd International Symposium on Compound Semiconductors (ISCS)* (2016), pp. 1–1.
65. A. I. Alhassan, E. C. Young, A. Y. Alyamani, A. Albadri, S. Nakamura, S. P. DenBaars, and J. S. Speck, "Reduced-droop green III–nitride light-emitting diodes utilizing GaN tunnel junction," Appl. Phys. Express **11**, 042101 (2018).

66. K. W. Hamdy, E. C. Young, A. I. Alhassan, D. L. Becerra, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Efficient tunnel junction contacts for high-power semipolar III-nitride edge-emitting laser diodes," Opt. Express, OE **27**, 8327–8334 (2019).
67. I. Wildeson, P. Deb, E. C. Nelson, and J. Kobayashi, "Methods for using remote plasma chemical vapor deposition (RP-CVD) and sputtering deposition to grow layers in light emitting devices," United States patent US10236409B2 (March 19, 2019).
68. I. Mann, S. Barik, J. D. BROWN, and D. Liu, "Buried activated p-(Al,In)GaN layers," United States patent US10355165B2 (July 16, 2019).
69. E. D. Russo, A. Mavel, V. F. Arcara, B. Damilano, I. Dimkou, S. Vézian, A. Grenier, M. Veillerot, N. Rochat, G. Feuillet, B. Bonef, L. Rigutti, J.-Y. Duboz, E. Monroy, and D. Cooper, "Multi-microscopy nanoscale characterization of the doping profile in a hybrid Mg/Ge-doped tunnel junction.," Nanotechnology (2020).
70. J. K. Sheu, Y. K. Su, G. C. Chi, M. J. Jou, and C. M. Chang, "Effects of thermal annealing on the indium tin oxide Schottky contacts of n-GaN," Appl. Phys. Lett. **72**, 3317–3319 (1998).
71. J. D. Hwang, G. H. Yang, W. T. Chang, C. C. Lin, R. W. Chuang, and S. J. Chang, "A novel transparent ohmic contact of indium tin oxide to n-type GaN," Microelectronic Engineering **77**, 71–75 (2005).
72. T. Minami, H. Sonohara, T. Kakumu, and S. Takata, "Physics of very thin ITO conducting films with high transparency prepared by DC magnetron sputtering," Thin Solid Films **270**, 37–42 (1995).
73. W. Götz, N. M. Johnson, J. Walker, D. P. Bour, H. Amano, and I. Akasaki, "Hydrogen passivation of Mg acceptors in GaN grown by metalorganic chemical vapor deposition," Appl. Phys. Lett. **67**, 2666–2668 (1995).

Chapter 3 Highly doped n-AlGaN with low resistivity for UV TJ LEDs

3.1 Introduction

AlGaN alloys have a wide range of applications in optical and electronic devices due to their attractive physical properties such as tunable wide bandgap, strong piezoelectricity, and a high breakdown field. Recently, deep ultraviolet (UVC) LEDs based on AlGaN materials have attracted significant interest for its disinfection applications such as water purification [1–4] and sterilization of critical care patient rooms [5,6].

Realizing highly conductive n-AlGaN with controlled doping is essential to achieve high performance devices. UV LEDs, for example, can benefit from the use of n-AlGaN based tunnel junctions (TJs) [7]. This is because the efficiency of UV LEDs is limited by the light extraction efficiency which is usually below 30% [8–17]. TJs can potentially increase the LEE by two times by enabling the use of highly reflective MgF_2-based mirrors in thin-film flip-chip UVC LEDs [18–22] and eliminating the need to use absorptive p-GaN [23,24]. TJs also facilitate current spreading and hole injection in UV LEDs [7,16,25].

Si-doped AlGaN has higher resistivity than GaN:Si due to several reasons. First, the dopant ionization energy of Si dopant in AlGaN is higher than in GaN and increases with increased AlN content [24,26–36]. The ionization energy of Si in $Al_xGa_{1-x}N$ increases from ~15 meV for x = 0 to 60-280 meV for x=1, with a value for 25-30 meV for x = 0.65. Second, Si also shows self-compensation at high doping level for $Al_xGa_{1-x}N$ with x > 0.5, leading to reduced electron concentration and increased resistivity as Si doping level increases (also known as the "knee behavior") [24,26,28–30,37–41]. This means that the carrier concentration increases with increased Si concentration at low doping region but lowers with increased Si concentration at high doping region. At high Al composition, compensating occurs, either through DX center formation for the Si dopants [24,30,41–52] or through V_{III}-associated complexes [28–30,51,53–58,58–64] .

Most of the studies of Si-doped AlGaN are done by metal organic chemical vapor deposition (MOCVD) [26–29,32,37,38,46,54,65–72], with some studies by plasma-assisted molecular beam epitaxy (MBE) [24,30,33,42–44] and few studies by NH_3-assisted MBE (NH_3 MBE) [31,39]. NH_3 MBE has several advantages such as being able to grow n-GaN with excellent transport properties [73], incorporating high levels of Si in n-GaN [74], and achieving a wide range of high-performance TJ devices [75–79]. It is thus of our interest to investigate Si-doping of AlGaN by NH_3 MBE.

In this study, we investigated n-type doping of $Al_xGa_{1-x}N$ by Si with Al fraction (x) around 60% by NH_3 MBE. This Al composition was of interest to this study since little absorption of UVC wavelength occurs at this composition [24]. Besides, the maximum carrier concentration can be achieved decreases with increased Al% [24,26,28,30,32,37,43,44,54,65,67]. The relationship between n-AlGaN quality and growth parameters including growth rate and Si cell

temperature was investigated. Low n-AlGaN contact resistance and a demonstration of UVC TJ LEDs (around 275 nm), grown with the optimized n-AlGaN condition were also discussed.

3.2 Experimental

The templates used for this study were AlN grown by MOCVD on Si-face c-plane 6H-silicon carbide (SiC) substrates. The templates were provided by Chris Zollner. The templates were crack free, with a threading dislocation density (TDD) around 8×10^8 /cm^3. Details on the low TDD AlN growth can be found elsewhere [80,81]. Before growth, the templates were coated with 500 nm of Ti on the back side by e-beam evaporation to assist the heat spreading and pyrometer temperature reading. Later, they were diced in to 1 cm × 1 cm squares, solvent-cleaned, and indium-bonded on to silicon wafers to transfer into the MBE. The samples were baked for 1 hour at 400 °C in vacuum before growth. The growth was done by Veeco 930 NH_3-assisted MBE with NH_3 as the group V source and solid effusion cells for Al, Ga, and Si. Beam flux measurements were done for the group III elements using ion gauge when the system is NH_3 free. Temperature was monitored using a pyrometer calibrated using the melting point of Al. The sample morphology was monitored in real time using reflection high-energy electron diffraction (RHEED). The growth was done around 780 °C with a NH_3 flow of 200 sccm. The group III fluxes were adjusted to get a growth rate of 109-426 nm/hr and an Al content around 60%. The doping level were controlled by growth parameters including the Si cell temperature.

The composition and relaxation of the AlGaN films were evaluated using reciprocal space mapping (RSM) of the $(10\bar{1}5)$ peak separation between the AlGaN film and the SiC substrate. The scan was done in an asymmetric scattering geometry using a high-resolution XRD with a

2D array detector. The analysis assumed Vegard's law for the AlGaN lattice and elastic constants. The thickness of the AlGaN films was determined by the spacing of fringes of the on-axis ω-2θ (0002) scan. Optical microscopy, atomic force microscopy (AFM), and scanning electron microscope (SEM) were used to characterize the morphology of samples. Atom probe tomography (APT) done by Dr. Bastien Bonef with a Cameca local electrode atom probe (LEAP) 3000X HR was used to evaluate the three-dimensional distribution of Al and Ga atoms and the alloy distribution.

The n-type doping of the AlGaN samples were evaluated by room temperature Hall measurements in a Van der Pauw geometry. The AlN on SiC templates underneath the n-AlGaN layer were confirmed to be insulating. The Si doping level, as well as the C, H, and O impurity levels were measured by Cameca IMS 7f Auto secondary ion mass microscopy (SIMS). The morphology of n-AlGaN was evaluated by atomic force microscopy (AFM). Contacts to the n-AlGaN were made using 10/150/20/300 nm of V/Al/V/Au metal stack. The sample was annealed in N_2 at 720 °C for 30 s to achieve an Ohmic contact. Circular transmission line measurement (CTLM) were done on the n-AlGaN with the annealed contact to get the contact resistance.

Finally, the optimized n-AlGaN condition was used to form a UVC hybrid tunnel junction (TJ) LED. MOCVD grown UVC LED with 0.5 nm p-GaN was patterned with SiO_2 to allow selective area growth of MBE n-$Al_{0.59}Ga_{0.41}N$ on top of the 0.5 nm MOCVD-grown p-GaN and n-AlGaN region as shown in Figure 3.1 (a). Only 0.5 nm of p-GaN was used to minimize the absorption by GaN. Figure 3.1 (b) shows the schematic of the TJ UV LED epitaxial structure. The lower 4 nm n++ layer forms the n-side of the TJ and was grown with high Si cell temperature (1450 °C) to achieve high donor concentration N_D. The 500 nm n^+ layer was

grown with the optimized condition for highest n-type carrier concentration and lowest resistivity to provide current spreading while maintaining low resistivity. The Si cell temperature was 1425 °C. The upper 4 nm n^{++} layer serves as the contact layer and was grown with the same condition as the lower n^{++} layer. The growth rate used for the regrowth was 426 nm/hr. The sample was processed into thin film flip-chip (TFFC) LEDs using the vanadium-based contact as both n and p-side contact. Details of the MOCVD epitaxial structure and the TFFC UV LED fabrication techniques can be found elsewhere [19,82,83]. The IV characteristics and electroluminescence (EL) spectrum of the TJ UV LED was measured with an ocean optics spectrometer and the IV compared with the reference UV LEDs without the TJ regrowth.

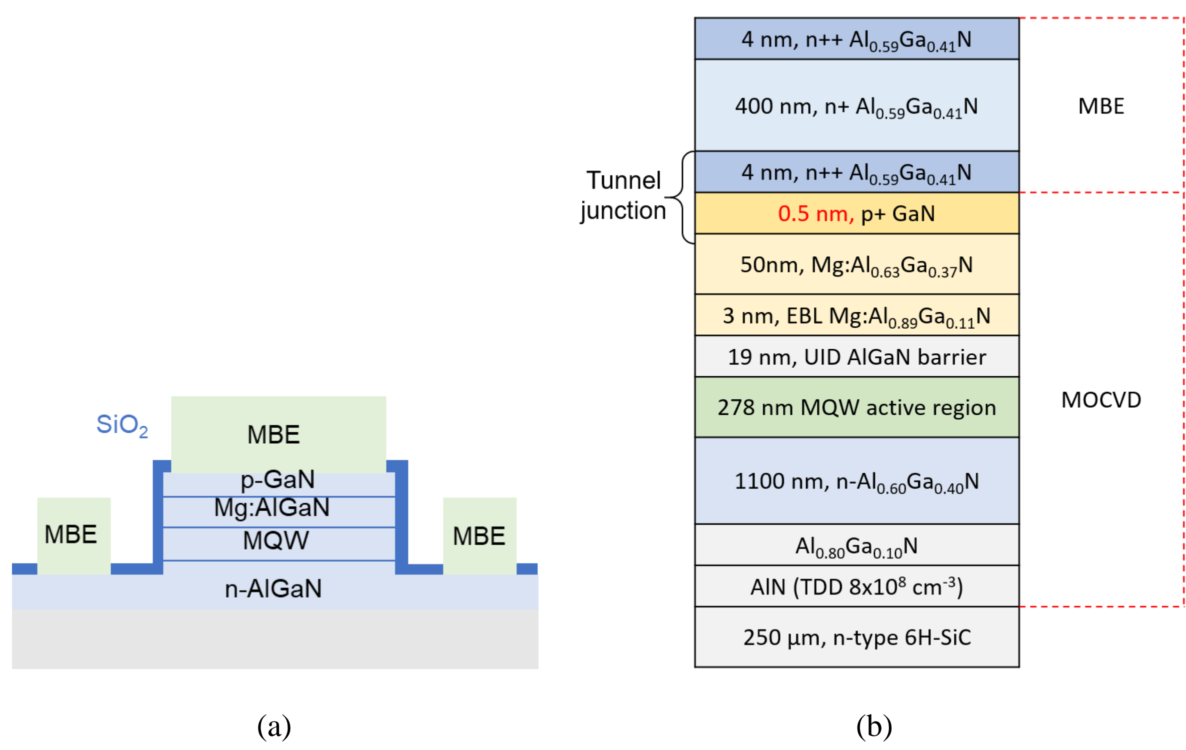
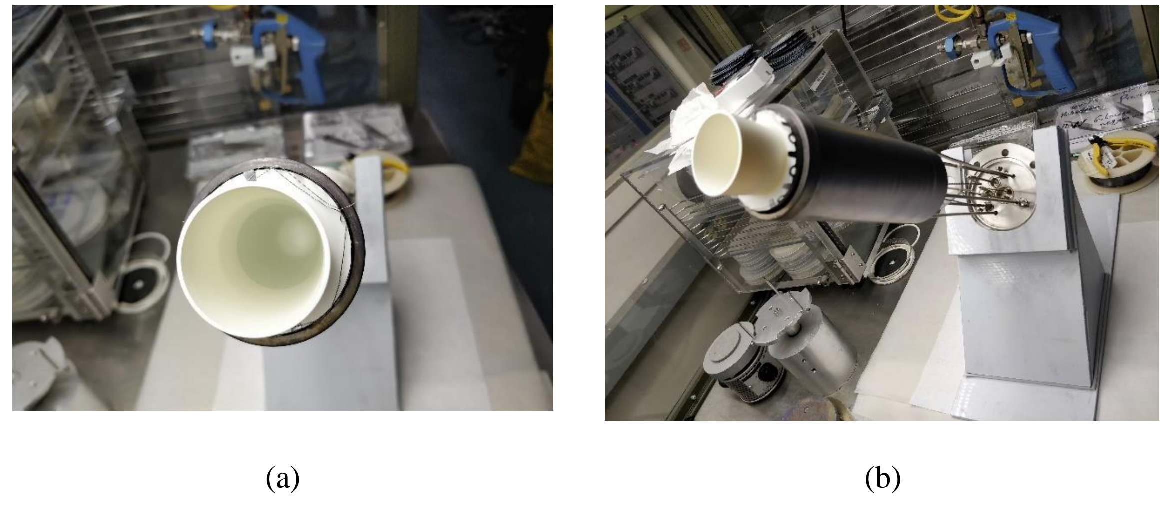


Figure 3.1 (a). MBE n-AlGaN regrowth was done on the on top of the p-GaN and n-AlGaN region of the MOCVD grown UVC LED sample to form hybrid TJ UVC LED. Figure courtesy Dr. Burhan SaifAddin. (b). Schematic of the UVC tunnel junction (TJ) LED epitaxial structure.

3.3 Results

3.3.1 Epitaxial growth of AlGaN

There were two Al effusion cells used in this experiment. One Al cell has big opening and long sleeve at the crucible opening to prevent Al creep out of the crucible and thus damage the cell. The second cell has narrow opening and narrow neck to prevent cell damage. It is generally easier to use the latter one since the smaller opening ensure that the cell opening can be fully covered by the shutter, and the Al flux is fully blocked when the shutter is closed. The former one not only have a bigger opening that is hard to cover 100%, it also had longer cell length, making it necessary to use a spacer with correct thickness.



(a) (b)

Figure 3.2 (a) Front view and (b) side view of an Al cell crucible.

Since Al is known to gather O and other type of impurities in epitaxial material, it is thus important to have low Al shutter leakage. A leaky Al shutter also causes undefined epitaxial layer boundaries. Figure 3.3 shows the SIMS measurement for Al shutter leakage check. Although there are still some Al incorporation in the GaN matrix when the shutter was close

and the Al cell was at 1150 °C, this level of incorporation ($<1\times10^{20}$ cm^{-3}) is negligible for most applications and no increased C, O, or H level was observed.

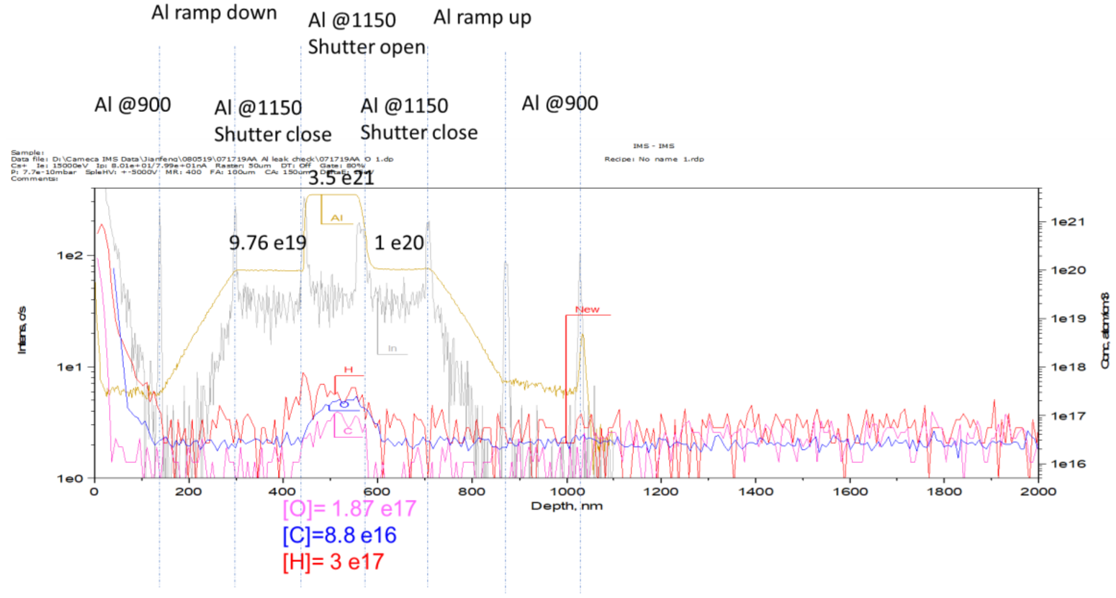


Figure 3.3 SIMS measurements of Al cell shutter leak check.

The use of Al cell also limits the maximum NH_3 flux one can use. High NH_3 flow rate increases the Al creep out of the cell and thus shorten cell life. Any growth using a flow rate above 200 sccm should be kept short.

The epitaxial growth of unintentionally doped (UID) AlGaN was carried out to map out the growth condition to achieve the desired crystal quality and alloy composition (~60%). Figure 3.4 (a) shows the SEM image of a sample with a 110 nm thick AlGaN layer, Al = 55.5%, and a growth rate of 218 nm/hr. The sample was crack free and no pits were observed. No cracks were observed for the grown UID AlGaN and n-AlGaN up to a thickness of 1 µm (the highest thickness investigated) as shown in the optical microscope (OM) image in Figure 3.4 (b). Figure 3.4 (c) shows the AFM image of MOCVD grown AlN on SiC template. The surface morphology was smooth with a root mean square (rsm) roughness of 0.3 nm. Figure 3.4 (d)

shows the AFM image of 100 nm $Al_xGa_{1-x}N$ layer grown by MBE on the template with x=65.5% and a growth rate of 216 nm/hr. Very few pits were observed on the sample surface. Note that the granular features in the AFM image of AlGaN are commonly observed in NH_3 MBE films. The rms roughness was 0.48 nm. The comparison of the sample's AFM images before and after the AlGaN growth suggested that the MBE growth did not degrade the morphology.

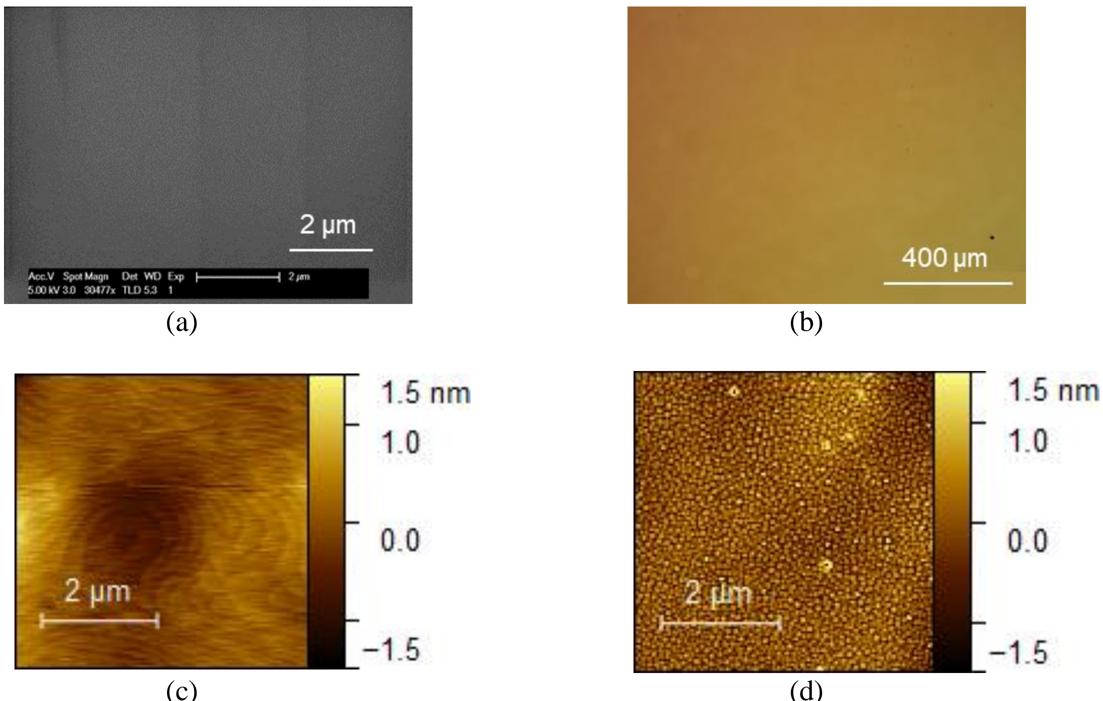


Figure 3.4 (a) SEM image of a crack-free AlGaN layer (110 nm), Al=55.5%, and a growth rate of 218 nm/hr. (b) Optical microscope image of a crack-free $Al_{0.59}Ga_{0.61}N$ layer (1 μm) grown at 210 nm/hr showing no cracks. (c) AFM image of the AlN on SiC template, which shows step flow growth. The rms roughness is 0.3 nm (d) AFM image of 100 nm AlGaN layer grown by MBE on the template with Al%=65.5% and a growth rate of 216 nm/hr. The surface was smooth and rms roughness is 0.48 nm.

Figure 3.5 (a) shows the ω-2θ scan of 100 nm $Al_{0.60}Ga_{0.40}N$ film grown at 218 nm/hr with clear thickness fringes. Figure 3.5 (b) shows an RSM scan of 400 nm $Al_{0.60}Ga_{0.40}N$ film grown with the same condition. The AlN layer is fully relaxed [80] while the AlGaN film for this

sample is coherent with the AlGaN layer as determined by the same Q_x values for the off axis $(10\bar{1}5)$ AlGaN (bottom) and AlN (top) peaks.

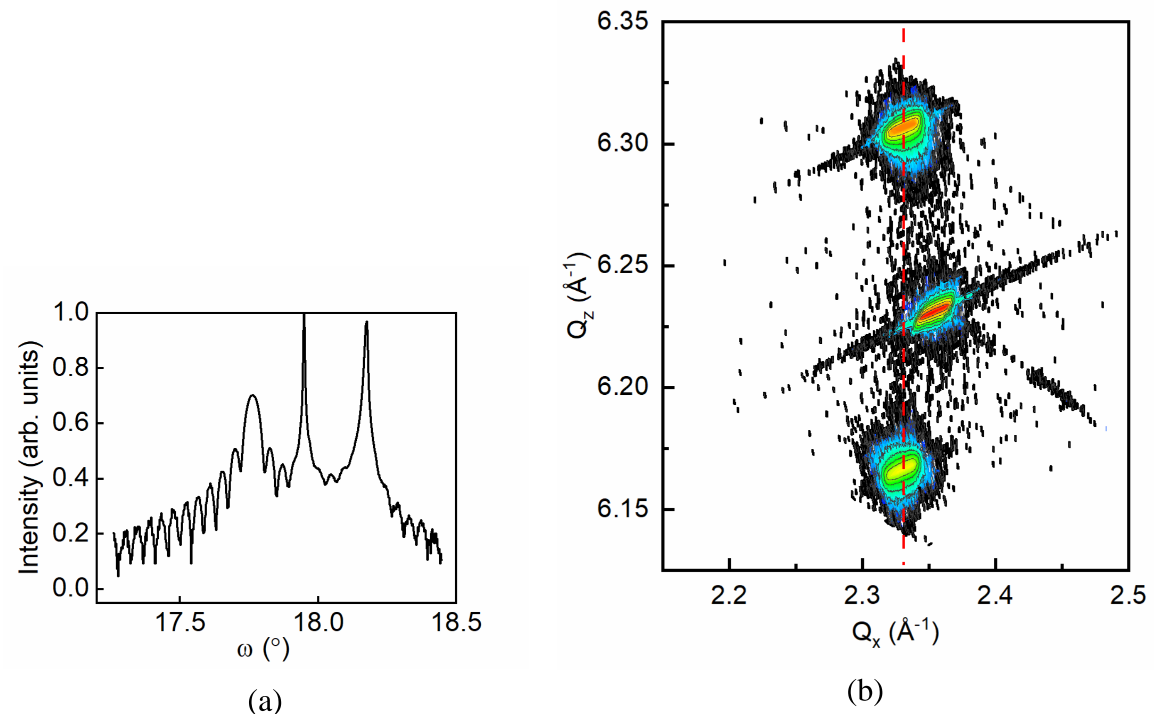


Figure 3.5 (a) ω-2θ scan of 100 nm $Al_{0.60}Ga_{0.40}N$ film grown at 218 nm/hr with clear thickness fringes. The spacings between the fringes were used to calculate the film thickness and growth rate. From left to right, the peaks are: AlGaN, SiC, and AlN peaks. (b) RSM scan of 400 nm fully strained $Al_{0.60}Ga_{0.40}N$ film grown at the same condition as in 3 (a). The separation between the SiC (in the middle) and the AlGaN peak (bottom) was used to calculate the Al% composition and relaxation ratio. The same Q_x between the AlN (top) and AlGaN peak shows that the AlGaN film is fully strained.

At fixed group III fluxes Φ_{III} (Φ_{Al}: 1.35×10^{-7} torr; Φ_{Ga}: 1.19×10^{-7} torr) and an NH_3 flow rate of 200 sccm, the growth temperature was varied in the range of 750-800 °C. Figure 3.6 shows that the Al% composition and growth rate were rather stable in this temperature range. The Al% changed within 3.5% and the growth rate varied within a 10% range.

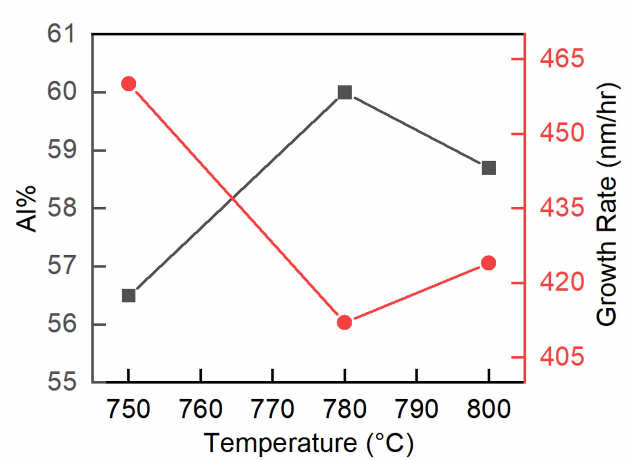


Figure 3.6 Alloy composition and growth rate dependence with the growth temperature.

The relationship between alloy composition and group III fluxes were also investigated. At a NH_3 flow rate of 200 sccm and a growth temperature of 800 °C, the Al flux Φ_{Al} was varied while keeping the Ga flux fixed at 6.08×10^{-8} torr. The measured Al% values are shown in Table 3.1. When the other growth parameters were kept the same, the Al content was determined by the group III fluxes. An incorporation factor (often referred to as a sticking coefficient) *s* was defined as:

$$s = \frac{N}{\Phi}$$

where N is the number of atoms incorporated into the AlGaN layer, and Φ was the supplied flux for this element. The Al% composition is thus determined by:

$$\text{Al\%} = \frac{N_{Al}}{N_{Al} + N_{Ga}}$$

$$= \frac{\Phi_{Al} \times s_{Al}}{\Phi_{Al} \times s_{Al} + \Phi_{Ga} \times s_{Ga}}$$

$$= \frac{\Phi_{Al} \times \mathrm{S}}{\Phi_{Al} \times \mathrm{S} + \Phi_{Ga}}$$

$$\text{where } S = \frac{s_{Al}}{s_{Ga}}$$

During grown calibration, we can get the value of S for a certain growth temperature from one calibration sample and use this value to predict the Al% composition for different Al and Ga fluxes when the change in group III flux were small. The calculated Al content value agrees well with the measured value for all samples investigated in this work. The value of S is above 1, suggesting that Al atoms more readily incorporated into the AlGaN film than the Ga atoms which is consistent with the higher Al-N bond energy (2.2 eV) compared to the Ga-N bond (1.93 eV) [84].

Table 3.1 The relationship between group III fluxes and Al%. $\boldsymbol{S} = \frac{s_{Al}}{s_{Ga}}$ is the ratio of incorporation factor between the two group III elements.

Al flux (torr)	Ga flux (torr)	Assumed S	Al% calculated	Al% measured
5.79×10^{-8}	6.08×10^{-8}	2.18	67.5%	67.5%
5.14×10^{-8}	6.08×10^{-8}	2.18	64.8%	64.5%
4.20×10^{-8}	6.08×10^{-8}	2.18	60.1%	59.8%

APT measurements of the AlGaN layer is shown in Figure 3.7. The Al% composition measured by APT is 59% and is in close agreement with the 58% Al composition calculated by XRD RSM scan. The Al% is constant in the growth direction for the thickness studied (60 nm). The alloy is random with no Al rich clusters observed [82].

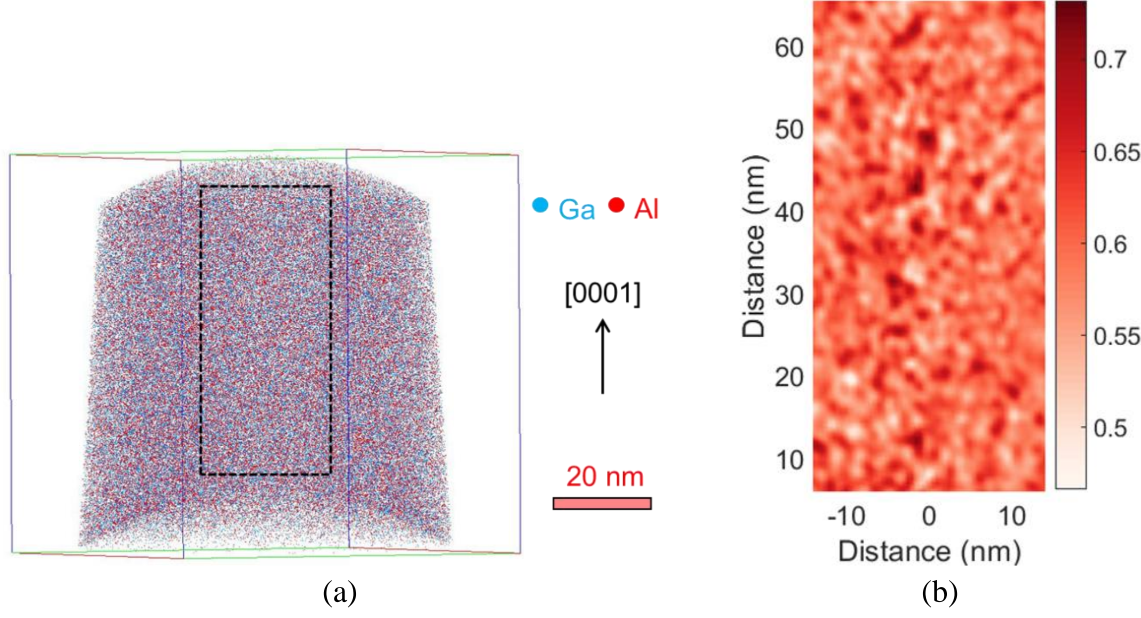


Figure 3.7 3D APT reconstruction of 60 nm of $Al_{0.59}Ga_{0.41}N$ showing Al and Ga atoms. (b) 2D distribution of the Aluminum fraction measured from the dashed rectangle shown in (a). APT data courtesy Dr. Batien Bonef.

3.3.2 Doping optimization for Si-doped AlGaN

The doping optimization of the n-AlGaN was done by varying the growth rate and Si cell temperature while keeping the Al% and other growth parameters the same. Figure 3.8 (a) shows the n-type carrier concentration, resistivity, and mobility of n-AlGaN (series 1) with an Al% of 61.6% and a growth rate of 109 nm/hr. The Si cell temperature was varied from 1375 to 1450 °C, at a step of 25 °C. The Si-doped AlGaN grown with a Si cell temperature of 1450 °C is insulating and no valid Hall data was acquired. Using a Si cell temperature of 1400 °C, both the lowest resistivity (10.5 mΩ·cm) and the highest n-type carrier concentration (1.2×10^{19} cm^{-3}) was achieved. Similar doping series (series 2) was done at 210 nm/hr for AlGaN with Al%= 59.4% as shown in Figure 3.8 (b). At this growth rate, the optimum Si cell temperature was at 1425 °C. The carrier concentration was 4×10^{19} cm^{-3}, the mobility was 48 cm^{2}·V·s^{-1}, and the

resistivity was 3 mΩ·cm. The morphology for this sample was measured by AFM and shown in Figure 3.9. No pits were observed on the surface. The RMS roughness is 0.6 nm.

The AlGaN:Si grown at the faster growth rate had wider optimal doping window, higher carrier concentration, and lower resistivities. Both doping profile show the "knee behavior" commonly observed for Si:AlGaN. As the Si cell temperature increased, the resistivity decreased while the carrier concentration increased at low doping region and the reverse happened at high doping region. The transition occurred at the Si cell temperature of 1400 and 1425 °C for series 1 and 2, respectively (refer to Figure 3.8).

SIMS measurements were done on the second growth series for the Si, C, H, and O concentration (Figure 3.10). The oxygen and carbon level were at $4\text{-}7\times10^{17}$ and 2×10^{16} cm^{-3}, respectively, and were stable at various Si cell temperature. When the Si cell temperature increase from 1400 °C to 1425 and then 1450 °C, the hydrogen incorporation increased from 1.5×10^{17} cm^{-3} to 7.5×10^{17} cm^{-3} and then to 1.8×10^{18} cm^{-3}.

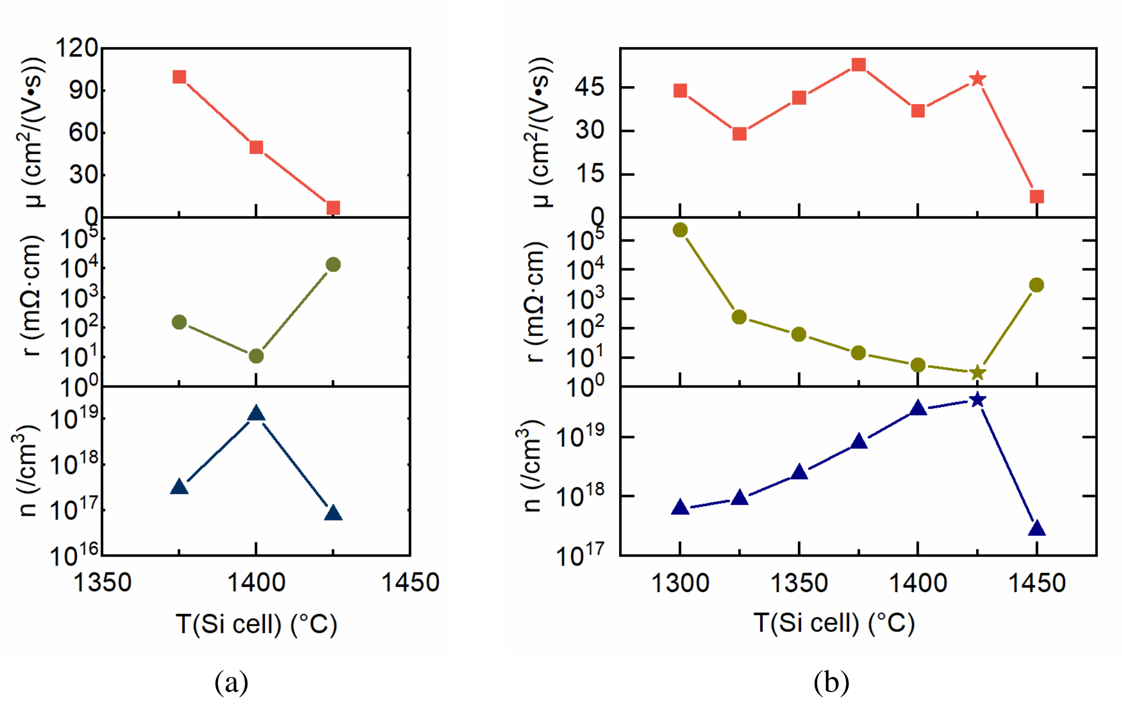


Figure 3.8 Doping optimization for n-AlGaN by varying the Si cell temperature using a growth rate of (a) 109 nm/hr at Al%=61.6% (series 1) and (b) 210 nm/hr at Al%=59.4% (series 2). The n-AlGaN grown at 109 nm/hr with the Si cell at 1450 °C was resistive and thus not shown in (a). The star shape denotes the optimum growth condition for the 210 nm/hr growth rate.

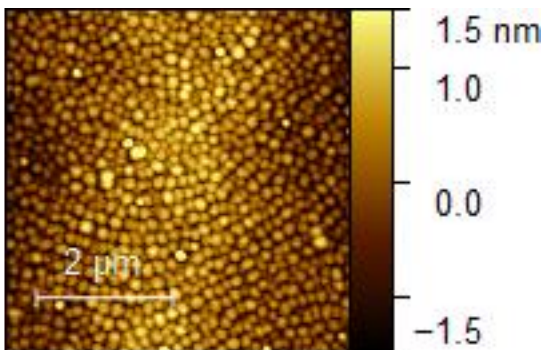


Figure 3.9 AFM image of the optimum n-AlGaN growth condition (star sign in Figure 6). The RMS roughness is 0.6 nm. There were no pits on the surface.

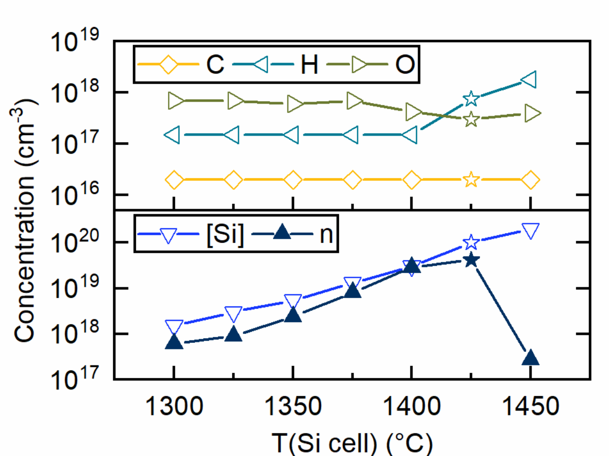


Figure 3.10 Si, C, H, and O concentration in n-AlGaN series 2 samples measured by secondary ion mass microscopy (SIMS). The n-type carrier concentration is included for comparison. The star shape denotes the optimum doping condition.

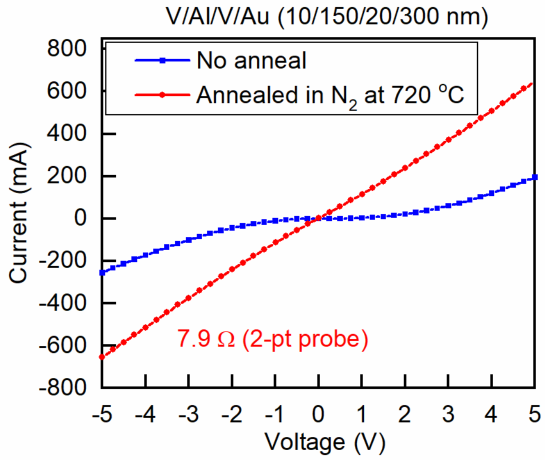


Figure 3.11 IV curve for CTLM pattern with 10 nm gap on n-AlGaN with vanadium-based contact before and after annealing in N_2 gas at 720 °C for 30 s.

CTLM measurements were done on a V/Al/V/Au contact deposited on a Si-doped $Al_{0.59}Ga_{0.41}N$. The growth of the AlGaN layers was done at the same time as the TJ regrowth and have the same epi structure as the MBE part in Figure 3.1 (b). The carrier concentration and resistivity for the n+ layer was 1.9×10^{19} cm^{-3} and 12 mΩ·cm respectively. Figure 3.11

shows the IV curve for the 10 nm gap CTLM pattern. The contact changed from Schottky to Ohmic after annealing in N2 gas at 720 °C for 30 s. The resistance of the ohmic contact was 7.9 Ω as measured by 2-point probe. CTLM measured on the sample showed that the specific contact resistance was 5.3×10^{-6}-8.9×10^{-6}. The transfer length was 2.3 μm. The sheet resistance was around 125 $\Omega\cdot\square^{-1}$. The contact resistance is low enough that it does not introduce any appreciable voltage penalty in the IV characteristics of the different LEDs in the later part of the study.

Indium has been shown to improve the conductivity of p-GaN [85] and Si-doped AlGaN [68] in literature. Attempts were made to use this technique in this study. However, the contact became less Ohmic while the resistivity increased.

4.3.3 UVC TJ LEDs

The optimized n-AlGaN growth condition was used to grow UVC TJ LEDs as shown in Figure 3.1(a). Figure 3.13 shows the AFM image for the regrowth area. The rms roughness was 2.2 nm.

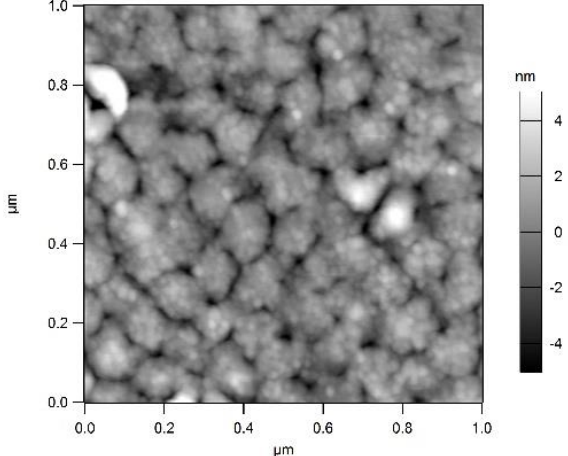


Figure 3.12 AFM images of the n-AlGaN regrown area on the UVC TJ LED.

Figure 3.13 (a) shows the EL spectrum of the TJ LED wafer before LED processing, where it was obtained from the UV light emitted below indium dots (50 μm in diameter). The EL emission wavelength was around 278 nm, which confirmed non-equilibrium hole injection through the TJ structure into the LED active region.

Figure 3.13 (b) shows the IV characteristics of the processed TJ LED as compared to an LED with the same MOCVD structure but without the TJ regrowth, and an identical LED without regrowth but with 5 nm of p-GaN on top of the MOCVD structure, which was reported elsewhere [82]. The LED with the ultrathin 0.5 nm p-GaN and no TJ regrowth did not turn on yet it turned on after adding the transparent n-AlGaN TJ structure. This is speculated to be a result of inefficient hole injection due to small thickness of p-GaN (0.5 nm). The TJ LED turn on voltage had an excess voltage of 4.1 V compared to the LED with 5 nm of p-GaN. The excess voltage is high compared to blue TJ LEDs grown with similar approach (<1 V) [75,86]. This is partially due to the wider band gap of AlGaN, the higher activation energy of carriers, and the lower doping concentration (N_A and N_D) in AlGaN material. More optimizations are needed to lower the excess voltage.

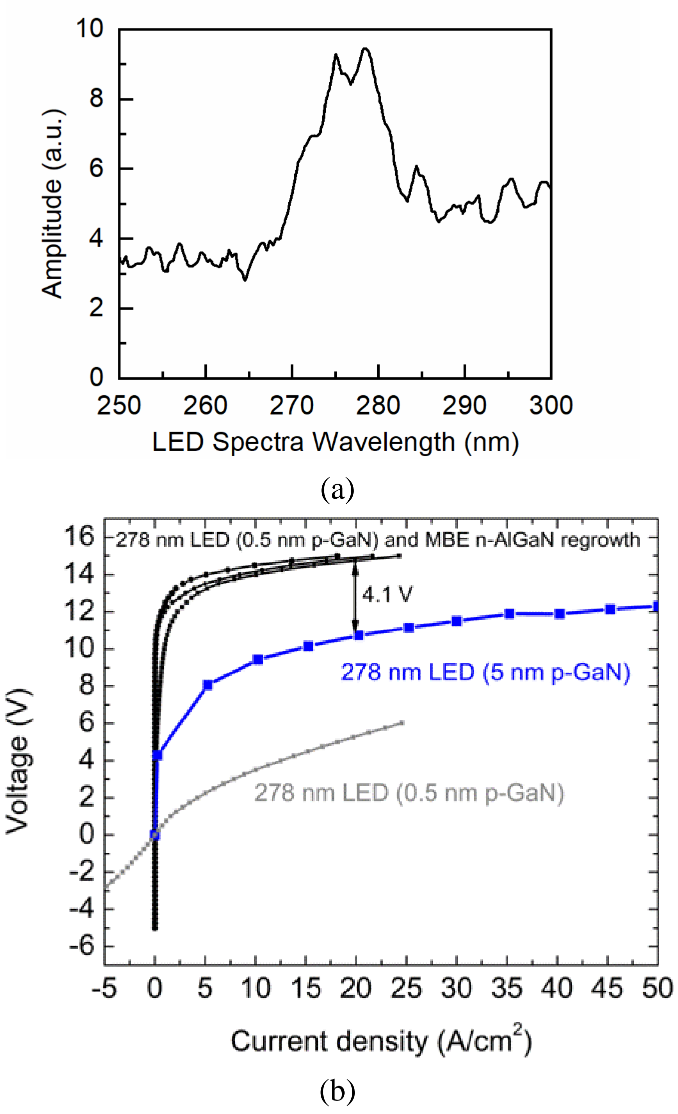


Figure 3.13 (a) Electroluminescence spectra of the UVC LED with TJ. (b) I-V characteristics for the processed TJ LED, an LED with the same MOCVD structure but without the TJ regrowth, and an identical LED without regrowth but with 5 nm of p-GaN on top of the MOCVD structure. Figure courtesy Dr. Burhan SaifAddin.

3.4 Conclusion

In this work, we demonstrated high carrier concentration, low resistivity n-AlGaN by NH_3 MBE with the Al% around 60%. The films had smooth morphology and were crack free for

the thickness investigated (up to 1 μm). XRD RSM scan was used to determine the alloy composition and the result agrees well with the APT result. The higher growth rate had a wider optimum doping window when varying the Si cell temperature. At a growth rate of 210 nm/hr, with a Si cell temperature of 1425 °C, n-AlGaN with a carrier concentration of 4×10^{19} /cm^3 and a resistivity of 3 mΩ·cm was achieved. SIMS measurements shows that the Si incorporation increases with increased Si cell temperature and the hydrogen incorporation increased at high cell temperature. Ohmic contacts were achieved on the n-AlGaN using annealed vanadium-based contact stack. The optimized n-AlGaN was employed to show that a transparent tunnel junction can significantly reduce the thickness of p-GaN in UVC LEDs, however, further research is needed to reduce the excess voltage (4.1 V).

3.5 Future work

To measure the N_D in the n-AlGaN, especially for the over-doped conditions, temperature-controlled Hall needs to be done. In this work, the voltage penalty for the UVC TJ LED is 4.1 V. This value is high compared to the voltage penalty (0.23-0.3 V) of blue TJ LED demonstrated in Chapter 2. Possible reasons for the high voltage penalty are: 1) the wider band gap of AlGaN (5 eV) compared to GaN (3.4 eV); 2) the lower doping concentration N_A and N_D of AlGaN and thus the wider depletion width; 3) the activation energy for both Mg and Si in AlGaN; and 4) limited number of optimizations done for the TJ structure, including optimizations on the layers' thickness and doping levels.

InGaN/GaN interlayers and polarization doped p-AlGaN by grading the Al% composition [87] are used in literature to improve the tunneling and the UV (TJ) LED performance. Figure

3.14 shows the hole concentration and band diagram simulation by SilenSe for a UV LED with and without Al% grading of 85%-55% in Mg:AlGaN layer.

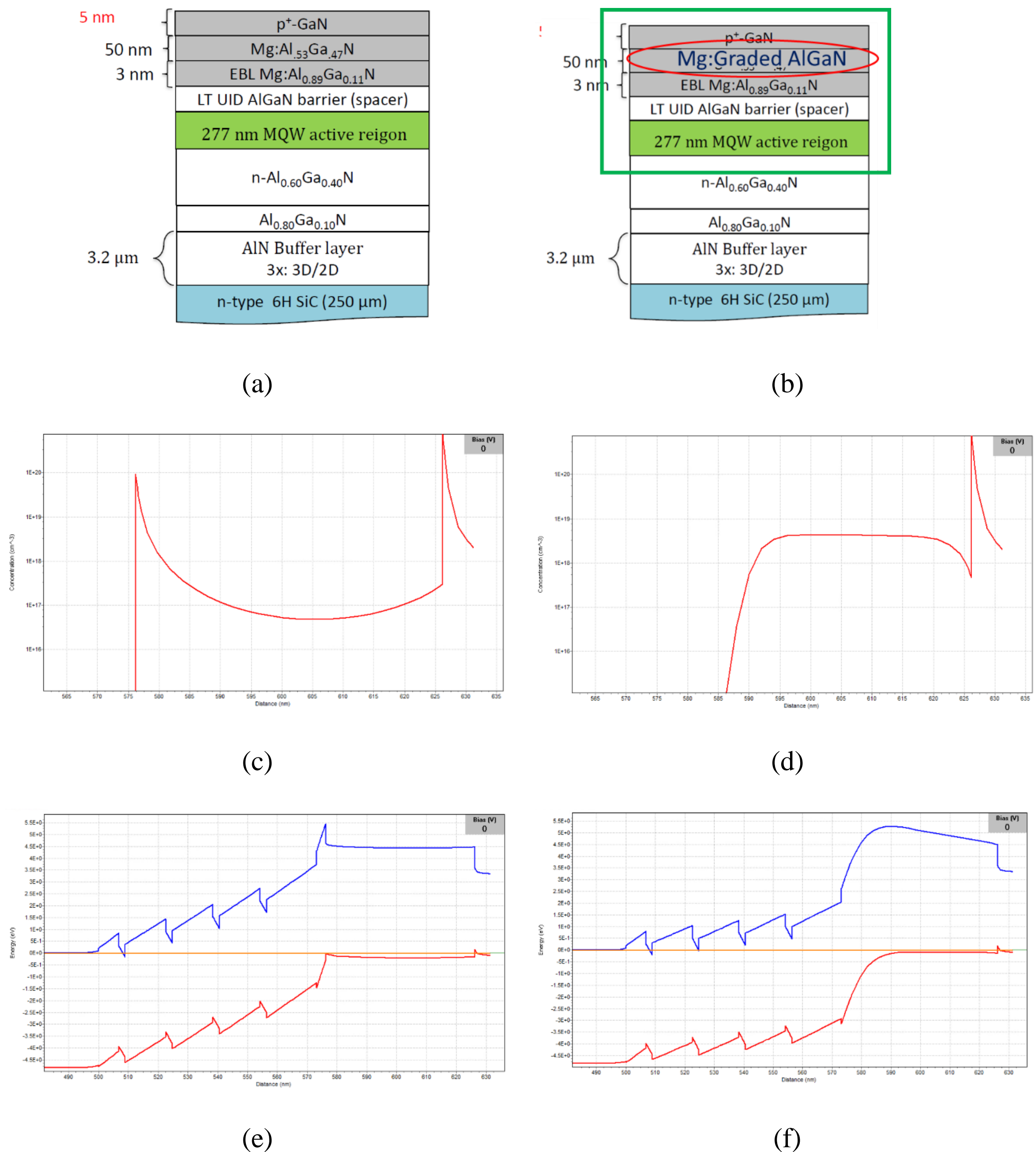


Figure 3.14 The hole concentration and band diagram for UV LEDs with and without Al% grading. (a) Schematic of UV LED. (b) Schematic of UV LED with Al% grading of 85-55% in Mg:AlGaN layer. (c) At a Mg concentration of 1×10^{19}, hole concentration, h, is ~10^{16}. (d) with grading, h is ~ 10^{18}. (e-f) Valence band is closer to Fermi level with grading.

The TJ UVC LED wafer in this study had a low yield since the flip-chip bonding was weak. Besides, the indium creeping on the regrowth surface also made the pressure uneven during bonding. The indium creeping was observed for SiO_2-involved growth only, possibly due to the better wetting between SiO_2 and In. Blank regrowth, improved In-Au flip-chip bonding, along with a larger mesa dimension will improve the yield.

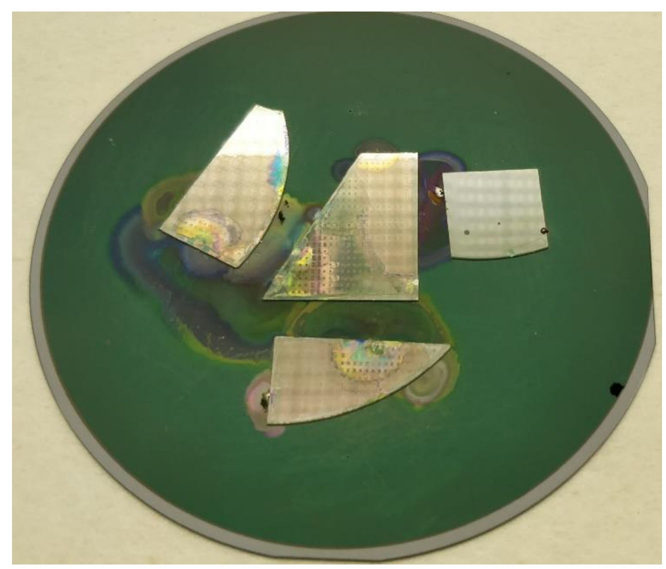


Figure 3.15 Images of samples after the regrowth. Indium-crept on the sample surface for UV LED wafers with SiO_2 hard mask. No such effect was observed for blank regrowth (for example, the sample on the top right).

All MBE UV TJ is of interest due to the high NH_3 MBE p-GaN and p-AlGaN quality [73] and the controlled impurity levels at the tunnel junction interface. Oxygen and carbon can act as DX centers in n-AlGaN [48-50], lowering the conductivity and creating potential non-radiative recombination centers. The interface impurities can be buried with the p-type regrowth at the regrowth interface, keeping them away from n-AlGaN layers.

References

1. G. Y. Lui, D. Roser, R. Corkish, N. J. Ashbolt, and R. Stuetz, "Point-of-use water disinfection using ultraviolet and visible light-emitting diodes," Science of The Total Environment **553**, 626–635 (2016).
2. K. Song, M. Mohseni, and F. Taghipour, "Application of ultraviolet light-emitting diodes (UV-LEDs) for water disinfection: A review," Water Research **94**, 341–349 (2016).
3. A. Kheyrandish, M. Mohseni, and F. Taghipour, "Development of a method for the characterization and operation of UV-LED for water treatment," Water Research **122**, 570–579 (2017).
4. S. Vilhunen, H. Särkkä, and M. Sillanpää, "Ultraviolet light-emitting diodes in water disinfection," Environ Sci Pollut Res **16**, 439–442 (2009).
5. P. Murphy, L. Kang, M. Fleming, C. Atkinson, R. Pryor, K. Cooper, E. Godbout, M. P. Stevens, M. Doll, and G. Bearman, "Effect of ultraviolet-C light disinfection at terminal patient discharge on hospital-acquired infections in bone marrow transplant and oncology units," American Journal of Infection Control **48**, 705–707 (2020).
6. J. Pagán and O. R. Lawal, "Coming of Age-UVC LED Technology Update," /paper/Coming-of-Age-UVC-LED-Technology-Update-Pag%C3%A1n-Lawal/da5db3d09120d99ed2c8116890c6f1952c1c7de0.
7. Y. Zhang, Z. Jamal-Eddine, and S. Rajan, "Recent progress of tunnel junction-based ultra-violet light emitting diodes," Jpn. J. Appl. Phys. **58**, SC0805 (2019).
8. T. Takano, T. Mino, J. Sakai, N. Noguchi, K. Tsubaki, and H. Hirayama, "Deep-ultraviolet light-emitting diodes with external quantum efficiency higher than 20% at 275 nm achieved by improving light-extraction efficiency," Appl. Phys. Express **10**, 031002 (2017).
9. Y. Guo, Y. Zhang, J. Yan, H. Xie, L. Liu, X. Chen, M. Hou, Z. Qin, J. Wang, and J. Li, "Light extraction enhancement of AlGaN-based ultraviolet light-emitting diodes by substrate sidewall roughening," Appl. Phys. Lett. **111**, 011102 (2017).

10. J. Yun and H. Hirayama, "Investigation of the light-extraction efficiency in 280 nm AlGaN-based light-emitting diodes having a highly transparent p-AlGaN layer," Journal of Applied Physics **121**, 013105 (2017).
11. H.-Y. Ryu, I.-G. Choi, H.-S. Choi, and J.-I. Shim, "Investigation of Light Extraction Efficiency in AlGaN Deep-Ultraviolet Light-Emitting Diodes," Appl. Phys. Express **6**, 062101 (2013).
12. J. Rass and N. Lobo-Ploch, "Optical Polarization and Light Extraction from UV LEDs," in *III-Nitride Ultraviolet Emitters: Technology and Applications*, M. Kneissl and J. Rass, eds., Springer Series in Materials Science (Springer International Publishing, 2016), pp. 137–170.
13. J. R. Grandusky, J. Chen, S. R. Gibb, M. C. Mendrick, C. G. Moe, L. Rodak, G. A. Garrett, M. Wraback, and L. J. Schowalter, "270 nm Pseudomorphic Ultraviolet Light-Emitting Diodes with Over 60 mW Continuous Wave Output Power," Appl. Phys. Express **6**, 032101 (2013).
14. T. Inazu, S. Fukahori, C. Pernot, M. H. Kim, T. Fujita, Y. Nagasawa, A. Hirano, M. Ippommatsu, M. Iwaya, T. Takeuchi, S. Kamiyama, M. Yamaguchi, Y. Honda, H. Amano, and I. Akasaki, "Improvement of Light Extraction Efficiency for AlGaN-Based Deep Ultraviolet Light-Emitting Diodes," Jpn. J. Appl. Phys. **50**, 122101 (2011).
15. B. T. Tran and H. Hirayama, "Growth and Fabrication of High External Quantum Efficiency AlGaN-Based Deep Ultraviolet Light-Emitting Diode Grown on Pattern Si Substrate," Scientific Reports **7**, 12176 (2017).
16. Y. Zhang, A. A. Allerman, S. Krishnamoorthy, F. Akyol, M. W. Moseley, A. M. Armstrong, and S. Rajan, "Enhanced light extraction in tunnel junction-enabled top emitting UV LEDs," Appl. Phys. Express **9**, 052102 (2016).
17. Y. Zhang, S. Krishnamoorthy, F. Akyol, S. Bajaj, A. A. Allerman, M. W. Moseley, A. M. Armstrong, and S. Rajan, "Tunnel-injected sub-260 nm ultraviolet light emitting diodes," Applied Physics Letters **110**, 201102 (2017).
18. C. Lalau Keraly, L. Kuritzky, M. Cochet, and C. Weisbuch, "Light Extraction Efficiency Part A. Ray Tracing for Light Extraction Efficiency (LEE) Modeling in Nitride LEDs," in *III-Nitride Based Light Emitting Diodes and Applications*, T.-Y.

Seong, J. Han, H. Amano, and H. Morkoc, eds., Topics in Applied Physics (Springer Netherlands, 2013), pp. 231–269.

19. B. K. SaifAddin, A. Almogbel, C. J. Zollner, H. Foronda, A. Alyamani, A. Albadri, M. Iza, S. Nakamura, S. P. DenBaars, and J. S. Speck, "Fabrication technology for high light-extraction ultraviolet thin-film flip-chip (UV TFFC) LEDs grown on SiC," Semicond. Sci. Technol. **34**, 035007 (2019).
20. B. K. SaifAddin, PhD thesis, University of California, Santa Barbara, Materials, *Development of Deep Ultraviolet (UV-C) Thin-Film Light-Emitting Diodes Grown on SiC*. (2018).
21. J. K. Kim, J. W. Lee, D.-Y. Kim, J. H. Park, E. F. Schubert, J. Kim, and Y.-I. Kim, "An elegant route to overcome fundamentally-limited light extraction in AlGaN deep-ultraviolet light-emitting diodes: preferential outcoupling of strong in-plane emission (Conference Presentation)," in *UV and Higher Energy Photonics: From Materials to Applications* (International Society for Optics and Photonics, 2016), Vol. 9926, p. 99260F.
22. H. Kim, S.-N. Lee, Y. Park, K.-K. Kim, J. S. Kwak, and T.-Y. Seong, "Light extraction enhancement of GaN-based light emitting diodes using MgF2/Al omnidirectional reflectors," Journal of Applied Physics **104**, 053111 (2008).
23. J. F. Muth, J. H. Lee, I. K. Shmagin, R. M. Kolbas, H. C. Casey, B. P. Keller, U. K. Mishra, and S. P. DenBaars, "Absorption coefficient, energy gap, exciton binding energy, and recombination lifetime of GaN obtained from transmission measurements," Appl. Phys. Lett. **71**, 2572–2574 (1997).
24. J. Hwang, W. J. Schaff, L. F. Eastman, S. T. Bradley, L. J. Brillson, D. C. Look, J. Wu, W. Walukiewicz, M. Furis, and A. N. Cartwright, "Si doping of high-Al-mole fraction AlxGa1−xN alloys with rf plasma-induced molecular-beam-epitaxy," Appl. Phys. Lett. **81**, 5192–5194 (2002).
25. Y. Zhang, S. Krishnamoorthy, F. Akyol, S. Bajaj, A. A. Allerman, M. W. Moseley, A. M. Armstrong, and S. Rajan, "Tunnel-injected sub-260 nm ultraviolet light emitting diodes," Appl. Phys. Lett. **110**, 201102 (2017).
26. Y. Taniyasu, M. Kasu, and N. Kobayashi, "Intentional control of n-type conduction for Si-doped AlN and AlXGa1−XN (0.42⩽x<1)," Appl. Phys. Lett. **81**, 1255–1257 (2002).

27. R. Collazo, S. Mita, J. Xie, A. Rice, J. Tweedie, R. Dalmau, and Z. Sitar, "Progress on n-type doping of AlGaN alloys on AlN single crystal substrates for UV optoelectronic applications," physica status solidi c **8**, 2031–2033 (2011).
28. M. L. Nakarmi, K. H. Kim, K. Zhu, J. Y. Lin, and H. X. Jiang, "Transport properties of highly conductive n-type Al-rich AlxGa1−xN(x⩾0.7)," Appl. Phys. Lett. **85**, 3769–3771 (2004).
29. Y. Taniyasu, M. Kasu, and T. Makimoto, "Electrical conduction properties of n-type Si-doped AlN with high electron mobility (>100cm^{2}V^{-1}s^{-1})," Appl. Phys. Lett. **85**, 4672–4674 (2004).
30. T. Ive, O. Brandt, H. Kostial, K. J. Friedland, L. Däweritz, and K. H. Ploog, "Controlled n-type doping of AlN:Si films grown on 6H-SiC(0001) by plasma-assisted molecular beam epitaxy," Appl. Phys. Lett. **86**, 024106 (2005).
31. M. Ahoujja, J. L. McFall, Y. K. Yeo, R. L. Hengehold, and J. E. Van Nostrand, "Electrical and optical investigation of MBE grown Si-doped AlxGa1−xN as a function of Al mole fraction up to 0.5," Materials Science and Engineering: B **91–92**, 285–289 (2002).
32. A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, M. G. Mil'vidskii, J. M. Redwing, M. Shin, M. Skowronski, D. W. Greve, and R. G. Wilson, "Properties of Si donors and persistent photoconductivity in AlGaN," Solid-State Electronics **42**, 627–635 (1998).
33. M. Stutzmann, O. Ambacher, A. Cros, M. S. Brandt, H. Angerer, R. Dimitrov, N. Reinacher, T. Metzger, R. Höpler, D. Brunner, F. Freudenberg, R. Handschuh, and C. Deger, "Properties and applications of MBE grown AlGaN," Materials Science and Engineering: B **50**, 212–218 (1997).
34. S. N. Mohammad and H. Morkoç, "Progress and prospects of group-III nitride semiconductors," Progress in Quantum Electronics **20**, 361–525 (1996).
35. V. W. L. Chin, T. L. Tansley, and T. Osotchan, "Electron mobilities in gallium, indium, and aluminum nitrides," Journal of Applied Physics **75**, 7365–7372 (1994).
36. Y.-H. Liang and E. Towe, "Progress in efficient doping of high aluminum-containing group III-nitrides," Applied Physics Reviews **5**, 011107 (2018).
37. M. C. Wagener, G. R. James, and F. Omnès, "Intrinsic compensation of silicon-doped AlGaN," Appl. Phys. Lett. **83**, 4193–4195 (2003).

38. F. Mehnke, X. T. Trinh, H. Pingel, T. Wernicke, E. Janzén, N. T. Son, and M. Kneissl, "Electronic properties of Si-doped Alx Ga1−xN with aluminum mole fractions above 80%," Journal of Applied Physics **120**, 145702 (2016).

39. B. Borisov, V. Kuryatkov, Yu. Kudryavtsev, R. Asomoza, S. Nikishin, D. Y. Song, M. Holtz, and H. Temkin, "Si-doped AlxGa1−xN(0.56⩽×⩽1) layers grown by molecular beam epitaxy with ammonia," Appl. Phys. Lett. **87**, 132106 (2005).

40. J. Pyeon, J. Kim, M. Jeon, K. Ko, E. Shin, and O. Nam, "Self-compensation effect in Si-doped $Al_{0.55}Ga_{0.45}N$ layers for deep ultraviolet applications," Jpn. J. Appl. Phys. **54**, 051002 (2015).

41. I. Bryan, Z. Bryan, S. Washiyama, P. Reddy, B. Gaddy, B. Sarkar, M. H. Breckenridge, Q. Guo, M. Bobea, J. Tweedie, S. Mita, D. Irving, R. Collazo, and Z. Sitar, "Doping and compensation in Al-rich AlGaN grown on single crystal AlN and sapphire by MOCVD," Appl. Phys. Lett. **112**, 062102 (2018).

42. R. Zeisel, M. W. Bayerl, S. T. B. Goennenwein, R. Dimitrov, O. Ambacher, M. S. Brandt, and M. Stutzmann, "DX-behavior of Si in AlN," Phys. Rev. B **61**, R16283–R16286 (2000).

43. D. Korakakis, H. M. Ng, K. F. Ludwig, and T. D. Moustakas, "Doping Studies of n- and p-Type $Al_xGa_{1-x}N$ Grown by ECR-Assisted MBE," MRS Online Proceedings Library Archive **449**, (1996).

44. M. Hermann, F. Furtmayr, A. Bergmaier, G. Dollinger, M. Stutzmann, and M. Eickhoff, "Highly Si-doped AlN grown by plasma-assisted molecular-beam epitaxy," Appl. Phys. Lett. **86**, 192108 (2005).

45. X. Thang Trinh, D. Nilsson, I. G. Ivanov, E. Janzén, A. Kakanakova-Georgieva, and N. Tien Son, "Negative-U behavior of the Si donor in Al0.77Ga0.23N," Appl. Phys. Lett. **103**, 042101 (2013).

46. P. Pampili and P. J. Parbrook, "Doping of III-nitride materials," Materials Science in Semiconductor Processing **62**, 180–191 (2017).

47. C. Skierbiszewski, T. Suski, M. Leszczynski, M. Shin, M. Skowronski, M. D. Bremser, and R. F. Davis, "Evidence for localized Si-donor state and its metastable properties in AlGaN," Appl. Phys. Lett. **74**, 3833–3835 (1999).

48. C. G. Van de Walle, "DX-center formation in wurtzite and zinc-blende AlGaN," Phys. Rev. B **57**, R2033–R2036 (1998).

49. L. Gordon, J. L. Lyons, A. Janotti, and C. G. Van de Walle, "Hybrid functional calculations of DX centers in AlN and GaN," Phys. Rev. B **89**, 085204 (2014).

50. N. T. Son, M. Bickermann, and E. Janzén, "Shallow donor and DX states of Si in AlN," Appl. Phys. Lett. **98**, 092104 (2011).

51. Q. Yan, A. Janotti, M. Scheffler, and C. G. Van de Walle, "Origins of optical absorption and emission lines in AlN," Appl. Phys. Lett. **105**, 111104 (2014).

52. J. S. Harris, B. E. Gaddy, R. Collazo, Z. Sitar, and D. L. Irving, "Oxygen and silicon point defects in $Al_{0.65}Ga_{0.35}N$," Phys. Rev. Materials **3**, 054604 (2019).

53. J. S. Harris, J. N. Baker, B. E. Gaddy, I. Bryan, Z. Bryan, K. J. Mirrielees, P. Reddy, R. Collazo, Z. Sitar, and D. L. Irving, "On compensation in Si-doped AlN," Appl. Phys. Lett. **112**, 152101 (2018).

54. M. D. McCluskey, N. M. Johnson, C. G. Van de Walle, D. P. Bour, M. Kneissl, and W. Walukiewicz, "Metastability of Oxygen Donors in AlGaN," Phys. Rev. Lett. **80**, 4008–4011 (1998).

55. T. Mattila and R. M. Nieminen, "Point-defect complexes and broadband luminescence in GaN and AlN," Phys. Rev. B **55**, 9571–9576 (1997).

56. C. Stampfl and C. G. Van de Walle, "Theoretical investigation of native defects, impurities, and complexes in aluminum nitride," Phys. Rev. B **65**, 155212 (2002).

57. I. Gorczyca, N. E. Christensen, and A. Svane, "Influence of hydrostatic pressure on cation vacancies in GaN, AlN, and GaAs," Phys. Rev. B **66**, 075210 (2002).

58. J. Slotte, F. Tuomisto, K. Saarinen, C. G. Moe, S. Keller, and S. P. DenBaars, "Influence of silicon doping on vacancies and optical properties of AlxGa1−xN thin films," Appl. Phys. Lett. **90**, 151908 (2007).

59. C. Stampfl and C. G. Van de Walle, "Doping of $Al_xGa_{1-x}N$," Appl. Phys. Lett. **72**, 459–461 (1998).

60. W. Walukiewicz, "Intrinsic limitations to the doping of wide-gap semiconductors," Physica B: Condensed Matter **302–303**, 123–134 (2001).

61. A. Uedono, K. Tenjinbayashi, T. Tsutsui, Y. Shimahara, H. Miyake, K. Hiramatsu, N. Oshima, R. Suzuki, and S. Ishibashi, "Native cation vacancies in Si-doped AlGaN

studied by monoenergetic positron beams," Journal of Applied Physics **111**, 013512 (2012).

62. T. Onuma, S. F. Chichibu, A. Uedono, T. Sota, P. Cantu, T. M. Katona, J. F. Keading, S. Keller, U. K. Mishra, S. Nakamura, and S. P. DenBaars, "Radiative and nonradiative processes in strain-free $Al_xGa_{1-x}N$ films studied by time-resolved photoluminescence and positron annihilation techniques," Journal of Applied Physics **95**, 2495–2504 (2004).
63. S. F. Chichibu, H. Miyake, Y. Ishikawa, M. Tashiro, T. Ohtomo, K. Furusawa, K. Hazu, K. Hiramatsu, and A. Uedono, "Impacts of Si-doping and resultant cation vacancy formation on the luminescence dynamics for the near-band-edge emission of Al0.6Ga0.4N films grown on AlN templates by metalorganic vapor phase epitaxy," Journal of Applied Physics **113**, 213506 (2013).
64. S. Washiyama, P. Reddy, B. Sarkar, M. H. Breckenridge, Q. Guo, P. Bagheri, A. Klump, R. Kirste, J. Tweedie, S. Mita, Z. Sitar, and R. Collazo, "The role of chemical potential in compensation control in Si:AlGaN," Journal of Applied Physics **127**, 105702 (2020).
65. K. B. Nam, J. Li, M. L. Nakarmi, J. Y. Lin, and H. X. Jiang, "Achieving highly conductive AlGaN alloys with high Al contents," Appl. Phys. Lett. **81**, 1038–1040 (2002).
66. P. Cantu, S. Keller, U. K. Mishra, and S. P. DenBaars, "Metalorganic chemical vapor deposition of highly conductive Al0.65Ga0.35N films," Appl. Phys. Lett. **82**, 3683–3685 (2003).
67. M. D. Bremser, W. G. Perry, T. Zheleva, N. V. Edwards, O. H. Nam, N. Parikh, D. E. Aspnes, and R. F. Davis, "Growth, Doping and Characterization of AlxGa1−xN Thin Film Alloys on 6H-SiC(0001) Substrates," Materials Research Society Internet Journal of Nitride Semiconductor Research **1**, (1996).
68. T. M. Al tahtamouni, A. Sedhain, J. Y. Lin, and H. X. Jiang, "Si-doped high Al-content AlGaN epilayers with improved quality and conductivity using indium as a surfactant," Appl. Phys. Lett. **92**, 092105 (2008).

69. K. Zhu, M. L. Nakarmi, K. H. Kim, J. Y. Lin, and H. X. Jiang, "Silicon doping dependence of highly conductive n-type Al0.7Ga0.3N," Appl. Phys. Lett. **85**, 4669–4671 (2004).

70. A. Kakanakova-Georgieva, D. Nilsson, X. T. Trinh, U. Forsberg, N. T. Son, and E. Janzén, "The complex impact of silicon and oxygen on the n-type conductivity of high-Al-content AlGaN," Appl. Phys. Lett. **102**, 132113 (2013).

71. Y. Shimahara, H. Miyake, K. Hiramatsu, F. Fukuyo, T. Okada, H. Takaoka, and H. Yoshida, "Growth of High-Quality Si-Doped AlGaN by Low-Pressure Metalorganic Vapor Phase Epitaxy," Jpn. J. Appl. Phys. **50**, 095502 (2011).

72. S. Keller, P. Cantu, C. Moe, Y. Wu, S. Keller, U. K. Mishra, J. S. Speck, and S. P. DenBaars, "Metalorganic Chemical Vapor Deposition Conditions for Efficient Silicon Doping in High Al-Composition AlGaN Films," Jpn. J. Appl. Phys. **44**, 7227 (2005).

73. E. C. H. Kyle, S. W. Kaun, P. G. Burke, F. Wu, Y.-R. Wu, and J. S. Speck, "High-electron-mobility GaN grown on free-standing GaN templates by ammonia-based molecular beam epitaxy," Journal of Applied Physics **115**, 193702 (2014).

74. L. Lugani, M. Malinverni, S. Tirelli, D. Marti, E. Giraud, J.-F. Carlin, C. R. Bolognesi, and N. Grandjean, "n+-GaN grown by ammonia molecular beam epitaxy: Application to regrown contacts," Appl. Phys. Lett. **105**, 202113 (2014).

75. E. C. Young, B. P. Yonkee, F. Wu, S. H. Oh, S. P. DenBaars, S. Nakamura, and J. S. Speck, "Hybrid tunnel junction contacts to III–nitride light-emitting diodes," Appl. Phys. Express **9**, 022102 (2016).

76. B. P. Yonkee, E. C. Young, C. Lee, J. T. Leonard, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Demonstration of a III-nitride edge-emitting laser diode utilizing a GaN tunnel junction contact," Opt. Express, OE **24**, 7816–7822 (2016).

77. C. A. Forman, S. Lee, E. C. Young, J. A. Kearns, D. A. Cohen, J. T. Leonard, T. Margalith, S. P. DenBaars, and S. Nakamura, "Continuous-wave operation of m-plane GaN-based vertical-cavity surface-emitting lasers with a tunnel junction intracavity contact," Appl. Phys. Lett. **112**, 111106 (2018).

78. M. Malinverni, D. Martin, and N. Grandjean, "InGaN based micro light emitting diodes featuring a buried GaN tunnel junction," Appl. Phys. Lett. **107**, 051107 (2015).

79. A. J. Mughal, E. C. Young, A. I. Alhassan, J. Back, S. Nakamura, J. S. Speck, and S. P. DenBaars, "Polarization-enhanced InGaN/GaN-based hybrid tunnel junction contacts to GaN p–n diodes and InGaN LEDs," Appl. Phys. Express **10**, 121006 (2017).
80. C. J. Zollner, A. Almogbel, Y. Yao, B. K. SaifAddin, F. Wu, M. Iza, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Reduced dislocation density and residual tension in AlN grown on SiC by metalorganic chemical vapor deposition," Appl. Phys. Lett. **115**, 161101 (2019).
81. H. M. Foronda, F. Wu, C. Zollner, M. E. Alif, B. Saifaddin, A. Almogbel, M. Iza, S. Nakamura, S. P. DenBaars, and J. S. Speck, "Low threading dislocation density aluminum nitride on silicon carbide through the use of reduced temperature interlayers," Journal of Crystal Growth **483**, 134–139 (2018).
82. B. K. SaifAddin, A. S. Almogbel, C. J. Zollner, F. Wu, B. Bonef, M. Iza, S. Nakamura, S. P. DenBaars, and J. S. Speck, "AlGaN Deep-Ultraviolet Light-Emitting Diodes Grown on SiC Substrates," ACS Photonics **7**, 554–561 (2020).
83. B. K. Saifaddin, M. Iza, H. Foronda, A. Almogbel, C. J. Zollner, F. Wu, A. Alyamani, A. Albadri, S. Nakamura, S. P. DenBaars, and J. S. Speck, "Impact of roughening density on the light extraction efficiency of thin-film flip-chip ultraviolet LEDs grown on SiC," Opt. Express, OE **27**, A1074–A1083 (2019).
84. T. Kuech, *Handbook of Crystal Growth: Thin Films and Epitaxy* (Elsevier, 2014).
85. E. C. H. Kyle, S. W. Kaun, E. C. Young, and J. S. Speck, "Increased p-type conductivity through use of an indium surfactant in the growth of Mg-doped GaN," Appl. Phys. Lett. **106**, 222103 (2015).
86. B. P. Yonkee, E. C. Young, J. T. Leonard, C. Lee, S. H. Oh, S. P. DenBaars, J. S. Speck, and S. Nakamura, "Hybrid MOCVD/MBE GaN tunnel junction LEDs with greater than 70% wall plug efficiency," in *2016 Compound Semiconductor Week (CSW) [Includes 28th International Conference on Indium Phosphide Related Materials (IPRM) 43rd International Symposium on Compound Semiconductors (ISCS)* (2016), pp. 1–1.
87. Y. Zhang, Z. Jamal-Eddine, and S. Rajan, "Recent progress of tunnel junction-based ultra- violet light emitting diodes," Jpn. J. Appl. Phys. **58**, SC0805 (2019).

Chapter 4 Growth development for low leakage high reverse breakdown GaN p-n diodes

4.1 Introduction

GaN has attracted a great amount of interests for its application in power semiconductor devices due to multiple desirable material properties. This include wide bandgap, low intrinsic carrier concentration, high breakdown field, high saturation velocity, and high thermal conductivity. Table 4.1 compares the material property of GaN compared to Si which is the conventional material choice for power electronics.

Table 4.1 Comparison of material properties between GaN and Si.

	GaN	Si
E_g (eV)	3.4	1.1
n_i (cm^{-3})	1.9×10^{-10}	1.5×10^{10}
F_{BR} (MV/cm)	3.4	0.3
v_{sat} (10^7 cm/s)	2.5	1.0
σ_{th} (W/m-K)	110	58

To investigate the application of GaN for power devices, GaN vertical p-n diodes was studied. GaN p-n diode is the base structure for more advanced GaN-based devices such as LEDs and power devices. A vertical configuration enables the current conduction in the vertical direction which is also the direction of growth. It also has smaller form factor compared to the lateral design.

There are several challenges to achieve low leakage current, high reverse breakdown voltage (V_{BR}) for a GaN p-n diode. First, the threading dislocation density (TDD) in the material needs to be low as it contributes to increased leakage and reduced breakdown voltage [1]. However, conventional GaN materials are grown on foreign substrate such as sapphire and have high TDD (> 10^9 /cm^3) [2]. High quality bulk GaN substrates has much lower TDD and is thus desirable for power devices. Second, to achieve a high V_{BR}, the net carrier concentration (N_{net}) in the drift region needs to be low. Figure 4.1 shows the charge and field profile for a GaN p-n diode. The drift region thickness is higher than the maximum depletion width W_{d_max} which correspond to the n-side depletion width when the peak field at the junction interface is at F_{BR} (breakdown field of GaN). The breakdown voltage is represented by the shaded area under the triangular field profile. The area is determined by the slope of the right-side of the triangle, which is proportional to N_{net}=N_D-N_A.

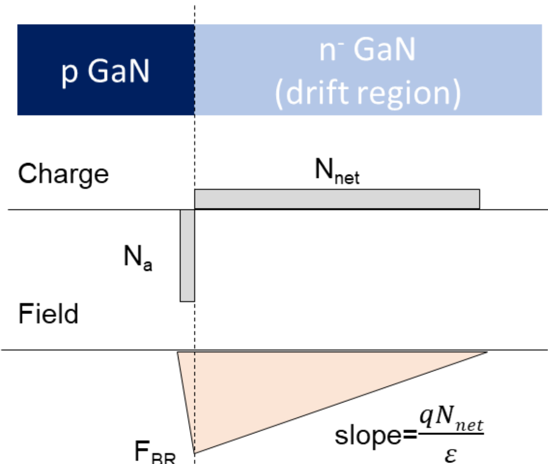


Figure 4.1 Charge and field profile for GaN p-n diode with lightly-doped drift region. Figure courtesy Dr. Yuewei Zhang.

The maximum breakdown field V_{BR_max} is thus,

$$V_{BR_max} = \frac{1}{2} F_{BR} \cdot W_{d_max} = \frac{1}{2} \frac{\varepsilon F_{BR}^2}{qN_{net}}$$

where F_{BR} is the breakdown voltage, W_{d_max} is the maximum depletion width, ε is the permittivity, q is the elementary charge. Figure 4.2 made by Dr. Yuewei Zhang shows the relationship between net charge concentration and maximum breakdown voltage for p-n diodes grown using different materials.

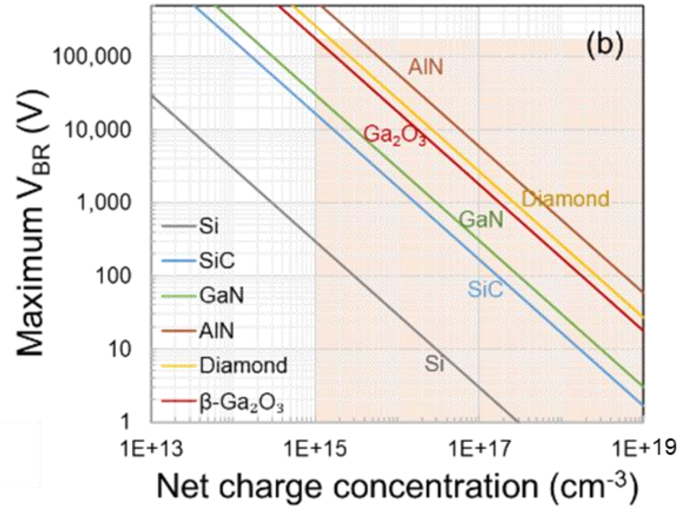


Figure 4.2 Maximum breakdown voltage as a function of the net charge concentration in the drift region for p-n diode grown using different materials. Figure courtesy Dr. Yuewei Zhang.

Un-intentionally doped (UID) GaN materials are n-type as grown due to the incorporation of impurities such as oxygen. Thus, low impurity concentration material is needed to form the drift region of the p-n diode. Other challenges for developing low leakage, high reverse breakdown GaN p-n diodes include field management, sidewall passivation, etc.

The scope of this study is focused on the growth development and is thus concentrated on developing low net doping level drift region GaN materials by NH_3 MBE. Combining the optimized growth condition with the high-quality p-GaN developed in the Chapter 1, we demonstrated GaN vertical diodes with low ideality factor (n=1.33) and high reverse break down voltage of over 1000 V.

4.2 Unintentionally doped GaN with low impurity concentration for n^- drift region

4.2.1 C/H/O levels vs growth rate by SIMS

To investigate the optimum growth rate for low impurity concentration drift region, we grew a SIMS stack by varying the grow rate from 0.6 to 1.7 µm/hr. The sample was grown by Dr. Morteza Monavarian and Clayton Qwah using a growth temperature of 820 °C on STN substrate. AlGaN marker layers were used to differentiate the layers of interests. The SIMS were done by Jianfeng Wang and Dr. Tom Mates. Figure 4.3 shows the SIMS result for O, C, and H levels in the material grown at 0.6, 1.0, 1.5, and 1.7 µm/hr, respectively. The results were summarized in table 4.2.

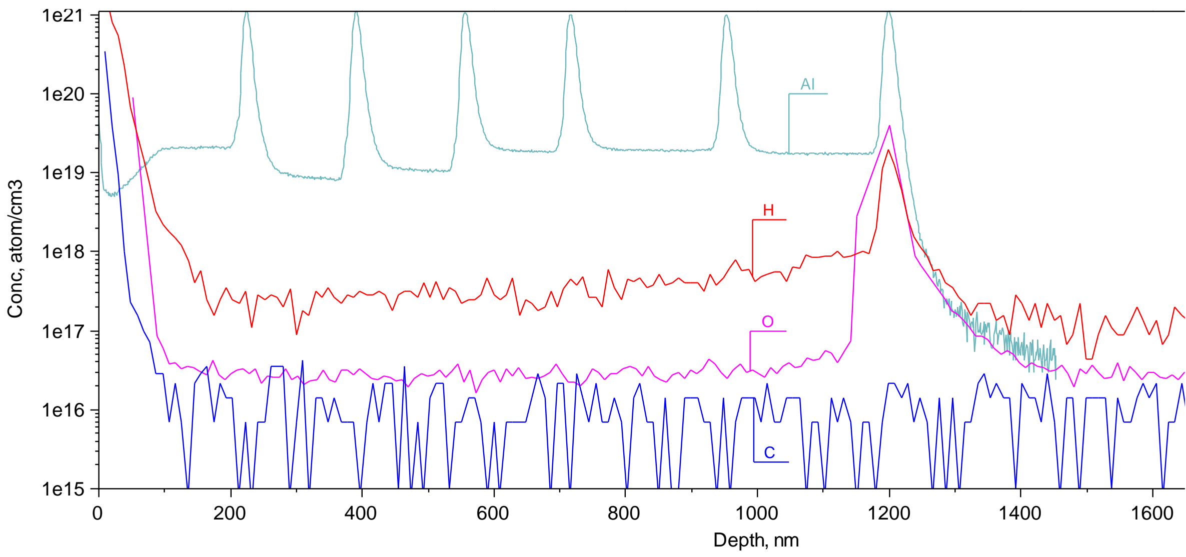


Figure 4.3 SIMS measurements for O, C, and H level in UID GaN layers grown using growth rate of 0.6, 1.0, 1.5, and 1.7 µm/hr from right to left.

Table 4.2 Summary of the SIMS result.

	Background	1.7 µm/hr	1.5 µm/hr	1.0 µm/hr	0.6 µm/hr
[O]	2.7×10^{16}	2.6×10^{16}	2.5×10^{16}	2.7×10^{16}	2.8×10^{16}
[C]	1×10^{16}	1×10^{16}	1×10^{16}	1×10^{16}	1×10^{16}
[H]	1×10^{17}	2.4×10^{17}	2.9×10^{17}	2.8×10^{17}	3.7×10^{17}

The O, C, and H levels were stable for the growth rate range investigated. The O and C levels were both below 3×10^{16} /cm^3. Oxygen acts as donor in GaN and carbon acts as deep level carriers. Having low oxygen and carbon level is promising in achieving low doping level materials.

4.2.2 N_{net} vs growth rate by CV measurements

Although SIMS enables us to measure some of the impurity concentrations, CV measurements provides us with a more direct way of evaluating the net carrier concentration (N_{net}) in the material. Defect-related carriers such as V_N can not be measured by SIMS but are taken into account in CV measurements.

1 µm of UID GaN were grown on STN substrates using growth rates of 0.37, 0.6, 1.02, and 1.68 µm/hr at a growth temperature of 820 °C. The samples were processed into metal-insulator-semiconductor (MIS) structure using 18.2 nm of SiO_2 deposited by atomic layer deposition (ALD) and 30/300 nm of Pt/Au by e-beam evaporation. Ohmic contacts were formed by scribing down to the STN layer using diamond scriber and covering the scribed area with indium using a soldering gun. The same indium contacts were also put down on the area

without UID GaN growth formed by the MBE faceplate clip mark. The indium contacts were confirmed to be ohmic before each measurement. Figure 4.4 shows the schematic of the processed samples.

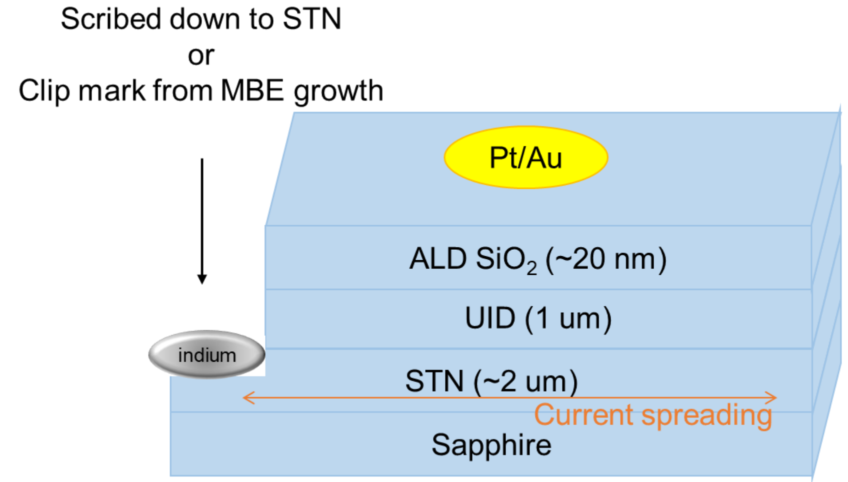
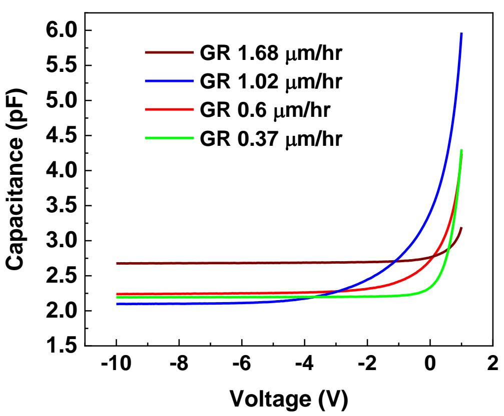


Figure 4.4 Schematics of processed sample used for CV measurements. Metal-insulator-semiconductor (MIS) structure was formed using ALD SiO_2 and Pt/Au.

CV measurements were done by Dr. Esmat Farzana as shown in the Figure 4.5. N_{net} increases linearly with the growth rate and was below 2×10^{16} /cm^3 for up to 1.7 μm/hr. We speculate this could be a sign of increased oxygen incorporation at higher growth rate. SIMS measurements from the last section did not show this trend possibly due to a lack of resolution since the oxygen levels in the layers of interests were very close to the background oxygen level. We are working on doing SIMS on the CV samples for more accurate results. Another speculation is that more V_N formed at higher growth rate due to the higher III/V ratio. More investigations are needed to further understand the increased carrier level.



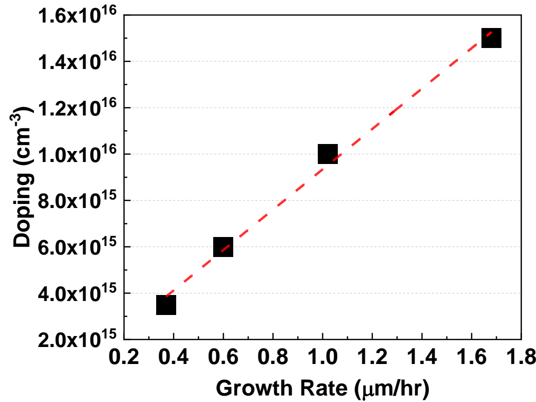


Figure 4.5 CV measurements of UID GaN grown at different growth rates. (a) Capacitance as a function of voltage. (b) Doping levels for different growth rate. Figure courtesy Dr. Esmat Farzana.

4.2.3 Morphology vs growth temperature by AFM

Two kinds of free-standing substrates were used for this study. The substrate manufactured by Lumilog Inc. had TDD of high 10^6 /cm^2. The susbtrate manufactured by Mistubishi Chemical Co. (MCC) had TDD of low 10^6 /cm^2. The emissivity of the Lumilog and MCC templates were calibrated using Al strip [3] to be 0.52. To achieve optimum morphology, 1 μm of UID GaN was grown on the MCC substrate at 0.6 μm/hr and at growth temperature of 800, 820, and 840 °C, respectively. Figure 4.6 shows the AFM images for the sample morphology. At 800 °C, smooth morphology was observed. At 820 and 840 °C, the sample surface shows "marks" and "pits", respectively. This indicates that a growth temperature of 800 °C results in the best morphology.

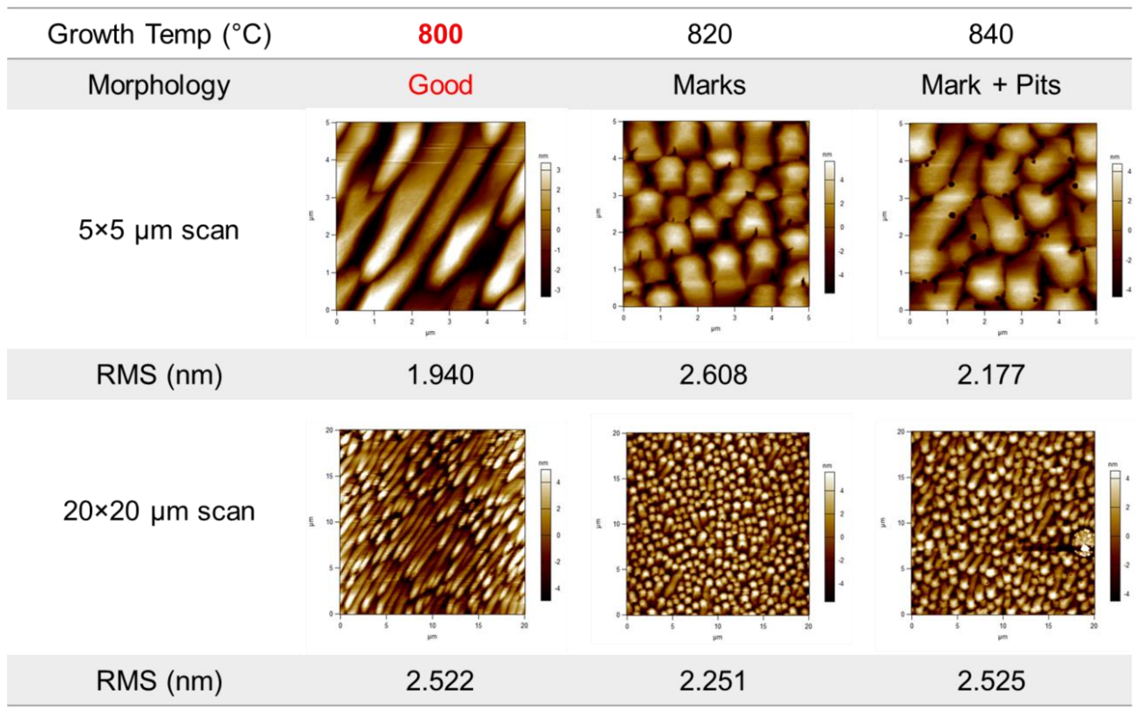


Figure 4.6 AFM of 1 µm of UID GaN grown on the MCC substrate at 0.6 µm/hr and at growth temperature of 800, 820, and 840 °C, respectively. Figure courtesy Kai Shek Qwah.

4.3 GaN p-n diode batch 1

The optimized n^- drift region condition and the high-quality p-GaN developed in Chapter 1 was used to grew batch 1 didoes. Figure 4.7 shows the schematic of the diode epi structure. The drift region thickness is 4 µm. Table 4.3 shows the type of templates and the growth conditions used for the diodes. The diodes were grown continuously except one of them had growth interrupt at the p-n junction interface. This was done by taking the samples out of the MBE after drift region growth, leaving the sample overnight in dry box, and loading the sample into the MBE for regrowth the next day. The interrupted diode was included to investigate the effect of impurity at regrowth interface. In the eventual device structure for this project, we hope to achieve GaN diode with buried p-region, and thus with regrowth involved. Figure 4.8

shows the AFM image (done by Clayton Qwah) for typical continuously grown diode. The morphology was smooth with no pits observed.

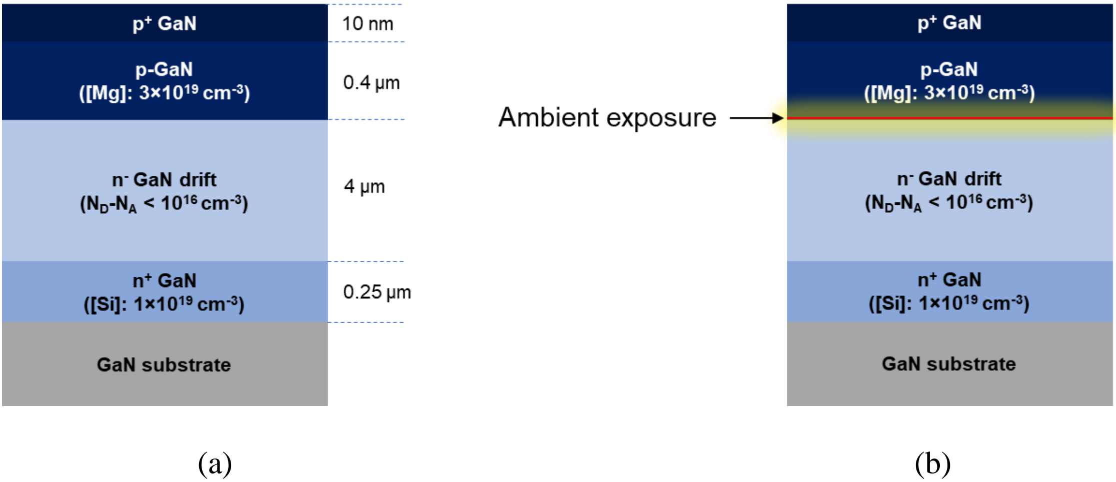


Figure 4.7 Schematic of the diode epi structure. The drift region was 4 µm thick. (a) Continuously grown diode. (b) Interrupted diode with ambient exposure at the p-n junction interface.

Table 4.3 Growth parameters and templates used for batch 1 diodes.

Template	Lumilog				MCC		
drift region growth rate (µm/hr)	0.6	1.02	1.68	0.6	0.6	1.4	1.4
drift region growth temp (°C)	820	820	820	800	800	800	800
continuous/ interrupted	C	C	C	C	C	C	interrupted at junction (taken out overnight)
AFM	Mark+pits	Good	Good	Good	Ok	Good	n-side: a few mark After p-side: rough

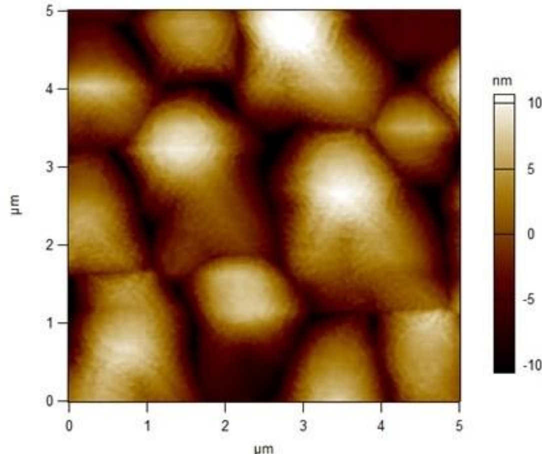
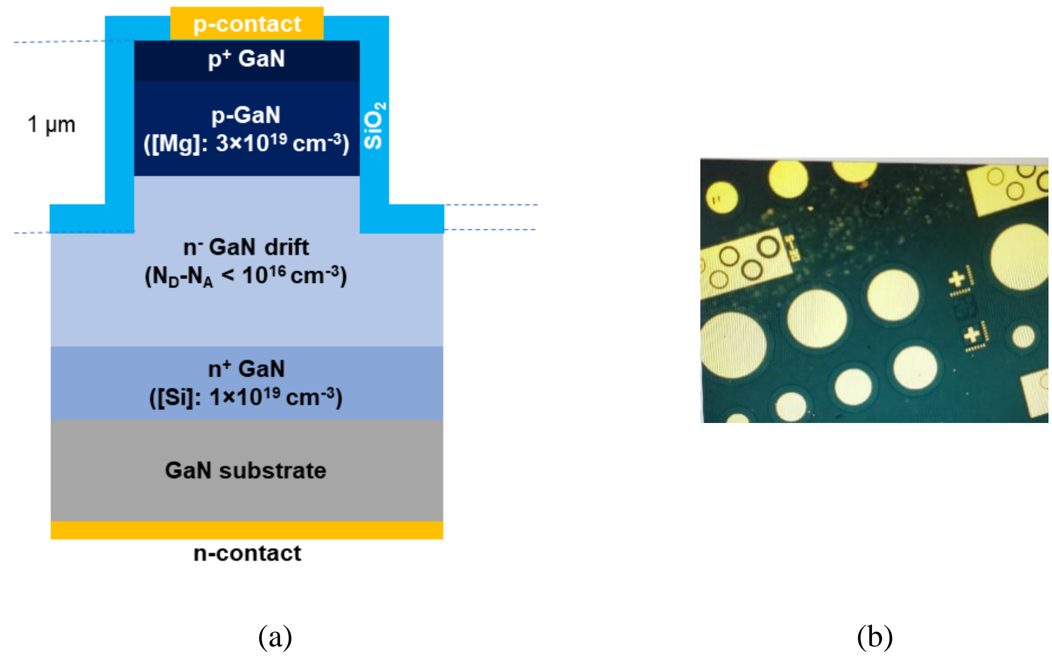


Figure 4.8 AFM image for typical continuously grown diode. The surface was smooth with no pits observed. Figure courtesy Kai Shek Qwah.

The diodes were processed into vertical structures as shown in Figure 4.9. The mesa was defined by RIE using $SiCl_4$. PECVD SiO_2 was used for sidewall passivation. Backside n-contacts were deposited using Ti/Au. Circular p-contacts were formed using Pd/Au. The diameter was 150-450 µm.



(a) (b)

Figure 4.9 Processed diode. (a) Schematics of the processed vertical GaN p-n diode. (b) Optical microscope image of the processed diode.

J-V performance of the diodes were measured by Jianfeng Wang and plotted by Dr. Morteza Monavarian, Jianfeng Wang, and Clayton Qwah. Typical forward J-V performance of batch 1 diodes is shown in Figure 5.10 (a) (b). The diode showed leakage in the voltage range of 1-2.8 V. The minimum specific on resistance (R_{on_sp}) was 1.77 mΩ·cm^2. The minimum ideality factor (n_{min}) was 1.73. The reverse J-V characteristics of the same devices is shown in Figure 4.11. The reverse breakdown voltage was 125 V.

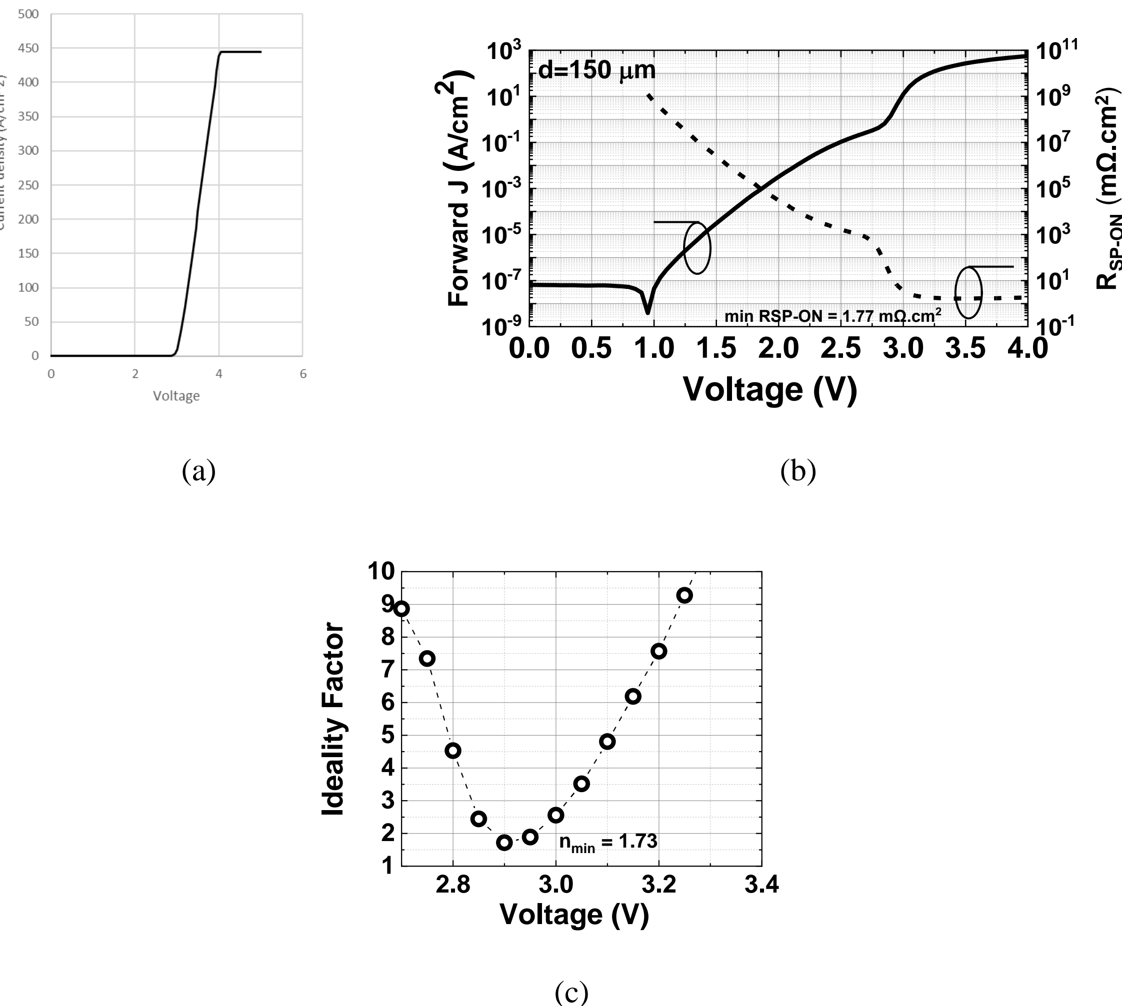


Figure 4.10 Typical forward J-V characteristics of batch 1 diodes in (a) linear and (b) log scale. (c) Ideality factor of the diode. Figure courtesy Dr. Esmat Farzana, Dr. Morteza Monavarian.

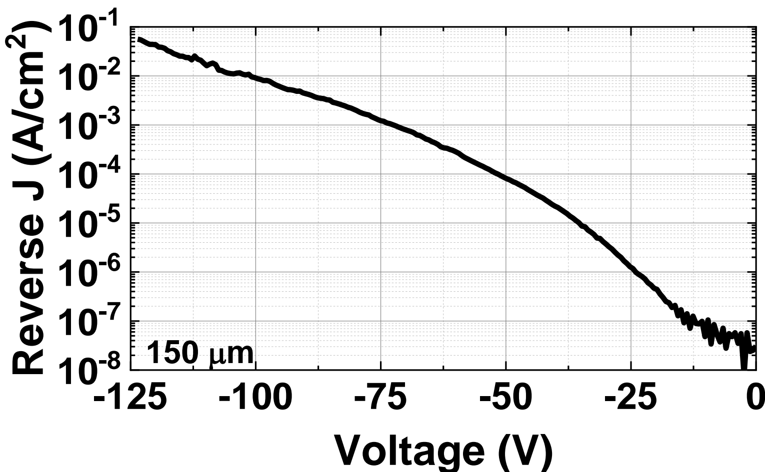


Figure 4.11 Reverse J-V characteristics of the diode. The reverse breakdown voltage was 125 V. Figure courtesy Dr. Esmat Farzana, Dr. Morteza Monavarian.

The electrical performance of the batch 1 diodes showed that further improvements were needed on both the growth side and the processing side.

Next, we compared the reverse voltage (V_{r_10}) for the diodes at a reverse current of -10 μA. Figure 4.12 shows the histogram of the reverse voltage value for the diodes with various diameter, growth condition, and grown with different substrates. One of the samples broke during processing and showed increased leakage as a result. The devices with smaller diameter showed better performance. This is probably due to the lower chance of having dislocation or sidewall-related defects due to smaller size. The diode samples grown at 800 °C had higher V_{r_10} compared to the ones grown at 820 °C. The samples grown at a growth rate range of 0.6-1.4 μm/hr all showed promising result.

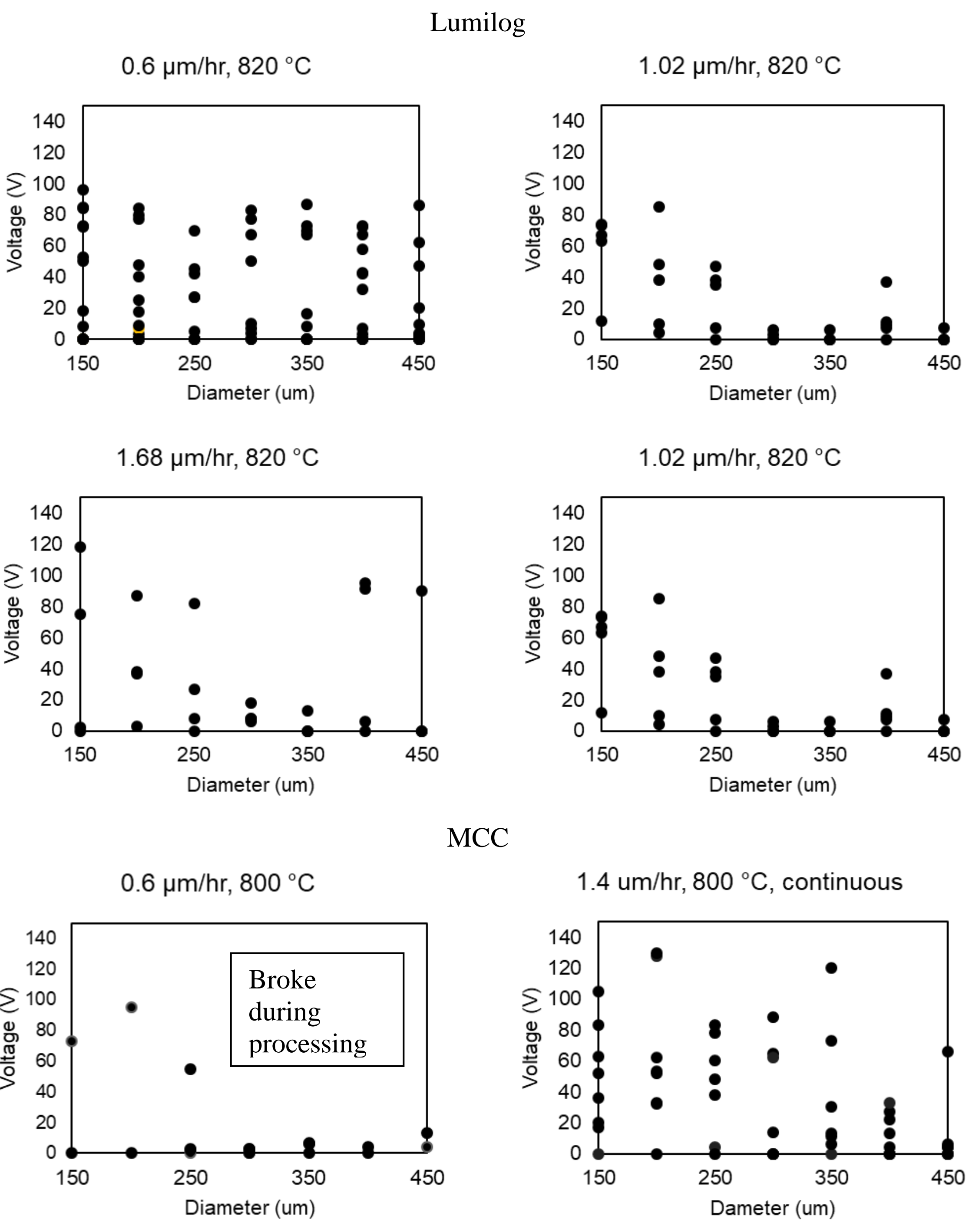


Figure 4.12 Histogram of reverse voltage (V_{r_10}) of the diodes when a reverse current of 10 µA was reached.

Similar comparison was done for diode samples grown with and without growth interruption (Figure 4.13). The interrupted diodes had much higher leakage than continuous diodes grown at the same condition. The V_{r_10} value was lower than 5 V for all devices tested.

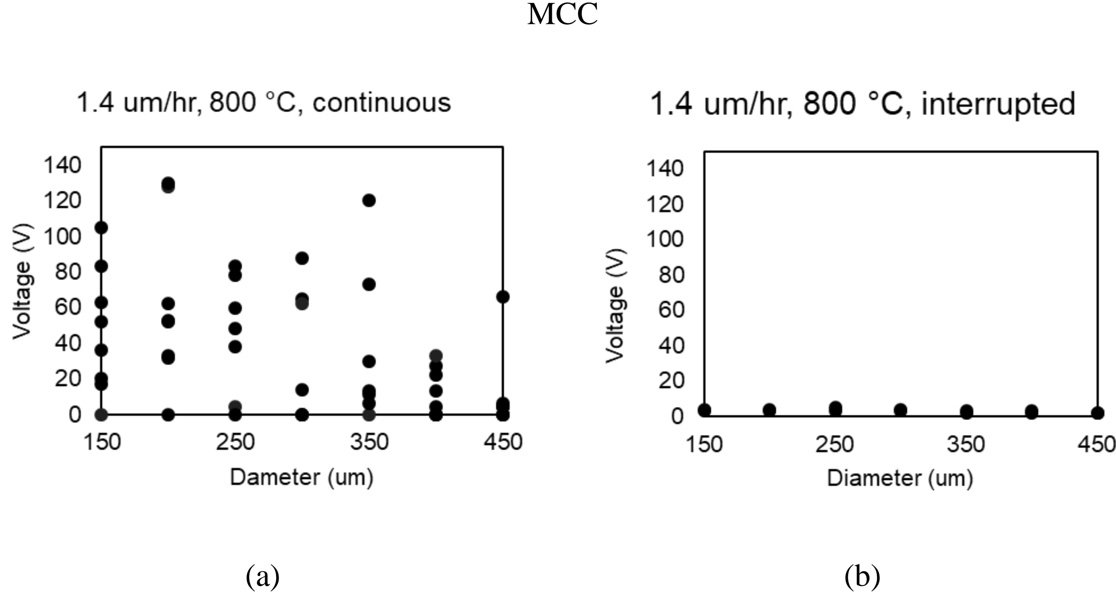


Figure 4.13 Comparison of V_{r_10} for (a) continuous and (b) interrupted diode.

4.4 GaN p-n diode batch 2

To further improve the diode performance, several optimizations was made. First, improved substrate cleaning procedure was done before samples growth to avoid contamination. Negative photoresist (PR) was used to protect the sample surface during dicing. Acetone, isopropanol sonication was done to remove the PR after dicing. In addition, piranha and BHF was used to further clean the surface. The samples were protected with fresh glass slides during backside metal deposition. The samples were also vacuum sealed and taken out of the package immediately before loading into the MBE. The samples without the improved cleaning showed

crater-like defect after growth as shown in Fig 4.14. No such defects were observed with the improved cleaning procedure.

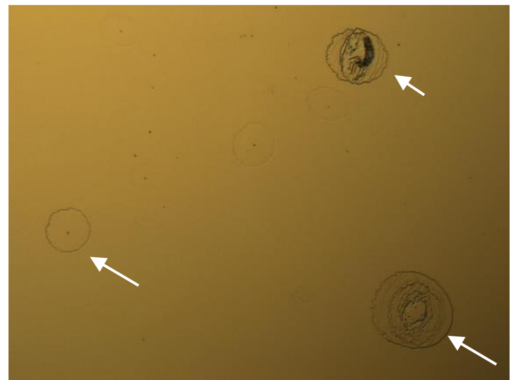


Figure 4.14 Samples grown without the improved cleaning procedure showed dust and crater-like defect after growth. Figure courtesy Dr. Morteza Monavarian.

Second, we used the optimized growth condition. A growth temp of 800 °C was used. AlGaN-involving growths were done before the diode growths unintentionally. Al getters oxygen in the growth environment and possibly reduced the impurity levels in the diode samples. Two continuous diode samples were grown using quarters of 2-inch substrates. The one grown on Lumilog substrate was grown at 0.6 µm/hr. The one grown on MCC substrate was grown at 1.4 µm/hr. The diode epi structure was the same as shown in Figure 4.7.

Third, the processing procedures and device structure were improved as shown in Fig 4.15. The processing was done by Dr. Esmat Farzana. The mesa was defined using Cl_2/BCl_3, resulting in beveled mesa of ~ 55°. The sidewall was treated with KOH after etching and passivated with Al_2O_3 deposited by ALD and Si_3N_4 deposited by PECVD.

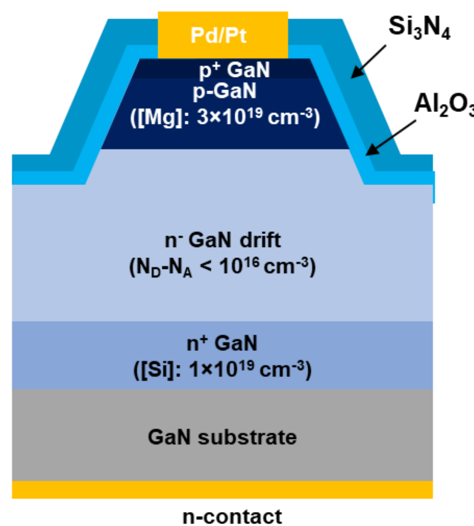
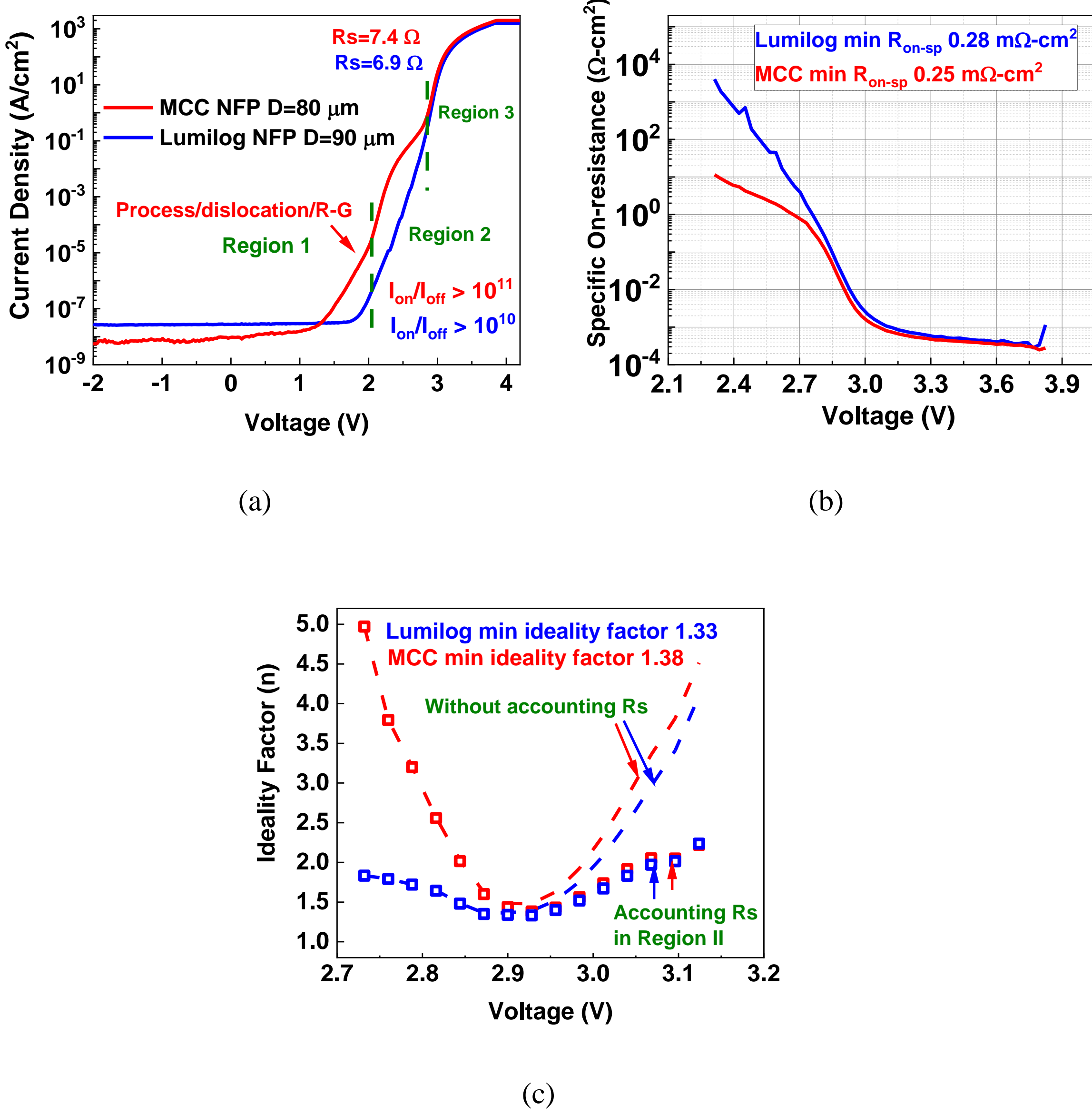


Figure 4.15 Schematics of batch 2 diodes after processing.

J-V performance of batch 2 diodes were measured by Dr. Esmat Farzana and plotted by Dr. Esmat Farzana and Dr. Morteza Monavarian. Typical forward J-V performance of batch 2 diodes is shown in Figure 4.16. The diode grown on MCC substrate showed leakage in the voltage range of 1-2.8 V. . The minimum ideality factor (n_{min}) was 1.38 and 1.33, the minimum specific on resistance (R_{on_sp}) was 0.25 and 0.28 $m\Omega \cdot cm^2$ for diodes grown on MCC and Lumilog substates, respectively.



(a) (b)

(c)

Figure 4.16 Batch 2 diode performance in forward bias. (a) J-V characteristics in log scale. (b) Specific on-resistance. (c) Ideality factor. Figure courtesy Dr. Esmat Farzana, Dr. Morteza Monavarian.

The reverse J-V characteristics of batch 2 diodes is shown in Figure 4.17. The reverse breakdown voltage was over 1000 V (detection limit of the instrument used to test the devices). The leakage current was found to be dominated by tool-related leakage. Progress are on-going

to assemble test setup with more accurate measurement of the leakage current and higher voltage range.

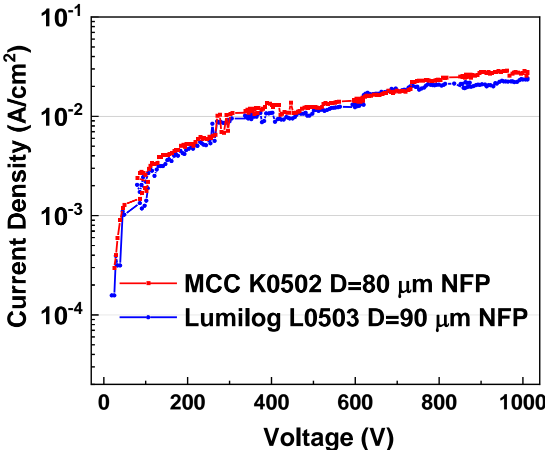


Figure 4.17 Batch 2 diode performance in reverse bias. The leakage current was found to be dominated tool-related leakage. Both samples showed breakdown voltage over 1000 V (highest voltage of the instrument used for testing). Figure courtesy Dr. Esmat Farzana, Dr. Morteza Monavarian.

Figure 4.18 made by Dr. Esmat Farzana compares the batch 2 diode performance achieved in this study to the results reported in literature [4–6]. Although only 4 μm of drift region was used, and the diodes didn't reach breakdown yet, the result is comparable to some of the best values reported and agrees with a drift region impurity range of mid 10^{15} /cm^3.

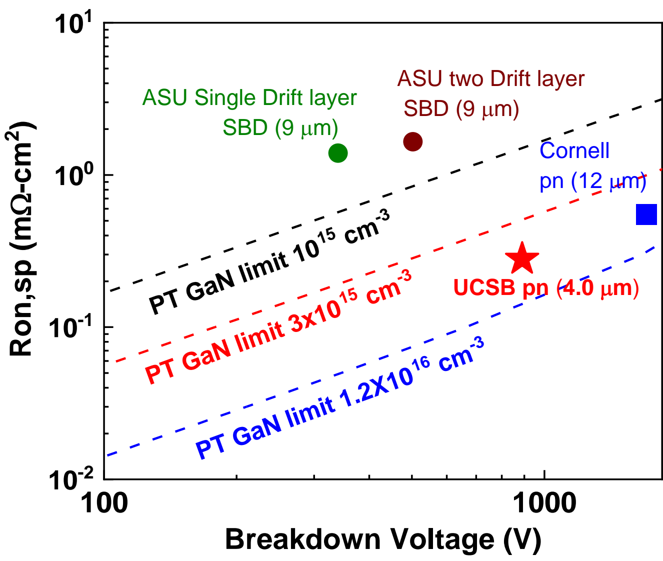


Figure 4.18 Comparison of the diode performance achieved in this study and reported in literature. Note the diode in this study had thinner (4 μm) drift region and didn't reach breakdown. Figure courtesy Dr. Esmat Farzana.

4.5 SIMS and CV analysis of batch 1 and 2 diodes

To investigate what caused the difference in device performance between the samples, SIMS were done by Zachary Biegler and Dr. Tom Mates. CV measurements were done by Dr. Esmat Farzana. Table 4.4 summarize the results. Samples grown with the same growth conditions (continuous growth, drift region growth temperature=800 °C) were compared.

Table 4.4 SIMS and CV measurements of the diode samples. Data courtesy Dr. Esmat Farzana, Dr. Tom Mates, Zachary Biegler.

Substrate	Drift region growth rate (μm/hr)	N_{net}=N_A-N_D by CV (/cm^3)		[O] by SIMS (/cm^3)	
		Batch #1	Batch #2	Batch #1	Batch #2
Lumilog	0.6	1×10^{16}	3×10^{15}	N/A	2×10^{16}
MCC	1.4	2-3×10^{16}	1×10^{16}	N/A	3×10^{16}

The lowest carrier concentration measured in the diodes were 3×10^{15} /cm^3. The samples grown on MCC substrates had higher N_{net} and O concentration than the ones grown on Lumilog substrates. Since MCC substrates have lower TDD, the inferior performance was speculated to be a result of the higher drift region growth rate. This agrees with the CV results discussed in Chapter 4.2.2. The higher growth rate was associated with higher Ga cell operating temperature. After each NH_3 recovery, the cells were dumped at a certain temperature to release the impurities absorbed by the charge material during recovery. This the temperature is ideally sufficiently higher than the highest operation temperature of the cells during growth. The dump temperature used before the diode growths might not be high enough. However, if the dump temperature is too high, the cells will be depleted quickly.

The batch 1 diode samples had higher N_{net} and O concentration than the batch 2 diode samples. Since all the other growth parameters used were the same. The improved performance was speculated to be a result of the AlGaN growth done before batch 2 diode growths. The Al gettered oxygen and lowered the impurity concentrations.

4.2 Conclusion

High quality UID GaN with low impurity level was developed for n^- diode drift region. The C, H, and O level and the net carrier concentration was measured for different growth rates. The surface morphology was optimized by changing the growth temperature. Two batches of diodes with drift region thickness of 4µm were demonstrated. Batch 1 diode showed that a drift region growth temperature of 800 °C resulted in the lowest leakage. Batch 2 diode with improved surface cleaning, growth condition, and device structure showed minimum low

ideality factor of 1.33, minimum specific on-resistance of 0.25 $m\Omega \cdot cm^2$, and reverse breakdown voltage of over 1000 V. The lowest net carrier concentration measured in the diodes were 3×10^{15} /cm^3.

References

1. C. A. Robertson, K. S. Qwah, Y.-R. Wu, and J. S. Speck, "Modeling dislocation-related leakage currents in GaN p-n diodes," Journal of Applied Physics **126**, 245705 (2019).
2. J. K. Sheu, M. L. Lee, and W. C. Lai, "Effect of low-temperature-grown GaN cap layer on reduced leakage current of GaN Schottky diodes," Appl. Phys. Lett. **86**, 052103 (2005).
3. B. M. McSkimming, F. Wu, T. Huault, C. Chaix, and J. S. Speck, "Plasma assisted molecular beam epitaxy of GaN with growth rates > 2.6µm/h," Journal of Crystal Growth **386**, 168–174 (2014).
4. H. Fu, X. Huang, H. Chen, Z. Lu, I. Baranowski, and Y. Zhao, "Ultra-low turn-on voltage and on-resistance vertical GaN-on-GaN Schottky power diodes with high mobility double drift layers," Appl. Phys. Lett. **111**, 152102 (2017).
5. Z. Hu, K. Nomoto, M. Qi, W. Li, M. Zhu, X. Gao, D. Jena, and H. G. Xing, "1.1-kV Vertical GaN p-n Diodes With p-GaN Regrown by Molecular Beam Epitaxy," IEEE Electron Device Letters **38**, 1071–1074 (2017).
6. H. Fu, K. Fu, S. R. Alugubelli, C.-Y. Cheng, X. Huang, H. Chen, T.-H. Yang, C. Yang, J. Zhou, J. Montes, X. Deng, X. Qi, S. M. Goodnick, F. A. Ponce, and Y. Zhao, "High Voltage Vertical GaN p-n Diodes With Hydrogen-Plasma Based Guard Rings," IEEE Electron Device Letters **41**, 127–130 (2020).

Chapter 5 Summary and future work

5.1 All MBE tunnel junctions for visible applications (on-going work)

5.1.1 Introduction

Hybrid tunnel junctions (TJs) have yielded some of the lowest voltage penalty in the literature [1,2], so does selective area regrowth method [3] which also put the regrowth interface at the junction between the n^{++} and p^{++} layers. However, this regrowth interface is exposed to air during the process and has impurity incorporation. Although surface cleaning procedure such as HF cleaning [1] can reduce the impurity levels at this interface, the amount and species of impurity incorporated at the interface is still not as controllable as if the two layers were grown consecutively in the same growth run [4,5]. For the purpose of understanding the mechanism of TJ, it is thus of great interested to investigate non-hybrid TJ. To combine MOCVD and MBE's advantage as stated in the last chapter, all MBE TJs were formed on top of commercial MOCVD blue LED wafers starting with p-GaN regrowth. This method also provides us with the ability to control the p-side doping in the TJ. The impurities

at the regrowth interface is buried with p-GaN regrowth. The high dopant concentration (N_D) in p-GaN, deplete the impurities within nanometers [5].

An InGaN interlayer is used in TJ to reduce the voltage and increase tunneling current [5–10]. The polarization charge reduces the tunneling distance, the lower bandgap energy of InGaN also lowers the tunneling barrier. The growth of InGaN by NH_3 MBE is limited by the low decomposition temperature of InGaN (~610 °C) [11] and high pyrolysis temperature of NH_3 (complete at 650 °C) [12]. Increased NH_3 overpressure will suppress the thermal decomposition of nitride films and is thus used during InGaN growth by NH_3 MBE [13].

5.1.2 Growth of InGaN by NH_3 MBE as interlayers

Since the growth of InGaN is sensitive to temperature, the calibration samples were grown using templates with Ti/Pd/Ti coating of 50/500/5 nm. InGaN calibration samples were grown on GaN on sapphire templates. One template had Ti/Pt/Ti coating while the other one didn't. The two templates were coloaded on Si wafer by indium bonding. The growth was done at 605 °C with Ga flux of 6.87×10^{-8} torr and In flux of 4.80×10^{-8} torr. Figure 5.1 shows the ω-2θ scan of the (002) peak for the InGaN calibration samples. The one grown on template with backside metal coating have an In content of 6.0% and a growth rate of 106 nm/hr while the one without have an In content of 6.4% and a growth rate of 107 nm/hr. The <1% composition difference for the two samples indicates that the temperature for coloaded sample were almost the same. Growths done at similar conditions showed that a 15 °C difference in growth temperature led to ~3% difference in In%.

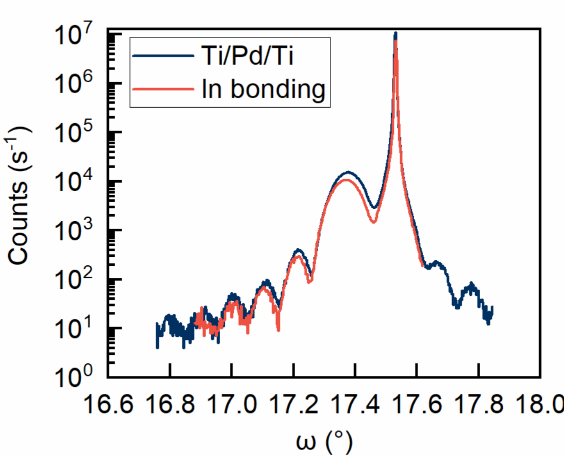


Figure 5.1 ω-2θ scan for InGaN sample coloaded by indium-bonding during growth. The sample with backside coating had In%=6.0% while the one without backside coating had In%=6.4%. In growth rate for the two samples were 106 and 107 nm/hr, respectively.

Thus, it is reliable to use the pyrometer temperature reading of a sample with the backside metal coating as the growth temperature for all the samples coloaded with it. Growth was also done using indium-bonded sample only and was unsuccessful, indicating that the pyrometer reading for indium-bonded sample without backside metal coating is unreliable.

5.1.3 Experimental details for developing all MBE tunnel junction blue LEDs

The MBE regrowth was done on commercial MOCVD grown blue LED wafer. The wafer were activated in-situ in the MOCVD reactor after growth. Before regrowth, the wafer was diced into 1cm × 1 cm squares, cleaned with isopropanol and acetone, and then dipped in buffered HF (BHF) for 1min. The samples were vacuum sealed and taken out of the vacuum package immediately prior to indium-bonding on to silicon wafers and transferring into the MBE. The samples were baked at 400 °C for 1 hour in vacuum in the MBE before growth.

The regrowth was done in a Veeco 930 MBE with NH_3 as the nitrogen source and solid effusion cells for Ga and Si. A Riber valved Mg cell was used with Mg flux controlled by the valve opening. Reflection high-energy electron diffraction (RHEED) was used to monitor the sample surface morphology in real time. The growth temperature was monitored by a calibrated pyrometer. A GaN on sapphire sample with Ti/Pd/Ti backside coating on the back was used to facilitate the temperature measurement. A 200 sccm NH_3 flow was used during non-InGaN growth while 500 sccm flow was used for InGaN-related growth. The NH_3 overpressure (below 10^{-5} Torr) was low enough to prevent hydrogen re-passivation of the p-type layers. The n-GaN growth rates were calibrated using high-resolution x-ray diffraction. The doping densities were calibrated using Hall measurements or secondary ion mass spectrometry (SIMS).

To investigate the effect of using InGaN interlayer, two series of sample were grown. Series A had GaN regrowth only while series B had InGaN involved in the regrowth. Four regrowth conditions were done for each series. Condition 1: n-side TJ regrowth. This provide us with a comparison between all MBE TJ and hybrid TJ. Condition 2: p-type regrowth. The voltage comparison between condition 2 samples and the standard sample processed with ITO indicates the voltage drop on the p-regrowth region of the all MBE TJ. Condition 3: all MBE TJ with BHF cleaning (1 min dip) done at the tunnel junction interface. These samples provide information about how the impurities at the junction affect the LED performance. Condition 4: continuously grown all MBE TJ. Figure 5.2 shows the schematic of the LED structures.

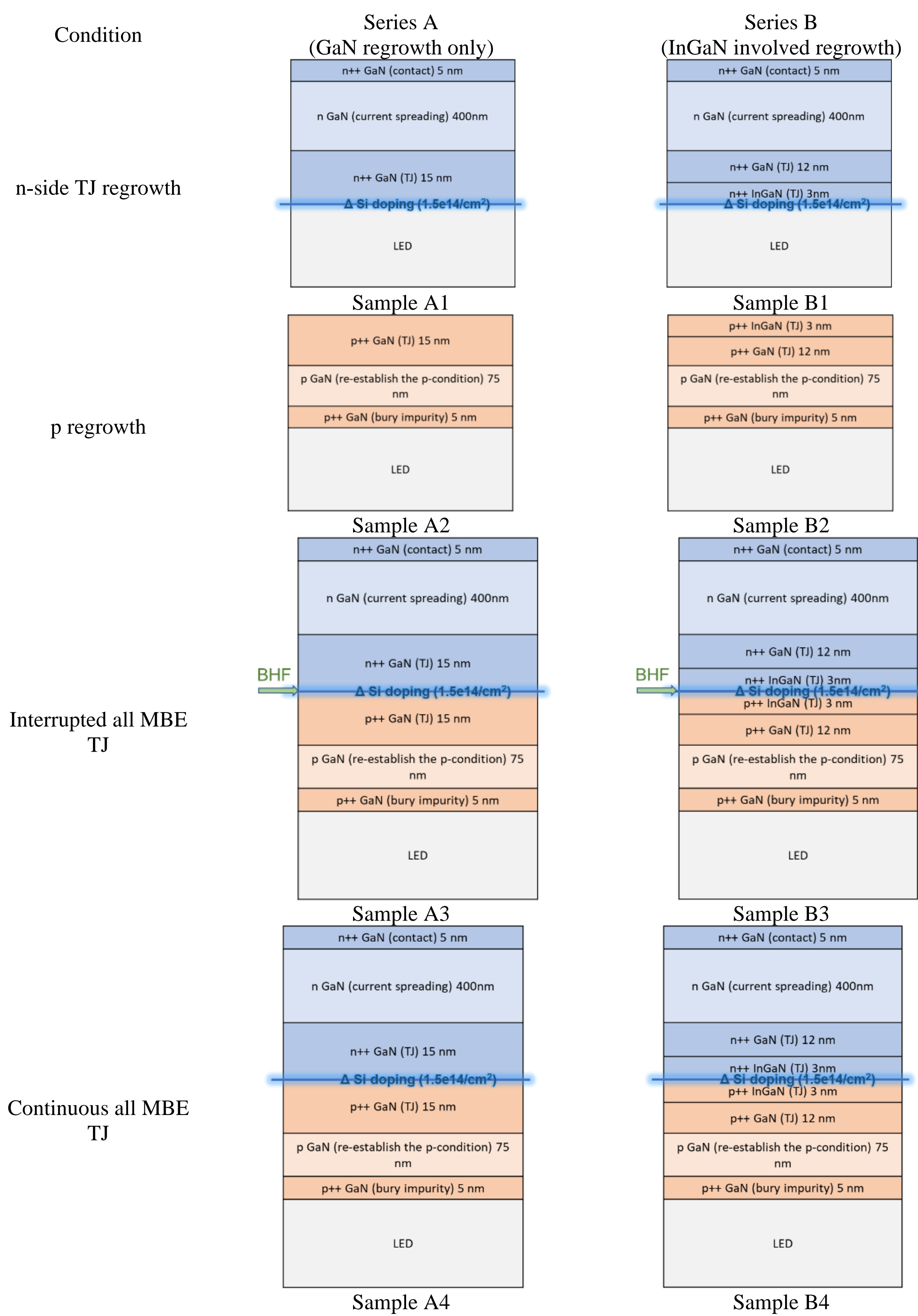


Figure 5.2 Schematic of the regrowth LEDs' epitaxial structure.

The regrowth condition for sample B4 is explained here as representative for the regrowth condition since it contains all layers involved in the regrowth for all samples. The Mg-doped GaN layers were grown at 760 °C with an In flux of 1.5×10^{-7} torr as a surfactant [14]. Mg valve opening for the lower, middle, and Mg-doped layers were 100%, 49%, and 100%, respectively, targeting the Mg concentrations of 7×10^{19} , 2×10^{19} , and 3×10^{20} cm^{-3}. The growth rate was 320, 320, and 76 $nm\cdot hr^{-1}$. The p-GaN layer had a hole concentration of 3.5×10^{17} cm^{-3}, a resistivity of 1.25 $\Omega\cdot cm$, and a mobility of 14 $cm^2\cdot V^{-1}\cdot S^{-1}$ as determined by Hall measurements. InGaN layers were grown at 605 °C at a growth rate of 106 $nm\cdot hr^{-1}$ with a In composition of 6%. The InGaN layer was coherent with respective to the GaN layers. Mg-doped InGaN were grown with Mg valve opening of 100%, targeting a Mg concentration of 2×10^{20} cm^{-3}). A Si-δ-doped layer was grown targeting a surface concentration of ~1.5×10^{14} cm^{-2} , or approximately 13% of a monolayer. The growth was done by keeping the Si shutter open and the Ga shutter closed, during which the NH_3 flow was kept at 200 sccm. The growth temperature was kept at 605 °C for samples with Mg-doped InGaN and 700 °C for samples without Mg-doped InGaN. The Si-doped InGaN layer were grown with Si cell at 1435 °C, targeting a Si concentration of 1.8×10^{20} cm^{-3}. The n^{++} GaN layers were grown with Si cell temperature of 1435, 1420, and 1420 °C, at a growth rate of 76, 370, and 76 $nm\cdot hr^{-1}$, targeting Si concentrations of 2.6×10^{20}, 3×10^{19}, and 1.5×10^{20} cm^{-3}. The growth of the lower n^{++} GaN layer were initiated at 605 °C and acted as a "capping layer" for InGaN to prevent InGaN desorption. After 2 nm of growth, the growth temperature was ramped up to 700 °C. The BHF cleaning at the junction interface for sample A3 and B3 were done by taking the sample with p-side regrowth out of the MBE chamber and dipping it in BHF for 1 min. Then, the sample is vacuum sealed and taken out of the vacuum

package immediately prior to indium-bonding on to silicon wafers and transferring into the MBE again.

Process are on-going to characterize the samples, process the samples into LEDs and measure their electrical and optical performance.

5.1.4 Initial Results

Electroluminescence (EL) measurement of the LED wafers using indium dots (50 μm in diameter) showed emission for all samples. The emission wavelength was around 450 nm, which confirmed non-equilibrium hole injection through the TJ structure into the LED active region. Process are on-going to further characterize the samples, process the samples into LEDs and measure their electrical and optical performance.

5.2 Summary and future work

In this dissertation, III-nitride tunnel junctions and p-n diodes were developed using ammonia-assisted molecular beam epitaxy. High quality p-GaN was grown using a valved Mg cell. InGaN/GaN superlattice was shown to reduce the impurity concentration and improve the conductivity. A wide doping range was achieved, satisfying the desired Mg level for various applications. H_2 incorporation in GaN:Mg grown using high NH_3 flux was demonstrated. The GaN:Mg can be activated using high temperature annealing, leading to improved conductivity.

Hybrid tunnel junctions were studied for its use in visible applications. Blue hybrid tunnel junction LED with record low excess voltage showed the potential of using TJ in commercial devices. The applications of hybrid TJ in UV emitters were also studied. This was done by the development of highly doped n-AlGaN with low resistivity. All MBE tunnel junctions are being studied for its use in visible applications.

Lastly, vertical GaN p-n diodes with low leakage and high reverse breakdown was developed. The low impurity level drift region was achieved by optimizing the growth rate and growth temperature using SIMS, CV, and AFM. Combined with the high-quality p-GaN and improved device structure, GaN p-n diode with breakdown voltage of over 1000 V was achieved.

Moving forward, there are many things that can be done to further each part of this work. For applications of TJ in the visible range, we can compare the use of hybrid TJ and all MBE TJ, therefore understanding the effect of regrowth interface impurities and its location. For UV TJ, we need to do temperature-controlled Hall measurement to measure the N_A and N_D levels in n-AlGaN. We also need to lower the excess voltage by epi structure optimization and

improve the yield by having larger devices size, improving flip chip yield, etc. The use of interlayers is of interests to both TJ applications.

As for GaN p-n diodes, there are things that can be done on both the growth side and cleaning/processing side. On the growth side, thicker drift region is needed to achieve high breakdown voltage. Using a faster growth rate will greatly ease the growth if there's no increased impurity incorporation. This can be enabled by the use of large volume Ga cell. Graphite crucible can be baked at extremely high temperature compared to PBN crucible and should be used for the Ga cell. In the eventual device, buried p-region will be involved, thus the diode structure will contain regrowth interface. Si has been a major concern with regrowth interface. Having Si spike will greatly lower the breakdown voltage of the diode. Investigations are needed to remove the Si.

References

1. E. C. Young, B. P. Yonkee, F. Wu, S. H. Oh, S. P. DenBaars, S. Nakamura, and J. S. Speck, "Hybrid tunnel junction contacts to III–nitride light-emitting diodes," Appl. Phys. Express **9**, 022102 (2016).
2. B. P. Yonkee, E. C. Young, S. P. DenBaars, S. Nakamura, and J. S. Speck, "Silver free III-nitride flip chip light-emitting-diode with wall plug efficiency over 70% utilizing a GaN tunnel junction," Appl. Phys. Lett. **109**, 191104 (2016).
3. P. Li, H. Zhang, H. Li, M. Iza, Y. Yao, M. S. Wong, N. Palmquist, J. S. Speck, S. Nakamura, S. Nakamura, S. P. DenBaars, and S. P. DenBaars, "Size-independent low voltage of InGaN micro-light-emitting diodes with epitaxial tunnel junctions using selective area growth by metalorganic chemical vapor deposition," Opt. Express, OE **28**, 18707–18712 (2020).
4. M. Malinverni, J.-M. Lamy, D. Martin, E. Feltin, J. Dorsaz, A. Castiglia, M. Rossetti, M. Duelk, C. Velez, and N. Grandjean, "Low temperature p-type doping of (Al)GaN layers using ammonia molecular beam epitaxy for InGaN laser diodes," Applied Physics Letters **105**, (2014).
5. S. Krishnamoorthy, F. Akyol, and S. Rajan, "InGaN/GaN tunnel junctions for hole injection in GaN light emitting diodes," Appl. Phys. Lett. **105**, 141104 (2014).
6. S. Krishnamoorthy, F. Akyol, P. S. Park, and S. Rajan, "Low resistance GaN/InGaN/GaN tunnel junctions," Appl. Phys. Lett. **102**, 113503 (2013).
7. S. Krishnamoorthy, P. S. Park, and S. Rajan, "Demonstration of forward inter-band tunneling in GaN by polarization engineering," Appl. Phys. Lett. **99**, 233504 (2011).
8. X. Yan, W. Li, S. M. Islam, K. Pourang, H. (Grace) Xing, P. Fay, and D. Jena, "Polarization-induced Zener tunnel diodes in GaN/InGaN/GaN heterojunctions," Appl. Phys. Lett. **107**, 163504 (2015).
9. S. Krishnamoorthy, D. N. Nath, F. Akyol, P. S. Park, M. Esposto, and S. Rajan, "Polarization-engineered GaN/InGaN/GaN tunnel diodes," Appl. Phys. Lett. **97**, 203502 (2010).
10. A. J. Mughal, E. C. Young, A. I. Alhassan, J. Back, S. Nakamura, J. S. Speck, and S. P. DenBaars, "Polarization-enhanced InGaN/GaN-based hybrid tunnel junction contacts to GaN p–n diodes and InGaN LEDs," Appl. Phys. Express **10**, 121006 (2017).
11. H. Saitoh, W. Utsumi, H. Kaneko, and K. Aoki, "The phase and crystal-growth study of group-III nitrides in a 2000°C at 20GPa region," Journal of Crystal Growth **300**, 26–31 (2007).
12. S. Mukherjee, S. V. Devaguptapu, A. Sviripa, C. R. F. Lund, and G. Wu, "Low-temperature ammonia decomposition catalysts for hydrogen generation," Applied Catalysis B: Environmental **226**, 162–181 (2018).
13. J. R. Lang and J. S. Speck, "NH_3-rich growth of InGaN and InGaN/GaN superlattices by NH_3-based molecular beam epitaxy," Journal of Crystal Growth **346**, 50–55 (2012).
14. E. C. H. Kyle, S. W. Kaun, E. C. Young, and J. S. Speck, "Increased p-type conductivity through use of an indium surfactant in the growth of Mg-doped GaN," Appl. Phys. Lett. **106**, 222103 (2015).

Appendices

Appendix A. Examples of ammonia MBE growth recipes

A.1 SIMS stack for Si doping

```
title ( SIMS for Si doping level )
temp Ga1Base 893
temp Ga1Tip 1093
temp Ga2Base 800
temp Ga2Tip 1000
temp Si 1300
temp InBase 708
temp InTip 808
! ----------a Marker Layer --------------
open In
open Ga1
wait 1:18
close In
! ========Bottom UID=========
wait 25:58
! ----------b Marker Layer --------------
open In
wait 1:18
close In
! ========1. n- layer : Si @ 1300 C
========
open Si
wait 25:58
close Si
temp Si 1435
! ----------c Marker Layer --------------
open In
wait 1:18
close In
! UID until Si stabilises
waitop
! ========2. n+layer : Si @ 1435 C
========
open Si
wait 25:58
close Si
! ----------d Marker Layer --------------
open In
wait 1:18
close In
! ======== Middle UID  ========
wait 25:58
! ----------e. Marker Layer --------------
open In
wait 1:18
close In
! ========3.  n++ layer : Si @ 1435
========
close Ga1
open Ga2
open Si
wait 21:26
close Si
close Ga2
open Ga1
! ----------f. Marker Layer --------------
open In
wait 1:18
close In
! ======== Top UID  ========
wait 25:58
temp sub 100
ramprate sub 150
writevalue NH3 50
waituntil (100 < sub < 450)
ramprate sub 60
writevalue NH3 0
```

A.2 All MBE tunnel junctions with InGaN interlayer

```
title ( 062720AA_all MBE TJ on LED)
! temp 760C
! Ga1 915/1115
! Ga2 826/1026
```

```
! In 766/866 (1.5e-7)
! Si 1435
writevalue NH3 200
! ==============1. p+GaN============
writevalue MgValveSetpoint 100
wait 10
open Ga1
open Mg
open In
wait 56
! ==============2. p GaN============
writevalue MgValveSetpoint 49
wait 14:04
close Ga1
temp Ga1Base 922
temp Ga1Tip 1122
! ==============3. p++GaN============
writevalue MgValveSetpoint 100
open Ga2
wait 9:28
close Mg
close In
close Ga2
! ==============4.
p++InGaN============
temp sub 760
temp Ga2Base 850
temp Ga2Tip 1050
temp InBase 730
temp InTip 830
waitop
! temp 608
writevalue NH3 500
waitop
open Ga2
open In
open Mg
wait 1:41
close Mg
close In
close Ga2
writevalue MgValveSetpoint 30
! ==============5. delta Si============
writevalue NH3 200
waitop
open Si
wait 5:18
close Si
! ==============6.
n++InGaN============
writevalue NH3 500
waitop
open In
open Ga2
open Si
wait 1:41
close In
close Ga2
close Si
! ===============7 n++ GaN
cap============
temp Ga2Base 826
temp Ga2Tip 1026
writevalue NH3 200
waitop
open Ga2
open Si
wait 1:35
close Ga2
close Si
! ==============8. n++
GaN============
temp sub 760
writevalue NH3 200
waitop
! temp 700 on In sample
open Ga2
open Si
wait 7:53
close Ga2
close Si
! ==============9. n GaN============
temp Si 1420
open Ga1
open Si
wait 1:4:52
close Ga1
close Si
! ==============10. n++
GaN============
open Ga2
open Si
wait 3:57
close Ga2
close Si
! ==============end============
writevalue NH3 50
ramprate sub 150
temp sub 100
waituntil (100 < sub < 450) 1
writevalue NH3 0
ramprate sub 60
waitop
! home Mg
```

A.3 Continuous vertical diode

```
title (Diode for Arpa-E_UID 1020nm/hr)
! Ga1 905/1105 Si 1435 In 550/650
! Ga2 907/1107
! Mg home
! 820C, Lumilog FS, e=0.59
writevalue NH3 200
!                              ==============n+
layer================
open Ga1
open Si
wait 40:32
close Ga1
close Si
temp Si 300
!                              =============UID
layer=================
temp Ga1Base 934
temp Ga1Tip 1134
wait 2:00
open Ga1
open Ga2
wait 3:55:18
close Ga1
close Ga2
!                               ==============p
layer==================
temp Ga1Base 905
temp Ga1Tip 1105
temp Ga2Base 844
temp Ga2Tip 1044
temp InBase 716
temp InTip 816
waitop
! adjust temp to 750C
! make sure Ga1 and In cell reach temp
writevalue MgValveSetpoint 55
wait 10
open Ga1
open Mg
open In
wait 1:4:52
close Ga1
close Mg
close In
!                               ============p++
layer=================
writevalue MgValveSetpoint 100
wait 10
open Ga2
open Mg
open In
wait 5:00
close Ga2
close Mg
close In
!
=================END=============
==
writevalue MgValveSetpoint 50
temp Ga1Base 250
temp Ga1Tip 300
temp Ga2Base 250
temp Ga2Tip 300
temp InBase 250
temp InTip 300
temp Si 300
temp sub 100
ramprate sub 150
writevalue NH3 50
waituntil (100 < sub < 450)
ramprate sub 60
writevalue NH3 0
waitop
```

Appendix B. Calibrations for NH_3 MBE growths

B.1 Emissivity calibrations

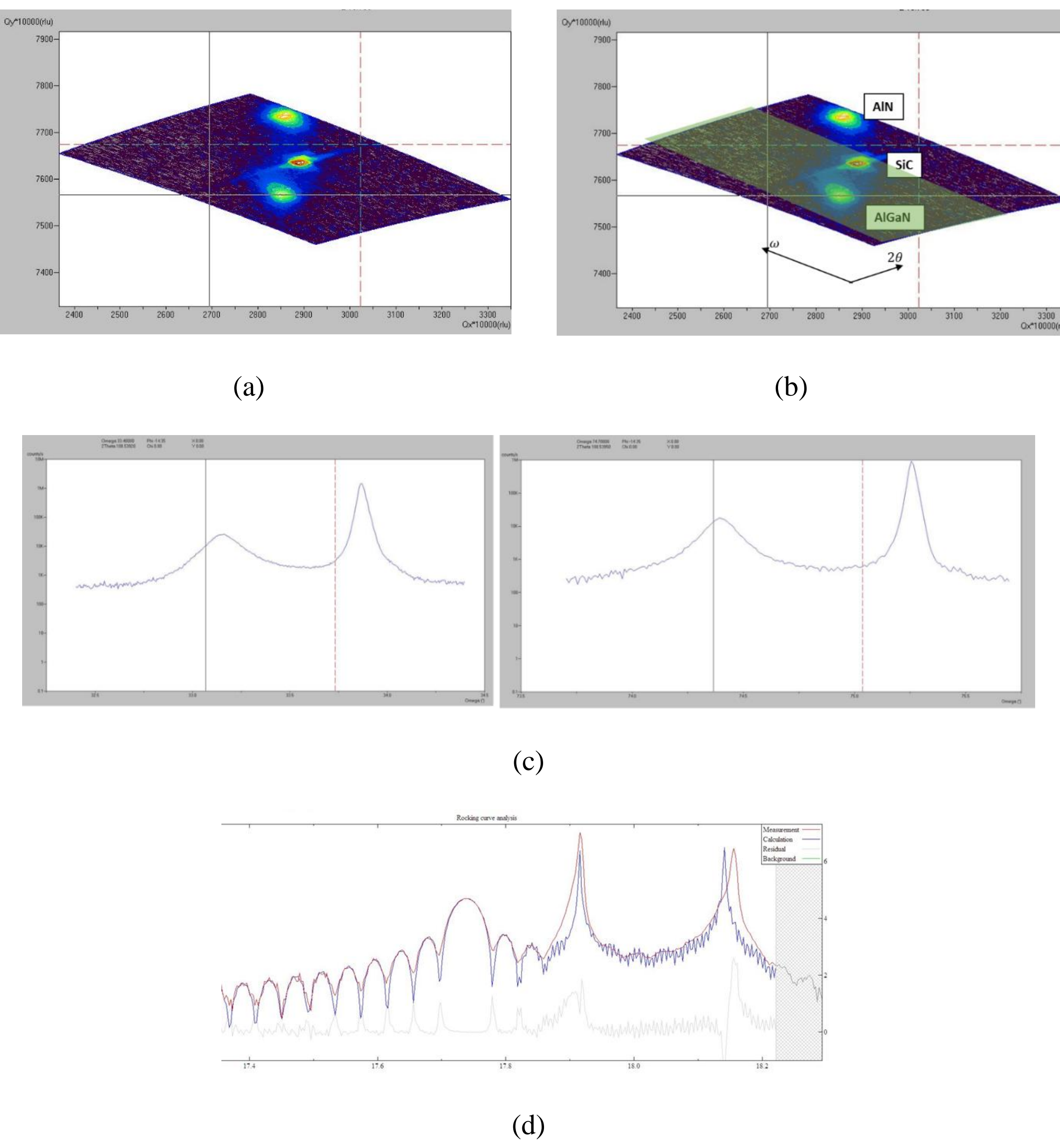
Emissivity calibrations are done to get accurate temperature readings on the Pyrometer. The standard way of emissivity calibration which involves the use of Al metal strip can be found in Ref. [1]. This approach calibrates the sample surface temperature using the melting point of Al (660 °C).

An alternative way is to use the calibrated sample as standard to calibrate other samples co-loaded on the same Si wafer by indium-bonding. It is generally safe to assume the temperature of co-loaded samples are roughly the same. The samples, however, needs to be freshly bonded as the indium might alloy with the backside metal which will change the emissivity. This also means that when the sample backside is coated with metal by e-beam evaporation, the emissivity is mainly dependent on the initial metal layer. For example, for Ti/Pd/Ti 50/5000/5 nm coated sample, the emissivity is largely determined by Ti. The indium-bonded sample with the same backside coating still have the same emissivity (when the indium bond is fresh). The sequence of accuracy for temperature reading calibration is: Al-assisted calibration on sample with backside metal coating > co-loading calibration on sample with backside metal coating > calibration on indium bonded-only sample. Indium also evaporate during growth, making it hard to have consistent emissivity throughout the growth especially at high temperature or high NH_3 flow rate during which the indium evaporation is faster. For temperature-sensitive growth such as growth of InGaN, backside metal should always be used.

B.2 Growth rate and composition calibrations for AlGaN

The growth rate calibration for III-nitrides can be done by doing ω-2θ scan of the (0002) peak using XRD (triple axis mode). The thickness fringes give the layer thickness. Usually, a 23-200 nm layer is easy to fit for the layer thickness. Sharp regrowth interface with lattice mismatch is needed to form the fringes. In the case of GaN growth calibrations on GaN on sapphire substrate, a AlN or AlGaN layer of ~3 nm is used at the regrowth interface.

There are three ways to measure the Al composition in AlGaN film grown on AlN on SiC template: 1) Reciprocal space map (RSM) of the $(10\bar{1}5)$ peak. By comparing the peak separation between the AlGaN and SiC peaks, one can get the Al% and degree of relaxation for the AlGaN layer; 2) paired ω scan. This method is also done using the Pixel detector. This method is fast, but the peaks are hard to find sometimes; 3) Doing ω-2θ scan of the (0002) peak and fit for the AlGaN composition using Globalfit software by inputting a degree of relaxation. The three methods gave relatively the same Al% as shown in table B1.



(a) (b)

(c)

(d)

Figure B1. Methods to do Al% composition and ratio of relaxation calibration. (a) RSM scan of the (10$\bar{1}$5) peaks. (b) Schematic of paired ω scan. (c) AlGaN and SiC peak separation measured by paired ω scan. (d) ω-2θ scan of the (0002) peak and fit for the AlGaN composition using Globalfit.

The three methods described here were combined with the sticking factor method mentioned in Chapter 3. Steps to do fast calibrations at the start of an AlGaN growth campaign is thus: 1)

grow AlGaN calibration samples of roughly 100 nm based on previous growth calibrations; 2) RSM scan to get the Al% and relaxation ratio (usually fully coherent; 3) Calculate the sticking factor S based on the result; 4) Calculate the Al Ga flux needed to achieve the desired composition and grow the next sample; 5) ω-2θ scan of the (0002) peak on the sample. Use the fringe spacings to get the thickness and use the peak positions and relaxation ratio form step 2 to fit for the Al% by using Rigaku GlobalFit software (version 2.1.1). The software simulates the XRD pattern for the input structure with the assumed Al composition and compares the simulation result to the measured value; 6) Continue step 4-5 until the desired composition is achieved.

Appendix C. Hall measurements

C.1 Room temperature Hall measurements

When doing Indium dot measurements, the dots can either be put within the sample border (Figure B3 (a)) or on the sample corners (Figure B3 (b)). Depending on the conductivity of the substrate, the location matters. The former one gives more accurate result and works with insulating substrates. The latter one avoids parallel conduction channel from conductive substrates.

(a) (b)

Figure C1. Indium dot Hall measurements where (a) the dots are put on the corners (b) the dots are put within the sample border.

C.2 Temperature-controlled Hall measurements

Details on the theory of temperature-controlled Hall measurements can be found at [2]. Figure B4 shows the experimental setup. The contact cement can also be replaced by low temperature glue.

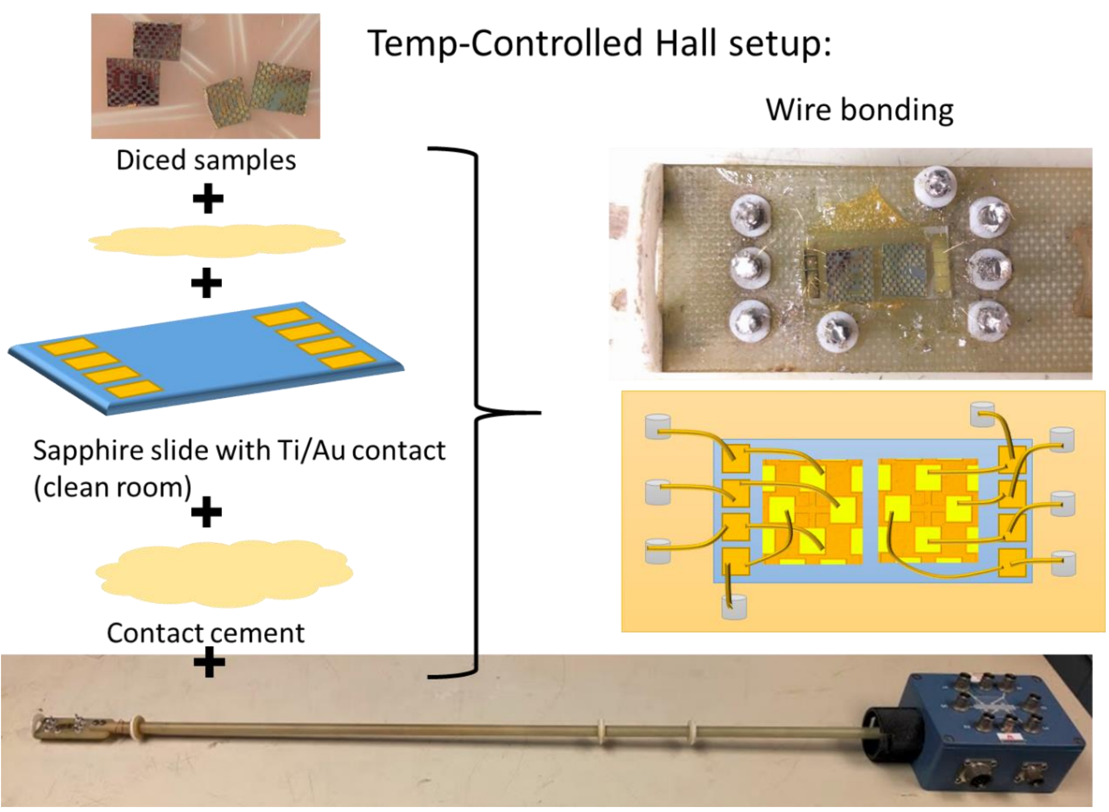


Figure C2. Temperature-controlled Hall measurement setup.

Appendix D. SIMS measurements

Tips for SIMS sample growth:

- Use Al as marker layer
- During growth: put rough layers on top to avoid damaging the entire structure
- The sharpness of the delta Al layer shows the resolution of measurement
- Do solvent clean, gold coating, and GaAs sputtering to lower the atmospheric contamination background level and at their effect from the sample surface at the initiation of the measurement
- The flatness of the sputter crater is dependent on the surface roughness and will determine the accuracy of reading and the resolution depth-wise.

Appendix E. Process travelers

E.1 Pd/Au vs TJ LED

Wafer Prep			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Surface treatment	Acid bench	Aqua Regia (HNO3+HCl 1:3), boil 120C, cover, 10min, Repeat 3x (140C two beakers to save time)	Doesn't matter which acid first, Improves contact resistance, do it right before PECVD1
Clean	Acid bench	DI rinse, N2 blow	
SiO2 deposition	PECVD #1	300nm	Follow procedure on tool, roughly 7.1A/s (7' 10"), include 3 Si monitors
Check SiO2 thickness	Ellipsometer	Standard measurement	Basic model "thermal SiO2" is good enough
Mesa Etch (+)			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Bake off water	Spin bench	Hot Plate, 115C	
Mesa lithography	Spin bench	PR: SPR 220-3.0, (3500 RPM / 20000 RPM/sec, 30 Sec) HMDS fume for 5min before PR	change recipe 1 or 0, N2 blow before PR, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razor Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 115C, 90 sec	Cover when done
Expose	Contact aligner	25 sec, 7.0 mW/cm2	Do not use iLine filter, soft contact
Post exposure bake	Spin bench	Hot Plate, 115C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 sec	**Gently** scroll around, dip in water when done, N2 blow dry
Microscope check			
UV ozone descum	UV-Ozone	10 min (+30" exhaust)	10 min 30 total, 10 min O2, put Si monitors in too
SiO2 removal	HF bench	approx 45s (check with Si monitors first)	Test etch time with Si monitor at 45s, if clean then test 2nd at 40s
Mesa etch	RIE #5	SiCl4 GaN etch, ~25 nm / min	
Water		2min in beaker	Water removes any remaining Cl, improve conductivity
NMP clean	Solvent bench	Warm NMP 80C preheat>20min, sonicate high, 10min	when done, pipet it and put it in holder
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI, high settings	Use right side ultrasonic (room temp)

SiO2 removal	HF bench	BHF, 3 mins, DI rinse	
Measure etch depth	DECTAC		make sure etch is to required depth
HCl Dip	Acid bench	30s	Immediately before tool
SiO2 deposition	PECVD #2	150nm + take out, cool down, water dip + rotate sample, 150 nm	Follow procedure on tool, roughly
Check SiO2 thickness	Ellipsometer	Standard measurement	Basic model "thermal SiO2" is good enough
p-contacts (-)			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Bake off water	Spin bench	Hot Plate, 115C	
p-contact lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 sec)	recipe 0 or 1, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razor Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	
Expose	Contact aligner	10 sec, 7.0 mW/cm2	Do not use iLine filter, soft contact
Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 Sec	sticks very well, shake very well
Microscope check			Look for PR undercut
UV ozone descum	UV-Ozone	10 min (+30" exhaust)	10 min 30 total, 10 min O2, put Si monitors in too
SiO2 removal	HF bench	approx 80s (check with Si monitors first)	Test etch time with Si monitor at 45s, if clean then test 2nd at 40s
Microscope check			Look for PR and SiO2 undercut
HCl Dip	Acid bench	HCL, 30 sec, DI Rinse	immediately before deposition (remove GaN oxide)
p-contact deposition	E-Beam #4	Pd/Au, 30/300 nm, start at <2e-6, Pd has oxide on surface	Check condition of Pd and Au during loading, Check Au box, Pd@ 1 2(150A/30s), Au @1 2 (100A/30s) 5 (200A/30s)
Liftoff	Solvent bench	NMP, 80C, 10 min	Use left side (heated >80C) ultrasonic, low settings
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings
n-contacts (-)			
Bake off water	Spin bench	Hot Plate, 115C	
n-contact lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 sec)	change recipe 1 or 0, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razor Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	

Expose	Contact aligner	10 sec, 7.0 mW/cm2	Do not use iLine filter, soft contact
Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 Sec, sticks well, shake very well	
Microscope check			Look for PR undercut
UV ozone descum	UV-Ozone	10 min (+30" exhaust)	10 min 30 total, 10 min O2, put Si monitors in too
SiO2 removal	HF bench	approx 45s (same as p-contact SiO2 opening time)	
Microscope check			Look for PR and SiO2 undercut
HCl Dip	Acid bench	HCL, 30 sec, DI Rinse	immediately before deposition (remove GaN oxide)
n-pad deposition	E-Beam #3	Ti/Au, 30/300nm (move around/amplitute=0)	Ti@ 1 2(150A/30s), Au @1 2 (100A/30s) 5 (200A/30s)
Liftoff	Solvent bench	NMP, 80C, 10 min	Use left side (heated >80C) ultrasonic, low settings
Clean	Solvent bench	3 min ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings

E.2 ITO vs TJ LED

Standard (vs TJ) LED w/ SiO2 isolation (p: ITO+Cr/Ni/Au)			
Wafer Prep			
Surface treatment	Acid bench	Acqua Regia (HNO3+HCl 1:3), boil 180C, cover, 10min, Repeat 3x	Doesn't matter which acid first, Improves contact resistance, ramp=0 (fastest)
Solvent Clean (only if acqua regia a long time ago)	Solvent Bench	Acetone 2min, Iso 2min, DI 15s+3X+2min, N2 Dry	RT, high intensity/frequency
BHF		30 sec	
ITO Deposition	E-Beam #2	110 nm ITO (hot)	680C on tool, actual 300C, use Si pieces as monitor
Check ITO thickness	Ellipsometry		
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Mesa / ITO Etch (+)			
Bake off water	Spin bench	Hot Plate, 115C, 3min	
Mesa lithography	Spin bench	PR: SPR 220-3.0, (3500 RPM / 20000 RPM/sec, 30 Sec)	change recipe 1 or 0, N2 blow before PR, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razer Blade	Remove ~1mm of PR from edges of sample

Soft bake	Spin bench	Hot Plate, 115C, 90 sec	Cover when done
Expose	Contact aligner	25 sec, 7.5 mW/cm2	Do not use iLine filter
Post exposure bake	Spin bench	Hot Plate, 115C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 sec, vertical and lateral	Gently scroll around, flush in water when done, N2 blow dry
Microscope check			
UV ozone descum	UV-Ozone	10 min	10 min 30 total, 10 min O2
Microscope check			
ITO Etch	RIE #2	Methane, Hydrogen, Argon / O2	(5 min MHA, 50 sec O)*2, 3 min MHA,5min O2 ~110 nm
Mesa etch	RIE #5	SiCl4 GaN etch, 27 nm / min TJ 425nm thicker, together possible	
Water		2min Al dish	Water removes any remaining Cl, improve conductivity
NMP clean	Solvent bench	Warm NMP 80C preheat>20min (no need if sonicate), sonicate high/8 int/8freq, 10min	when done, pipet it and put it in holder
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI, high/high intensity/high frequency	Use right side ultrasonic (room temp)
DI	DI	DI, N2 blow dry	
Measure etch depth	DECTAC		make sure etch is to required depth
ITO Etch (+)			
Solvent Clean	Solvent Bench	Acetone 2min, Iso 2min, DI 15s+3X+2min, N2 Dry	RT, low intensity/frequency
ITO lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 Sec)	change recipe 1 or 0, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razer Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	
Expose	Contact aligner	10 sec, 7.5 mW/cm2	Make sure no iLine filter, vacuum sample not flow gas
Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 sec	scroll and shake well
UV ozone descum	UV-Ozone	10 min	
ITO Etch	RIE #2	Methane, Hydrogen, Argon / O2	5 min MHA, 50 sec O2, 3 min MHA ~110 nm
NMP clean	Solvent bench	Warm NMP 80C, sonicate high/8 int/8freq, 10min	when done, pipet it and put it in holder
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)
Measure etch depth	DECTAC		make sure etch is to required depth

n-contacts (-)			
Bake off water	Spin bench	Hot Plate, 115C	
n-contact lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 sec)	recipe 5, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razer Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	
Expose	Contact aligner	10 sec, 7.5 mW/cm2	Do not use iLine filter
Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 Sec	
UV ozone descum	UV-Ozone	10 min (O2 plasma 30'' 300 pressure 100W)	
HCl Dip (1 water :1 HCl)	Acid bench	HCL, 40 sec, DI flush 2 min	add HCl to water, immediately before deposition (remove oxide)
n-contact deposition	E-Bean #3	Ti/Au, 30/300 nm	Ti @ 1, Au @1 2.5 (150A/30s) 4.5 (300A/30s)
Liftoff	Solvent bench	NMP, 80C, 10 min, sonicate on low settings	Use left side (heated >80C) ultrasonic, low settings
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings
p-pad (-)			
Bake off water	Spin bench	Hot Plate, 115C	
p-contact lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 sec)	change recipe 1 or 0, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razer Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	
Expose	Contact aligner	10 sec, 7.5 mW/cm2	Do not use iLine filter
Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 Sec	
UV ozone descum	UV-Ozone	10 min + 30 s	
HCl Dip (1 water :1 HCl)	Acid bench	HCL, 30 sec, DI Rinse	immediately before deposition (remove GaN oxide)
p-pad deposition	E-Bean #4	Cr/Ni/Au, 25/20/500nm	Cr 1/ Ni 1/ Au @1 2.5 (150A/30s) 4.5 (300A/30s)
Liftoff	Solvent bench	NMP, 80C, 10 min	Use left side (heated >80C) ultrasonic, low settings
Clean	Solvent bench	3 min ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings

E.3 Miscellaneous for LED processing

Beaker Prep

DI	DI bench	DI	Thorough water rinse
Solvent clean	Solvent bench	Acetone Iso Methanol	outside: spray Inside: fill
			sonicate on high settings/high intensity/high frequency
Aqua Regia	Acid bench		If have metal
Pirana	acid bench	Pirana	
Align Mask			
Align top left with x&y			
Align bottom left with angel			
Tweezer Clean			
Solvent clean	Solvent Bench	Acetone, methanol, iso	Rinse (spray with bottles) in spinner and blow dry
DI	DI bench	DI	Rinse (spray with bottles) and blow dry
Mask Clean			
Fresh mask from ECE	No need to clean		Don't open it outside of clean room
Used positive mask with PR		wipe gently with acetone (Iso)+blow dry	crank up N_2 pressure ~50, sonicate if needed
Used negative mask with PR		AZ kiwk strip, sonicate 10min @80C, Al foil cover, high	
		water-Acetone-blow dry	
		Or: wipe with Kwik strip-DI-Iso-blowdry	
Standard clean			
Solvent clean	Solvent Bench	Ace 2-3min in beaker, Iso 2-3min in beaker	Especially important for metal deposition
DI	DI	DI beaker 15s running water, rinse 3 times, 2min running water	
		N_2 blow dry	30 N_2 pressure
Or Ace/Iso/DI	Solvent Bench	3min each in beaker	
PR			
Positive PR		removing materials	Thick, redish, profile: _/¯_
Negative PR		Adding materials	Profile:_\¯/_
PECVD #2			
SiO_2 deposition	PECVD #2	coat: 5' or 10'(bit better), deposition 9'45'' ~320nm	
		wet(wipe inside/stage with water & iso)+standard clean	
		clean: 1' for 2' of SiO_2	
HDMS			
HDMS	PR bench	many samples: fume for 5min	samples on paper wipe, with a small dish having ~ 1cm of HDMS in it, cover with a large dish

		a few samples: HDMS sit on sample for 1min, spin	same recipe as PR, spin HDMS before PR
PR residue			
Pirana	Acid bench	pirana 30s-1min, DI	till no extra bubble
HF SiO2 etch test			
SiO2 etch	Acid bench	BHF, find clean/no clean boundary	center clean: enough, 90% clean: should be good
			98%:safe, slightly over etch center area, value chose
			(SiO2 thicker on edges)
			do another 2s if no good undercut
HF SiO2 etch how to see over-etch by microscope			
why			vertical etch finish- then lateral etch (undercut)
SiO2 undercut check	Microscope at end of bay	approach 1: bright field,current spreading device	
		approach 2: DF, current spreading device	
		SiO2 undercut; PR & PR undercut (bright band due to depth difference); mesa	
Scroll sample			
		up down & sideways	
Restart litho			
solvent clean	solvent bench	NMP spin in white spinner	
		Ace/Iso/DI	
clean chuck			
	PR bench	razor blade scratch-EBR wipe-blow	
litho PR spin			
		put on sample, turn chuck 360 to see if center&cover chuck, spin & blow w/o PR	
expose			
		ST [soft contact] pressed down/HP (ok)	
HCl			
removes GaN:O	not needed for ITO	better no do if have metal	cold ITO get etched, annealed ITO fine
RIE #5			

wait 2hrs if last person did SiCl4	SiCl4 comes from bubbler	at 25C, need time to recover	

E.4 Diode_v1

Wafer Prep			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Surface treatment	Acid bench	Aqua Regia (HNO3+HCl 1:3), boil 120C, cover, 10min, Repeat 3x	Any acid first, Improves contact resistance, do it right before PECVD1, ramp=0, 140C if 2 beakers on plate
Clean	Acid bench	DI rinse, N2 blow	
HCl Dip	Acid bench	30s	Immediately before tool
SiO2 deposition	PECVD #2 or #1	300nm, PECVD #2: 9'45''=~320nm	Follow procedure on tool, roughly 7.1A/s (7' 10"), include 5 Si monitors
Check SiO2 thickness	Ellipsometer	Standard measurement	Basic model "thermal SiO2" is good enough
Mesa Etch (+)			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Bake off water	Spin bench	Hot Plate, 115C, 3min	
Mesa lithography	Spin bench	PR: SPR 220-3.0, (3500 RPM / 20000 RPM/sec, 30 Sec), 5min HMDS fume treatment before PR	change recipe 1 or 0, N2 blow before PR, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razor Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 115C, 90 sec	Cover when done
Expose	Contact aligner	25 sec, 7.0 mW/cm2	Do not use iLine filter, soft contact
Post exposure bake	Spin bench	Hot Plate, 115C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 sec	Gently scroll around, dip in water when done, N2 blow dry
Microscope check			
UV ozone descum	UV-Ozone	10 min (+30" exhaust)	10 min 30 total, 10 min O2, put Si monitors in too
SiO2 removal	HF bench	approx 45s (check with Si monitors first)	Test etch time with Si monitor at 45s (#1), if clean then test 2nd at 40s, ~ 85s for #2
Mesa etch	RIE #5	SiCl4 GaN etch, ~25 nm / min	
Water		2min in Al dish/beaker	Water removes any remaining Cl, improve conductivity
NMP clean	Solvent bench	NMP 80C, sonicate high, 10min	when done, pipet it and put it in holder

Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI, high intensity	Use right side ultrasonic (room temp)
SiO2 removal	HF bench	BHF, 3 mins, DI rinse	*2 the time to etch off SiO2
Measure etch depth	DECTAC		make sure etch is to required depth
HCl Dip	Acid bench	30s	Immediately before tool
SiO2 deposition	PECVD #2 or #1	150nm + take out, cool down, water dip + rotate sample, 150 nm	Follow procedure on tool, roughly 7.1A/s (2x 3' 5"), include 3 Si monitors
Check SiO2 thickness	Ellipsometer	Standard measurement	Basic model "thermal SiO2" is good enough
p-contacts (-)			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Bake off water	Spin bench	Hot Plate, 115C	
p-contact lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 sec)	recipe 0 or 1, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razor Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	
Expose	Contact aligner	10 sec, 7.0 mW/cm2	Do not use iLine filter, soft contact
Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 Sec	Scroll around strongly, sticks very well
Microscope check			Look for PR undercut
UV ozone descum	UV-Ozone	10 min (+30" exhaust)	10 min 30 total, 10 min O2, put Si monitors in too
SiO2 removal	HF bench	#1: approx 45s (check with Si monitors first) #2: ~80s	Test etch time with Si monitor at 45s, if clean then test 2nd at 40s
Microscope check			Look for PR and SiO2 undercut
HCl Dip	Acid bench	HCL, 30 sec, DI Rinse	immediately before deposition (remove GaN oxide)
p-contact deposition	E-Beam #4	Pd/Au, 30/300 nm	Check condition of Pd & Au during loading, Pd@ 1 2(150A/30s), Au @1 3 (150A/30s) 5 (300A/30s), pump till <2e-6 (Pd oxide cause pressure spike)
Liftoff	Solvent bench	NMP, 80C, 10 min	Use left side (heated >80C) ultrasonic, low settings. Don't dry bw NMP/Ace
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings
n-contacts (-)			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings
Bake off water	Spin bench	Hot Plate, 115C	
Mesa lithography	Spin bench	PR: SPR 220-3.0, (Recipe 5), 5min HMDS fume treatment before PR	change recipe 1 or 0, N2 blow before PR, Fully coat wafer, no bubbles

Soft bake	Spin bench	Hot Plate, 115C, 90 sec	Cover when done
n-contact deposition	E-Beam #3	Ti/Au, 30/300nm	Ti@ 1 2(150A/30s), Au @1 2 (100A/30s) 5 (200A/30s), Ti amplitude big, Au aplitude=0
clean off protective PR	Solvent bench	NMP, 80C, 10 min	Use left side (heated >80C) ultrasonic, low settings. Don't dry bw NMP/Ace
Clean	Solvent bench	3 min ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings
Bake off water		3 min 115C	bake samples before testing

E.5 Diode_v2

Wafer Prep			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Surface treatment	Acid bench	Aqua Regia (HNO3+HCl 1:3), boil 120C, cover, 10min, Repeat 3x	Any acid first, Improves contact resistance, do it right before PECVD1, ramp=0, 140C if 2 beakers on plate
Clean	Acid bench	DI rinse, N2 blow	
HCl Dip	Acid bench	30s	Immediately before tool
SiO2 deposition	PECVD #2 or #1	300nm, PECVD #2: 9'45''=~320nm	Follow procedure on tool, roughly 7.1A/s (7' 10"), include 5 Si monitors (keep a few Si pieces for calibrations)
Check SiO2 thickness	Ellipsomet er	Standard measurement	Basic model "thermal SiO2" is good enough
Dice wafers	Dicing saw	Use slow dice speed and 30RU blade	epi-side touching stage, bulk GaN recipe, flange 52mm, change blade: 30r instead of ru
Mesa Etch (+)			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Clean	Acid bench	Piranha (H_2SO_4:H_2O_2=3:1) 5min	Or till bubble disappear
Bake off water	Spin bench	Hot Plate, 115C, 3min	
Mesa lithography	Spin bench	PR: SPR 220-3.0, (3500 RPM / 20000 RPM/sec, 30 Sec), 5min HMDS fume treatment before PR	change recipe 1 or 0, N2 blow before PR, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razor Blade - very careful due to the fragile substrates!!!	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 115C, 90 sec	Cover when done
Expose	Contact aligner	25 sec, 7.0 mW/cm2	Do not use iLine filter, soft contact
Post exposure bake	Spin bench	Hot Plate, 115C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 sec	**Gently** scroll around, dip in water when done, N2 blow dry

Microscope check			
UV ozone descum	UV-Ozone	10 min (+30" exhaust)	10 min 30 total, 10 min O2, put Si monitors in too
SiO2 removal	HF bench	approx 45/85s (check with Si monitors first)	Test etch time with Si monitor at 45s (PECVD #1), if clean then test 2nd at 40s, ~ 85s for #2
Mesa etch	RIE #5	Cl_2 GaN etch, ~100 nm / min	Etch pass the junction
DI Water		2min in Al dish/beaker	Water removes any remaining Cl, improve conductivity
NMP clean	Solvent bench	NMP 80C, sonicate high, 10min	when done, pipet it and put it in holder
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI, high intensity	Use right side ultrasonic (room temp)
SiO2 removal	HF bench	BHF, 3 mins, DI rinse	*2 the time to etch off SiO_2
Measure etch depth	DECTAC		make sure etch is to required depth
Sidewall Treatment and Passivation			
Etch damage removal	Develop bench	Soak in TMAH or AZ400k at 80C for 10min	
HCl Dip	Acid bench	30s	Immediately before tool
Sidewall passivation	ALD	SiO2	~20nm, standard SiO2 recipe, include 5 Si monitors
SiO2 deposition	PECVD #2 or #1	150nm + take out, cool down, water dip + rotate sample, 150 nm	Follow procedure on tool, roughly 7.1A/s (2x 3' 5"), include the 5 Si monitors
(Other side-wall passivation)		SOG/ALD SiO_2+SOG/ALD Al_2O_3 (no Si or plasma)/ebeam-2 SiO2(no plasma)/BCB(spin-on, thick)…	
Check SiO2 thickness	Ellipsometer	Standard measurement	Basic model "thermal SiO2" is good enough
p-contacts (-)			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Try no sonication and pipetting first. Use right side ultrasonic (room temp)/ low settings
Bake off water	Spin bench	Hot Plate, 115C	
p-contact lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 sec)	recipe 0 or 1, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razor Blade (delete to not to break wafer)	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	
Expose	Contact aligner	10 sec, 7.0 mW/cm2	Do not use iLine filter, soft contact

Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 Sec	Scroll around strongly, sticks very well
Microscope check			Look for PR undercut in Nomarski mode
UV ozone descum	UV-Ozone	10 min (+30" exhaust)	10 min and 30 sec total, 10 min O2, put Si monitors in too
SiO2 removal	HF bench	#1: approx 45s (check with Si monitors first) #2: ~80+ALD s	Test etch time with Si monitor at 45+ALDs (PECVD #1), if clean then test 2nd at 40+ALDs, ~ 85+ALDs for #2
Microscope check			Look for PR and SiO2 undercut
HCl Dip	Acid bench	HCl, 30 sec, DI Rinse	immediately before deposition (remove native oxide, etc.)
p-contact deposition	E-Beam #4	Pd/Au, 30/300 nm	Check condition of Pd & Au during loading, Pd@ 1 2(150A/30s), Au @1 3 (150A/30s) 5 (300A/30s), pump till <2e-6 (Pd oxide cause pressure spike)
Liftoff	Solvent bench	NMP, 80C, 10 min	Use left side (heated >80C) ultrasonic, low settings (freq and amp). Don't dry bw NMP/Ace
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Try no sonication and pipetting first. Use right side (room temp) ultrasonic, low settings
Field plate			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Bake off water	Spin bench	Hot Plate, 115C	
Field plate lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 sec)	recipe 0 or 1, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razor Blade (delete to not to break wafer)	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	
Expose	Contact aligner	10 sec, 7.0 mW/cm2	Do not use iLine filter, soft contact
Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 Sec	Scroll around strongly, sticks very well
Microscope check			Look for PR undercut in Nomarski mode
UV ozone descum	UV-Ozone	10 min (+30" exhaust)	10 min and 30 sec total, 10 min O2, put Si monitors in too
HCl Dip	Acid bench	HCL, 30 sec, DI Rinse	immediately before deposition (remove GaN oxide)

Field plate deposition	E-beam #3	Ti/Al/Au (50/200/50 nm) - K. Nomoto, ... , G. Xing, IEEE IEDM 15, 237-240 (2015)	Ti@ 1 2(150A/30s), Au @1 2 (100A/30s) 5 (200A/30s), Ti amplitude big, Au aplitude=0, Al deposition condition?
Liftoff	Solvent bench	NMP, 80C, 10 min	Try no sonication and pipetting first. Use left side (heated >80C) ultrasonic, low settings. Don't dry bw NMP/Ace
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings
n-contacts (-)			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings
Bake off water	Spin bench	Hot Plate, 115C	
Mesa lithography	Spin bench	PR: SPR 220-3.0, (Recipe #5 - slow, prevent wafer from breaking), 5min HMDS fume treatment before PR	recipe 5, N2 blow before PR, Fully coat wafer, no bubbles
Soft bake	Spin bench	Hot Plate, 115C, 90 sec	Cover when done
Backside n-contact deposition	E-Beam #3	Ti/Au, 30/300nm	Ti@ 1 2(150A/30s), Au @1 2 (100A/30s) 5 (200A/30s), Ti amplitude big, Au aplitude=0
clean off protective PR	Solvent bench	NMP, 80C, 10 min	Try no sonication and pipetting first. Use left side (heated >80C) ultrasonic, low settings. Don't dry bw NMP/Ace
Clean	Solvent bench	3 min ACE, ISO, DI	Use right side (room temp) ultrasonic, low settings
Bake off water		3 min 115C	bake samples before testing

E.6 CV for UID on STN

CV for UID on STN			
Wafer Prep			
Clean	Solvent bench	3 min Sonicate: ACE, ISO, DI	Use right side ultrasonic (room temp)/ high settings
Surface treatment	Acid bench	Aqua Regia (HNO3+HCl 1:3), boil 120C, cover, 10min, Repeat 3x	Doesn't matter which acid first, Improves contact resistance
Metal lift off	Acid bench	BHF:HNO3=1:1, 2 min	clean off the metal from last trail
Clean	Acid bench	DI rinse, N2 blow	
ALD SiO2			
bake off water	Spin bench	Hot Plate, 115C	

SiO2 deposition	ALD	standard SiO2 recipe	~20 nm
Schottky-contacts			
Bake off water	Spin bench	Hot Plate, 115C	
n-contact lithography	Spin bench	PR: nLOF 2020 (3000 RPM / 20000 RPM/sec, 30 sec)	recipe 1 or 0, Fully coat wafer, no bubbles
Remove edge beads	Spin bench	Razer Blade	Remove ~1mm of PR from edges of sample
Soft bake	Spin bench	Hot Plate, 110C, 90 sec	
Expose	Contact aligner	10 sec, 7.0 mW/cm2	Do not use iLine filter
Post exposure bake	Spin bench	Hot Plate, 110C, 60 sec	
Develop	Developer bench	AZ300MIF, 50 Sec	
Microscope check			Look for PR undercut
UV ozone descum	UV-Ozone	10 min (O2 plasma 30" 300 pressure 100W)	10 min 30 total, 10 min O2
HCl Dip	Acid bench	HCL, 30 sec, DI flush 2 min	add HCl to water, immediately before deposition (remove oxide)
Schottky-contact deposition	E-Bean #3	Pt/Au, 30/300 nm, cover an edge with tape/Al foil, ~1.5mm	start deposition at 2e-6, Pt@0.5 1(150A/30s) 2 (300A/30s), Au @1 2.5 (150A/30s) 4.5 (300A/30s)
Liftoff	Solvent bench	NMP 80C overnight (caused metal peal off. Should have done 15 min)	
Clean	Solvent bench	spray ACE, ISO, DI	
Microscope check			
Ohmic-contact (Indium)			
Diamond scraber	Hall setup		Near edge/corner area, scibe deep enough to reach STN (>1um deep)
Apply Indium	Hall setup	Heat up indium, apply to scribed area	

References

1. B. M. McSkimming, C. Chaix, and J. S. Speck, "High active nitrogen flux growth of GaN by plasma assisted molecular beam epitaxy," Journal of Vacuum Science & Technology A **33**, 05E128 (2015).

2. E. C. H. Kyle, S. W. Kaun, E. C. Young, and J. S. Speck, "Increased p-type conductivity through use of an indium surfactant in the growth of Mg-doped GaN," Appl. Phys. Lett. **106**, 222103 (2015).