**UNIVERSITY OF CALIFORNIA,
IRVINE**

Analysis and Design of High-Speed CMOS Frequency Dividers

Thesis

submitted in partial satisfaction of the requirements
for the degree of

Master

in Electrical & Computer Engineering

by

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2015

DEDICATION

To my family

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LIST OF ABBREVIATIONS

CML ..... Current-Mode Logic
DFF ..... D Flip-Flop
ILFD ..... Injection Locked Frequency Divider
SOC ..... System-on-Chip
CMOS ..... Complementary Metal-Oxide Semiconductor
NMOS ..... Negative-Channel Metal-Oxide Semiconductor
PMOS ..... Positive-Channel Metal-Oxide Semiconductor
LPF ..... Low Pass Filter

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ABSTRACT OF THE THESIS

Theory and Design of High-Speed CMOS Frequency Dividers

By

Fatemehe Molainezhad

Master Degree

in Electrical & Computer Engineering

University of California, Irvine, 2015

Professor Michael Green, Chair

A frequency divider is one of the most fundamental and challenging blocks used in high-speed communication systems. Three high-speed dividers with different topologies, LC-tank frequency divider, CML ring frequency divider, and CML DFF frequency divider with negative feedback, are analyzed based on the locking phenomena. The locking to the injected signal happens as long as the frequency and the amplitude of the injected signal are in the desired operation region of the divider's sensitivity curve. A phase shift (which is a function of both frequency and the amplitude of the injected signal) occurs in the circuit and the divider will be locked to the injected frequency.

Locking to an external signal may not necessarily occur just by considering the frequency of the injection signal being in the locking range, even if the frequency of the injection signal is very close to the self-oscillation frequency in a wide locking range scenario without the proper injected signal amplitude.

To measure the phase shift, $\varphi(A_{inj}, \omega_{inj})$ when the oscillator is locked to the injected frequency, a novel procedure is developed. This procedure gives us a very precise tool to measure the locking phase, instantaneous phase, or the phase between any two signals inside the topology loop and provides a good ability for better understanding of the injection locking concept and the behavior of the divider in the presence of an injected signal. The simulations are using transistor models from TSMC 65nm CMOS process.

CHAPTER 1. INTRODUCTION

1.1 Overview

A frequency divider is a fundamental block in many systems. Such circuits are widely used in high-speed communication systems and are considered as one of the most challenging blocks to design in both wired and wireless transceivers [2]. Frequency dividers have been the subject of extensive study for decades and a number of papers have been published about this subject. Different approaches for injection locking phenomena have been investigated and several novel frequency dividers that allow for higher frequencies and wider locking ranges have been proposed.

In [4], it is described how the injection of an external signal into an oscillator affects both the instantaneous amplitude and instantaneous frequency if the self-oscillation frequency is close to the injection frequency. Using the assumption that the time constants in the oscillator circuit are small compared to the length of one beat cycle, a differential equation is derived which gives the phase between the oscillator output voltage and the injected signal as a function of time.

In [5], it is shown that locking to an external signal can occur when the frequency of the injected signal is within a certain range of frequencies, called the "locking range," that contains the self-oscillation frequency. An oscillator is said to be locked when the phase difference θ between the locking signal and the oscillator is constant, so that the instantaneous frequency difference, $d\theta/dt$, is equal to zero.

In [6], it is presented if the amplitude and frequency of I_{inj} are chosen properly, the circuit indeed oscillates at ω_{inj} rather than at ω_o and injection locking occurs.

In [1], two main categories of clock dividers are described: The first category includes those that operate entirely based on injection locking, such as the LC-tank and the ring oscillator frequency dividers. The second category includes divide-by-two circuits based on D flip-flops (DFF) realized by current mode logic (CML) with negative feedback. In the latter category due to the presence of nonlinearities, a wider frequency locking range, which is usually desirable, can result.

In this thesis, three different topologies, LC-tank, CML ring, and CML DFF frequency dividers are designed to achieve higher operation speed and minimum power consumption. They are analyzed based on the following condition: As long as the frequency $\omega_{inj} = \omega_o + \Delta\omega$ and the amplitude A_{inj} of the injected signal *are in the desired operation region of the frequency divider's sensitivity curve,* a phase shift, φ (A_{inj} , ω_{inj}) will occur in the circuit and the oscillator will be locked to the injected frequency.

The DFF frequency divider has a very wide sensitivity curve, which is a big advantage for this topology. On the other hand, the frequency divider realized by a CML ring oscillator has a higher self-oscillation frequency, but its sensitivity curve is not as wide as that of the DFF frequency divider. Finally, an LC-tank frequency divider has a very narrow sensitivity curve, but its self-oscillation frequency is much higher than either of the other two topologies and thus it is suitable to be used in some applications for very high-frequency operation.

The variations of instantaneous frequency and phase are analyzed for all three dividers. The instantaneous frequency can vary due to both changing the amplitude of the injection signal and/or changing the phase between the injection and the oscillation signals. Controlling the amplitude and the starting time to inject the signal can be used to reduce the settling time and allow a faster locking to the injected frequency.

Based on the model of each topology and the concept of injection locking, the relationship between the instantaneous and the locking phase is mathematically formulated. The analytical results are then compared with the simulation results utilizing a procedure that is developed to measure locking phase, instantaneous phase, or the phase between any two signals.

1.2 Outline

The remainder of thesis is organized as follows. Chapter 2 provides an overview of published work on frequency dividers with an emphasis on high-speed clock dividers based on the LC-tank frequency divider, CML ring frequency divider, and DFF frequency divider. This overview covers the theoretical analysis of injection locking concept, frequency locking range, and a derivation of the instantaneous phase, $d\theta/dt$.

Chapter 3 analyzes the three divider topologies based on the injection-locking concept and their sensitivity curves. The instantaneous frequency and phase when an external signal is injected is analyzed in detail. A procedure is developed to measure the phase between two the signals and verifying that the derivative of the instantaneous phase is equal to zero when the divider locks to the injected frequency.

Chapter 4 models the three divider topologies, and equations are derived for the locking phase and the instantaneous phase. The analytical results are discussed and compared with the simulation results that are generated using transistors models from TSMC 65nm CMOS process.

Chapter 5 summarizes the findings and the conclusions.

CHAPTER 2. REVIEW OF PUBLISHED WORK

2.1 A Study of Injection-Locking and Pulling in Oscillators

A study of injection locking and pulling between coupled oscillators realized in CMOS integrated circuits was reported in [6]. This paper describes the concept of injection locking, based on Adler's formulation [6]. In the simple oscillator shown in Figure 2-1(a), the resonance frequency of the tank is $\omega_o = 1/\sqrt{LC_L}$. The ideal inverter provides the complementary 180^o phase shift which is needed to close the feedback loop and ensures the oscillation.

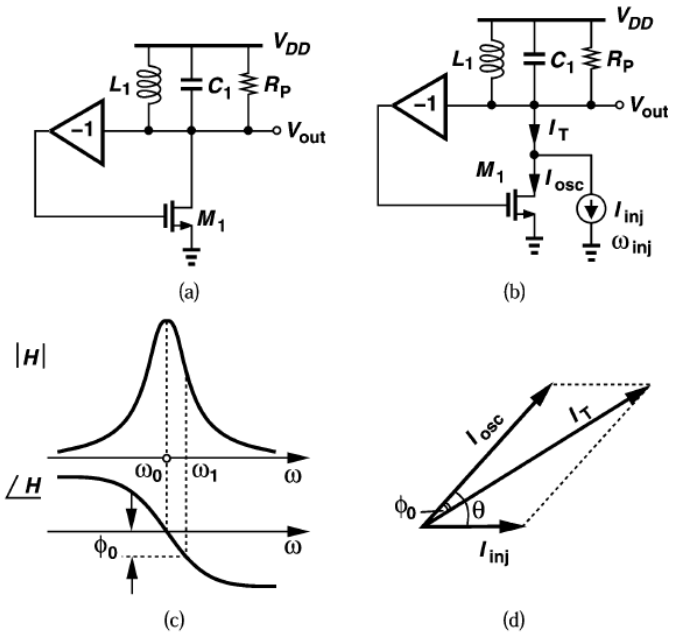

Figure 2-1 (a) Conceptual oscillator, (b) Frequency shift by injection, (c) Open-loop characteristics, and (d) Phase difference between input and output currents [6].

Figure 2-1(b) shows that conceptual oscillator when an external signal is injected to the output node. As described in [6], "if the amplitude and frequency of I_{inj} are chosen properly", injection locking occurs and the circuit oscillates at the injection frequency rather than at ω_o. By

considering this condition the paper describes that the tank provides phase φ_o at $\omega_{inj} \neq \omega_o$, therefore V_{out} rotates with respect to the sum current I_T. It also describes that I_{inj} forms an angle θ with I_{osc} such that the output voltage becomes aligned with resultant current. As a result, V_{out} and I_{inj} must have a phase difference as shown in Figure 2-1(d). Using this concept of injection locking, the locking range for LC-tank oscillator is formulated as following:

$$\omega_o - \omega_{inj} = \frac{\omega_o}{2Q} \cdot \frac{I_{inj}}{I_{osc}} \cdot \frac{1}{\sqrt{1 - \frac{I_{inj}^2}{I_{osc}^2}}} \tag{2-1}$$

The above equation shows how the amplitude of injected signal changes the locking range. When the amplitudes of injected signal decreases while the injection frequency is held fixed, to maintain phase φ_o which corresponds to the oscillation frequency, I_{osc} must form a bigger angle with respect to I_{inj}. This paper also shows the application of the injection locking when oscillator operates as a divide by two and investigates the nonlinearities in injection locking for LC-tank oscillator.

2.2 Analysis of Nonlinearities in Injection-Locked Frequency Dividers

Analysis of nonlinearities in injection-locked frequency dividers is reported in [2]. This paper investigated the locking range of frequency dividers and it was shown that the wider locking range as the case for CML DFF frequency divider is due to the presence of nonlinearities. The paper also presents a different approach to the analysis of nonlinearities in ILFD and introduces a new definition and then proposes a new frequency divider topology based on the new definition.

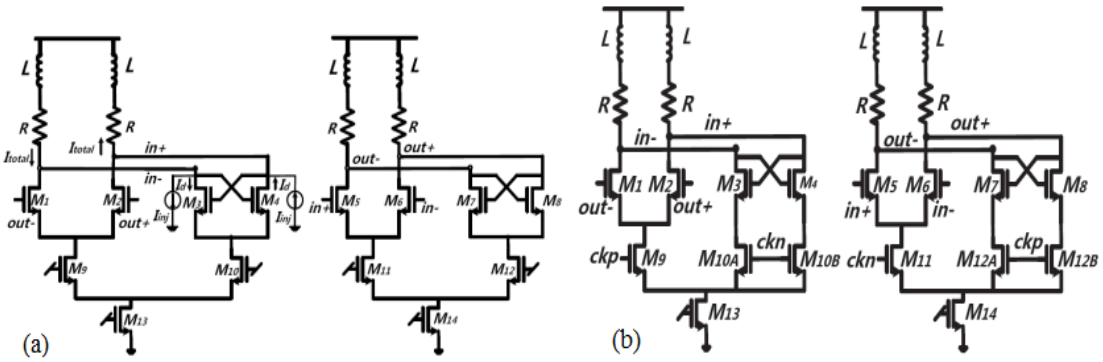

Figure 2-2 (a) Current injection mode of CML-DFF divider, (b) Schematic of new frequency divider [2].

Figure 2-2(a) shows an equivalent schematic of a conventional DFF divider, but with half-rate current sources I_{inj} injected directly into the output nodes. As discussed in [2], it can be shown that this is equivalent to the normal voltage injection with an appropriate conversion factor, but lends itself better to a more detailed analysis. If the divider is under free-running condition, then the drain currents I_d are equivalent to I_{osc}. I_{total} is the total current conducted through the resistors. The phase relationships between currents I_{inj}, I_{osc}, and I_T determine the divider frequency range. For normal injection locking, as the case for LC or ring oscillator dividers, it is generally assumed that all three currents stay in phase at the self-oscillation frequency, regardless of the amplitude of the injected current. However as shown in [2], this does not hold for the DFF clock divider.

A new definition is introduced in [2]: the *In-Phase Frequency*, which is the frequency at which injected current signal, I_{inj}, I_{osc}, and I_T, all remain in phase as a function of a given amplitude of I_{inj}. The fundamental cause of the strong nonlinearity existing in the DFF frequency divider can be narrowed down to the latch structure. Then the paper proposes a new frequency divider topology based on that technique which provides robust operation and wide lock-in while exhibiting higher operating frequency, as shown in Figure 2-2(b). The new topology employs a cross-coupled source follower in place of the latch, which maintains nonlinearity similar to that

of the conventional DFF clock divider, while decreasing the capacitance at the output nodes, thereby increasing the self-oscillation frequency.

2.3 A Study of Locking Phenomena in Oscillators

A study of locking phenomena in oscillators is reported in [4]. This paper explains how the instantaneous amplitude and frequency of vacuum tube-based oscillators are both affected when an external signal with a frequency very close to the natural frequency of the oscillator is injected to the loop. A differential equation for the phase between feedback and injected signals as a function of time is derived under the assumption that time constants in the oscillator are small compared to the oscillation period.

The main purpose of this paper is to derive a differential equation for the oscillator phase as a function of time and how it is related to the phase and amplitude relationships between oscillator voltage and injected signal. The derived equation also describes the transient and steady state behaviors of the oscillator. It is assumed in the analysis that the frequency of the injected signal is close to the self-oscillation frequency.

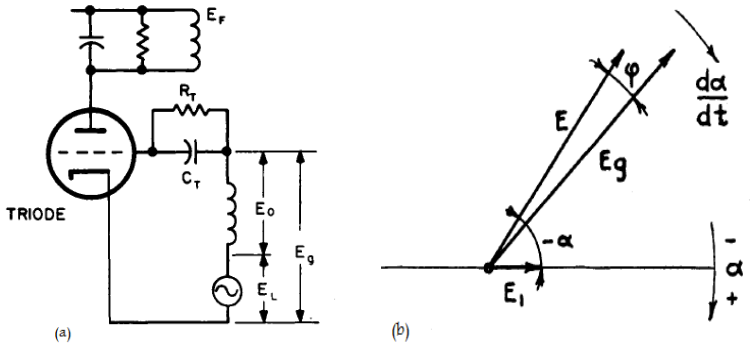

Figure 2-3 (a) Adler's model for oscillator circuit, (b) Vector diagram of instantaneous voltages for oscillator [4].

Adler investigated locking phenomena in vacuum tube-based oscillators using the model in Figure 2-3(a). The grid voltage, E_g is the vector sum of the injected voltage E_L and the tank voltage E_F which is transformer-coupled into the grid and denoted as E_o in the diagram. The following symbols are used:

ω_o = self-oscillation or "natural" frequency

ω_l = frequency of injected signal

$\Delta\omega_o$= "undisturbed" beat frequency (or inherent frequency difference)$(\omega_o - \omega_l)$

ω = oscillator's instantaneous frequency

$\Delta\omega$ = instantaneous beat frequency (or instantaneous frequency difference)$(\omega - \omega_l)$

Q = quality factor of tuned circuit.

Using the following three assumptions, the differential equation for the model in Figure 2-3(a) was developed.

1) $\omega_o /2Q >> \Delta\omega_o$; that is, the locking frequency should be very close to the natural frequency of the tuned circuit.

2) $T << 1/\Delta\omega_o$; that is, the time contestants in the oscillator are small compared to the oscillation period.

3) $E_L / E_o << 1$; that is, the amplitude of injected signal is much smaller than the output voltage.

Adler's derivation of the phase as a function of time was based on the vector diagram of instantaneous voltages shown in Figure 2-3(b). Under the presence of an injected signal, there is a phase angle φ between the voltage E returned through the feedback circuit and the grid voltage E_g. Assuming $E_L / E_o << 1$, Figure 2-3(b) gives:

$$\varphi = \frac{E_L \sin(-\alpha)}{E_o} = -\frac{E_L}{E}\sin\alpha \tag{2-2}$$

It is also concluded in [4] that under the presence of an injected signal, the instantaneous frequency would exceed ω_o by an amount which will produce a lag equal to φ. For locking frequencies close to the oscillator's natural frequency, this phase can be written as:

$$\varphi = A(\omega - \omega_0) = A[(\omega - \omega_l) - (\omega_o - \omega_l)] = A[\frac{d\alpha}{dt} - \Delta\omega_o] \tag{2-3}$$

where $A=2Q/\omega_o$ for small values of φ.

Combining equations (2-1) and (2-2) would result Adler's equation [4]:

$$\frac{d\alpha}{dt} = -\frac{E_l}{E}.\frac{\omega_o}{2Q}\sin\alpha + \Delta\omega_o \tag{2-4}$$

Equation (2-3) derives the instantaneous angular beat frequency, $\Delta\omega = d\alpha/dt$ as a function of the oscillator's natural frequency, oscillator voltage and injected signal amplitudes, and the phase relationship between them.

CHAPTER 3. High Frequency Clock Dividers

A frequency divider is a challenging block, especially for high-frequency and low-power operation used in high-speed communication systems. In this chapter, three different topologies, LC-tank, CML ring, and CML DFF frequency dividers are analyzed based on the following locking condition: As long as the frequency, $\omega_{inj} = \omega_o + \Delta\omega$ and the amplitude, A_{inj} of the injected signal *are in the desired operation region of the frequency divider's sensitivity curve,* a phase shift, $\varphi(A_{inj}, \omega_{inj})$ will be created and the oscillator is locked to the injected frequency.

The instantaneous frequency and phase of the frequency dividers are analyzed when the divider is under an injected signal. A new procedure is developed to measure any phase difference between two signals when the oscillator is locked. The simulations are using transistor models from TSMC 65nm CMOS process with the power supply voltage of 1.2V.

In the following sections, the three types of frequency dividers are discussed in detail.

3.1 High-Speed Frequency Divider Based on CML D Flip-Flop

Since the CML DFF frequency divider is primarily based on a CML structure, one of the key points to analyze this topology is the design and specifications of CML buffer.

3.1.1 CML Buffer

Figure 3-1 shows the structure and the dc characteristics of a simple resistive load CML buffer. In such structures, the large-signal characteristic of the transistors is of primary importance. In other words, the intention is to have the current steered completely from one leg to another at the target speed.

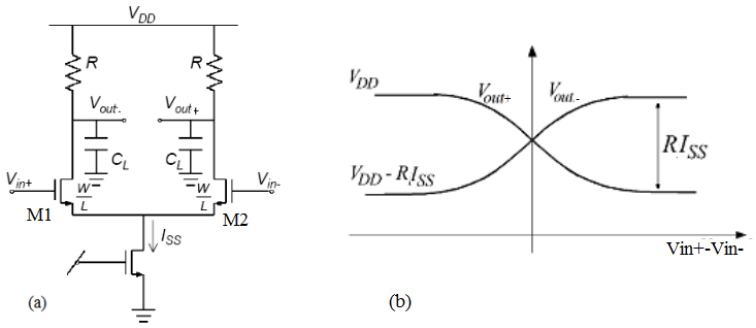

Figure 3-1 (a) CML differential pair [10], (b) Characteristics of a simple CML buffer [9].

To derive the voltage swing that is illustrated in Figure 3-1, the exact values of *high* and *low* output voltages should be determined. When the input voltage, V_{in+} goes high, the tail current I_{ss} is conducted through transistor M_1 and as a result V_{out-} falls to $V_{dd} - I_{ss}R$. Similarly V_{out+} reaches V_{dd}. These voltages correspond to output *low* and output *high*, respectively. The dc characteristics of a simple resistive load CML buffer is shown in Figure 3-1(b). Since output voltages *high* and *low* are $V_{High}=V_{dd}$ and $V_{Low}=V_{dd} - I_{ss}R$ respectively, the output swing voltage is, $V_{swing}= V_{High} - V_{Low}= I_{ss}R$ [10]. The condition to achieve full current switching is given by:

$$V_{swing} \geq (V_{GS} - V_t)_{Id=Iss} = \sqrt{\frac{2I_{ss}}{\mu_n C_{ox}\frac{W}{L}}} = V_{\min} \qquad (3\text{-}1)$$

where V_{min} is the minimum differential voltage that is required to completely turn off one transistor. By dividing both sides of (3-1) by V_{min}, we have $(V_{swing} / V_{min}) >1$ as the condition for current being fully switched [10].

Typical chosen V_{swing} is equal to $0.3\times V_{dd}$ to guarantee, 1) being large enough to allow sufficient gain-bandwidth product and 2) being small enough to prevent transistors from going into triode [10].

One systematic approach to size and bias CML structures for high-speed operations is to cascade three stages of similar buffers and connect an ideal signal source of the desired speed to

the input of the first buffer. This configuration represents a close to real condition for the middle buffer since its input signal is generated from a buffer with real load and its output stage is looking at a real load. The buffer size, both transistors and resistors, and bias condition should be made in such a way that when looked differentially, the input and the output of the second buffer have the same voltage swing. This ensures that 1) the input voltage swing is large enough to steer the current completely from one leg to another and also 2) provides similar voltage swing for the next stage. Having similar voltage swings at both input and output of middle buffer guarantees that signal logic will be passed through stages at the desired speed.

To determine low power consumption, considering the electro-migration constraints for the buffer, the proper value for current source, I_{ss} is chosen to be 400uA [10]. Assuming V_{dd} =1.2V, the typical swing voltage is equal to $V_{swing} = 0.3 \times V_{dd} = 0.4$V. On the other hand, $V_{swing} = I_{ss}R$, as a result the load resistance should be $R=1k$. Based on these values the proper W/L ratio of the transistors would be 60 which is resulted from simulation.

3.1.2 CML D Flip-Flop Divider

A simple topology of a divide-by-two D-flip-flop frequency divider, shown in Figure 3-2, consists of two cascaded D-latches with a negative feedback configuration.

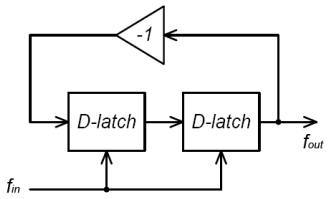

Figure 3-2 Topology of a DFF frequency divider.

A static DFF frequency divider, realized by current mode logic, (CML) with negative feedback is shown in Figure 3-3. The maximum operation frequency of this structure is generally limited by its parasitic capacitances.

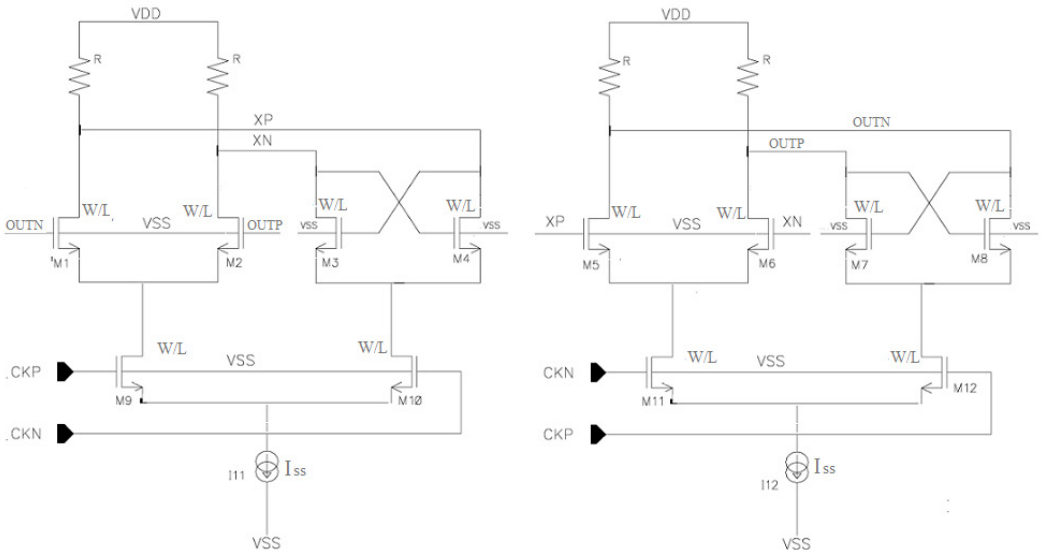

Figure 3-3 CML D Flip-Flop clock divider schematic.

Depending on the design specification, each CML D-latch can utilize different components and structures as output load. Initially, the static loads are implemented by fixed resistors. This implementation suffers from the process variations. However, it has the advantage of providing the same rising and falling times that are equal to $\tau=R\times C_L$. The load capacitance C_L is the sum of the buffer's gate-source parasitic capacitance $C_{gs,b2}$ of the second latch, the gate-source parasitic capacitance $C_{gs,c1}$ of cross-coupled transistor for the first latch, the buffer's drain-substrate parasitic capacitance $C_{ds,b1}$ for the first latch, and the drain-substrate parasitic capacitance $C_{ds,c1}$ of the cross-coupled for the first latch where $C_{gs} = \gamma C_{ox} WL$ [10].

The common-mode output voltage for the circuit shown in Figure 3-3, is given by:

$$V_{cm,out} = V_{dd} - 0.5 \times I_{ss} R \tag{3-2}$$

where $V_{cm,out}$ is the common-mode output voltage, V_{dd} is the power supply voltage, I_{ss} is the current source, and R is the resistor load. Because the output voltage of each D-latch is applied to the input voltage of another D-latch, $V_{cm,out} = V_{cm,in}$. Substituting V_{dd} =1.2V, I_{ss} = 400uA, and R=1k in equation (3-2), would result $V_{cm,out}$ =1V.

The optimum common-mode input clock voltage, $V_{cm,clk}$ that is applied to the clock inputs, CKP/N is found by varying the common-mode voltage using differential *dc* sweep runs. Define signals applied to the CKP/N inputs as $V_{cm} + V_{ramp}$ and $V_{cm} - V_{ramp}$ where V_{ramp} voltage is varied from –400mV to 400mV with step size of 10mV while the V_{cm} voltage is varied from 0.4V to 1V with step size of 0.1V. The drain currents of the clocked differential transistor pairs are then monitored. Simulation results for finding the optimum common-mode input voltage for CKP/N inputs are shown in Figure 3-4.

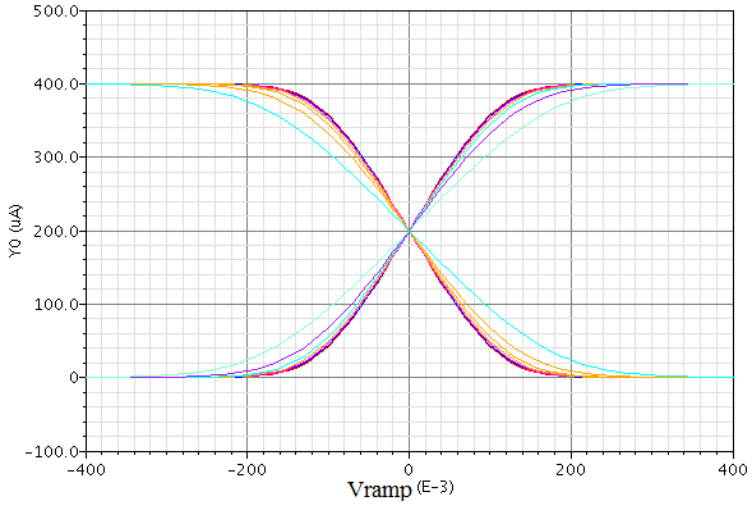

Figure 3-4 Finding optimum common-mode input voltage for CKP/N inputs.

The optimum input common-mode voltage occurs when the current is fully steered from one branch to another while all transistors stay in saturation region. If the common-mode input voltage goes higher, then the clock differential pair transistors can go into triode region, which decreases g_m. For a lower input common-mode voltage, the current source enters the triode

region. Based on the simulation result shown in Figure 3-4 and the common-mode output voltage value, $V_{cm,out}$ =1, and the optimal value for $V_{cm,clk}$ would be 0.6 volt subsequently.

The circuit parameters of the DFF frequency divider shown in Figure 3-3 are listed in Table 3-1.

Table 3-1 Circuit parameters of the DFF frequency divider.

Circuit Parameters	I_{ss}	V_{dd}	W/L	R
Value	400u	1.2v	60	0.9k

3.1.3 Plotting Sensitivity Curve

A clock divider can be accurately characterized by its sensitivity curve [3], which specifies the minimum injected input clock amplitude, at a given frequency, for the divider to lock.

The procedure that is used to plot the frequency divider's sensitivity curve is defined by following steps:

1) Find the self-oscillation frequency (F_{self}) when the clock amplitude is zero as shown in Figure 3-5(a).
2) Apply a differential sinusoid voltage to the differential *CKP/N* inputs with maximum clock amplitude (V_m) which is V_{swing} /2. Run a parametric analysis sweeping the clock frequency, for example from ω_o -10G to ω_o +10GHz. Monitor the frequency of differential output voltage using Cadence's "frequency" function. If the range is too wide or too narrow change it until to find the minimum (F_{Min-m}) and maximum (F_{Max-m}) frequencies that oscillator operates as the divide-by-two correctly as is shown in Figure 3-5(b).

3) Reduce the clock amplitude (V_{m-1}), and re-run the parametric analysis with frequency sweep range less than previous run. Similar to step (2) find the minimum ($F_{Min-m-1}$) and maximum ($F_{Max-m-1}$) frequencies which oscillator operates as the divide-by-two correctly.

4) Repeat step (3) until the clock amplitude will be close to zero is shown in Figure 3-5(c).

5) Connect the points in the following order

(F_{Min-m},V_m), ($F_{Min-m-1}$,V_{m-1}), ... (F_{self},0), ... ($F_{Max-m-1}$,V_{m-1}), (F_{Max-m},V_m)

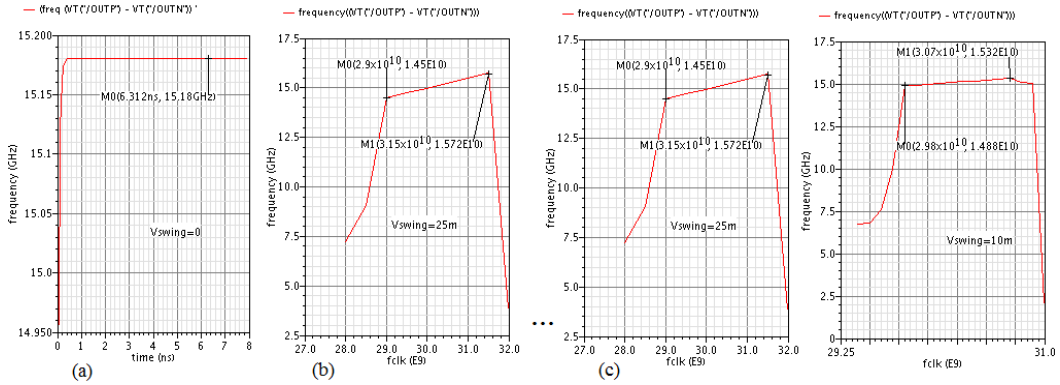

Figure 3-5 Sample of the simulation results for plotting the DFF divider's sensitivity curve.

Connecting the points to make the plot can be done in Excel or by running a skill code program which is loaded in Cadence's Interface Window, *CIW*. Based on the circuit parameter values given in Table 3-1 and the above procedure, the DFF frequency divider's sensitivity curve shown in Figure 3-6 is found by running a series of parametric transient simulations.

The CML DFF frequency divider has a very wide sensitivity curve such that $\Delta\omega$ is comparable with its ω_0 as shown in Figure 3-6, which is a desirable characteristic. It is important to note that, if the divider is to be used in a synthesizer, one of necessary conditions for locking is that the VCO frequency range should be within *the desired operation region of the frequency divider's sensitivity curve*.

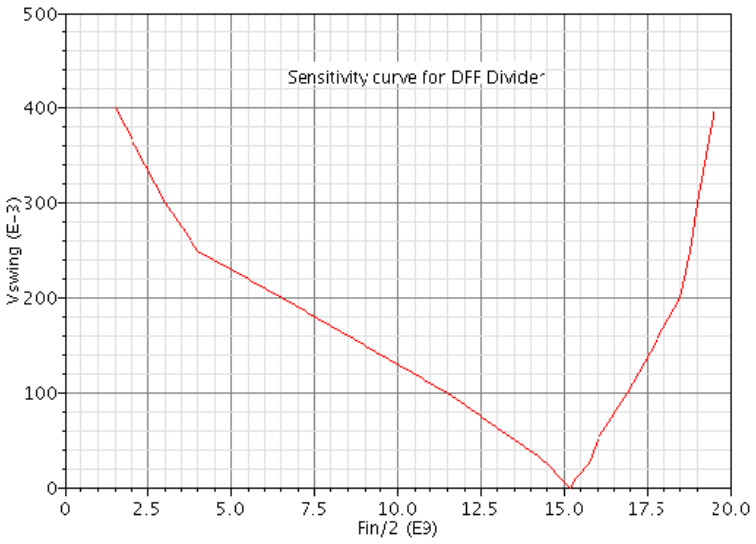

Figure 3-6 Sensitivity curve for the DFF frequency divider.

3.1.4 Procedure to Measure Phase Difference Between Two Signals

To measure the phase shift, φ when the oscillator is locked to the injected frequency a novel procedure is developed. This procedure gives us a very precise tool to measure the locking phase, instantaneous phase, or any phase shift between two signals inside the topology loop and provides a good ability for better understanding of injection locking concept and the behavior of the divider under an impressed signal. The procedure that is used to measure the phase difference between two signals is defined by following steps:

1) Run the transient simulations with the desired setup.
2) Find the time of zero crossing points for the rising edge of any two desired signals (voltage or current), Sig_1t_0, Sig_1t_1, ... Sig_1t_n and Sig_2t_0, Sig_2t_1, ... Sig_2t_n

   where Sig_1t_m is the time of the m^{th} zero crossing point of the first signal, Sig_1.
3) For all the zero crossing times (t_0, t_1, ... t_n), calculate the following:
   a. $Freq_m = 1/(Sig_1t_m - Sig_1t_{m-1})$ for m=0 ... n

where $Freq_m$ is the inverse of the time difference between two consecutive zero crossing points.

b. $Phase_m = 360 \times (Sig_2 t_m - Sig_1 t_m) \times Freq_m$ for m=0 ... n

where $Phase_m$ is the m^{th} phase shift between the two signals

Implementation of the procedure is done by a skill code program which is loaded in Cadence's Interface Window, *CIW* or in the ocean program.

3.1.5 Analyzing Instantaneous Frequency and Phase for DFF Divider

In this section, the variation of instantaneous frequency is analyzed. The instantaneous frequency can vary due to 1) changing the amplitude of the injection signal and/or 2) changing the phase between the injection signal and the oscillation output signal. When an external signal is injected to the loop of the oscillator, there is a transient duration that the amplitude and the instantaneous frequency (the difference between two consecutive zero crossing points) of the oscillation changes until the divider locks and they are settled. Note that the frequency and the amplitude of the injected signal should be in the desired operation region of the frequency divider's sensitivity curve in order to guarantee the locking happens.

To investigate the variation of instantaneous frequency, a differential sinusoid voltage signals is applied to the differential *CKP/N* inputs of the DFF frequency divider shown in Figure 3-3 when the DFF frequency divider is free running. Figure 3-7 shows an example of the injected signal and the resulting divider output signal.

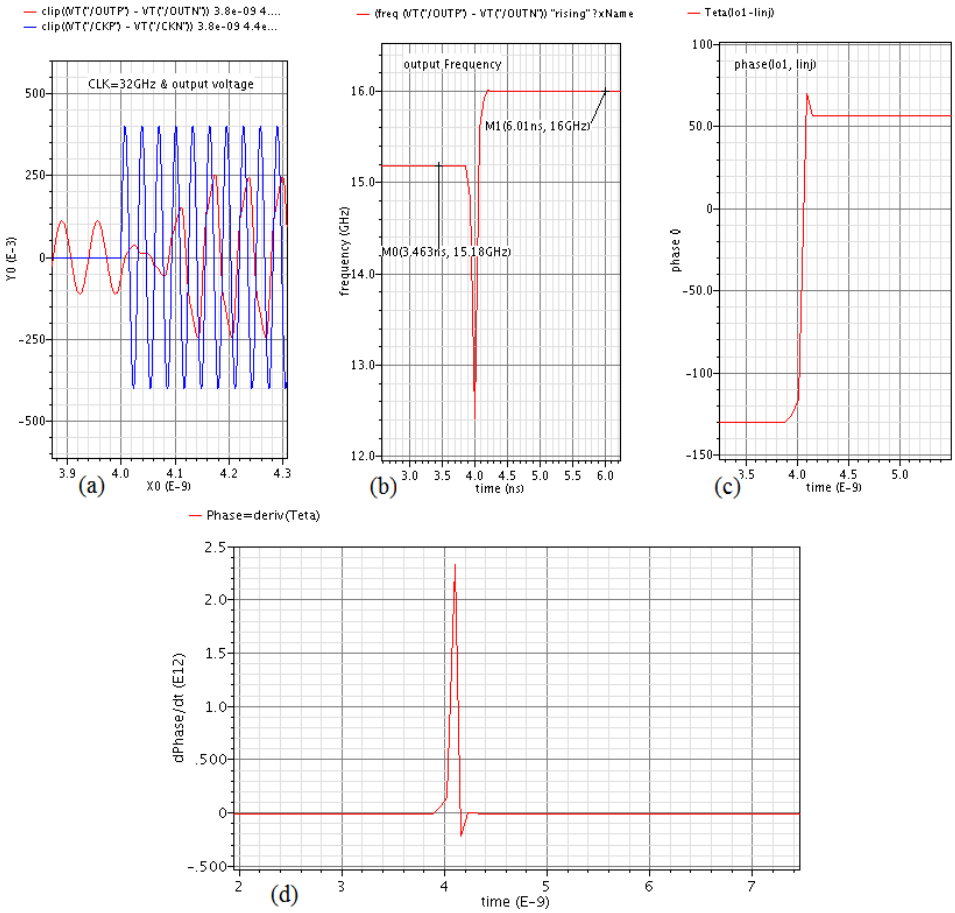

Figure 3-7 Simulation results for an injected signal and its effect on instantaneous frequency.

Figure 3-7(a) shows two signals: 1) the differential clock input with amplitude equal to 400mV and injection frequency equal to 32GHz which is applied at the starting time of 4ns and 2) the differential output of the DFF frequency divider which oscillates at free running frequency of 15.18GHz until 4ns and then locks after a few cycles to the 16GHz frequency that is half of the input 32GHz injection frequency. Figure 3-7(b) shows the locking states and also the transition of oscillation frequency between the two stable conditions. Figure 3-7(c) shows the phase between the output and injection currents. The derivative of the phase is zero when the divider locks to the frequency of the injected signal as shown in Figure 3-7(d).

To determine the variation of instantaneous frequency when the amplitude of the injection signal is changed, the following tests are done. Figure 3-8 shows the results.

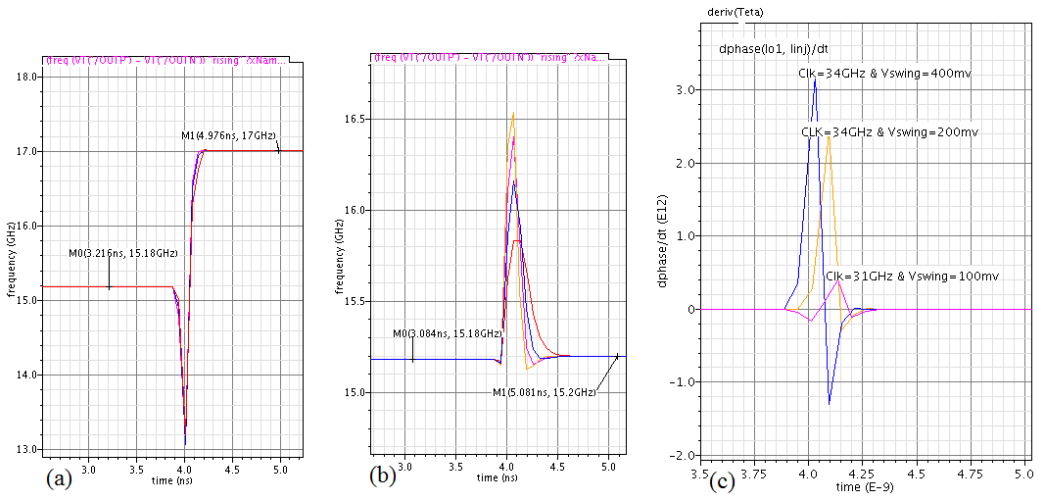

Figure 3-8 Simulation results when the clock amplitude is changed for DFF divider.

Figure 3-8(a) shows just a small change in the instantaneous frequency when the 34GHz clock amplitude is varied from 200mV to 400mV with the step size of 100mV. For clock amplitudes less than 50mV, the divider cannot lock to the 34GHz input frequency. Figure 3-8(b) shows the result when a 30.4GHz input clock amplitude is varied from 20mV to 50mV with the step size of 10mV. Simulation results show that amplitude variations of injection signal do not have notable impact on the instantaneous frequency. Figure 3-8(c) shows the derivative of the phase for a few cases when the divider locks to the frequency of the injected signal.

We now consider the effect of the time at which the injection signal is applied while the clock amplitude and frequency are held constant.

The starting time when the clock is injected to the divider, can occur anytime during the oscillation cycle. For example, it can occur around the zero crossing in rising or falling edges or in the peaks of the cycle.

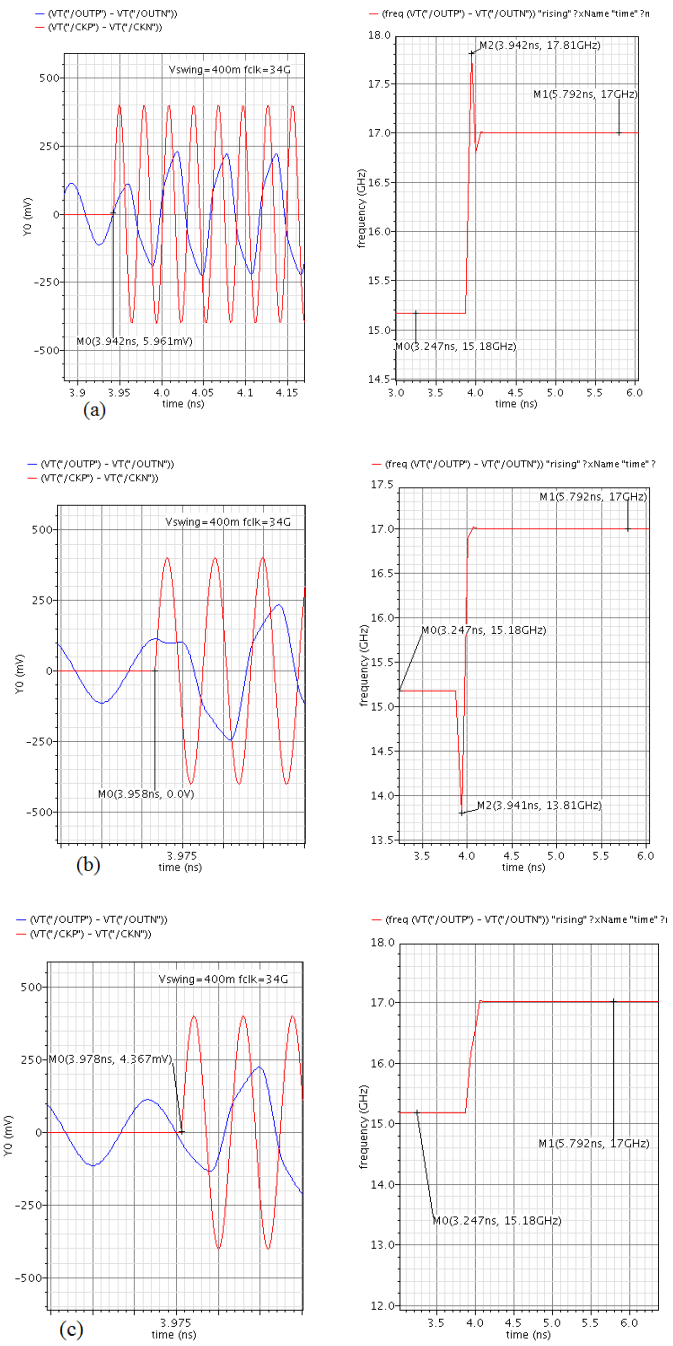

Figure 3-9 Simulation results when the clock is applied at different starting times for DFF divider.

Figure 3-9 shows the simulation result when the clock is applied to the divider at different stating times. Figure 3-9(a) shows the case when starting time is at 3.942ns and is around the zero crossing in the rising edge of oscillation cycle. Figure 3-9(b) shows the case when starting time is at 3.958ns and is around the peak of the oscillation cycle. Figure 3-9(c) shows the case

when starting time is at 3.978ns and is around the zero crossing in the falling edge of oscillation cycle. As the simulation results show, the instantaneous frequency is changed significantly by changing the phase between the injection signal and the oscillation signal. The transient response behavior and the settling time are both affected by the variation of the phase between the injection signal and the oscillation signal. However, in all cases the same steady-state behavior is reached.

More simulations are done to show how the settling time is affected by the variation of the phase between the injection and the oscillation signals. In the following tests the starting time to inject the clock is changed by constant step size during one period of the divider oscillation. Figure 3-10 shows the simulation results.

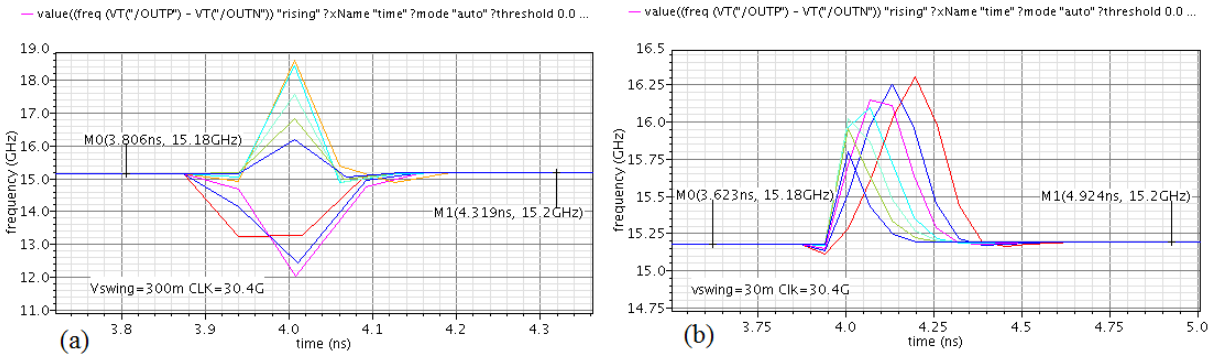

Figure 3-10 Transient response due to phase variations of the injection signal for DFF divider.

Figure 3-10(a) shows the results when the starting time to inject the clock is changing from 3.997ns to 4.007ns with the step size of 1ps. The clock amplitude is 300mV and its frequency is constant and equal to 30.4GHz. Figure 3-10(b) shows the simulation results when the clock amplitude is reduced to 30mV.

Simulation results show that the settling time is affected significantly by the variation of the phase between the injection and the oscillation signals and the injection signal amplitude. By

controlling the clock amplitude and the starting time to inject the clock, the settling time can be reduced and as a result a faster locking to the injected frequency occurs.

3.2 High-Speed Frequency Dividers Based on CML Ring

The problem with a CML divide-by-two D-flip-flop frequency divider is that the output nodes of two D-latches see a large capacitance load. The cross-coupled transistor pair used in the D-latch is one of the main contributors to the output capacitance [3]. Different techniques and topologies are suggested to reduce [1], [7] or eliminate [3] the parasitic capacitance of the cross-coupled transistor pair. One of the topologies that eliminates the cross-coupled transistor pairs, is the CML ring frequency divider which is realized by CML buffers as shown in Figure 3-11.

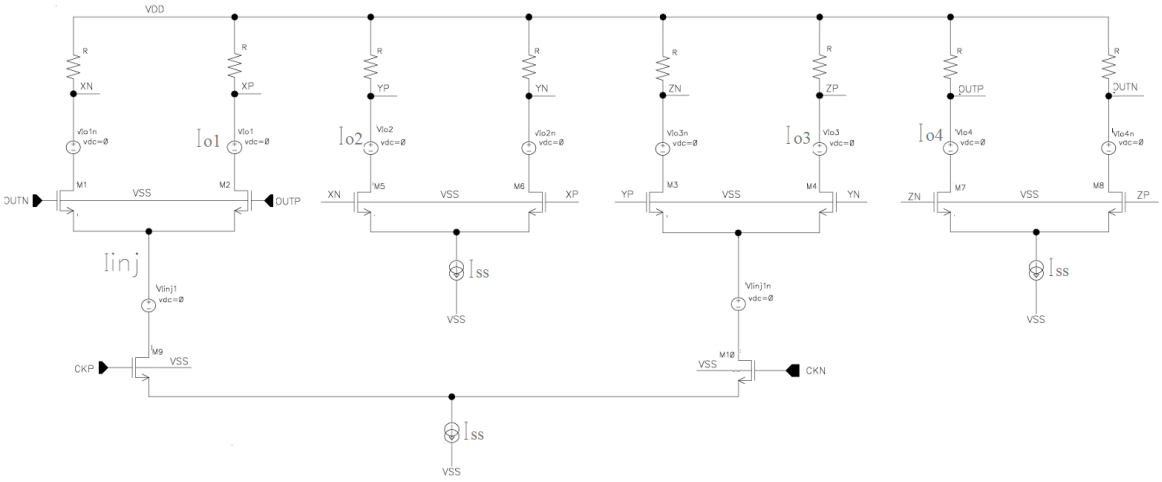

Figure 3-11 CML ring clock divider schematic.

By eliminating the cross-coupled transistor pair as shown in Figure 3-11, the capacitance at output nodes is reduced and as a result the higher speed can be achieved [3]. However, it has the same rising and falling times that are equal to $\tau=RC_L$ which C_L is defined by $C_L = C_{ds,bi} + C_{gs,b(i+1)}$. The capacitance, $C_{ds,bi}$ is the buffer's drain-substrate parasitic of any given buffer and capacitance $C_{gs,b(i+1)}$ is the buffer's drain-substrate parasitic of the following buffer, where C_{gs} =

$\gamma C_{ox}WL$ [10]. As a result the load capacitance size, C_L of the CML ring frequency divider is the half of the load capacitance size of the CML DFF frequency divider.

The CML ring frequency divider exhibits a substantial increase in the maximum frequency with the wide range of operation. In this configuration CML buffers function as both low-pass filter and amplifier., Also the CML buffer functions as a single balanced mixer when a full rate clock is applied. A realization of single balanced mixer is shown in Figure 3-12.

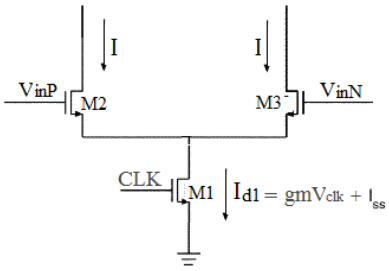

Figure 3-12 Realization of single balanced mixer.

It is assumed all the transistors are in saturation region and identical. When a sinusoidal clock signal, V_{CK} is applied to the *CLK* input, the drain current of the transistor M_1, will be $I_{d1}=(g_mV_{CK}+I_{ss})$. The clock signal is defined as $V_{CK}=A\cos\omega t$. A differential sinusoid voltage is applied to the differential $V_{inP/N}$ inputs and the positive input is $V_{inP}=B\cos\omega_o t$. This is a time variant linear system, therefore $I = I_{d1} \times I_{in}$, where I_{in} is $g_mV_{inP/N}$, subsequently:

$$I = (I_{ss} + g_mV_{CK}) \times g_mV_{inP/N} \tag{3-3}$$

By substituting $V_{CK}=A\cos\omega t$ and $V_{inP/N}=B\cos\omega_o t$ in (3-3), the result would be:

$$I = (I_{ss} + g_mA\cos\omega t) \times g_mB\cos\omega_o t$$

$$I = I_{ss}g_mB\cos\omega_o t + g_m^2AB\cos\omega t\cos\omega_o t \tag{3-4}$$

We know that $\cos\omega_o t \times \cos\omega t = 1/2(\cos(\omega - \omega_o)t + \cos(\omega + \omega_o)t)$, and $\cos(\omega + \omega_o)t$ is filtered out by its *RC* low pass filter. Therefore (3-4) can be simplified to:

$$I = I_{ss} g_m B \cos \omega_o t + \frac{1}{2} g_m^2 AB \cos(\omega - \omega_o)t \quad (3\text{-}5)$$

When the divider is locked, ω is equal to $2\times\omega_o$, (3-5) can be written as:

$$I = K \cos \omega_o t \quad (3\text{-}6)$$

where $K = I_{ss}\, g_m B + 0.5\mathrm{AB}(g_m)^2$.

3.2.1 Circuit Parameters Design

The CML buffer presented in Section 3.1.1 is used in the ring oscillator design. When I_{ss} is set to 600uA and V_{swing} is set to 0.4V, R=0.9k. The transistor size of the ring buffers have the same ratio W/L of 60 as the previously designed CML buffer's transistor size.

The common-mode output voltage, $V_{cm,out}$ for the circuit that is shown in Figure 3-11, is $V_{cm,out} = V_{dd} - 0.5\times I_{ss}R$. Because the output voltage of each buffer is applied to the input voltage of next buffer, we have $V_{cm,out} = V_{cm,in}$, where $V_{cm,in}$ is the common-mode input voltage for each buffer. By knowing V_{dd} =1.2V, I_{ss} = 600uA, and R=0.9k, we have $V_{cm,out} = V_{cm,in}$ =0.93V.

The optimum common-mode input clock voltage, $V_{cm,clk}$ that is applied to the clock inputs, CKP/N inputs is the same as DFF frequency divider's common-mode input clock voltage. The optimal value for $V_{cm,clk}$ is 0.6V. The circuit parameters of the ring frequency divider shown in Figure 3-11 are listed in Table 3-2.

Table 3-2 Circuit parameters of the ring frequency divider.

Circuit Parameters	I_{ss}	V_{dd}	W/L	R
Value	600uA	1.2V	60	0.9k

3.2.2 CML Ring Frequency Divider's Sensitivity Curve

The procedure that is defined in Section 3.1.3 is used to plot the sensitivity curve of the ring frequency divider shown in Figure 3-11. Based on the circuit parameter values in Table 3-2 and the defined procedure, the points are obtained to plot the sensitivity curve. In the first step, the self-oscillation frequency is found. Figure 3-13 shows the self-oscillation frequency of the ring frequency divider.

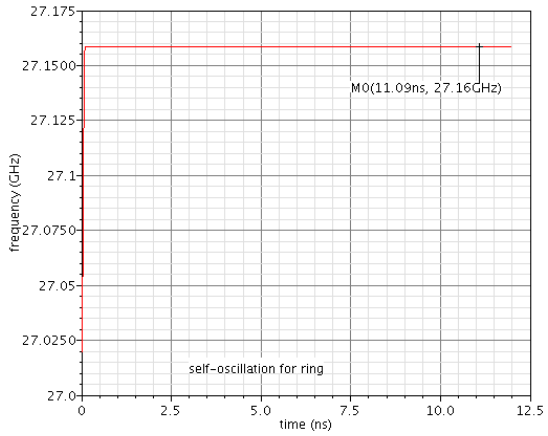

Figure 3-13 Self oscillation frequency for ring divider.

Figure 3-13 gives the (F_{self},0) point in the sensitivity curve, where F_{self}=27.16GHz is the self-oscillation frequency when clock amplitude is zero volts. In next steps all the points (F_{Min-m},V_m) and (F_{Max-m},V_m), the minimum and maximum output frequencies when clock amplitude is defined at certain value in the sensitivity curve are found. For example when the clock amplitude is 400mV, the simulation gives two points as shown in Figure 3-14.

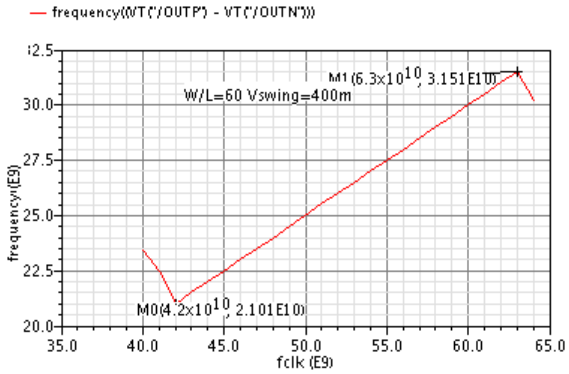

Figure 3-14 An example of finding two points in the sensitivity curve for V_m=400mV.

Figure 3-14 provides the (21GHz, 400mV) and (31.5GHz, 400mV) points in the sensitivity which are the minimum and maximum output frequencies that divider locks when clock amplitude is 400mV. When clock amplitude is varied, the minimum and maximum output frequencies that divider locks will be changed. Therefore, similar to this example all the points are found and connected to plot the ring frequency divider's sensitivity curve shown in Figure 3-15.

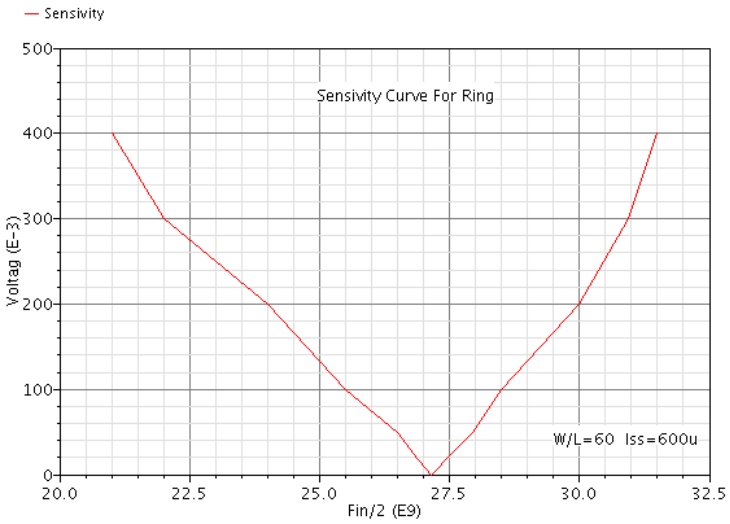

Figure 3-15 Sensitivity curve for 4-stage ring frequency divider.

In summary CML ring frequency divider has a wide sensitivity curve, but is not as wide as CML DFF frequency divider sensitivity curve and its self-oscillation frequency is also higher.

3.2.3 Analyzing Instantaneous Frequency and Phase Shift

The variation of instantaneous frequency is analyzed similar to CML DFF frequency divider. As described in Section 3.1.5, the instantaneous frequency can vary due to 1) changing the amplitude of the injection signal and/or 2) changing the phase between the injection signal and the oscillation output signal by applying the injection signal at different starting time during the oscillation cycle. To investigate the variation of instantaneous frequency, a differential sinusoidal voltage signal is applied to the differential CKP/N inputs of the CML ring frequency divider shown in Figure 3-11 when the ring frequency divider oscillates in its free running frequency. It should be noted that the frequency and the amplitude of the injected signal should be in the desired operation region of the divider's sensitivity curve in order to guarantee that locking occurs. Figure 3-16 shows an example of the injected signal and the resulting divider output signal.

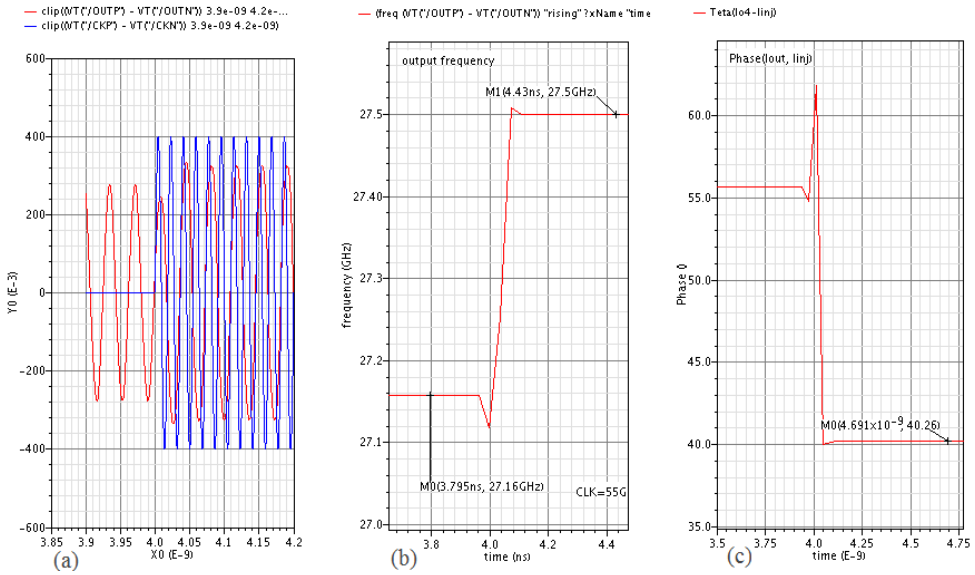

Figure 3-16 An example of the effect of an injected signal on instantaneous frequency and phase for ring divider.

As shown in Figure 3-16(a), the differential clock input with amplitude equal to 400mV and injection frequency equal to 55GHz is applied with starting time of 4ns. It also shows the differential output of the ring frequency divider which oscillates at free running frequency until 4ns and then locks after a few cycles to the 27.5GHz frequency that is half of the 55GHz injected clock frequency. Figure 3-16(b) shows the locking states and also the transition of oscillation frequency between the two stable conditions. Figure 3-16(c) shows the phase between the output and injection currents.

To investigate the variation of instantaneous frequency and phase as a result of variations of the injection signal amplitude, the following tests are done. Figure 3-17 shows the results.

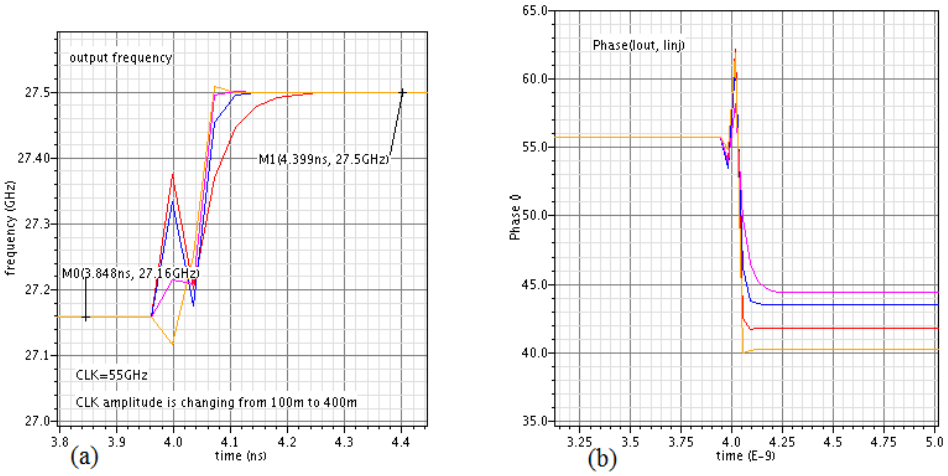

Figure 3-17 Simulation results when the clock amplitude is changed for ring divider.

Figure 3-17(a) shows the zero crossing changes while the clock amplitude is varied. The 55GHz clock signal is injected at starting time equal to 4ns and is varied from 100mV to 400mV with the step size of 100mV. Figure 3-17(b) shows the phase between the output current and injection current when the 55GHz clock amplitude is varied from 100mV to 400mV with the step size of 100mV. Simulation results show, when the injection signal amplitude changes 1) it does not have notable impact on the instantaneous phase but the locking phase is changed and 2) it has

a notable impact on the instantaneous frequency and the settling time. The settling time increases when the injection signal amplitude decreases.

Now, the clock amplitude and frequency are held constant while the starting time to inject the clock is changed. The following tests show the effect of the different starting time to apply the clock on the instantaneous frequency. The starting time can occur at anytime during the oscillation cycle. Figure 3-18 shows an example of the injected signal and the resulting divider output signal, while the starting time to inject the clock is changed.

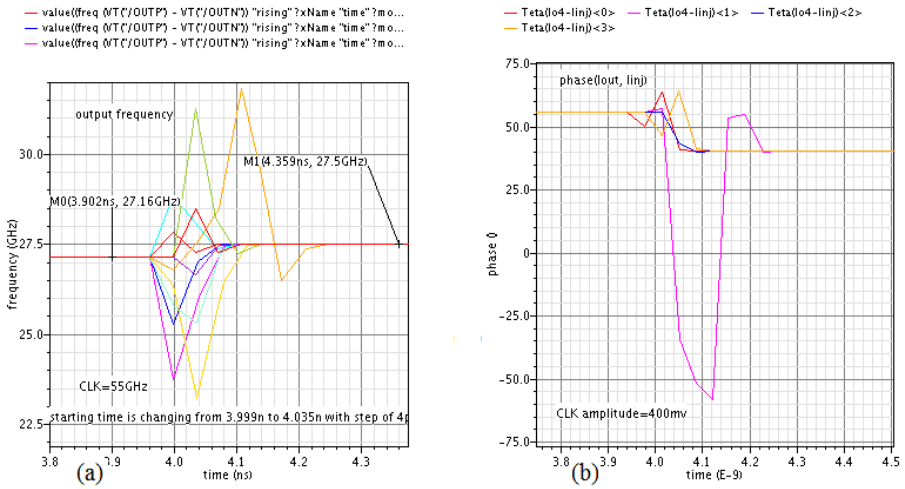

Figure 3-18 Simulation results when the clock is applied at different starting times for ring divider.

Figure 3-18(a) shows the result when the starting time to inject the55GHz, 400mV clock is changing from 3.999ns to 4.035ns with a step size of 4ps. Figure 3-18(b) shows the phase between the output current and injection current when the starting time to inject the clock is varied from 3.999ns to 4.035ns with the step size of 4ps. Simulation results show when the starting time to inject the clock is changing while the clock signal amplitude and clock frequency are constant: 1) it has a notable impact on the instantaneous phase but the locking phase is not changed and 2) it has a significant impact on the instantaneous frequency and the settling time.

The settling time decreases when the starting time of the injection signal is around the zero crossing of oscillation cycle.

The time derivative of the phase difference between I_{out} and I_{inj} becomes zero and when the frequency divider locks. Figure 3-19(a) shows this behavior during the self-oscillation and when it locks to injected signal's frequency.

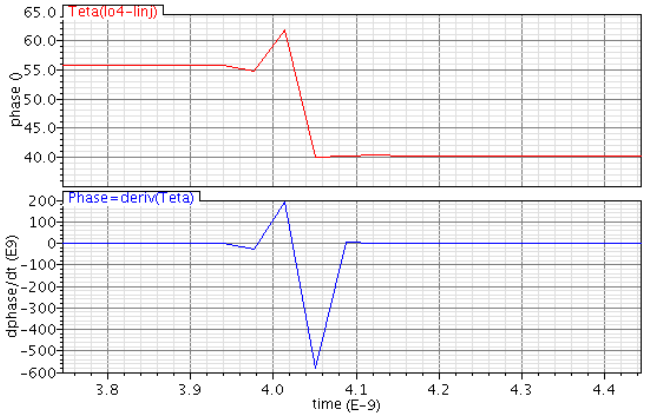

Figure 3-19 The instantaneous phase due to injection signal for ring divider.

3.3 High-Speed Frequency Dividers Based on LC-tank Oscillator

The LC-tank oscillator can be designed as either single-ended or differential type. The differential type has higher rejection of common mode interferers and stronger attenuation of even-order harmonics than the single-ended type. Therefore, the differential type is commonly required in most applications although it needs more components and consumes more power. The LC-tank frequency divider is realized by a differential LC-tank oscillator where input clock is fed through the source as shown in Figure 3-20.

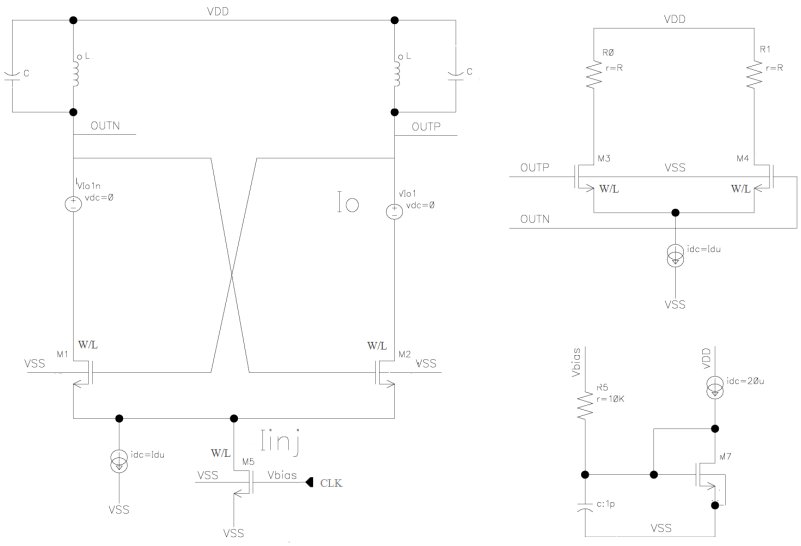

Figure 3-20 LC-tank frequency divider schematic.

The resonant frequency of the tank is $\omega_o = 1/\sqrt{LC_L}$. This type of divider is suitable for very high-frequency operation, however, it occupies a large area due to the on-chip inductor.

To design of the LC-tank oscillator parameters circuit, we use the same transistor size that is used in the DFF and ring frequency dividers. The current source, I_{ss} was set to 400uA. As shown in Figure 3-20, the divider output is connected to the input of a CML buffer to provide a realistic load capacitance. The capacitance C_L is the sum of the gate-source parasitic capacitance, $C_{gs,b}$ of the buffer, the gate-source parasitic capacitance $C_{gs,c}$ of the cross-coupled transistor pair, the drain-substrate parasitic capacitance $C_{ds,c}$ of the cross-coupled transistor pair, the tank capacitor, C, and parasitic capacitance of the inductor $C_{P,L}$ where $C_{gs} = \gamma C_{ox} WL$ [10] and $C_{P,L}=1/(L\omega^2_{SRF})$. For this circuit the self-resonant frequency of the inductor is 5 times the self-oscillation frequency. Based on simulation results, the proper value for inductor is 1nH. The circuit parameters of the LC-tank frequency divider shown in Figure 3-20 are listed in Table 3-3.

Table 3-3 Circuit parameters of the LC-tank frequency divider.

Circuit Parameters	I_{ss}	V_{dd}	W/L	L	C	C_L
Value	400uA	1.2V	60	1nH	3.69fF	13.16fF

3.3.1 LC-tank Frequency Divider's Sensitivity Curve

The procedure that is defined in Section 3.1.3 is used to plot the sensitivity curve of the LC-tank frequency divider shown in Figure 3-20. Based on the circuit parameters value in Table 3-3, the points are obtained to plot the sensitivity curve. In the first step, the self-oscillation frequency is found. Figure 3-21 shows the self-oscillation frequency of the LC-tank frequency divider.

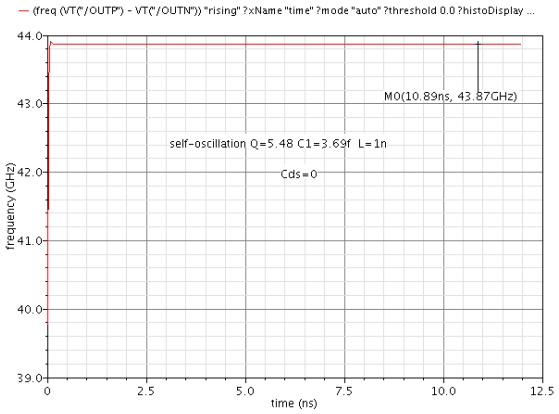

Figure 3-21 Self oscillation frequency for LC-tank frequency divider.

Figure 3-21 gives the (F_{self},0) point in the sensitivity curve, where F_{self}=43.87GHz is the self-oscillation frequency when clock amplitude is zero volts. By varying the amplitude, the points (F_{Min-m},V_m) and (F_{Max-m},V_m) in the sensitivity curve will be found. Figure 3-22 shows an example that is used to find the minimum and maximum output frequencies that divider locks when the clock amplitude is 400mV, 300mV, 200mV, or 100mV.

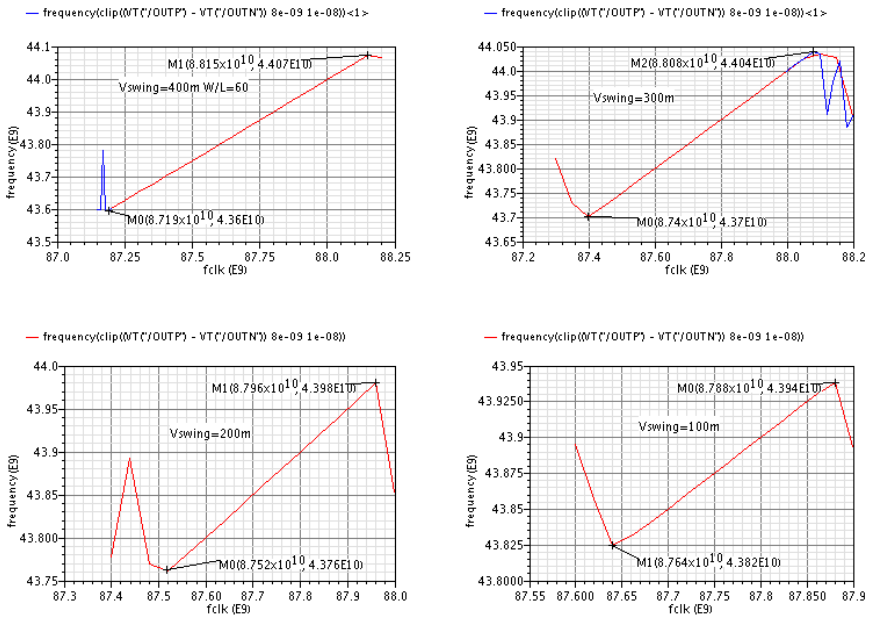

Figure 3-22 An example to find (F_{Min-m},V_m) and (F_{Max-m},V_m) points for the LC-tank divider.

Figure 3-22 gives (43.6GHz, 400mV) and (44.07GHz, 400mV) points for the minimum and the maximum output frequencies that divider locks when clock amplitude is 400mV. For clock amplitude of 300mV, (43.7GHz, 300mV) and (44.04GHz, 300mV) points are found. For clock amplitude of 200mV, (43.76GHz, 200mV) and (43.98GHz, 200mV) points and for 100mV (43.82GHz, 100mV) and (43.94GHz, 200mV) points are found respectively. Similar to this example more points are found and connected to plot the LC-tank frequency divider's sensitivity curve as shown in Figure 3-23.

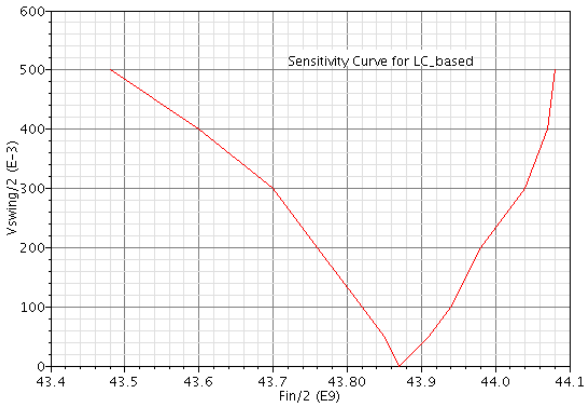

Figure 3-23 Sensitivity curve for LC-tank frequency divider.

The LC-tank frequency divider has a very narrow sensitivity curve, but its self-oscillation frequency is much higher than the other two topologies. This frequency divider is capable to have a much higher self-oscillation frequency, therefore suitable to be used in some applications for very high frequency operation.

3.3.2 Analyzing Instantaneous Frequency and Phase Shift for LC-tank

The variation of instantaneous frequency for the LC-tank is analyzed similar to the other two frequency dividers. As described in Section 3.1.5, the instantaneous frequency can vary due to 1) changing the amplitude of the injection signal and/or 2) changing the phase between the injection signal and the oscillation signal by applying the injection signal at different starting time during the oscillation cycle.

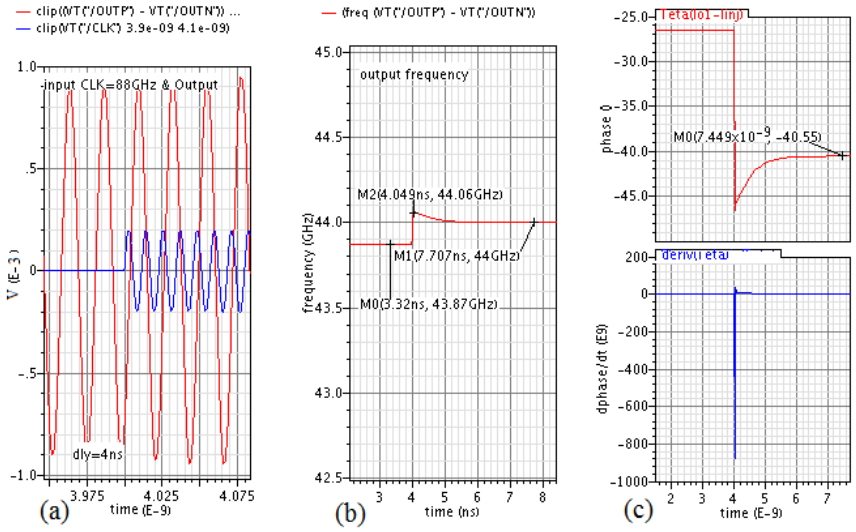

Figure 3-24 An injected signal and its effect on LC-tank frequency divider's output.

To investigate the variation of instantaneous frequency, a sinusoidal voltage signal is applied to the clock input, CLK of the LC-tank frequency divider shown in Figure 3-20 when the LC-tank frequency divider oscillates in its free running frequency. It should be noted that the

frequency and the amplitude of the injected signal should be in the desired operation region of the LC-tank frequency divider's sensitivity curve in order to guarantee that locking happens.

Figure 3-24 shows an example of the injected signal and the resulting divider oscillation output signal. As shown in Figure 3-24(a), the clock input with amplitude equal to 400mV and injection frequency equal to 87.9GHz is applied with starting time at 4ns. It also shows the differential output of the LC-tank frequency divider which oscillates at free running frequency until 4ns and then locks after a few cycles to the 43.95GHz frequency that is half of the 87.9GHz injected frequency. Figure 3-24(b) shows the locking states and also the transition of oscillation frequency between the two stable conditions. Figure 3-24(c) shows the phase difference between the output and injection signal and also shows the time derivative of the phase that is equal to zero when the divider locks.

To determine the variation of instantaneous frequency as a result of changing the amplitude of the injection signal while the injected frequency and the starting time to inject the clock are held constant, the following tests are done. Figure 3-25 shows the results.

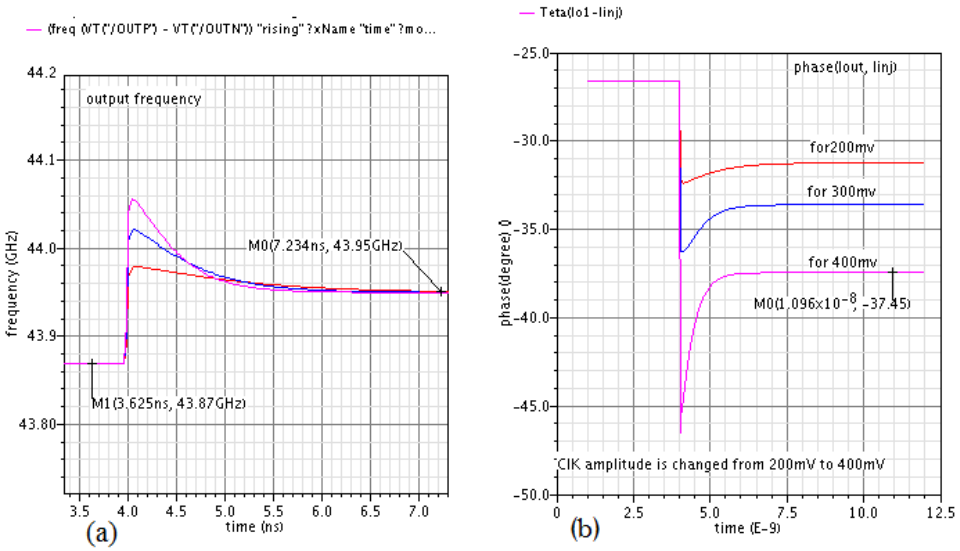

Figure 3-25 Simulation results when the clock amplitude is changed for LC-tank divider.

Figure 3-25(a) shows that the transition response changes while the 87.9GHz clock amplitude that is injected at starting time equal to 4ns, is varied from 200mV to 400mV with a step size of 100mV. Figure 3-25(b) shows the variations of phase when the 87.9GHz clock amplitude is varied from 200mV to 400mV with the step size of 100mV. Simulation results show, when the injection signal amplitude changes, it has a notable impact on the instantaneous frequency and the settling time. The settling time increases when the injection signal amplitude decreases. They also show that the locking phase between the output and injection signal is changing when the clock amplitude is varied.

Now, the clock amplitude and frequency are held constant while the starting time to inject the clock is changed. The following tests show the effect of the different starting time to apply the clock on the instantaneous frequency. The starting time can occur at any time during the oscillation cycle. Figure 3-26 shows an example of the injected signal and the resulting divider's oscillation output signal, while the starting time to inject the clock is changed.

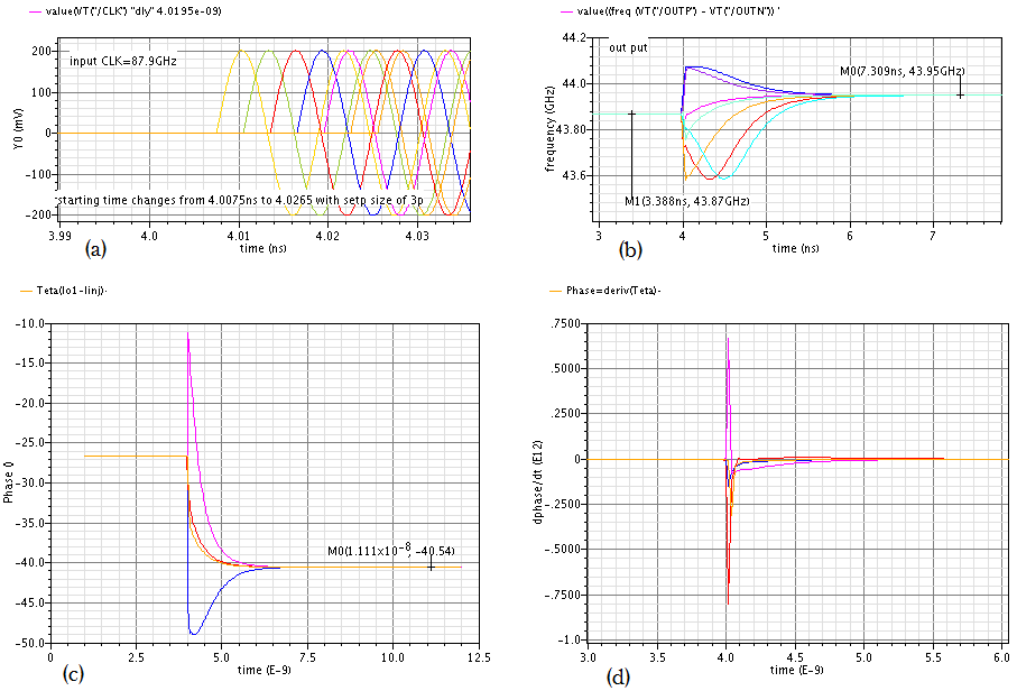

Figure 3-26 Simulation results when the clock is applied at different starting times for LC-tank divider.

Figure 3-26(a) shows the clock when the injection starting time is changing from 4.007ns to 4.026ns with a step size of 3ps. The 87.9GHz clock amplitude is set to 100mV. Figure 3-26(b) shows the transient response behavior of oscillation frequency between the two stable conditions when the starting time to inject the signal is changing. Figure 3-26(c) and Figure 3-26(d) show the variations of instantaneous phase when the injection starting time is changing from 4.007ns to 4.026ns with a step size of 3ps. The simulation results show that the instantaneous frequency, settling time and instantaneous phase are changed significantly by the variation of the phase between the injection signal and the oscillation output signal. And also show that the locking phase between the output and injection signal is constant when the starting time to inject the signal is varied.

Figure 3-27 shows an example of the variation of instantaneous output frequency as a result of changing the amplitude of the injection signal and the starting time to inject the clock while the injected frequency is constant.

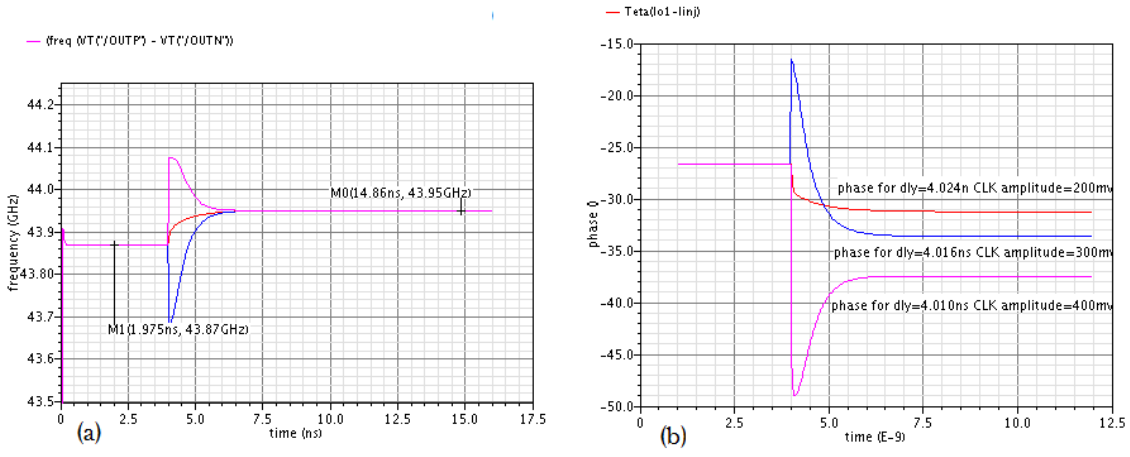

Figure 3-27 Simulation results when the clock amplitude and injection starting times are varied.

Figure 3-27 shows the changes in the transition response while the 87.9GHz clock amplitude is varied from 400mV to 200mV with a step size of 100mV and also the starting time to inject the clock is changing from 4.01ns to 4.024ns with a step size of 6ps. The simulation

results show that the instantaneous frequency and settling time are changed significantly and the locking phase between the output and injection signal is changed when the clock amplitude is varied.

CHAPTER 4. Analyzing Locking Phase

In this section, three different topologies, LC-tank frequency divider, CML ring frequency divider, and CML DFF frequency divider, will be modeled. Based on model and topology, the locking and the instantaneous phase equations will be derived. The analytical results will be compared and discussed with the simulation results.

4.1 LC-Tank Frequency Dividers

For simplicity of the analysis, a differential half rate frequency current is injected into the tank nodes instead of the clock voltage with full rate frequency as shown in Figure 4-1.

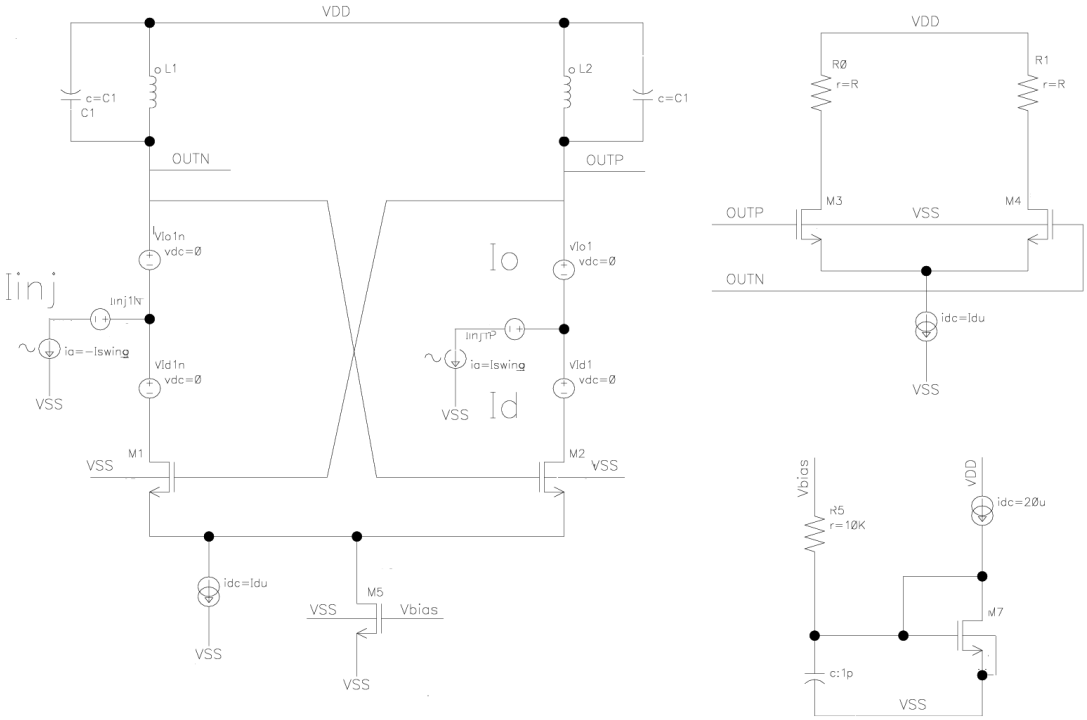

Figure 4-1 Schematic of the LC-tank frequency divider with current injected to the tank nodes.

This circuit shown in Figure 4-1 can be modeled as shown in Figure 4-2.

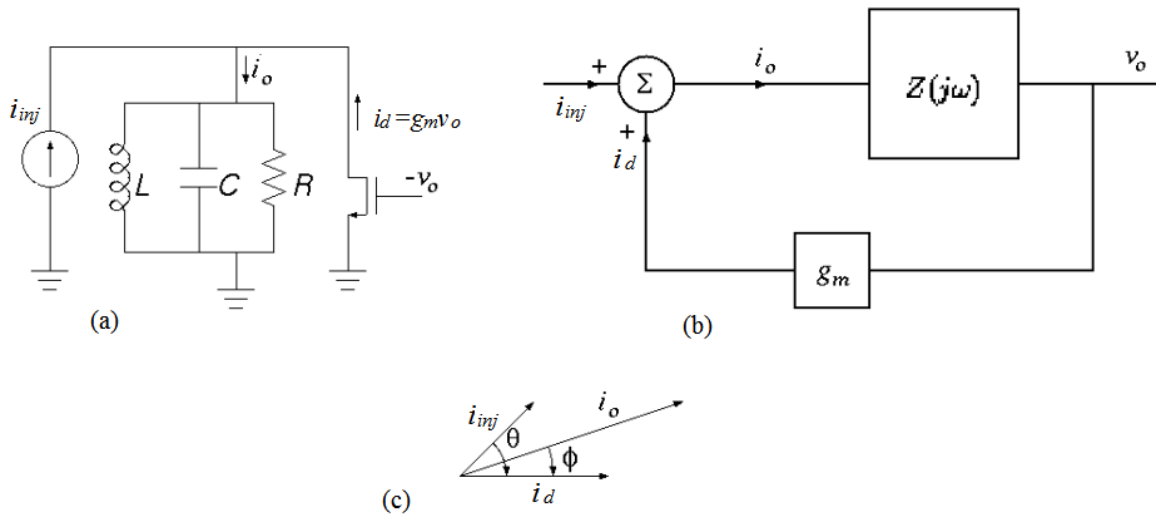

Figure 4-2 (a) Equivalent circuit, (b) Block diagram and (c) Vector representation of LC-tank divider.

An equivalent circuit for the LC-tank divider is shown in Figure 4-2(a), where i_{inj} is the injected current, i_d is the feedback current, and their sum is output current, $i_o = i_d + i_{inj}$. The block diagram equivalent is shown in Figure 4-2(b). A vector representation of the three currents is shown in Figure 4-2(c) where the locking phase, φ is the angle between the feedback current i_d and the sum current i_o, which goes to the load; phase θ is the angle between the feedback current i_d and the current i_{inj} that is injected into the drain.

Using the procedure to measure phases described in Section 3.1.1, Figure 4-3 is the simulated vector representation of the three currents in Figure 4-2(c).

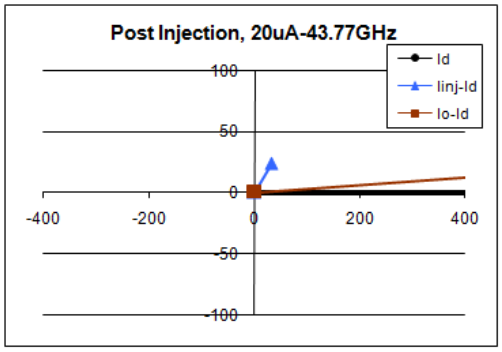

Figure 4-3 An example of simulation results showing vector representation of the three.

From Figure 4-2(c), we can write the sum current i_o as a complex number by the following relation:

$$i_o = i_d + i_{inj}\cos\theta + j i_{inj}\sin\theta$$

$$\tan\varphi = \frac{i_{inj}\sin\theta}{i_d + i_{inj}\cos\theta} = \frac{i_{inj}}{i_d}.\frac{\sin\theta}{1+\frac{i_{inj}}{i_d}\cos\theta} \tag{4-1}$$

This is an important periodic function that appears in any type of divider. The graph in Figure 4-4 shows one period of the negative of this function for three different values of the modulation index i_{inj}/i_d:

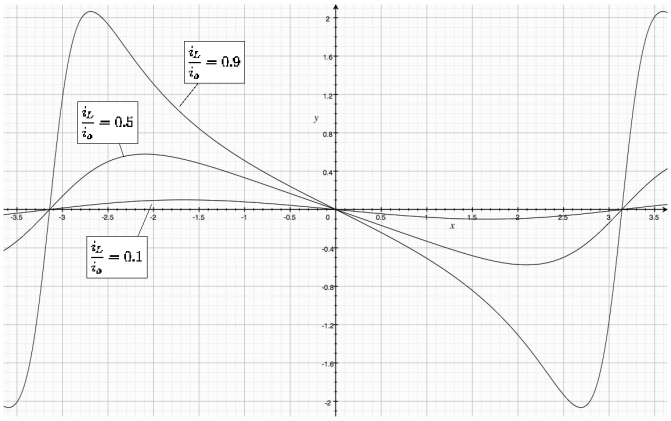

Figure 4-4 Periodic function that appears in any type of divider.

To find the phase shift, first the output impedance should be formulated. The output impedance, $Z(j\omega)$ for LC-tank can be written as:

$$Z(j\omega) = \frac{j\omega L}{(1-\omega^2 LC) + j\omega\frac{L}{R}} \tag{4-2}$$

where R, C, and L are the output resistance, capacitance, and inductance, respectively and the phase shift of this impedance is given by:

$$\varphi = \arg[Z(j\omega)] = \frac{\pi}{2} - \tan^{-1}\left(\frac{\omega\frac{L}{R}}{1-\omega^2 LC}\right) \tag{4-3}$$

We have $\tan^{-1}\alpha = \frac{\pi}{2} - \tan^{-1}\alpha^{-1}$, and (4-3) can be rewritten as:

$$\varphi = f(\omega) = \tan^{-1}(\frac{1-\omega^2 LC}{\omega\frac{L}{R}}) \tag{4-4}$$

Assuming $\omega=\omega_o+\Delta\omega$ is in the desired operation region of the frequency divider's sensitivity curve, then the Taylor expansion for $f(\omega)$ around ω_o would be:

$$\varphi = f(\omega) = f(\omega_o) + f'(\omega_o)(\omega-\omega_o) + f''(\omega_o)(\omega-\omega_o)^2 + ... \tag{4-5}$$

where $\omega_o = \frac{1}{\sqrt{LC}}$ is the self-oscillation frequency of the divider. Then we can write the following:

$$f(\omega_o) = \tan^{-1}(\frac{1-\omega_o{}^2 LC}{\omega_o\frac{L}{R}}) \tag{4-6}$$

As expected, phase shift at the self-oscillation frequency is equal to zero.

To find the first-order term of (4-5), using $\frac{d}{dx}\tan^{-1}u = \frac{1}{1+u^2}\frac{du}{dx}$ and assuming $u = \frac{1-\omega_o{}^2 LC}{\omega_o\frac{L}{R}}$, we have:

$$f'(\omega_o) = \frac{1}{1+(\frac{1-\omega_o{}^2 LC}{\omega_o\frac{L}{R}})^2}\cdot\frac{-2\omega_o{}^2 L^2 C/R - (1-\omega_o{}^2 LC)L/R}{\omega_o{}^2\frac{L^2}{R^2}} \tag{4-7}$$

By substituting $\omega_o = \frac{1}{\sqrt{LC}}$ in (4-7), it simplifies to $f'(\omega_o) = -2RC$, therefore we have:

$$f'(\omega_o)(\omega-\omega_o) = -2RC(\omega-\omega_o) \tag{4-8}$$

If we multiply and divide the equation (4-8) by ω_o, we will have:

$$\varphi = -2R.\sqrt{\frac{C}{L}}.\frac{\Delta\omega}{\omega_o} \tag{4-9}$$

The sensitivity curve for this topology is very narrow and we can assume $\Delta\omega << \omega_o$ for any ω chosen in the desired frequency divider operation region of its sensitivity curve. Considering the typical ω_o and $\Delta\omega$ provided in Table 4-1, $\Delta\omega/\omega_o < 0.01$ and consequently $(\Delta\omega/\omega_o)^2 < 10^{-4}$. Therefore, the second-order term can be ignored.

Now, we should investigate the correctness of assuming *tan(φ)* equal to φ. In order to calculate the value of $2R \times \sqrt{\frac{C}{L}}$, the values of R and C should be known. We have f_o=43.87GHz and L=1nH, therefore per $\omega_o = 1/\sqrt{LC_L}$, it would result to C=13.16fF. Considering $R_p = Q_L L \omega_o$, where L=1nH and Q_L=5.5, then R_p =1.51k. Knowing the values of R, C, and L we can calculate the value of the coefficient in equation (4-9):

$$2R \times \sqrt{\frac{C}{L}} \approx 11$$

But the load capacitor has also quality factor, Q_c. It is necessary to know the overall quality factor, Q_t to calculate a more accurate value for $R_p = Q_t L \omega_o$. The overall Q_t is:

$$\frac{1}{Q_t} = \frac{1}{Q_L} + \frac{1}{Q_c}$$

A practical way to calculate the overall Q_t is running an *ac* analysis simulation, looking at the output impedance, measuring the -3dB band-width and calculating the overall quality factor using $Q_t = \omega_o / \Delta\omega_{3dB}$ where $\Delta\omega_{3dB}$ is the -3dB band-width and ω_o is the self-oscillation frequency for LC-tank. The ac analysis simulation result is shown in Figure 4-5.

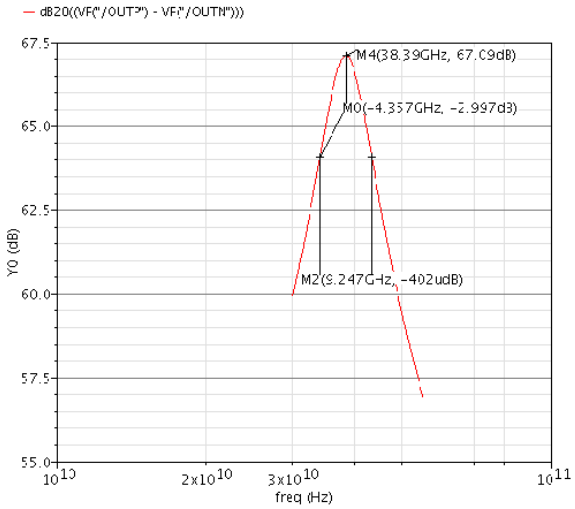

Figure 4-5 Finding the quality factor.

From Figure 4-5, we can calculate the overall quality factor, Q_t =38.4/9.25=4.15. Knowing L=1nH, Q_t =4.15, and f_o= 43.87GHz, R_p= Q_t $L\omega_o$ is equal to 1.144k. Therefore the value of the coefficient in equation (4-9) would be:

$$2R\times\sqrt{\frac{C}{L}}\approx 8.3$$

Table 4-1 shows the value of φ in equation (4-9), and $tan\varphi$ for different values of locking frequencies, ω where $\omega=\omega_o+\Delta\omega$ is in the desired operation region given by the sensitivity curve shown in Figure 3-23.

Table 4-1 Comparison of φ and tanφ for LC-tank frequency divider.

Locking frequency, ω (GHz)	43.67	43.77	43.95	43.48 (min)	44.1 (max)
$\Delta\omega$ (GHz)	0.2	0.1	0.08	0.39	0.23
$\varphi=2R\times\sqrt{\frac{C}{L}}\times\frac{\Delta\omega}{\omega_o}$ (rad)	0.038	0.019	0.015	0.074	0.044
$tan\varphi$	0.038	0.019	0.015	0.074	0.044

Table 4-1 verifies that we can assume φ and $tan\varphi$ are equal, therefore we can combine equations (4-1) and (4-9), and it would result:

$$-2RC\Delta\omega = \frac{i_{inj}}{i_d}.\frac{\sin\theta}{1+\frac{i_{inj}}{i_d}\cos\theta} \tag{4-10}$$

Now, the following variable substitutions can be made:

- $\Delta\omega_o = \omega - \omega_o = (\omega - \omega_{inj}) - (\omega_o - \omega_{inj})$ where ω_{inj} is the injection frequency.
- $\Delta\omega_o = (\omega_o - \omega_{inj})$

Note that $(\omega - \omega_{inj})$ is the difference between the injection frequency and the oscillator output instantaneous frequency, which based on Figure 4-2(c) is the same as the derivative of θ with respect to time. Applying these substitutions in equation (4-10), we have:

$$-2RC[\frac{d\theta}{dt} - \Delta\omega_o] = \frac{i_{inj}}{i_d}.\frac{\sin\theta}{1+\frac{i_{inj}}{i_d}\cos\theta} \tag{4-11}$$

W can rewrite equation (4-11) and get to the following differential equation:

$$\frac{d\theta}{dt} = -\frac{1}{2RC}.\frac{i_{inj}}{i_d}.\frac{\sin\theta}{1+\frac{i_{inj}}{i_d}\cos\theta} + \Delta\omega_o \tag{4-12}$$

If we first consider the case where the injected frequency is the same as the self-oscillation frequency (i.e., where $\Delta\omega_o = 0$), then Figure 4-4 shows two equilibrium points: a stable equilibrium at $\theta = 0$ and an unstable equilibrium at $\theta = \pm\pi$. For the case where $\Delta\omega_o \neq 0$, Figure 4-4 curve would be shifted up or down by that amount.

4.1.1 Validating Calculation of φ by Simulation Results for LC-tank Divider

Now, we need to verify the calculated values of φ by the simulation result. Figure 4-6 shows the locking frequency and the locking phase when an ac current with half-rate frequency and 20uA amplitude is injected to the drain, i_{inj}.

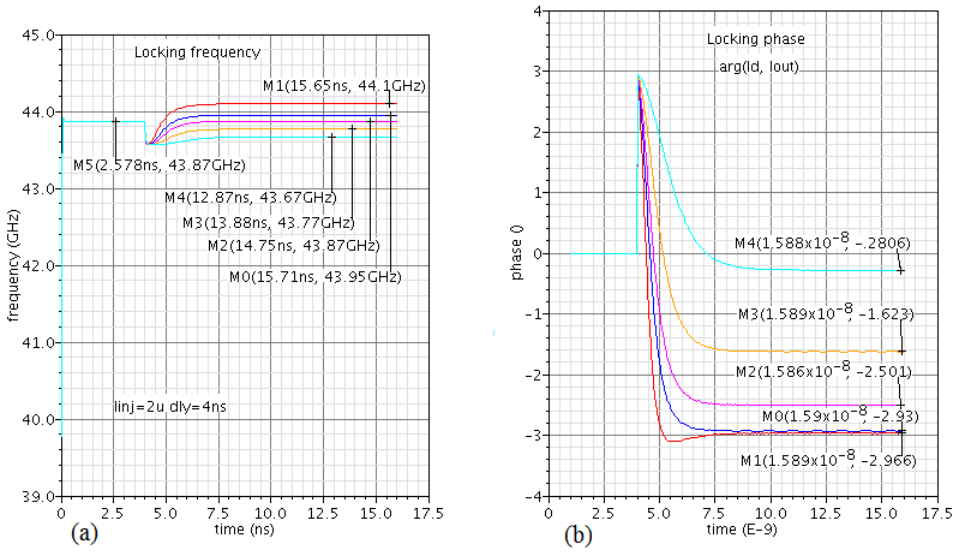

Figure 4-6 Simulation results for LC-tank based frequency divider.

Figure 4-6(a) shows the simulations results for the LC-tank frequency divider which is free running at the frequency of 43.87GHz until 4ns. A 20uA current with starting time of 4ns with frequencies of 43.67-, 43.77-, 43.87-, 43.95-, and 44.1-GHz is injected to the divider. The LC-tank divider locks at the injected frequency after a few cycles. Figure 4-6(b) shows the locking phase, φ between the drain current of the transistor M_1, i_d and the current that goes to the total load, i_o corresponding to the injected frequencies. Table 4-2 compares the φ value from calculation and simulation.

Table 4-2 Comparison of calculation and simulation values of φ for LC-tank divider.

Locking frequency, ω (GHz)	43.67	43.77	43.87 (ω_o)	43.95	44.1 (max)
$\varphi = -2R.\sqrt{\frac{C}{L}}.\frac{\Delta\omega}{\omega_o}$	-2.168°	-1.084°	0	0.867°	2.493°
φ from simulation	0.281°	1.622°	2.501°	2.931°	2.966°
φ from simulation-2.501°	-2.220°	-0.879°	0	0.430°	0.465

The value of φ from simulation, the third row in Table 4-2, is not equal to zero at self-oscillation similar to the calculated value in the second row. Although the expression in (4-9) is independent of the injection amplitude, the simulation does show some dependency on it. This difference seems to be the reason that φ from simulation is not zero at ω_o. In order to better comparison of the calculated and simulated values, the simulation values are subtracted from the self-oscillation value (2.501^o). These latter values are shown in the last row of Table 4-2.

Comparing the values in the second and the last rows of Table 4-2 implies when the absolute value of $\Delta\omega$ increases, the absolute value of φ also increases in both calculation and simulation. But the values are different.

For a better comparison, more simulations were done for ω_{inj} values that are in the desired operation region and also very close to ω_o. The simulation results are shown in Figure 4-7. For these simulations, similar to the previous case, the LC-tank frequency divider is in the self-oscillation mode until 4ns with the free running frequency of 43.87GHz and a 20uA current is injected starting at 4ns. The frequency values of injected signal are 43.85-, 43.86-, 43.87-, 43.88-, and 43.89-GHz. Figure 4-7 shows the locking frequency and phase, corresponding to these frequencies. Table 4-3 summarizes the value of φ from calculation and simulation.

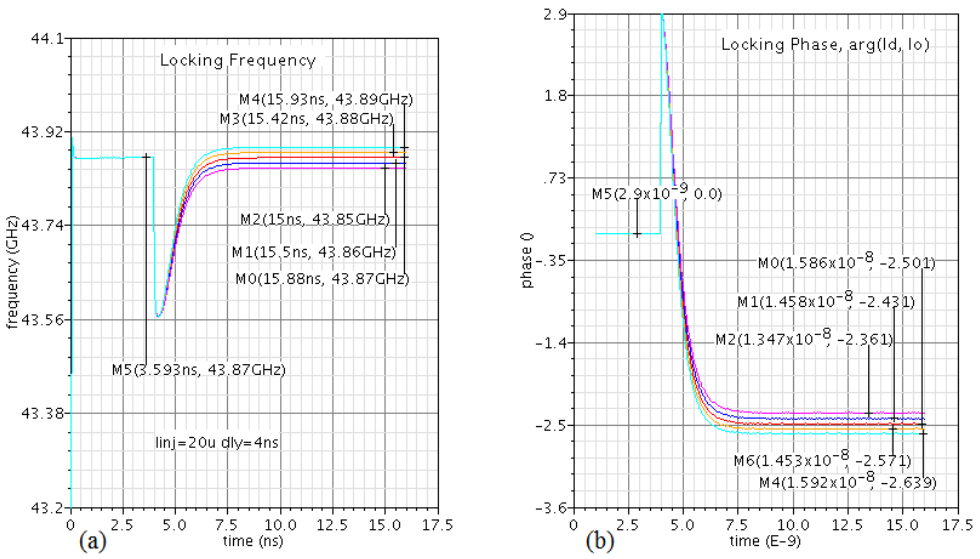

Figure 4-7 Simulation results showing the locking frequency and phase for LC-tank divider.

Table 4-3 Comparison of calculation and simulation values of φ for frequencies closer to ω_o.

Locking frequency, ω (GHz)	43.85	43.86	43.87 (ω_o)	43.88	43.89
$\varphi = -2R.\sqrt{\frac{C}{L}}.\frac{\Delta\omega}{\omega_o}$	-0.217°	-0.108°	0	0.108°	0.217°
φ from simulation	2.361°	2.431°	2.501°	2.571°	2.639°
φ from simulation-2.501°	-0.140°	-0.070°	0	0.070°	0.138°

Comparing the values in the second and last rows of Table 4-3 shows when the absolute value of $\Delta\omega$ increases, the absolute value of φ also increases in both calculation and simulation. It also shows when $\Delta\omega$ doubles, the value of φ from both simulation and calculation almost doubles similar to calculation results, although there is a difference between the calculated and simulation values. The difference between the values can be related to the inherent difference between simulation and calculation. In calculation, equation (4-9), φ depends on the injection frequency while in simulation, it is a function of both the frequency and amplitude of injection signal.

Table 4-4 shows the value of φ from simulation results is a function of both the frequency and amplitude of injection signal.

Table 4-4 Simulation results for different frequency and amplitude values of injected signal.

		i_{inj}				
		20uA	15uA	10uA	5uA	0uA
ω	43.67GHz	φ=0.28 ^{o}				
	43.72GHz	φ=1.02 ^{o}	φ=0.18 ^{o}			
	43.77GHz	φ=1.62 ^{o}	φ=0.88^o	φ=0.06 ^{o}		
	43.82GHz	φ=2.11 ^{o}	φ=1.42 ^{o}	φ=0.73 ^{o}	φ=0.2 ^{o}	
	43.87GHz (ω_0)	φ=2.51 ^{o}	φ=1.82 ^{o}	φ=1.18 ^{o}	φ=0.53 ^{o}	φ=0
	43.92GHz	φ=2.8 ^{o}	φ=2.11 ^{o}	φ=1.46 ^{o}	φ=0.77 ^{o}	
	43.97GHz	φ=2.99 ^{o}	φ=2.28 ^{o}	φ=1.54 ^{o}		
	44.02GHz	φ=3.03 ^{o}	φ=2.3 ^{o}			
	44.07GHz	φ=3.06 ^{o}				

Analyzing the values in Table 4-4, points out the difference between calculation and simulation results. Despite the independence of the calculation values to the injection amplitude, the simulation results for the same $\Delta\omega$ with different injection amplitudes are not the same. For instance, the value of φ from simulation for ω=43.77GHz are -1.62^o, -0.88^o and -0.06^o when injection amplitudes of 20uA, 15uA and 10uA respectively while the calculation value for the same frequencies from Table 4-2 is -1.084 ^{o} without any dependencies to injection amplitude.

4.2 CML Ring Frequency Divider

Similar to LC-tank frequency divider, for simplicity of the analysis a differential current at half-rate frequency is injected to the output nodes as shown in Figure 4-8, instead of injecting the signal via the clock voltage inputs at full-rate frequency.

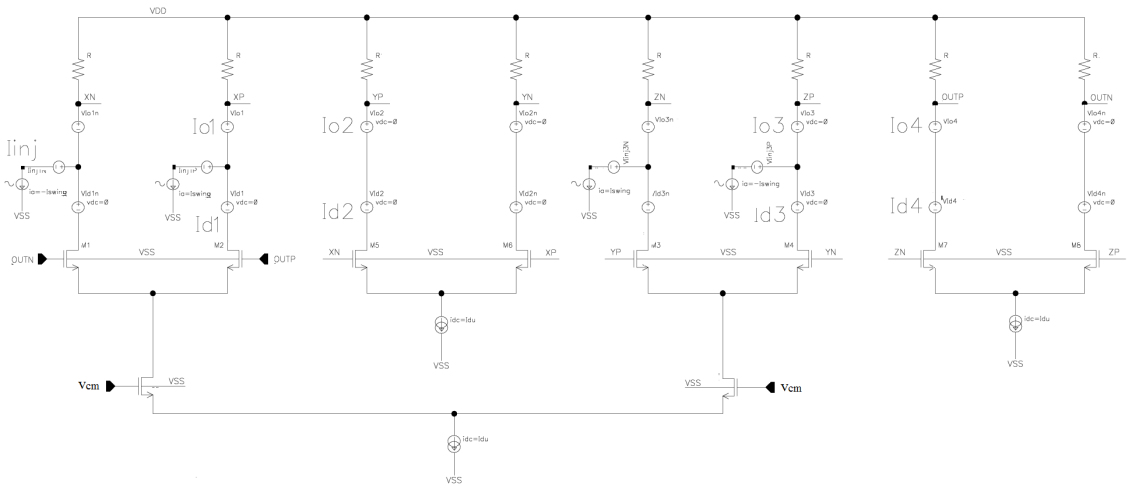

Figure 4-8 Schematic of the ring frequency divider with current injected to output nodes.

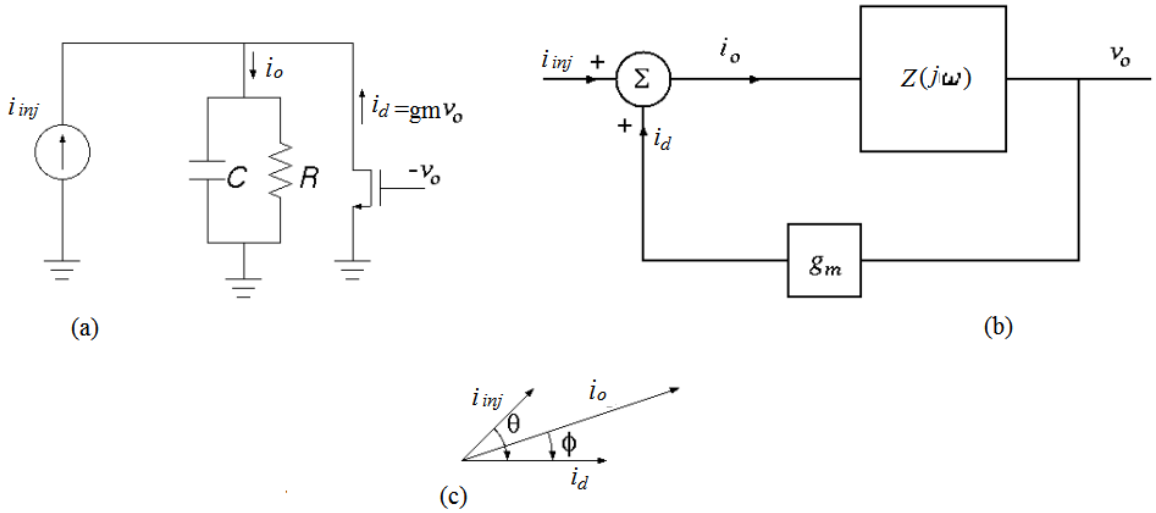

Figure 4-9 (a) Equivalent circuit, (b) Block diagram and (c) Vector representation for ring divider.

The circuit shown in Figure 4-8 can be modeled as shown in Figure 4-9. An equivalent circuit corresponding to the first stage of an *n*-stage ring (driven by the output V_o of the last stage) is shown in Figure 4-9(a) where i_{inj} is the injected current, i_d is the feedback current which is the drain buffer current of the first stage, and their sum is, $i_o = i_d + i_{inj}$ which goes to the total load of the first stage. The block diagram form is shown in Figure 4-9(b). A vector representation of the three currents is shown in Figure 4-9(c) where the locking phase φ is the angle between the feedback current, i_d and the sum current, i_o, and phase θ is the angle between the feedback

current, i_d and the injection current, i_{inj} that is injected to the drain buffer of the first stage. Figure 4-10 is an example of a simulation result showing the vector representation of the three currents similar to Figure 4-9(c).

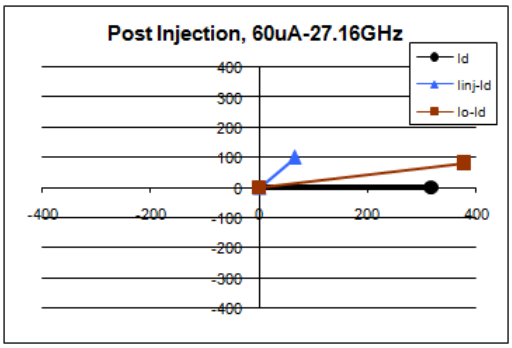

Figure 4-10 Vector representation of the three currents in ring frequency divider.

To find the phase shift, the output impedance should be formulated first. The output impedance, $Z(j\omega)$ of the first stage can be written by the following equation:

$$Z(j\omega) = \frac{R}{1 + j\omega RC} \tag{4-13}$$

and based on the block diagram shown in Figure 4-9(b) the output impedance of n stages is:

$$Z(j\omega) = \frac{g_m^{n-1} R^n}{(1 + j\omega RC)^n} \tag{4-14}$$

where R and C are respectively the output resistance and capacitance of each stage. The resulting phase shift due to each buffer impedance is given by:

$$\arg[Z(j\omega)] = -\tan^{-1}(\omega RC) \tag{4-15}$$

If the divider has n stages, then the phase shift of each stage is π/n. Thus, assuming n is even, the overall phase shift around the loop can be written as:

$$\varphi = \pi + n\arg[Z(j\omega)] = \pi - n\tan^{-1}(\omega RC)$$

$$\varphi = f(\omega) = \pi - n\tan^{-1}(\omega RC) \tag{4-16}$$

where the π term corresponds to the inverting connection between the output of the last stage and input of the first stage. Without injection, the divider will self-oscillate at frequency ω_o, and the phase shift around the loop is equal to 2π. When a signal with a frequency of ω is injected in to the loop where $\omega=\omega_o+\Delta\omega$ *is in the desired operation region of its sensitivity curve,* then phase shift φ will be created, and the phase shift around the loop is also equal to 2π as shown in Figure 4-11.

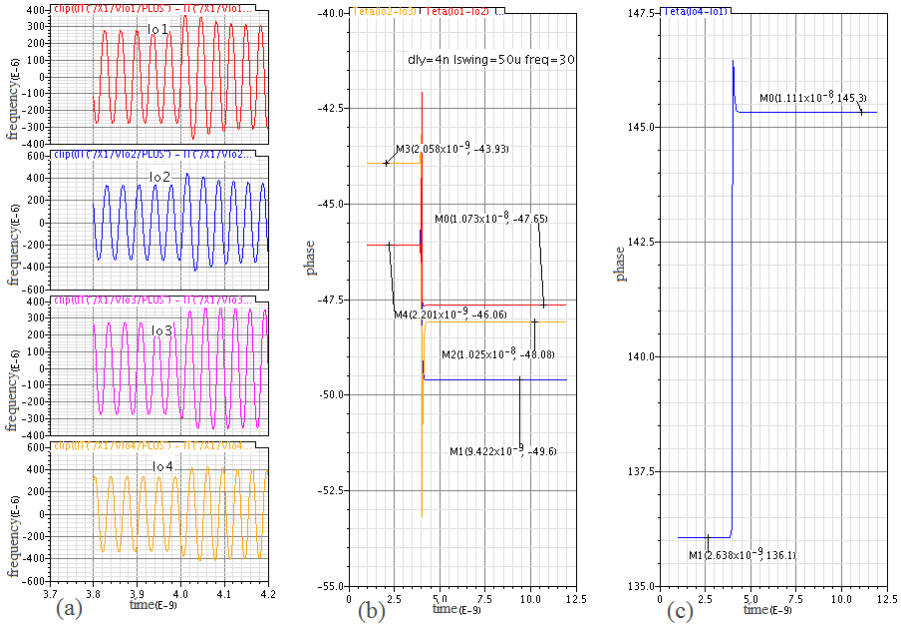

Figure 4-11 Amplitude and phase of current signals of different stages.

Figure 4-11(a) shows the output currents of each stage. Where the ring frequency divider oscillates at its free running frequency until 4ns when the injection signal is applied to the loop and as a result the frequency and amplitude of the output currents change until locked.

Figure 4-11(b) shows the phase between each stage before and after injection when divider locks. It can be seen in this figure that the phase between the first and second stages, $\theta(I_{o1},I_{o2})$ is equal to -46.06^o before injection and is equal to -47.65^o after injection. The phase between the second and third stages, $\theta(I_{o2},I_{o3})$ is equal to -43.93^o before injection and is equal to -48.08^o after

injection. The phase between the third and fourth stages, $\theta(I_{o3},I_{o4})$ is equal to -46.06° before injection and is equal to -49.06° after injection. Figure 4-11(c) shows the phase between the fourth and first stages, $\theta(I_{o4},I_{o1})$ is equal to 136.1° before injection and is equal to 145.3° after injection. The sum of all phases before injection is equal to -46.06° + -43.93° +-46.06° +136.1° = $0.05^{o} \cong 0$ and the sum of all phases after injection is also equal to -47.65°+ -48.08° + -49.6° +$145.3^{o} = 0.03^{o} \cong 0$. The sums are almost zero. This result verify that the phase shift around the loop after injection is also equal to 2π, although the phases between the individual stages have been changed due to the injection.

The phase shift $\varphi = f(\omega)$ is a function of ω. The Taylor expansion of $f(\omega)$ around ω_o is:

$$\varphi = f(\omega) = f(\omega_o) + f'(\omega_o)(\omega - \omega_o) + f''(\omega_o)(\omega - \omega_o)^2 + ... \tag{4-17}$$

knowing that

$$f(\omega_o) = \pi - n\tan^{-1}(\omega_o RC)$$

which is the phase shift at the self-oscillation frequency and is equal to zero.

We have $\frac{d}{dx}\tan^{-1} u = \frac{1}{1+u^2}\frac{du}{dx}$ and assuming $u = \omega_o RC$, then the first and second-order polynomials of the Taylor expansion would be:

$$f'(\omega_o)(\omega - \omega_o) = -\frac{nRC}{1+(\omega_o RC)^2}(\omega - \omega_o) \tag{4-18}$$

and

$$f''(\omega_o)(\omega - \omega_o)^2 = -\frac{2n\omega_o (RC)^3}{[1+(\omega_o RC)^2]^2}(\omega - \omega_o)^2 \tag{4-19}$$

We know that the phase shift around the loop at self-oscillation frequency for n-stage ring oscillator is $\pi = n \times tan^{-1}(\omega_o RC)$, therefore for the 4-stage CML ring oscillator, we have:

$$\frac{\pi}{4} = \tan^{-1}(\omega_o RC) \Rightarrow RC = \frac{1}{\omega_o}$$

where RC in expressions (5) and (6) is replaced by $RC=1/\omega_o$, we have:

$$f'(\omega_o)(\omega-\omega_o) = -\frac{nRC}{1+(\omega_o RC)^2}(\omega-\omega_o) = \frac{n}{2}.\frac{\Delta\omega}{\omega_o} \tag{4-20}$$

$$f''(\omega_o)(\omega-\omega_o)^2 = -\frac{2n\omega_o(RC)^3}{[1+(\omega_o RC)^2]^2}(\omega-\omega_o)^2 = \frac{n}{2}.(\frac{\Delta\omega}{\omega_o})^2 \tag{4-21}$$

Now, we need to investigate if the second-order polynomial in (4-21) can be ignored. Table 4-5 shows the calculated values for the first- and second-order polynomials of the Taylor expansion, namely expressions (4-20) and (4-21), considering $n=4$ and $\omega=\omega_o+\Delta\omega$ is in the desired operation region given by its sensitivity curve shown in Figure 3-15.

Table 4-5 First and second-order Taylor expansion polynomials of ring divider.

ω_o =27.16GHz, n=4 Locking frequency, ω (GHz)	$\Delta\omega$ (GHz)	$\frac{n}{2}\frac{\Delta\omega}{\omega_o}$		$\frac{n}{2}(\frac{\Delta\omega}{\omega_o})^2$	
28.16	1.00	0.074rad	4.22°	0.0027rad	0.155°
29.16	2.00	0.148rad	8.44°	0.012rad	0.62°
30.00	2.84	0.21rad	11.98°	0.022rad	1.25°
24.00	3.16	0.23rad	13.3°	0.027rad	1.55°
31.50 (max)	4.34	0.32rad	18.31°	0.051rad	2.93°
21.00 (min)	6.16	0.45rad	25.99°	0.103rad	5.89°

Looking at values in Table 4-5, the second-order polynomial values are much smaller than the first-order polynomial values. The value of $\Delta\omega/\omega_o$ ($(\Delta\omega/\omega_o)^2$) is less than 0.11 (0.01) for frequencies close to self-oscillation frequency and less than 0.22 (0.05) in the worst case for frequencies on the edge of locking range, therefore (4-17) can be approximated by its first-order Taylor expansion polynomial.

$$\varphi = f(\omega) = f(\omega_o) + f'(\omega_o)(\omega - \omega_o) + \ldots$$

$$f(\omega) = \pi - n\tan^{-1}(\omega_o RC) + \frac{-nRC}{1+(\omega_o RC)^2}(\omega - \omega_o) \tag{4-22}$$

Therefore, the phase difference due to the injected signal is:

$$\varphi \approx -\frac{nRC}{1+(\omega_o RC)^2}\Delta\omega \tag{4-23}$$

Using an argument similar to LC-tank , from Figure 4-9(c) we can write:

$$\tan\varphi = \frac{i_{inj}\sin\theta}{i_d + i_{inj}\cos\theta} = \frac{i_{inj}}{i_d}.\frac{\sin\theta}{1+\frac{i_{inj}}{i_d}\cos\theta} \tag{4-24}$$

Similar to LC- tank, we need to investigate the correctness of assuming φ is equal to $tan\varphi$.

Table 4-6 shows the value for the first-order polynomials of expression (4-20), φ and $tan\varphi$ for locking frequencies.

Table 4-6 Comparison of the values of first-order polynomial, φ and $tan\varphi$.

Locking frequency, ω (GHz)	28.16	29.16	30	24	31.5 (max)	21 (min)
$\Delta\omega$ (GHz)	1	2	2.84	3.16	4.34	6.16
$\varphi = 2.\frac{\Delta\omega}{\omega_o}$ (rad)	0.074	0.148	0.21	0.23	0.32	0.45
$tan\varphi$	0.074	0.148	0.21	0.23	0.33	0.48
Error	0%	0%	0%	0%	3.125%	6.67%

Table 4-6 shows that we can assume φ and $tan\varphi$ are equal for frequencies close to the self-oscillation frequency and within 6.7% in the worst case, for frequencies close to the edge of locking range. Though, we should be careful to generalize this assumption. In this case, equations (10) and (11) could be combined, therefore we have:

$$-\frac{nRC}{1+(\omega_o RC)^2}\left(\frac{d\theta}{dt}-\Delta\omega_o\right)=\frac{i_{inj}}{i_d}\cdot\frac{\sin\theta}{1+\frac{i_{inj}}{i_d}\cos\theta} \tag{4-25}$$

Consequently, the differential equation is:

$$\frac{d\theta}{dt}=-\frac{1+(\omega_o RC)^2}{nRC}\cdot\frac{i_{inj}}{i_d}\cdot\frac{\sin\theta}{1+\frac{i_{inj}}{i_d}\cos\theta}+\Delta\omega_o \tag{4-26}$$

for *n* stages. If we consider the case with m points that signals at full-rate frequency are injected to the divider, then the expression in (4-26) should be modified to:

$$\frac{d\theta}{dt}=-\frac{1+(\omega_o RC)^2}{RC}\cdot\frac{mi_{inj}}{ni_d}\cdot\frac{\sin\theta}{1+\frac{i_{inj}}{i_d}\cos\theta}+\Delta\omega_o \tag{4-27}$$

Equation (4-27) implies: 1) The derivative of θ with respect to time, $d\theta/dt$, depends not only on the injection ratio I_{inj}/I_d, but also to the product of the self-oscillation frequency and the *RC* time constant. Normally this product is constant for a given value of *n*. For the divider shown in Figure 4-8**,** it is normal to apply two points of injection, *m=2* by applying a differential signal. 2) When $d\theta/dt$ is equal to zero, the divider is locked.

4.2.1 Validating Calculation of φ by Simulation Results for Ring Divider

Now, we need to verify the calculated values of φ by the simulation result. Figure 4-12 shows the locking frequency and the locking phase when a 50uA current, I_{inj} with half-rate frequency is injected to the drain buffer of the first and the third stages, as shown in Figure 4-8. ω is in the desired operation region of frequency divider's sensitivity curve.

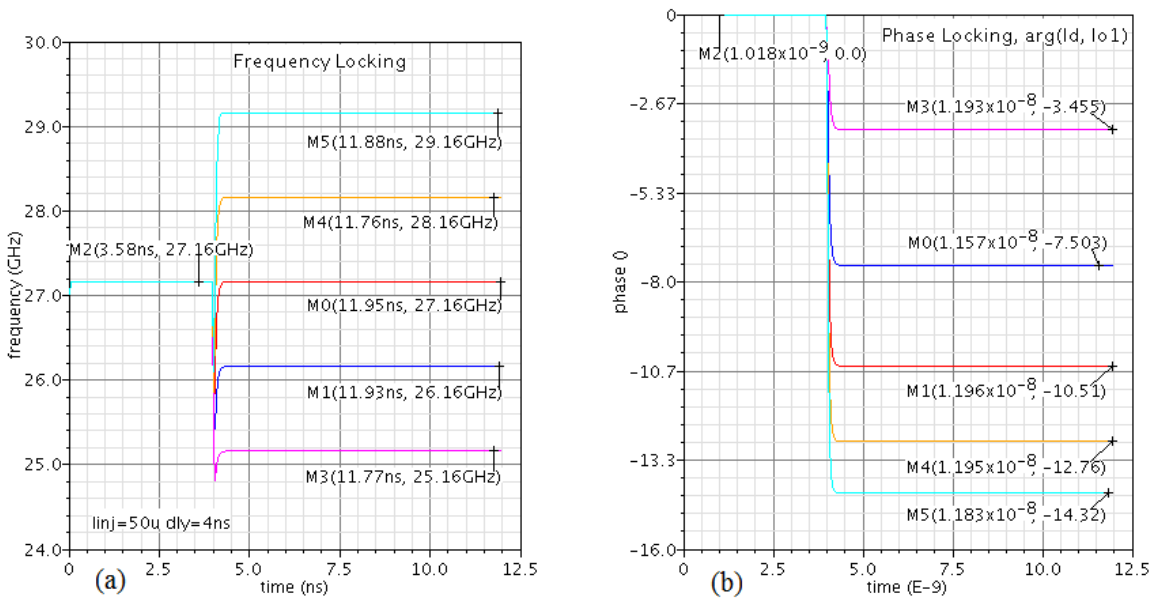

Figure 4-12 Simulation results showing locking frequency and phase for ring divider.

Table 4-7 Comparison of calculation and simulation values of φ for ring divider.

Locking frequency, ω(GHz) , I_{inj}=50uA	25.16	26.16	27.16 (ω_o)	28.16	29.16
$\varphi = 2 \times \frac{\Delta\omega}{\omega_o}$	-8.44 °	-4.22 °	0	4.22 °	8.44 °
φ from simulation	3.455 °	7.503 °	10.51°	12.76 °	14.32 °
φ from simulation-10.51°	-7.055 °	-3.007 °	0	2.21 °	3.71 °

Figure 4-12(a) shows the simulations results for ring frequency divider which is in free running at frequency of 27.16GHz until 4ns and a 50uA current with frequencies of 25.16-, 26.16-, 27.16-, 28.16-, and 29.16-GHz is injected with a starting time of 4ns. The ring frequency divider locks at the injected frequency after few cycles. Figure 4-12(b) shows the locking phase, φ between the drain buffer current, i_{d1} and the current which goes to the total load, i_{o1} for the first stage corresponding to the injection frequencies. The phase values shown in Figure 4-12(b) have units of degree.

Table 4-7 shows the locking phase, φ corresponding to locking frequencies from the calculation and simulation. The simulation value of φ, the third row in Table 4-7, is not equal to zero at self-oscillation similar to the calculated value in the second row. One of the reasons could be because the simulation value of φ is a function of both the frequency and amplitude of injection signal. Similar to the LC-based divider, for better comparison of the calculated and simulated values, the simulation values are subtracted from the self-oscillation value (10.51^{o}). These latter values are shown in the last row of Table 4-7.

Comparing the values in the second and the last rows of Table 4-7 implies that: 1) when the absolute value of $\Delta\omega$ increases, the absolute value of φ also increases in both calculation and simulation, and 2) when the $\Delta\omega$ value multiplies by two, the value of φ almost multiplies by two. It seems that the simulation results confirm a similar trend as calculation, although the values are different.

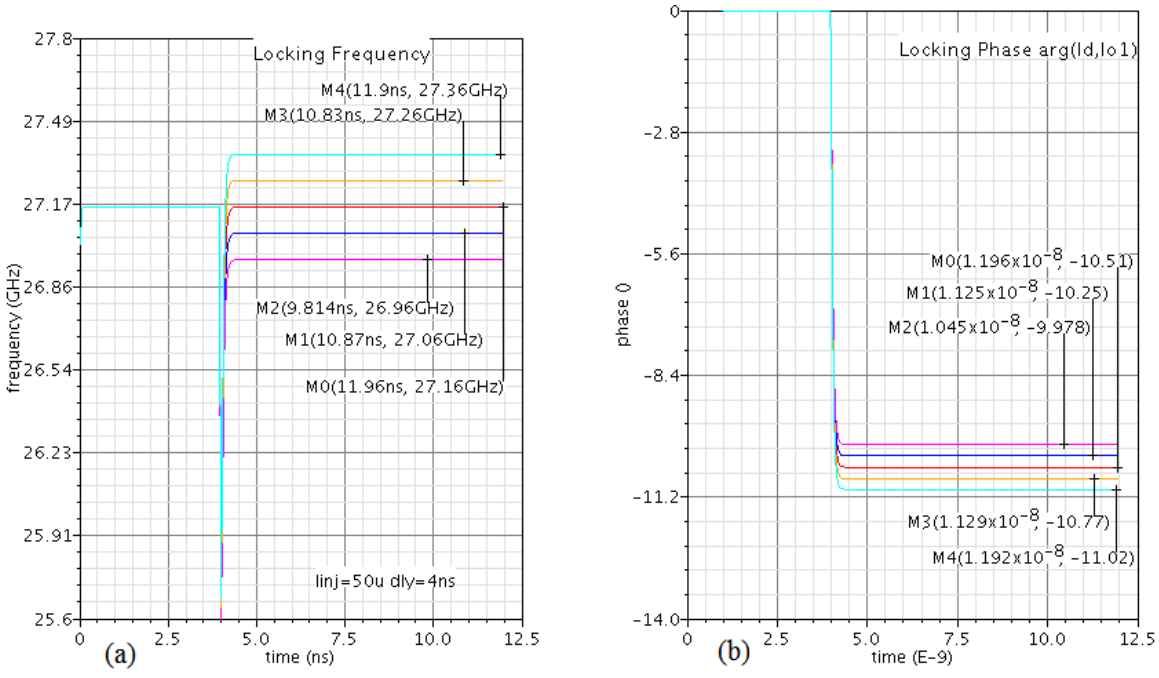

Figure 4-13 Simulation results of injection frequencies very close to ω_o.

More simulations were done for ω_{inj} values closer to ω_o .The injection frequencies are in the desired operation region of the divider's sensitivity curve. The simulation results are shown in Figure 4-13. Similar to previous tests, Figure 4-13(a) shows the simulation results of ring frequency divider which is free running at 27.16GHz until 4ns and a 50uA current is injected at a starting time of 4ns. The values of injection frequency are 26.96-, 27.06-, 27.16-, 27.26-, and 27.36-GHz. Figure 4-13(b) shows the locking phase, φ corresponding to these frequencies.

Table 4-8 Comparison of calculation and simulation values of φ for ring divider.

Locking frequency, ω(GHz)	26.96	27.06	27.16 (ω_o)	27.26	27.36
$\varphi = 2.\frac{\Delta\omega}{\omega_o}$	-0.84 ^{o}	-0.42 ^{o}	0	0.42 ^{o}	0.84 ^{o}
φ from simulation	9.98 ^{o}	10.25 ^{o}	10.51 ^{o}	10.77 ^{o}	11.02 ^{o}
φ from simulation-10.51^o	-0.53 ^{o}	-0.26 ^{o}	0	0.26 ^{o}	0.51 ^{o}

Table 4-8 summarizes the φ value from calculation and simulation of the latter tests. Comparing the values in the second and the last rows of Table 4-8 shows when the absolute value of $\Delta\omega$ increases, the absolute value of φ also increases in both calculation and simulation. It also shows when $\Delta\omega$ doubles, the value of φ from both simulation and calculation doubles although there is a difference between the calculated and simulation values. The difference between the values is related to the inherent difference between simulation and calculation. In calculation, φ depends on the injection frequency while in simulation, it is a function of both the frequency and amplitude of injection signal.

Ignoring the differences between the calculated and simulation values , the simulation results confirm the calculation results for injection frequencies very close to ω_o.

4.3 CML D Flip-Flop Frequency Divider

Similar to LC-tank frequency divider, for simplicity of the analysis a differential current with half-rate frequency is injected to the output nodes as shown in Figure 4-14, instead of injecting the signal via the clock voltage inputs at full-rate frequency.

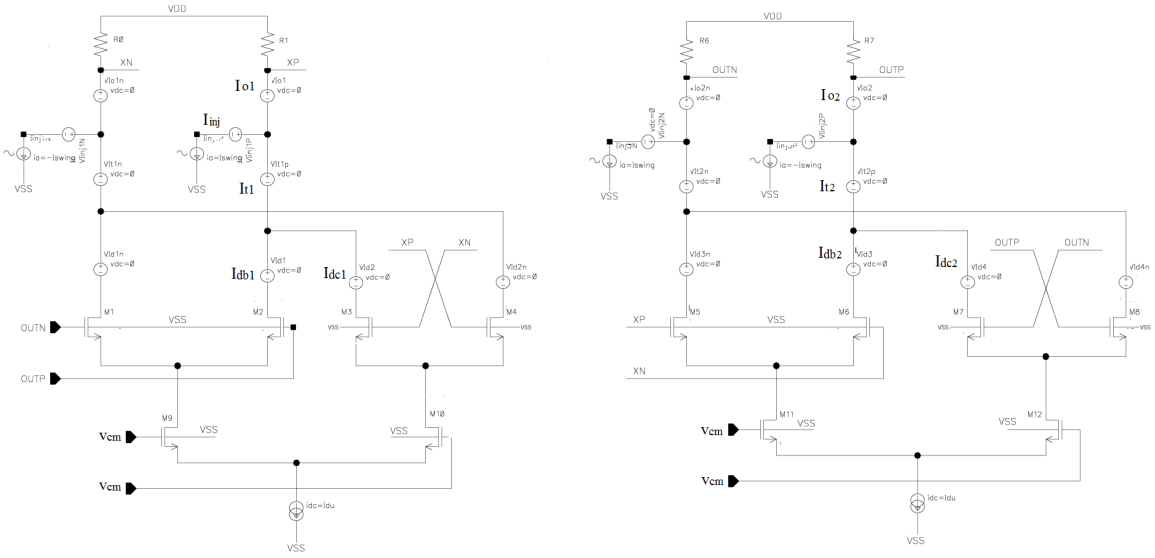

Figure 4-14 Schematic of the DFF frequency divider with current injected to output nodes.

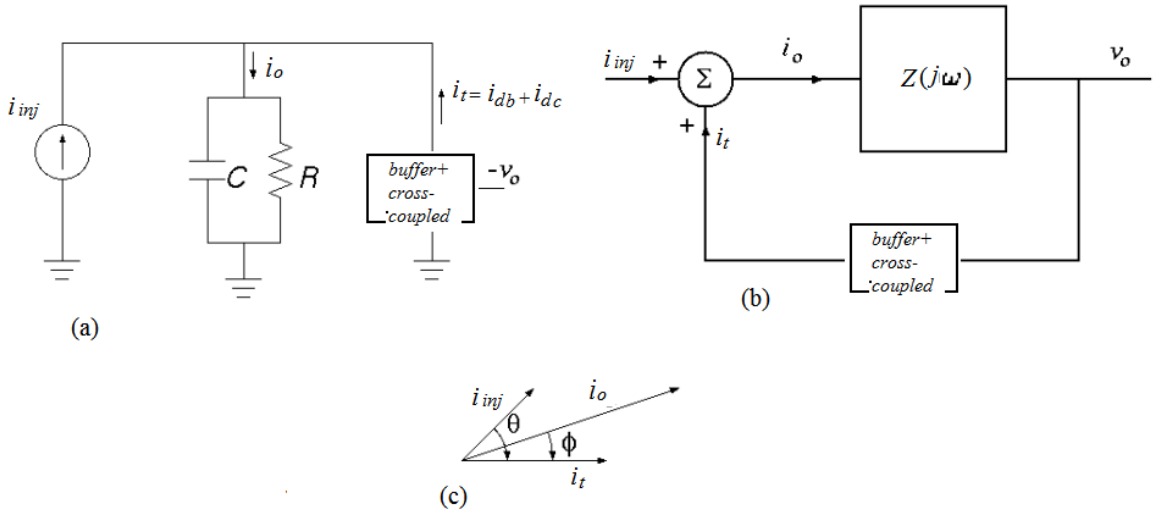

Figure 4-15 (a) Equivalent circuit, (b) Block diagram and (c) Vector representation for the DFF divider.

The circuit shown in Figure 4-14 can be modeled as shown in Figure 4-15. An equivalent circuit corresponding to the first latch of the DFF frequency divider (driven by the output V_o of the second latch) is shown in Figure 4-15(a); The block diagram is shown in Figure 4-15(b); And a vector representation of the three currents is shown in Figure 4-15(c), where i_t is the sum of the buffer current, i_{db} that is the feedback current and the cross coupled current, i_{dc}; Locking phase, φ is the angle between the sum current, i_t and the current goes to the total load, i_o for the first latch; The phase angle θ, is the angle between the sum current, i_t and the injection current i_{inj} that is injected to the sum of the drain buffer current and drain cross coupled current. Using the procedure to measure phases described in Section 3.1.1, Figure 4-16 is an example of a simulation result showing the vector representation of the three currents in Figure 4-15(c).

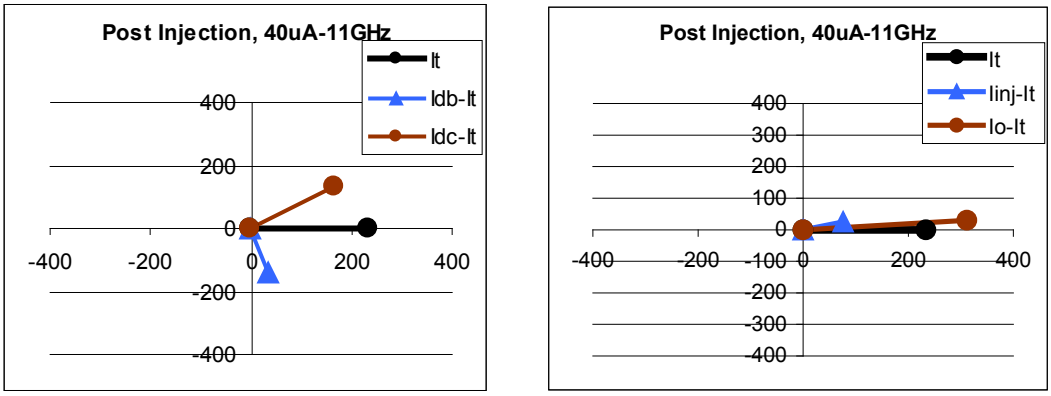

Figure 4-16 Vector representation of the three currents in DFF frequency divider.

From vector representation shown in Figure 4-15(c), we can write i_o as real and imaginary terms by the following equation:

$$i_o = i_t + i_{inj}\cos\theta + j i_{inj}\sin\theta$$

$$\tan\varphi = \frac{i_{inj}\sin\theta}{i_t + i_{inj}\cos\theta} = \frac{i_{inj}}{i_t}\cdot\frac{\sin\theta}{1+\frac{i_{inj}}{i_t}\cos\theta} \qquad (4\text{-}28)$$

To find phase shift, the output impedance should be found first. The output impedance, $Z(j\omega)$ for the first latch can be written as the following equation:

$$Z(j\omega) = -\frac{R}{gm_c R - 1} \cdot \frac{1}{1 - j\omega \frac{CR}{gm_c R - 1}} \tag{4-29}$$

where R, C, and gm_c are the output resistance, capacitance, and the trans-conductance of the cross coupled transistors pair, respectively of each latch. Assuming:

$$R_{eq} = R \,||\, \frac{-1}{gm_c} = -\frac{R}{gm_c R - 1} \tag{4-30}$$

and then combining equations (4-29) and (4-30), consequently results:

$$Z(j\omega) = \frac{R_{eq}}{1 + j\omega R_{eq} C} \tag{4-31}$$

The phase shift due to impedance is given by:

$$\arg[Z(j\omega)] = -\tan^{-1}(\omega R_{eq} C) \tag{4-32}$$

The DFF output impedance is:

$$Z(j\omega)_{DFF} = \frac{R^2_{eq}}{(1 + j\omega R_{eq} C)^2} \tag{4-33}$$

Because the DFF divider has *2* Latches, the phase shift of each latch is $\pi/2$. Thus, the overall phase shift around the loop can be written as:

$$\varphi = \pi + 2\arg[Z(j\omega)] = \pi - 2\tan^{-1}(\omega R_{eq} C)$$

$$\varphi = f(\omega) = \pi - 2\tan^{-1}(\omega R_{eq} C) \tag{4-34}$$

where the π term corresponds to the inversion realized by the inverting connection between the output of the second latch and input of the first latch. Without injection, the divider will self-oscillate at frequency ω_0, and the phase shift around the loop will be 2π. When a signal with the

frequency ω is injected in to the loop, assuming the frequency, $\omega=\omega_o+\Delta\omega$ *is in the desired operation region of its sensitivity curve,* then the phase shift φ will be created, although the phase shift around the loop will be 2π again.

The phase shift $\varphi=f(\omega)$ is a function of ω and the Taylor expansion for $f(\omega)$ around ω_o would be:

$$\varphi = f(\omega) = f(\omega_o) + f'(\omega_o)(\omega-\omega_o) + f''(\omega_o)(\omega-\omega_o)^2 + ... \tag{4-35}$$

knowing that

$$f(\omega_o) = \pi - 2\tan^{-1}(\omega_o R_{eq} C) \tag{4-36}$$

is the phase shift at the self-oscillation frequency.

We have $\frac{d}{dx}\tan^{-1} u = \frac{1}{1+u^2}\frac{du}{dx}$ and assume that $u = \omega_o R_{eq} C$, then :

$$f'(\omega_o)(\omega-\omega_o) = -\frac{2R_{eq}C}{1+(\omega_o R_{eq} C)^2}(\omega-\omega_o) \tag{4-37}$$

$$f''(\omega_o)(\omega-\omega_o)^2 = -\frac{4\omega_o (R_{eq}C)^3}{[1+(\omega_o R_{eq} C)^2]^2}(\omega-\omega_o)^2 \tag{4-38}$$

Now the question is whether or not the second-order polynomial given in (4-38) can be ignored when compared to the first-order polynomial given in (4-37). To simplify the equations (4-37) and (4-38), the relationship between time constant, $R_{eq}C$ and self-oscillation frequency, ω_o can be found using $T_{osc} = 2n.t_p$ where t_p is a propagation delay of each latch and is equal to $t_p = 0.69\times R_{eq}C$.

$$\omega_o = \frac{1}{2.n.t_p} \Rightarrow R_{eq}C = \frac{1}{2\times 2\times 0.69\omega_o} \cong \frac{1}{2.8\omega_o}$$

By substituting $R_{eq}C$ in the first and the second-order polynomials of the Taylor expansion given in expressions (4-37) and (4-38), with $R_{eq}C = 1/(2.8\omega_o)$, we have:

$$f'(\omega_o)(\omega-\omega_o) \cong 0.7\times\frac{\Delta\omega}{\omega_o} \tag{4-39}$$

Table 4-9 shows the calculated values for the first and the second-order polynomials of the Taylor expansion given in (4-35), considering $\omega=\omega_o+\Delta\omega$ is in the desired operation region given by its sensitivity curve shown in Figure 3-6.

Table 4-9 First and second-order Taylor expansion polynomials of DFF divider.

ω_0 =15.18GHz Locking frequency, ω (GHz)	$\Delta\omega$ (GHz)	$f'(\omega_o)(\omega-\omega_o)$ $=0.7\times\frac{\Delta\omega}{\omega_o}$		$f''(\omega_o)(\omega-\omega_o)^2$ $=0.15\times(\frac{\Delta\omega}{\omega_o})^2$	
16.18	1.00	0.046rad	2.64 º	6.51^{-04}rad	0.037 º
17.18	2.00	0.092rad	5.28 º	2.61^{-03}rad	0.149 º
11.00	4.18	0.193rad	11.04 º	0.012rad	0.651 º
7.00	8.18	0.377rad	21.61 º	0.044rad	2.52 º
19.5 (max)	4.32	0.199rad	11.41 º	0.012rad	0.696 º
2G (min)	13.18	0.868rad	34.8 º	0.113rad	6.49 º

Looking at Table 4-9 values, the second-order polynomial values are within 6% of the first-order polynomial values for frequencies close to the self-oscillation frequency and less than 18% in the worst case, for frequencies close to the edge of locking range. Therefore, the Taylor expansion in (4-35) can be approximated by its first-order polynomial.

$$\varphi = f(\omega) = f(\omega_o) + f'(\omega_o)(\omega-\omega_o) + \ldots$$

$$f(\omega) = \pi - 2\tan^{-1}(\omega_o RC) + \frac{-2R_{eq}C}{1+(\omega_o R_{eq}C)^2}(\omega-\omega_o) \tag{4-40}$$

As a result, the phase difference due to the injected signal is:

$$\varphi \approx -\frac{2R_{eq}C}{1+(\omega_o R_{eq}C)^2}\Delta\omega \qquad (4\text{-}41)$$

Now, we need to investigate the correctness of assuming φ is equal to $tan\varphi$. Table 4-10 shows the value of φ in equation (4-41), and $tan\varphi$ for different values of injection frequencies, ω where $\omega=\omega_o+\Delta\omega$ is in the desired operation region given by the divider's sensitivity curve shown in Figure 3-6.

Table 4-10 Comparison of the values of first-order polynomial, φ and $tan\varphi$ for DFF divider.

Locking frequency, ω (GHz)	16.18	17.18	11.0	7.0	19.0	2.0
$\Delta\omega$ (GHz)	1G	2	4.18	8.18	4.32	13.18
$\varphi = 0.7\times\frac{\Delta\omega}{\omega_o}$ (rad)	0.046	0.092	0.193	0.377	0.199	0.868
$tan\varphi$ (rad)	0.046	0.092	0.195	0.395	0.202	1.18
Error	0%	0%	1.04%	4.77%	1.5%	35.9%

Table 4-10 shows that we can assume φ and $tan\varphi$ to be equal for the injection frequencies which are close to the self-oscillation frequency, the first few columns from left, but the difference widens up as $\Delta\omega$ increases. This is due to the fact that the desired operation region in sensitivity curve for DFF divider is very wide, and the approximation of $tan\varphi$ being equal to φ cannot be generalized for all injection frequencies in the desired operation region of sensitivity curve.

4.3.1 Validating Calculation of φ by Simulation Results for DFF Divider

The next step is to see whether or not the calculated value for φ is matching the simulation result. Table 4-11 summarizes the calculation and simulations results for DFF frequency divider which is in the self-oscillation frequency of 15.18GHz until 4ns, and a 40uA current with

frequencies of 7-, 11-, 13.18-, 14.18-, 15.18-, 16.18-, 17.18-, and 19-GHz is injected starting at 4ns. The DFF frequency divider locks at the injected frequency after a few cycles. The locking phase, φ is the phase between i_{t1} and the current that goes to the total load, i_{o1} corresponding to the injected frequencies for the first latch. The injected frequencies are in the desired frequency divider operation region.

Table 4-11 Comparison of calculation and simulation values of φ for DFF divider when I_{inj}=40uA.

Locking frequency, ω(GHz) I_{inj}=40uA	7.0	11.0	13.18	14.18	15.18 (ω_o)	16.18	17.18	19.0
$\varphi=0.7\times(\Delta\omega/\omega_o)$	-21.67°	-11.04°	-5.28°	-2.64°	0	2.64°	5.28°	11.41°
φ from simulation	-57.32°	-5.42°	7.11°	10.25°	12.77°	14.90°	16.75°	19.90°
φ from simulation -12.77°	-70.09°	-18.19°	-5.66°	-2.52°	0	2.13°	3.98°	5.13°

As mentioned earlier, the simulated values are dependent on the amplitude of the injected signal. This might be one of the reasons why the value of φ from simulation, the third row in Table 4-11, is not equal to zero at self-oscillation similar to the calculated value in the second row. In order to better comparison of the calculated and simulated values, the simulation value is subtracted from its self-oscillation value (12.77°). This latter value is shown in the last row of Table 4-11.

Comparing the values in the second and the last rows of Table 4-11 shows when the absolute value of $\Delta\omega$ increases, the absolute value of φ also increases in both calculation and simulation, in the other word shows the calculation follows the same trend as simulation result. The values in the table show when the absolute value of $\Delta\omega$>1GHz ($\Delta\omega/\omega_o\cong 0.07$), the difference between simulated and calculated values of φ gets bigger than 4% (23%) on the negative (positive) values of $\Delta\omega$.

Table 4-11 values are for the injection amplitude of 40uA where the desired operation region of sensitivity curve is wide and covers a wide range of frequencies. Since the simulation results convey that the model matches better for the injection signal frequencies closer to self-oscillation frequency, one way to evaluate this, would be to lower the injection signal amplitude where the desired operation region of sensitivity curve becomes narrower. Following are the results when injection current amplitude is 10uA and 5uA.

When the injection current amplitude is 10uA, the desired operation region of sensitivity curve is narrower. The injected frequencies chosen for simulation are 13.68-, 14.18-, 14.68-, 15.18-, 15.68-, 16.18-, and 16.68-GHz with the starting time of 4ns. Table 4-12 summarizes the calculation and simulation results when I_{inj}=10uA.

When the injection current amplitude is 5uA, the desired operation region of sensitivity curve gets even more narrower. The injected frequencies chosen for simulation are 14.48-, 14.68-, 14.98-, 15.18-, 15.38-, 15.68-, and 15.88-GHz.

Table 4-12 Comparison of calculation and simulation values of φ for DFF divider when I_{inj}=10uA.

Locking frequency, ω(GHz) $I_{inj=}10uA$	13.68	14.18	14.68	15.18 (ω_o)	15.68	16.18	16.68
$\varphi=0.7\times(\Delta\omega/\omega_o)$	-3.96°	-2.64°	-1.32°	0	1.32°	2.64°	3.96°
φ from simulation	-4.17°	0.42°	2.85°	4.51°	5.69°	6.48°	7.01°
φ from simulation -4.51°	-8.68°	-4.09°	-1.67°	0	1.18°	1.97°	2.50°

Table 4-13 Comparison of calculation and simulation values of φ for DFF divider when I_{inj}=5uA.

Locking frequency, ω(GHz) $I_{inj=}5uA$	14.48	14.68	14.98	15.18 (ω_o)	15.38	15.68	15.88
$\varphi=0.7\times(\Delta\omega/\omega_o)$	-1.85°	-1.32°	-0.53°	0	0.53°	1.32°	1.85°
φ from simulation	-0.84°	0.52°	1.87°	2.52°	3.01°	3.49°	3.63°
φ from simulation -2.52°	-3.36°	-1.99°	-0.65°	0	0.50°	0.98°	1.11°

Results in Table 4-11, Table 4-12, and Table 4-13 validate when the absolute value of $\Delta\omega$ increases the absolute value of φ also increases in both calculation and simulation, but the values are different between calculation and simulation.

Analyzing the values in Table 4-11, Table 4-12, and Table 4-13, also points out another difference between calculations and simulation results. Despite the independence of the calculation values to the injection amplitude, the simulation results for the same $\Delta\omega$ with different injection amplitudes are not the same. For instance, the φ from simulation for ω=14.68GHz in Table 4-12, and Table 4-13 are -1.67^{o} and -1.99^{o} respectively as opposed to their calculation values being -1.32 ^{o} for both cases.

Summarizing the findings in Table 4-11, Table 4-12, and Table 4-13, it can be noted that the calculation values for φ depend on the injection frequency but the measured values of φ from simulation, are a function of both frequency and amplitude of injection signal. This is in accordance with the findings for LC-tank and ring frequency dividers that were previously presented.

It should be noted that for small values of $\Delta\omega$ the assumption of φ being equal to $tan\varphi$ is valid for DFF frequency divider. As a result, equations (4-28) and (4-41) could be combined and with the same argument that have been done for LC-tank and ring frequency dividers, we can write:

$$-\frac{2R_{eq}C}{1+(\omega_o R_{eq}C)^2}\left(\frac{d\theta}{dt}-\Delta\omega_o\right)=\frac{i_{inj}}{i_t}.\frac{\sin\theta}{1+\frac{i_{inj}}{i_t}\cos\theta} \tag{4-42}$$

The resulting differential equation is:

$$\frac{d\theta}{dt} = -\frac{1+(\omega_o R_{eq} C)^2}{2R_{eq}C} \cdot \frac{i_{inj}}{i_t} \cdot \frac{\sin\theta}{1+\frac{i_{inj}}{i_t}\cos\theta} + \Delta\omega_o \tag{4-43}$$

As mentioned earlier, this is only valid when the injections amplitude is very low and the injection frequency is very close to self-oscillation frequency.

CHAPTER 5. SUMMARY AND CONCLUSIONS

In this thesis, three high-speed dividers, the LC-tank frequency divider, the CML ring frequency divider, and the CML DFF frequency divider with negative feedback, are analyzed based on a defined condition for injection locking. Based on the model of each topology and the concept of injection locking, the instantaneous and locking phase equations are mathematically formulated.

It should be noted that for the case of DFF frequency divider because of its very wide desired operation region, the derived equations are mainly valid either for lower injection amplitudes where the desired operation region of its sensitivity curve is relatively narrow or injection frequencies very close to its self-oscillation frequency regardless of injection amplitude.

The analytical results are compared with the simulation results utilizing a novel procedure that is developed to measure locking phase, instantaneous phase, or the phase between any two signals. This procedure provides a good ability to better understand the behavior of the divider under an impressed signal.

Regarding the locking phase, the simulation results follow a similar trend as the derived equations for all three topologies although the absolute values are different. The difference between the values can be related to the inherent difference between simulation and calculation. In calculation, locking phase φ depends on the injection frequency while in simulation, it is observed to be a function of both the frequency and amplitude of injection signal.

In summary, considering the locking phase as a function of both frequency and amplitude of the injection signal, opens a new chapter in this area of research.

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