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Device Physics and Material Properties of Two-Dimensional Semiconductors

By

Sujay Bharat Desai

A dissertation submitted in partial satisfaction of the

requirements for the degree of

Doctor of Philosophy

in

Engineering – Electrical Engineering and Computer Sciences

in the

Graduate Division

of the

University of California, Berkeley

Committee in charge:

Professor Ali Javey, Chair
Professor Junqiao Wu
Professor Tsu-Jae King Liu
Professor Jeffrey Bokor

Spring 2018

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Abstract

Device Physics and Material Properties of Two-Dimensional Semiconductors

by

Sujay Bharat Desai

Doctor of Philosophy in Electrical Engineering and Computer Sciences

University of California, Berkeley

Professor Ali Javey, Chair

Device architecture and materials innovations have enabled transistor scaling for the last several decades, boosting the performance of electronics, increasing the speed of communication and computational systems, lowering power consumption and reducing costs per operation. Two-dimensional (2D) materials have gained tremendous attention in the last decade, after the discovery of graphene which has exceptional properties like high carrier mobility, ultra-thin van der Waals connected layers (~ 0.3 nm thick), high tensile strength, etc.

Transition metal dichalcogenides (TMDs) are a family of 2D materials similar to graphene, with an important difference, many of them have an electronic bandgap. Some examples like MoS_2 and WS_2 are also direct-band gap materials at the monolayer limit (~ 0.7 nm thick). The impressive electronic and optical properties along with their ultra-thin nature, have made them potential candidates for use in future electronics and optoelectronic applications, along with other nanomaterials like carbon nanotubes.

Device physics and the electronic and optical properties of two-dimensional semiconductors are investigated in this thesis, with emphasis on TMDs. The first chapter presents an outline of the thesis and introduces 2D materials. Chapter 2 investigates the electronic properties of TMDs with focus on applications in sub-5 nm gate length transistors for low-power applications. MoS_2 channel transistors with 1-nm long carbon nanotube (CNT) gate electrodes are experimentally demonstrated, showing good On/Off current ratio of ~ 10^6 and good subthreshold swing of ~ 65 mV/decade. The electrostatics of the transistors are investigated using simulations which demonstrate an effective channel length of ~ 1 nm in the On state and ~ 4 nm in the Off state.

Chapter 3 considers the impact of an atomic-scale gate on the performance of nanoscale transistors, for example 2D materials like graphene and metallic TMDs like WTe_2, and 1D gates like graphene nanoribbons (GNRs) and CNTs. As the size of gates approaches atomic-limits, the low electronic density of states (DOS) in the gate limits the channel charge and thus the drain current. In addition, the gate DOS can be engineered to achieve a desired shape for the transfer characteristics of a transistor. The effect of gate quantum capacitance on nanoscale transistors is experimentally demonstrated, with the observation of room-temperature quantization features in CNT gated ultra-thin silicon-on-insulator (SOI) transistors (~ 3 nm thick SOI layer), which can be correlated to the Van Hove singularities in the 1D DOS of the CNT gate.

Strain engineering is an important tool used to boost mobility of carriers and enhance the performance of transistors. In chapter 4, the evolution of the electronic band structure of multilayer WSe_2 as a function of uniaxial tensile strain is investigated using photoluminescence and Raman spectroscopy. A strain induced indirect to direct bandgap transition is observed in multilayer WSe_2 with a ~ 35 x increase in photoluminescence in bilayer WSe_2.

Chapter 5 focuses on a materials processing technique to selectively obtain large area monolayer 2D materials preferentially, with high yield. A gold mediated exfoliation technique is developed to selectively transfer monolayer 2D materials onto arbitrary substrates. A gold layer deposited on top of a 2D material crystal induces strain in the top-most monolayer, resulting in a reduction of the van der Waals coupling strength of the top-most monolayer with the bulk crystal. This enables the selective peeling of the top most monolayer with high predictability and large size. The monolayers obtained, for the specific examples of TMDs were characterized using electrical device, AFM and XPS measurements, and photoluminescence and Raman spectroscopy.

The next two chapters discuss the device physics and analysis of 2D materials based devices in the context of large-area and bright light emitting monolayer devices, and lateral 2D heterostructures, using simulations and analytical modeling. A new scheme for operating light emitting devices is discussed in chapter 6. Monolayer TMD devices on insulating substrates are operated with pulsed gate voltages resulting in transient electroluminescence. The emission mechanism, generation of bipolar carrier concentration and calculation of device efficiency are discussed in detail. The light output is independent of contact barrier height and the pulsed gating technique may be useful especially for materials which are difficult to dope p, and n type, for example wide bandgap semiconductors. Finally, the monolayers absorb only ~ 10% of visible light and can be used for large area transparent displays.

Chapter 7 discusses the device physics of lateral 2D heterostructures considering the specific case of monolayer-few layer MoS_2. Using device simulations, with Kelvin Force Probe microscopy and photocurrent measurements, it is shown that a type-I heterostructure exists at the interface. Lateral 2D heterostructures by thickness modulation offer a unique way to obtain atomically sharp heterostructures with potential applications in optoelectronic devices like photodetectors. Chapter 8 presents the main conclusions of the thesis, and presents an outlook into the future of two-dimensional semiconductors.

To

my parents, my sister,

my friends and my mentors

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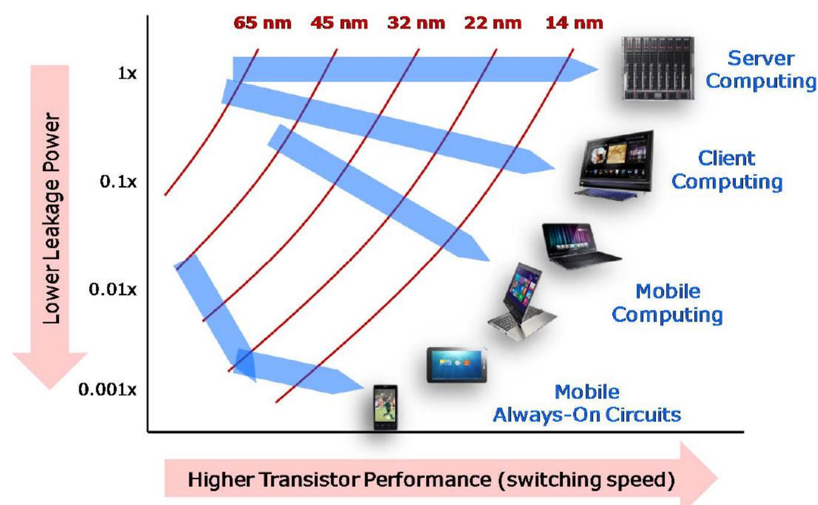
1

Introduction

1.1 Transistor scaling and materials innovation

Moore's law and transistor scaling have been the backbone of the semiconductor industry for the last several decades. Transistor sizes have been continuously scaled down, enabling us to pack more of them per unit area of a silicon die. It has led to a boost in performance of electronics, increased communication speeds, and enabled devices which are more energy efficient and also cheaper per unit operation. It has enabled many technological advancements we see today, like supercomputers, data-centers, cloud-storage and smartphones (figure 1). Throughout this time period, the transistor architecture has steadily changed and the number of materials and elements used to create an integrated circuit have steadily increased. Strain engineering of silicon to enhance electron and hole mobility in transistors and the replacement of SiO_2 gate oxide with high-k dielectrics along with the transition to 3D FinFET transistors were the monumental changes in the last two decades.



[1]

Figure 1: Electronics applications as a function of power consumption versus performance

As transistor scaling continues, it is becoming increasingly difficult to scale the transistors without impacting performance. Short channel effects, and direct source-to-drain tunneling in the sub-5 nm gate length regime, along processing related challenges remain the main roadblocks for Moore's law to continue. As part of the search for possible solutions to continue improving the performance of electronics and optoelectronics devices, two-dimensional (2D) materials have gained tremendous attention in the last decade, primarily after the discovery of graphene which

[1] M. Bohr, Intel Development Forum 2014

has exceptional properties like high carrier mobility, ultra-thin van der Waals connected layers (~ 0.3 nm thick), high tensile strength, etc. Transition metal dichalcogenides (TMDs) are a family of 2D materials similar to graphene. They are layered and many of them have a large bandgap. Some examples like MoS_2 and WS_2 are also direct-band gap materials at the monolayer limit (~ 0.7 nm thick). The impressive electronic and optical properties along with their ultra-thin nature, have made them potential candidates for use in future electronics and optoelectronic applications, similar to other nanomaterials like carbon nanotubes. This thesis investigates the device physics and the electronic and optical properties of two-dimensional semiconductors, with emphasis on TMDs (figure 2).

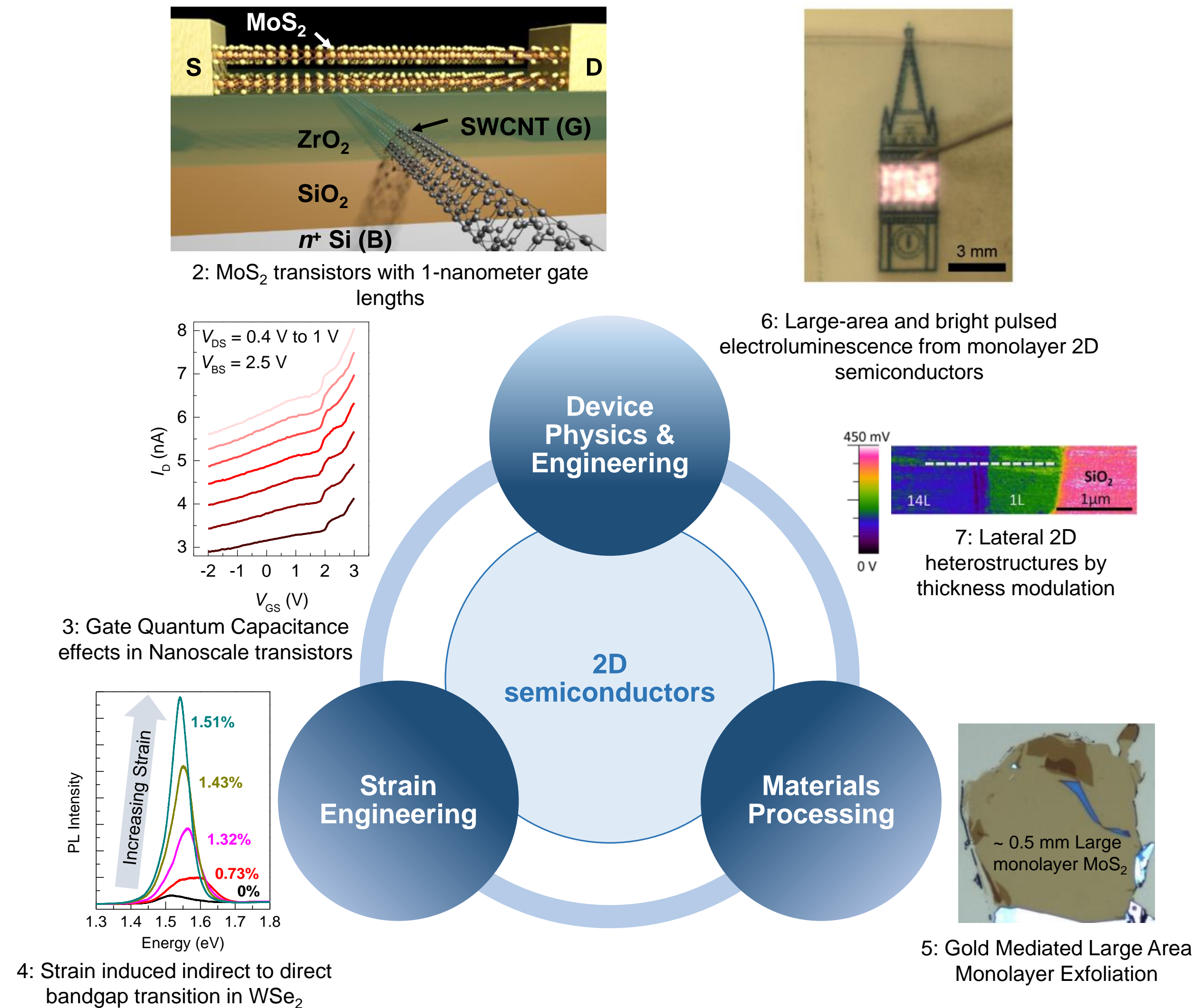


Figure 2: Thesis outline, highlighting the main projects and results, with emphasis on device physics and materials properties of 2D semiconductors. Numbering refers to the chapter numbers.

1.2 2D materials at the scaling limit of physical gate length

As transistors are scaled down, device architectures deviating from the bulk-planar MOSFET, for example FinFETs and ultra-thin body transistors perform better because of the better electrostatic control of the gate over the channel charge. However, when all the components of a transistor including the channel thickness are scaled down, surface roughness becomes an increasingly important factor, especially for 3D materials like Si. It is not possible to achieve atomically smooth silicon at thicknesses on the atomic scale, which is required for the ultimate scaled transistors. The surface roughness in channel would translate to variations in material properties along the channel, for example bandgap and mobility, and the presence of dangling bonds would degrade the performance of the device (figure 3).

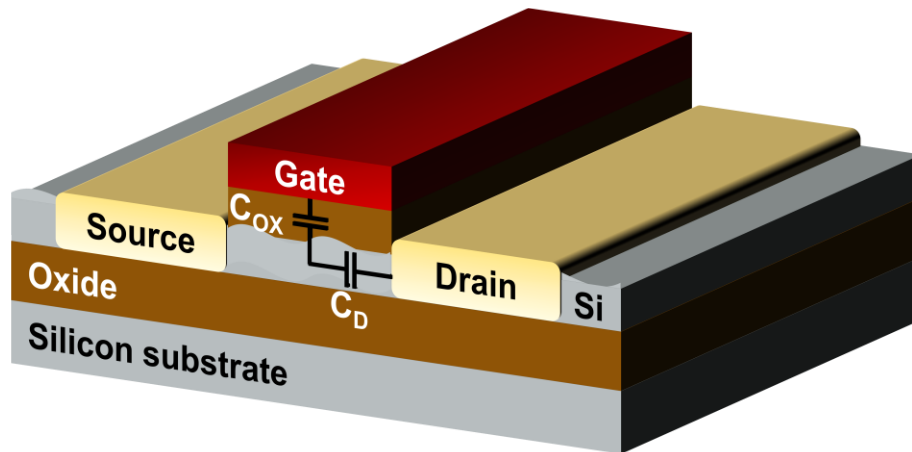


Figure 3: Schematic of an ultra-thin channel transistor, emphasizing important factors to consider with device scaling, for example, coupling of channel with drain and surface roughness of channel

The dielectric constant of the channel is also an important factor in determining the level of short channel effects in a transistor. A low in-plane dielectric constant would help reduce the capacitive coupling to the drain and thus yield a lower characteristic length which would help scale the physical gate length. At the same time, a higher dielectric constant out-of-plane would help increase the capacitive coupling to the gate and aid in reducing the short channel effects further. In the sub-5 nm gate length regime, direct source to drain tunneling is predicted especially for low effective mass materials like Si (figure 4). A large band gap, low in-plane dielectric constant and larger carrier effective mass are all important in mitigating direct source to drain tunneling.

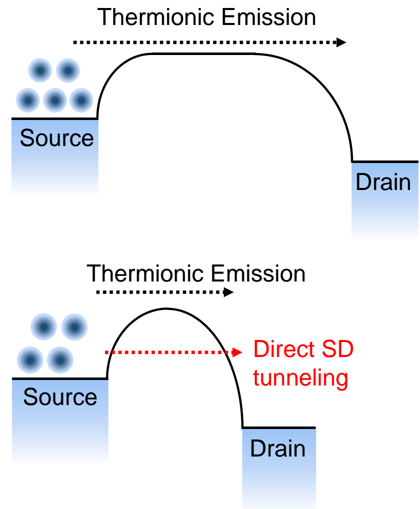


Figure 4: Schematic representation of current components at different gate lengths. At short gate lengths, direct source to drain tunneling which is undesirable becomes significant

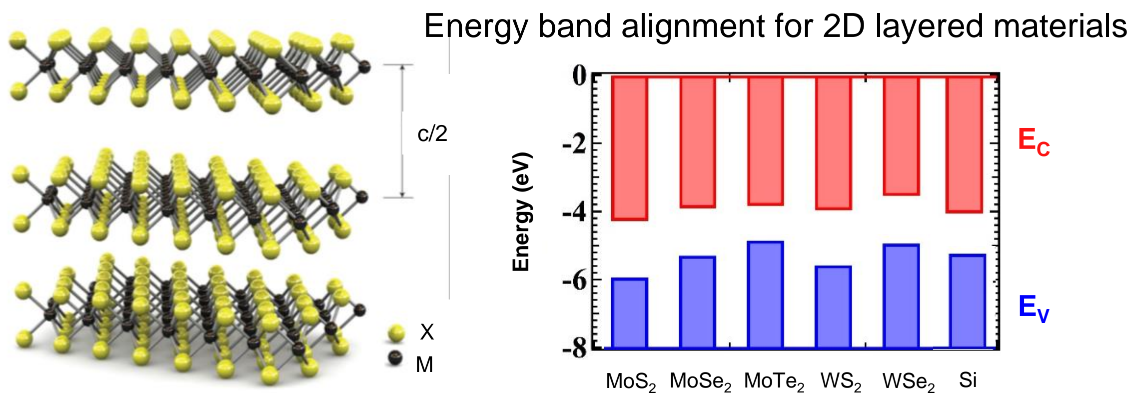


Figure 5: Schematic of TMD crystal structure and energy band alignment for some 2D layered materials relative to silicon

Relative to silicon, TMDs have uniform atomic scale thickness (example MoS_2 monolayer is ~ 0.7 nm thick), higher effective mass of carriers (0.55 m_0 for MoS_2 compared to 0.19 m_0 for silicon), larger bandgaps (MoS_2 monolayer ~ 1.85 eV, MoS_2 bilayer ~ 1.5 eV) and lower in-plane dielectric constants (~ 4 for MoS_2) (figure 5). These electronic and material properties make these materials very interesting for applications in transistors at the scaling limits of gate length.

Chapter 2 investigates the electronic properties of TMDs with focus on applications in sub-5 nm gate length transistors for low-power applications. MoS_2 channel transistors with 1-nm long carbon nanotube (CNT) gate electrodes are experimentally demonstrated, showing good On/Off current ratio of ~ 10^6 and good subthreshold swing of ~ 65 mV/decade. The electrostatics of the transistors are investigated using simulations which demonstrate an effective channel length of ~ 1 nm in the On state and ~ 4 nm in the Off state.

1.3 Effect of gate quantum capacitance in nanoscale transistors

Chapter 3 considers the impact of an atomic-scale gate on the performance of nanoscale transistors, for example 2D materials like graphene and metallic TMDs like WTe_2, and 1D gates like graphene nanoribbons (GNRs) and CNTs. As the size of gates approaches atomic-limits, the low electronic density of states (DOS) in the gate limits the channel charge and thus the drain current. In addition, the gate DOS can be engineered to achieve a desired shape for the transfer characteristics of a transistor. The effect of gate quantum capacitance on nanoscale transistors is experimentally demonstrated for the first time, with the observation of room-temperature quantization features in CNT gated ultra-thin silicon-on-insulator (SOI) transistors (~ 3 nm thick SOI layer), which can be correlated to the Van Hove singularities in the 1D DOS of the CNT gate.

1.4 Strain Engineering of 2D materials

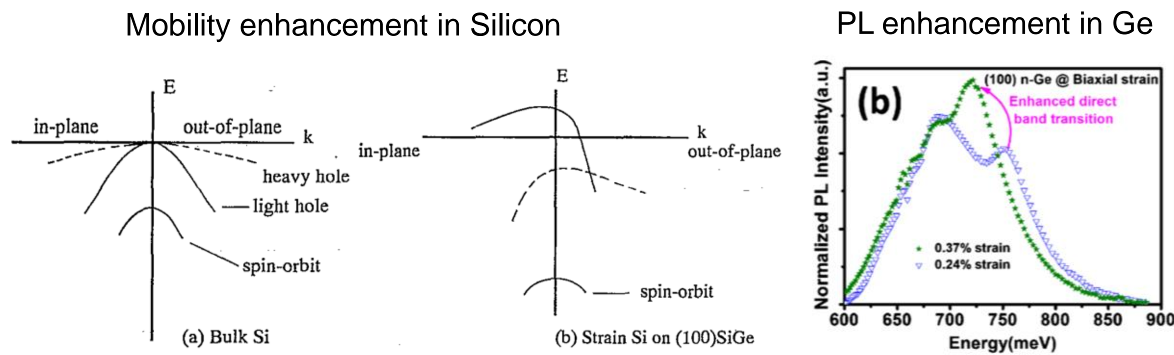


Figure 6: Applications of strain engineering in materials: Enhancement of carrier mobility in silicon and photoluminescence enhancement in germanium

Strain engineering is an important tool used to boost mobility of carriers and enhance the performance of transistors (figure 6). TMDs like MoS_2, WSe_2 and WS_2 are direct bandgap materials at the monolayer limit. However, thicker layers of these materials, from bilayer to bulk are indirect bandgap in nature (figure 7). For applications like solar cells and photodetectors, thicker direct bandgap materials are preferred, so that maximum amount of light can be absorbed in the material.

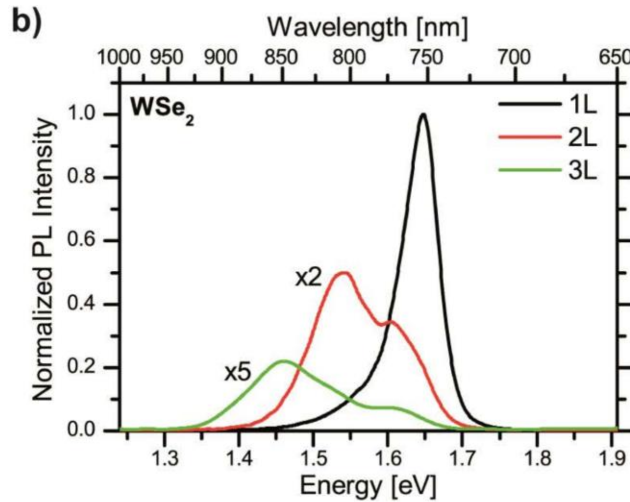


Figure 7: Photoluminescence of WSe_2 as a function of layer thickness (Tonndorf, P; R. Opt. Expr. 2013, 21 (4), 4908−4916)

In chapter 4, the evolution of the electronic band structure of multilayer WSe_2 as a function of uniaxial tensile strain is investigated using photoluminescence and Raman spectroscopy. A strain induced indirect to direct bandgap transition is observed in multilayer WSe_2 with a ~ 35 x increase in photoluminescence in bilayer WSe_2. The motivation to study the impact of strain on multilayer WSe_2 was the relatively small difference between the indirect and direct band gap energies in multilayer WSe_2, relative to other TMDs like MoS_2. For example, the difference between the indirect and direct bandgap is ~ 300 meV for bilayer MoS_2, as compared to only 40 meV for bilayer WSe_2 (figure 8).

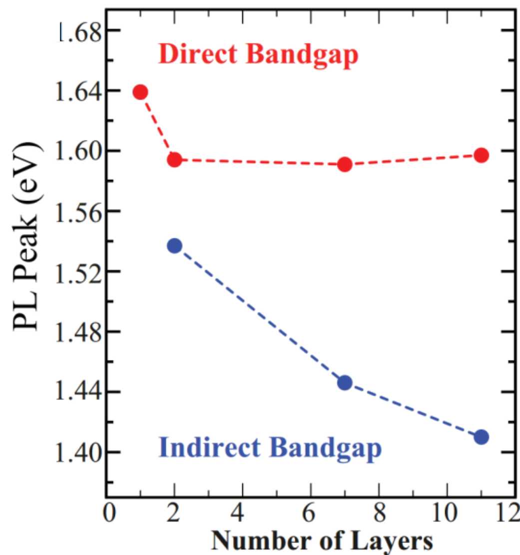
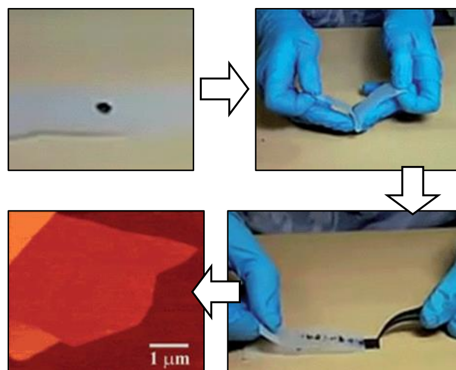


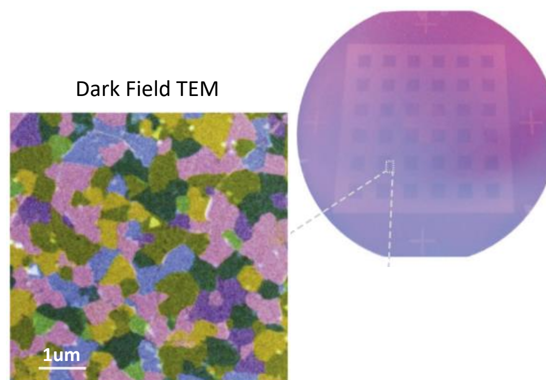
Figure 8: Evolution of the direct and indirect bandgap energies in WSe_2 as a function of layer thickness (Sahin, H.; Phys. Rev. B: Condens. Matter Mater. Phys. 2013, 87 (16), 165409)

1.5 Large-area monolayer exfoliation of 2D materials

Top down: Tape exfoliation method

Bottom Up: Chemical Vapor Deposition





DOI: 10.1039/C5TA00252D (Review Article) *J. Mater. Chem. A*, 2015, **3**, 11700-11715

Nature **520**, 656-660, (30 April 2015)

Figure 9: Common ways to obtain monolayer TMDs, mechanical exfoliation and chemical vapor deposition

Scotch tape exfoliation from bulk crystals, a technique used first to obtain monolayer graphene is one of the easiest techniques to obtain monolayer TMDs. However, the samples obtained using the mechanical tape exfoliation method, are of random thickness, monolayers and few layers are obtained with very low yield and the size of the obtained flakes is typically very small ~ 5 µm. Another way to obtain monolayer TMDs is by bottom up synthesis using techniques like chemical vapor deposition. However the quality of grown materials is dependent on growth conditions, which determines grain sizes, defect density, strain, stoichiometry, etc.

Chapter 5 focuses on a materials processing technique to selectively obtain large area monolayer 2D materials preferentially, with high yield. A gold mediated exfoliation technique is developed to selectively transfer monolayer 2D materials onto arbitrary substrates. A gold layer deposited on top of a 2D material crystal induces strain in the top-most layer, resulting in a reduction of the van der Waals coupling strength of the top-most layer with the bulk crystal. This enables the selective peeling of the top most layer with high predictability and large size. The monolayers obtained, for the specific examples of TMDs were characterized using electrical device, photoluminescence, Raman, AFM and XPS measurements.

1.6 Simulation and modeling of 2D materials based devices

Chapters 6 and 7 discuss the device physics and simulation based analysis of 2D materials based devices in the context of large-area and bright light emitting monolayer devices, and lateral 2D heterostructures.

Light emitting diodes consist of pn junctions formed by doping a semiconductor p and n type. This is difficult for 2D materials because of their ultra-thin nature. Substitutional doping would damage the 2D layer and other forms of doping like charge-transfer doping negatively

impact the optical properties and light emission efficiency of 2D materials. To circumvent this problem, a new scheme for operating monolayer semiconductor based light emitting devices is discussed in chapter 6. Monolayer TMD devices on insulating substrates are operated with pulsed gate voltages resulting in transient electroluminescence. The emission mechanism, generation of bipolar carrier concentration and calculation of device efficiency are discussed in detail. The light output is independent of contact barrier height and the pulsed gating technique may be useful especially for materials which are difficult to dope p, and n type, for example wide bandgap semiconductors. Finally, the monolayers absorb only ~ 10% of visible light and can be used for large area transparent displays.

Semiconductor heterostructures are widely used in LEDs, lasers and other optoelectronic devices. III-V materials are amongst the most widely used materials for this application because of the relative ease of forming heterostructures of different type and barrier height. However lattice mismatch in 3D heterostructures made from III-V materials can lead to defects and dislocations which degrade performance of the device. At the same time, it is difficult to define atomically sharp heterostructures using III-V materials since the boundary is generally graded due to inter-diffusion of atoms during growth. Chapter 7 discusses the device physics of lateral 2D heterostructures by means of thickness modulation, considering the specific case of monolayer-few layer MoS_2. Using device simulations, with Kelvin Force Probe microscopy and photocurrent measurements, it is shown that a type-I heterostructure exists at the interface.

2

[2]MoS_2 Transistors with 1-Nanometer Gate Lengths

2.1 Direct source-to-drain tunneling and short channel effects

As Si transistors rapidly approach their projected scaling limit of ~ 5 nm gate lengths, exploration of new channel materials and device architectures is of utmost interest (*1-3*). This scaling limit arises from short channel effects (*4*). Direct source-to-drain tunneling and the loss of gate electrostatic control on the channel severely degrade the OFF-state leakage currents, thus limiting the scaling of Si transistors (*5, 6*). Certain semiconductor properties dictate the magnitude of these effects for a given gate length. Heavier carrier effective mass, larger band gap and lower in-plane dielectric constant yield lower direct source-to-drain tunneling current (*7*). Uniform and atomically thin semiconductors with low in-plane dielectric constants are desirable for enhanced electrostatic control of the gate. Thus, investigation and introduction of semiconductors that have more ideal properties than Si could lead to further scaling of transistor dimensions with lower OFF-state dissipation power.

Transition metal dichalcogenides (TMDs) are layered 2-dimensional (2D) semiconductors that have been widely explored as a potential channel material replacement for Si (*8-11*), and each material exhibits different band structure and properties (*12-16*). The layered nature of TMDs allows uniform thickness control with atomic level precision down to the monolayer limit. This thickness scaling feature of TMDs is highly desirable for well-controlled electrostatics in ultrashort transistors (*3*). For example, monolayer and few-layer MoS_2 have been shown theoretically to be superior to Si at the sub-5 nm scaling limit (*17, 18*).

The scaling characteristics of MoS_2 and Si transistors as a function of channel thickness and gate length are summarized in Fig. 1. We calculated direct source-to-drain tunneling currents ($I_{SD\text{-}LEAK}$) in the OFF-state for different channel lengths and thicknesses using a dual-gate device structure (Fig. S1) as a means to compare the two materials. MoS_2 shows more than two orders of magnitude reduction in $I_{SD\text{-}LEAK}$ relative to Si mainly because of its larger electron effective mass along the transport direction ($m_n^* \sim 0.55m_0$ for MoS_2 versus $m_n^* \sim 0.19m_0$ for Si [100]) (*19*), with a trade-off resulting in lower ballistic ON-current. Notably, $I_{SD\text{-}LEAK}$ does not limit the scaling of monolayer MoS_2 even down to the ~ 1 nm gate length, presenting a major advantage over Si [more details about calculations in supplementary materials (*20*)]. Finally, few-layer MoS_2 exhibits a lower in-plane dielectric constant (~ 4) compared to bulk Si (~ 11.7), Ge (~ 16.2) and GaAs (~ 12.9), resulting in a shorter electrostatic characteristic length (λ) as depicted in Fig. S2 (*21*).

The above qualities collectively make MoS_2 a strong candidate for the channel material of future transistors at the sub-5 nm scaling limit. However, to date, TMD transistors at such small

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[2] Reprinted with permission from Sujay B. Desai, et. al., *Science*, 354, 99-102, 2016, Copyright 2016 American Association for the Advancement of Science

gate lengths have not been experimentally explored. Here, we demonstrate 1D gated 2D semiconductor field-effect transistors (1D2D-FET) with a single-walled carbon nanotube (SWCNT) gate, a MoS_2 channel and physical gate lengths of ~ 1 nm. The 1D2D-FETs exhibit near ideal switching characteristics, including a subthreshold swing (SS) of ~ 65 mV/decade at room temperature and high ON/OFF current ratios. The SWCNT diameter d ~ 1 nm for the gate electrode (*22*) minimized parasitic gate to source-drain capacitance, which is characteristic of lithographically patterned tall gate structures. The ~ 1 nm gate length of the SWCNT also allowed for the experimental exploration of the device physics and properties of MoS_2 transistors as a function of semiconductor thickness (i.e., number of layers) at the ultimate gate length scaling limit.

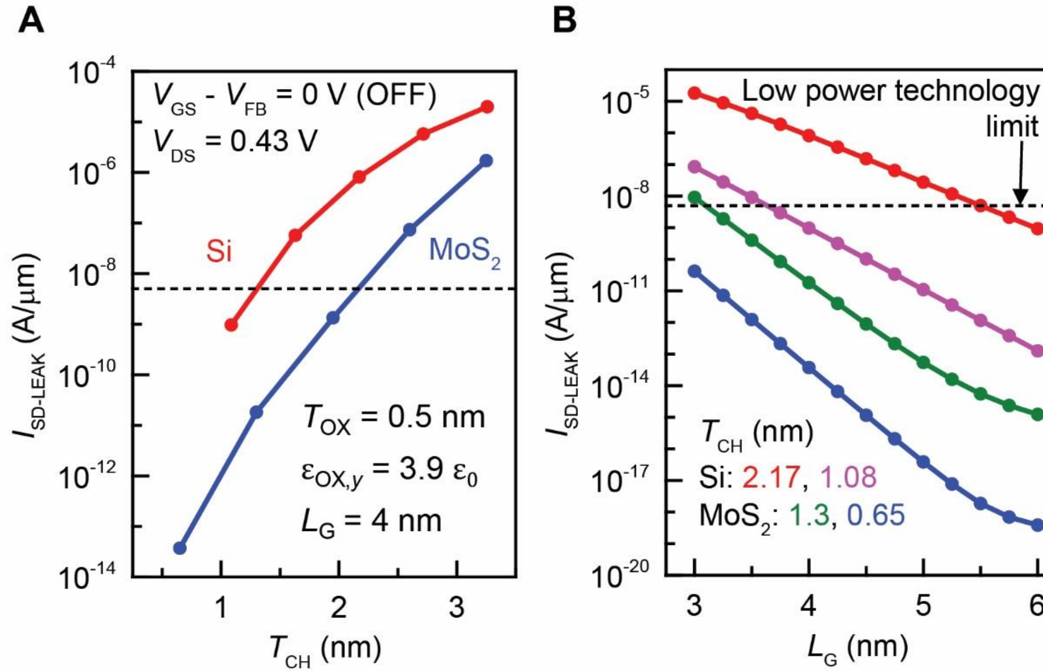


Figure 1: Direct source-to-drain leakage current. **(A)** Normalized direct source-to-drain leakage current ($I_{SD\text{-}LEAK}$), calculated using the WKB approximation as a function of channel thickness T_{CH} for Si and MoS_2 in the OFF-state. $V_{DS} = V_{DD} = 0.43$ V from international technology roadmap for semiconductors (ITRS) 2026 technology node. **(B)** $I_{SD\text{-}LEAK}$ as a function of gate length L_G for different thicknesses of Si and MoS_2 for the same OFF-state conditions as figure 1A. The dotted line in figures 1A and 1B represents the Low Operating Power (LOP) limit for the 2026 technology node as specified by the ITRS.

2.2 Device structure and electrical characterization

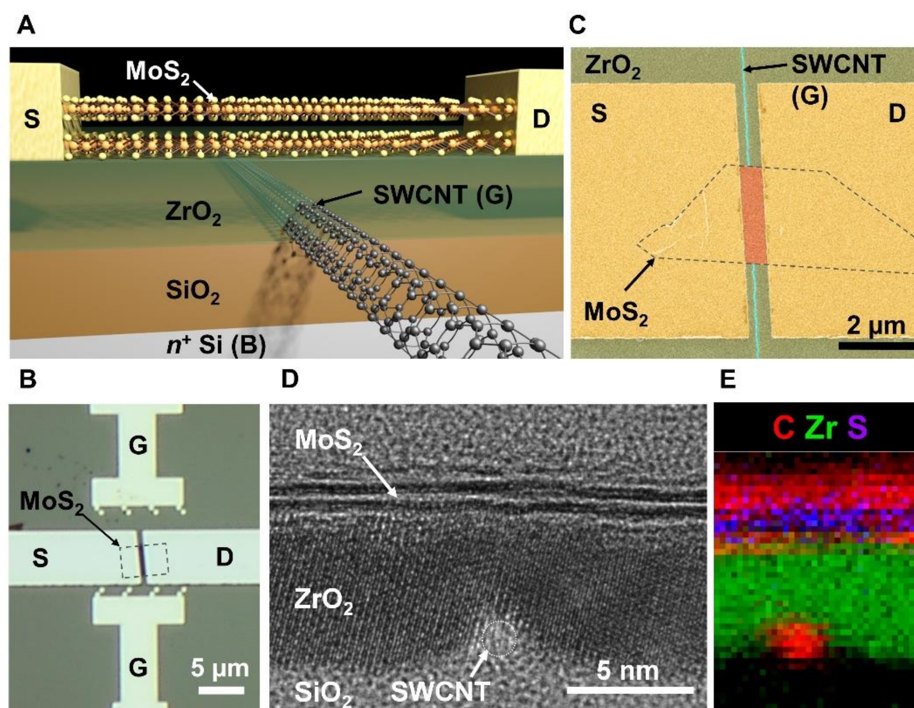


Figure 2: 1D2D-FET device structure and characterization. **(A)** Schematic of 1D2D-FET with a MoS_2 channel and SWCNT gate. **(B)** Optical image of a representative device shows the MoS_2 flake, gate (G), source (S) and drain (D) electrodes. **(C)** False-colored scanning electron microscope (SEM) image of the device showing the SWCNT (blue), ZrO_2 gate dielectric (green), MoS_2 channel (orange) and the Ni source and drain electrodes (yellow). **(D)** Cross-sectional TEM image of a representative sample showing the SWCNT gate, ZrO_2 gate dielectric and bilayer MoS_2 channel. **(E)** EELS map showing spatial distribution of carbon, zirconium and sulfur in the device region, conforming the location of the SWCNT, MoS_2 flake and the ZrO_2 dielectric.

The experimental device structure of the 1D2D-FET (Fig. 2A) consists of a MoS_2 channel (number of layers vary), a ZrO_2 gate dielectric, and a SWCNT gate, on a 50 nm SiO_2/Si substrate, with a physical gate length (L_G, ~ d) of ~ 1 nm. Long, aligned SWCNTs grown by chemical vapor deposition were transferred onto a n^+ Si/SiO_2 substrate (50 nm thick SiO_2) (*23*), located with scanning electron microscopy (SEM), and contacted with Pd via lithography and metallization. These steps were followed by atomic layer deposition (ALD) of ZrO_2, and pick-and-place dry transfer of MoS_2 onto the SWCNT covered by ZrO_2 (*14*). Nickel source and drain contacts were made to MoS_2 to complete the device. The detailed process flow and discussion about device fabrication is provided in Fig. S3.

Figure 2B shows the optical image of a representative 1D2D-FET capturing the MoS_2 flake, the source drain contacts to MoS_2 and the gate contacts to the SWCNT. The SWCNT and the MoS_2 flake can be identified in the false-colored scanning electron microscope (SEM) image of a representative sample (Fig. 2C). The 1D2D-FET consists of four electrical terminals; source (S), drain (D), SWCNT gate (G) and the n^+ Si substrate back gate (B). The SWCNT gate underlaps

the S/D contacts. These underlapped regions were electrostatically doped by the Si back gate during the electrical measurements, thereby serving as n^+ extension contact regions. The device effectively operated like a junctionless transistor (*24*), where the SWCNT gate locally depleted the n^+ MoS_2 channel after applying a negative voltage and thus turning OFF the device.

A cross-sectional transmission electron microscope (TEM) image of a representative 1D2D-FET (Fig. 2D) shows the SWCNT gate, ZrO_2 gate dielectric (thickness ~ 5.8 nm), and the bilayer MoS_2 channel. The topography of ZrO_2 surrounding the SWCNT and the MoS_2 flake on top of the gate oxide was flat as seen in the TEM image. This geometry is consistent with ALD nucleation initiating on the SiO_2 substrate surrounding the SWCNT, and eventually covering it completely as the thickness of deposited ZrO_2 exceeds the SWCNT diameter, *d* (*25*). The spatial distribution of carbon, zirconium, and sulfur was observed in the electron energy loss spectroscopy (EELS) map of the device region (Fig. 2E), thus confirming the location of the SWCNT, ZrO_2 and MoS_2 in the device (Fig. S4) (*20*).

The electrical characteristics for a 1D2D-FET with a bilayer MoS_2 channel (Fig. 3) show that the MoS_2 extension regions (the underlapped regions between the SWCNT gate and S/D contacts) could be heavily inverted (i.e., n^+ state) by applying a positive back gate voltage of V_{BS} = 5 V to the Si substrate. The I_D-V_{BS} characteristics (Fig. S5) indicate that the MoS_2 flake was strongly inverted by the back gate at V_{BS} = 5 V. The I_D-V_{GS} characteristics for the device at V_{BS} = 5 V and V_{DS} = 50 mV and 1 V (Fig. 3A), demonstrate the ability of the ~ 1 nm SWCNT gate to deplete the MoS_2 channel and turn OFF the device. The 1D2D-FET exhibited excellent subthreshold characteristics with a near ideal SS of ~ 65 mV/decade at room temperature and ON/OFF current ratio of ~ 10^6. The drain-induced barrier lowering (DIBL) was ~ 290 mV/V. Leakage currents through the SWCNT gate (I_G) and the n^+ Si back gate (I_B) are below the measurement noise level (Fig. 3A). The interface trap density (D_{IT}) of the ZrO_2-MoS_2 interface estimated from SS was ~ 1.7×10^{12} cm^{-2} eV^{-1}, which is typical for transferred MoS_2 flakes (*26*) because of the absence of surface dangling bonds (*20*).

Figure 3B shows the I_D-V_{DS} characteristics at different V_{GS} values and fixed V_{BS} = 5 V. The I_D-V_{GS} characteristics depended strongly on the value of V_{BS}, which affects the extension region resistance. The inversion of the extension regions increased with increasing V_{BS}, thus reducing the series resistance and contact resistance and led to an increase in the ON-current and an improvement in the SS. At more positive values of V_{BS}, V_{GS} had to be more negative in order to deplete the MoS_2 channel, which in turn made the threshold voltage more negative. Above V_{BS} = 1 V, the SS and I_{ON} did not improve any further and the extension regions were strongly inverted (Fig. 3C). Thus, the 1D2D-FET operated as a short channel device.

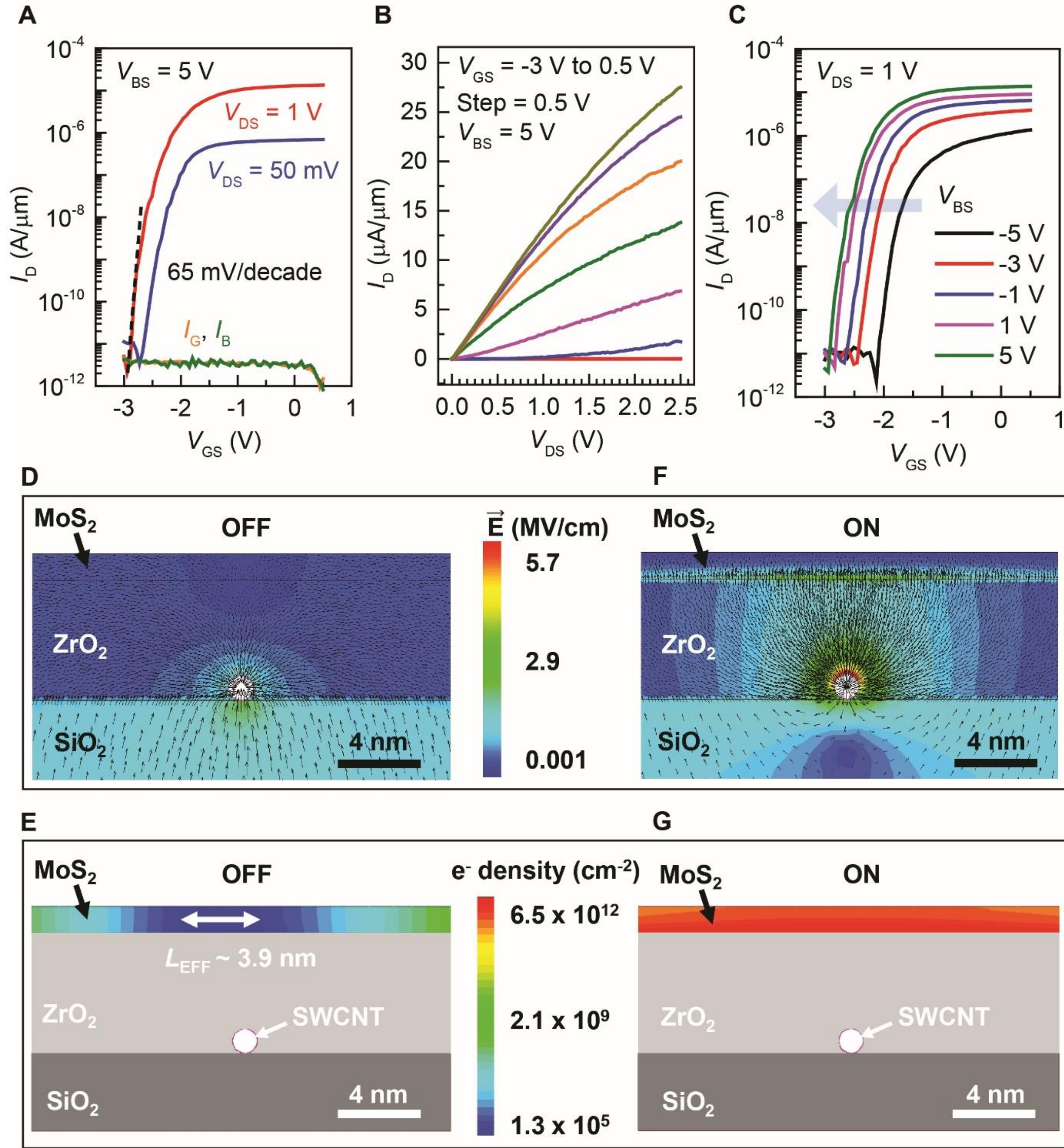


Figure 3: Electrical characterization and TCAD simulations of 1D2D-FET (A) I_D-V_{GS} characteristics of a bilayer MoS_2 channel SWCNT gated FET at V_{BS} = 5 V and V_{DS} = 50 mV and 1 V. The positive V_{BS} voltage electrostatically dopes the extension regions n^+. **(B)** I_D-V_{DS} characteristic for the device at V_{BS} = 5 V and varying V_{GS}. **(C)** I_D-V_{GS} characteristics at V_{DS} = 1 V and varying V_{BS} illustrating the impact of back gate bias on the extension region resistance, SS, ON-current and device characteristics. Electric field contour plots for a simulated bilayer MoS_2 device using TCAD in the **(D)** OFF and **(F)** ON-state. Electron density plots for the simulated device using TCAD in the **(E)** OFF and **(G)** ON-state. The electron density in the depletion region is used to define the effective channel length (L_{EFF}). L_{EFF} ~ d ~ L_G in the ON-state and $L_{EFF} > L_G$ in the OFF-state because of the fringing electric fields from the SWCNT gate.

2.3 Simulation results and electrostatics

We performed detailed simulations using Sentaurus TCAD to understand the electrostatics of the 1D2D-FET. The OFF- and ON-state conditions correspond to (V_{GS} - V_T) of -0.3 V and 1.5 V, respectively (which give an ON/OFF current ratio ~ 10^6). The electric field contour plot (Fig. 3D) in the OFF-state has a region of low electric field in the MoS_2 channel near the SWCNT, indicating that it is depleted. The reduced electron density in the MoS_2 channel (Fig. 3E), and the presence of an energy barrier to electrons in the conduction band (Fig. S6A) are also consistent with the OFF-state of the device. The extension regions are still under inversion because of the positive back gate voltage. The electron density of the MoS_2 channel in the depletion region can be used to define the effective channel length (L_{EFF}) of the 1D2D-FET, which is the region of channel controlled by the SWCNT gate (*27-29*). The channel is considered to be depleted if the electron density falls below a defined threshold ($n_{threshold}$). The OFF-state L_{EFF}, defined as the region of MoS_2 with electron density $n < n_{threshold}$ ($n_{threshold} = 1.3\times10^5$ cm^{-2}), for this simulated 1D2D-FET is L_{EFF} ~ 3.9 nm (Fig. 3E). Note that L_{EFF} is dependent on V_{GS} and the value of $n_{threshold}$ (Fig. S7).

As the device is turned OFF, the fringing electric fields from the SWCNT (Fig. 3D) deplete farther regions of the MoS_2 channel, and thus increase L_{EFF}. The short height of the naturally defined SWCNT gate prevents large fringing fields from controlling the channel, and hence achieves a smaller L_{EFF} compared to lithographically patterned gates (Fig. S8). The electric field and electron density contours for the device in the ON-state confirm the strong inversion of the channel region near the SWCNT (Fig. 3, F and G) with L_{EFF} ~ L_G = 1 nm. The energy bands in this case are flat in the entire channel region (Fig. S6B), with the ON-state current being limited by the resistance of the extension regions and mainly the contacts. Doped S-D contacts along with shorter extension regions will result in increased ON-current.

The impact of T_{OX} scaling on short channel effects like DIBL was also studied using simulations (Fig. S9). The electrostatics of the device improves, and the influence of the drain on the channel reduces as T_{OX} is scaled down to values commensurate with L_G. This effect is seen by the strong dependence of DIBL on T_{OX}, thus demonstrating the need for T_{OX} scaling and high-k 2D dielectrics to further enhance the device performance.

2.4 Channel thickness dependence

The effect of MoS_2 thickness on the device characteristics was systematically explored. At the scaling limit of the gate length, the semiconductor channel thickness must also be scaled down aggressively as described earlier. The electrostatic control of the SWCNT gate on the MoS_2 channel decreased with increasing distance from the ZrO_2-MoS_2 interface. Thus, as the MoS_2 flake thickness was increased, the channel could not be completely depleted by applying a negative V_{GS}. Because of this effect, the SS for a 12 nm thick MoS_2 device (~ 170 mV/decade) was much larger than that of bilayer MoS_2 (~ 65 mV/decade), and as the thickness of MoS_2 was increased to ~ 31

nm the device could no longer be turned OFF (Fig. 4A). The experimental SS as a function of MoS_2 thickness was qualitatively consistent with the TCAD simulations (Fig. 4B and S10), showing an increasing trend with increasing channel thickness. The unwanted variations in device performance caused by channel thickness fluctuations (Fig. 4B and S10), and the need for low OFF-state current at short channel lengths (Fig. 1 and 3), thus justify the need for layered semiconductors like TMDs at the scaling limit.

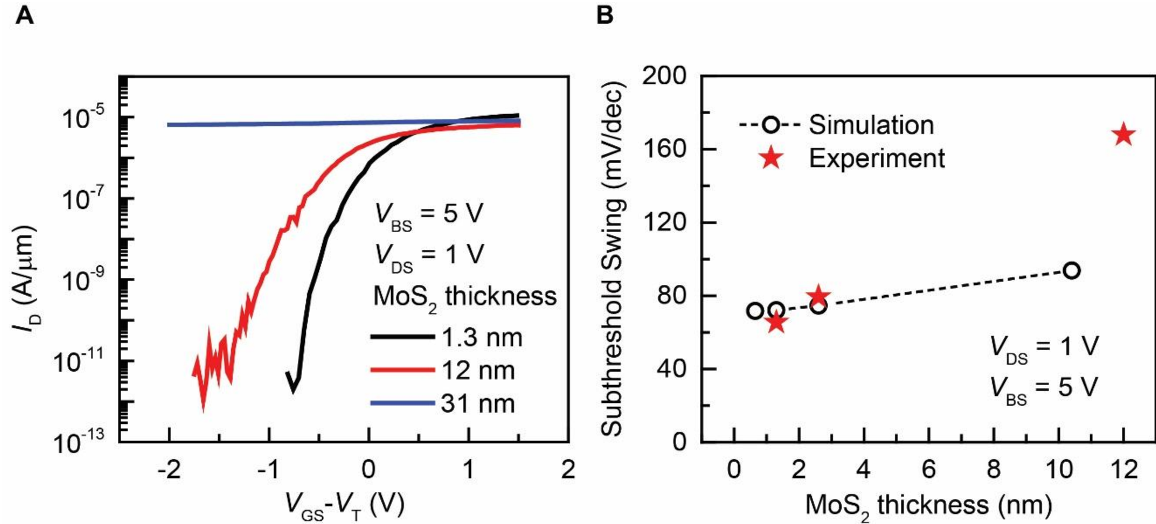


Figure 4: MoS_2 thickness dependence. (A) Dependence of MoS_2 channel thickness on the performance of 1D2D-FET. SS increases with increasing MoS_2 channel thickness. **(B)** Extracted SS from experimental curves and TCAD simulations show increasing SS as channel thickness T_{CH} increases.

TMDs offer the ultimate scaling of thickness with atomic level control, and the 1D2D-FET structure enables the study of their physics and electrostatics at short channel lengths by using the natural dimensions of a SWCNT, removing the need for any lithography or patterning processes which are challenging at these scale lengths. However, large-scale processing and manufacturing of TMD devices down to such small gate lengths are existing challenges requiring future innovations. For instance, research on developing process-stable low-resistance ohmic contacts to TMDs, and scaling of the gate dielectric by using high-κ 2D insulators is essential to further enhance device performance. Wafer-scale growth of high quality films (*30*) is another challenge toward achieving very-large-scale integration of TMDs in integrated circuits. Finally, fabrication of electrodes at such small scale lengths over large areas requires significant advances in lithographic techniques. Nevertheless, the work here provides new insight into the ultimate scaling of gate lengths for a FET by surpassing the 5 nm limit (*3-7*) often associated with Si technology.

2.5 Supporting Information

Materials and methods:

SWCNT growth on quartz: Aligned SWCNTs were grown according to a process similar to (*23*) modified to deliver a low aligned SWCNT density. 4" ST-cut quartz wafers were purchased from Hoffman Materials, Inc. then annealed at 900°C for 8.5 hours to repair the surface crystal. A ≈3.66 Å film of iron (99.95% pure) was evaporated using electron-beam evaporation onto 4µm wide stripes defined using photo-lithography at a rate of 0.33 Å/s. This was followed by metal liftoff and resist removal. The sample was grown in a 5" diameter FirstNano EasyTube 3000 CNT CVD furnace. The temperature was ramped to 610 °C in O_2 for calcination, then to 865 °C in 120 sccm H_2 at 315 Torr for reduction of the iron catalyst. After stabilizing temperature for 10 minutes, 1 SLM of CH_4 was introduced to the chamber to begin growth. After one hour, the sample was cooled in H_2 ambient. The SWCNT density as measured by SEM was 1 SWCNT per 15 µm across the wafer.

SEM (scanning electron microscopy) imaging was performed using a Zeiss Gemini Ultra-55 field emission scanning electron microscope (FESEM). A ~ 1 kV accelerating voltage was used for imaging the devices and to register the locations of the SWCNTs with respect to pre-patterned lithography markers.

AFM (atomic force microscopy) was performed using a Digital Instruments Nanoscope Dimension 3100 AFM. The AFM was done in the tapping mode using ~ 300 kHz resonance frequency, Budget sensors Tap300-G tapping mode tips.

TEM (transmission electron microscopy) / STEM (scanning transmission electron microscopy): High resolution TEM/STEM imaging was performed using a probe-corrected JEM-ARM200F (JEOL USA, Inc.) operated at 200 kV. HAADF-STEM imaging was carried out with a 24 mrad convergence semi-angle electron beam and the collection angle for the ADF detector was set to 90-370 mrad.

Elemental Mapping: Electron energy loss spectroscopy (EELS) and energy dispersive spectroscopy (EDS) mapping was performed with a Gatan Enfina spectrometer and X-MaxN 100TLE detector (Oxford Instruments), respectively. The collection angle for the EELS spectrum was set to be 31 mrad. The spatial resolution of the mapping is 0.27 nm/pixel and the collection time is 0.4 s/pixel.

Electrical characterization: Electrical measurements were performed under vacuum (~ 10^{-5} mbar) in Lakeshore vacuum probe station using Agilent Technologies B1500A Semiconductor Device Analyzer.

Analytical 2D electrostatics model for Dual Gate Metal-Oxide-Semiconductor Field-Effect Transistor (DGMOS-FET) (*21, 31*)

A symmetric DGMOS-FET structure is assumed as shown in Fig. S1. An analytical solution to the 2D Poisson equation is derived assuming a channel material with anisotropic dielectric constant using the approach taken in reference (*21*).

$$\vec{\nabla}.\vec{D} = \rho \ldots (1)$$

$$\begin{bmatrix} Dx \\ Dy \\ Dz \end{bmatrix} = \begin{bmatrix} \varepsilon x & 0 & 0 \\ 0 & \varepsilon y & 0 \\ 0 & 0 & \varepsilon z \end{bmatrix} \begin{bmatrix} Ex \\ Ey \\ Ez \end{bmatrix} \ldots (2)$$

$$\varepsilon_x \frac{\partial^2 \varphi}{\partial x^2} + \varepsilon_y \frac{\partial^2 \varphi}{\partial y^2} = qN_A \ldots (3)$$

Equation 3 is Poisson's equation in 2D considering an anisotropic dielectric constant. Here the axes of transport X and Y (Fig. S1) are assumed to coincide with the crystal axes of the material. Thus the electric permittivity tensor is diagonal. To solve the differential equation 3 and get an analytical expression for the electric potential, we assume the first term on the left hand side to be much smaller than the second term (quasi-2D approximation). The 2D electric potential in the channel region is then computed similar to the procedure in reference (*21*).

$$\varphi(x, y) = \frac{y^2 \varepsilon_{OX,y}(V_{GS} - V_{FB} - \varphi_S(x))}{\varepsilon_{CH,y} T_{CH} T_{OX}} - \frac{y \varepsilon_{OX,y}(V_{GS} - V_{FB} - \varphi_S(x))}{\varepsilon_{CH,y} T_{OX}} + \varphi_s(x) \ldots (4)$$

Here $\varphi_s(x)$ is the surface potential.

Equation 4 is evaluated at the center of the channel to give $\varphi_C(x) = \varphi(x, \frac{T_{CH}}{2})$ and is then expressed in terms of $\varphi_C(x)$ by replacing $\varphi_s(x)$. $\varphi(x, y)$ which is expressed in terms of $\varphi_C(x)$ must satisfy equation 3. After substitution into equation 3 and simplification we get,

$$\frac{\partial^2 \varphi_C(x)}{\partial x^2} + \frac{1}{\lambda^2}\left(V_{GS} - V_{FB} - \varphi_C(x) - \frac{qN_A \lambda^2}{\varepsilon_{CH,x}}\right) = 0 \ldots (5)$$

where λ is the characteristic length of the device.

$$\lambda = \sqrt{\frac{\varepsilon_{CH,x} T_{CH} T_{OX}}{2\varepsilon_{OX,y}}\left(1 + \frac{\varepsilon_{OX,y} T_{CH}}{4\varepsilon_{CH,y} T_{OX}}\right)} \ldots (6)$$

From the above equation we see that the characteristic length depends on the dielectric constant along both x and y. The larger the dielectric constant along y, the more the influence of gate voltage and smaller the characteristic length and short channel effects. On the other hand, a large dielectric constant along x means the influence of drain voltage on the channel increases and short channel effects such as DIBL become more prominent. The boundary conditions for solving equation 5 are $\varphi_C(0) = V_{bi}$ and $\varphi_C(L_G) = V_{bi} + V_{DS}$. Considering the case of very light to no

doping in the channel i.e. N_A ~ 0 (hence $V_{bi} = \frac{E_g}{2q}$) , and solving equation 5 with the above boundary conditions we get,

$$\varphi_C(x) = (V_{GS} - V_{FB})\left(1 - e^{-\frac{x}{\lambda}}\right) + V_{bi}e^{-\frac{x}{\lambda}} - \frac{\sinh\left(\frac{x}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)}(V_{GS} - V_{FB} - V_{bi})\left(1 - e^{-\frac{L}{\lambda}}\right) + V_{DS}\frac{\sinh\left(\frac{x}{\lambda}\right)}{\sinh\left(\frac{L}{\lambda}\right)} \quad \ldots (7)$$

Using $\varphi_C(x)$ as found above, the potential at the surfaces $\varphi_S(x)$ and the 2D potential in the entire channel $\varphi(x, y)$ can also be computed using equation 4. The barrier between the source and drain in the OFF-state is dependent on V_{bi} and hence the bandgap (E_g) of the semiconductor. The larger the bandgap, the larger is the OFF-state barrier between source and drain. λ determines the shape of the barrier between source and drain.

The quasi-2D model provides a good qualitative analysis of the electrostatics in a DGMOSFET for comparing different channel materials. For more accurate analysis, first principle calculations and self-consistent solutions of the Schrodinger-Poisson equations are essential.

Direct source-to-drain tunneling leakage

A qualitative estimate of the amount of direct source-to-drain tunneling in a material in the OFF-state can be obtained using the electrostatic model derived above. The WKB approximation (equation 8) is used to compute the probability of tunneling across the energy barrier, and the Landauer relation (equation 9) is used to calculate the leakage current due to tunneling (*32, 33*).

$$T(E) = e^{-\frac{2}{\hbar}\int_{x_i}^{x_o}\sqrt{2m^*(E_C(x)-E)}dx} \quad \ldots (8)$$

$$I_{SD-LEAK} = \frac{2q}{h}\int_{E_S}^{E_{C,max}} M(E)\,T(E)\left[f\left(E, E_{F,S}\right) - f\left(E, E_{F,D}\right)\right] dE \quad \ldots (9)$$

$$M(E) = \frac{W\sqrt{2m^*(E-E_S)}}{\pi\,\hbar} \quad \ldots (10)$$

The parameter values used for the calculations in Fig. 1 are given in table S1.

In equation 8, $T(E)$ is the tunneling probability through the energy barrier at energy level E. x_o and x_i indicate the extent of the barrier. $E_C(x)$ is the conduction band profile between the source and drain from x_i to x_0. m^* is the effective mass of the carriers tunneling through the barrier.

In equation 9, $I_{SD\text{-}LEAK}$ is the direct source to drain leakage current. $M(E)$ is the number of ballistic modes of transport at energy E (equation 10) (*32*), E_S is the energy level of the source (reference) and $E_{C,max}$ is the top of the conduction band profile between the source and drain. $f(E)$ is the Fermi-Dirac distribution and $E_{F,S}$ and $E_{F,D}$ are the Fermi levels in source and drain respectively.

TMDCs have a higher effective mass along the direction of transport (e.g. $m_n^* \sim 0.55m_0$ for MoS_2 versus $m_n^* \sim 0.19m_0$ for Si [100]) (*19, 34*) which reduces the tunneling probability and therefore $I_{SD\text{-}LEAK}$. Figure 1 discusses the impact of effective mass on transistor scaling using the example of a symmetric double-gate MOSFET (DGMOS-FET) structure (Fig. S1). Figure 1A shows normalized $I_{SD\text{-}LEAK}$ as a function of channel thickness for Si and MoS_2. The channel conduction band profile required to calculate $I_{SD\text{-}LEAK}$ is derived using the analytical 2D DGMOS-FET electrostatic model proposed in ref (*21*). The parameter values used in the calculations (table S1) account for quantum mechanical effects on the bandgap, dielectric constant and effective mass at ultra-thin channel thicknesses (*19, 35-39*). MoS_2 shows more than two orders reduction in $I_{SD\text{-}LEAK}$ compared to Si due to the larger electron effective mass. Figure 1B plots the dependence of $I_{SD\text{-}LEAK}$ on L_G. The dotted lines in Fig. 1A and 1B represent the Low Operating Power (LOP) limit for the 2026 technology node as specified by the international technology roadmap for semiconductors (ITRS) (*40*). Figure 1B reveals that for similar channel thickness, MoS_2 transistors can be scaled to shorter gate lengths as compared to Si.

Calculation of D_{IT}

$$SS = \frac{kTln(10)}{q}\left(1 + \frac{C_D + C_{IT}}{C_{OX}}\right) \ldots (11)$$

Equation 11 relates SS to the interface trap density for the device (*41*). Here *k* is the Boltzmann constant, *T* is temperature in Kelvin and *q* is the charge of an electron. For the 1D2D-FET structure, C_D (depletion capacitance) ~ 0, C_{IT} (interface trap capacitance) = qD_{IT} and C_{OX} (oxide capacitance) = ε_{OX}/T_{OX}. ε_{OX} is the permittivity of the gate oxide (ZrO_2 dielectric constant ~ 25 (*42*)) and T_{OX} is the oxide thickness (~ 5.8 nm) measured from TEM in Fig. 2D.

Analytical derivation of parasitic capacitance from fringing electric fields

Figure S8 shows the fringing electric field lines in an underlap transistor. The fringing electric field lines lead to parasitic capacitance ($C_{parasitic}$) and a larger effective channel length (L_{EFF}).

$$C_{OX} = \frac{L_G W \varepsilon_{OX}}{T_{OX}} \ldots (12)$$

$$C_{parasitic} \approx \int_{T_{OX}}^{T_{ZrO2}} \left(\frac{2W\varepsilon_{OX}}{\pi y}\right) dy = \left(\frac{2W\varepsilon_{OX}}{\pi}\right) \ln\left(\frac{T_{ZrO2}}{T_{OX}}\right) = \left(\frac{2W\varepsilon_{OX}}{\pi}\right) \ln\left(1 + \frac{T_G}{T_{OX}}\right) \ldots (13)$$

Equation 12 gives the capacitance C_{OX} for the parallel electric field lines from the gate electrode to the channel. ε_{OX} is the electric permittivity of the gate dielectric, *W* is the width and L_G is the physical gate length. $T_{OX} = (T_{ZrO2} - T_G)$ is kept constant for devices of different gate heights (T_G). Equation 13 calculates the parasitic capacitance due to the fringing electric field lines from the gate electrode and is dependent on T_G. Larger the height of the electrode, higher is the parasitic capacitance. The natural short height of a SWCNT helps achieve small L_{EFF} and small $C_{parasitic}$ compared to lithographically patterned tall gate structures. The above simplistic analytical derivation for $C_{parasitic}$ assumes the fringing electric field lines to be circular (Fig. S8) and

underestimates the capacitance. For accurate analysis, simulation of the 2D electrostatics in the device is essential.

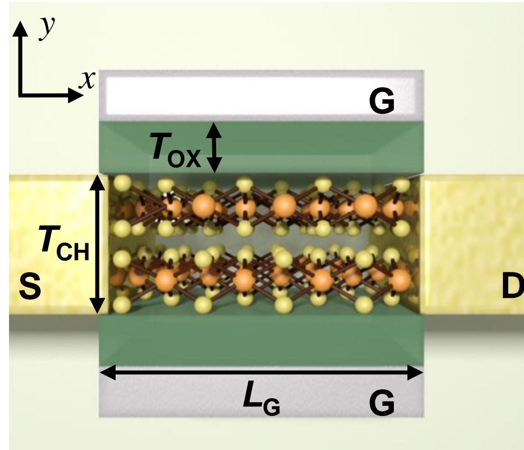


Figure S1: Schematic of dual-gated metal-oxide-semiconductor-field-effect-transistor. Schematic of a symmetric dual-gated metal-oxide-semiconductor-field-effect-transistor (DGMOS-FET) used to study impact of channel material properties on the scaling limit of transistors in Fig. 1.

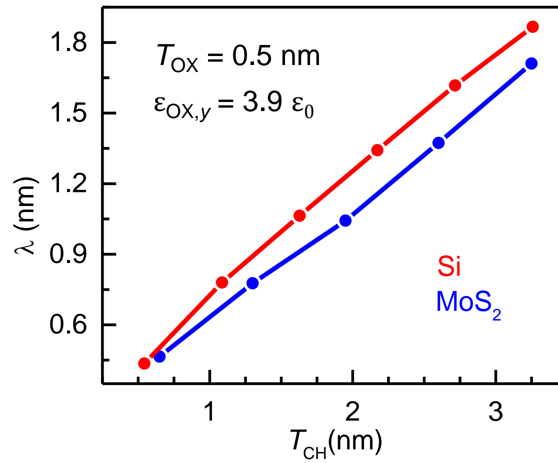
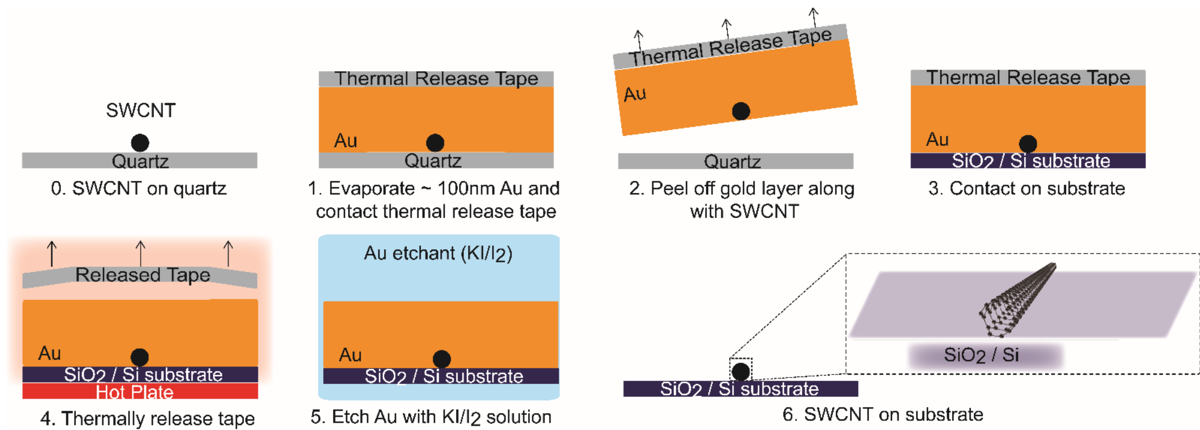
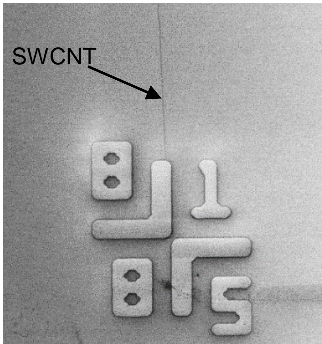
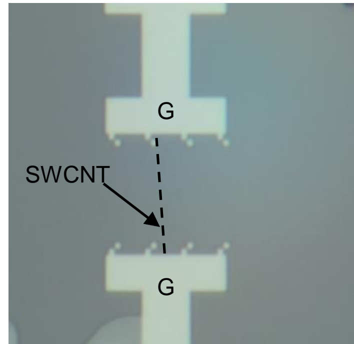
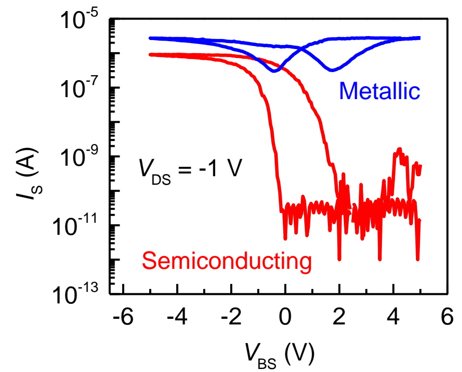


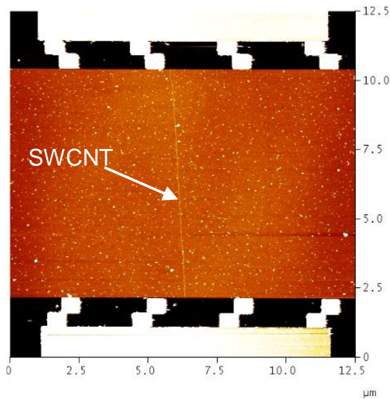
Figure S2: Dependence of characteristic length on channel thickness. Device electrostatic characteristic length (λ) as a function of channel thickness (T_{CH}) for Si and MoS_2.

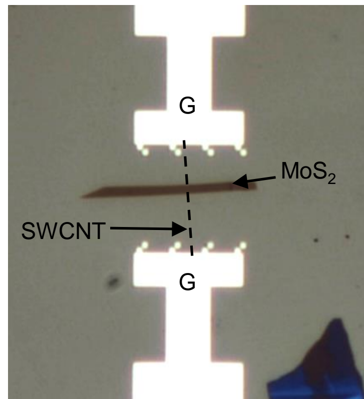












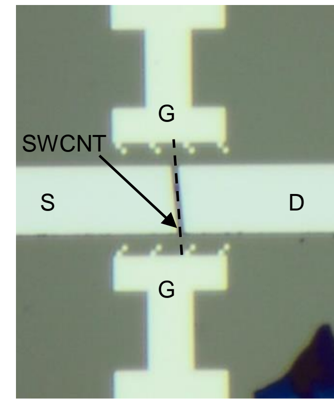


Figure S3: Detailed process flow for SWCNT gated MoS_2 FET

Figure S3 shows the detailed process flow for the device fabrication. The first step of the process involves the transfer of grown SWCNT from the growth substrate (quartz) to the target 50 nm SiO_2 / Si substrate using gold as the transfer layer (*23*) (Fig. S3A). The target substrate is pre-patterned with 0.5/30 nm Cr/Pt alignment markers. These alignment markers are used to relatively locate the transferred SWCNT in a scanning electron microscope (SEM) image (Fig. S3B). Care is taken to

ensure the SWCNTs are not damaged during the SEM by minimizing the exposure time under the electron-beam. Gate electrodes are then patterned using electron-beam lithography followed by 30 nm Pd evaporation and liftoff process (Fig. S3C). I_S-V_{BS} measurements of the SWCNT devices help to identify the metallic or semiconducting nature of the SWCNT (Fig. S3D). After the measurement, the SWCNT devices are mapped with an atomic force microscope (AFM) to find the relative location of the SWCNT with respect to the gate electrodes (Fig. S3E). Post the AFM map, ZrO_2 gate dielectric is deposited using atomic layer deposition (ALD) and the MoS_2 flake is transferred on top using a dry pick and transfer method (*14*) using poly(methyl methacrylate) (PMMA) as the transfer medium (Fig. S3F). The AFM map taken prior to the ALD is then used as a mask for a second electron-beam lithography step, to pattern the source and drain electrodes (Ni 40 nm) as shown in Fig. S3G, thus completing the device fabrication.

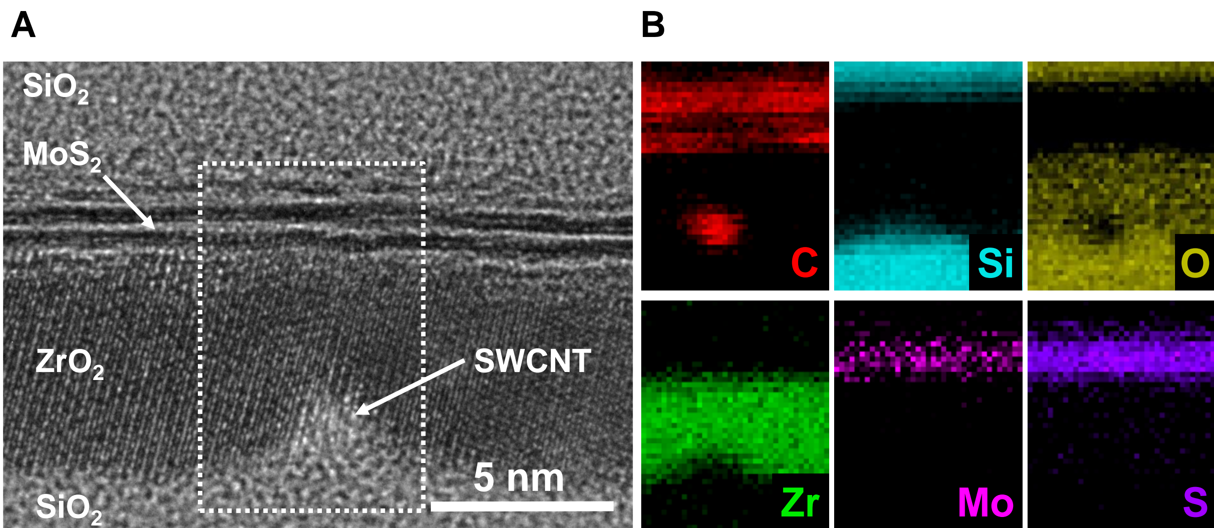


Figure S4: EELS map. EELS mapping of the 1D2D-FET showing the spatial location of the different elements (EDS map is shown for Mo). Carbon mapping clearly indicates the position of the SWCNT under the ZrO_2 gate dielectric and the MoS_2 flake on top of it. Carbon seen on top of the ZrO_2 can be attributed to organic residue like PMMA and contaminants from processing steps and dry transfer of MoS_2.

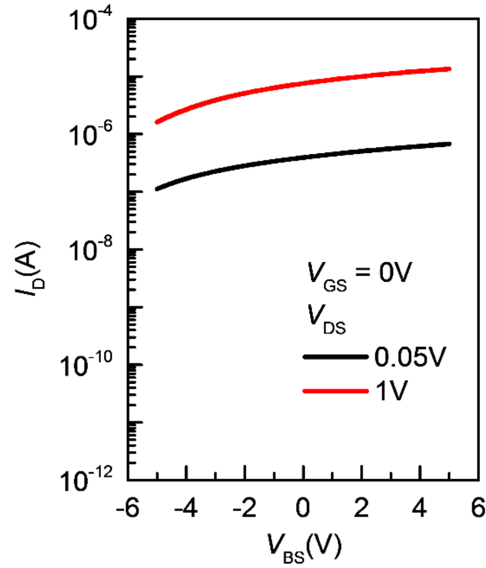


Figure S5: I_D-V_{BS} characteristics obtained by varying the n^+ Si back gate. I_D-V_{BS} characteristics for the device in Fig. 3A-C. The MoS_2 extensions regions are completely inverted using the Si back gate at V_{BS} = 5 V.

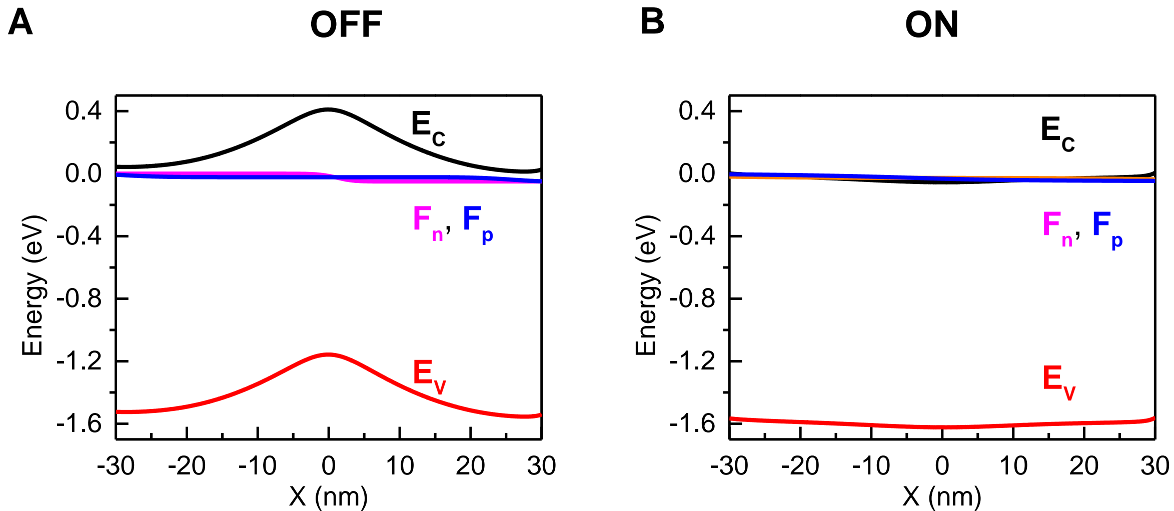


Figure S6: Energy band diagrams in ON and OFF-states. Energy band diagrams corresponding to the TCAD simulations in Fig. 3D-G. V_{BS} = 5 V, V_{DS} = 50 mV, (V_{GS} - V_T) = 1.5 V (ON) and (V_{GS} - V_T) = -0.3 V (OFF), for the 2L MoS_2 device. In the OFF-state the bias applied to the SWCNT creates a barrier which opposes the flow of carriers from source to drain. In the ON-state no barrier exists to the flow of electrons from the source to drain and the ON-current is limited by the series resistance of the extension regions.

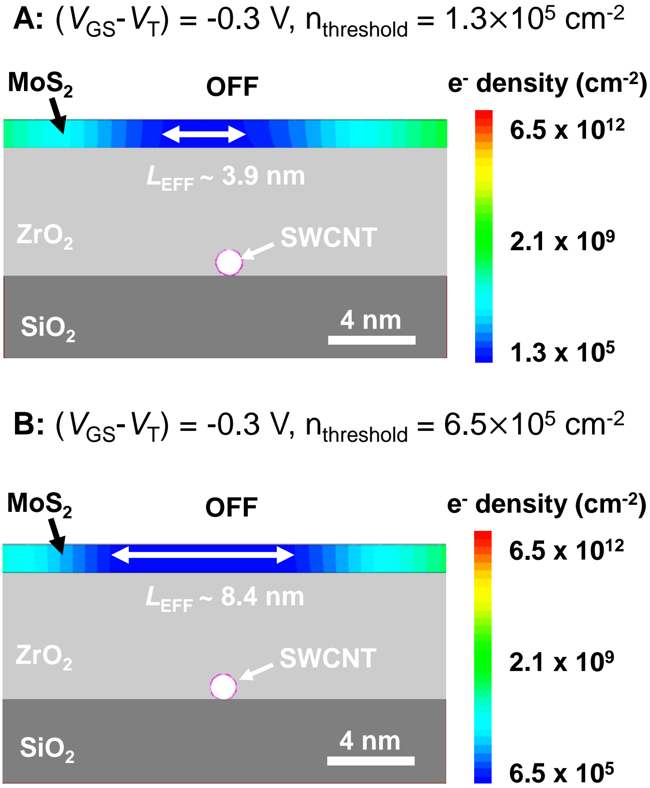


Figure S7: Electron density contour plots. Dependence of L_{EFF} on the definition of OFF-state and $n_{thershold}$ (electron density below which the channel is considered depleted) for V_{BS} = 5 V, V_{DS} = 50 mV (*27-29*). The OFF-state corresponds to (V_{GS} - V_T) = -0.3 V and ON-state corresponds to (V_{GS} - V_T) = 1.5 V (or an ON/OFF current ratio of ~ 10^6). L_{EFF} is of the order of 5 nm as seen from the simulations. The 2D electron density is obtained by multiplying the 3D density obtained from simulations with T_{CH}, by assuming uniform distribution along the thickness of MoS_2.

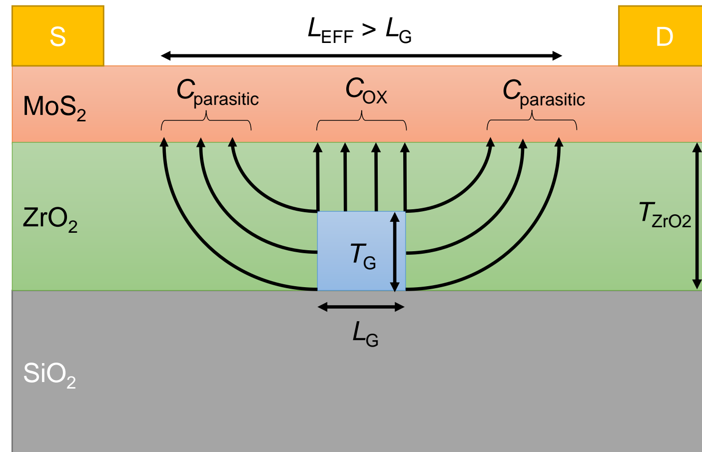


Figure S8: Parasitic capacitance and dependence on gate height. Effective channel length (L_{EFF}) > physical gate length (L_G) due to fringing electric field. L_{EFF} and $C_{parasitic}$ increase as the height of the gate (T_G) increases, for the same value of T_{OX} ($T_{ZrO2} - T_G$). L_{EFF} and $C_{parasitic}$ are small for a SWCNT gate as compared to lithographically defined gates because of the naturally short height of a SWCNT, and hence less fringing electric field lines coupling to the channel (*43*).

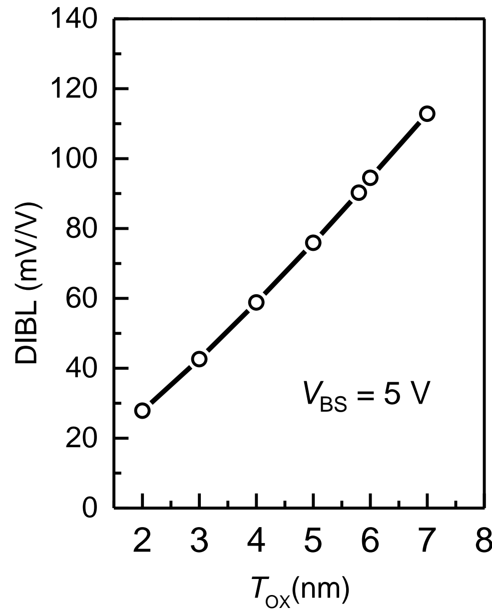


Figure S9: Dependence of DIBL on gate oxide thickness. Drain-induced barrier-lowering (DIBL) as a function of the ZrO_2 thickness calculated using simulations. Effective oxide thickness (EOT) scaling helps improve the electrostatics in the device and reduce DIBL.

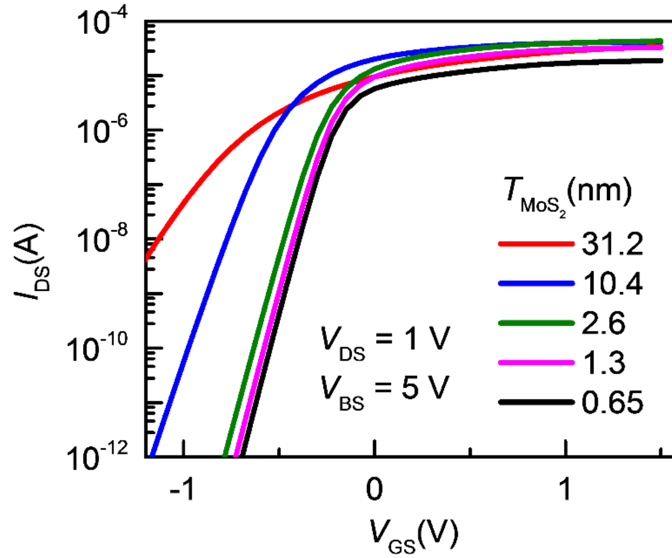


Figure S10: Thickness dependence of MoS_2. I_{DS}-V_{GS} curves for several different channel thicknesses from TCAD simulations used to calculate SS in Fig. 4B. The TCAD results qualitatively match the experimental trends. Doping of MoS_2 (N_D) is assumed to be 10^{17} cm^{-3}, and the dielectric constant of ZrO_2 = 25 (*42*). Electron affinity of MoS_2 is assumed to be 4 eV (*44*). All other values are as specified in table S1. For more quantitative comparison, the analysis must involve simulation of the 2D density of states for MoS_2, correction for contact resistance, oxide and interface traps, along with using more accurate values for m^*, E_G, N_D, etc.

Table S1: Parameter values used for calculations in Fig. 1 and Fig. S2. Values have been extracted

MoS_2				**Si**			
T_{CH} (nm)	**ε (relative)** (*35*)	**E_G** (*38*)	**m_e*** (*19*)	**T_{CH} (nm)**	**ε (relative)** (*36*)	**E_G** (*37*)	**m_e*** (*39*)
0.65	3.93	1.88	~ 0.55	0.5431	4.39		~ 0.22
1.3	4.71	1.59	~ 0.55	1.0862	6.62	1.90	~ 0.22
1.95	4.90	1.47	~ 0.55	1.6293	7.66	1.46	~ 0.22
2.6	6.24	1.44	~ 0.55	2.1724	8.70	1.31	~ 0.22
3.25	7.71	1.42	~ 0.55	2.7155	9.73	1.23	~ 0.22
10.4	~ 10	~ 1.3	~ 0.55	3.2586	10.32	1.19	~ 0.22
31.2	~ 10.5	~ 1.3	~ 0.55				

from references (*19, 35-39*). The effects of quantum confinement at atomic-scale channel thicknesses on parameter values like bandgap, dielectric constant and effective mass are considered for more accurate analysis. The bandgap values for MoS_2 correspond to the optical bandgap from photoluminescence spectra. The bandgap of Si is obtained from optical absorption spectra.

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3

[3]Gate Quantum Capacitance Effects in Nanoscale Transistors

3.1 Introduction

Nanomaterials like graphene, transition metal dichalcogenides (TMDs), carbon nanotubes (CNTs) and graphene nanoribbons (GNRs) have been proposed as potential materials for use in future scaled transistors [1-7]. These materials have low electronic density of states (DOS) resulting from their low-dimensional nature. The impact of quantum capacitance (C_Q) of a low-dimensional channel material has become increasingly important, with increasing oxide capacitance (C_{OX}) resulting from aggressively scaled effective oxide thicknesses (EOT) [8, 9]. As the overall transistor and physical gate dimensions continue to shrink, nanomaterials like graphene and carbon nanotubes have been proposed as potential gate electrode materials because of their large conductivity at these atomic-scale sizes [1, 6, 10]. However, with the finite number of atoms in atomic-scale gates comes the problem of low gate DOS, which also impacts transistor characteristics and performance.

The gate charge (Q_G) in an ideal MOSFET is always equal and opposite of the total channel charge (Q_{CH}) in the semiconductor [11]. An applied drain-source bias (V_{DS}) across the channel results in a flow of the inversion charge (Q_{INV}) and hence the drain current (I_D). For MOSFETs with large-volume metal gate electrodes, the gate has a large DOS and an almost infinite capacity to balance Q_{CH}. However, for a low-dimensional atomic-scale gate the limited gate DOS limits Q_G, thereby limiting Q_{CH}, especially in inversion when Q_{INV} is large. The starvation of DOS in the gate will dictate the I_D characteristics in this case.

In this work, we consider the impact of gate C_Q on the transistor characteristics by developing an analytical electrostatics model for a bulk silicon channel MOSFET [10]. This is studied by computing the functional dependence of the gate electrostatic potential (V_Q) and the value of Q_G on the gate DOS and the applied gate bias (V_{GS}), for several different gate materials with different dimensionalities [10, 12]. We experimentally demonstrate for the first time, room-temperature gate C_Q effects on the I_D characteristics for an ultra-thin silicon-on-insulator (SOI) channel transistor with a 1-dimensional (1D) single walled carbon nanotube (SWCNT) gate electrode. Quantization features resulting from the Van Hove singularities in the DOS of the CNT gate are observed in the transfer characteristics of the device. Finally, we discuss the potential of engineering the gate DOS to tailor the shape of the I_DV_{GS} characteristics of a device and the impact of gate C_Q on the performance of nanoscale transistors.

[3] A manuscript similar to this chapter has been submitted to a peer-reviewed journal for publication

3.2 Analytical electrostatics model

The concept of gate C_Q limited transistors is illustrated in figure 1a using the example of a bulk silicon channel MOSFET with gate electrodes of varying dimensionality. Figure 1b shows the DOS for the specific case of carbon based gates; graphite for 3D, graphene for 2D and carbon nanotube for 1D gate [13-15]. In a MOSFET with a bulk 3D gate, the gate DOS is very large and thus it can accommodate any Q_G needed to support an equal and opposite charge in the channel ($Q_{CH} = Q_{INV} + Q_{DEP}$), where Q_{INV} and Q_{DEP} are the inversion and depletion charge densities respectively. As the dimensionality of the gate and the physical size reduces, the gate DOS is limited and in this case V_Q is related to Q_G by equation 1 [8, 10].

$$Q_G = \int_0^{V_Q} C_Q(V')\mathrm{d}V' \ldots (1)$$

Here C_Q represents the quantum capacitance of the gate and can be calculated using equation 2.

$$C_Q(V_Q) = q^2 \int_{-\infty}^{\infty} g(E)\left(-\frac{\partial f(E, E_{F,G})}{\partial E}\right)\mathrm{d}E \ldots (2)$$

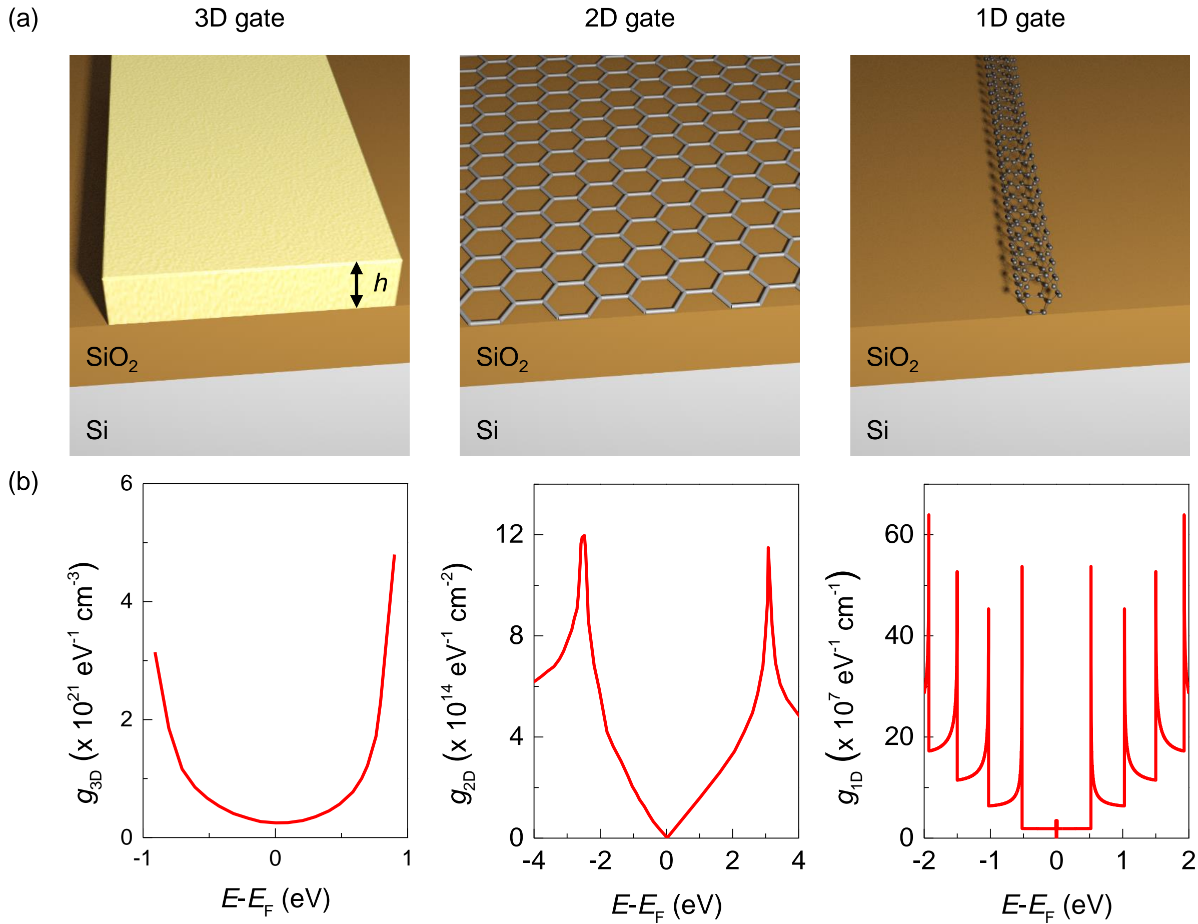


Figure 1: Gate quantum capacitance effects in nanoscale transistors: (a) Schematic of a bulk Si MOSFET and (b) the density of states for 3D (graphite, h = 100 nm), 2D (graphene) and 1D (CNT (n,m) = (18,18)) gate

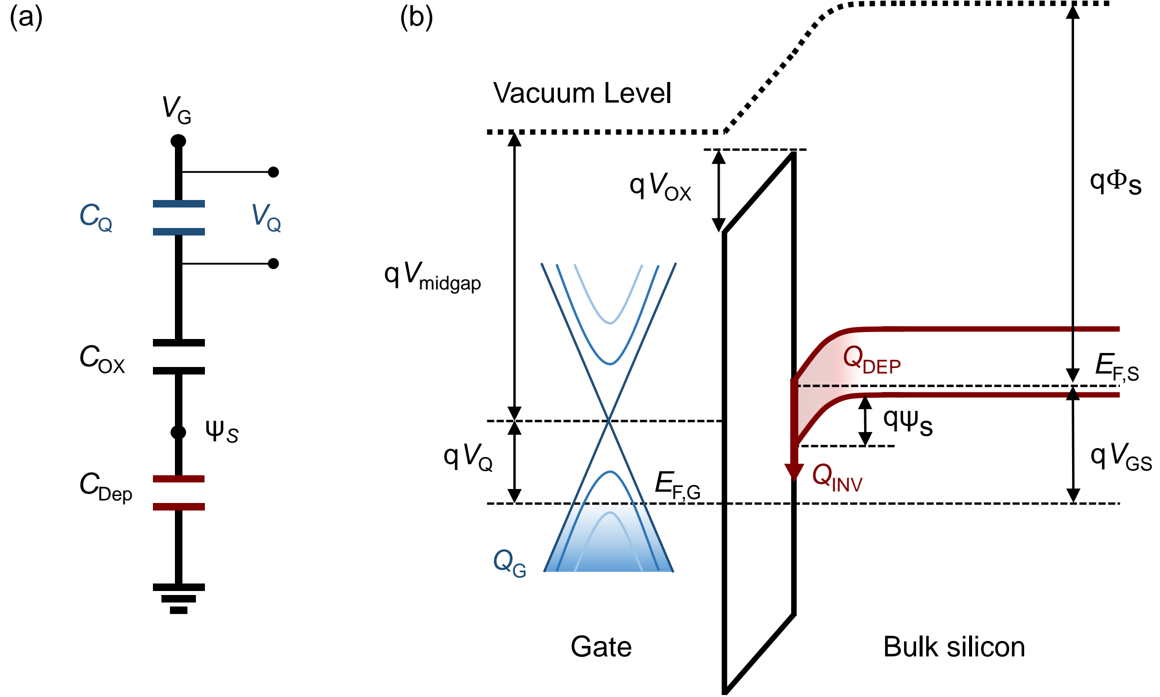


Figure 2: Equivalent model and energy band diagram: (a) Capacitance model for bulk Si MOSFET considering quantum capacitance of the gate electrode. (b) Energy band diagram showing the different model parameters

The electrostatic potential of the gate $V_Q = -(E_{F,G}/q)$, where $E_{F,G}$ is the Fermi level of the gate. $g(E)$ is the electronic density of states of the gate, $f(E, E_{F,G})$ is the Fermi-Dirac distribution and q is the electronic charge. The equivalent circuit model including the gate C_Q is shown in figure 2a. Figure 2b depicts the energy band diagram for the device (with p-doped bulk silicon) along the gate to channel direction. The first few energy bands of the gate material are schematically represented for the example case of a semi-metallic gate. V_{midgap} corresponds to the work function of the gate material in the intrinsic state. For example in the case of a graphene gate, V_{midgap} equals V_{Dirac} which corresponds to the Dirac point of graphene [10, 12]. In inversion, when a gate bias V_{GS} is applied to the MOSFET a potential difference V_Q develops across the gate corresponding to the charge Q_G. Equation 3 describes the relation among all the parameters mentioned here,

$$V_{GS} = V_Q + V_{OX} + (V_{midgap} - \Phi_s) + \psi_s \ldots (3)$$

Here the voltage across the gate oxide $V_{OX} = (Q_G/C_{OX})$, ψ_s is the band bending in the channel near the interface and $\Phi_s = \left(\chi_{Si} + \frac{E_{G,Si}}{2} + \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right)$ is the work function of bulk silicon with χ_{Si}, $E_{G,Si}$ n_i and N_A^- being the electron affinity, band gap, intrinsic carrier concentration and ionized acceptor ion concentration in bulk Si respectively [11]. In inversion, $\psi_s = 2\phi_f = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right)$ and Q_{INV} can be calculated using equation 4,

$$Q_{INV} = Q_G - Q_{DEP} = Q_G - qN_A\sqrt{\left(\frac{2\varepsilon_{Si}*2\phi_f}{qN_A}\right)} \ldots (4)$$

Solving equations 1-4 numerically, V_Q, Q_G and Q_{INV} can be computed for a fixed value of the other parameters and for an applied bias V_{GS}. Details of the calculations are provided in the supporting information.

Using the electrostatic model developed here, V_Q, Q_G and Q_{INV} values are calculated as a function of V_{GS} for several different gate materials ranging from 3D, 2D to 1D gates (figure 3). For 3D gates (figure 3a and 3d) we consider TiN and graphite gates with a thickness (h) of 100 nm. We observe that for bulk 3D gates like TiN and graphite which have large electronic DOS near the Fermi level, V_Q is very small and almost zero (figure 3a and figure S1) [13, 16, 17]. This is consistent with the case of an ideal metal gate for which $V_Q = 0$ for all values of Q_G, because of the infinite DOS and hence infinite capacitance of the metal. Correspondingly, Q_{INV} for 3D gates closely follows the expression for MOSFET inversion charge density given by $Q_{INV} = C_{OX}$ (V_{GS} - V_T) (figure 3d) [11]. Thus in the case of 3D gates, the gate DOS does not limit Q_{INV} and thus does not impact the MOSFET I_D characteristics.

Figures 3b and 3e show the calculated values of V_Q and Q_{INV} for 2D gates, specifically for the case of graphene and monolayer WTe_2 which is metallic in the 1T phase [14, 18-20]. Due to the limited DOS for these gate materials and especially for graphene around the Dirac point, V_Q is a larger fraction of the applied V_{GS}, and correspondingly Q_{INV} is less than the value for the case of an ideal metal gate. Thus Q_{CH} is limited by the Q_G which is dictated by $g(E)$ for the gate. The impact of the gate DOS on Q_{INV} versus V_{GS} characteristics is most prominently visible for 1D gates. The specific cases considered here are a semiconducting GNR with chirality (n,m) = (15,0) and a metallic CNT with chirality (n,m) = (18,18) as shown in figures 3c and 3f [15]. Quantization features resulting from the Van Hove singularities in the DOS for the GNR and CNT are visible in the V_Q versus V_{GS} and Q_G versus V_{GS} characteristics in figures 3c and 3f respectively. Similar to the case of 2D gates the gate DOS limits the Q_{INV} and more interestingly the features of the gate DOS get capacitively mapped onto the transfer characteristics of the device because I_D is linearly proportional to Q_{INV}. Thus engineering the DOS of the gate is a useful technique to obtain desired transfer characteristics. The DOS for all the different gate materials used in the calculations are provided in figure S1. All the calculations were performed for $T = 10$ K. The impact of temperature induced broadening is studied by calculating Q_G as a function of V_Q at $T = 10$ K and 300 K for the CNT and GNR cases mentioned earlier (see methods and figure S2).

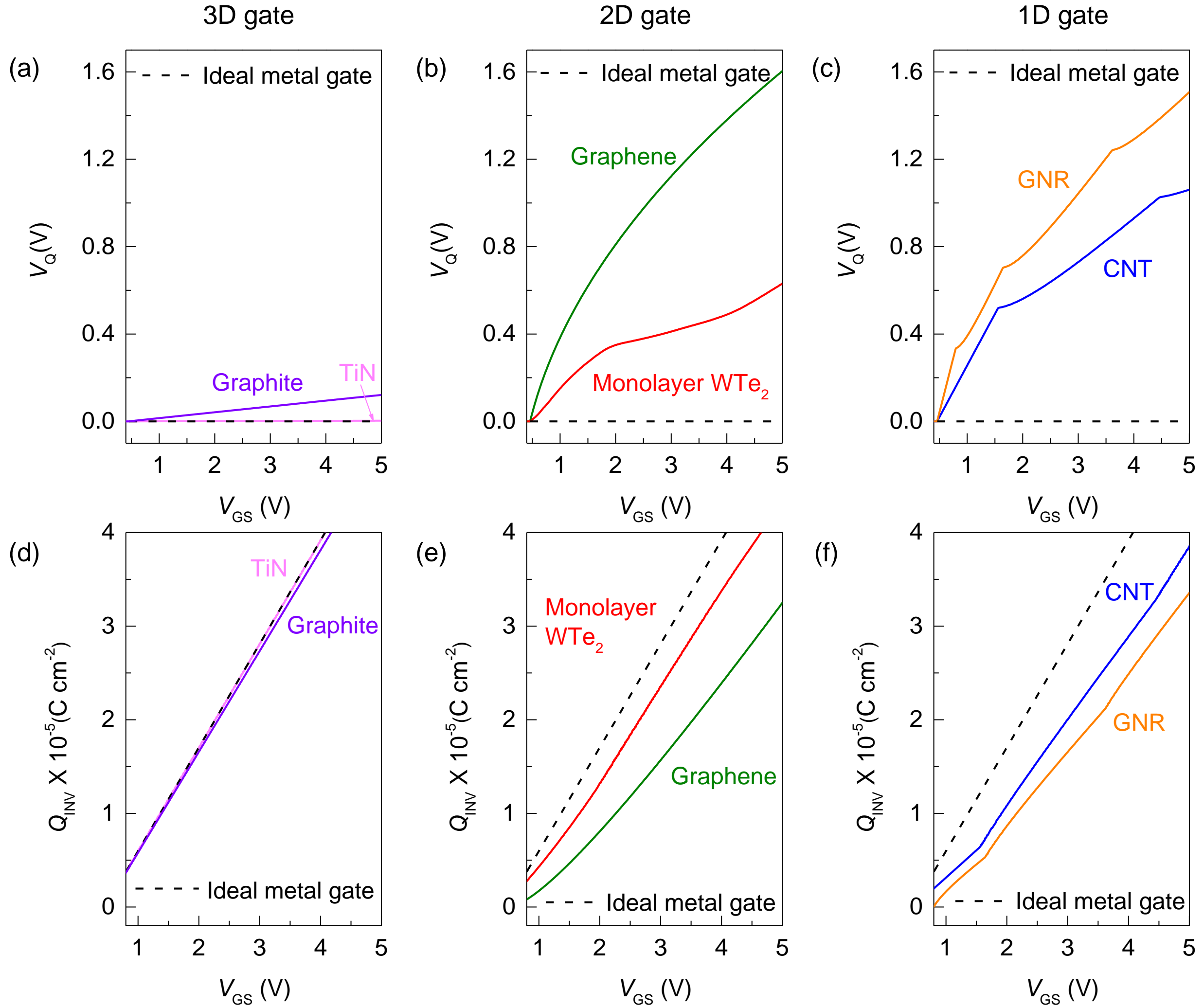


Figure 3: Electrostatic potential and charge calculations: (a-c) Electrostatic potential of the gate (V_Q) and (d-f) inversion charge density (Q_{INV}) versus V_{GS} for 3D, 2D and 1D gate electrode cases. 3D: 100 nm thick TiN and graphite, 2D: graphene and monolayer WTe_2, 1D: semiconducting GNR (n,m) = (15,0) and metallic CNT (n,m) = (18,18). All calculations at T = 10K. Dotted line indicates case for an ideal metal gate with infinite DOS.

3.3 Carbon nanotube gated ultra-thin silicon-on-insulator transistors

We experimentally demonstrate for the first time the effect of the gate C_Q on the I_DV_{GS} characteristics using an ultra-thin SOI channel (T_{SOI} ~ 2.5 – 3.5 nm, ~ 27.5 nm thick buried oxide (BOX) and ~ 3 nm thick Al_2O_3 top gate oxide) transistor with a single walled CNT top gate (G), silicon substrate bottom gate (B) and nickel silicide source (S) and drain (D) contacts. The device structure is illustrated schematically in figure 4a. Figure 4b shows the top view optical microscope image of a representative device showing the Ni S/D fingers, the SOI channel and the Pd contacts to the CNT gate and the Ni S/D fingers. The CNTs are perpendicular to the CNT catalyst line seen in figure 4b [6].

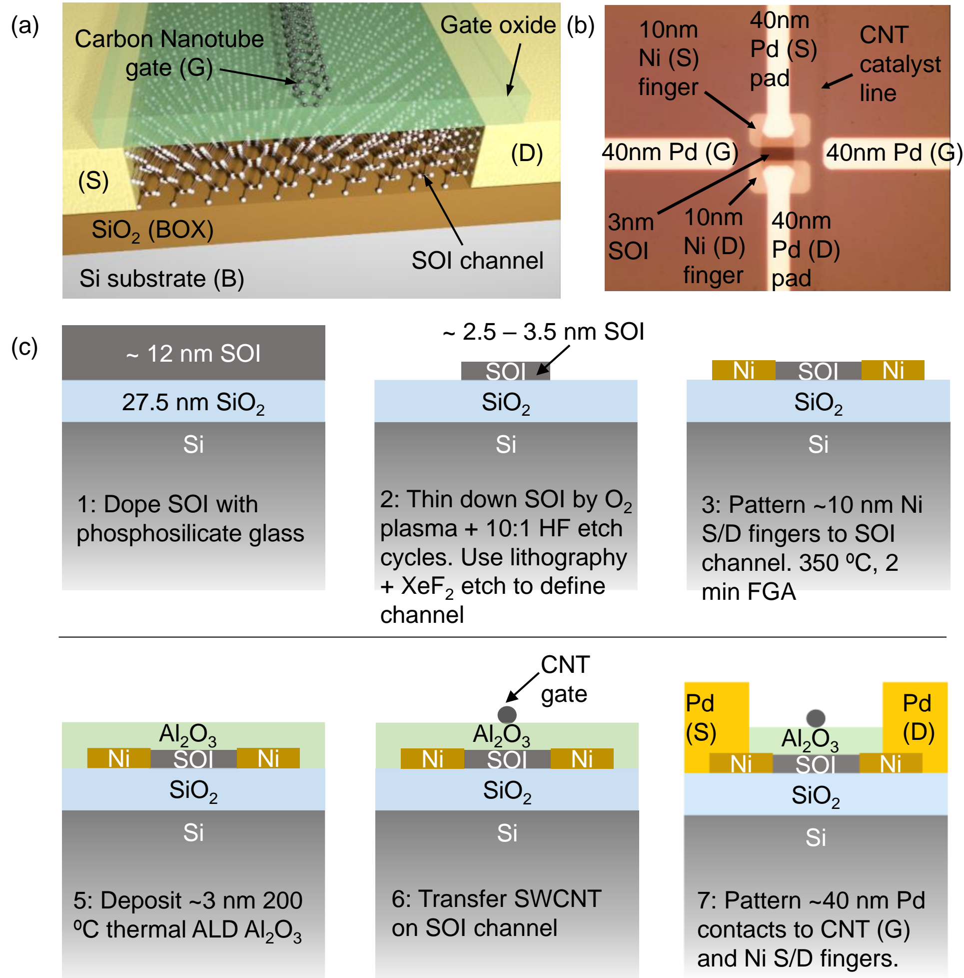


Figure 4: CNT gated SOI MOSFET device structure and process flow: (a) Schematic and (b) Optical microscope image of a representative device (top view). (c) Fabrication process flow

The fabrication process flow for the device is described in detail in figure 4c. The original SOI wafer has T_{SOI} ~ 12 nm which is heavily n-doped using phosphosilicate glass (PSG) (~ 5 × 19 cm^{-3} doping level) [21]. T_{SOI} is reduced using repeated cycles of O_2 plasma oxidation followed by etching of the oxide layer in 10:1 HF for 10 s [22]. A layer of SOI ~ 1.5 nm thick is removed for every cycle and T_{SOI} is monitored using ellipsometry, optical contrast and AFM measurements (figure S3). The impact of T_{SOI} on the $I_D V_{BS}$ characteristics is studied in figure S4. I_D reduces dramatically as T_{SOI} decreases because of increasing channel and contact resistance. Raised S/D in an optimized device design would reduce the contact resistance. For T_{SOI} > 3 nm, the bottom gate control is poor as evident from the low I_{ON}/I_{OFF} ratio in figure S4 indicating that the SOI layer is very heavily doped.

Once the SOI layer is of the desired thickness (T_{SOI} ~ 2.5 – 3.5 nm), the channel region is patterned using photolithography followed by XeF_2 vapor etch. 10 nm thick Ni S/D finger contacts to the channel are patterned using photolithography followed by thermal evaporation and metal liftoff. The devices are annealed at this stage in 5% forming gas for 2 minutes at 350 ºC to silicide

the contacts and reduce the contact resistance. Post silicidation, ~ 3 nm thick Al_2O_3 top gate oxide is deposited using thermal atomic layer deposition (ALD) at 200 ºC followed by the transfer of SWCNTs onto the devices [23]. Finally, ~ 40 nm thick Pd contacts are patterned to contact the CNTs as well as the Ni S/D fingers using photolithography followed by electron-beam evaporation and metal liftoff process. The rationale behind patterning the S/D contacts to the SOI in two steps using the 10 nm thick Ni S/D intermediary fingers is to minimize the topography height difference on the chip, which greatly impacts the yield of the CNT transfer step subsequently. All the details of the fabrication process flow are provided in the methods section.

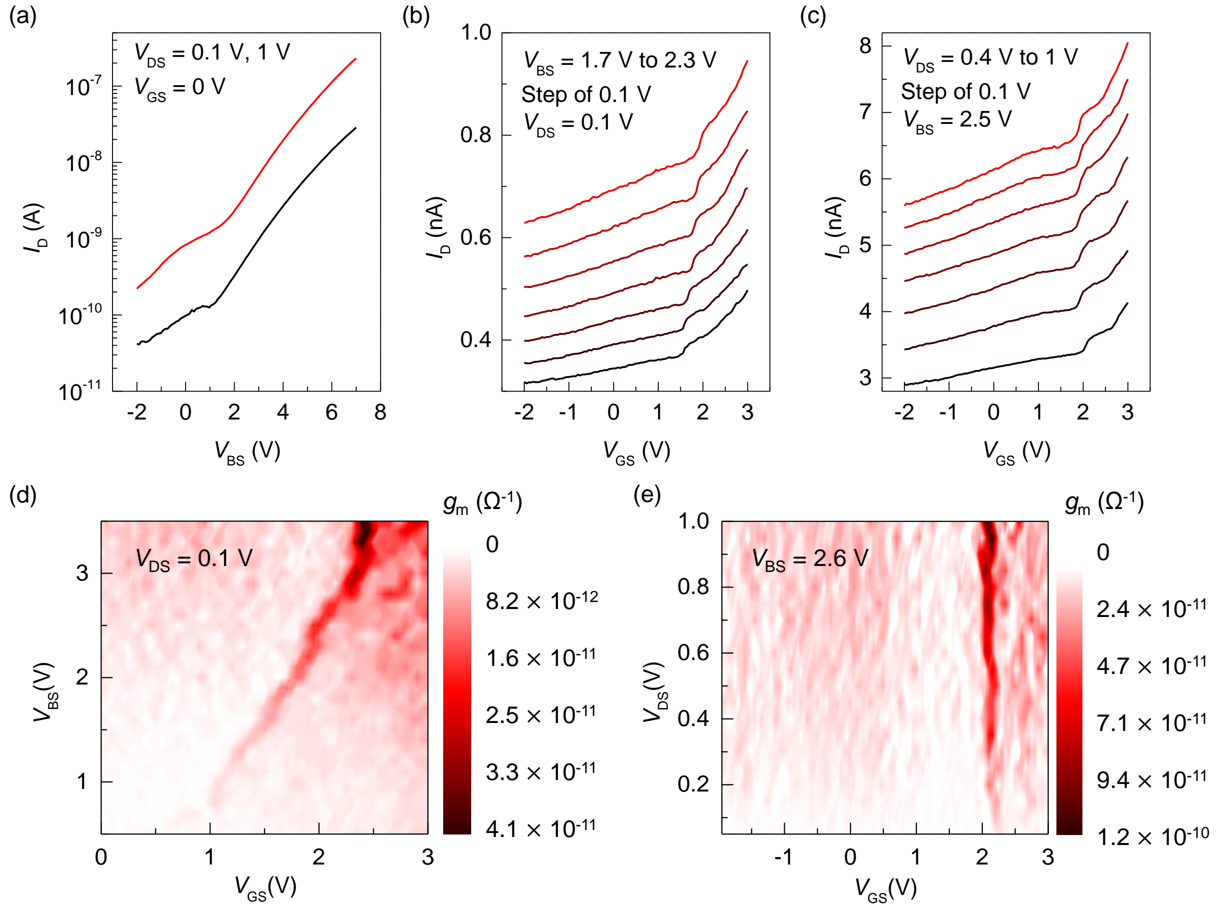


Figure 5: Electrical characteristics of CNT gated SOI MOSFET: (a) I_DV_{BS} (b-c) I_DV_{GS} for different V_{BS} and V_{DS} values respectively. g_m contour plots for (d) fixed V_{DS} and (e) fixed V_{BS} values respectively. Q_{CH} limited by Q_G due to finite DOS of CNT gate.

Figure 5 shows the electrical characteristics measured for the CNT gated SOI MOSFET described in figure 4. The I_DV_{BS} characteristics for a fixed V_{GS} are shown in figure 5a. Figures 5b and 5c show the I_DV_{GS} characteristics for fixed V_{DS} and V_{BS} respectively, which have the quantization signature resulting from the Van Hove singularities and finite DOS of the CNT gate as depicted in figure 3 and figure S2 [15]. The influence of the bottom gate on the transfer characteristics can be qualitatively understood using figure 5b. The quantization features in I_DV_{GS} correspond to the condition when the V_{GS} is large enough such that $E_{F,G}$ moves into the next higher

sub-band of the CNT. This results in the observed jump in Q_G or Q_{INV} corresponding to the Van Hove singularity at the quantized energy level for the CNT. As V_{BS} is increased Q_{CH} and ψ_s both increase and a larger V_{GS} is required to surpass the same Van Hove singularity. Thus the position of the quantization features shift right with increasing V_{BS} as seen in figure 5b. This dependence of the position of the quantum energy levels on V_{BS} and V_{GS} can be mapped using the g_m contour plot in figure 5d. V_{DS} does not alter the Q_{CH} and ψ_s significantly and hence does not affect the position of the quantization features as is evident from figure 5c and the g_m contour plot in figure 5e.

It is important to note that the quantization features in the $I_D V_{GS}$ characteristics are not because of the ultra-thin nature of the SOI channel. This can be understood from the lack of quantization features in the long-channel $I_D V_{BS}$ characteristics in figure 5a as well as the T_{SOI} dependent $I_D V_{BS}$ measurements in figure S4. Also all the measurements were performed at room temperature and the presence of distinct quantization features in $I_D V_{GS}$ can be explained by the low level of scattering induced distortion. This is because the carriers which are quantum confined in the gate are static and they impact I_D capacitively. The complete dataset for this device as well as electrical characteristics of other representative devices are provided in figures S5 – S7. The likely sources of hysteresis in the transfer characteristics shown in figures S5 – S7 are trapped charges in the ALD Al_2O_3 gate oxide and water molecules and contaminants on top of the CNT and the device which is unpassivated.

3.4 Conclusion

Thus we study the impact of gate C_Q on the electrical characteristics of nanoscale transistors using a bulk silicon MOSFET electrostatics model. For low-dimensional gates, Q_G limits Q_{CH}. We experimentally observe for the first time at room-temperature, gate DOS limited $I_D V_{GS}$ characteristics for an ultra-thin SOI channel transistor with a CNT gate. Further work would involve improving I_{ON} using raised S-D, and increasing the prominence of quantization features by using a high-k top gate oxide to increase C_{OX}.

With continued scaling of transistors it will be of increasing importance to consider the impact of gate C_Q on transistor characteristics and I_D. This effect should be independent of the device architecture (FinFET, Gate-all-around FET, etc.) and proper design of the gate and choice of the material will be important aspects in device design. By tailoring $g(E)$ in the gate, it would be possible to achieve desired transfer characteristics for the device. A specific example is the case of a 0D quantum dot gate on a 1D channel (figure S8). The δ-function gate DOS would result in step-like $I_D V_{GS}$ characteristics which can have potential applications like multi-state logic and memory [24]. Additionally, the reduced total gate capacitance ($C_G^{-1} = C_{OX}^{-1} + C_Q^{-1}$) would affect the dynamic response of the device and hence affect the circuit performance. Proposals involving the use of low dimensional materials for other applications like the S/D contacts and interconnects, [2, 4] must also be investigated similarly.

3.5 Methods

Device fabrication and characterization

The fabrication process starts with a silicon-on-insulator (SOI) wafer with ~ 12 nm thick SOI layer, ~ 27.5 nm thick buried oxide (BOX). Low-pressure chemical vapor deposition

(LPCVD) phosphosilicate glass (PSG) is deposited on the wafer at 450 ºC, using silane, oxygen and 25% phosphine (in a Tystar furnace) [21]. Subsequently, rapid thermal annealing (RTA) was carried out at 1000 ºC for 30 s to drive dopants into the SOI layer. RTA was repeated 3 more times (total RTA time = 120 s), each time the wafer was rotated by 90º. This was performed to ensure the dopant drive-in and activation was uniform across the wafer, and to offset any non-uniformities in the RTA chamber heat profile. The PSG layer is then completely etched away in 10:1 HF. From ellipsometry, the thickness of the SOI layer post *n*-doping is ~ 9 – 9.5 nm.

The SOI layer is then thinned down using repeated cycles of silicon oxidation followed by removal of the oxide layer. The SOI layer is oxidized using O_2 plasma at 120 W power for 5 minutes. The oxide is then etched using a 10:1 HF dip for 10 s. This constitutes a single cycle, and removes ~ 1.5 nm thick SOI layer at a time. The process is repeated until the SOI layer is thinned down close to ~ 3 nm. Piranha / UV based oxidation may also be used to thin down the SOI layer controllably since it forms a self-limiting oxide layer ~ 1 nm thick similar to the O2 plasma method [22].

i-line photolithography process is used to pattern the SOI channel regions for the ~ 3 nm thick SOI layer. XeF_2 based etching (using Xactix system) is used to etch the unmasked SOI regions and form the channel. The XeF_2 and N_2 pressures were set at 1 Torr and 7 Torr respectively, each etch cycle was 8 s long and 3 cycles were used. XeF_2 is highly selective against SiO_2, and this was the primary reason for selecting it as an etchant for the SOI channel step, because the BOX is relatively thin to start with. Post resist-removal, another photolithography step using a bilayer liftoff resist / i-line process is used to pattern the S/D fingers. Ni (10 nm) was deposited using thermal evaporation, and the contact finger regions were stripped of any native oxide in 50:1 HF for 25 s, immediately prior to loading the samples for evaporation. Post evaporation and metal liftoff in PG remover at 80 ºC for 30 min, the samples were annealed in 5% forming gas at 350 ºC for 2 minutes to form nickel silicide at the S/D finger regions and obtain good quality contacts to the SOI layer.

Al_2O_3 (~ 3 nm thick) is deposited on top of the device at 200 ºC using thermal ALD (Cambridge Fiji F200 system) based on TMA (Tri-methyl aluminum) and H_2O process. Single walled aligned carbon nanotubes (CNTs) (density of CNTs is ~ 1 – 3 CNTs per 5 µm) are then transferred on top of the device with the CNTs along the direction perpendicular to the SOI channel direction as described in the process details in reference [6, 23]. Finally, using bilayer resist photolithography, G contacts are patterned to the carbon nanotubes, and at the same time, pads to the Ni S/D fingers are also patterned. The sample is overdeveloped in the TMAH developer during this step in order to ensure that the ALD Al_2O_3 which is on top of the S/D fingers is completely etched away by the TMAH, ensuring that a good contact can be formed between the S/D fingers and the S/D pads. Finally, 30 nm Pd is evaporated on the samples using electron beam evaporation, followed by metal liftoff in PG Remover at 80 ºC for 30 min to complete the device fabrication. The devices are characterized inside a Lakeshore vacuum probe station, at a pressure of ~ 1×10^{-5} mbar, using a B1500A / 4155C semiconductor parameter analyzer.

Electrostatic modeling and extraction of Q_{INV}

Q_{INV} is extracted from Q_G using equation 4. Q_G is obtained by solving equations 1 – 3. The units of C_Q are F cm^{-1}, F cm^{-2} and F cm^{-3} for 1D, 2D and 3D gates respectively. Q_{INV} and Q_G

are charge densities per unit area. Hence for the case of 1D gates we use, $C_Q' = C_Q/L$ where, L is the length of the GNR or the diameter of the CNT. Similarly, for the case of 3D gates we use $C_Q' = C_Q*h$, where h is the thickness of the gate. For the examples considered in this work, L = 1.7217 nm for the GNR ((n,m) = (15,0)) and L = 2.4408 nm for the CNT ((n,m) = (18,18)) and h = 100 nm for the graphite and TiN 3D gates. V_{midgap} = 4.56 V (corresponding to the intrinsic work function of graphene) was assumed for all the materials in the calculations [12, 17, 25]. V_T = 4.56 V was also assumed when calculating Q_{INV} for an ideal MOSFET in figure 3. A different value of V_{midgap} would simply result in a lateral shift in the calculated plots in figure 3. Modified equations of bulk silicon properties were used in the calculations to account for the dependence on temperature [26].

$$N_C = 6.2 \times 10^{15} \times T^{3/2}\, cm^{-3}$$

$$N_V = 3.5 \times 10^{15} \times T^{3/2}\, cm^{-3}$$

$$E_{G,Si} = 1.17 - \frac{4.73 \times 10^{-4}\, T^2}{T + 636}\, eV$$

$$N_A^- = \sqrt{\frac{N_V N_A}{2}}\, e^{-\frac{E_A}{kT}}$$

Here N_A is the doping of bulk silicon, E_A corresponds to the Boron dopant activation energy in silicon which is 0.045 eV [27]. For all calculations, we assume $N_A = 10^{13}$ cm^{-3}, T_{OX} = 2 nm and dielectric constant of high-k oxide k_{OX} = 25.

3.6 Supporting Information

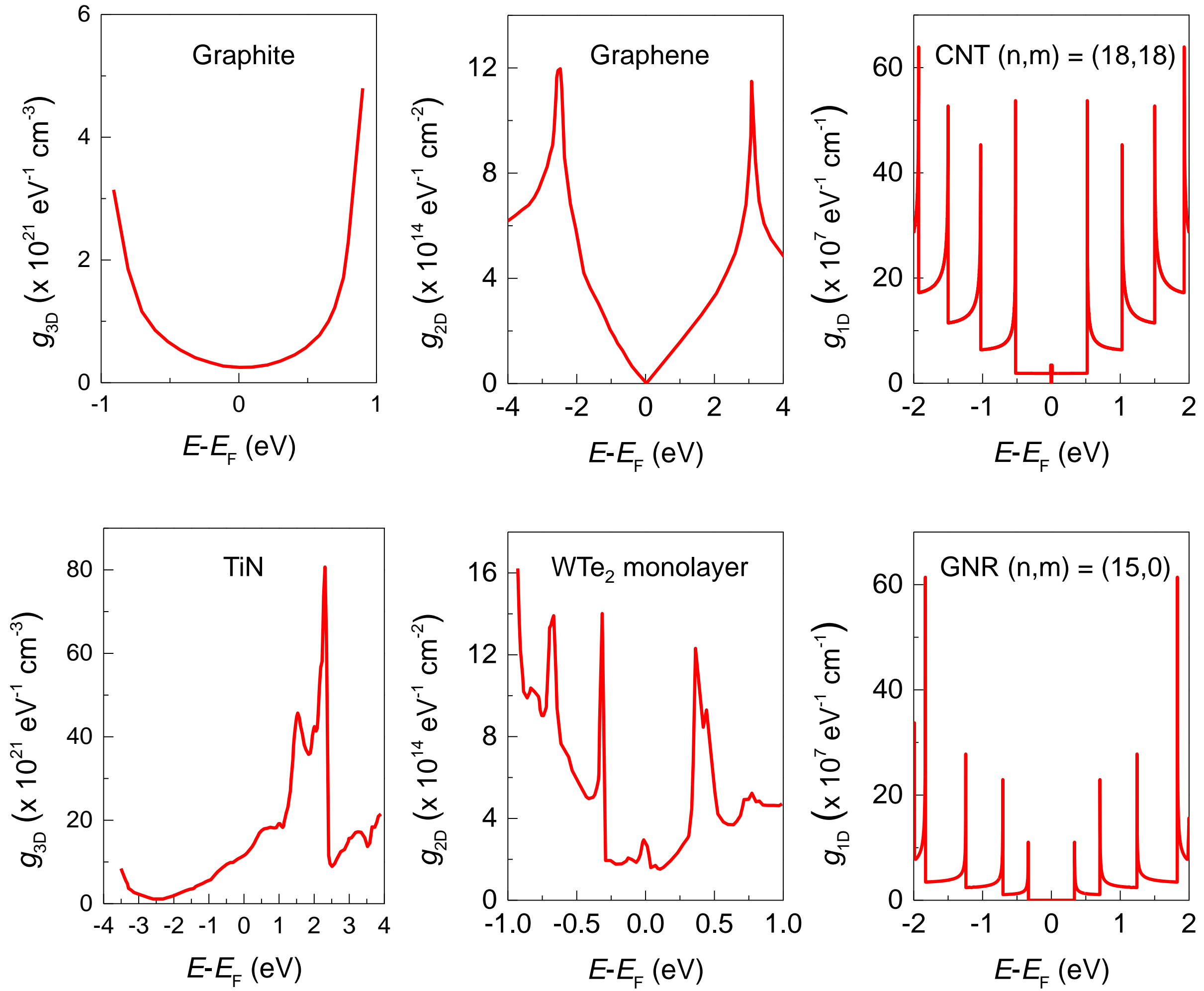


Figure S1: Density of states for different materials used in the calculations for figure 3. 3D: TiN and graphite (h = 100 nm thick gates); 2D: graphene and monolayer WTe_2; 1D: CNT and GNR gates

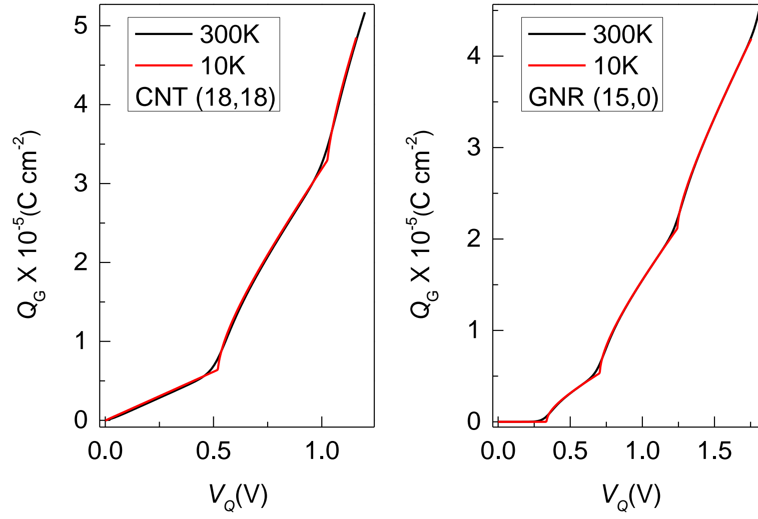
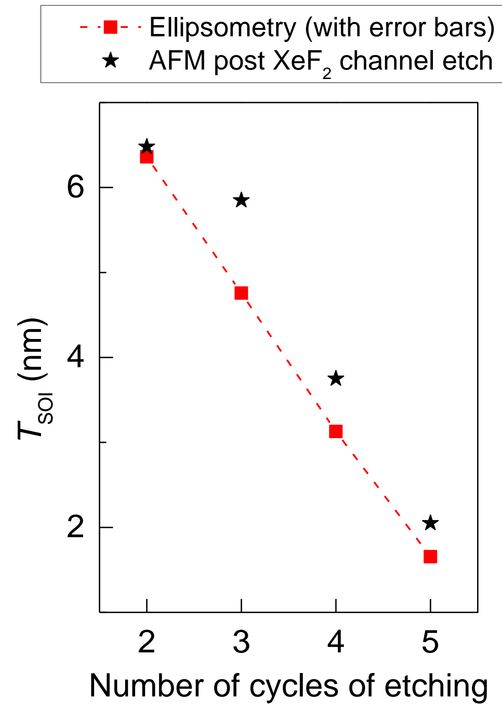


Figure S2: Gate charge Q_G as a function of the electrostatic potential of the gate (V_Q) at T = 10 K and 300 K for CNT and GNR gate electrodes



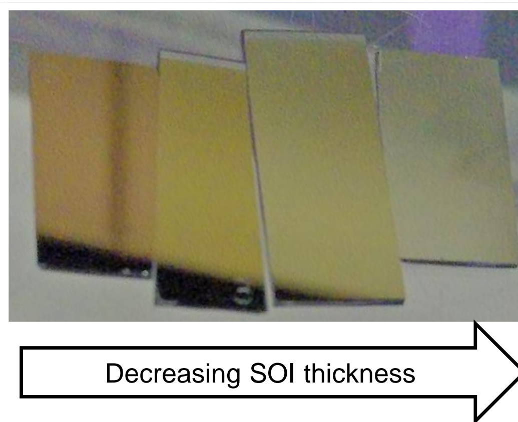


Figure S3: Monitoring the thickness of SOI layer as a function of number of etch cycles using ellipsometry, atomic force microscopy (AFM) (post etching of channel using XeF_2) and optical contrast (camera image). Ellipsometry measurements have an error bar calculated from 3 measurements conducted on different parts of the sample. The AFM measured values are slightly higher since the XeF_2 etch is not 100% selective against SiO_2 and thus the total height from AFM equals T_{SOI} + thickness of etched SiO_2 which is typically ~ 0.5 nm. T_{SOI} reduces by ~ 1.5 nm every etching cycle

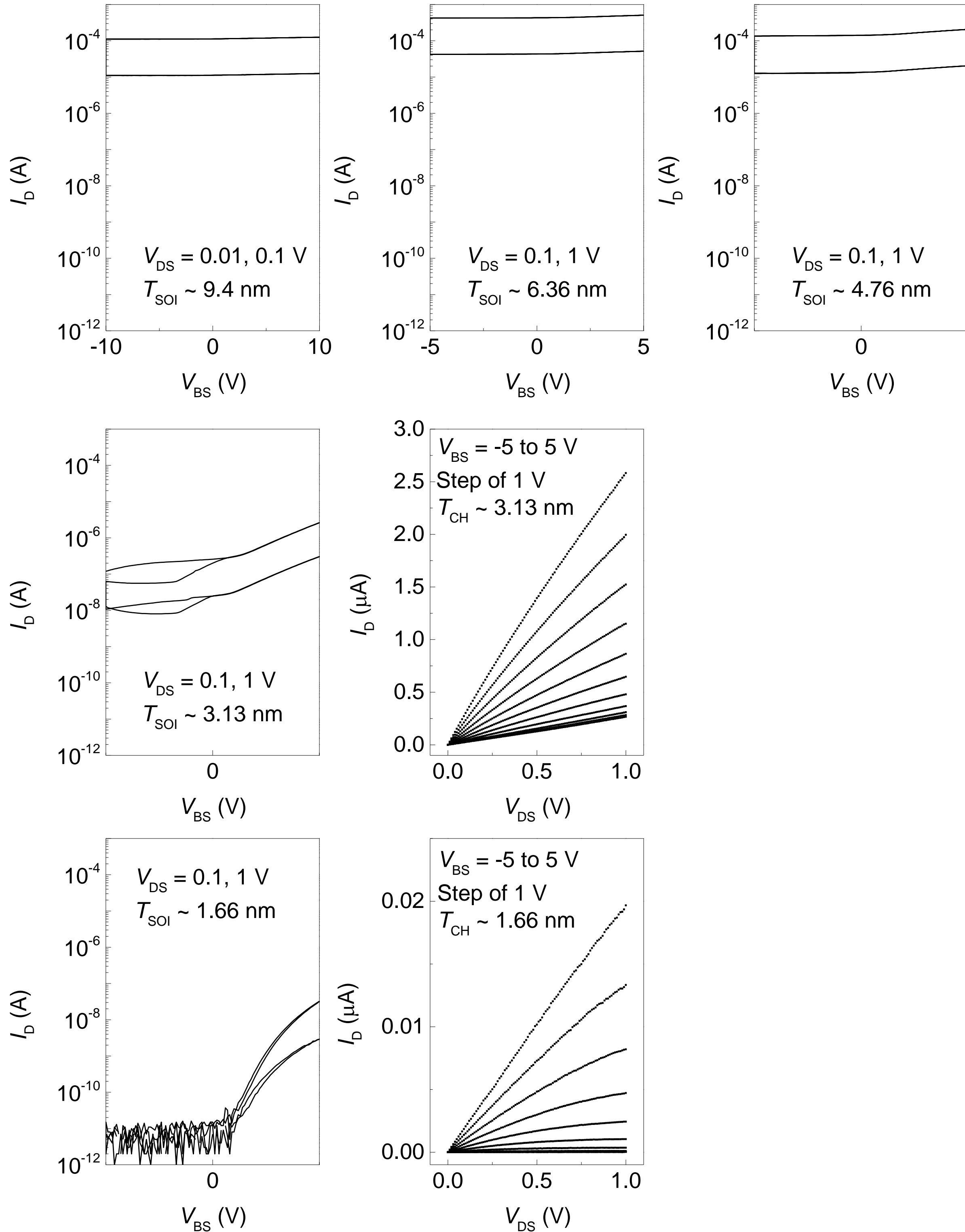


Figure S4: $I_D V_{BS}$ characteristics for different values of T_{SOI}. $I_D V_{DS}$ characteristics are also shown for T_{SOI} = 1.66 nm and 3.13 nm.

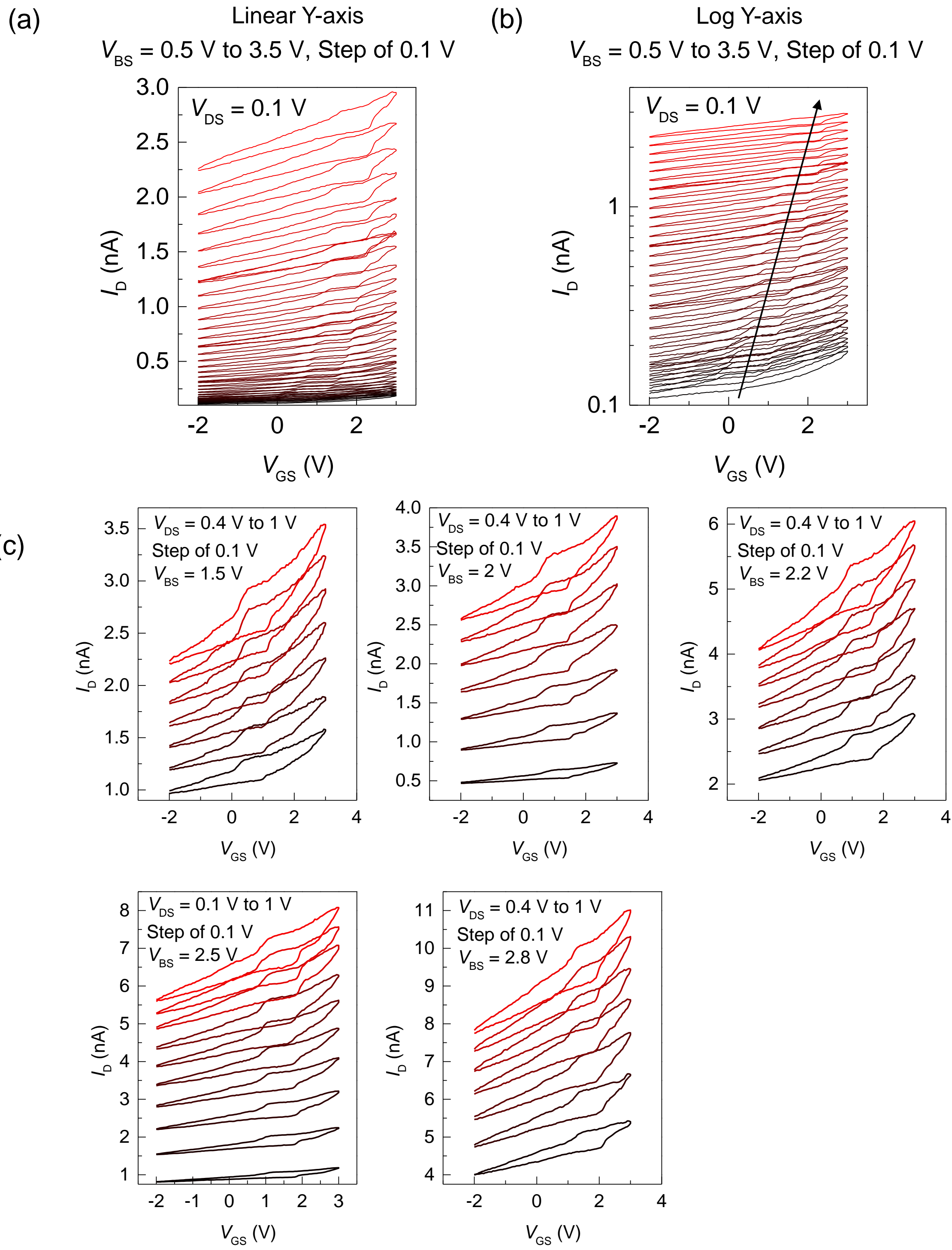


Figure S5: (Other data for device in figure 5) $I_D V_{GS}$ characteristics at fixed V_{DS} and varying V_{BS} plotted on the (a) linear and (b) log y-axis scale showing the right shift of the quantization features with increasing V_{BS}. (c) $I_D V_{GS}$ characteristics keeping V_{BS} fixed, and stepping the V_{DS} voltage.

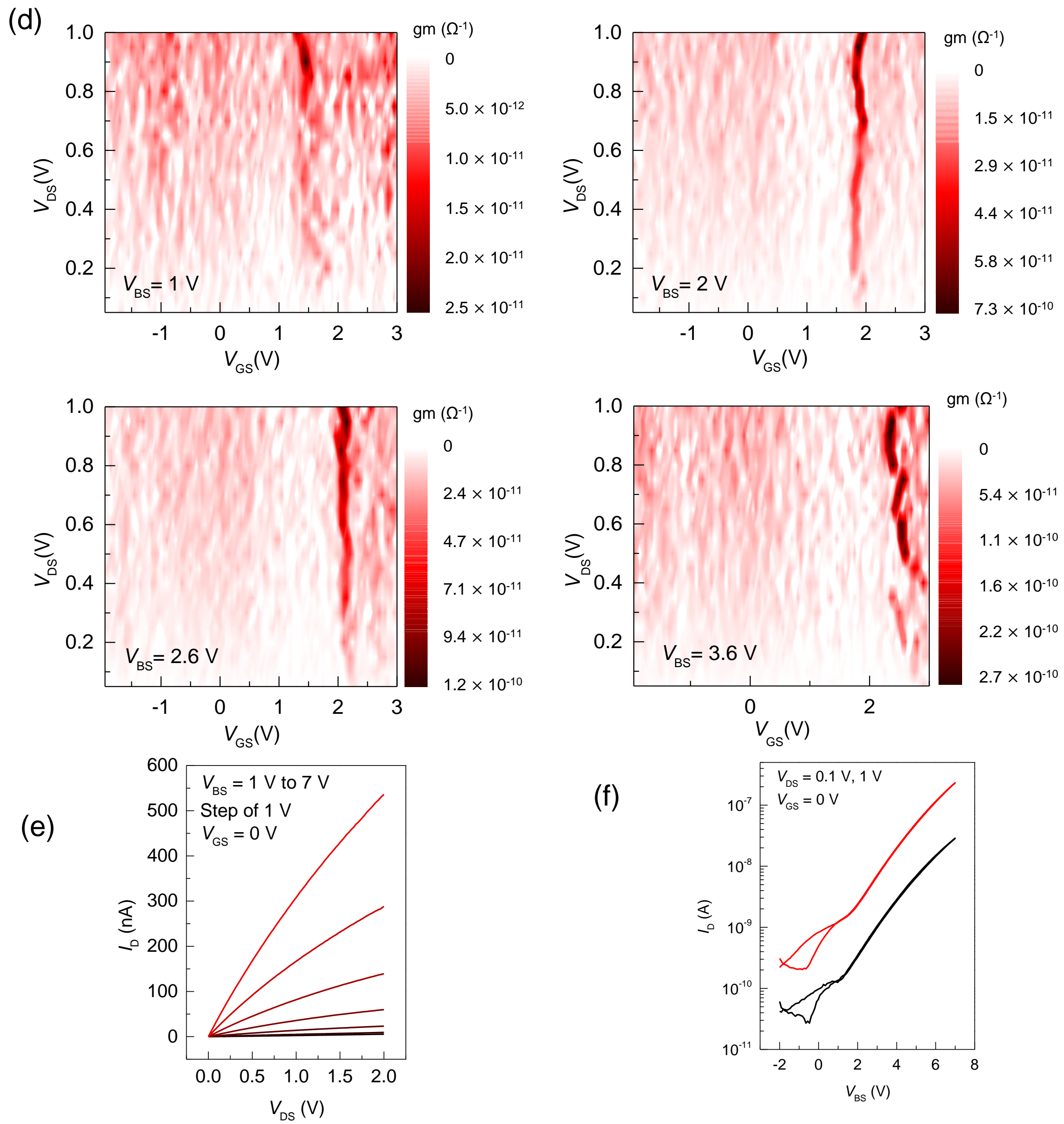


Figure S5 (continued): (Other data for device in figure 5) (d) g_m contour maps as a function of V_{DS} and V_{GS} for a fixed V_{BS}. (e) $I_D V_{DS}$ characteristics for different values of V_{BS} keeping V_{GS} fixed. (f) $I_D V_{BS}$ characteristics for different values of V_{DS} keeping V_{GS} fixed

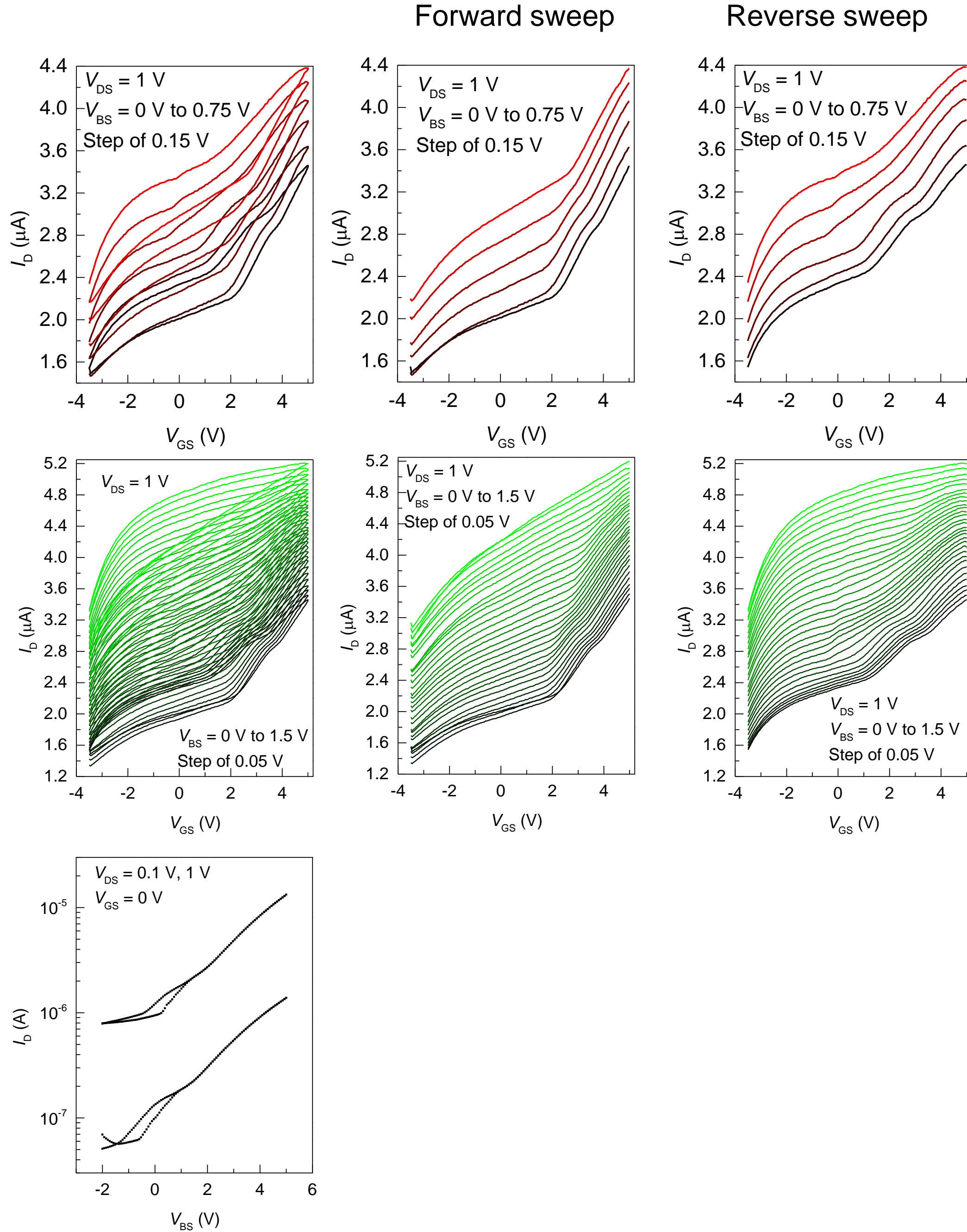


Figure S6: Device data for device 2. I_DV_{GS} characteristics at fixed V_{DS} and varying V_{BS} for both sweep directions, and the I_DV_{BS} characteristics at fixed V_{GS}. Differences in transfer characteristics arise from differences in chirality of CNT gate, varying T_{SOI}, C_{OX} and other similar parameters affected by batch-to-batch process variations.

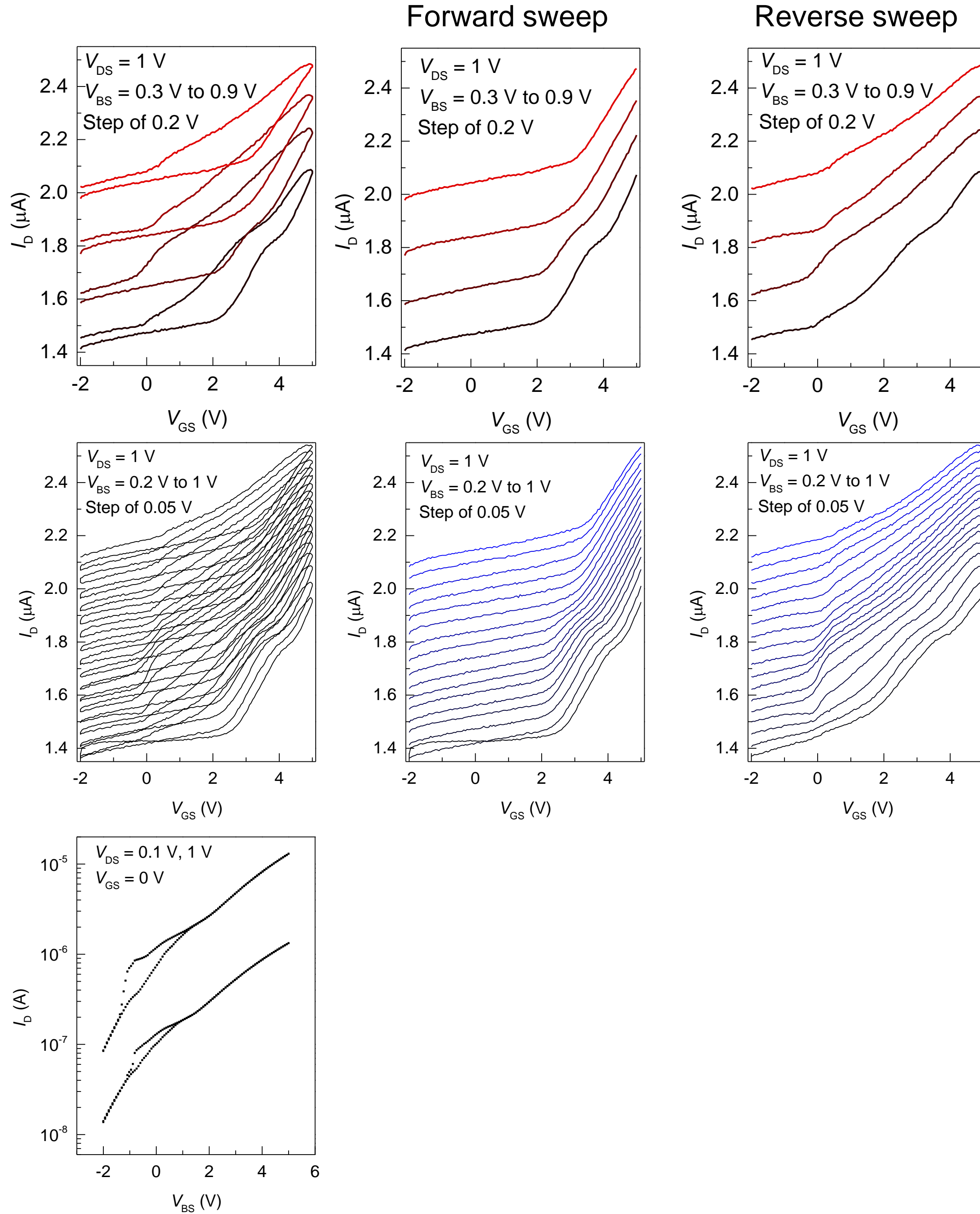
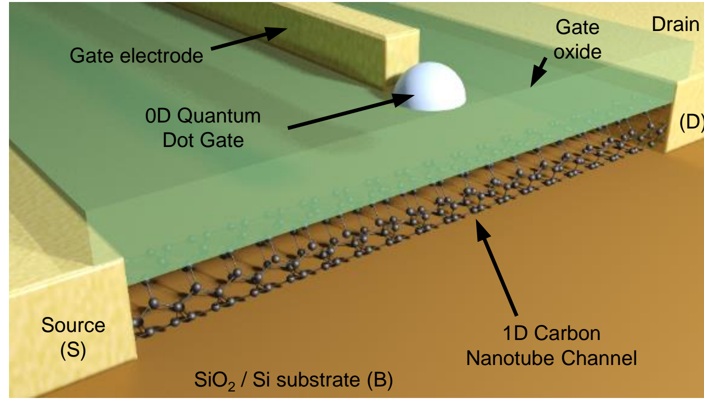


Figure S7: Device data for device 3. I_DV_{GS} characteristics at fixed V_{DS} and varying V_{BS} for both sweep directions, and the I_DV_{BS} characteristics at fixed V_{GS}. Differences in transfer characteristics arise from differences in chirality of CNT gate, varying T_{SOI}, C_{OX} and other similar parameters affected by batch-to-batch process variations.



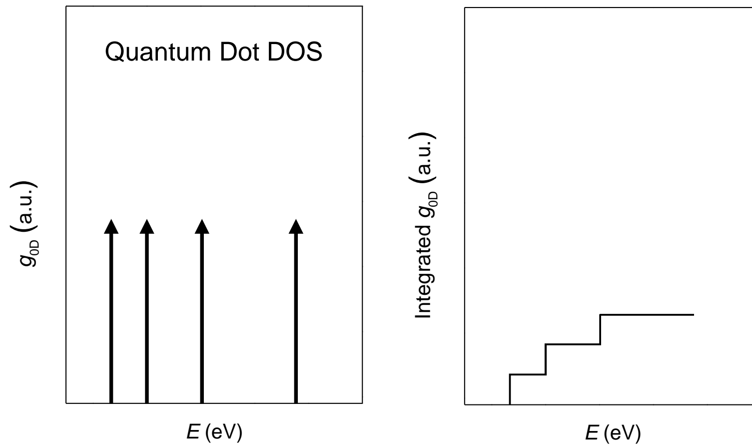


Figure S8: Schematic for a conceptual device with a 0D quantum dot gate with a 1D CNT channel. The gate DOS is limited and consists of δ-functions corresponding to each quantized energy level. The C_Q and Q_{INV} in the channel will have a step like dependence on V_{GS} corresponding to the integrated DOS shown in the figure. This device structure can have potential applications in multi-level logic or memory.

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4

[4]Strain Induced Indirect to Direct Bandgap Transition in Few-Layer WSe_2

4.1 Introduction

Transition metal dichalcogenides (TMDCs) are a class of materials consisting of transition metals M-(Mo, W, Sn, etc.) covalently bonded to chalcogens X-(S, Se, Te) which arrange in stacked layers held together by Van der Waals forces. Due to their layered structure and sizable bandgaps, semiconducting TMDCs such as MoS_2 and WSe_2 have established themselves as strong candidates for future electronic and optoelectronic applications [1-8]. It has been shown that monolayer MoS_2 and WSe_2 exhibit a direct bandgap (K-K) with strong photoluminescence (PL) [9-11]. For example, monolayer MoS_2 has a high PL quantum yield on the order of ~ 4×10^{-3} (ref. 9), and monolayer WSe_2 is found to exhibit greater PL intensity than MoS_2 (ref. 11). However, multilayers of these TMDCs have an indirect bandgap and show significantly weaker PL [9, 11, 12]. The indirect nature of multilayer TDMCs therefore limits their application in optoelectronic devices such as light-emitting diodes, photodetectors and lasers.

Strain can be used to modulate the band structure and engineer the properties of a material. Specifically, the lattice constant and van der Waals gap for TMDCs change by strain. This leads to a direct change in the electronic band structure and hence the energies of the conduction band (CB) minima and valence band (VB) maxima for the material. If the energy difference of the indirect and direct bandgaps is small, then it may be possible to achieve a crossover from one to the other using strain. For example, Ge shows an indirect to direct bandgap transition when strained due to the small difference of its two energy bandgaps [13, 14]. The effect of strain on TMDCs has been studied for MoS_2 as a model TMDC material [15]. However for MoS_2 multilayers, the direct and indirect bandgap differ by a large value (i.e., ~300 meV for bilayer MoS_2) [9] and hence no transition is seen on the application of up to 2.2% uniaxial tensile strain [15]. In contrast to MoS_2, WSe_2 multilayers have a much smaller difference between the direct and indirect bandgaps, on the order of 40 meV for bilayer WSe_2[16]. Thus, a crossover from indirect to direct bandgap should be possible in multilayer WSe_2 for practically achievable strain values, similar to the case of Ge. However, to date, strain engineering of WSe_2 multilayers has not been explored, and this unique property of WSe_2 has not been exploited.

In this work, we experimentally demonstrate a drastic increase in PL intensity for multilayer WSe_2 (2-4 layers thick) by applying uniaxial tensile strain of up to ~ 2%. The maximum PL amplification observed at this strain for bilayer WSe_2 is ~ 35×. The PL intensity of strained bilayer WSe_2 is comparable to that of an unstrained WSe_2 monolayer measured under similar experimental conditions. A significant PL intensity increase is also detected for trilayer and

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quadlayer WSe_2 upon uniaxial strain. Density functional theory (DFT) calculations further confirm a strain-induced indirect to direct transition in multilayer WSe_2, due to opposite shifts of the CB minima at the K and Σ points in the reciprocal space, explaining the PL emission enhancement observed in the experiment.

4.2 Uniaxial tensile strain in bilayer WSe_2

A two-point bending method is used to apply uniaxial tensile strain to the WSe_2 flakes, as illustrated in Fig. 1a. WSe_2 is first exfoliated onto a Si/SiO_2 (260 nm thick) substrate which is mapped using an optical microscope [17, 18] (and atomic force microscope) to find flakes with the desired number of layers (1-4). Each flake is then transferred to a clear and flexible polyethylene terephthalate glycol-modified (PETG) substrate of 1.5 mm thickness using poly methyl methacrylate (PMMA) as the transfer medium [19]. The PMMA caps the flake on the PETG and acts as a clamp thus enabling the application of large strain. The bent PETG is approximated by a circular arc for calculation of strain which can be computed as shown in Fig. 1a (more details on the sample preparation and strain calculation can be found in the supporting information (SI)).

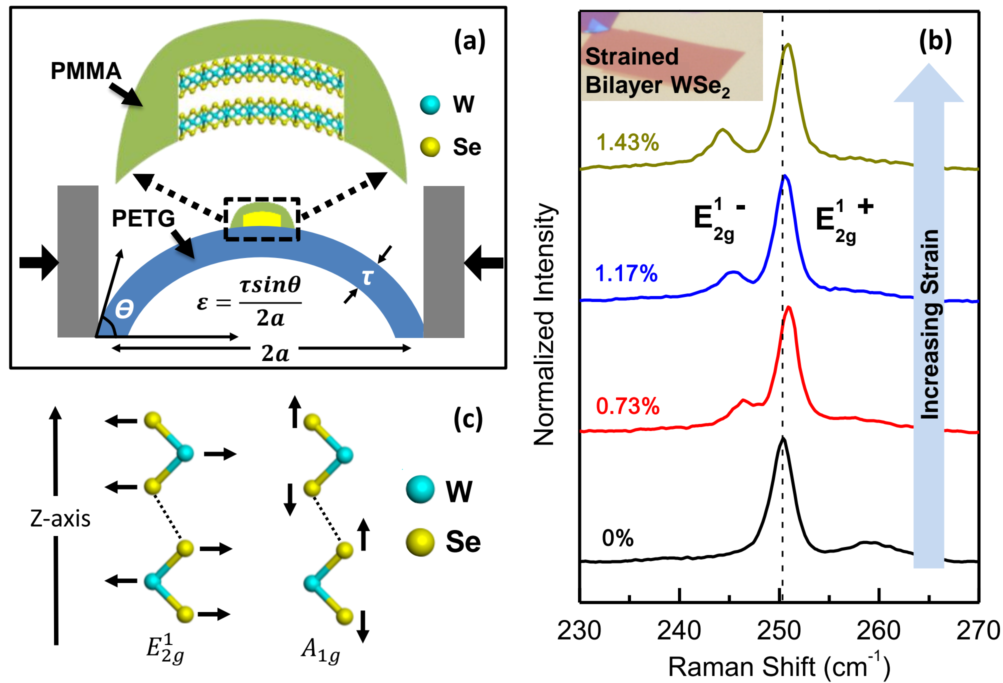

Figure 1: (a) Schematic of the two-point bending apparatus along with the method to compute strain. WSe_2 flake encapsulated by PMMA is transferred onto flexible PETG. τ is the thickness of the PETG, ε is the strain, Θ is the angle of the tangent at the minimum strain point and 2a is the separation of the bent PETG. (b) Raman spectra for bilayer WSe_2 at different strain. E^1_{2g} degeneracy breaks under strain and the mode splits into E^{1-}_{2g} and E^{1+}_{2g} which show a left and right shift from the original Raman peak. Inset shows the optical microscope image of the bilayer WSe_2 flake used in this study. (c) The schematic of E^1_{2g} and A_{1g} Raman active modes of WSe_2.

In addition to the WSe_2 flake of interest, a MoS_2 monolayer is also transferred onto the same PETG in close proximity to the WSe_2 flake. This MoS_2 monolayer serves as an internal reference for predicting strain using data in reference 15, in addition to calculating strain from the bending geometry. Fig. S1a and Fig. S1b show the evolution of the PL and Raman data for the monolayer MoS_2 reference with strain. The strain predicted using this reference sample shows an almost 1:1 correlation with the calculated strain from the bending geometry as is shown in Fig. S1c. Raman and PL measurements (Horiba Scientific LabRAM HR 800) were taken for strained WSe_2 at several representative spots with site-to-site variation arising from local strain profile of the flakes (see SI, Fig. S2). A 532 nm laser with 8-80 µW power and a spot size of ~0.5µm was used. The lowest laser power giving appreciable signal-to-noise ratio (SNR) is used in order to prevent damage to the TMDC flakes, while making sure that the Raman and PL peaks do not shift due to heating effects in the sample.

4.3 Raman spectroscopy and photoluminescence enhancement

Fig. 1b shows the Raman spectra for bilayer WSe_2 under different uniaxial tensile strain up to ~ 1.43%. The atomic vibrations corresponding to the E^1_{2g} (in-plane) and A_{1g} (out-of-plane) Raman modes for WSe_2 are shown in Fig. 1c [16, 20]. Under application of strain, the degeneracy of the E^1_{2g} mode is broken and the peak splits into two peaks, E^{1+}_{2g} and E^{1-}_{2g}. The two peaks move in opposite directions from the original peak, with E^{1-}_{2g} left shifting by a large amount compared to the E^{1+}_{2g} peak which shows a right shift. Raman shift is an indicator of the amount by which the lattice constant is changed. Also a left shift indicates tensile strain or increase in the lattice constant whereas a right shift indicates compressive strain or a reduction in the lattice constant. Thus E^{1-}_{2g} and E^{1+}_{2g} correspond to the vibrational modes parallel and perpendicular to the direction of strain. The peak splitting increases as strain is increased. Thus Raman splitting and shift are clear indicators of strain application on the sample.

Fig. 2a depicts the evolution of the bilayer WSe_2 PL with strain. A drastic enhancement in PL intensity for bilayer WSe_2 is clearly seen as the uniaxial tensile strain is increased. The peak at no strain is broad and the PL peak intensity is more than an order of magnitude less than that for unstrained monolayer WSe_2 which is also shown in Fig. 2a for reference. As strain increases, a second peak at higher energy corresponding to the direct valley transition (K_C-K_V) appears (In the notation K_C, Σ_V, etc., the subscript C and V represent the CB minima and VB maxima of the electronic band structure respectively with the corresponding position in the reciprocal space given by K, Σ, Γ, etc. Refer to SI Fig. S3 for more information). This peak shows a red shift with increasing strain and at the same time the PL intensity increases significantly. Simultaneously, we also observe the peak corresponding to the indirect valley transition (Σ_C-K_V) showing a small blue shift. At ~ 1.5% strain, the bilayer PL intensity is amplified by ~25×. The full width half maximum (FWHM) also decreases from 110 meV at 0% strain to 62 meV at 1.5% strain which is comparable to the FWHM for unstrained monolayer WSe_2 (61.6 meV) . The PL signal from the strained bilayer WSe_2 is comparable to that from the unstrained monolayer WSe_2 measured under identical laser power and acquisition time conditions.

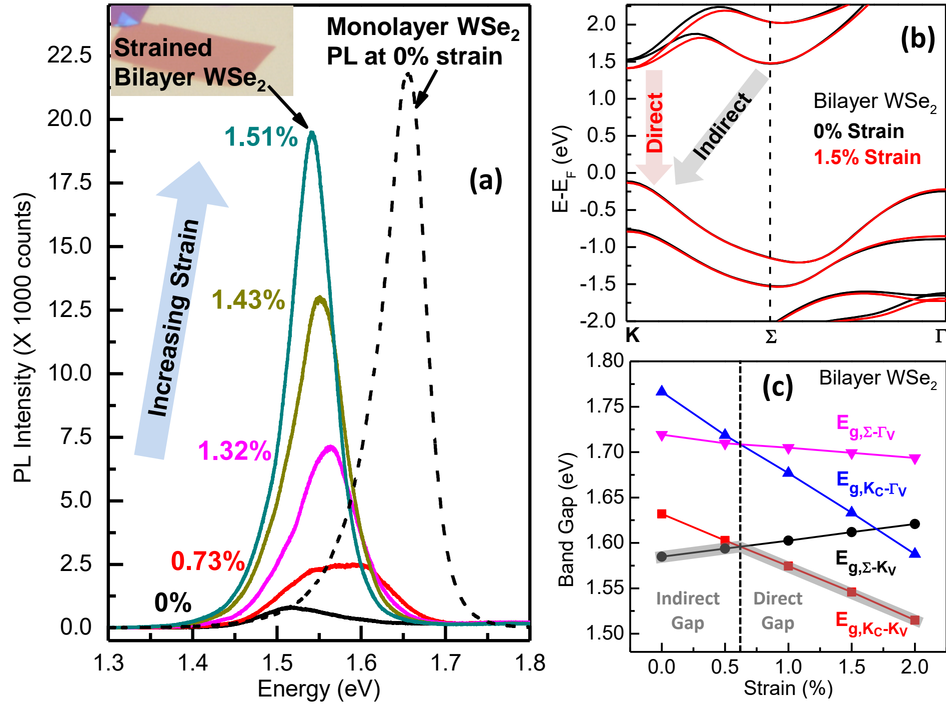

Figure 2: (a) Bilayer WSe_2 PL spectra at different strain. PL of unstrained monolayer WSe_2 on SiO_2 is shown for comparison. Inset shows the optical microscope image of the bilayer WSe_2 flake used in this study. (b) Electronic band structure for bilayer WSe_2 with and without strain using HSE-DFT. CB and VB changes under strain are clearly seen with the K point CB minima decreasing drastically in energy whereas the Σ point CB minima increases slightly; thus showing the indirect to direct bandgap transition. (c) Bandgap energies for different transitions of bilayer WSe_2 calculated using HSE-DFT.

4.4 Density functional theory calculations

The drastic increase in the PL intensity and reduction of FWHM for bilayer WSe_2 under strain can be understood with the help of DFT calculations. In this study DFT calculations were performed using the projector-augmented wave (PAW) pseudo-potential through the Vienna Ab-initio simulation package (VASP) [21] [22]. For the atomic structural relaxation, generalized gradient approximation (GGA) method was used with Perdew–Burke–Ernzerhof (PBE) exchange-correlation functional [23]. The Brillouin-zone sampling was done by the 9×9×1 Monkhorst-Pack scheme. It is well-known that the DFT calculation within GGA underestimates the bandgap of a semiconductor, thus, to obtain more accurate E-*k* relation, Heyd-Scuseria-Ernzerhof (HSE) exchange correlation potential with spin orbit coupling was used to model the band structure with increased k-point sampling of 15×15×1 (ref. 24). HSE gives a larger bandgap than LDA and GGA simulations, but a smaller bandgap than GW calculations. It has also been indicated that the optical gap is related to the GW bandgap subtracting the exciton binding energy. To verify, GW quasi-particle (QP) calculation, non-self-consistent G_0W_0 was also performed (details can be found in the SI Fig. S7) [25]. The band-structure by the G_0W_0 calculations has an approximately *k*-independent shift of the conduction bands with regard to the valence bands (0.65 eV increase between K_C-K_V), without changing the direct or indirect bandgap feature (see Fig. S7), similar to what has been shown before with or without strain [26]. The GW bandgap is larger than HSE

bandgaps. An exciton binding energy of about 1eV has been reported for monolayer dichalcogenide materials, but with uncertainty. The value varies by about a factor of two if different *k* point grids are used in simulation [26], and it decreases by about a factor of two from monolayer to bilayer [27]. It is also dependent on the surrounding electrostatic environment. The uncertainty of the exciton binding energy makes a comparison to experiment difficult. On the other hand, it is found that the PL peak energy agrees with the bandgap of the HSE calculation. This is a coincidence, which could be due to cancellation of the blue shift by GW correction and red shift by exciton binding. Nevertheless, instead of introduce fitting parameters for uncertainty of the exciton binding energy, the band-structures from the HSE calculations with spin orbit coupling (SOC) are presented next, since we are mainly interested in the indirect to direct bandgap transitions with strain applied. Structure relaxation was first performed to determine the relaxed atomistic structure in the presence of uniaxial strain, and the band structure in the presence of strain was subsequently calculated.

Fig. 2b compares the electronic band structure for bilayer WSe_2 at 0% and 1.5% uniaxial tensile strain calculated within DFT using the HSE exchange-correlation functional. Inspection of Fig. 2b reveals that 1.5% strain lowers the energy of the CB minima at the (six-fold degenerate) K points by 86 meV resulting in a transition from indirect to direct bandgap. The energy of the CB minima at the Σ points interestingly shows an increase of 27 meV at 1.5% strain. The transition from indirect to direct bandgap predicted by DFT thus qualitatively explains the 25× increase in PL intensity observed experimentally at ~ 1.5% strain (Fig. 2a).

The CB minima at the K points of WSe_2 exhibit dominant W d_{Z^2} orbital character (refer to SI Fig. S4). Under strain, the interlayer W-W distance changes and hence the orbital overlap. As a result, the energy of the CB minima at the K-points changes by a large amount leading to a crossover from indirect to direct bandgap. The different bandgap energies as calculated using DFT are compiled in Fig. 2c. The transition from indirect to direct bandgap is predicted to happen at ~ 0.625% strain. Experimentally the transition is observed at a higher strain value, however, the trend predicted by DFT is consistent with the experimental data. This discrepancy between DFT and the experimental data can be attributed to the underestimation of bandgap from DFT calculations or from a difference between applied and actual strain due to local strain effects as discussed in Fig. S2.

4.5 Photoluminescence amplification factor model

To understand the PL intensity amplification quantitatively, the electron occupancy at the direct CB valleys at the K-points must be considered. Fig. 3a schematically illustrates the occupancy of the CB and the VB under laser illumination. The Fermi level splits into quasi-Fermi levels for electrons, F_n and holes, F_p respectively. Tensile strain changes the CB minima, with the direct CB valleys K_C moving down while the indirect CB valleys Σ_C moving up in energy. The occupancy of electrons in each valley therefore correspondingly changes with strain.

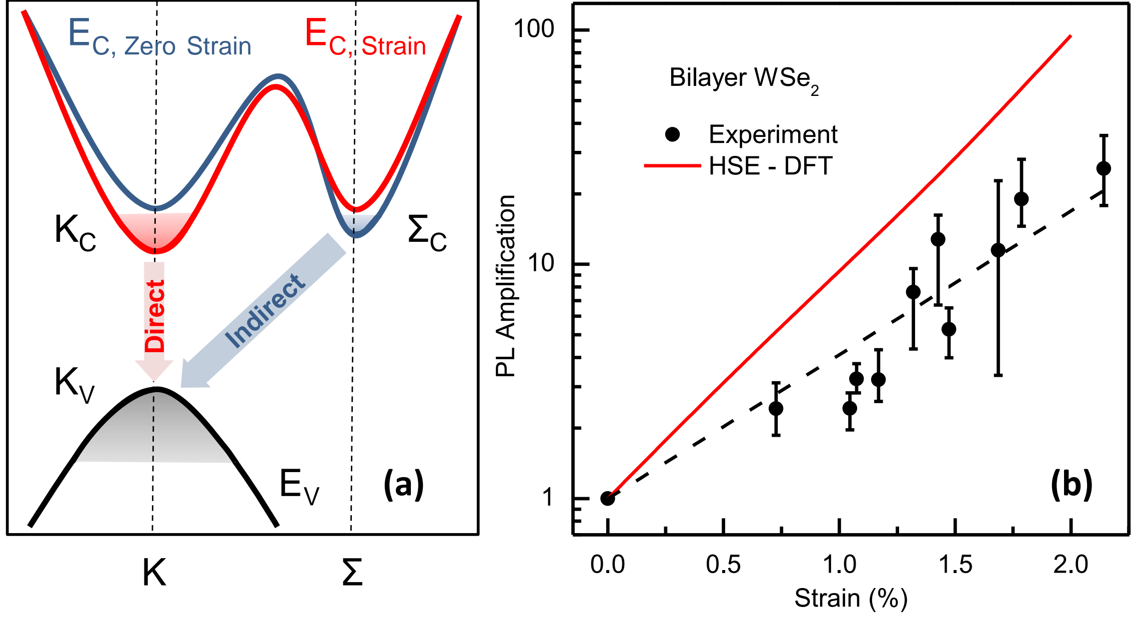

Figure. 3: (a) Schematic band structure, qualitatively showing occupancy of K_C and Σ_C CB minima at strain and zero-strain conditions and under illumination. (b) Bilayer WSe_2 PL amplification versus strain. Experimental data for multiple WSe_2 samples measured at several spots on the flake show increasing PL amplification with increasing strain. Theory prediction using HSE-DFT is consistent with the experimental trend. Symbols represent average PL amplification whereas the error bars represent the maximum and minimum error.

We make a set of simplifying assumptions to arrive at the theoretical prediction. To first order, we assume there is no radiative recombination from the indirect transition (Σ_C-K_V) and all the radiative recombination is from the direct transition (K_C-K_V) only. This is a fair assumption given that a radiative recombination event for the indirect bandgap requires a phonon for momentum conservation, which makes the probability of the event very small compared to radiative recombination for the direct bandgap (K_C-K_V). Next, the internal radiative efficiency η_{int} for the K_C-K_V transition is given by Eq. 1,

$$\eta_{int} = \frac{Anp}{Anp + Bnp^2 + Cn} = \frac{Ap}{Ap + Bp^2 + C} \qquad (1)$$

Here '*Anp*' represents the radiative recombination rate given by the product of the electron concentration n in the CB valley, the majority hole concentration p in the VB and the rate constant A. The other two terms, B and C represent the non-radiative recombination rate constants for Auger and Shockley-Read-Hall (SRH) processes, respectively [28]. We see that η_{int} depends only on the majority carrier concentration and we assume the rate constants A, B and C to be constant with strain. The PL intensity is given by Eq. 2,

$$PL \propto \left[\eta_{int} \times \frac{n(DG)}{n(DG) + n(IG)} \times \left(n(DG) + n(IG)\right)\right] \qquad (2)$$

where *n(DG)* and *n(IG)* are the number of electrons in the direct and indirect CB valley respectively. Thus the PL intensity is proportional to the fraction of radiative recombination from the direct valley, fraction of carriers in the direct valley and total number of carriers generated by laser illumination. PL amplification (ratio of the PL peak intensity at non-zero strain to that at zero strain) can thus be described by Eq. 3,

$$PL\ amplification = \frac{n(DG)_{strain}}{n(DG)_{zero\ strain}} \qquad (3)$$

Using the Boltzmann approximation for calculating carrier concentrations we get,

$$PL\ amplification = \frac{e^{\left(\frac{-E_G(DG)_{strain}}{kT}\right)}}{e^{\left(\frac{-E_G(DG)_{zero\ strain}}{kT}\right)}} \qquad (4)$$

Here $E_G(DG)_{zero\ strain}$ and $E_G(DG)_{strain}$ are the direct bandgap (DG) values at zero strain and non-zero strain conditions respectively. These are taken from the DFT calculations for different strain points and thus we get the theoretical prediction of PL amplification. Since the CB valley shifts linearly with strain, the PL amplification changes exponentially with strain, as indicated by the red line in Fig. 3b. Figure 3b also shows the PL amplification vs. strain for multiple bilayer WSe_2 samples for different representative spots (represented by the error bars) along with the experimental data fit. The theoretical prediction using DFT is consistent with the experimental data, with only a slightly steeper slope. This difference between experiment and calculation can be due to the reasons highlighted earlier and also due to the simplifying assumptions related to the rate constants A, B, and C in Eq. 1.

4.6 Mono, tri and quad layer WSe_2 strain

We also examined the effect of strain on different thicknesses of WSe_2. Fig. 4a-b show the PL and Raman data for monolayer WSe_2 under strain. Raman spectra clearly show the splitting and shift of the Raman modes as is observed for bilayer WSe_2 indicating application of strain. PL for monolayer WSe_2 shows a drastic increase with strain. This indicates that monolayer WSe_2 remains direct bandgap even under uniaxial tensile strain and the difference between the indirect and direct CB minima increases further, as predicted by Eq. 4. The results are consistent with the HSE-DFT analysis shown in Fig. S5a-b and are in stark contrast to monolayer MoS_2 behavior which in fact undergoes a direct to indirect transition on application of uniaxial tensile strain [15]. The PL and corresponding Raman spectra at different strain for trilayer and quadlayer WSe_2 are shown in Fig. 4c-d and Fig. 4e-f respectively. The background PL from the PMMA and PETG is subtracted from the trilayer and quadlayer WSe_2 PL. The PL intensity gets amplified with strain for both trilayer and quadlayer. We also see a second peak corresponding to the direct gap appearing at higher energy which shows a red shift with increasing strain. Thus all results and trends are consistent with earlier observations for bilayer WSe_2. The decreasing PL amplification as a function of number of layers, for a given strain, is an indicator that the direct to indirect CB valley difference increases with thickness [16].

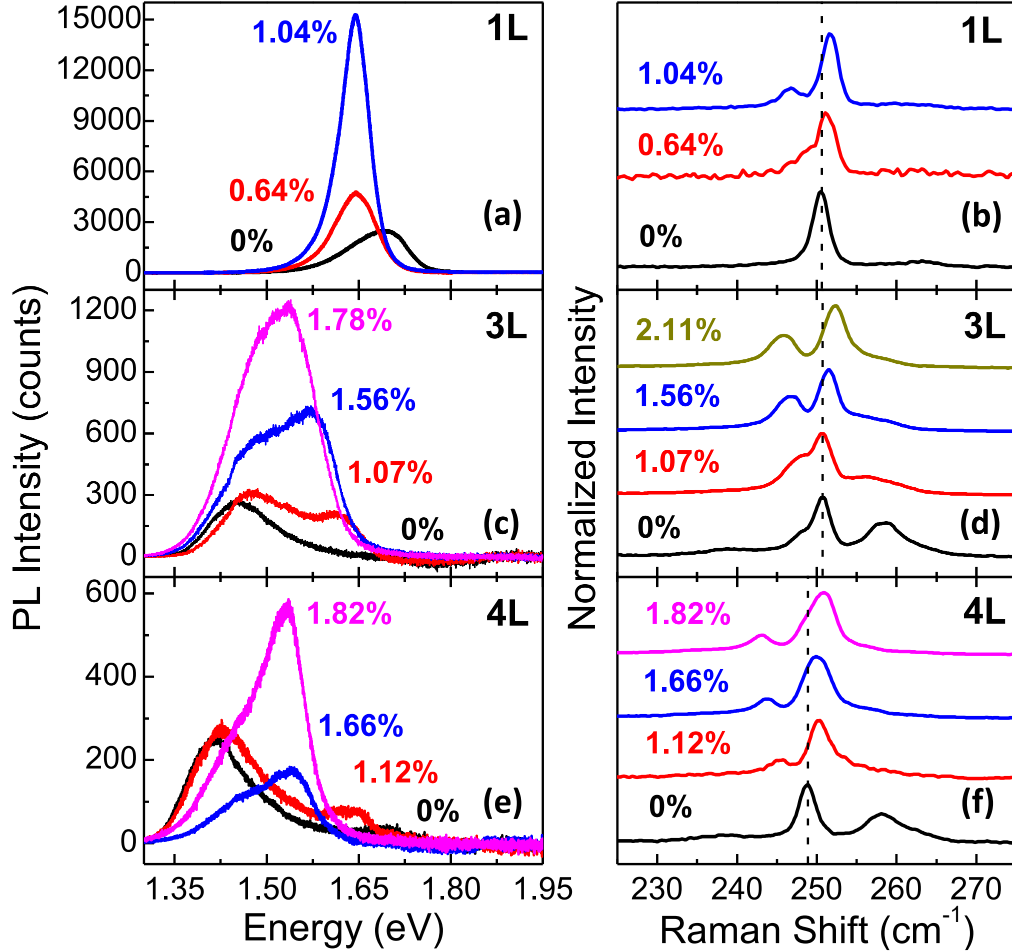

Figure 4: PL and Raman spectra at different strain for (a-b) Monolayer, (c-d) Trilayer and (e-f) Quadlayer WSe_2. In (c) and (e), a second peak corresponding to K_C-K_V transition is seen at higher energies which red shifts with strain. Σ_C-K_V peak blue shifts by a slight amount. Raman spectra in all cases show splitting under strain.

The PL trends of Fig. 2 and Fig. 4 together as a function of layer thickness can be understood by looking at the relative occupancies of the K_C $\left(\frac{n(DG)}{n(DG)+n(IG)}\right)$ and Σ_C $\left(\frac{n(IG)}{n(DG)+n(IG)}\right)$ valleys when illuminated by the laser as shown in Fig. 5a. The peak values (for WSe_2 2-4 layers) are extracted from the PL data of Fig. 2a and Fig. 4c, e. As the K_C - Σ_C difference reduces with increasing strain, the PL increases drastically resulting in the two peaks merging. From the occupancy plots we can clearly understand the dependence of the critical strain required to bring about an indirect to direct bandgap crossover, on the number of layers. Bilayer WSe_2 shows an increase in the K_C occupancy at a lower strain as compared to trilayer. The same trend is valid between trilayer and quadlayer WSe_2. Fig. 5b shows the PL amplification at ~1% strain as a function of layer number. The PL amplification achievable for a given strain value reduces as layer number increases. Fig. S6a-b show the PL and Raman spectra at different strain values for bulk WSe_2 (~ 30 nm). We see a slight Raman peak splitting for bulk WSe_2 but no significant change in the PL spectrum. This is consistent with the fact that the difference of ~ 200 meV between the indirect and the direct CB minima for bulk WSe_2 at zero strain [16] is so large that it is difficult to induce a crossover from indirect to direct bandgap with the maximum strain achievable by the

experiment. We thus see a drastic increase in the PL intensity only for few-layer (1-4) WSe_2 samples due to limitation of the maximum strain applicable by the experimental setup.

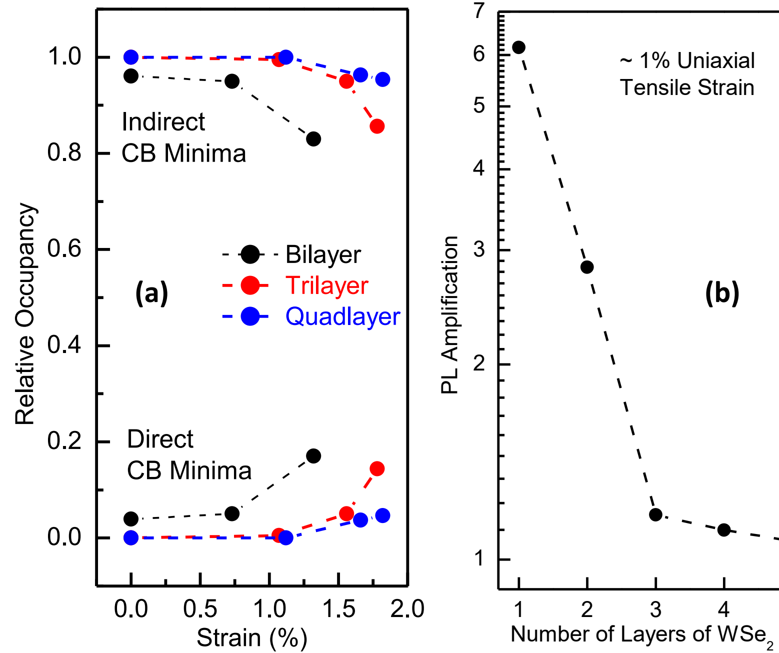

Figure 5: (a) Relative occupancy of the direct and indirect CB minima for bilayer, trilayer and quadlayer WSe_2 as a function of strain. Peak values for occupancy calculations are extracted from the PL data. (b) PL amplification at 1% strain vs. number of layers. PL amplification reduces with layer number since the direct and indirect bandgap difference at zero strain increases with layer number.

In conclusion, WSe_2 multilayers are shown to exhibit drastic increase in PL intensity under the application of uniaxial tensile strain. Multilayer WSe_2 with a direct bandgap is experimentally demonstrated and predicted by DFT by applying tensile strain. Moving forward, band structure and bandgap engineering with strain can be used as a method to change the mobility of carriers in WSe_2. At the same time, increased PL emission properties make strained multilayer WSe_2 a promising contender for optoelectronic devices. In addition to emission properties, future absorption studies under strain would provide great insight into the potential use of WSe_2 in applications like photovoltaics and photodetectors.

4.7 Supporting information

Sample preparation method:

WSe_2 (2dsemiconductors.com) was mechanically exfoliated using the adhesive tape method onto 260 nm SiO_2/Si substrate (SVM wafers). The chips were mapped to find the flakes of desired thickness using an optical microscope based on the color and contrast of the flakes, which is determined by the thickness of the underlying oxide (260 nm) and the refractive index of WSe_2. The flakes were then transferred by a dry transfer technique [19] using PMMA (MicroChem) as the transfer medium, onto a clear and flexible PETG substrate of 1.5 mm thickness. The samples

were subsequently annealed at 125° C for 5 minutes so that the flake and PMMA handling medium stick to the PETG. The partial thermoforming /softening of the PETG at the annealing temperature helps clamp the flake along with the PMMA enabling the application of large strain.

Strain Calculation and MoS_2 internal reference:

The bent PETG substrate is approximated as a circular arc for the purpose of strain calculation. A snapshot of the bent PETG is taken at each strain condition and then the parameters *'Θ'* and *'a'* as shown in Fig. 1a are extracted. The strain at the top surface of the PETG is given by $\varepsilon = \frac{\tau}{2R}$ where τ is the thickness of the PETG and R is the radius of the bent PETG. From geometry $R = \frac{a}{sin\theta}$ which gives $\varepsilon = \frac{\tau sin\theta}{2a}$. The computed strain is valid for low angles of *'Θ'*. At large *'Θ'* the circular arc approximation fails and the maximum strain is ~ 20% higher [29]. For this work, all strain values are computed using the circular arc approximation. The strain computed is also compared with strain calculated from a MoS_2 internal reference flake which is discussed in Fig. S1 in more detail.

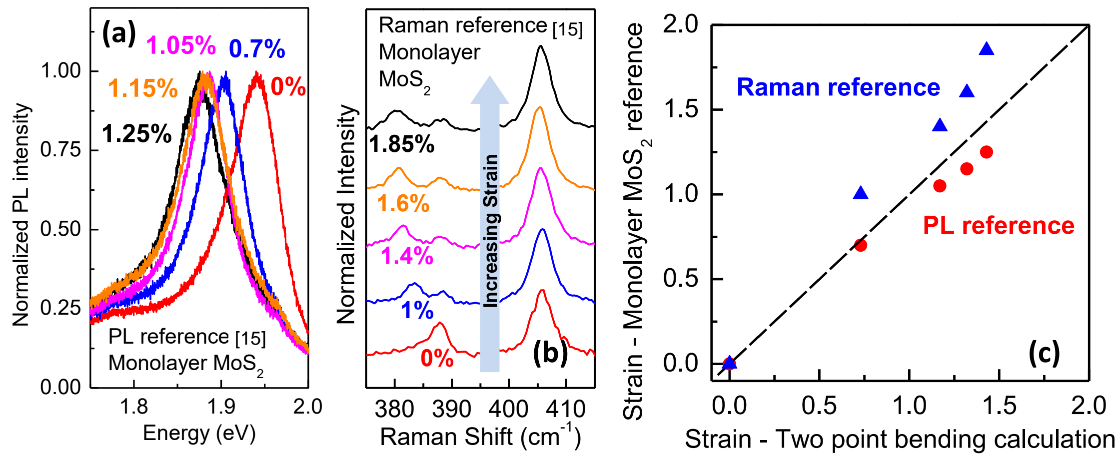

Figure S1: (a) PL spectra for monolayer MoS_2 for varying strain. The shift in the PL peak is used to calculate strain from reference [15]. The absolute peak value is different from that in ref. [15] possibly due to substrate effects (Reference [15] used polycarbonate whereas we use PETG). (b) Raman spectra for monolayer MoS_2 for varying strain. Again the shift in the Raman peak is used to compute strain from reference [15]. (c) The strain from the PL and Raman references in (a) and (b) is plotted versus the strain computed for the same samples from our own two-point bending calculation showing an almost 1:1 correlation.

Local Strain effects and reversibility of strain:

The Raman and PL measurements over multiple spots on a flake show that small local variations in strain exist on a flake even at zero strain. The local strain effects can be due to multiple reasons such as existing defects, ripples, folds or edges in the flake. In addition small strain can also be induced by thicker adjacent flakes or during the processing of the sample. Multiple spots on a flake were measured and representative data discussed in this work represents the modal trends seen at each strain. A PL line scan on a bilayer sample also shows that local strain variations are over a much larger scale than the spot size of the laser.

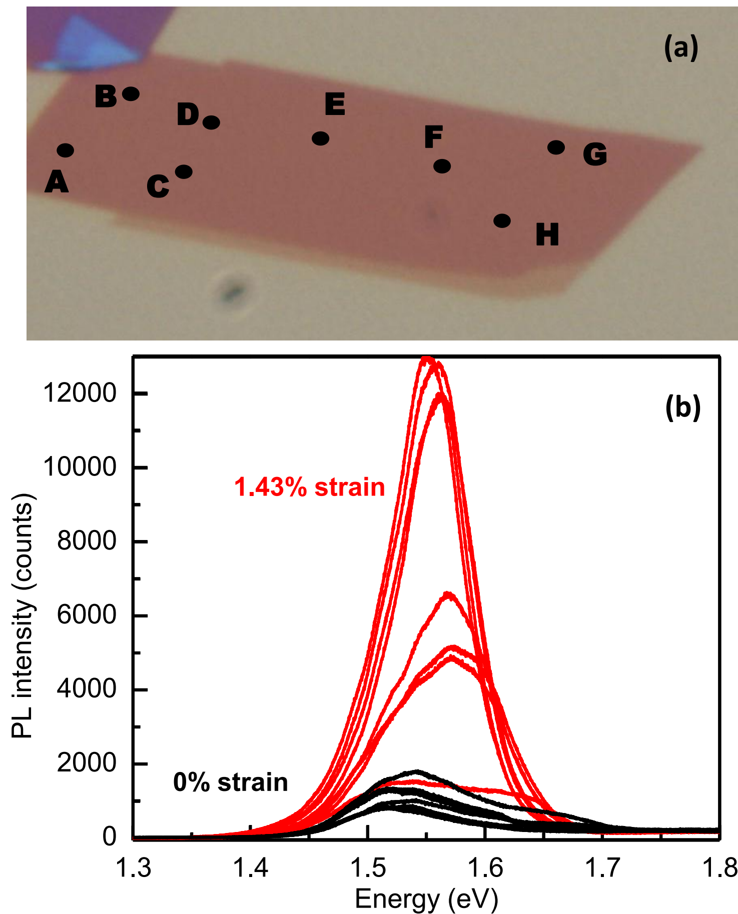

Figure S2: (a) Optical image of bilayer WSe_2 flake showing the spots where PL and Raman spectra are measured. (b) PL spectra for different spots at a given strain indicating the variation in PL due to local strain effects.

Repeated straining experiments with PETG samples were also performed to check the reversibility of strain application. This is important so as to verify that the flake does not slip on the substrate and the strain measured is actually the strain imparted to the flake. The reversibility in trends for a bilayer sample were seen up to a strain of ~ 1.04%. For very large strain, the PETG enters the plastic regime and cannot return to its original unbent shape.

Density functional theory analysis of WSe_2 under uniaxial tensile strain:

Heyd-Scuseria-Ernzerhof (HSE) exchange correlation potential with spin orbit coupling was used to model the electronic band structure for WSe_2. An ultra-soft PAW pseudo-potential with semi-core electrons and a cut-off energy of 400eV for the plane waves was used. For strained WSe_2, structure relaxation was first performed to determine the relaxed atomistic structure in the presence of uniaxial strain, and the band structure in the presence of strain was subsequently calculated. Structural relaxation is achieved by minimizing the energy with a tolerance of 1 meV (for total energy in the range of 44-45eV). Fig. S3 schematically represents the direction of application of strain in the DFT calculations and the reciprocal space of WSe_2.

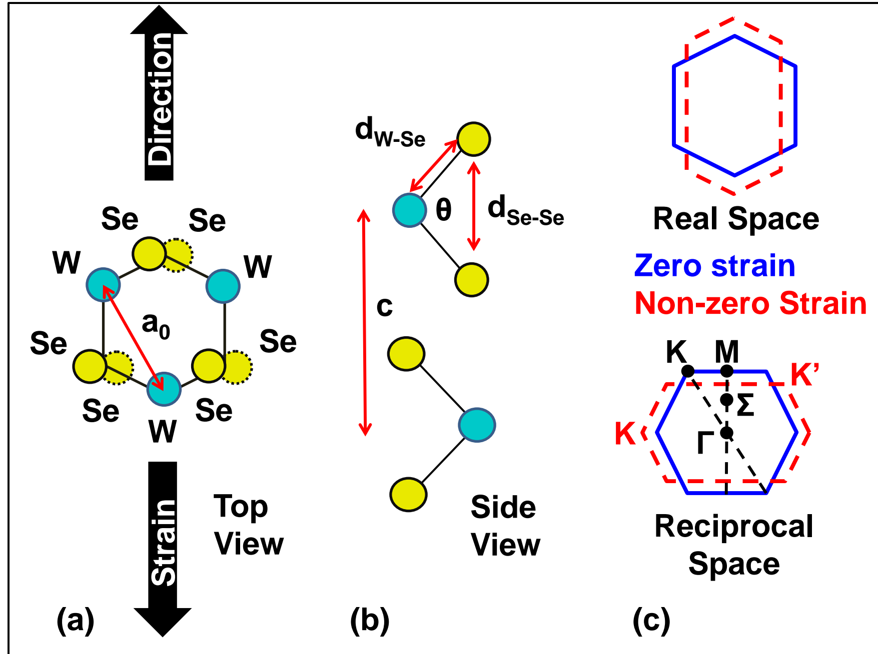

Figure S3: (a) Top view of WSe_2 showing direction of strain (b) Side view of WSe_2 (c) Real and reciprocal space of WSe_2 with and without strain. Reciprocal space shows the K, M, Σ and Γ points.

We see that the crystal lattice and the reciprocal space get stretched when strain is applied. For monolayer WSe_2 as strain is applied the intra-layer Se-Se distance decreases; whereas for bilayer WSe_2 the Se-Se intra-layer and inter-layer distances decreases whereas the W-Se bond length at the outer Se increases. The degeneracy of the 6 K points is however maintained because the positions of the K, M, Σ, etc. points may have changed, but the E-*k* relation along two different directions say K- Γ and K'- Γ (Fig. S3c) will still be the same because the reciprocal lattice vectors have also changed.

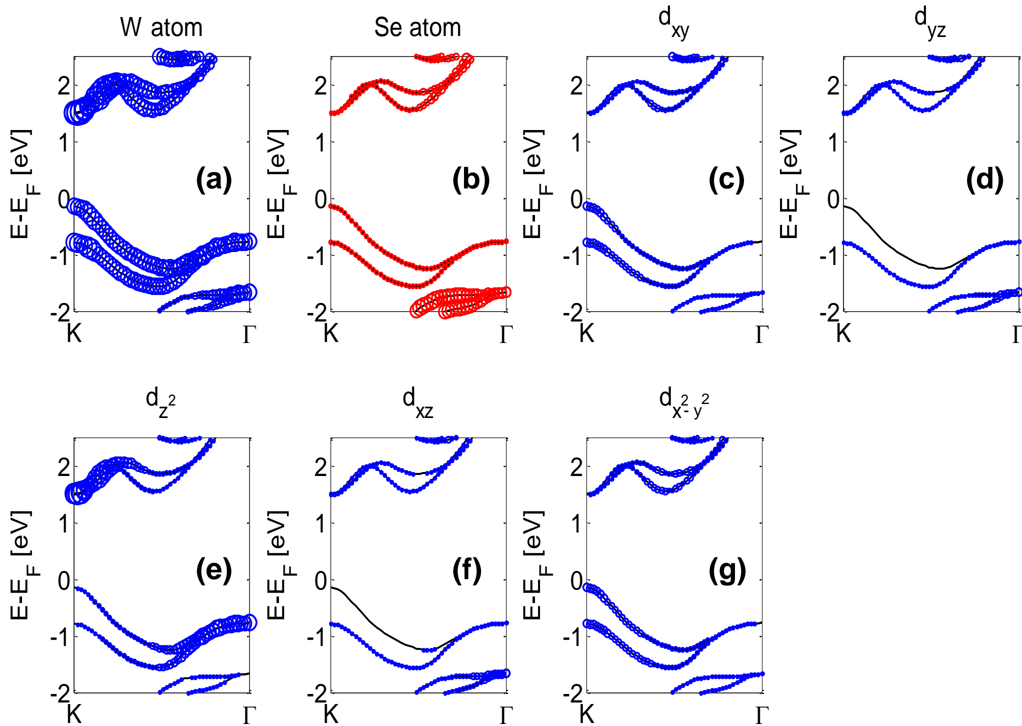

Figure S4: Electronic band structure for unstrained monolayer WSe_2 from HSE-DFT simulations showing the relative contribution of different orbitals to the energy bands, which is directly proportional to the size of the circles on the curves. (a) W atom orbital and (b) Se atom orbital contributions. (c-g) Different W orbital contributions to the energy bands.

Fig. S4a and Fig. S4b clearly illustrate that the W atom orbitals dominantly contribute to the energy bands near the conduction band (CB) minima and the valence band (VB) maxima. From Fig. S4c to Fig. S4g we also understand that the contribution of the W d_{Z^2} orbital to the CB minima at the K point is maximum. The above observations are found to be true for bilayer WSe_2 as well from the DFT calculations. Thus change of the interlayer W-W distance in strained bilayer WSe_2 and hence the orbital overlap for the d_{Z^2} orbitals affects the CB minima at the K point drastically and leads to an indirect to direct bandgap transition as explained in Fig. 2b in the main text.

Effect of uniaxial tensile strain on monolayer WSe_2:

Monolayer WSe_2 PL spectra at different strain in Fig. 4a clearly show an increase in PL intensity with increasing strain. Also peak shifts and FWHM becomes narrower. For no strain case the PL peak is at 1.7eV (shifted from 1.65eV when on SiO_2) and also shows a significant red tail. This can be possibly due to substrate and excitonic effects in WSe_2. Raman spectra at different strain for monolayer WSe_2 in Fig. 4b show peak splitting of the E^1_{2g} mode indicating that strain is applied on the flake.

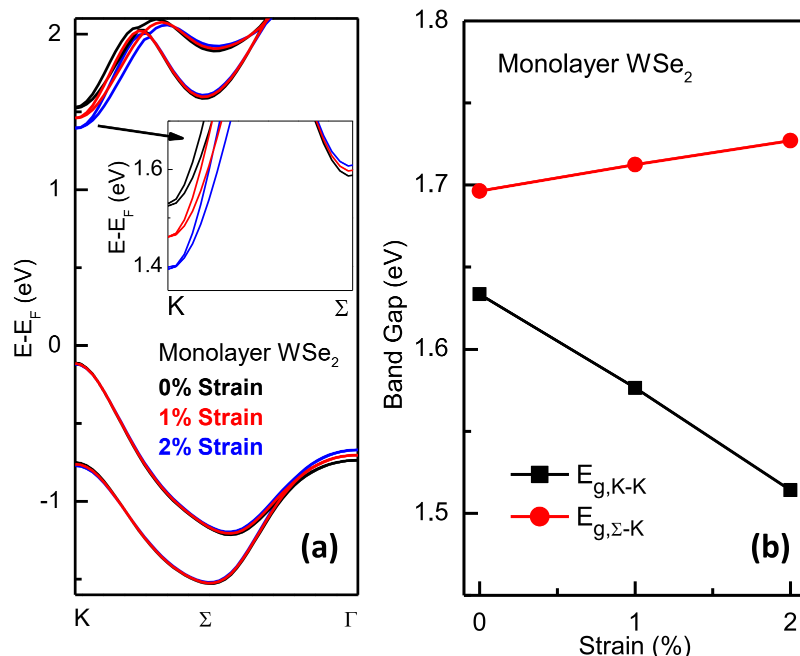

Figure S5: (a) Electronic band structure for monolayer WSe_2 from HSE-DFT simulations showing the bandstructure w and w/o strain. CB minima at K point moves down drastically indicating that monolayer WSe_2 remains direct bandgap even under tensile strain and the difference between the indirect and the direct valleys increases further. (b) Indirect and direct bandgap values obtained from HSE-DFT simulations for monolayer WSe_2.

Raman and PL spectra at different strain for bulk WSe_2:

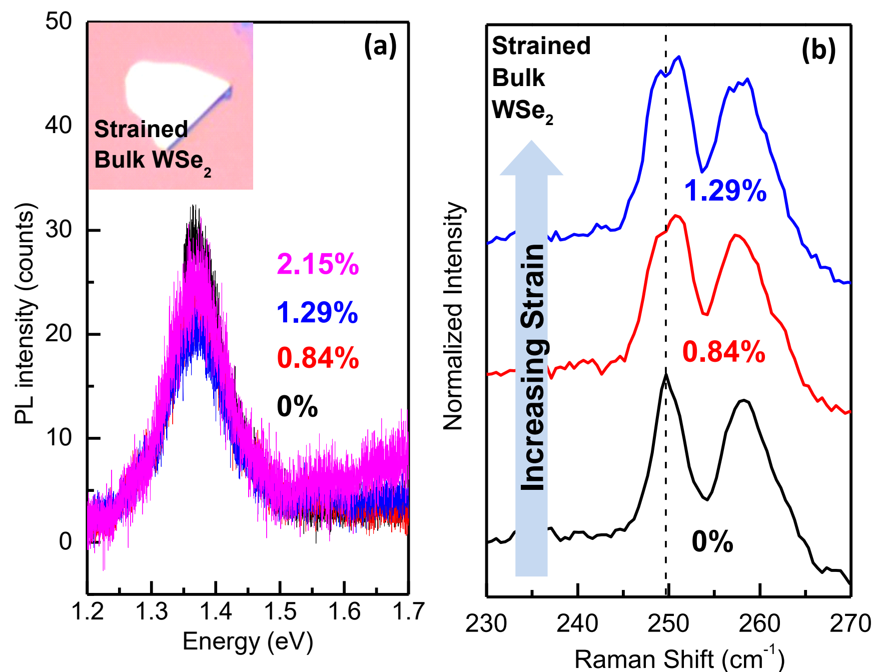

Figure S6: (a) PL and (b) Raman spectra at different strain for bulk WSe_2. Inset shows corresponding flake. Peak splitting seen in all spectra at non-zero strain. PL spectra at different

strain for bulk WSe_2 show no change in PL consistent with the fact that for bulk WSe_2 the direct and indirect bandgap difference is very large (~200meV) [16], thus requiring huge strain for a crossover.

G_0W_0 calculation approach:

In the following GW quasi-particle (QP) calculation, non-self-consistent G_0W_0 was used to reduce the computational cost [25]. Same atomistic relaxed structure was used as in the main text. HSE exchange-correlation functional was used to obtain wave functions for the GW calculation. Although this step is not essential, this method has been suggested to improve agreement with experiments [30]. The Brillouin zone sampled with a $6 \times 6 \times 1$ k-point mesh. The band-structure was Wannier interpolated using the WANNIER90 program [31]. From the figure S7a, ~0.65 eV shift of CBM as regard to the valence band can be observed. In figure S7b, splitting the valence bands due to spin orbital coupling is shown.

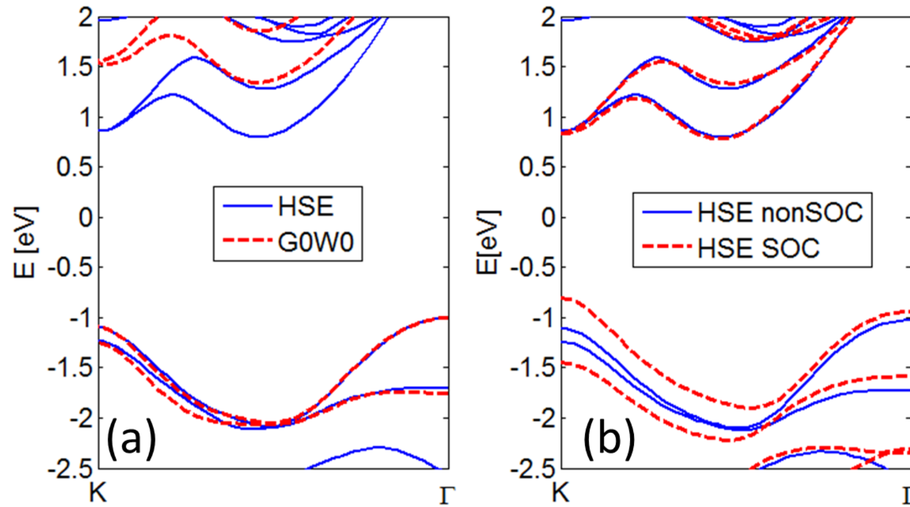

Figure S7: (a) Comparison of Wannier interpolated HSE-DFT and G_0W_0 calculation. SOC is not considered and no strain is applied. (b) Comparison of spin orbital coupling (SOC) effect in HSE-DFT calculation. Band splitting in the K point of the valence band can be observed.

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5

[5]Gold Mediated Exfoliation of Ultra Large Optoelectronically Perfect Monolayers

5.1 Introduction

Transition metal dichalcogenides (TMDCs) are a class of layered materials analogous to graphene which have aroused immense interest in the last few years as a potential platform for future electronic and optoelectronic applications [1, 2]. The layers in these materials are held together by weak van der Waals (vdW) forces making it easy to cleave them to the limit of a monolayer (a single unit of 3 atomic layers, comprised of 1 layer of the transition metal atoms sandwiched between 2 layers of the chalcogen atoms). Monolayers of many TMDCs like MoS_2, WS_2, WSe_2 and $MoSe_2$ are especially exciting since they are direct band gap semiconductors, making them ideal for applications in devices such as LEDs, lasers, photodiodes, etc. Their naturally passivated surfaces, sizeable bandgaps (~1 – 2 eV), atomic scale thickness (~0.7 nm), and low dielectric constant (~ 4) also make them suitable candidates for replacing silicon at the metal-oxide-semiconductor field-effect transistor (MOSFET) scaling limit due to mitigated short channel effects [3].

Monolayer TMDC flakes typically produced using the tape exfoliation method (similar to Scotch® tape method used for graphene [4]) are small in size (~5 μm) and the yield of the procedure is poor. Simple modifications like exfoliating the flakes on a hot plate result in a slight increase in the size of flakes achieved [5]. Tape exfoliation of monolayers relies on the probability of cleaving the crystal such that (N-1) layers remain adhered to the tape while only a monolayer is transferred onto the SiO_2 substrate. The interaction of TMDCs with the SiO_2 substrate is weak, resulting in a low probability of the above event and, consequently, minimal control over the flake size. The small size of the exfoliated flakes makes their characterization difficult. Techniques such as Angle-resolved photoemission spectroscopy (ARPES), X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS), etc. which require large area macroscopic samples are difficult to apply to small monolayer samples. Small flakes from the tape exfoliation method also limit the size of electronic devices and circuits which can be fabricated per flake to just a few transistors [6].

5.2 Gold-mediated exfoliation technique

In this work we demonstrate an exfoliation technique using evaporated gold films [7, 8] to exfoliate large area TMDC monolayers onto various substrates such as SiO_2/Si and quartz. Gold is known to have a strong affinity for chalcogens, especially to sulphur atoms with which it forms

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a semi-covalent bond with bond strength of approximately 45 kcal mol^{-1} [9, 10]. The interaction between gold and sulphur has been used in the formation of self-assembled monolayers (SAM) of thiolated organic molecules on gold surfaces [10] and gold-thiolate complexes. The same idea is used in this work by selectively increasing the adhesion of the topmost layer of a bulk TMDC crystal to gold by evaporating a thin film on it and subsequently peeling it off from the bulk crystal. The detailed process flow is illustrated in Figure 1a. Gold (~100 – 150 nm) is evaporated onto bulk MX_2 (M = Mo or W; X = S or Se) crystals. The gold atoms bond with the chalcogen atoms of the topmost layer of MX_2. The interaction of the topmost layer with the evaporated gold is stronger than the vdW interactions of that same layer with the bottom layers of MX_2. This enables selective peel-off of the topmost layer using a thermal release tape which is later stuck onto the desired target substrate (SiO_2/Si or quartz). The thermal tape is then released on a hot plate (~130 ^oC) and the substrate is treated with a mild O_2 plasma to remove the tape residue from the surface. The O_2 plasma power and etching time are kept low to ensure that the gold does not get etched away thereby exposing the underlying monolayer MX_2. The gold film is then etched using KI/I_2 wet etch (Transene Gold Etch – type TFA for four minutes) which does not etch the TMDC flakes. This is followed by a 10 minute acetone clean and IPA rinse to remove any residues, to obtain the large area monolayers.

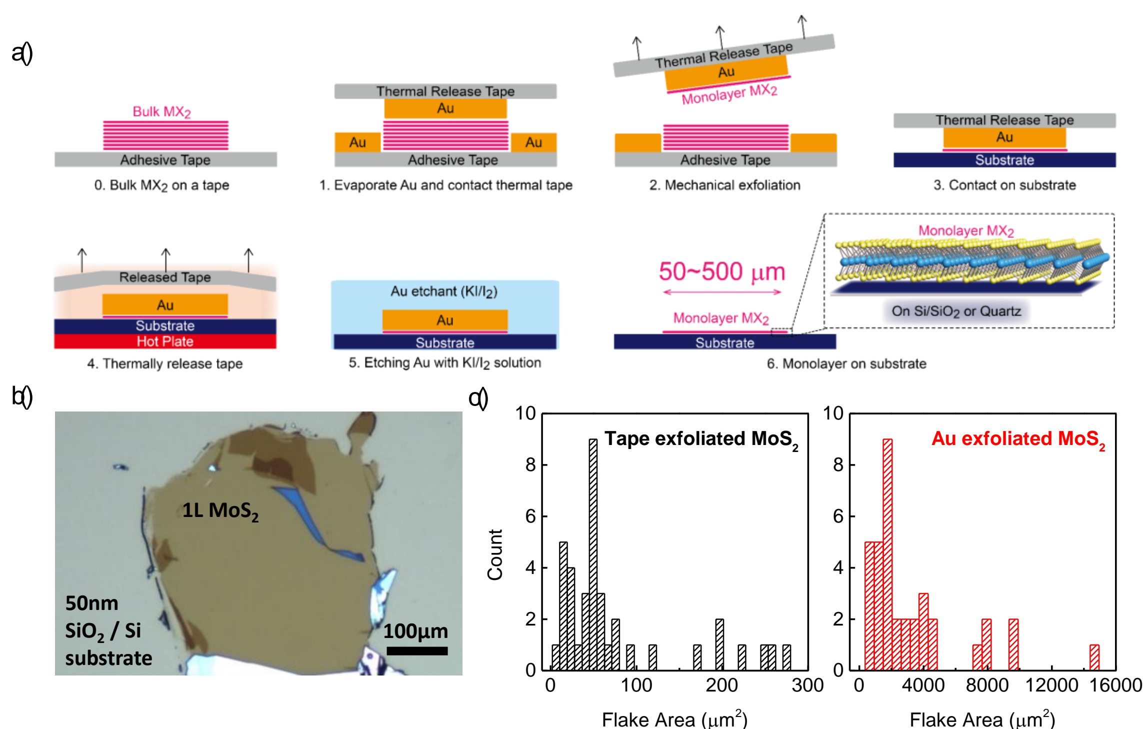

Figure1: (a) Schematic illustration of Au exfoliation process (b) Optical microscope image of large monolayer MoS_2 flake (c) Histogram of flake areas for tape exfoliated versus Au exfoliated MoS_2

The relatively strong binding of the gold to the topmost layer of MX_2 enhances the probability of the crystal to cleave right at the topmost layer, increasing both the yield and the size of the flakes obtained. Using this technique, large area MoS_2 monolayers with lateral dimensions up to ~500 µm are obtained. Figure 1b shows the optical image of one such large monolayer on a

50 nm SiO_2 / Si substrate. The process was also used to exfoliate other TMDCs such as WS_2 and WSe_2 (Figure S1b-c). For the scope of this paper we focus on the exfoliation and characterization of MoS_2 as a model system for all TMDCs. The histograms in Figure 1c show that the flake area for MoS_2 flakes obtained by the gold (Au) exfoliation method is ~10000 times larger than that of flakes obtained by the tape exfoliation method. The size of the monolayer flakes exfoliated by gold is primarily limited by the size of the source MoS_2 crystal domains and may be increased in the future by the use of large sized flat crystals. Figure S2 shows the optical microscope images of several Au exfoliated MoS_2 samples on 50 nm SiO_2/Si substrates. The images indicate that exfoliated monolayer area is larger than that of multilayer MoS_2, thereby demonstrating that Au adheres preferentially to the topmost layer of MoS_2. The exfoliated bulk regions may be attributed to cleaving at potential defect sites in the source crystal. Also, we empirically observed that the probability of obtaining Au exfoliated monolayers is several times more in contrast to the tape exfoliation method. The exfoliation method described here does not involve the double transfer of exfoliated monolayers like the technique in Ref. [7] which first requires exfoliation onto an Au substrate followed by transfer to the target substrate. Furthermore, the flakes are uniform over a large area which is important for electrical device applications.

The success of the Au mediated exfoliation of large-area MoS_2 can be attributed to two main factors. First, as noted above, the Au binds to the S atoms quite strongly which enables its adhesion to the topmost layer of MoS_2. A second factor also contributes to the single layer selectivity of the process: as shown by previous calculations, large mismatch in lattice constants causes strain between the topmost layer of MoS_2 and gold [11]. The first layer of MoS_2 is compliant and can slip relative to the underlying substrate, which slightly weakens its bond with the other layers of the bulk MoS_2 crystal. Similarly, strain due to evaporated metal films was also used to exfoliate single layer graphene as shown in [11].

5.3 XPS characterization of gold-exfoliated MoS_2

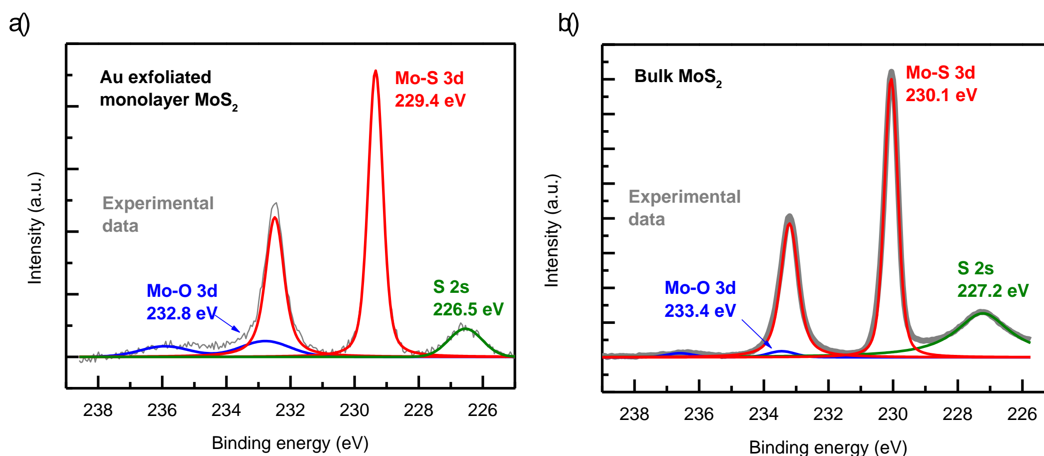

Figure2: (a) XPS experimental data and fitted Voigt curves for a Au exfoliated monolayer MoS_2. (b) XPS experimental data and fitted curves for the bulk MoS_2 crystal source.

Prior to this work, because of the small size of tape exfoliated flakes, surface characterization of MoS_2 monolayers has only been possible with PEEM (Photoemission electron microscopy) [12]. Gold exfoliated monolayers are sufficiently large to be characterized by standard XPS measurements. XPS measurements were performed using a macroscale monochromatic Al Kα excitation source, and allowed direct comparison of the monolayers to the bulk crystal used for our source material (Figure 2). Following background subtraction and fitting (experiment details are given in methods section), the XPS data for monolayer MoS_2 is found to be qualitatively similar to the XPS spectrum of MoS_2 bulk crystal with some notable differences in the peak binding energies. Of particular note is the red shift (~0.7 eV) in the binding energy for monolayer MoS_2 compared to bulk MoS_2. This is consistent with charge transfer from the underlying silicon substrate to the monolayer MoS_2 flake. This XPS measurement demonstrates the importance of the Au exfoliation technique towards accelerating monolayer TMDC research since measurements such as PEEM require bright light sources which are typically limited to synchrotron facilities.

5.4 Optical characterization of gold-exfoliated MoS_2

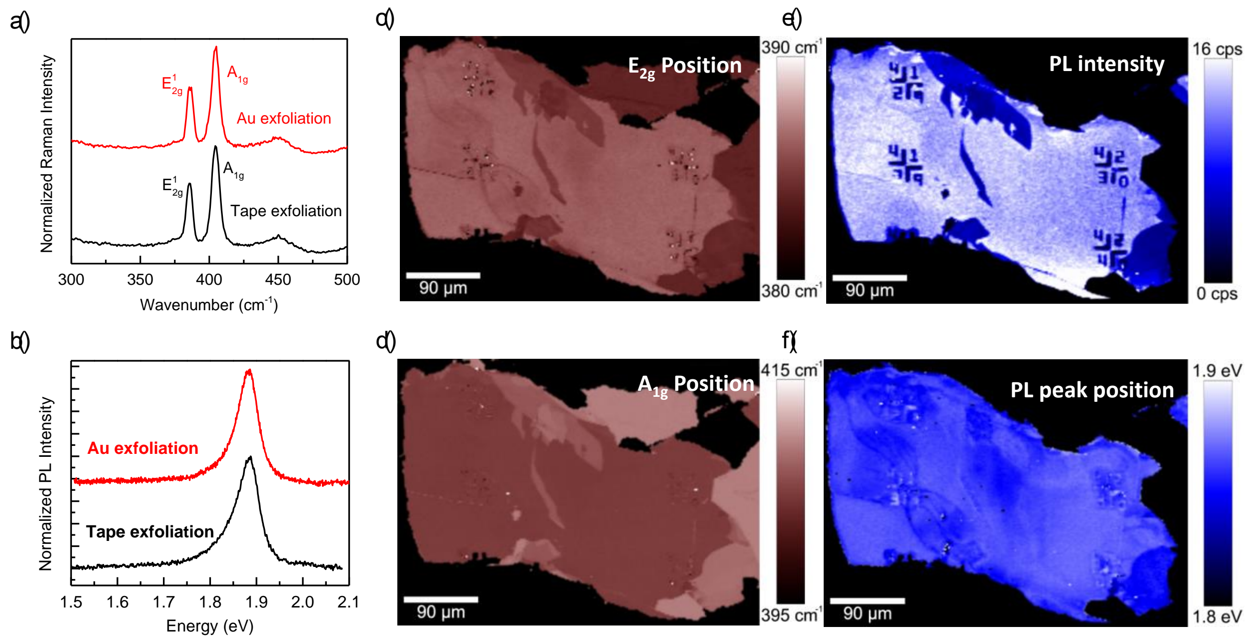

Figure3: (a) Raman spectra comparison for Au exfoliated flake versus tape exfoliated flake (b) Photoluminescence spectra comparison for Au exfoliated flake versus tape exfoliated flake (c-d) Raman peak E^1_{2g} and A_{1g} maps of monolayer MoS_2 flake in Figure 1b. (e-f) PL peak intensity and position maps of monolayer MoS_2 flake in Figure 1b

The Au exfoliated MoS_2 flakes undergo a multi-step process, including Au evaporation, KI/I_2 etching and acetone cleaning. Apart from XPS, careful characterization by optical and electrical measurements is necessary to compare their quality to flakes from the tape exfoliation method. Figure 3a-b show that the Raman and photoluminescence (PL) spectra for Au exfoliated MoS_2 flakes are identical to those of tape exfoliated MoS_2 flakes. No new features or peaks are observed in both Raman and PL. Identical Raman peak positions also indicate that the flakes are

not strained. Figure 3c-d show the Raman map of the position of the E^1_{2g} and the A_{1g} peaks of MoS_2 for the large flake shown in Figure S1a. The Raman peak position value can be used to identify the monolayer and multilayer MoS_2 regions of the flake [13]. The peak positions are quite uniform over the entire area of the monolayer flake away from any markers on the chip. Near the markers (5/35 nm Cr/Au thick) we see a slight variation in the peak position indicating that the MoS_2 locally is strained due to substrate topography [14]. Figure 3e-f show the PL peak position and intensity map for the same flake. This map is also quite uniform over the entire monolayer region except for the strain fields near the markers which is visible in the PL peak position map. The absence of strain and the uniformity of Raman and PL over the large area of MoS_2 is of utmost significance for device applications. Strain induced variations of the bandgap, mobility and effective mass can all affect device performance, resulting in statistical variations of intrinsic parameters like threshold voltage, ON/OFF current, etc. similar to problems caused by line edge roughness in modern MOSFETs.

Photoluminescence quantum yield (QY) measurement, which provides a quantitative estimate of the fraction of radiative recombination in a material over total recombination, is an accurate way to gauge optoelectronic quality. For an ideal material with zero defects (i.e. trap states) and low carrier concentration the QY should be 100% at low injection levels where carrier-carrier interactions such as Auger or biexcitonic recombination are not dominant. However, it has been experimentally found that the tape exfoliated MoS_2 flakes have poor QY of the order of ~1% at most [2] due to defects such as vacancies pre-existing in the bulk crystal. Recently, we demonstrated that it is possible to repair / passivate defects in tape exfoliated MoS_2 flakes using bis(trifluoromethane)sulfonimide (TFSI, Sigma-Aldrich), an organic superacid, leading to a drastic enhancement in QY to almost 100% [15]. The same treatment procedure is applied here to the Au exfoliated large-area MoS_2 flakes. Figure 4a shows the PL spectrum for the Au exfoliated monolayer MoS_2 before and after the chemical treatment. The PL intensity increased by a factor of ~238× after treatment for this sample. Figure 4b shows the QY measured over a pump-power dynamic range of six orders of magnitude for both tape exfoliated (from ref. [15]) and Au exfoliated MoS_2 monolayers, before and after the chemical treatment. The details of the measurement are provided in Ref. [15]. The chemical treatment results in almost 100% internal QY, yielding ultra-large optoelectronically perfect monolayer flakes at low pump-power as was observed previously in tape exfoliated samples. Furthermore, at higher injection levels we observe a reduction in the QY consistent with intrinsic biexcitonic recombination which was observed in tape exfoliated flakes; both samples show the onset of biexcitonic recombination at similar pump-power. These observations suggest that the optical quality, defect type and defect passivation mechanism are similar for MoS_2 flakes obtained from both exfoliation methods.

5.5 Electrical characterization of gold-exfoliated MoS_2

Electrical characterization of Au exfoliated monolayer MoS_2 was performed to comprehensively compare its quality against tape exfoliated flakes and extract important device parameters such as mobility. Figure 5a shows the cross section schematic of a back-gated monolayer MoS_2 MOSFET fabricated on 50 nm SiO_2 / n^{++} Si substrate with Ni source and drain contacts. Figure 5b is a representative image of fabricated monolayer MoS_2 devices with varying channel lengths. The arbitrarily shaped monolayer MoS_2 flakes are pattern etched into a regular shape channel to ensure deterministic current flow from source to drain thereby permitting accurate extraction of device parameters. Details of the device fabrication are described in the methods

section. Figure 5c-d show the I_D-V_{GS} and I_D-V_{DS} characteristics for a long channel (L = 20 µm) device measured in vacuum. The Si substrate is used as the global back gate with the 50 nm SiO_2 layer serving as the gate dielectric. The electrical characteristics show typical long channel MOSFET behavior with saturation observed in the I_{DS}-V_{DS} characteristics.

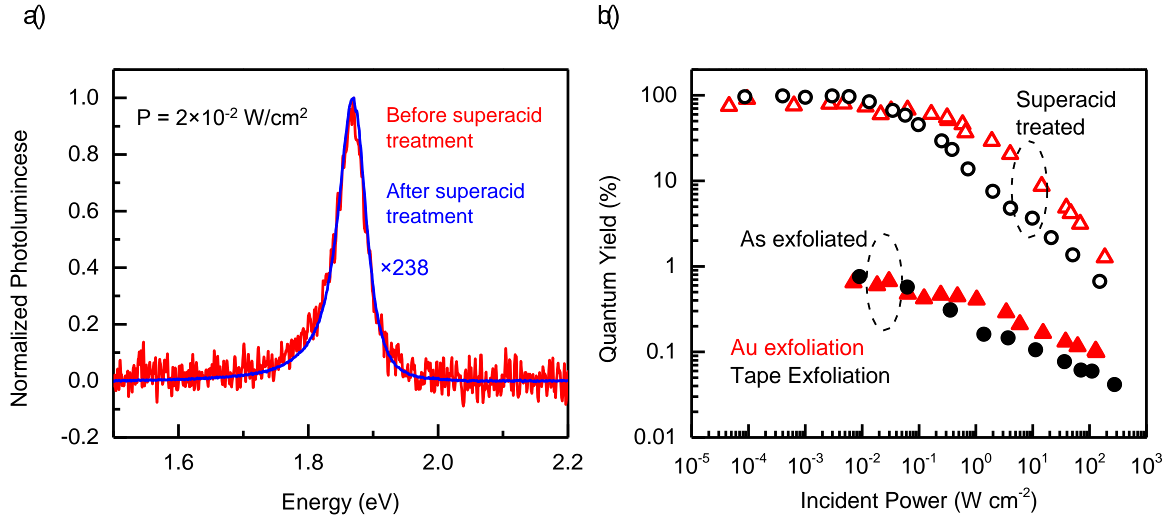

Figure4: (a) PL spectra before and after chemical treatment on Au exfoliated monolayer MoS_2 (b) Quantum Yield versus incident power intensity for tape exfoliated and Au exfoliated monolayer MoS_2 before (as exfoliated) and after chemical treatment (TFSI).

After accounting for the large contact resistance (R_C) which leads to a huge underestimation of mobility of carriers as described in Ref. [16], the mobility for electrons is calculated to be ~26 $cm^2\ V^{-1}\ s^{-1}$ for the L = 20 µm monolayer MoS_2 device in Figure 5c-d (R_C ~ 3.85 MΩ-µm, (V_G - V_T) ~ 6 V). The value of extracted mobility is consistent with the range of values reported in literature for monolayer MoS_2 [17]. The electrical characteristics of Au exfoliated flakes are thus found to be similar to those of monolayer MoS_2 flakes from tape exfoliation. The long channel length MOSFETs (L = 20 and 30 µm) further demonstrate the uniformity of the monolayer MoS_2 flakes over a large area which is essential for building complex circuits.

In conclusion, we have demonstrated an exfoliation technique utilizing the interaction strength of Au with chalcogens to preferentially obtain large areas of monolayer TMDCs on various substrates with high yield compared to the standard tape exfoliation method. Through extensive electrical and optical characterization we conclude that the quality of flakes obtained by the tape exfoliation and by the Au exfoliation techniques is the same. Ultra-large optoelectronically perfect MoS_2 monolayers with a PL QY of ~ 100% were obtained after treatment with an organic superacid. Standard XPS performed on ultra-large area monolayer MoS_2 illustrates the importance of this technique for expanding research capabilities. Automating and mechanizing the transfer process described in this work may be explored in the future for more controlled exfoliation and transfer of TMDC monolayers onto desired substrates. Ultimately, this technique can advance the possibility of large scale fabrication of monolayer TMDC devices.

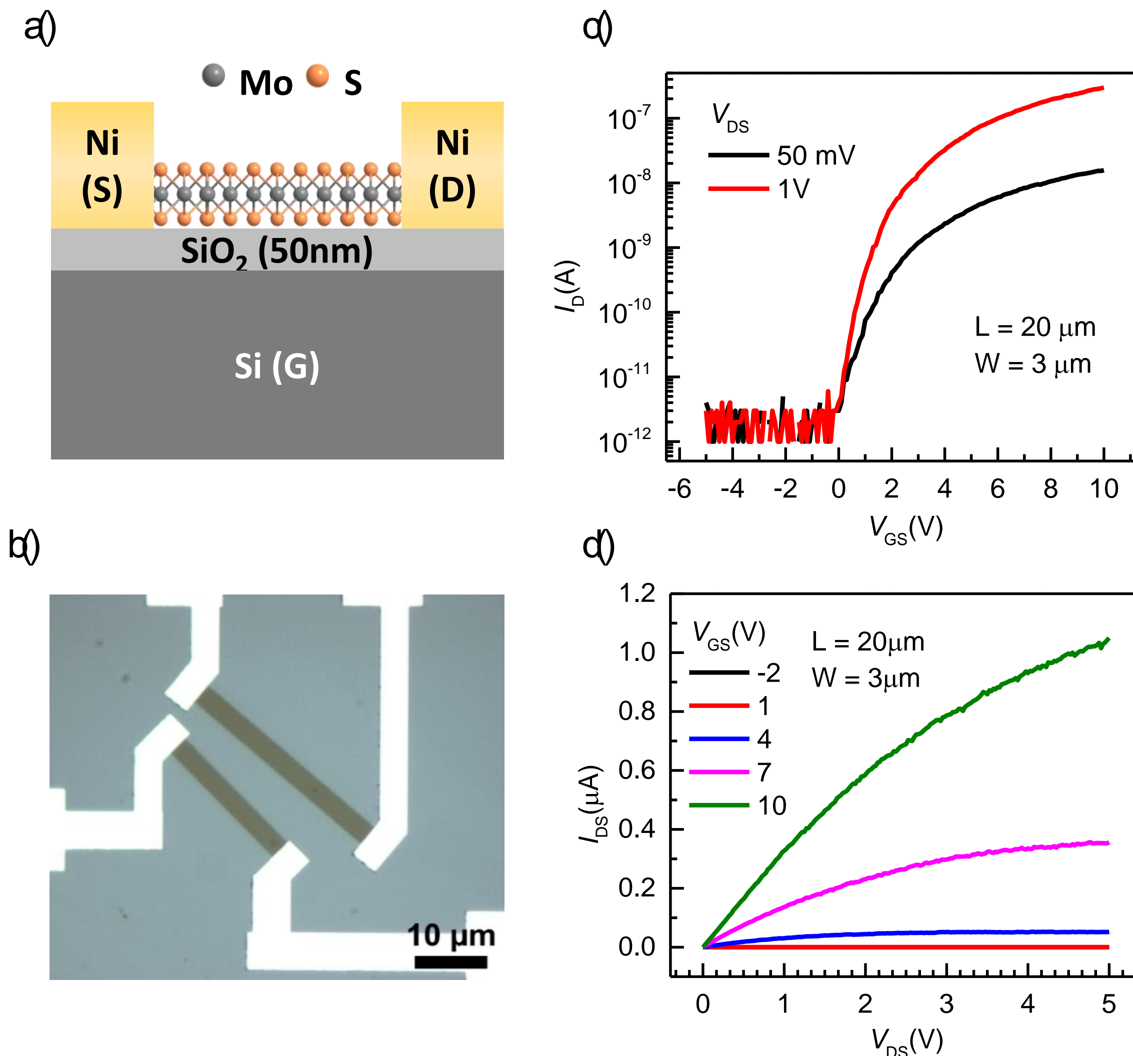

Figure5: (a) Schematic illustration of a monolayer MoS_2 back gated MOSFET (b) Representative completed device post MoS_2 patterned etching and contact formation (c-d) I_D-V_{GS} and I_D-V_{DS} data for L = 20 µm, W = 3 µm device, respectively

5.6 Experimental Section

XPS measurements:

XPS measurements were performed on a Kratos AXIS Ultra DLD spectrometer, using a monochromatic Al K-Alpha excitation source (spot size is 1mm × 2mm). Instrument work function was calibrated immediately prior to the measurement using a sputtered Au reference, utilizing the valence band Fermi edge and Au 4f position for the energy reference. Measurement of the bulk material was performed on a freshly exfoliated surface, using a slot aperture defining an area approximately 700 µm × 300 µm. Measurement of a large (approximately 50 µm × 60 µm) monolayer, exfoliated by Au exfoliation method and transferred using a dry pick-and-place method [12] to the silicon analysis substrate, was performed using the same excitation source and pass energy resolution, and the field of view was limited to approximately 400 µm × 400 µm by

tuning of the electrostatic lens and use of a small area aperture. Charge correction for the MoS_2 samples was performed using the adventitious carbon C 1s peak position [18]

Molybdenum and sulfur core level curve fits were performed using Voigt line shapes, with doublet spin orbit splitting area ratios defined to the normal 3:2 ratio for the 3d 5/2 and 3/2 components. Background subtraction was performed in combination with curve fits using the well-known Shirley background for the Au reference and MoS_2 bulk sample, and an alternative linear background for the monolayer. This alternate was necessary due to a more prominent linear background lineshape present in the Mo 3d and S 2s analysis area, likely due to substrate contributions to the spectra.

Raman and PL mapping:

High resolution PL mapping was performed using a WITec Alpha 300RA equipped with a piezo electric scanning stage. The sample was excited using the 532 nm line of a frequency-doubled Nd:YAG laser as the excitation source and focused on the sample using a 100× objective. The laser power is 2 μW with a diffraction limited spot size. QY measurement conditions are described in [15]

Sample preparation for photoluminescence quantum yield measurements:

For quantum yield measurements MoS_2 (SPI Supplies) was exfoliated on quartz (using Au exfoliation method). Monolayers were identified by optical contrast. Samples were treated using bis(trifluoromethane)sulfonimide (TFSI, Sigma-Aldrich) using the following preparation procedure: TFSI (20 mg) was dissolved in 1,2-dichloroethane (10 ml) (DCE, Sigma-Aldrich) to make a 2 mg ml^{-1} solution. The solution is further diluted with 1,2-dichlorobenzene (DCB, Sigma-Aldrich) or DCE to make a 0.2 mg ml^{-1} TFSI solution. The sample was then immersed in the 0.2 mg ml^{-1} solution in a tightly closed vial for 10 min on a hotplate (100 °C). The sample was removed and blow dried with nitrogen without rinsing and subsequently annealed at 100 °C for 5 min.

Electrical device fabrication:

Electron beam lithography is used to pattern an etch mask using PMMA C4 resist (MicroChem Corp.). XeF_2 etching [19] is used to then pattern the monolayer into long strips which form the channel region of the MOSFET. The resist is removed in acetone following which the source-drain contacts are patterned using electron-beam lithography. 40nm Ni is evaporated using thermal evaporation followed by subsequent liftoff in acetone to form the contacts.

5.7 Supporting Information

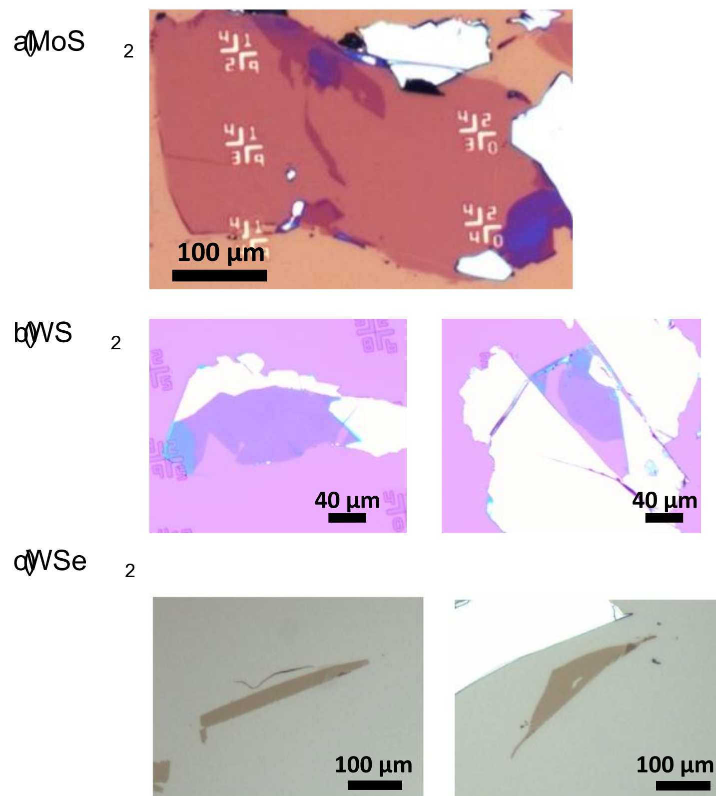

Figure S1: Optical microscope images of TMDC flakes exfoliated by Au exfoliation method (a) MoS_2 (b) WS_2 (c) WSe_2. This demonstrates the application of the Au exfoliation method to different TMDC materials. Raman and photoluminescence spectroscopy maps in Figure 3(c-f) are measured for the MoS_2 flake shown in (a).

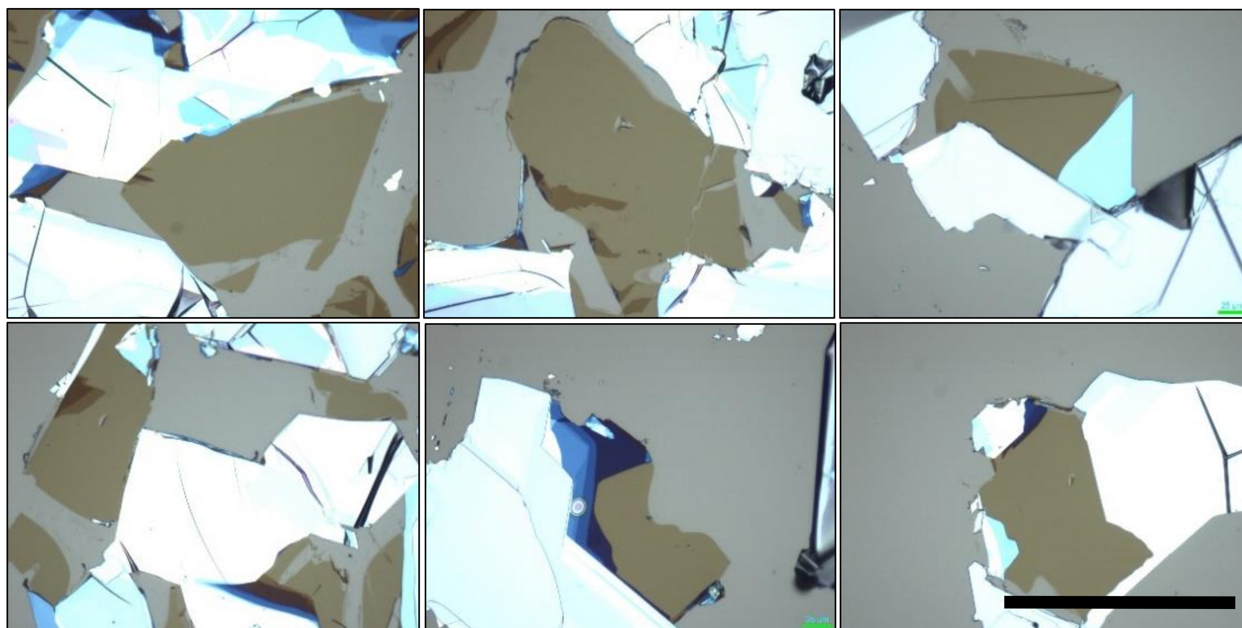

Figure S2: Optical microscope images for several large area MoS_2 flakes obtained from Au exfoliation method on 50nm SiO_2 / Si substrate. Scale bar = 200μm

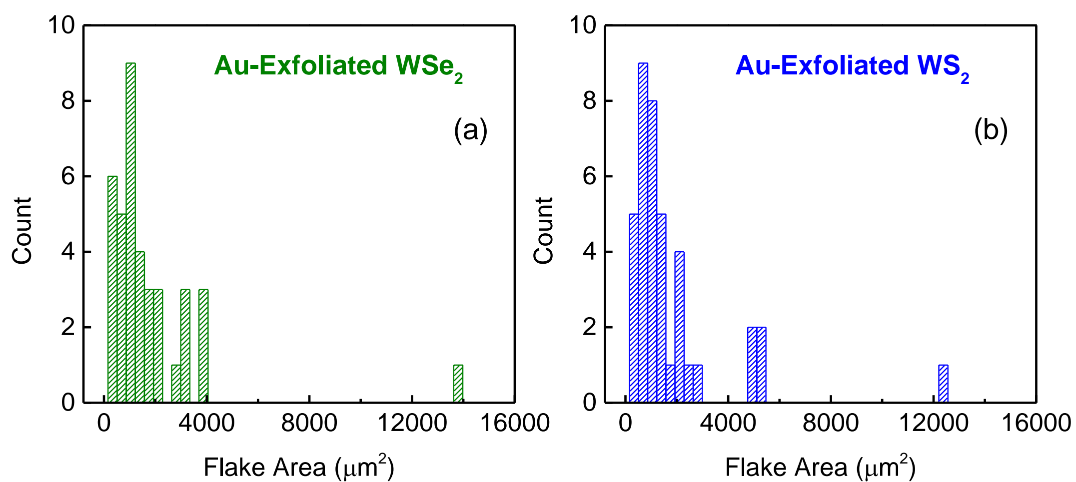

Figure S3: Histogram of flake area for gold exfoliated flakes of (a) WSe_2 and (b) WS_2. The histograms show that the gold exfoliation method can be extended easily to other TMDCs and yields flakes of similar size as MoS_2.

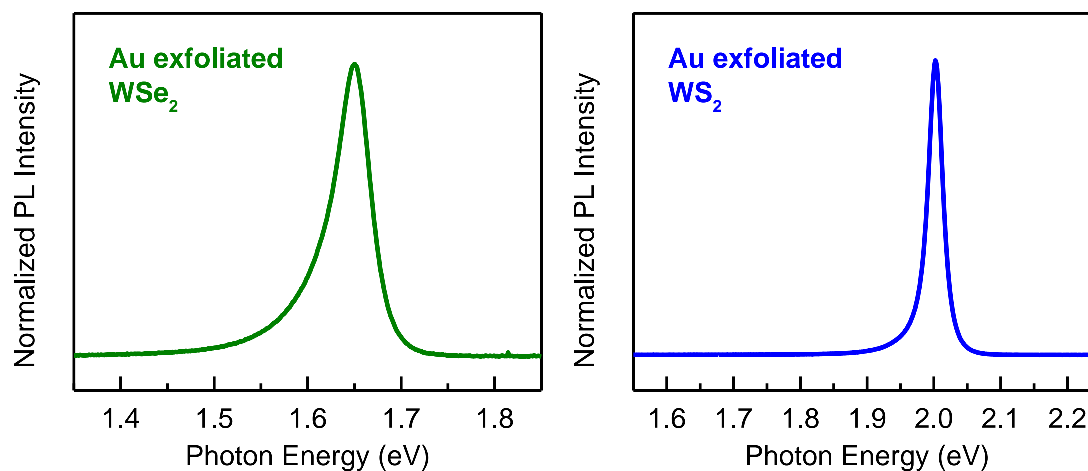

Figure S4: Photoluminescence (PL) measurements for gold exfoliated flakes of WSe_2 and WS_2. The bright PL observed from the flakes is an indicator of the quality of the flake and demonstrates the compatibility of different TMDCs with the gold etchant.

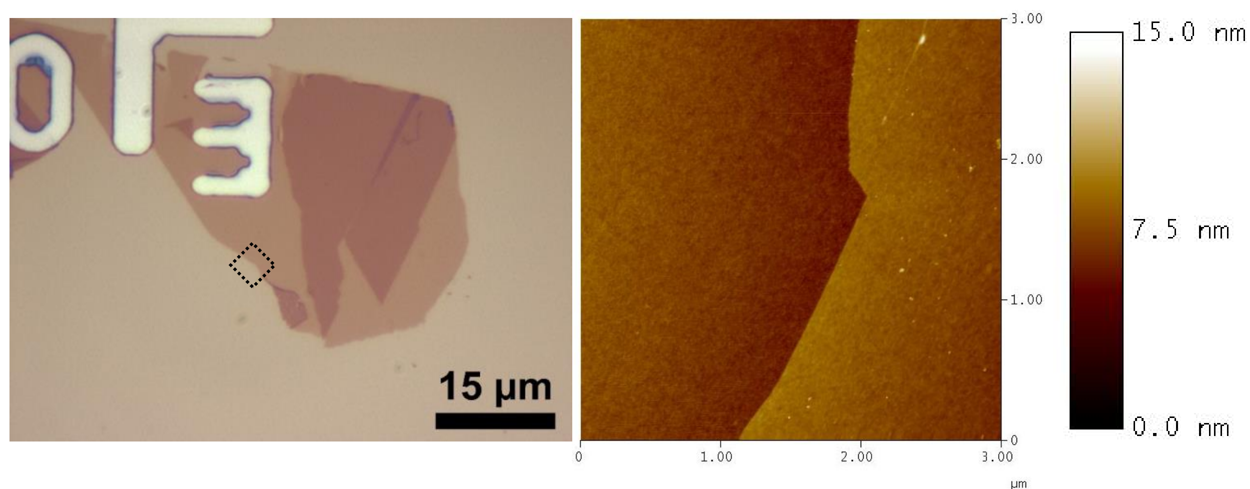

Figure S5: Optical microscope image shows the flake on which atomic force microscopy (AFM) was performed in the dotted region. The AFM image shows the morphology of the MoS_2 flake is uniform without wrinkles or folds.

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[6]Large-area and bright pulsed electroluminescence in monolayer semiconductors

6.1 Introduction

Transition metal dichalcogenides (TMDCs) such as WSe_2 and MoS_2 are semiconducting analogues of graphene, and are candidate materials for next generation optoelectronic and electronic devices[1-5]. Their unique properties include naturally terminated surfaces at the monolayer limit (~0.7 nm), which when coupled with appropriate passivation of defect sites can result in near-unity photoluminescence (PL) quantum-yield (QY)[3,6]. In addition, monolayer TMDCs display a myriad of attractive and unique physical properties including the lack of inversion symmetry, chiral light emission, and the ability to form heterostructures without the need for lattice matching[7-9]. Recent advances in the synthesis of high quality TMDCs *via* chemical vapor deposition (CVD) demonstrate their potential for scalability[10,11]. The high PL QY and sub-nanometer thickness of TMDCs can be leveraged to develop large-area, transparent and efficient light emitting devices[3,6]. However, despite their exceptional material properties, a key challenge for TMDC light emitting devices to date has been the formation of ohmic contacts to electrons and holes in the same device. Ohmic contacts in traditional light emitting diodes (LEDs) are essential to minimize resistive losses and achieve high injection levels[12]. In previous works, steady-state electroluminescence (EL) was obtained in TMDCs using *p-n* junctions formed *via* electrostatic or chemical doping[13-15]. More recently, EL from complex quantum well heterostructures utilizing graphene with hexagonal boron-nitride tunnel barriers has been demonstrated[16,17]. However, the lack of suitable bipolar ohmic contacts remains to be a significant issue, ultimately limiting the performance of TMDC light emitting devices[1].

Inspired by the first electroluminescent device, the light-emitting-capacitor[18-21], we achieve efficient bipolar carrier injection and light emission in TMDCs *via* transient mode operation using a single metal-semiconductor contact (source). In this two-terminal device, the source is grounded and an AC voltage is applied to the gate electrode. Alternating electron and hole populations are injected into the monolayer TMDC from the source contact. Notably, the carrier injection is weakly dependent on the Schottky barrier height (φ_B) (*i.e.* polarity of the contact) because of the large tunneling currents present at the source during the gate voltage (V_g) transients. The transient-electroluminescent (t-EL) device achieves bright EL at high injection levels. We demonstrate a millimeter scale device with bright EL (peak power of 193 μW cm^{-2}) from a ~0.7 nm thick monolayer in ambient room lighting. Finally, we show a large area device fabricated on a quartz substrate, which is transparent in the off-state by using indium tin oxide (ITO) electrodes.

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6.2 Operation and device structure of the t-EL device.

Figure 1a shows a schematic of the t-EL device, consisting of a monolayer TMDC on a heavily doped silicon substrate (gate) with a 50 nm thick SiO_2 layer as the gate oxide. The TMDC is contacted with one metal electrode (source), and a bipolar square wave is applied between the gate and source. As shown in Fig. 1b, EL is only observed near the source contacts and the emission region laterally extends from the contact edge by ~3 μm (Supplementary Fig. 1). We fabricated devices based on four of the most heavily studied monolayer TMDCs by employing this generic device structure, specifically: WS_2, MoS_2, WSe_2 and $MoSe_2$[22,23]. All four of the studied materials show EL, with the spectral emission shape closely matching their respective PL (Fig. 1c).

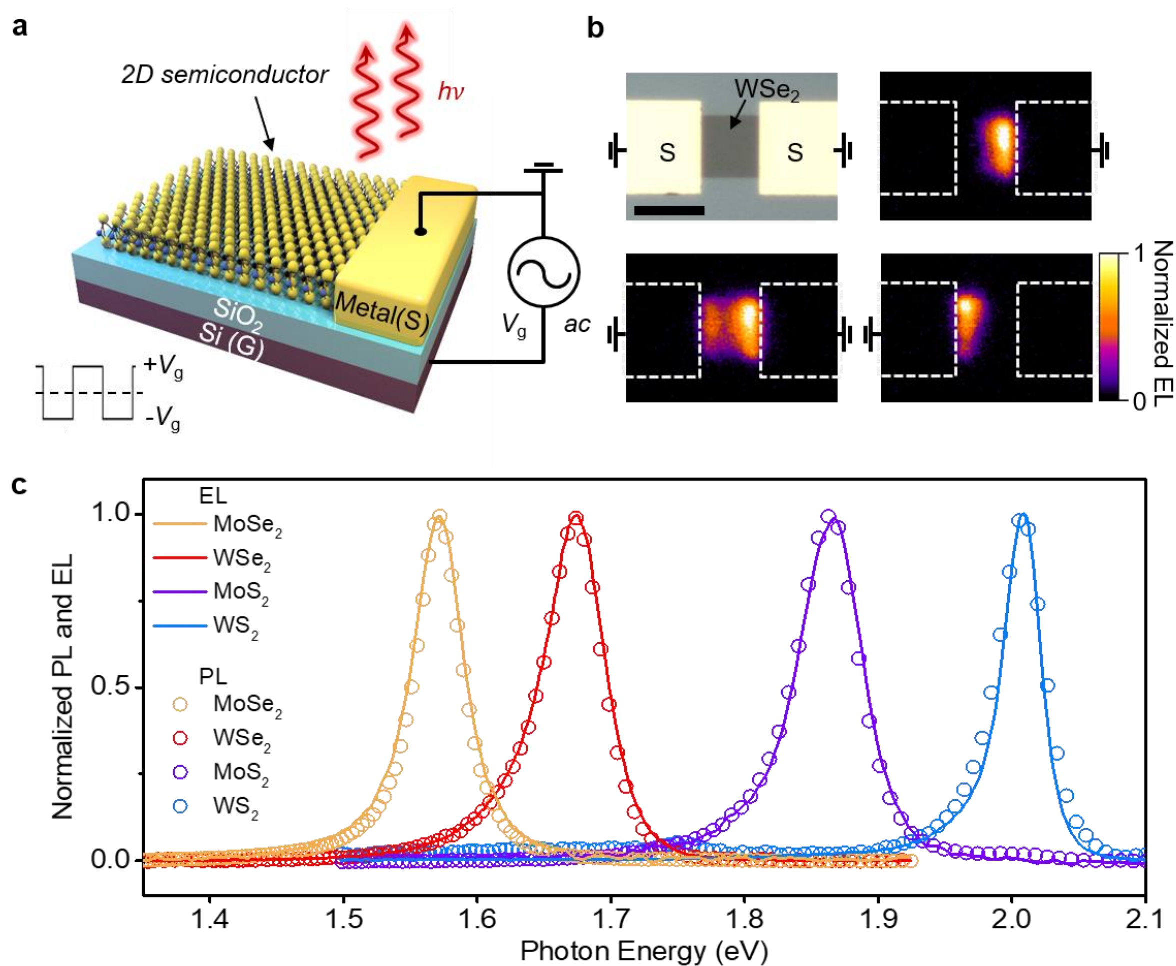


Fig. 1 Transient EL in TMDCs. **a** Schematic of the t-EL device. An AC voltage is applied between the gate and source electrodes and emission occurs near the source contact edge. **b** Optical and EL image of a WSe_2 device, showing that emission is only observed near the grounded source contacts. Scale bar is 10 μm. **c** EL and PL spectra measured for $MoSe_2$, WSe_2, MoS_2 and WS_2 monolayer devices.

6.3 Carrier injection and light emission mechanism.

We performed time-resolved electroluminescence (TREL) measurements to understand the dynamic performance and the mechanism of light emission in the t-EL device. The measured TREL from a WSe_2 device and the corresponding V_g square wave are shown in Fig. 2a and Supplementary Fig. 2 (the operation mechanism is also depicted in Supplementary Video 1). Pulsed EL is observed at each V_g transition and has a full width half maximum of 8 ns. EL emission in the device increases linearly with frequency (f) as shown in Supplementary Fig. 3 and Supplementary Note 2, with no changes in spectral shape. Note that the EL is stable with a variation (~±25%) in intensity over time (Supplementary Fig. 4). The emission mechanism can be elucidated from the sequence of energy band diagrams (simulated *via* Sentaurus TCAD) shown in Fig. 2b, Supplementary Fig. 5 and 6 as well as the carrier densities and radiative recombination rate shown in Fig. 2c. When V_g is held at -6 V, the hole density in the semiconductor is large and approaches its steady-state value ($p_0 \sim 1.9\times10^{12}$ cm^{-2}). When V_g is switched to +6 V the field across the capacitive component of the device (*i.e.* SiO_2 gate dielectric) cannot change instantaneously. As a result, the applied voltage is dropped across the resistive parts of the device including the semiconductor and the source contact, but is dominated by the latter. The large voltage drop and the steep energy band bending at the Schottky contact lead to large transient tunneling currents. Injected electrons diffuse inward while holes exit the semiconductor through the contact or recombine with incoming electrons. Thus, the hole density shows a continuous decrease whereas the electron density in the semiconductor increases until it reaches its steady-state value ($n_0 \sim 1.9\times10^{12}$ cm^{-2}). At steady-state, the band bending in the semiconductor and at the contact decreases (Supplementary Fig. 5 and 6) and the tunneling currents subside. The excess electron and hole populations simultaneously present (large quasi-Fermi level splitting) during the AC transient result in pulsed light emission. Similarly, this mechanism can also explain the emission from the device during a -6 V to +6 V V_g transient. The large transient tunneling currents in the t-EL device allow for efficient modulation of the carrier densities in the semiconductor, surmounting the large Schottky barriers typically associated with non-ohmic contacts to TMDCs. Simulated transient currents are shown in Supplementary Fig. 7 and the various current components present are discussed in detail in the Supplementary Note 3.

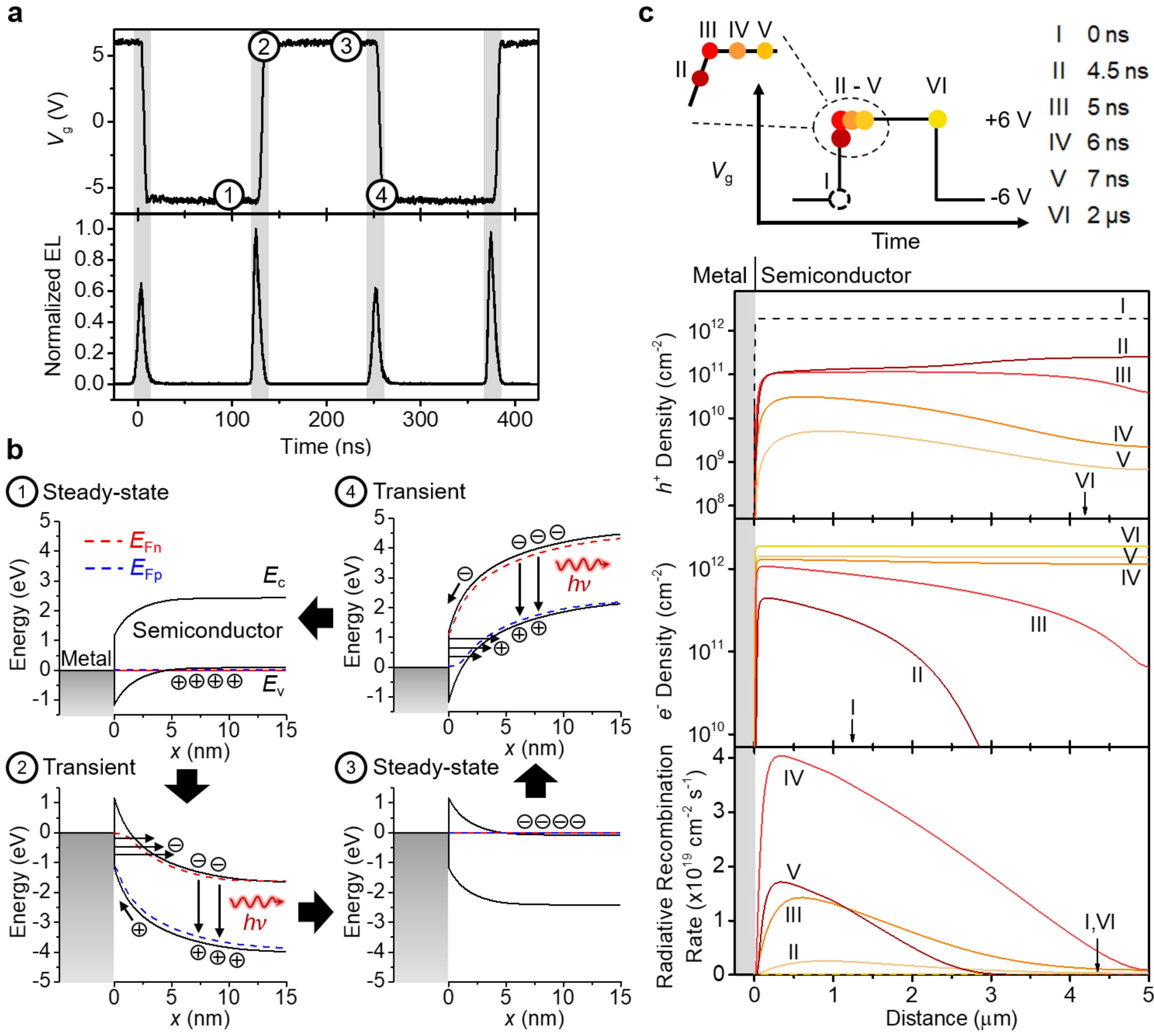


Fig. 2 Operation mechanism. **a** Time-resolved electroluminescence and the corresponding V_g, showing that EL occurs at the V_g transients (time points 2 and 4). **b** Band diagrams at different times during the operation cycle, corresponding to panel A. E_{Fn} and E_{Fp} indicate the quasi-Fermi levels for electrons and holes respectively. **c** V_g pulse applied to the simulated device and the corresponding electron/hole density and radiative recombination rate. Simulations were performed for material parameters corresponding to WSe_2 using a 50 nm thick gate oxide and $V_g = \pm 6$ V (simulated band diagrams are also shown in Supplementary Fig. 5 and 6).

6.4 Schottky barrier height and gate-voltage dependence.

The impact of φ_B on transient carrier injection and light emission is further studied by fabricating WSe_2 devices with electrodes prepared by sputtering (ITO), thermal evaporation (Au, Ag, Ni, MoO_x), as well as transferred van der Waals few-layer graphene contacts. The different contacts result in ~3 orders of magnitude variation in the on-current when the device is configured as a transistor (Supplementary Fig. 8). However, the corresponding t-EL devices show a maximum variation in the integrated emission intensity of only ~4× as shown in Fig. 3a (error bars indicate

standard deviation of EL intensity measured from five or more different devices). WSe_2 transistor characteristics for Ag, Ni and graphene contracts are shown in Fig 3b. TCAD simulations similarly show negligible difference in integrated EL for varying φ_B over the range of ohmic ($\varphi_B = 0.05$ eV) to mid-gap ($\varphi_B = E_g/2$) (Supplementary Fig. 9). The relative intensity of emission during the two V_g transients, however, does vary for devices with varying φ_B. As shown in the TREL of a hole selective contact device (Supplementary Fig. 10), the EL intensity at $+V_g$ to $-V_g$ transient is stronger than the other transient. This is consistent with simulation results (Supplementary Fig. 11) and discussed in the Supplementary Note 4. In addition to the effect of φ_B, we also studied the dependence of EL on varying V_g (Fig. 3c and Supplementary Fig. 12). EL is observed from the device when V_g is greater than the turn-on voltage (V_t), whose precise value is dependent on the bandgap (E_g) of the material and parasitic resistances in the device. We experimentally observe a higher V_t for WS_2 (4.1 V) as compared to WSe_2 (2.0 V) which is qualitatively consistent with the larger E_g of WS_2[24].

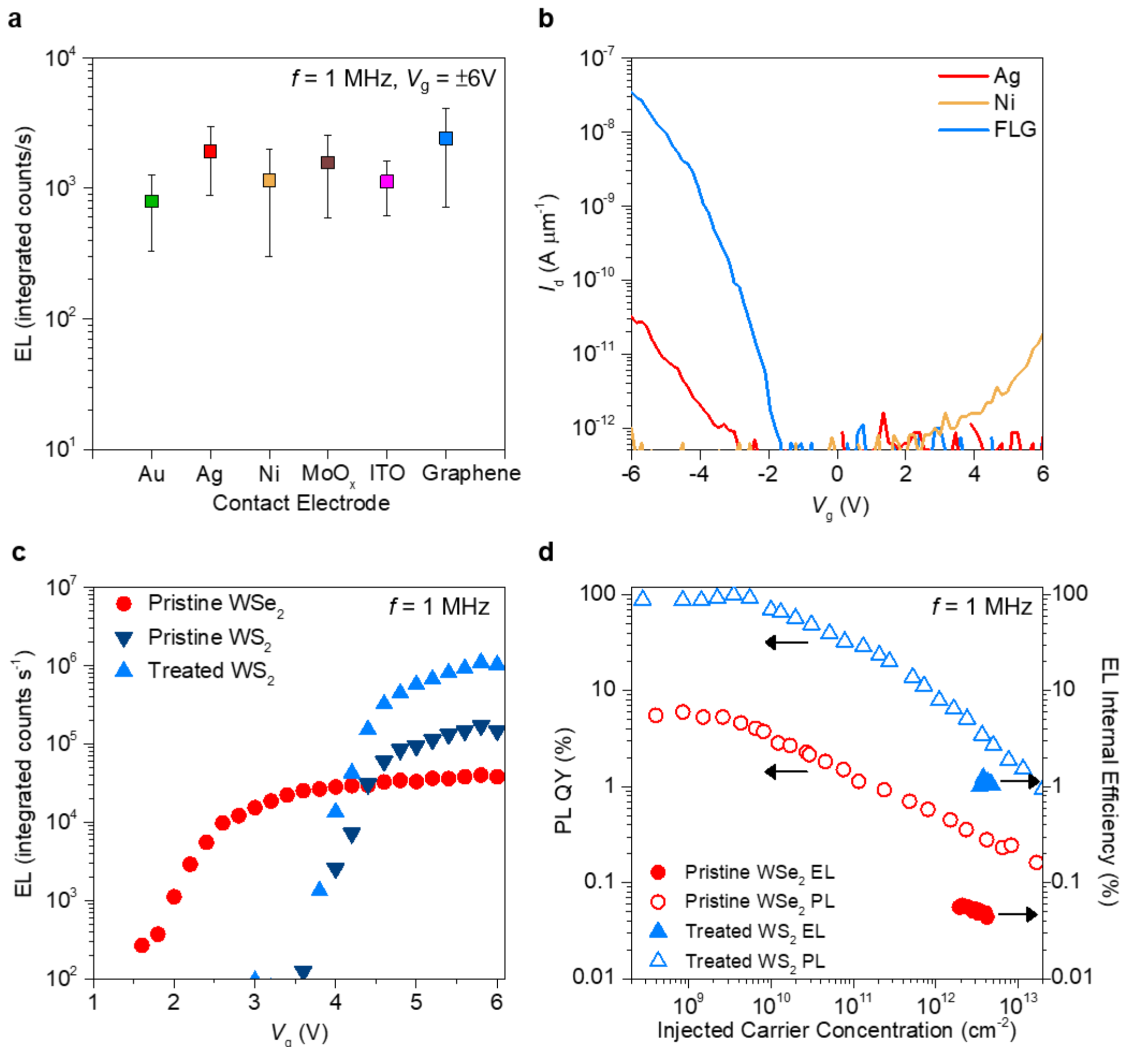


Fig. 3 Contact and voltage dependence. **a** EL from WSe_2 devices fabricated using various source contacts. Error bars indicate standard deviation of EL intensity measured from five or more different devices. **b** I_d-V_g characteristics of WSe_2 devices contacted by Ag, Ni and few-layer

graphene source electrodes. **c** Voltage dependence of EL for WSe_2 and WS_2 devices (WS_2 before and after superacid treatment). **d** PL QY and EL internal efficiency measured for a WSe_2 device and a superacid-treated WS_2 device as a function of injected carrier concentration.

The efficiency in traditional light emitting devices is defined as the number of emitted photons over the total current. However, for the t-EL device, transient current measurement is challenging due to device and measurement setup parasitic capacitances as well as the high slew rate (1.6 V ns^{-1}) of the V_g square wave. Given this limitation, we define EL internal efficiency (η_i) based on the total steady-state carrier concentration, which represents the maximum number of carriers which can undergo radiative recombination in a given V_g cycle. The efficiency is thus defined as: $\eta_i = \frac{\text{photons/cycle}}{(n_o+p_o)\times\text{Area}}$ (Supplementary Equation 6). The sum of the steady-state concentrations, (n_0+p_0) is given by $C_g(2V_g\text{-}E_g\, q^{-1})q^{-1}$ (Supplementary Equation 7). Here, n_0 and p_0 are the steady-state electron and hole concentrations corresponding to a positive and negative V_g respectively, C_g (69.1 nF cm^{-2} for 50 nm SiO_2 gate oxide) is the areal gate capacitance and q is the elementary charge. The analytical value of n_0+p_0 closely matches that from simulations at sufficiently high V_g (Fig. 2c and Supplementary Fig. 13). η_i approaches 100% for the case where the PL QY is unity and all the steady-state carriers present in the device undergo recombination during a V_g transient. In practice, PL QY may not be 100%, and only a fraction of the steady-state carriers will undergo recombination in the semiconductor, while the remainder exit through the contact due to the finite slew rate of the AC source. Further details on the efficiency calculation are provided in the Supplementary Note 6.

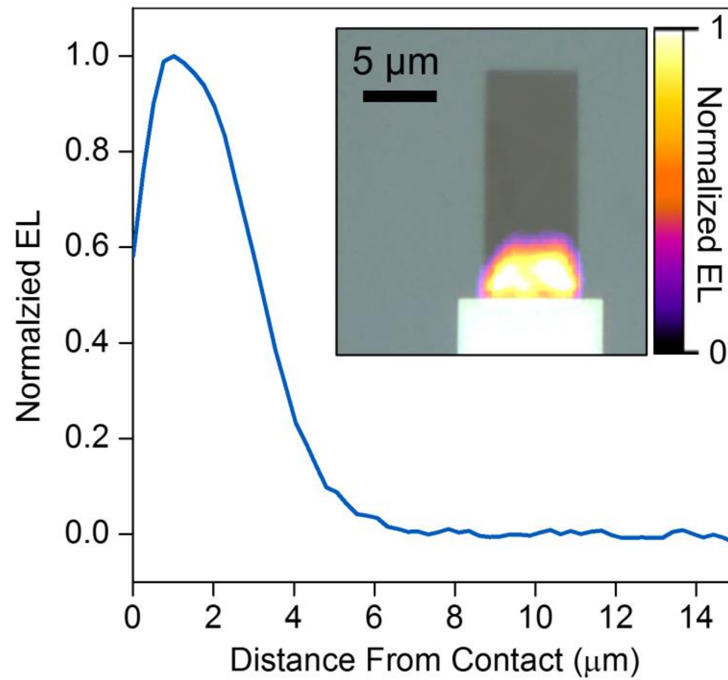
The WSe_2 t-EL device at $n_0+p_0 = 2.1\times10^{12}$ cm^{-2} (calculated from Supplementary Equation 7 for V_g = 3.2 V and E_g = 2.34 eV) has an EL external efficiency (η_e) of 0.01% (Supplementary Fig. 14)[24]. The η_i of this device is extracted from η_e by considering the escape cone and optical interference from the Si substrate with a 50 nm SiO_2 layer[3,25]. Using this method, we calculate η_i of ~0.06%. To contrast the performance of the t-EL device relative to the PL QY of the material, the steady-state and quasi-steady-state PL are measured using a continuous-wave and pulsed laser respectively (Fig. 3d, Supplementary Note 1 and Supplementary Fig. 15). The droop observed in PL QY at high injection levels has been previously attributed to biexcitonic recombination in 2D semiconductors[3,6]. The calculated η_i for WSe_2 ~ 0.06% has an upper bound equal to the PL QY of the material (~ 0.3%) (Fig. 3d). The efficiency of the device can be improved by utilizing a material with a high PL QY. We fabricated WS_2 devices where the semiconductor surface is passivated using a non-oxidizing organic superacid: bis(trifluoromethane)sulfonimide, which has been shown to enhance the PL QY at low injection levels (< 10^9 cm^{-2}) to > 95%[3,6]. In this superacid-treated device, we obtain a peak η_e of ~0.27% at n_0+p_0 ~3.8×10^{12} cm^{-2} (calculated from Supplementary Equation 7 for V_g = 5.8 V and E_g = 2.88 eV), corresponding to η_i ~1.2% (the EL for this device before and after treatment are shown in Supplementary Fig. 16)[24]. We note that the η_i is still significantly limited by the PL QY droop at high injection levels (3.4%) (Fig. 3c and Supplementary Fig. 17). The effect of biexcitonic recombination on the PL QY is shown in Supplementary Fig. 18. This indicates that for pump levels in the range of 10^{12} cm^{-2}, WS_2 which has a C_{bx} of ~0.1 cm^2 s^{-1}, η_e can be improved to ~40% by sufficiently lowering C_{bx}. The next phase for improving the efficiency involves engineering the radiative lifetime and biexcitonic recombination rate by properly selecting the substrate and/or top coating. Similar efforts are made in III-V thin film devices, where the radiative recombination rate is highly dependent on the optical mode density and refractive index of the medium[26].

In summary, we have demonstrated bright EL at high injection levels using transient mode operation *via* a simple dopant-free device which does not require complex heterostructures to achieve light emission. EL from this device is weakly dependent on the Schottky barrier height or polarity. The transient EL concept demonstrated in this work can be extended to large bandgap materials in the future, for which achieving ohmic contacts to both carrier types is particularly challenging. We show that this device structure can be scaled-up to obtain light emission on millimeter length scales. The ability to realize large-scale light emission from monolayer semiconductors opens numerous potential opportunities in the field of 2D materials and can lead to the realization of transparent displays. Our results also suggest that the main factors limiting the performance of the t-EL device is PL QY droop due to biexcitonic recombination. The device performance can be further improved through engineering of the optical medium[3,25]. Finally, unlike traditional LEDs, the exposed light emitting surface of these devices also permits for the direct integration of plasmonic structures, nano-antennas, and photonic crystals, which could allow for the fabrication of high-speed devices or the development of electrically pumped 2D lasers[27-29].

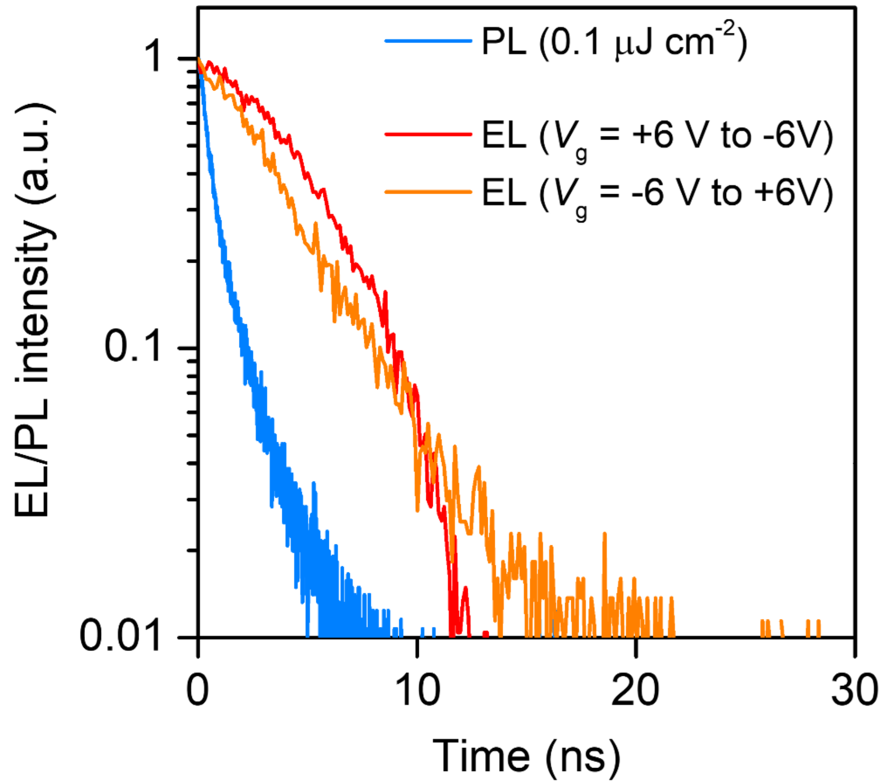
6.5 Device Simulations

Simulations were performed in Sentaurus TCAD, where the device structure consists of a monolayer of WSe_2, with the following material parameters used: E_g = 2.34 eV, $\varepsilon = 4\varepsilon_0$, $\mu_n = \mu_p$ = 100 $cm^2V^{-1}s^{-1}$, $\tau_{n,SRH} = \tau_{p,SRH}$ = 2.5 ns, $m_e^* = m_h^*$ = 0.345 m_0 and a SiO_2 gate oxide thickness of 50 nm. A non-local tunneling model accounts for the dependence of tunneling currents at the metal-semiconductor contact. Simulation snapshots record the transient device characteristics, recombination rates and carrier densities, at several different instances, immediately before, during and after a V_g pulse edge. The slew rate of the gate voltage pulse used in the transient simulations is 2.4 V ns^{-1}. For simulations shown in Fig. 2, Supplementary Fig. 5, 6, and 13 ambipolar contacts ($\varphi_{Bn} = \varphi_{Bp} = E_g/2$) were used. The recombination models employed here are based on free carriers and material properties for GaAs were used for all parameters not specified above; however, the simulation adequately captures the physics of device operation and light emission qualitatively. For accurate quantitative analysis of this device, first-principle calculations and inclusion of the exciton physics of 2D materials are needed.

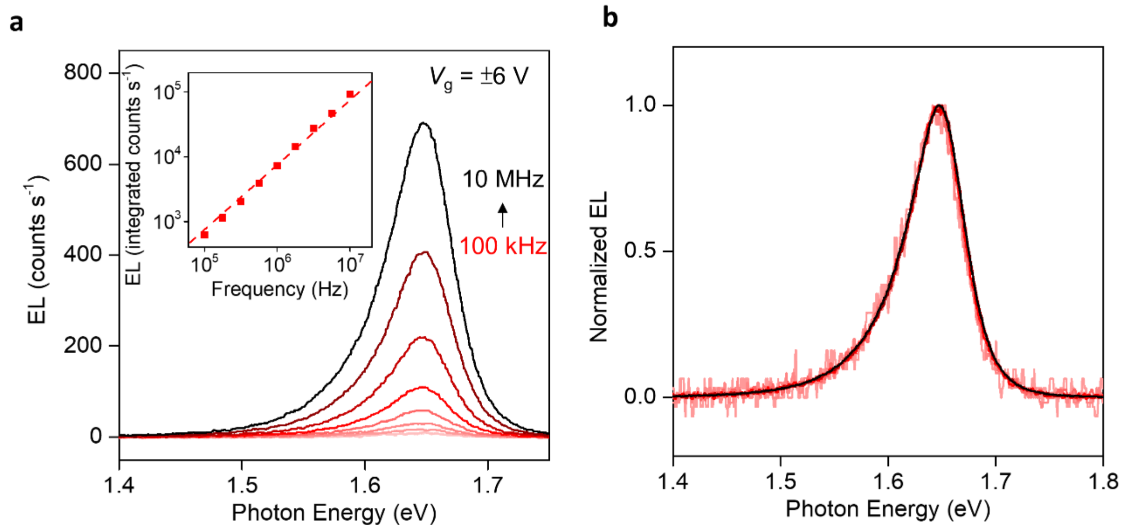
6.6 Supplementary Figures



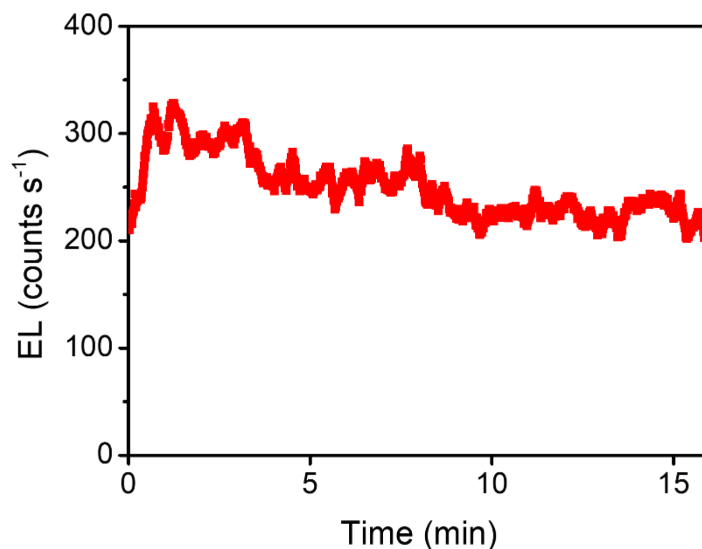
Supplementary Figure 1 | Spatial profile of EL. Spatial profile of EL intensity for a WSe_2 t-EL device fabricated with a single source contact. Inset shows superimposed optical and EL image. Measurement was taken with $V_g = \pm 9$V at a frequency of 1 MHz. The EL peak is ~1 μm from the contact edge with a FWHM of ~3.3 μm; note that the experimental values are limited by the resolution of the optical system (~500 nm).



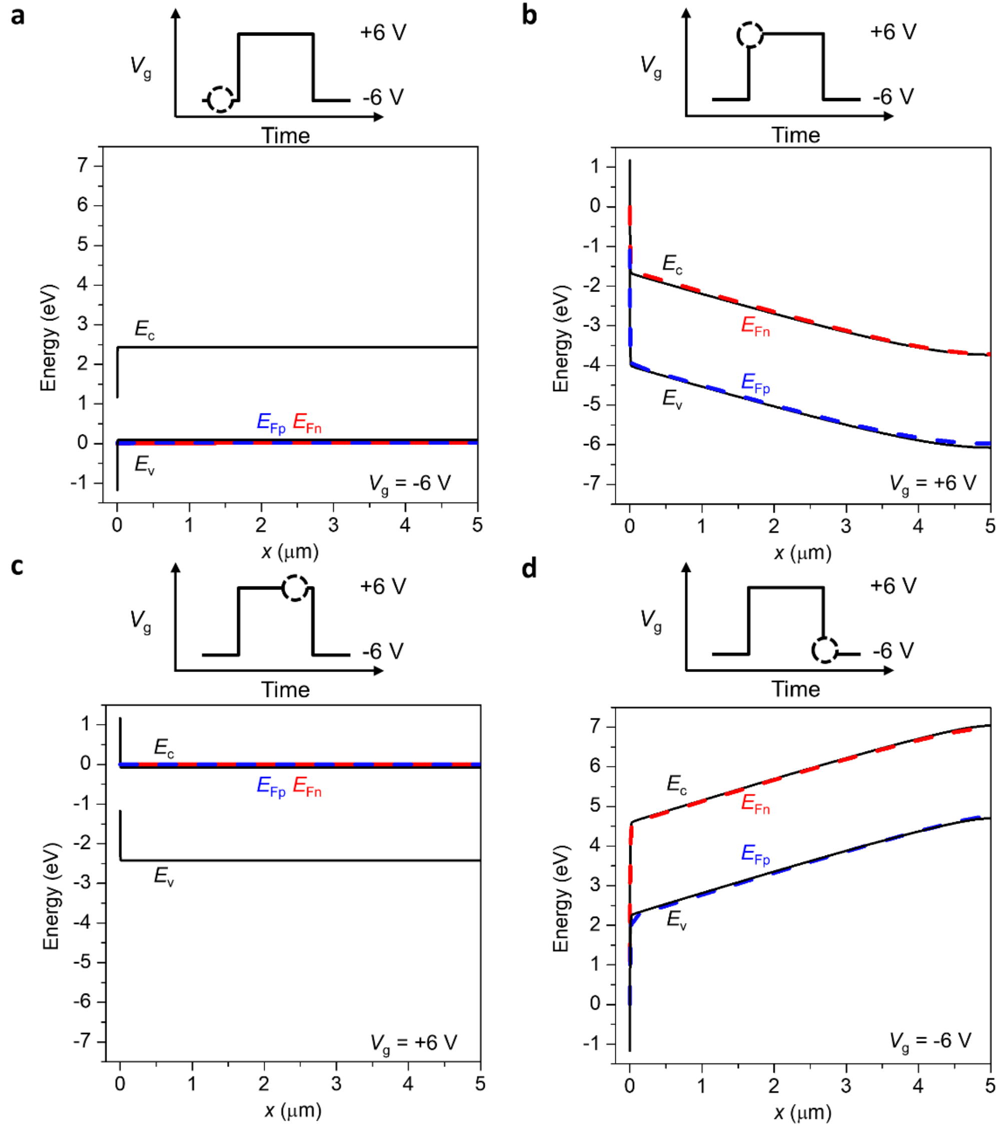
Supplementary Figure 2 | TRPL and TREL decay. Time resolved PL decay measured at an injection level of 0.1 μJ cm^{-2} and time resolved EL decay measured at gate transitions of V_g = +6 V to -6 V and V_g = -6 V to +6 V.



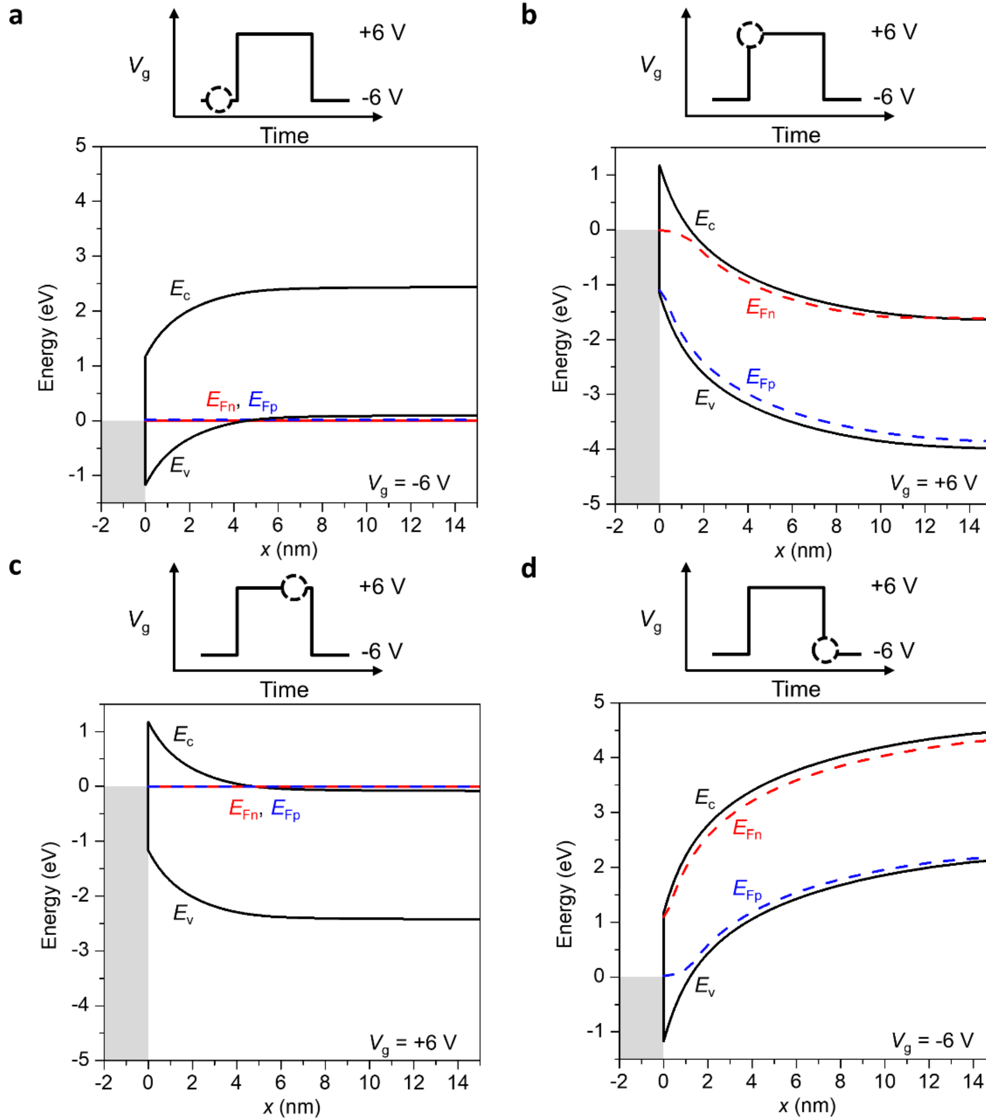
Supplementary Figure 3 | Frequency dependence. (a) EL spectra of a WSe_2 device operated at gate frequencies ranging from 100 kHz to 10 MHz. Inset shows integrated EL counts per cycle as a function of operating frequency. The superlinar increases EL versus frequency is attributed to time dependent variation in the device (Supplementary Fig. 4). **(b)** Normalized EL spectra of Supplementary Fig. 3a.



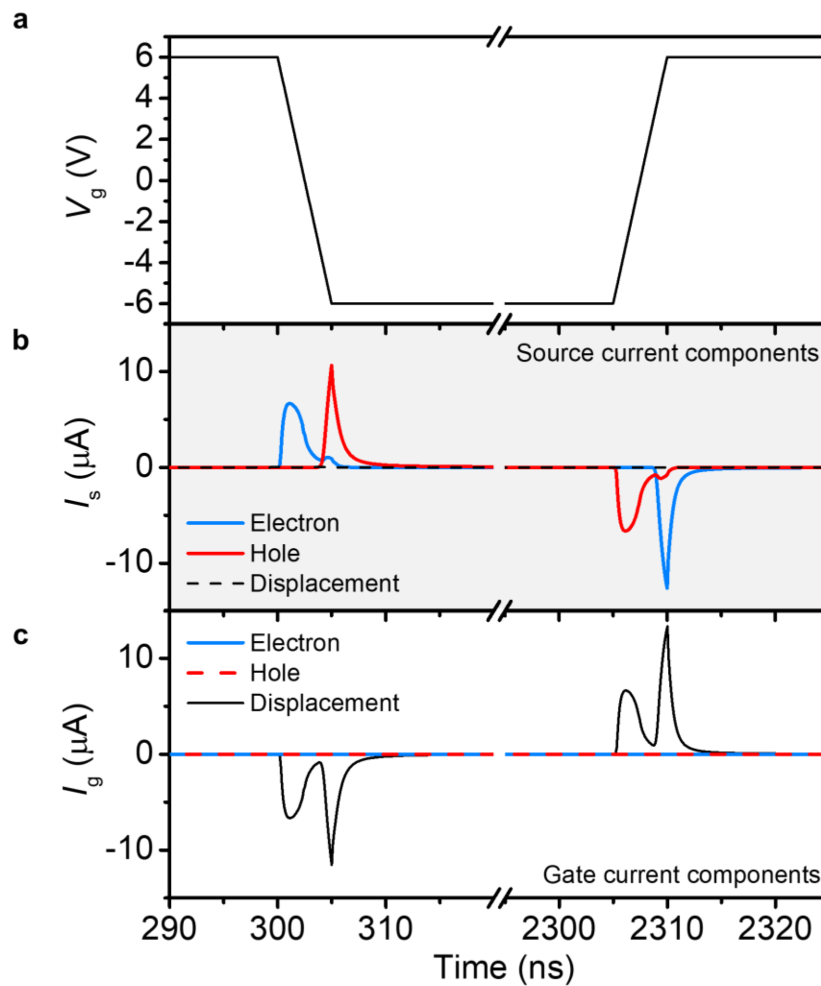
Supplementary Figure 4 | Device stability. EL counts measured for a WSe_2 device operated for fifteen minutes in ambient with no encapsulation. The device shows a maximum variation of 50% over the full operation time.



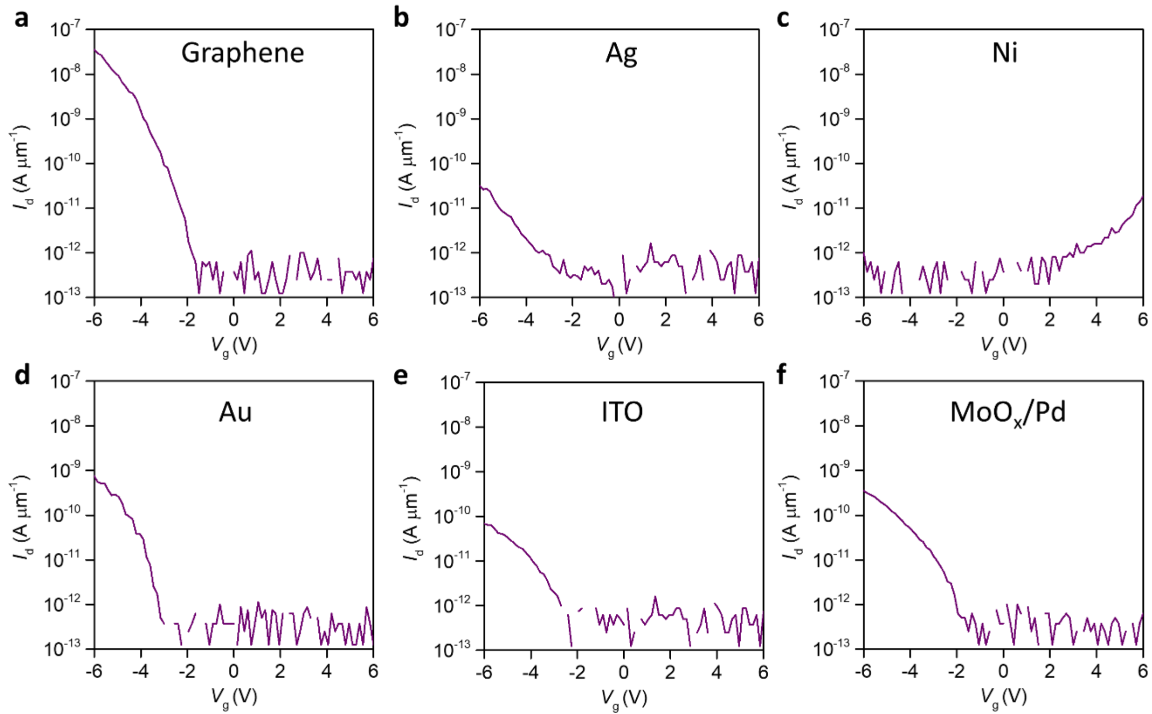
Supplementary Figure 5 | Simulated band diagrams. **(a)** Band diagram at V_g = -6 V, immediately before V_g transient. **(b)** Band diagram immediately after switching bias to V_g = +6 V. **(c)** Band diagram at V_g = +6 V, immediately before V_g transient. **(d)** Band diagram immediately after switching bias to V_g = -6 V. Simulations were performed for material parameters corresponding to WSe_2, further details are provided in the methods.



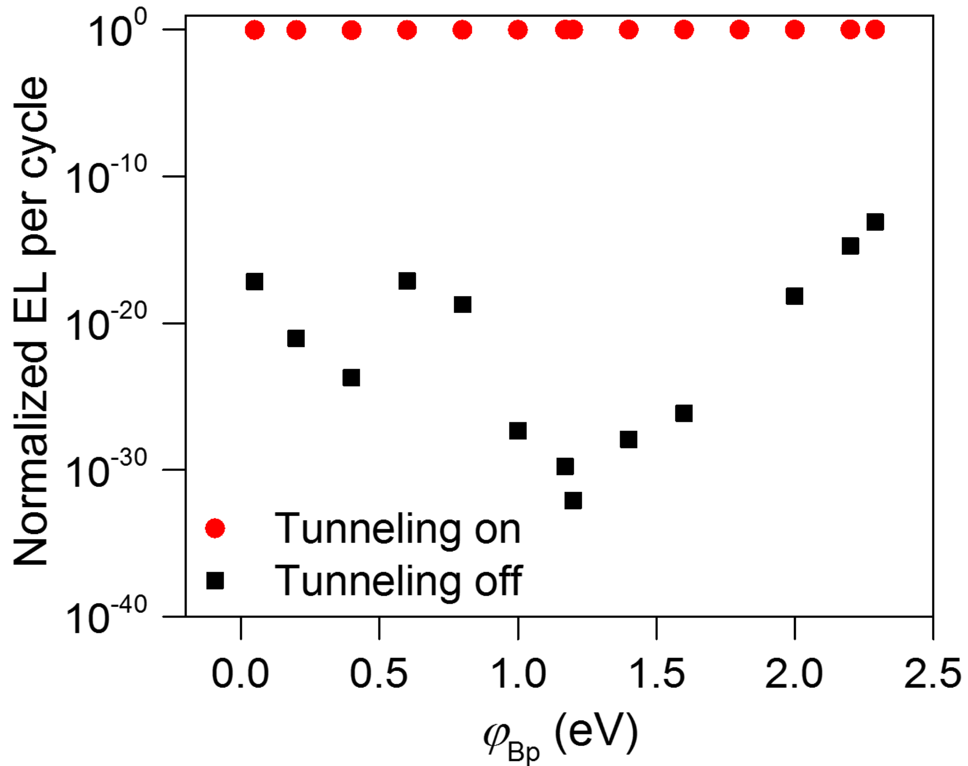
Supplementary Figure 6 | Simulated band diagrams near the contact edge. Data shown here is from Supplementary Fig. 5, expanded near the Schottky contact for clarity. **(a)** Band diagram at V_g = -6 V, immediately before V_g transient. **(b)** Band diagram immediately after switching bias to V_g = +6 V. **(c)** Band diagram at V_g = +6 V, immediately before V_g transient. **(d)** Band diagram immediately after switching bias to V_g = -6 V. Simulations were performed for material parameters corresponding to WSe_2, further details are provided in the methods.



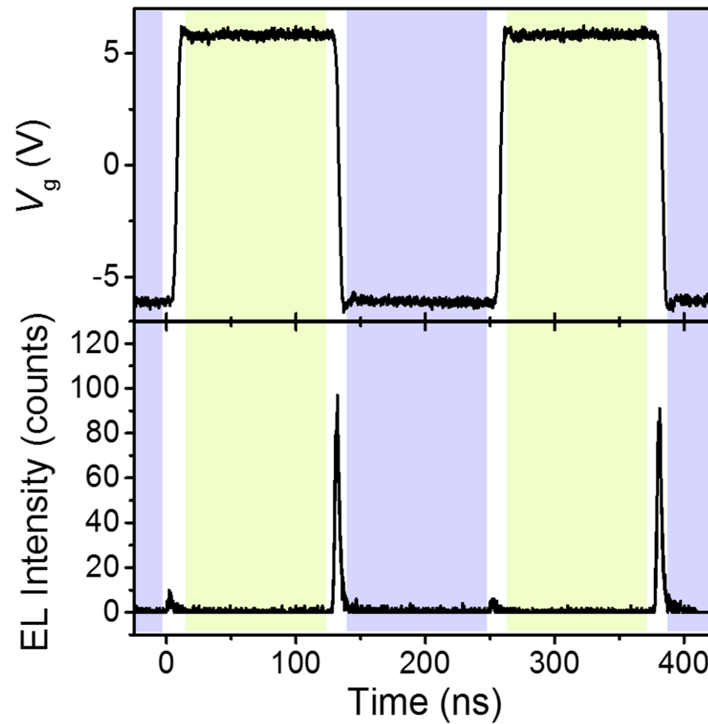
Supplementary Figure 7 | Transient current components. **(a)** V_g as a function of time. Corresponding source (I_s) and gate (I_g) currents are shown in **(b)** and **(c)**, respectively. I_s is dominated by electron and hole components, while the displacement current is relatively negligible. I_g is dominated by the displacement current. Simulations were performed for material parameters corresponding to WSe_2, further details are provided in the methods.



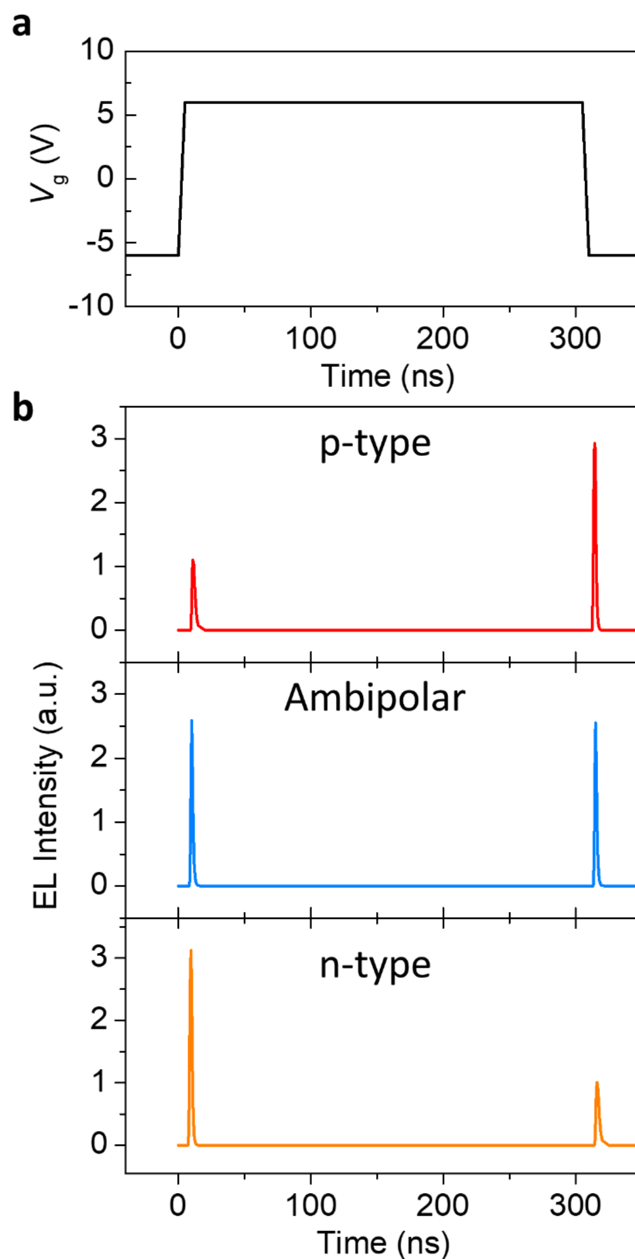
Supplementary Figure 8 | I_d-V_g characteristics of WSe_2 devices with various contacts. I_d-V_g characteristics of representative WSe_2 devices shown in Fig. 3a, fabricated with **(a)** transferred few-layer graphene (FLG) contacts, **(b)** thermally evaporated Ag, **(c)** thermally evaporated Ni, **(d)** thermally evaporated Au **(e)** sputtered ITO, and **(f)** thermally evaporated MoO_x/Pd[1]. $|V_{ds}| = 1$ V for all cases.



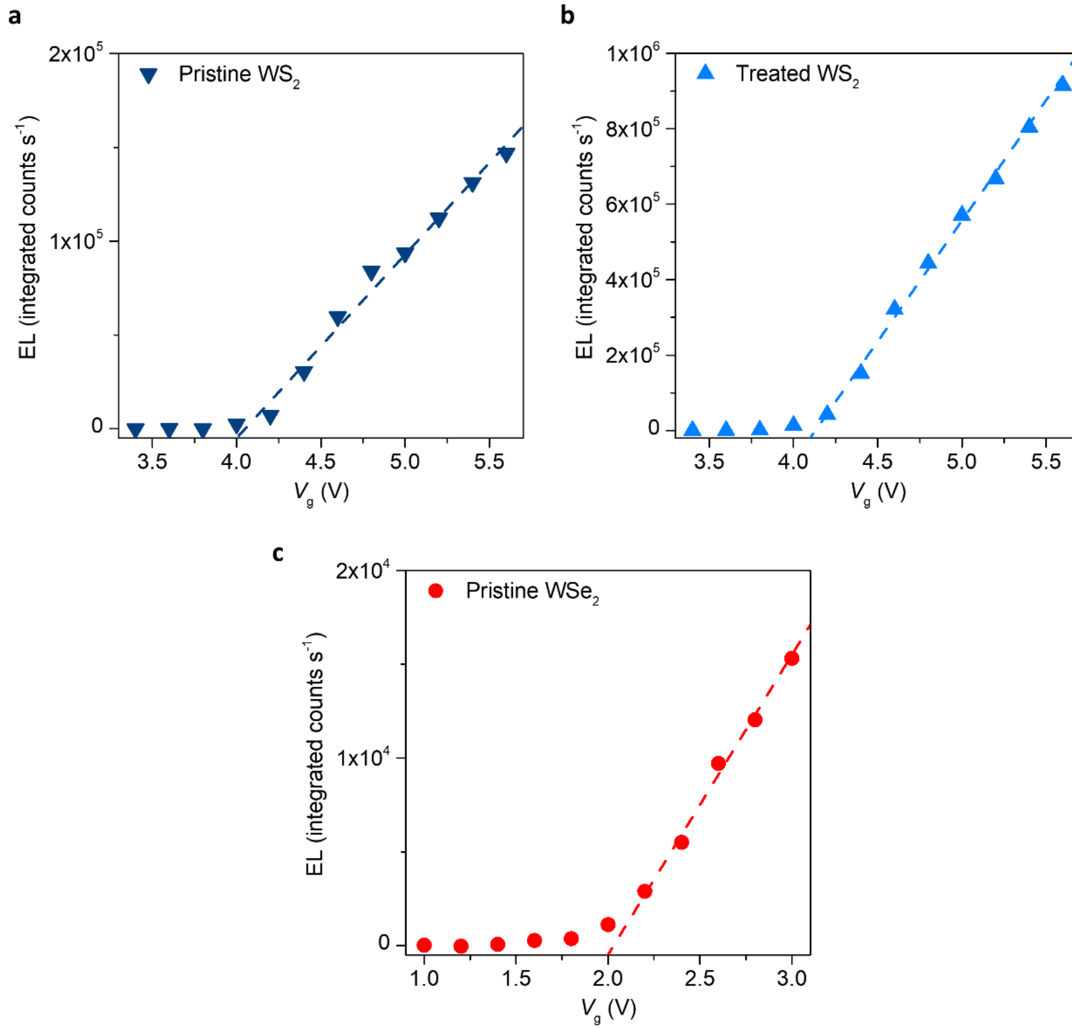
Supplementary Figure 9 | Dependence of EL on Schottky barrier height. Simulated EL integrated per gate cycle for a device where the Schottky barrier height is varied (note that φ_{Bn} + φ_{Bp} = E_g). Simulations were performed in the case where tunneling was allowed (red circles) and unaccounted for (black squares). Simulated EL shows negligible dependence on the Schottky barrier height when we account for the tunneling current. The integrated EL intensity for the case where the tunneling model is off is orders of magnitude lower and is dependent on the Schottky barrier height and several simulation parameters such as gate work function, which was assumed to be 5.1 eV. Simulations were performed for material parameters corresponding to WSe_2, further details are provided in the methods.



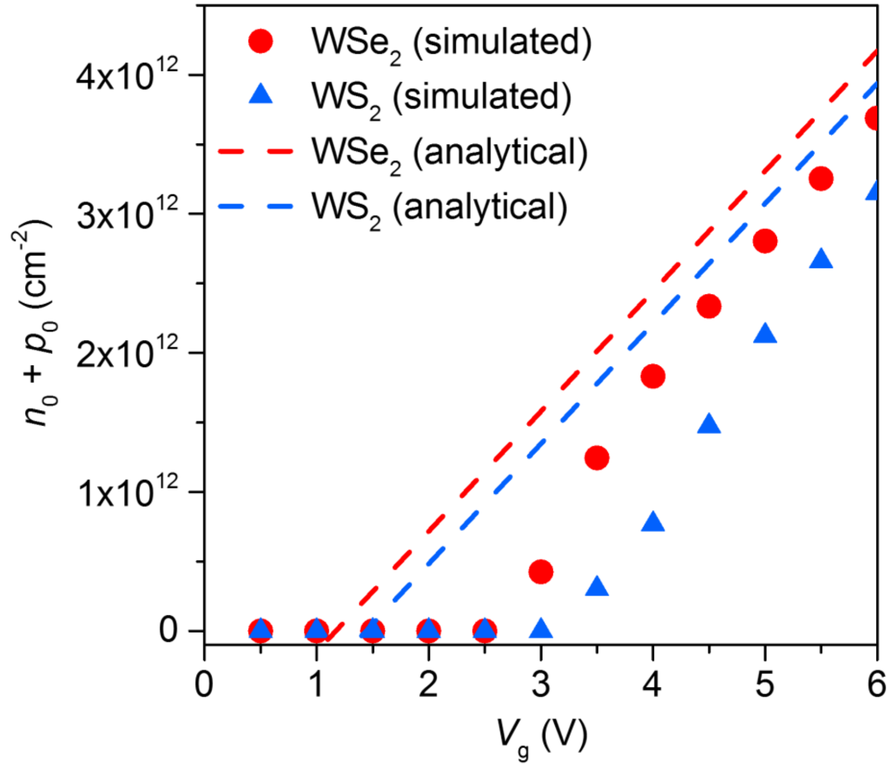
Supplementary Figure 10 | TREL of a WSe_2 device with unipolar MoO_x/Pd contacts. TREL measured for a WSe_2 device with unipolar MoO_x/Pd contacts, which show a large Schottky barrier to electrons and a low Schottky barrier to holes.



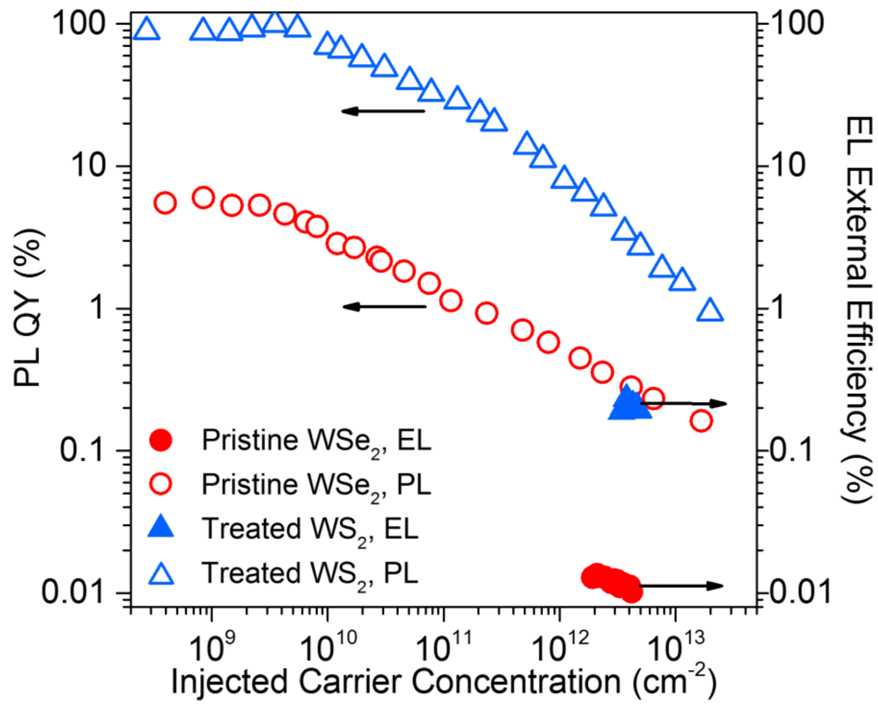
Supplementary Figure 11 | Simulated TREL for p-type, ambipolar and n-type devices. (a) Gate voltage as a function of time. **(b)** Simulated TREL for devices with varying Schottky barrier height; specifically, the cases of Fermi level pinning at conduction band (n-type), mid-gap (ambipolar) and valance band (p-type). Simulations were performed for material parameters corresponding to WSe_2, further details are provided in the methods.



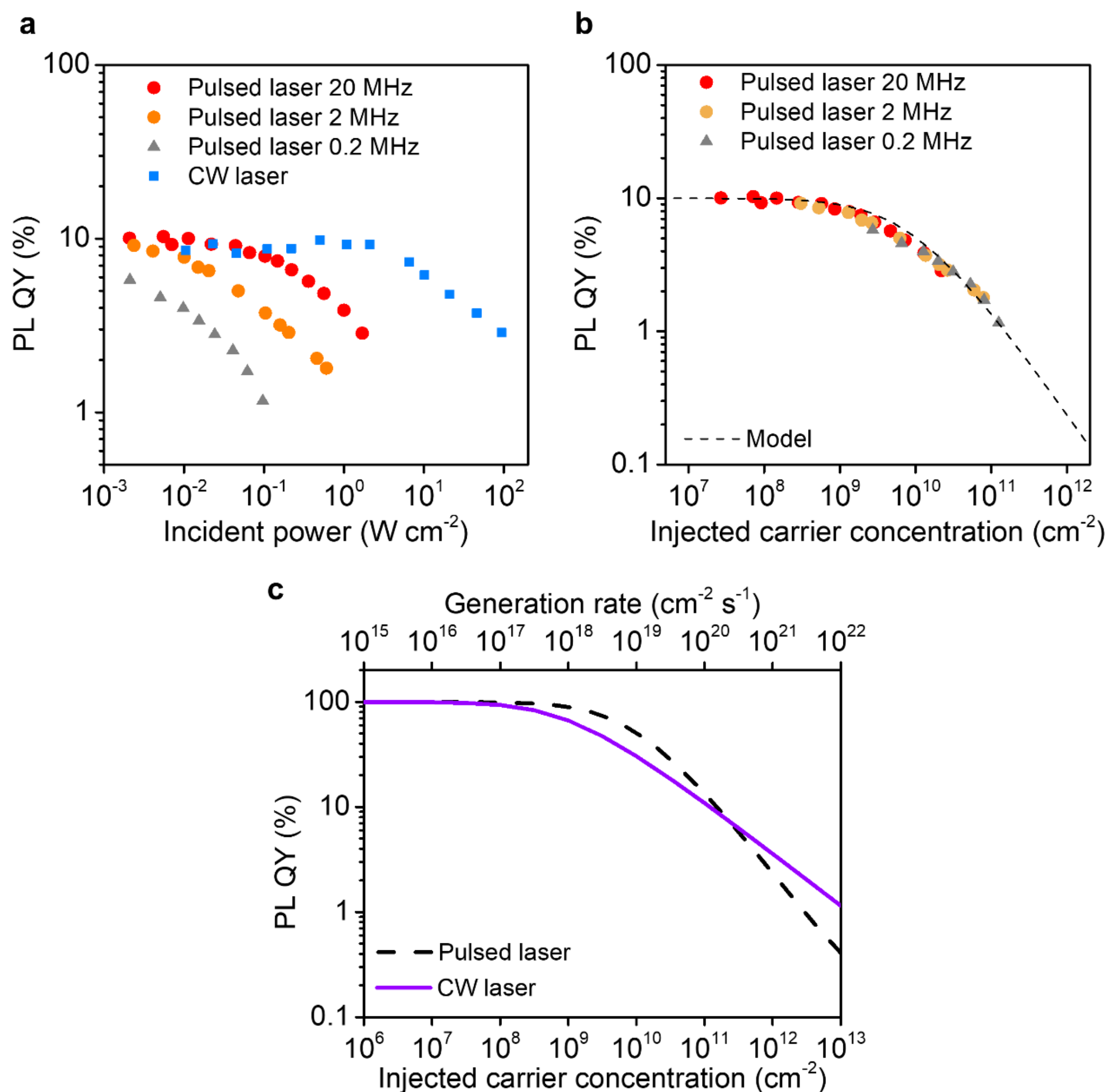
Supplementary Figure 12 | V_g dependence of EL characteristics. EL measured for a WS_2 device before **(a)**, and after superacid treatment **(b)**, as well as a WSe_2 device **(c)**, as a function of injected carrier concentration. Note that V_t for the WSe_2 and WS_2 devices are 2.0 V and 4.1 V, respectively.



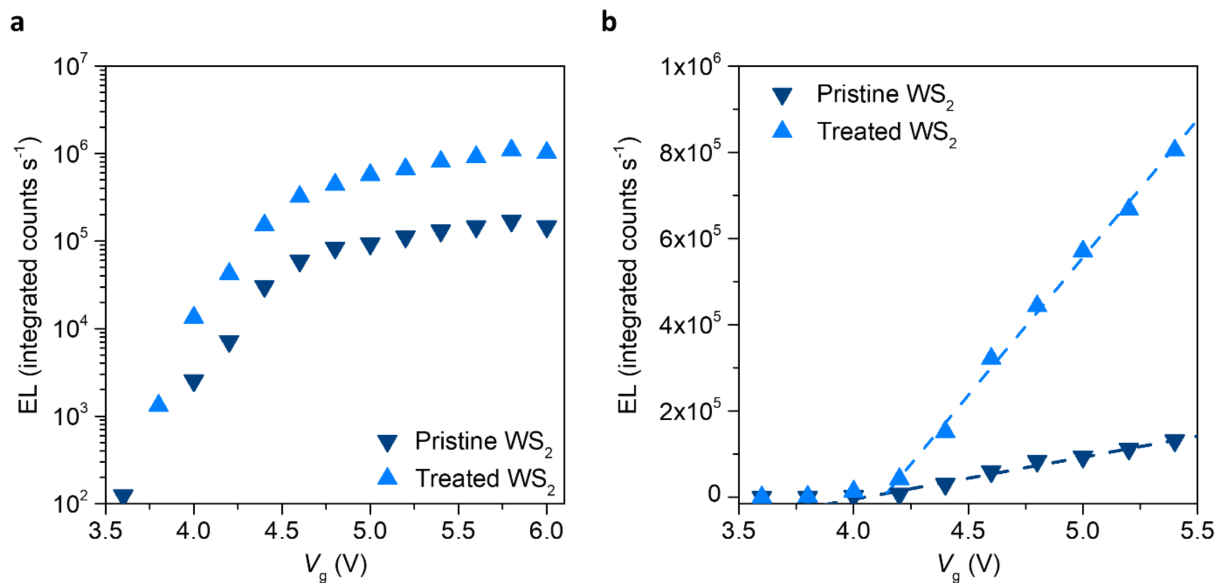
Supplementary Figure 13 | Total steady-state injected carrier concentration as a function of applied voltage. n_0+p_0 extracted from simulations and calculated using Supplementary Equation 4 for WSe_2 and WS_2 devices as a function of applied V_g. The injected carrier concentration at low V_g is overestimated by Supplementary Equation 4 because it does not account for the voltage dropped across the length of the semiconductor during a V_g transient. E_g values used for the simulations and analytical calculations are 2.34 eV and 2.88 eV for WSe_2 and WS_2 respectively[2].



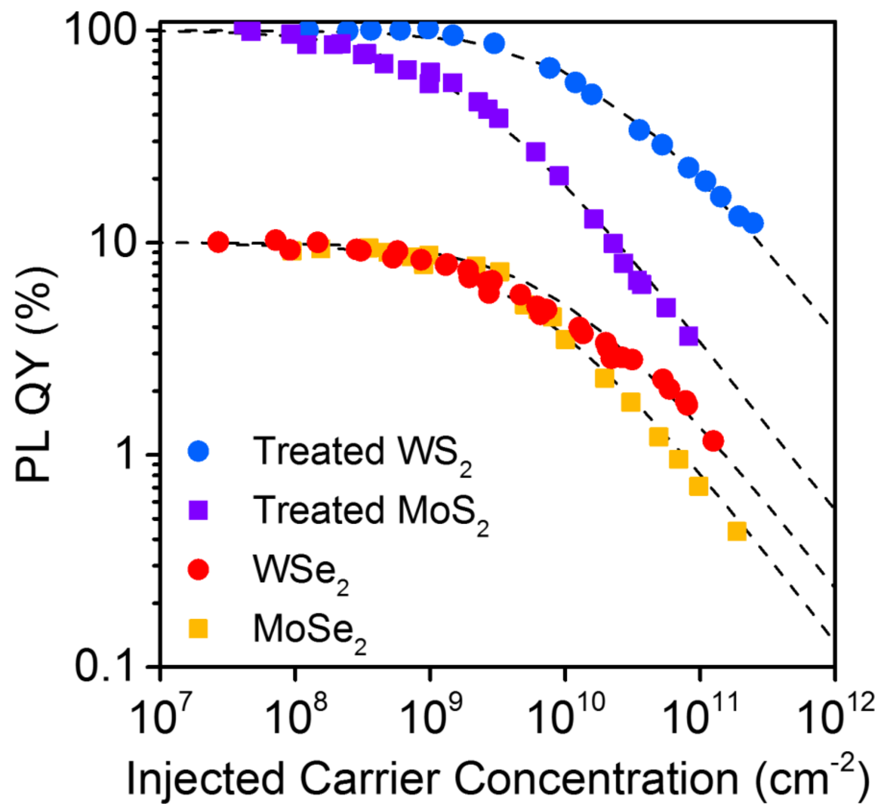
Supplementary Figure 14 | PL QY and EL external efficiency. PL QY and EL external efficiency as a function of injected carrier concentration measured for a WSe_2 device and a superacid-treated WS_2 device.



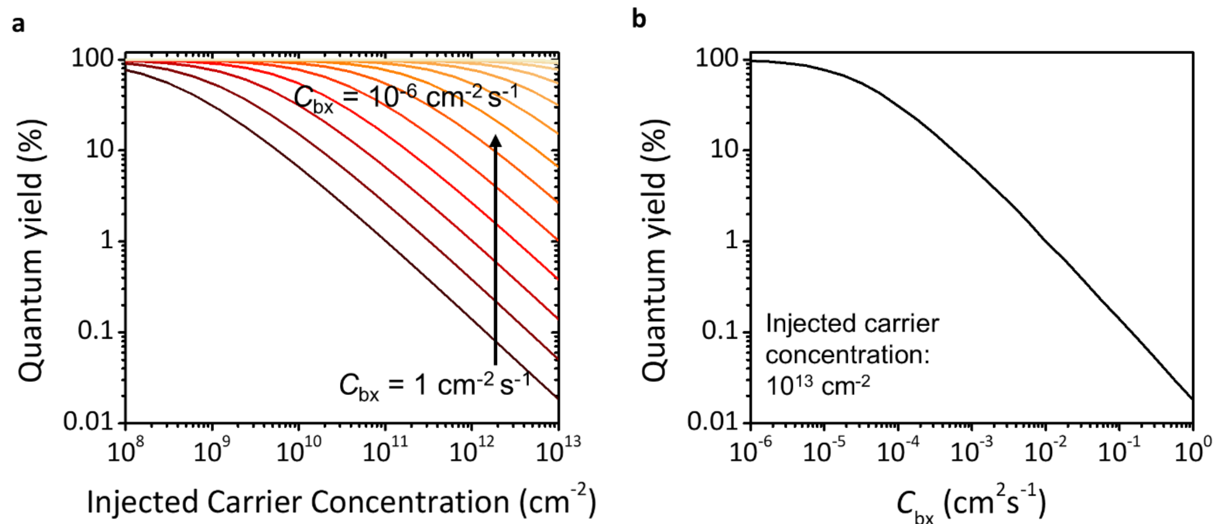
Supplementary Figure 15 | Quasi-steady-state PL QY. (a) QY measured as a function of incident average power for a CW laser and a pulsed laser with repetition rates of 0.2, 2, and 20 MHz; excitation wavelength is 514 nm in all cases. **(b)** Quasi-steady-state QY as a function of incident carrier concentration from measurements shown in panel **(a)**; dashed line shows recombination model. **(c)** Modeled recombination for steady state (purple) and quasi-steady-state (black) excitation.



Supplementary Figure 16 | EL from WS_2 before and after superacid treatment. V_g dependence of EL from a WS_2 device before (pristine) and after superacid treatment (treated), plotted in **(a)** logarithmic and **(b)** linear scale.



Supplementary Figure 17 | Quasi-steady state PL QY of TMDCs. PL QY of exfoliated $MoSe_2$, CVD WSe_2, and of superacid treated WS_2 and MoS_2 measured using a pulsed laser. Dashed lines show recombination model.



Supplementary Figure 18 | Estimation of PL QY for materials with varying C_{bx}. (a) An estimation of efficiency versus injected carrier concentration while tuning the C_{bx} of a material with a PL radiative lifetime of 10 ns. **(b)** The estimated QY of a material with varied C_{bx} from 1 to 10^{-6} cm^{2}s^{-1} under the injected carrier concentration of 10^{13} cm^{-2}.

6.7 Supplementary Notes

Supplementary Note 1. Quasi-steady state recombination kinetics.

The time dependent luminescence decay in 2D materials can be calculated using a recombination model for 2D excitonic systems presented in our previous work:

$$\frac{d\langle N(t)\rangle}{dt} = -\frac{\langle N(t)\rangle}{\tau_r} - C_{bx}\langle N(t)\rangle^2 \tag{1}$$

where $\langle N(t)\rangle$ is the exciton concentration as a function of time (t), τ_r is the exciton lifetime, and C_{bx} is the biexcitonic recombination rate[3-5]. Solving this differential equation yields:

$$\langle N(t)\rangle = \frac{\langle N(0)\rangle\, e^{-\frac{t}{\tau_r}}}{1 + \tau_r \langle N(0)\rangle C_{bx} \left(1 - e^{-\frac{t}{\tau_r}}\right)} \tag{2}$$

where the boundary condition, $\langle N(0)\rangle$, is the initial exciton concentration. From Supplementary Equation 2, we can then calculate the PL QY during quasi-steady-state operation as a function of initial exciton density. The modeled values are in excellent agreement with quasi-steady-state QY measured using a pulsed laser with varying repetition rates as shown in Supplementary Fig. 15.

Supplementary Note 2. AC frequency dependence.

EL spectra measured with f ranging from 100 kHz to 10 MHz are shown in Supplementary Fig. 3a and the spectral shape was observed to be f independent (Supplementary Fig. 3b). The EL intensity per cycle shows minimal frequency dependence because $1/f$ is much larger than the EL decay time constant (~ 8 ns, Supplementary Fig. 2). This shows that the device can be operated at frequencies as high as 10 MHz, and is ultimately limited to a modulation frequency of 125 MHz corresponding to the EL decay time constant. This is the fastest electrically modulated light emitting device reported for TMDCs[6].

Supplementary Note 3. Current components during AC transient.

The total gate current ($I_{g,total}$) in a two-terminal t-EL device can be described by Supplementary Equation 3:

$$I_{g,total} = I_{g,DC} + I_{g,AC} \approx I_{g,AC} = I_{g,displacement} \tag{3}$$

where, $I_{g,DC}$ is the DC leakage current and $I_{g,AC}$ is the AC current at the gate electrode induced by the applied AC bias (V_g transients). From steady-state I_d-V_g measurements and capacitance measurements of the gate impedance as a function of frequency, we observe that the gate oxide shows no leakage current. Thus, the total gate current is mainly composed of the AC current, which is the displacement current generated by the changing electric fields in the device during a V_g transient. The corresponding current at the source terminal can be described by Supplementary Equation 4.

$$I_{\mathrm{s,total}} = I_{\mathrm{s,DC}} + I_{\mathrm{s,AC}} \approx I_{\mathrm{s,AC}} \tag{4}$$

The DC component of the current is again negligible. The AC current at the source contact is a combination of the electron, hole and displacement currents as shown in Supplementary Equation 5.

$$I_{\mathrm{s,AC}} = I_{\mathrm{s,hole}} + I_{\mathrm{s,electron}} + I_{\mathrm{s,displacement}} \tag{5}$$

It is not possible to experimentally measure these components separately, however Sentaurus simulations can help us understand the current components in more detail. Simulations (Supplementary Fig. 7) indicate that the major current components at the source electrode are the electron and hole currents, and their relative magnitude depends on the particular edge in the V_g transient. The simultaneous presence of electrons and holes in the semiconductor leads to EL emission.

Supplementary Note 4. EL dependence on Schottky barrier heights.

For devices with varying Schottky barrier (φ_B) heights, the relative intensity of EL at each V_g transient also shows large variations, although the integrated EL per cycle remains independent of φ_B. This can be qualitatively explained considering the specific example where we have hole selective; contacts to the semiconductor. In this case, during a $-V_g$ to $+V_g$ transient, the level of electrons which tunnel into the semiconductor is very low because of the large Schottky barrier height to electrons. This results in a smaller net bipolar carrier concentration in the semiconductor which translates to lesser EL. However, during the $+V_g$ to $-V_g$ transient, a large number of holes are injected into the semiconductor because of the smaller barrier height, resulting in a net larger bipolar carrier concentration, and hence larger EL. For the case of n-type contacts to the semiconductor, the mechanism can be similarly explained, and we obtain larger EL during the $-V_g$ to $+V_g$ transient relative to the $+V_g$ to $-V_g$ transient.

Supplementary Note 5. Efficiency calculation.

The EL internal efficiency of the t-EL device can be extracted from the ratio of the total number of emitted photons per cycle to the steady-state electron (n_0) and hole (p_0) concentrations:

$$\eta_{\mathrm{i}} = \frac{\int_0^T \int_0^L R \, dx \, dt}{(n_{\mathrm{o}} + p_{\mathrm{o}})L} = \beta(\mathrm{PL\ QY}) \tag{6}$$

Here T is the time period, L is the length of the device, R is the radiative recombination rate and β is the fraction of steady-state carriers which undergo recombination during a V_g transient. The value of (n_0+p_0) can be calculated using Supplementary Equation 6. During a $-V_g$ to $+V_g$ transient (total change of $2V_g$), the net voltage dropped at the Schottky source contact is equal to the sum of the barrier heights to electrons and holes ($\varphi_{Bn} + \varphi_{Bp} = E_g$). Thus,

$$(n_{\mathrm{o}} + p_{\mathrm{o}}) = \frac{C_{\mathrm{ox}}\left[2V_{\mathrm{g}} - \left(\varphi_{\mathrm{Bn}} + \varphi_{\mathrm{Bp}}\right) q^{-1}\right]}{q} \tag{7}$$

To achieve steady-state carrier densities, sufficient voltage must be applied to enable large band bending and thus achieve significant tunneling through the Schottky barriers. As such this equation is only valid for sufficiently high V_g, which is shown in Supplementary Fig. 13. The integral in the numerator is equal to the total number of photons emitted per cycle. The internal efficiency is unity

when the PL QY is 100% and all of the steady-state carriers undergo recombination (β = 1). Practically, due to the finite slew rate of the AC source and a finite radiative recombination rate, a fraction of the steady-state carriers exit the semiconductor through the source contact without recombining ($\beta \neq 1$). The external efficiency is given by:

$$\eta_e = \eta_i \, \eta_{ext} \tag{8}$$

where η_{ext} is the light extraction efficiency. This is calculated using $(4n^2)^{-1}$ where n is the refractive index of the medium, as well as the optical interference from the Si substrate with a 50 nm SiO_2 layer. The enhancement factor for Si/SiO_2 is experimentally determined to enhance the light-outcoupling by 1.6× for WSe_2 and 2× for WS_2.

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7

[7] MoS_2 Heterojunctions by Thickness Modulation

7.1 Introduction

Semiconducting transition metal dichalcogenides (TMDCs) with a layered crystal structure exhibit unique electrical[1, 2] and optical properties.[3-5] TMDCs provide opportunities in exploring new device concepts given their atomic level flatness, and ability to form van der Waals (vdW) heterostructures with strong interlayer coupling.[6-8] For instance, vdW heterobilayers of MoS_2/WSe_2 have been recently reported to exhibit spatially *direct* light absorption but spatially *indirect* light emission, representing a highly intriguing material property.[9, 10] Here, we explore the optoelectronic properties of lateral "hetero"-junctions formed on a single crystal of MoS_2 of varying thickness (i.e., number of layers). As a result of the quantum confinement effect,[11] when the thickness of a MoS_2 crystal is scaled down to a monolayer the optical band gap increases from 1.29 eV (indirect) to 1.85 eV (direct).[12, 13] The change in the band structure and the electron affinity of MoS_2 with layer number opens up the path to the formation of atomically sharp heterostructures, not by changing composition but rather by changing layer thickness. We experimentally examine the surface potential of this thickness modulated heterojunction by using Kelvin probe force microscopy (KPFM). We further use scanning photocurrent microscopy (SPCM) to probe the photoresponse of the junction. A large photocurrent response is observed at the monolayer/multilayer junction interface which confirms the presence of a strong built-in electric field at the interface. Device modeling is used in parallel to experiments to understand the underlying mechanism of the observed photocurrents and the band-alignments at the junction interface, suggesting the formation of a type-I heterojunction.

SPCM has been previously used to study the photoresponse of metal contacted MoS_2 transistors, where the channel thickness for MoS_2 was uniform throughout the device.[14, 15] The results have shown that the photoresponse is primarily driven by the metal/MoS_2 Schottky contacts and photothermoelectric effect.[15] In distinct contrast to previous studies, we observe that the peak photoresponse is spatially located at the MoS_2 monolayer/multilayer junction for our lateral heterojunctions and not at the metal contacts.

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7.2 Band offset extraction at the monolayer-multilayer MoS_2 junction

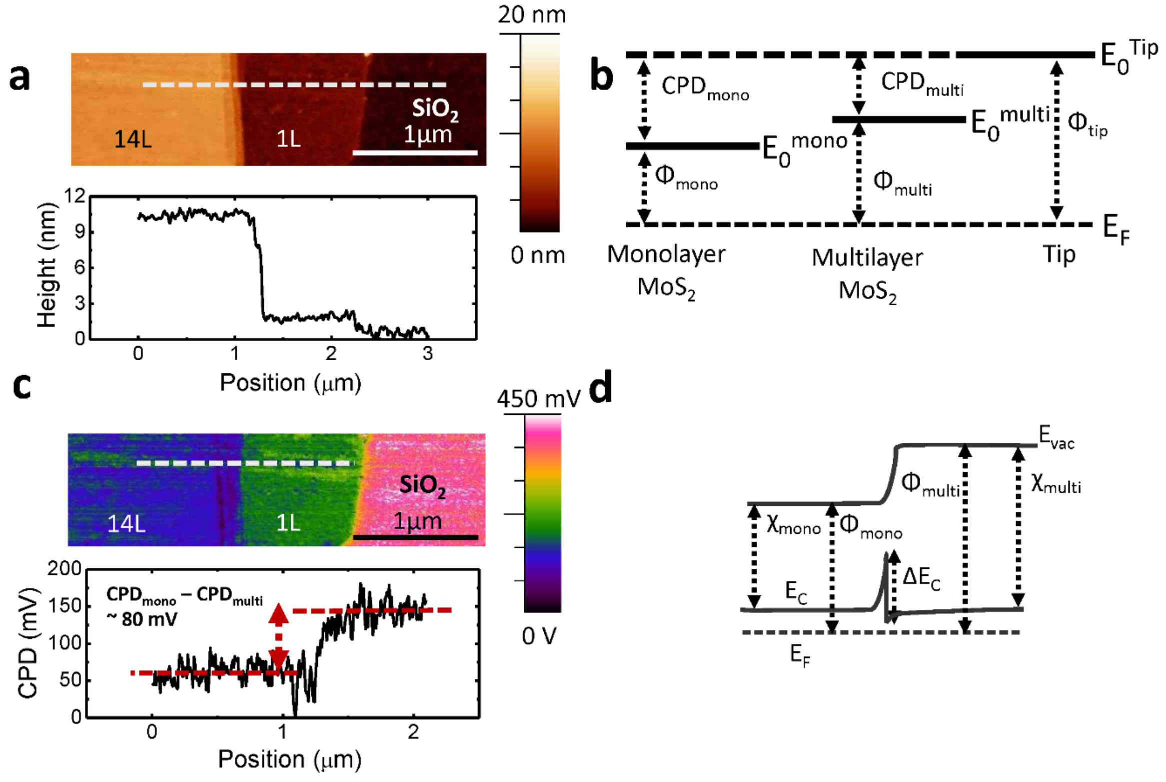

Figure 1. a. Atomic Force Microscope (AFM) image of a monolayer-multilayer MoS_2 flake. b. Representative energy band diagrams of isolated monolayer and multilayer MoS_2 with respect to the AFM tip, depicting CPD and work function values. c. Kelvin Force Probe Microscope (KPFM) image of a representative 1L-14L MoS_2 flake. d. Representative band diagram of a monolayer-multilayer device at equilibrium.

KPFM is performed to spatially map the surface potential, and shed light on the band offsets at the monolayer-multilayer interface. The sample surface topography and contact potential difference (CPD) between the tip and sample are measured simultaneously.[16, 17] Figure 1a demonstrates a monolayer-multilayer junction flake with 10 nm of multilayer (~14 layers; 14L) thickness. In this particular flake, monolayer to multilayer transition occurs across ~100 nm of the lateral distance in a terraced manner. KPFM is performed using a Bruker MultiMode atomic force microscope under ambient conditions. A Si cantilever tip coated with Pt-Ir (SCM-PIT, Bruker Co.) is used in the tapping mode. Electrical contacts to the MoS_2 flake were grounded during the measurements. An AC voltage of 2 V is applied to the tip while the tip height is kept constant at 5nm. The measured DC voltage of the tip, corresponding to CPD, determines the work function difference between the AFM tip (Pt-Ir) and each region of the MoS_2 flake,[18, 19] i.e., $\mathrm{CPD_{mono}} = \frac{(\Phi_{tip} - \Phi_{mono})}{e}$ for the monolayer side and $\mathrm{CPD_{multilayer}} = \frac{(\Phi_{tip} - \Phi_{multilayer})}{e}$ for the multilayer side. Φ_{mono}, $\Phi_{multilayer}$, and Φ_{tip} are the work functions of monolayer MoS_2, multilayer MoS_2, and the surface of AFM tip, respectively (Fig. 1b). The measured surface potential difference, $\Delta\mathrm{CPD} = \mathrm{CPD_{mono}} - \mathrm{CPD_{multilayer}} = \left(\frac{\Phi_{multilayer} - \Phi_{monolayer}}{e}\right)$, corresponds to the band bending in the

vacuum level E_{vac} at thermal equilibrium, and is also equal to the workfunction difference between the monolayer and the multilayer (Fig. 1b). KPFM map of a representative 1L-14L flake is shown in Fig. 1c. From KPFM measurements, the workfunction difference is found to be ~80 meV (Fig. 1c).[20, 21] Next, we focus on obtaining the energy band diagram for the heterojunction by first extracting the conduction band offset at the interface. The conduction band offset $\Delta E_C = (\chi_{multilayer} - \chi_{mono})$ at the heterojunction corresponds to the electron affinity difference between the monolayer (χ_{mono}) and multilayer ($\chi_{multilayer}$). The workfunction difference between monolayer and multilayer is related to effective density of states (N_C), ΔE_C and doping levels (N_D) as shown in Eq. 1.

$$\Phi_{multi-mono} = \left[\Delta E_C - kT \left(\ln \frac{\left(\frac{N_{D,multi}}{N_{C,multi}}\right)}{\left(\frac{N_{,Dmono}}{N_{C,mono}}\right)} \right) \right] \cdots (1)$$

Boltzmann approximation is considered while deriving Eq. 1. Next we assume the doping level per unit volume is identical in both monolayer and multilayer flakes. Thus Eq. 1 becomes,

$$\Phi_{multi-mono} = \Delta E_C - kT\left(\frac{3}{2}\right) \ln\left(\frac{(m_n^*)_{mono}}{(m_n^*)_{multi}}\right) \ldots (2)$$

$\Phi_{multi-mono}$ is measured from KPFM, effective mass values for electrons are taken to be $m^*_{n,mono} = 0.407\ m_0$ and $m^*_{n,multi} = 0.574\ m_0$.[22], From these parameters, ΔE_C of ~67 meV at the 1L-14L interface is extracted. This band offset corresponds to a type-I heterojunction as depicted in the qualitative band diagram of Figure 1d. Note that the relative values of the dielectric constant of monolayer and multilayer MoS_2 determine the electric fields and hence the band bending on both sides of the heterojunction. The dielectric constants are assumed to be the same (~ 4) in this work.[23]

7.3 Photoresponse at the monolayer-multilayer MoS_2 junction

Scanning photocurrent microscopy (SPCM), a spatially resolved photodetection technique that combines electrical measurement and local illumination with a focused laser beam is used to probe the local photoresponse of the monolayer-multilayer MoS_2 devices.[24-29] Optical image of a representative device is shown in Figure 2a. Here, the device consists of a 1L-5L MoS_2 junction. The channel lengths for the monolayer and the multilayer regions are ~2 μm each. The contact to the monolayer is defined as the source electrode and is electrically grounded. The contact to the multilayer MoS_2 serves as the drain electrode to which an external voltage, V_{DS} is applied during the measurements. The heavily doped Si substrate serves as the global back-gate to which voltage, V_G can be applied to modulate the electric potential in MoS_2. The device is locally illuminated by a focused laser beam (wavelength: 488 nm, diameter: ~ 1 μm) as depicted in Figure 2b. The spatial resolution of the scanning stage is 0.1 μm. The light current, I_{light} is recorded as the laser spot is scanned across the length of the device. The photocurrent, $I_{photocurrent}$, is then obtained as a function of illumination spot by subtracting the dark current of the device, I_{dark}, from I_{light}. In contrast to previous reports studying the photoresponse in MoS_2 single layer or multilayer devices (Fig. S2),[3, 14, 15, 30] the peak photocurrent in our device is observed at the monolayer-multilayer interface rather than the metal/semiconductor junction. Figure 2c shows the spatial response of the photocurrent along the dashed line of Fig. 2a at $V_G = 0$ V and laser intensity of 0.78 μW. Source-drain voltage is varied from -0.5 V to 0.5 V. Even without source drain bias ($V_{DS} = 0$ V), a finite short circuit

current (~8 nA) is measured as seen in the inset of Figure 2c. This implies that the expected band bending and the resulting built-in electric field that is induced by the difference in the electron affinities of the monolayer and multilayer MoS_2 regions is capable of separating the electron-hole pairs generated at the monolayer-multilayer interface. The dependence of the photocurrent on V_{DS} and the excitation power is investigated to further characterize the monolayer-multilayer junction devices. The peak photocurrent, corresponding to the local illumination of the monolayer-multilayer interface, is measured at different illumination intensities of 2 nW, 0.78 µW, 2 µW and 10 µW and V_{DS} of -0.5 V to 0.5 V at V_{GS} = 0 V (Figure 2d). The photocurrent increases as the applied V_{DS} bias is increased due to the contribution of the enhanced drift current and decreased transit time of the electrons.[3] The increase in the photocurrent with the illumination intensity can be attributed to generation of higher number of electron-hole pairs. It is important to note that in all different intensities and V_{DS} values the peak photocurrent response is observed at the monolayer-multilayer heterojunction.

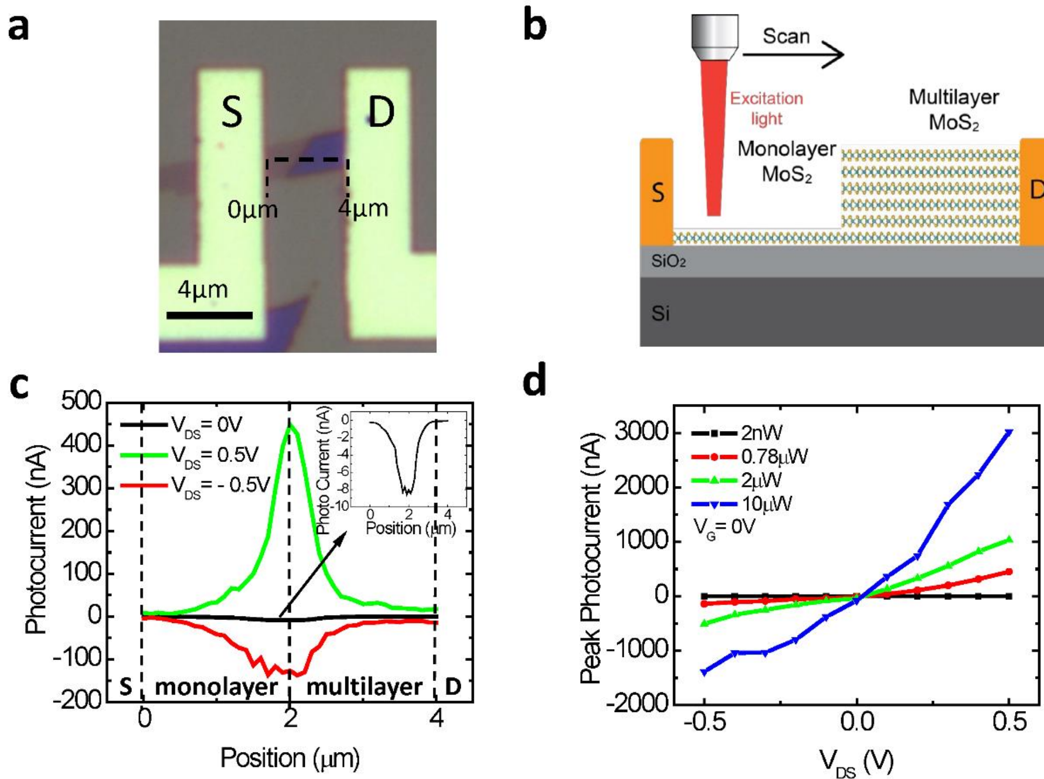

Figure 2. a. Optical microscope image of the monolayer-multilayer device with Ni/Au (30nm/30nm) contacts. b. Schematic representation of the SPCM measurement. c. Photoresponse of the monolayer-multilayer MoS_2 flake versus position along the dashed line at V_G = 0 V, with illumination power of 0.78 µW and with V_{DS} = - 0.5 V, V_{DS} = 0.5 V and V_{DS} = 0 V. d. Peak photocurrent vs. V_{DS} at V_{GS} = 0 V with different illumination powers.

7.4 Device Modeling

Device modeling was performed using TCAD Sentaurus to further understand the junction properties for a monolayer-multilayer device. For the Sentaurus simulations a ΔE_C ~ 67 meV, calculated from the KPFM data is used. The doping level for both monolayer and multilayer regions are assumed to be $N_{D,mono} = N_{D,multi} = 10^{18}$ cm^{-3}.[34] The effect of the back gate is modeled as a change in the device doping concentration. The effective mass values are taken to be m^*_e ~ 0.407 m_0 for the monolayer and m^*_e ~ 0.574 m_0 for the multilayer as described earlier.[22] The dielectric constants are assumed to be the same $\varepsilon_{mono} = \varepsilon_{multilayer} = 4\ \varepsilon_0$.[23] For the simulated device, the exact dimensions of the measured device presented in Figure 2 are used. Electron affinities are assumed to be $\chi_{monolayer} = 4$ eV[35] and $\chi_{multilayer} = 4.067$ eV, such that $\Delta E_C = 67$ meV as obtained earlier using the experimental KPFM data. Measured values for bandgap of monolayer (1.85 eV) and 5 layers (1.4 eV) are used.[12] A light window of 1 µm is used that corresponds to the spot size of the laser and shined in the center of the junction. A laser wavelength of 488 nm and an absorption coefficient of ~10^6 cm^{-1} for the monolayer and 10^5 cm^{-1} for the multilayer side is assumed for the simulations.[14, 36] Thus with the assumptions stated above and using the KPFM information, simulations revealed a type – I heterojunction band alignment in the monolayer – multilayer MoS_2 heterojunction flake as seen in Fig 3a-c.

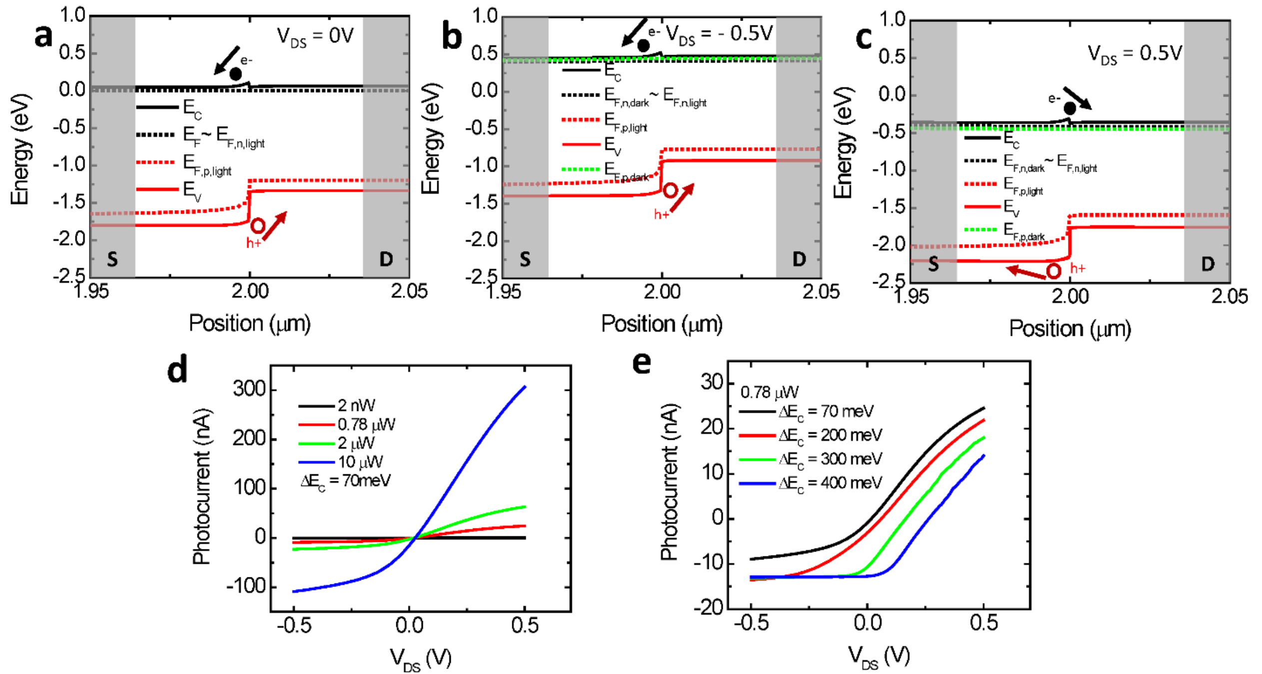

Figure 3. Simulated band diagrams at a, $V_{DS} = 0$ V, b, $V_{DS} = -0.5$ V and c, $V_{DS} = 0.5$ V in dark and with light shined at the monolayer – multilayer MoS_2 junction. d. Simulated photocurrent vs. V_{DS} at different laser powers. e. Simulated photocurrent vs. V_{DS} with different ΔE_C values.

Figure 3a shows the simulated band diagram at $V_{DS} = 0$ V for the dark condition and when light is illuminated at the monolayer-multilayer interface. Under illumination, Fermi levels split ($E_{F,n}$ and $E_{F,p}$) as a result of the generation of the electron hole pairs. At a simulated laser power of

0.78μW, low level injection conditions prevail and no change in the quasi Fermi level for electrons is observed as seen in Fig. 3a. At zero V_{DS} bias, due to the built-in electric field at the heterojunction, electrons that are generated at the monolayer side of the monolayer-multilayer junction are swept to the monolayer side (source). However electrons generated at the multilayer side are subjected to a barrier height of 67 meV. Holes do not encounter any barrier and freely move to the multilayer side (drain). This is consistent with the measured SPCM data, where a negative photocurrent of 8 nA is recorded at zero V_{DS} signifying that the electrons are collected at the source (monolayer) and holes at the drain (multilayer) side.

When a negative V_{DS} (Fig. 3b) is applied to the multilayer side (drain), there is a higher built-in electric field and a wider depletion region at the junction. A wider depletion region at the monolayer side allows the separation of a larger number of photogenerated electron-hole pairs thus resulting in a larger negative photocurrent compared to the case of zero V_{DS} as the electrons get swept to the monolayer side (source) and holes swept to the multilayer side (drain) freely. However electrons generated at the multilayer side still face a barrier height of ~67 meV, just like in the case of zero bias. By applying a positive V_{DS} (Fig. 3c) the barrier height for electron transport from the monolayer to the multilayer is nearly diminished. Electron-hole pairs generated at the monolayer side contribute to the photocurrent since holes move to the monolayer side (source) freely and electrons can go over the decreased barrier height and move to the multilayer side (drain). Whereas, electron-hole pairs generated at the multilayer side don't contribute to the photocurrent since holes see a barrier of ΔE_V (~0.383eV). This current flow mechanism is consistent with measuring positive photocurrent at $V_{DS} > 0$ and measuring negative photocurrent for $V_{DS} < 0$ as seen in Fig. 2d.

Photocurrent vs. applied V_{DS} is also simulated in TCAD Sentaurus with different illumination intensities. The same parameters and assumptions that are used to generate the band diagrams mentioned above are used to simulate the V_{DS} and the light intensity dependence of the photocurrent. In the SPCM measurements, as seen in Fig. 2c, at $V_{DS} = 0$ V a negative photocurrent is observed. As the applied bias is increased to $V_{DS} = 0.1$ V, photocurrent becomes positive (Fig. 2d). This implies that the experimental crossover from the negative photocurrent to positive photocurrent is in between $V_{DS} = 0$ V and $V_{DS} = 0.1$ V. The simulated photorcurrents are shown in Fig. 3d-e. The simulation is in qualitative agreement with the experimental data, with the transition from the negative to positive photocurrent occurring at positive V_{DS} values. The negative to positive photocurrent crossover voltage is sensitive to the parameter values assumed for the simulations. Figure 3e illustrates the large dependence of the simulated crossover voltage on the ΔE_C value. Quantitative differences between the simulated and experimental data can also arise from the presence of a terraced junction as described in Fig. 1a, compared to the ideal step heterojunction simulated in Sentaurus. The Sentaurus simulations however qualitatively explain the experimental data and all the trends, but a quantitative analysis warrants simulations or first principle calculations using exact values of absorption coefficient, electron affinities, effective masses, doping, carrier lifetimes, diffusion lengths, etc.

7.5 Conclusion

In conclusion, the type-I heterojunctions enabled by lateral thickness modulation of MoS_2 are demonstrated. The junction properties are characterized by KPFM and SPCM. A workfunction difference of 80 meV is measured by KPFM. Furthermore, a conduction band offset of 67 meV is extracted from the difference in the electron affinities and work functions of the monolayer and multilayer regions of the MoS_2. Photocurrent generation at the monolayer-multilayer heterojunction is observed with SPCM. The peak photocurrent generation at the monolayer-multilayer junction is attributed to the electric field in the depletion region at the heterojunction formed by the difference in the band gaps and the electron affinities of the monolayer and the multilayer flake. A short circuit current of 8 nA is measured due to the built-in electric field being able to separate and collect the generated electron hole pairs at the monolayer-multilayer junction. The photoresponsivity of the monolayer-multilayer MoS_2 junction is studied with respect to the incident light power and the source-drain bias. The demonstration of the type-I heterojunction on the same MoS_2 flake will inspire further investigation regarding the electronic transport properties of the atomically sharp type-I band alignment in the TMDC flakes.

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8

Conclusion and outlook

The insatiable need for better performance, at low cost and low power consumption will drive electronics innovations in terms of device structure, materials innovation, and process integration. With continued advancement of materials processing, the integration of nanomaterials and low dimensional systems is inevitable. It will be useful to summarize all the key results of this thesis to gain insight and plan for the future.

2D materials like MoS_2 and WSe_2 have remarkable materials properties even at monolayer limits. The higher effective masses and larger bandgaps of these materials along with the low dielectric constants make them ideal candidates for low power applications in the sub-5 nm physical gate length regime. The demonstration of carbon nanotube gated MoS_2 transistors is a useful step in this direction, but for large scale integration of these nanomaterials, high quality wafer scale growth and process stable doping of 2D materials remain as key challenges. Additionally, MoS_2 may not be the most optimal material of choice for all applications, and it would be useful to consider other channel materials like WSe_2 which has an effective mass of ~ 0.35 m_0 for electrons. This will allow for a better trade-off between ballistic current which will dictate the On current of the transistor and the level of direct source-to-drain-leakage, which will determine the On/Off current ratio of the transistor.

Apart from 2D scaling, the use of 2D materials in 3D integration for back end of line electronics layers remains an interesting application, mainly given the possibility of low temperature growth and low temperature processing of these materials [1]. Previous demonstrations of 3D monolithic CMOS integration using mechanically exfoliated 2D material layers for implementing basic digital and analog circuits show the promise for reducing circuit footprint [2, 3]. Monolithic integration of 2D materials on top of existing silicon based logic would allow for much higher electronics density. Potential back-end-of-line applications for which 2D materials would be useful would be memory driving circuits and I/O circuits. Further work in the area of high quality low-temperature growth using techniques like plasma sulfurization / selenization and atomic layer deposition is thus essential.

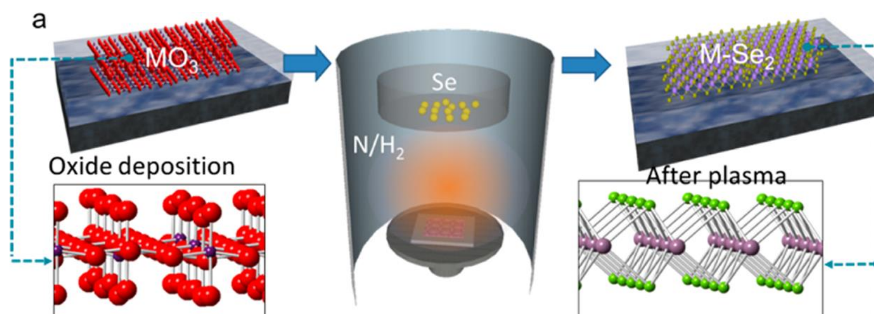

Figure 1: Low-temperature selenization of transition metal oxides [1]

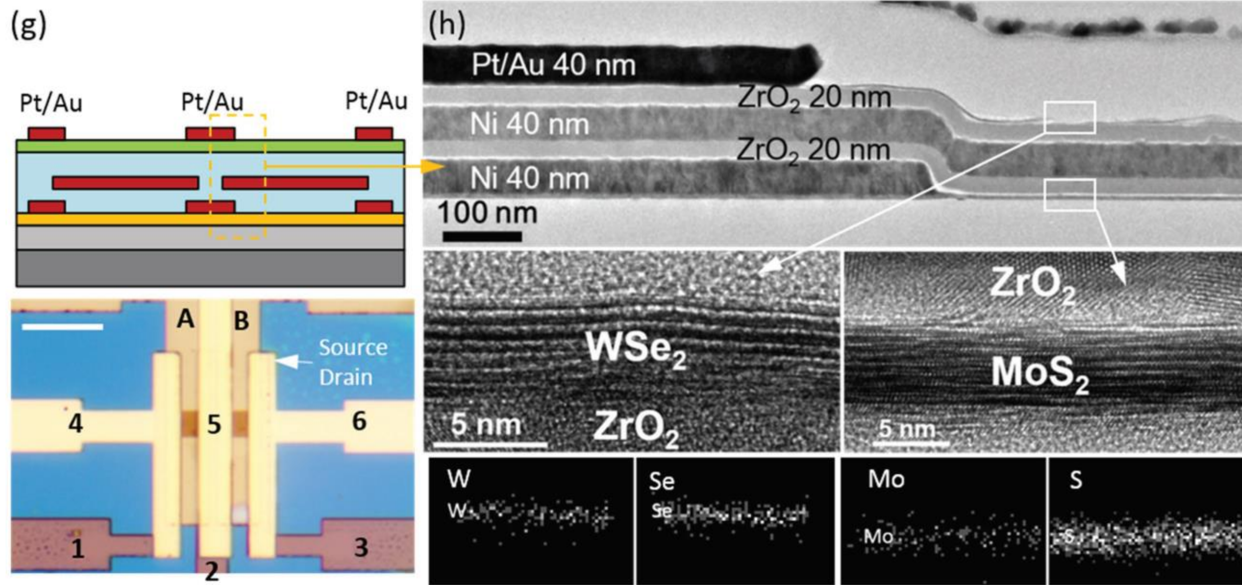

Figure 2: Cross section schematic, top view microscope image and cross section TEM image of 3D CMOS inverter made using MoS_2 and WSe_2 as channel materials [2]

As transistor sizes shrink to the atomic scale and so do the physical dimensions of the gate, the quantum capacitance of the gate will become an important factor which must be considered while evaluating the performance of the transistors. The gate structures today are already complicated structures consisting of TiN / TaN layers with metal fills of W or Co. As the sizes of the gates shrink, the thickness of these layers will also reduce and gate quantum capacitance will affect the channel charge. The demonstration of quantization features in SOI channel with CNT gate transistors, resulting from the Van Hove singularities of the CNT prove that by engineering the DOS of the gate, it is possible to design and obtain pre-determined transfer characteristics. Further work involving devices should be aimed at improving the On currents and also making the steps more prominent. For the specific case of gate DOS being delta functions with respect to energy, a transconductance curve with steps can be obtained, with potential applications in multi-level memory and logic applications, which would lead to denser electronics.

Strain engineering leads to a drastic improvement in the photoluminescence of multilayer WSe_2 and the largest change is for a bilayer. It would be important to correlate this change in PL properties with the material parameters like carrier lifetime and internal photoluminescence quantum yield. Additionally, it would be important to investigate the electrical properties of WSe_2 under strain, *v.i.z.* carrier mobility and electronic bandgap change. Strain engineered growth of WSe_2 observing similar effects on PL of CVD grown materials has already been achieved [4]. Implementing strain in 2D material based electronic devices and finding suitable ways to maintain strain remain unsolved challenges.

The gold mediated exfoliation method was demonstrated mainly for TMDs. However in principle it could be applicable to other 2D materials as well. An investigation into the mechanism of coupling between the topmost layer of the layered material and the gold would provide insight into the exact mechanisms responsible for the high yield of monolayers from this process. This in turn would allow for the proper selection of the material to be deposited on top of the layered crystal, so as to optimize the level of strain induced in the topmost layer of the crystal, while at the

same time not inducing any defects in the process. Finally, developing a technique / process to transfer patterned monolayer TMDs using this technique would be ideal for integrating 2D monolayers on top of arbitrary substrates.

The monolayer light emitting devices, and the pulsed electroluminescence technique is ideal for application in cases where the semiconductors are hard to dope p/n type, and which mostly form Schottky contacts. This is specifically the case for wide-bandgap semiconductors which may be used to achieve ultra-violet light emission using the simple operation mechanism described in chapter 6. The pulsed EL technique is also useful for monolayer semiconductors which are hard to dope using traditional doping strategies like substitutional doping.

The efficiency of these devices is low, and the large band bending during the transient which is responsible for allowing bipolar injection from the same contact, may be the reason for the same. Scaling the gate oxide thickness would potentially help reduce the gate voltage needed for the operation of the device, and hence lower the level of potential hot-carriers at the Schottky contact. Finally, for the materials used for demonstrating the concept of transient EL, the PL internal quantum yield is very low at high carrier injection values because of biexcitonic recombination mechanism. Finding materials which have a lower biexcitonic recombination coefficient is therefore critical to the development of higher efficiency light emitting devices using this technique. Another technique to reduce the biexcitonic recombination coefficient may be encapsulating the 2D light emitting layer in materials with different dielectric constants, thereby changing the excitonic binding energy of the material.

Lateral 2D heterostructures by means of thickness modulation, provide an interesting and convenient way to form atomically sharp and well defined heterostructures. The large variation in the band gap for 2D materials like TMDs in the few layer range is the factor which make this possible, allowing for applications like photodetectors.

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