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GaAs/AlGaAs based Intensity and Phase Modulators @ 1.55 Microns Directly Grown on Silicon Substrates

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by

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VITA

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PUBLICATIONS

1) Prashanth Bhasker, Justin Norman, John E Bowers, Nadir Dagli," *Intensity and Phase Modulators at 1.55 μm in GaAs/AlGaAs Layers Directly Grown on Silicon*", Journal of Lightwave Technology, 2018. **36**(18): p. 4205-4210
2) Prashanth Bhasker, Justin Norman, John E Bowers, Nadir Dagli," *Low Voltage, High Optical Power Handling, Bulk Compound Semiconductor Electro-Optic Modulator at 1550 nm*", in preparation
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7) Prashanth Bhasker, Justin Norman, John E Bowers, Nadir Dagli," *Intensity and Phase Modulators at 1.55 μm with InAs/InGaAs Quantum Dots Epitaxially Grown on Silicon*" in CLEO Pacific Rim Conference 2018. 2018. Hong Kong: Optical Society of America

8) Prashanth Bhasker, Selim Dogru, Nadir Dagli.” *Active-Passive Integration using a-Si Waveguides for Substrate Removed Electro-Optic Modulators”* in 2018 IEEE Photonics Conference (IPC). 2018

9) Prashanth Bhasker, Chen Shang, John E Bowers, Nadir Dagli,” *Low Loss, Compact Waveguides in GaAs/Oxidized AlGaAs Layers Directly Grown on Silicon”* in *Conference on Lasers and Electro-Optics*. 2019. San Jose, California: Optical Society of America

ABSTRACT

GaAs/AlGaAs based Intensity and Phase Modulators @ 1.55 Microns Directly Grown on Silicon Substrates

by

Prashanth Bhasker

Optical modulators have been an integral part of fiber optic communication link. Low drive voltage, wide electrical bandwidth, low optical propagation loss, high extinction ratio, easier fabrication and low cost are some of desired properties of an optical modulator. Silicon, III-V and lithium niobate are the most prominent used material systems for modulators. Silicon modulators, being attractive in terms of the substrate cost and mature fabrication process, are limited in using only the free-carrier plasma dispersion effect for designing optical modulators as opposed to Pockel's effect and Quantum confined stark effect used in III-V based modulators which would enable one to design even more efficient devices.

In the past years, heterogeneous approach enabled to integrate III-V based active photonic devices on to Silicon using bonding. However, the size and the cost of III-V substrate limits scaling the approach over bigger silicon wafers. To overcome that and to integrate efficient III-V based photonic devices on much bigger silicon wafers, in recent years, there has been efforts carried out to grow GaAs/AlGaAs material system directly on Silicon substrates. High performance GaAs material system-based quantum dot lasers @ 1.3 μm have been demonstrated with this technique. This approach can overcome the size limitation associated with III-V based substrates.

GaAs and its lattice matched layers exhibit Pockel's effect and could be used to design modulators on silicon substrate. In this work, for the first time, experimental proof of Pockel's effect on GaAs/AlGaAs layers directly grown on silicon substrates is reported. GaAs/AlGaAs MZM's @ 1.55 μm grown on mis-cut silicon substrates had an electrical design equivalent to NPIN diode. Device demonstrated a low propagation loss of 1.5±0.5 dB/cm and a $V_{\pi}L$ product of 1.5±0.1 V.cm. V_{π} of a 4 mm MZM was 3.6 V.

Challenges in designing high speed MZM's on silicon substrate is then analyzed and a modified microstrip electrode design with significant improvement in terms of electrical loss (5 dB/cm @ 67 GHz) and dispersion as opposed to the widely used coplanar electrodes is demonstrated. These electrodes were then integrated with GaAs MZM as a traveling wave design. 3 dB and 6 dB EO bandwidth of 4 mm MZM were 9.6 GHz and 18.5 GHz respectively. A modified modulator design is proposed to improve the electrical bandwidth of the modulator along with the simulation results. Preliminary experimental results on the drive voltage and propagation loss of the modified design on on-axis silicon wafer is presented. Device demonstrated a $V_{\pi}L$ product of 1.745±0.035 V.cm and propagation loss of less than 3 dB/cm. 8 mm MZM demonstrated a low drive voltage of 2.2 V under push pull. Finally, compact GaAs based waveguide on Silicon using selective oxidation of high Aluminum content AlGaAs layers is reported with a low propagation loss of 4 dB/cm.

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1 Introduction

1.1 Overview

This chapter briefly summarizes the popular modulator technologies with its advantages and disadvantages. One of the widely used material systems for optical modulators are the lithium niobate based Mach-Zehnder modulators (MZM). Lithium niobate exhibit Pockel's effect which makes it suitable for fabricating phase modulators which are in turn converted into an intensity modulator using MZM designs. On-substrate lithium niobate based modulators are typically few centimeters in length and have V_π (voltage required to achieve π phase change) greater than 4 V. Its low refractive index contrast (Δn~0.02) doesn't allow compact waveguides leading to increase in size and the drive voltage of the modulators. In the recent years, lithium niobate thin films are bonded on to silicon with silicon dioxide as bottom cladding. This leads to improved optical confinement and without the need for any doped semiconductor layers, lithium niobate bonded on to silicon substrates have demonstrated impressive optical and electrical results [1] respectively. Device had a low drive voltage of 2.3 V for 1 cm long device, combined with an electro-optic RF bandwidth exceeding 60 GHz. This approach still involves bonding of the lithium niobate films and later with the III-V based Lasers which might be challenging, and its success greatly depends on the bonding quality. Furthermore , lithium niobate modulators also suffer from optical damage at high optical powers [2]. High optical power handling modulators could be useful for analog optical links.

III-V based optical modulators are designed based on Pockel's effect, quantum confined stark effect, band filling effect and free carrier plasma dispersion effect. Ultra-low

drive voltages [3] and high electrical bandwidths [4] have been demonstrated using quantum well cores and MZM designs. High performance compact electro-absorption modulators have also been demonstrated in InP material system [5]. These electro-absorption modulators can be easily integrated with the lasers. Size limitation and the cost of III-V substrates are some of the limiting factors. Hybrid integration approach involving bonding of III-V on to silicon substrate enabled the use of low-cost bigger silicon wafers. However, size limitation of III-V substrate limits scaling this approach over much bigger silicon wafers. To overcome this size and cost limitation, III-V epitaxial growth directly on silicon would be a solution. In recent years, there have been significant efforts in developing this growth technique. Using certain buffer layers, defect densities have been brought down to acceptable level. High performance quantum dot lasers @ 1.3 μm [6] have been demonstrated using this growth technique. With laser being demonstrated, developing modulators based on this approach would enable homogenous integration of III-V based photonic devices. GaAs/AlGaAs material system exhibit Pockel's effect and being transparent @ 1.55 μm would enable to develop electro-optic MZM's on silicon wafer. Point of comparison for this thesis is with the already available silicon based MZM's. So, in the next section, brief summary of silicon MZM's are presented.

1.2 Silicon Modulators

Silicon with its Centro-symmetric crystal structure doesn't exhibit Pockel's effect. Silicon modulators use free carrier plasma dispersion effect for refractive index change and is given by [7]

$$\Delta n = -\left(\frac{q^2\lambda^2}{8\pi^2 c^2 \epsilon_0 n}\right)\left(\frac{\Delta N}{m_e} + \frac{\Delta P}{m_h}\right)$$

$$\Delta \alpha = -\left(\frac{q^3\lambda^2}{4\pi^2 c^3 \epsilon_0 n}\right)\left(\frac{\Delta N}{m^2{}_e \mu_e} + \frac{\Delta P}{m^2{}_h \mu_h}\right)$$

Where

Δn- refractive index change

$\Delta \alpha$-free carrier induced absorption

ΔN-Change in Electron Concentration

ΔP-Change in Hole Concentration

m_e, m_h-Effective mass of electrons, holes

μ_e, μ_h-Electron and hole mobility

λ-Wavelength of operation

q- Electron charge

c-Velocity of light

n-refractive index of material

Cross section of typically used silicon phase modulator is shown in Figure 1. Its typically a rib waveguide with a PN diode formed laterally. Optical fundamental mode has maximum intensity in the depletion region of PN diode. Refractive index change is directly proportional to change in electron and hole concentration as the applied bias is varied and is inversely proportional to the effective mass of the electrons and holes. For higher concentration change, refractive index changes also increase leading to a lower $V_\pi L$ product for the MZM at the expense of increased propagation loss. So, typically silicon based MZM's

have higher propagation loss (>7 dB/cm) and have a $V_\pi L$ product between 0.85 V.cm [8] and 3.15 V.cm [9]. Their active modulator lengths are between 3-4 mm. Even though the $V_\pi L$ product for silicon MZM's are lower, their V_π is still higher as a result of shorter device length.

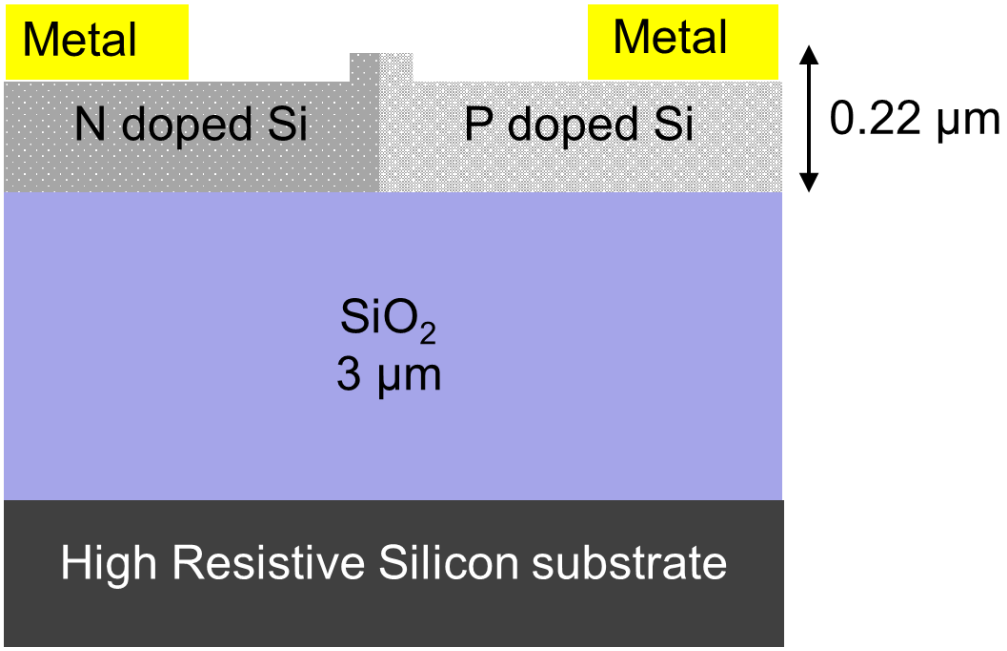

Figure 1 Cross section of silicon Phase Modulator

Silicon based MZM's are typically fabricated on high resistive silicon substrate to achieve lower electrical loss. Their resistivity is around 1-6 kΩ.cm. Low loss coplanar electrode lines have been demonstrated on these substrates [10] and subsequent integration of silicon modulator with these coplanar lines have demonstrated high speed MZM's [9]. [9] had a DC drive voltage of 7.5 V using 4.2 mm active modulator length and 11 dB/cm propagation loss. Device had reported a good 3 dB EO Bandwidth of 35 GHz. Most of the silicon based MZM's have been based on lateral PN junction approach with slight variation in the doping concentrations.

Using ring-based designs, low drive voltage of 2.5 V and 56 Gb/s data rate have been demonstrated [11]. These devices are sensitive to temperature variations and have a narrow optical bandwidth over which they can operate. There have also been some work based on vertical PN diode MZM's reported in the past [12]. [13] reported on the design of a vertical PIN silicon MZM with a low $V_\pi L$ of 0.74 V.cm and a simulated propagation loss of 42 dB/cm. Without inducing phase shift from external materials such as graphene or ITO, silicon based MZM suffer from high drive voltages and high propagation losses. Their mature processing technology and low cost appears to be one of the biggest attractive factors and has led to the commercialization of them.

1.3 III-V Modulators directly grown on Silicon

As of 2019, only the growth of GaAs/AlGaAs on Silicon is optimized and so advantages of having a GaAs based modulator on Silicon will only be discussed subsequently. Electron effective mass of GaAs is $0.067m_o$ while that of silicon is $0.26m_o$ [14]. So, for same amount of carrier concentration change, refractive index change is going to be higher in case of GaAs than silicon. Mobility of N doped GaAs is greater than 2500 while that of silicon is less than 800 and so for the same doping levels, free carrier absorption loss will be lower in GaAs based modulator when compared to silicon. With higher mobilities, semiconductor doped layer resistance could be lower which could be useful for improving the electrical bandwidth of travelling wave MZM's. As explained before, GaAs/AlGaAs material system exhibit Pockel's effect in addition to the free carrier plasma effect which can be used to reduce the V_π of the MZM's. AlGaAs with aluminum concentration greater than 20 % have band gap greater than 1.6 eV which is twice higher than the photon energy @ 1.55 μm. This could also

be used to design modulators capable of handling high optical powers with negligible two photon absorption.

1.4 Outline

The scope of this thesis is to investigate the possibility of using III-V growth technique on silicon substrate to develop efficient GaAs/AlGaAs MZM's based on Pockel's effect on silicon substrates.

Chapter 2 discusses the GaAs/AlGaAs MZM's epitaxial design, simulation results and fabrication procedure. Experimental optical transmission results of MZM's at low frequency, grown on both Silicon and GaAs substrates are then presented. High optical power handling capability of these devices on GaAs substrate are demonstrated with experimental proof of negligible optical absorption at a power of 160 mW being coupled into the modulator.

Chapter 3 discusses the challenges in designing a high speed MZM on silicon substrates. Advantages and disadvantages of the widely used coplanar electrodes are discussed. Modified electrode design based on microstrip structure is proposed along with the simulation results. Fabrication of these microstrip electrodes was developed using gold plating and BCB planarization techniques. Experimental results on the electrical loss and the dispersion of both the coplanar and microstrip electrodes are finally presented outlining the advantages of microstrip design over coplanar design for modulators on silicon substrates.

Chapter 4 explains the high-speed design of modulator explained in Chapter 2 along with the simulation and the experimental results. A modified design is proposed to improve the electrical bandwidth of the modulator along with the preliminary results on optical transmission along with the propagation loss. Simulations are then presented to discuss the improvement in bandwidth that could be achieved with the proposed design.

Chapter 5 discusses the fabrication of compact GaAs based waveguides directly grown on Silicon by selective oxidation of high aluminum content AlGaAs layers. Preliminary results on the propagation loss of the devices are presented. Possible future work to fabricate ultra-compact modulator by selective implantation of dopants into these waveguides are discussed and fabrication steps are analyzed.

Chapter 6 discusses my previous work based on InP MQW modulators grown on InP substrates. Focus of this work is the active passive integration using amorphous silicon (a-Si) waveguides and to reduce the coupling loss from the fibers. Tapers were designed and fabricated on a-Si waveguides to couple the light in and out of the InP MQW waveguides. Fabrication of the device is discussed along with the experimental results of the taper transition and the coupling loss.

1.5 References

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2 GaAs/AlGaAs based Modulators on Silicon Substrates

2.1 Introduction

Refractive index of certain materials such as Indium Phosphide (InP), Gallium Arsenide (GaAs) which lacks inversion symmetry, could be changed by applying electric field. With a doped semiconductor as the electrode for applying field and a PIN diode operating in reverse bias, various electro optic modulators have been demonstrated across different material systems. But for a low drive voltage modulator, bonding and substrate removal have proven to be a promising solution. Substrate removal enables to have thin intrinsic region which in turn leads to strong electric field combined with tightly confined optical mode. It involves bonding processed III-V epilayer onto transfer substrate such as semi-insulating GaAs and then removing the growth substrate [1]. But with the complexity involved with bonding, substrate removed devices remains challenging to be integrated with conventional foundry techniques.

Maximum index contrast between the different epilayers that could be grown across InP and GaAs at 1.55 μm ranges between 0.4-0.45. With that value, bottom cladding layer must be sufficiently thick to prevent the optical mode from leaking into the substrate which results in limitations in designing thin intrinsic region. There is always a tradeoff between simultaneously reducing the thickness of the intrinsic region (I-region) and increasing the overlap of the optical mode in case of substrate-on devices. Since conventional devices greatly reduce the processing complexity of bonding, substrate-on low drive voltage wide bandwidth modulators are desired with lesser complex fabrication process.

GaAs/AlGaAs material system have been widely suitable for variety of opto-electronic applications. Low drive voltage modulators have been demonstrated using substrate removal suitable for high speed operation [2]. Over the recent years, considerable progress has also been made over GaAs/AlGaAs epitaxial growth on Silicon substrate [3]. Direct epitaxial growth on Silicon would help in overcoming the cost and size limitation of III-V substrate. So, with a low drive voltage, substrate-on modulator design, it might be possible to demonstrate similar performance on epitaxially grown layers on silicon substrates at lower substrate cost. This chapter discusses and explains the design and operation of GaAs/AlGaAs based electro optic modulator operating at 1.55 μm epitaxially grown on Silicon substrates. Chapter begins with device description followed by processing flow. Chapter is concluded by experimental results of modulator performance of devices both on GaAs and Silicon substrates in low frequency. High optical power handling capability of these modulators are also discussed.

2.2 Device Description

With a PIN diode operating in reverse bias, it is possible to apply electric field across the intrinsic region(I-region). Drive voltage of an electro-optic phase modulator is directly and inversely proportional to the thickness of I-region and overlap of the optical mode with I-region respectively. Overlap should be maximized while simultaneously reducing the thickness of I-region and maintaining single mode condition for the waveguide.

Epilayers were grown by molecular beam epitaxy (MBE) at 600^{o}C on a semi-insulating Gallium Arsenide substrate (GaAs). Semi-Insulating substrate was used instead of doped substrate to reduce microwave electrical loss for high speed operation. For epitaxial growth on Silicon, mis-cut silicon substrate was used to reduce antiphase domains [4]. The

epitaxial layers were grown on (100) Silicon intentionally tilted 6° towards (111). Initially a 1 μm unintentionally doped GaAs on 1 μm unintentionally doped Ge buffer layer were grown via chemical vapor deposition (CVD) on silicon. The as-grown CVD buffer was found to contain a dislocation density of ~$2x10^8$ cm^{-2}. Before growing the device layers, two pairs of alternating layers of GaAs (0.2 μm)/AlAs (0.2 μm) were grown as etch stop layers. Following that, n^+ GaAs (0.1 μm), n $Al_{0.9}Ga_{0.1}As$, $1*10^{17}$ cm^{-3} (1.2 μm), unintentionally doped (UID) $Al_{0.2}Ga_{0.8}As$ (0.25 μm), UID $Al_{0.9}Ga_{0.1}As$ (0.02 μm), p $Al_{0.2}Ga_{0.8}As$, $4*10^{17}$ cm^{-3} (0.1 μm), n $Al_{0.9}Ga_{0.1}As$, $1*10^{17}$ cm^{-3} (1.2 μm) and n^+ GaAs (0.1 μm) were grown as the device layers. Device is electrically equivalent to two back to back diodes (NPIN) connected in series. To reduce the microwave loss due to p-doped layers, NPIN is preferred instead of a PIN design. Depending on the bias polarity, one of the diodes will always be forward biased and the other one will always be reverse biased. The forward biased diode will only carry small reverse leakage current since both the diodes are connected in series and hence most of the applied bias would drop across the reverse biased diode. Under high speed operation, it is equivalent to two capacitors in series. Since the I-region of top NP diode is thinner than the bottom PIN diode, capacitance of the top NP diode is much greater than the bottom PIN diode. Hence, the effective capacitance is approximately equivalent to the capacitance of the bottom PIN diode. Cross section of the epitaxial stack is also shown in Figure 2.

The core and the part of I-region are designed to be $Al_{0.2}Ga_{0.8}As$. $Al_{0.2}Ga_{0.8}As$ has a bandgap (1.673 eV) greater than twice the photon energy at 1.55 μm suitable to reduce two-photon absorption at high input powers. P and N region are designed to be $Al_{0.2}Ga_{0.8}As$ and $Al_{0.9}Ga_{0.1}As$ respectively. Doping in P and N regions were kept moderately low to reduce the propagation loss. Thin 0.02 μm UID $Al_{0.9}Ga_{0.1}As$ acts as the barrier to prevent carrier flow in

reverse bias. n^+ GaAs is used for making alloyed ohmic contacts to the top and the bottom diodes. The bottom and the top n $Al_{0.9}Ga_{0.1}As$ (1.2 μm) serve as the optical cladding and is sufficiently thick enough to reduce the optical mode overlap with the n^+ GaAs layer.

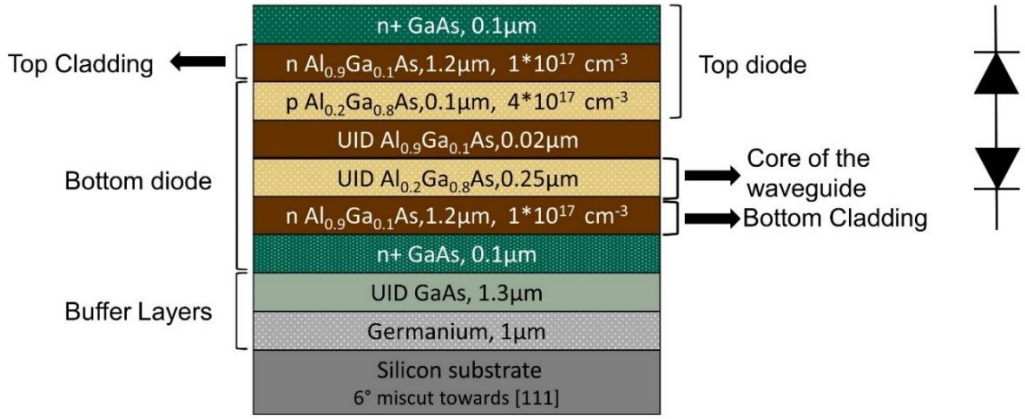

Figure 2 Epitaxial Layer Stack

Passive waveguide was designed to be a rib waveguide which is 1.9 μm wide and 1.2 μm deep. 1.2 μm deep etch includes 0.1 μm n^+ GaAs and 1.1 μm n $Al_{0.9}Ga_{0.1}As$. n $Al_{0.9}Ga_{0.1}As$ was not completely etched to maintain single mode condition for the chosen width of 1.9 μm. This would result in additional capacitance over the entire width of mesa structure due to the doping in the $Al_{0.9}Ga_{0.1}As$ layer. For DC and low frequency operation, additional capacitance wouldn't affect the modulator performance. Overlap of the optical mode with the etched sidewall is minimum with this design which is crucial for low propagation loss.

Optical mode profile and the cross section of the rib waveguide structure is shown in Figure 3. Optical mode field is intense in the bottom diodes I-region where the electric field would be maximum. Overlap of the optical mode with the individual epitaxial layers were calculated by computing the 3D mode profile using Rsoft and combining in Matlab. Overlap with the core under rib is 46.6% and 11.4% and 15% with top and bottom n $Al_{0.9}Ga_{0.1}As$

respectively. Overlap with P region is 13.3%. Further increasing the width of the rib waveguide or thickness of the I-region doesn't change the overlap significantly and might compromise the single mode condition.

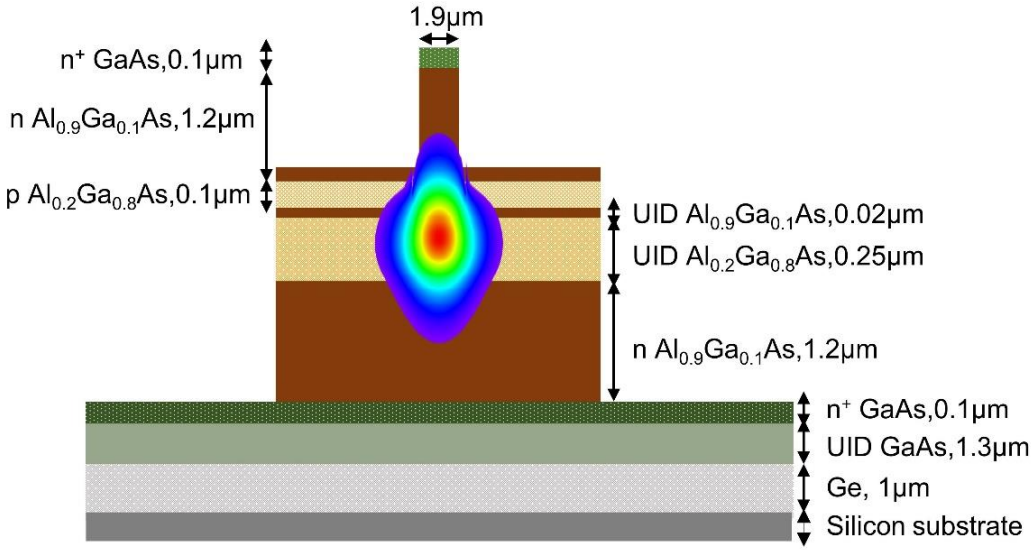

Figure 3 Passive Waveguide

2.3 Simulation

Contributions to the index change comes mainly from Linear electro-optic (LEO) and the plasma effect (PL). Contribution from LEO is dominant only after strong electric field is set up in the I-region. Depletion of charge in P and N regions contributes to PL effect. For the above optical design, band profiles and electric field were computed using SILVACO and optical mode profiles from Rsoft Beam Prop. Both the computed parameters were combined in Matlab to calculate the phase change as the applied reverse bias is increased.

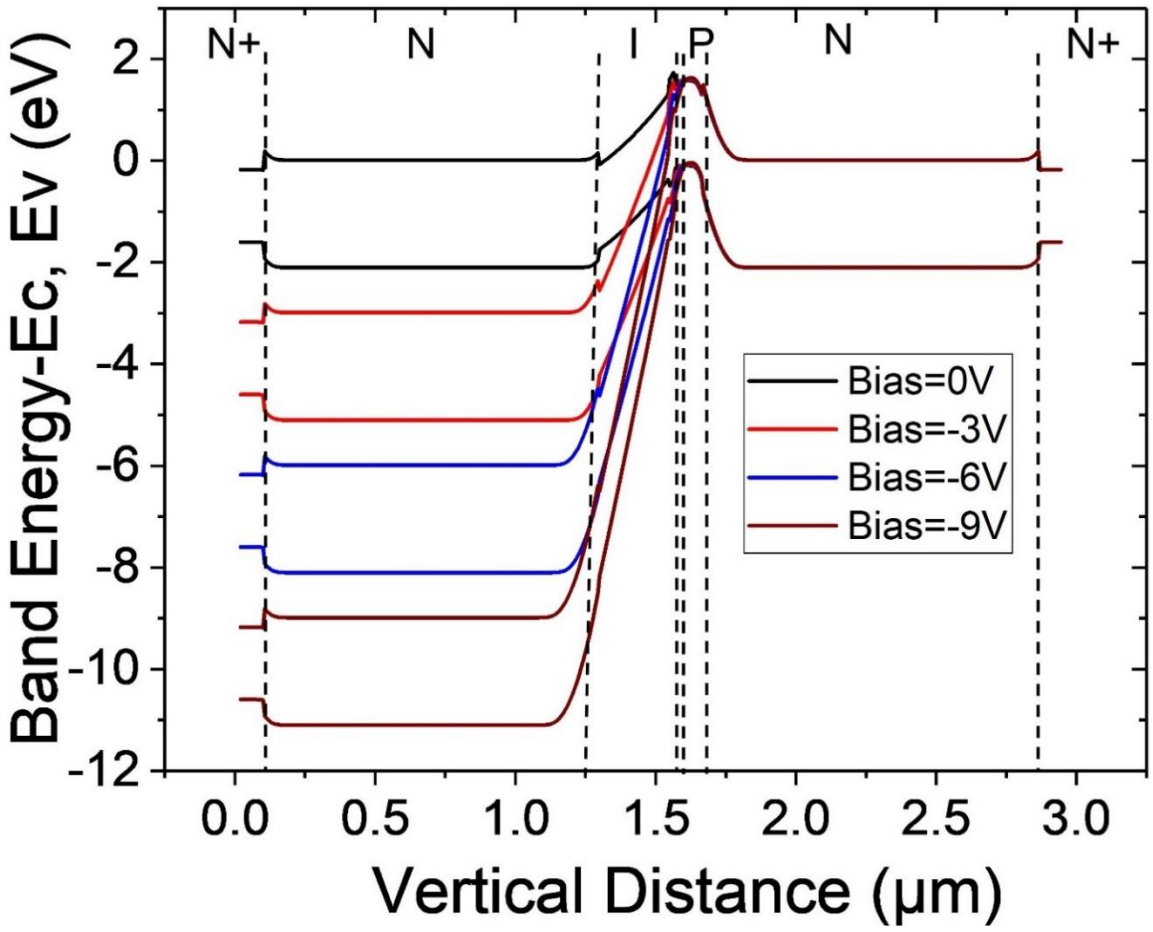

Figure 4 Band Diagram

For different bias voltages, band profiles and field distribution were calculated and is shown in Figure 4. Device biasing was set such that, the bottom thicker diode (PIN) is reverse biased under negative sweep. Under that biasing condition, most of the applied voltage drops across the bottom PIN diode as seen from the band bending. Un-intentional doping in the intrinsic region was assumed to be $1*10^{16}$ cm^{-3} in the simulation. With MBE growth, even lower background doping is possible in the intrinsic region.

As reverse bias is increased, there is depletion in doped layers. Since the bottom N layer is thick (1.2 μm), electric field will be maintained in the intrinsic region only until there

is charge in p $Al_{0.2}Ga_{0.8}As$ (0.1 μm). Once p layer is depleted, effective structure becomes like N-I-N design and current will start flowing between two n contacts. In Figure 5, simulated charge concentration for four different bias voltages 0, -3, -6 and -9 volts are shown. At zero volts, there is some charge spillage into the I-region due to band alignment which would eventually be depleted once the bias is increased. Since the applied bias drops only across the bottom PIN diode, there is no depletion in the top n $Al_{0.9}Ga_{0.1}As$. Thickness of the effective intrinsic region increases as much as 0.2 μm in the bottom n $Al_{0.9}Ga_{0.1}As$ layer. Similarly, maximum p doping almost drops to half at the bias voltage of -9V. As much as depletion will result in improving propagation loss of the device, increase in the thickness of effective I-region will increase the drive voltage. It is desirable to operate where thickness of effective I-region is close to the design value to get maximum modulation efficiency.

Effective phase change as the reverse bias is increased for an electrode length of 1cm was computed by calculating the electric field values along with the electro optic coefficient r_{41}. From Figure 6, most of the index change is contributed from the linear electro optic effect. Index change due to depletion of charge carriers is minimum when compared with LEO. For a device biased at -7V, when an input electrical signal is applied to only one arm of the interferometer, drive voltage for π phase change is 2V. For a push-pull operation where equal and opposite sinusoidal signal are applied to both arms of the interferometer, phase change would be opposite in both the arms and hence the total phase change required is only $\pi/2$. Drive voltage would then cut down to 1V. With this design, $V_\pi L$ product of 1 V.cm is possible under push-pull operation.

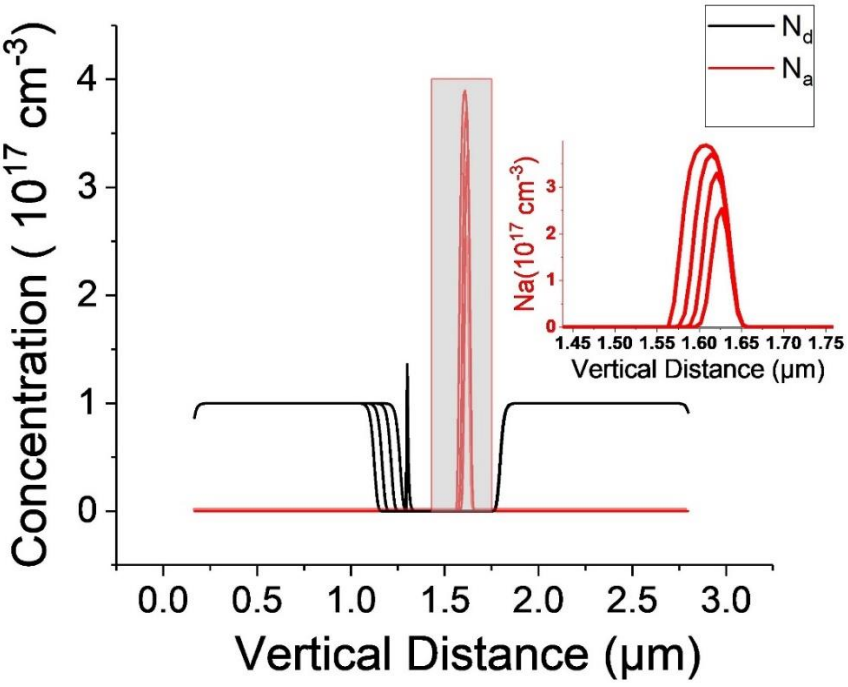

Figure 5 Charge Depletion vs Bias

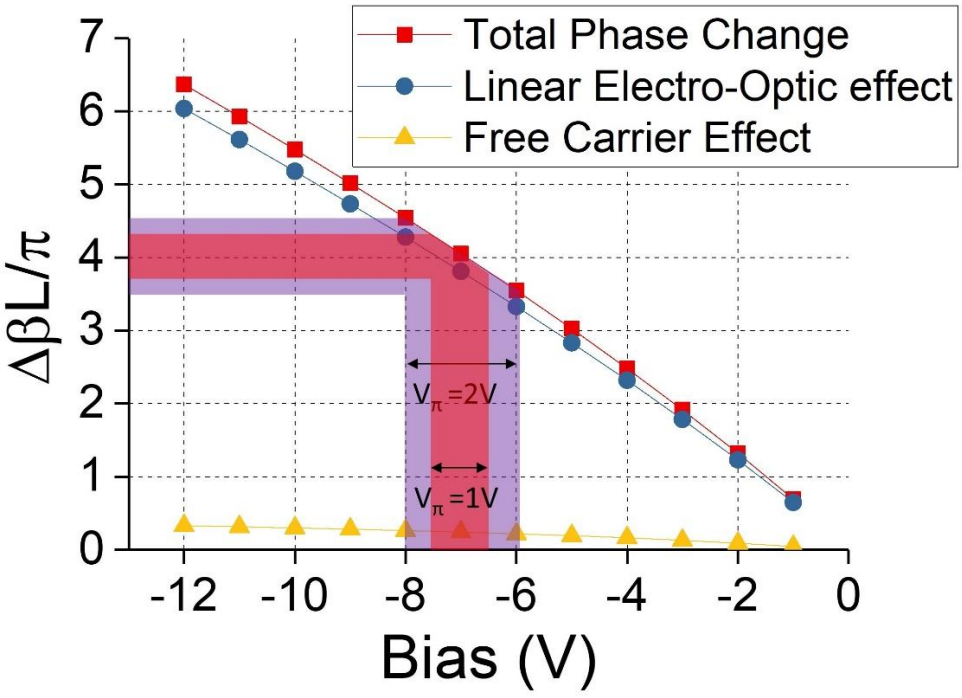

Figure 6 Phase change vs Applied Bias for 1cm device

2.4 Fabrication

For devices grown on (001) substrates, refractive index change due to linear electro optic effect will be positive and negative on two cleavage planes respectively. In order for the effects from LEO and PL to add up, waveguide has to be aligned along [110]. Before starting the fabrication, crystallographic planes has to be determined to correctly align the waveguide. In case of GaAs, depending upon the atomic density, different crystallographic planes have different etch rates when subjected to certain wet etchants. Epitaxial layers were completely removed to reach the growth substrate. With 200 nm silicon nitride hard mask patterned using photo resist, sample was etched in H_2SO_4:H_2O_2:H_2O:1:8:1 solution for 5 minutes. Microscope pictures of etched features are shown in Figure 7.

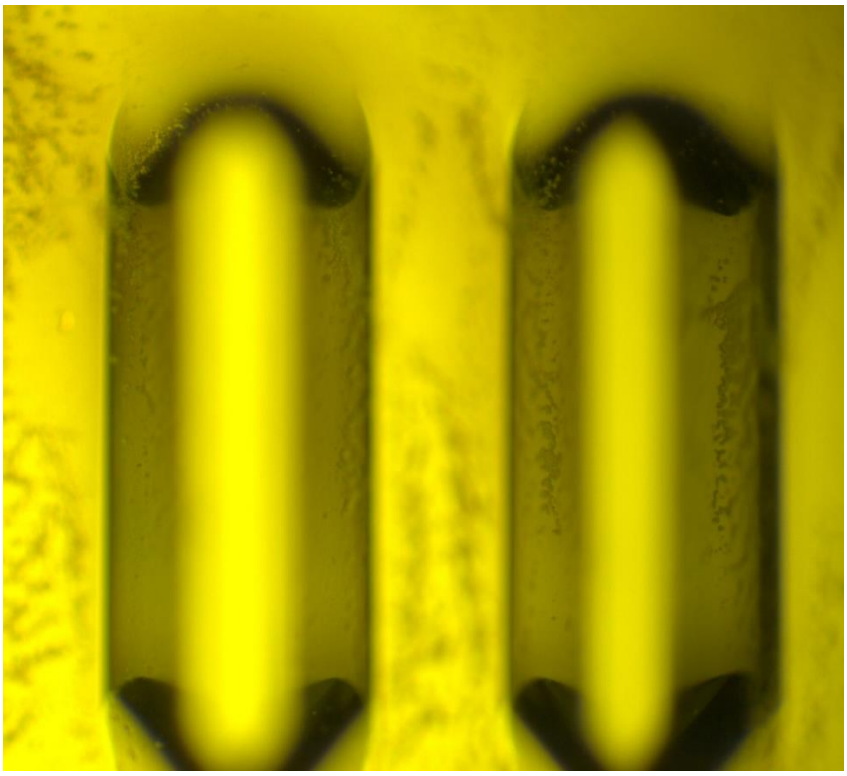

Figure 7 Crystal Orientation test

Along one of the crystallographic planes [$1\bar{1}0$], etch rate is faster than the other and had led to significant under cut. There is a trapezoidal profile along the other plane

corresponding to a slower etch rate [110]. Waveguides were aligned along [110] (parallel to major flat) during the fabrication. Since GaAs grown on Silicon should follow the same crystal orientation that of silicon, waveguides were directly aligned parallel to the major flat of the silicon wafer.

Process flow is shown in Figure 8. Processing was started by lifting off Ni/Ge/Au/Ni/Au 5/18/132/20/1200 nm contacts to highly doped n^+ GaAs. 500 nm thick PECVD oxide was used as an oxide hard mask for waveguide etching. Oxide was patterned using CHF_3 plasma using ICP etcher and a photo resist hard mask. After stripping off the photoresist, rib [n^+ GaAs -(0.1 μm) and n $Al_{0.9}Ga_{0.1}As$ (1.1 μm)], 1.9 μm wide was etched using Cl_2/N_2 plasma. Mesa, 20 μm wide was dry etched and stopped on bottom n $Al_{0.9}Ga_{0.1}As$. Remaining n $Al_{0.9}Ga_{0.1}As$ was wet etched using BHF. Because of the undercutting of $Al_{0.9}Ga_{0.1}As$, effective mesa width reduced to 16 μm. Similar contacts as the above were lifted off from the bottom n^+ GaAs. Both the contacts were annealed at 430^{o}C for 30 seconds in forming gas for making ohmic contacts. Sample was then subjected to selective (50 by 50 μm^2) proton implantation to isolate the arms of the interferometer. Three different implantation schedules with different energies were introduced to isolate n^+ GaAs, n $Al_{0.9}Ga_{0.1}As$ and p $Al_{0.2}Ga_{0.8}As$ respectively. Bottom n^+ GaAs is far deep for the proton implantation to reach and so, only the top layers were subjected to implantation. Sample was then planarized with 4.4 μm thick BCB @ 250^{o}C for 1 hour. BCB was blanket etched without any pattern in CF4 plasma until the top contacts were reached. At this point, Ni/Au 50/500 nm metal pads were lifted off for the top contacts. Finally, BCB is etched to reach the bottom metal contacts.

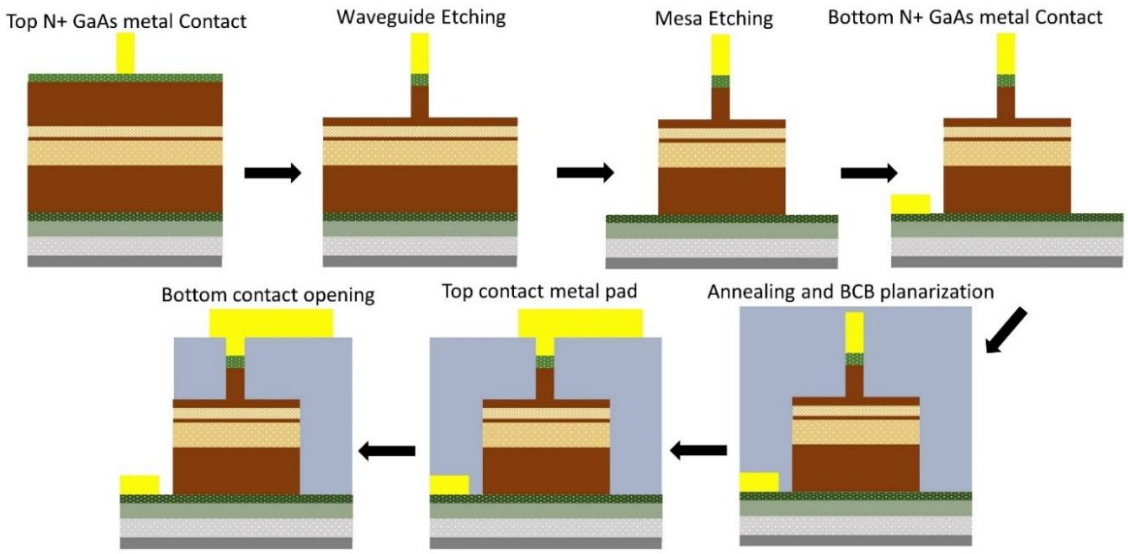

Figure 8 Processing flow for Modulator on Silicon

For devices grown on GaAs substrate, thicker silicon dioxide (1.6 μm) was deposited instead of BCB planarization approach to reduce stress related issues. Plan was to test the high optical power handling capability of the device and BCB sometimes gets damaged when exposed to high optical powers. Contacts to both and top and bottom n^+ GaAs were then reached by etching oxide with a photo resist hard mask. Bigger metal pads were finally lifted off for the top metal contact. For implantation, three different proton schedules with energies 170,130,80 KeV and one boron schedule with 70 KeV energy was used to isolate the arms of the interferometer. To simulate the penetration depth of implanted ions, SRIM software (Stopping and Range of Ions in Matter) was used with an Ion angle of 7 degrees. Ion penetration profile simulated is shown in Figure 9. For implantation, photoresist was used as the hard mask.

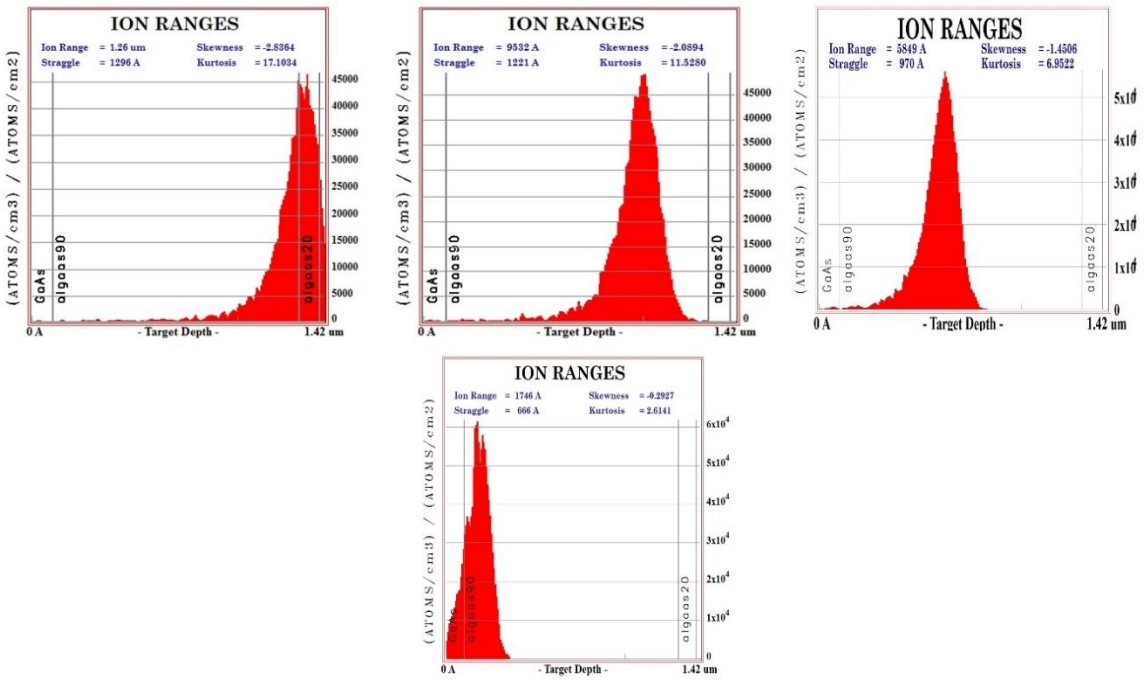

Figure 9 Implantation profile

2.5 Results-GaAs Substrate

Devices were tested both electrically and optically. Both the top and bottom GaAs contacts were tested to be ohmic , both on GaAs and Silicon substrates. TLM measurements were made on patterns on bottom N GaAs on the GaAs sample. Contact resistivity was calculated to be $1.47*10^{-6}$ $\Omega.cm^2$. Devices were cleaved and excited by a 2.5 μm spot size fiber at the input and the output response was measured using InGaAs photodetector after passing thorough a 20x microscope objective lens. SEM picture of cleaved facet is shown in Figure 10. As said before, thick oxide was used as a passivation in GaAs substrate instead of BCB planarization. Even with thicker oxide approach, there are little number of cracks appearing in bottom n $Al_{0.9}Ga_{0.1}As$. These facets weren't AR coated. Reason for the cracks is unclear and could be attributed either due to oxidation of high aluminum containing layers or stress due to cleaving.

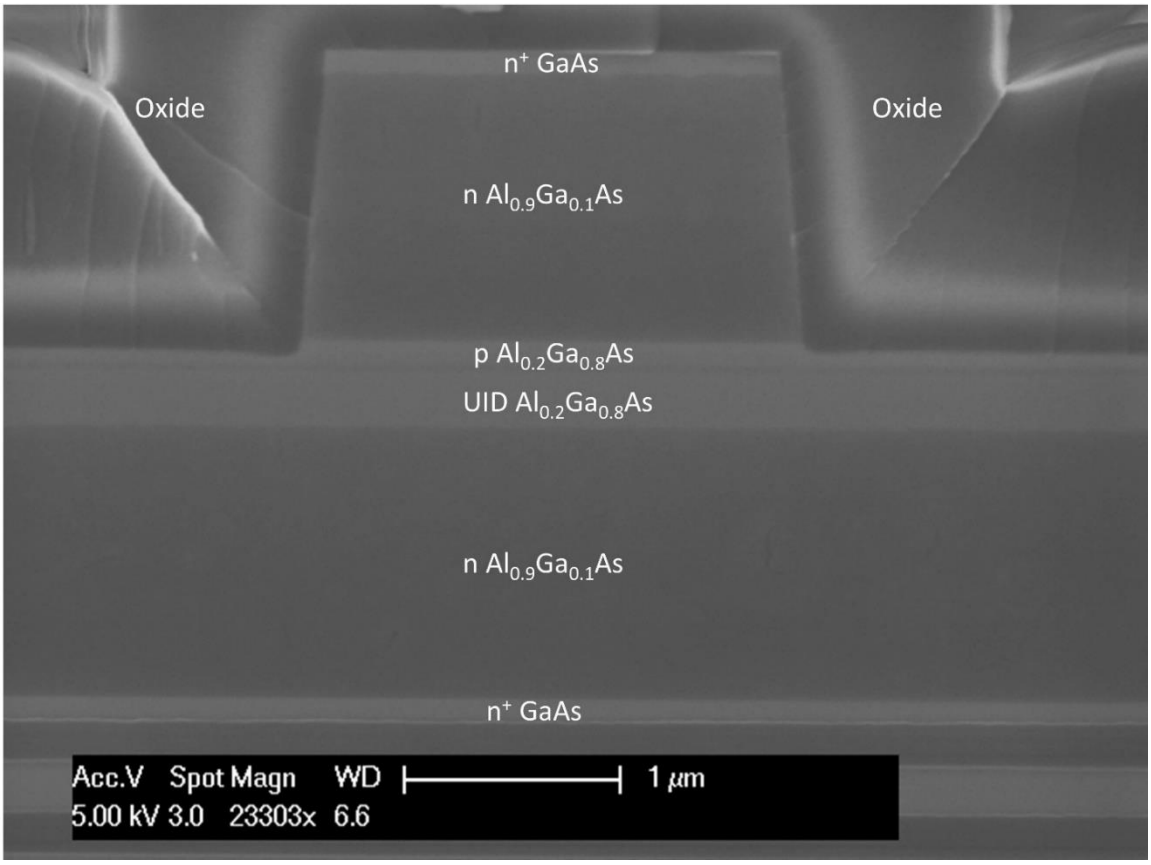

Figure 10 GaAs Substrate cleaved facet

For push pull operation, arms of the interferometer must be isolated to apply voltage to arms independently. Only the modulator on silicon substrate was subjected to proton implantation. For devices on GaAs substrate, high resistance of top *n* $Al_{0.9}Ga_{0.1}As$ cladding in narrow and long waveguides that join in the *y*-branch was used to provide isolation. Bottom n^+ GaAs is too heavily doped and wide to provide such isolation between the arms. So, *n* layer of bottom *pin* diode was kept at ground potential during the measurements. The measured resistance between the top *n* contacts of the arms of a MZM is greater than 0.2 MΩ and limits the current flow between top *n* contacts to less than 100 μA. Current and capacitance results as reverse bias voltage being varied for a 10 mm MZM is shown in Figure 11.

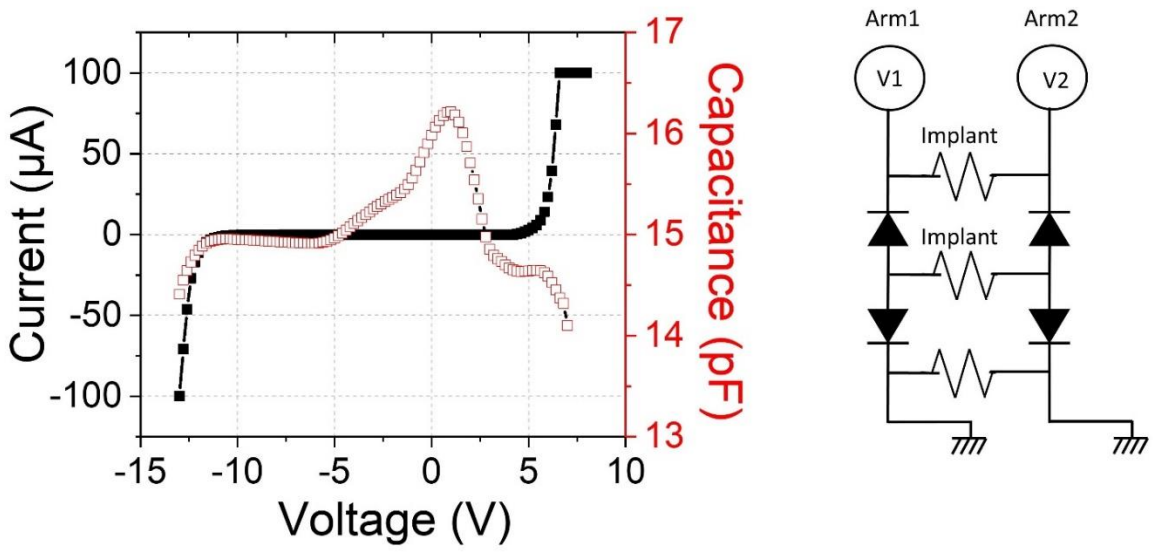

Figure 11 IV & CV- 10mm MZM

For the above electrical configuration, along the positive sweep, the top NP diode is reverse biased and along the negative sweep, the bottom PIN diode is reverse biased. Along the negative sweep, the device doesn't break down until negative -12 V and there is negligible current flow until that bias point. This rule out any index change related to heating effects. After -12 V, P layer completely depletes and current starts to flow between two N contacts. Along the positive sweep, because of the thin I-region of the NP diode, device breaks down quickly at around 5.5 V. Capacitance initially doesn't flatten out because of the unintentional doping in the I-region. As the reverse bias is increased on both the directions, charge in the I-region gets depleted until eventually capacitance flattens out. As the P layer completely depletes, capacitance starts to change rapidly in accordance with the current.

From the capacitance measurement of a square test structure with 110 by 200 μm dimension, capacitance per unit area is measured to be $1.88*10^{-16}$ F/μm^2. Dielectric constant of $Al_{0.2}Ga_{0.8}As$ ($\in_{0.2}$) and $Al_{0.9}Ga_{0.1}As$ ($\in_{0.9}$) are 12.556 and 10.372 respectively, calculated from linear interpolation of dielectric constant of GaAs and AlAs. Capacitance of the bottom

thicker diode is itself a series combination of barrier $Al_{0.9}Ga_{0.1}As$ ($t_{0.9} = 0.02\ \mu m$) and the core $Al_{0.2}Ga_{0.8}As$ ($t_{0.2} = 0.25\ \mu m$)

$$\frac{C_2}{A} = \epsilon_0 \left[\frac{\epsilon_{0.2}\epsilon_{0.9}}{\epsilon_{0.2}\ t_{0.9} + \epsilon_{0.9}\ t_{0.2}}\right]$$

$$= 4.05 * 10^{-16}\ {}^{F}/_{\mu m^2}$$

From the measured value of capacitance and simulated value for the thicker PIN diode, capacitance of NP diode is calculated to be $3.508 * 10^{-16}\ {}^{F}/_{\mu m^2}$. From the band diagram profile simulated using Silvaco, there is a depletion region along the thin NP mostly depleted along the n $Al_{0.9}Ga_{0.1}As$.

For a 10mm device with 1.9 μm waveguide width, total capacitance neglecting the parasitic capacitance is supposed to be 3.57 pF and for a 16 μm mesa width, the capacitance is supposed to be 30 pF. Rib waveguide etch depth was designed to be 1.3 μm (0.1 μm n^+ GaAs + 1.2 μm n $Al_{0.9}Ga_{0.1}As$). Loading effects in ICP leads to etch rate non-uniformity and because of that, etch proceeded into p $Al_{0.2}Ga_{0.8}As$ in some parts of the wafer. Effective area for the capacitance is 1.9 μm by 10000 μm in some parts of the devices and 16 μm by 10000 μm in the remaining parts of the devices where 16 μm is the width of mesa structure. Thus 14.9 pF capacitance for a 10-mm device is due to the parallel combination of device capacitance with different areas and parasitic capacitance due to the overlap of metal pad and doped semiconductor layers.

A sinusoidal modulating signal with a DC offset was applied for measuring the optical response. Sinusoidal modulating signal with equal amplitude and opposite polarity was applied to both arms of the interferometer for push pull measurements. The DC bias applied to both arms was the same. Normalized transfer function of an MZM with 1 cm long arms at

1.55 μm is shown in Figure 12. Drive voltage at -4 V bias is 2.16 V and 1.11 V under single arm and push pull drive respectively. Figure 13 shows the normalized transmission of the same device at two other reverse biases under push pull drive. Increasing the reverse bias to 8 V results in V_π of 1.01 V which is about 10% less compared to V_π under 4 V reverse bias. V_π goes up to 1.3 V at 2 V reverse bias, which is about a 20% increase compared to 4 V reverse bias operation and a 30% increase compared to 8 V reverse bias operation. This bias dependent drive voltage arises due to unintentional doping in the I-region. There is charge in the *i*-region as observed in the capacitance behavior, which reduces the electric field and its overlap with the optical mode.

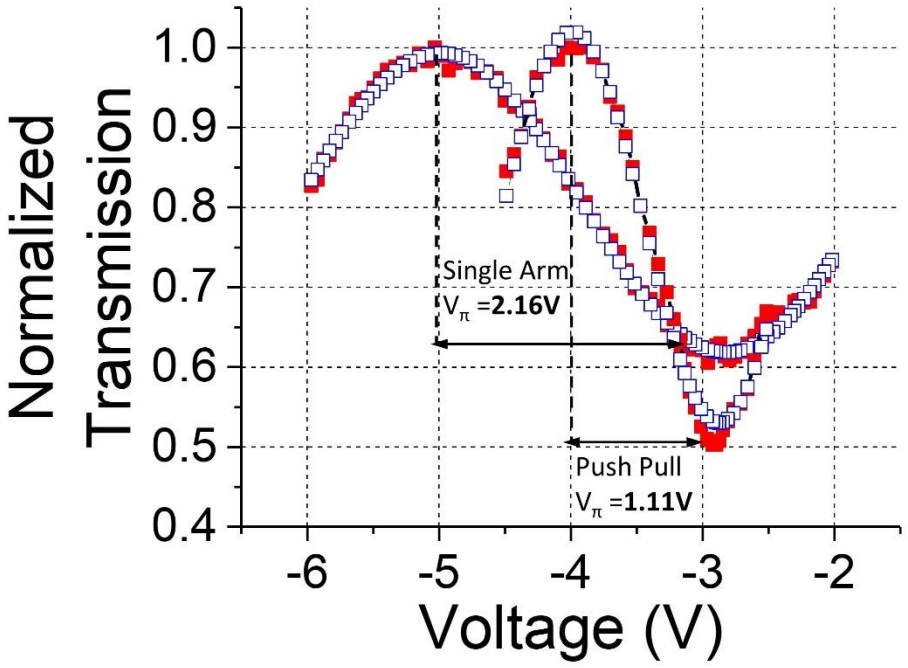

Figure 12 1 cm MZM on GaAs Substrate optical response @ bias=-4 V. Blue is the measured data and red curve is the fit with MZM transfer function.

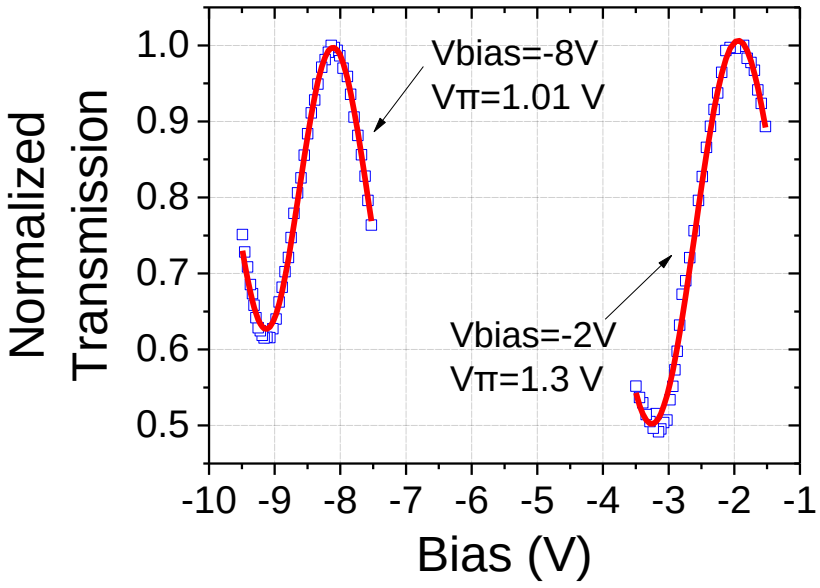

Figure 13 1 cm MZM on GaAs Substrate optical response @ bias=-2 V and -8 V. Blue is the measured data and red curve is the fit with MZM transfer function.

This increases V_π until all the charge is swept away. This happens after 5 V reverse bias. Change in V_π with bias voltage is negligible after this bias. Operation in this bias range is desirable since it not only gives the lowest V_π but also reduces the free carrier absorption due to depletion of holes in the *p* layer. On chip propagation loss is estimated to be ~ 4-5 dB/cm based on Fabry-Perot measurements. This is also a conservative measurement since the fringe visibility is reduced due to stray light. A major contributor to this loss is found to be the metal running along the waveguide sidewall connecting the top contact to the contact pads. Extinction ratio is low and around 3 dB. The main limitation of the extinction ratio is due to the deep mesa etch around waveguides. This provides a wide high index region, which acts as a multi-mode waveguide. During the input excitation the modes of this mesa waveguide are inevitably excited and travel from the input to the output. However, their overlap with the applied electric field is limited and they experience minimal modulation. This

provides at the output an unmodulated light level and decreases the extinction ratio and makes it somewhat coupling dependent. Furthermore, even under modulation, the higher order mode generated in the output waveguide after the *y*-branch leaks into and is trapped in this mesa waveguide. Some of this light is detected along with the modulated light in the output waveguide and reduces the extinction ratio. Appropriate mode transformers should eliminate this problem.

From Silvaco simulation, drive voltage under push-pull operation is 1 V. Maximum index change is contributed from linear electro optic effect. Drive voltage for an electro optic modulator operating under push pull in its simplified form is given as $V_\pi = \frac{\lambda}{2L}\frac{t}{n_{eff}^3 \Gamma r_{41}}$where λ is the wavelength, t is thickness of I-region, L is the length of electrode, n_{eff} is the effective index of fundamental mode, r41 is the electro optic coefficient and Γ is the overlap of the optical mode with I-region. With λ=1.55 μm, t=0.27 μm, L= 1 cm, n_{eff}=3.077, r_{41}=1.46 pm/V and Γ=0.466, drive voltage is 1.055 V which is close to experimental and the simulated values from commercial solvers.

In order to investigate the optical power handling capability of the modulator a phase modular optical transfer function and current voltage characteristics were measured at increasing optical input powers. The output of a 1.55 μm DFB laser was amplified using a high optical power fiber amplifier. The fraction of the input power that couples into the waveguide depends on the coupling loss. This loss has two components. One is the reflection from the facet and the other is the mode mismatch loss between the waveguide mode and the tapered fiber mode. Reflection loss is estimated to be around 1.3 dB per facet. Calculations indicate a mode mismatch loss of about 6.2 dB per facet. Therefore, total coupling loss per facet is around 7.5 dB. This means only about 18% of the optical power available from the

source enters the waveguide and is referred to as coupled input power. Figure 14 shows a 5.5 mm phase modulator and its transfer function as a function of applied voltage which corresponds to a coupled input power of 35 mW. In this case, output power of the modulator coupled to a detector is 3 mW. In this measurement, lower *pin* diode is reverse biased.

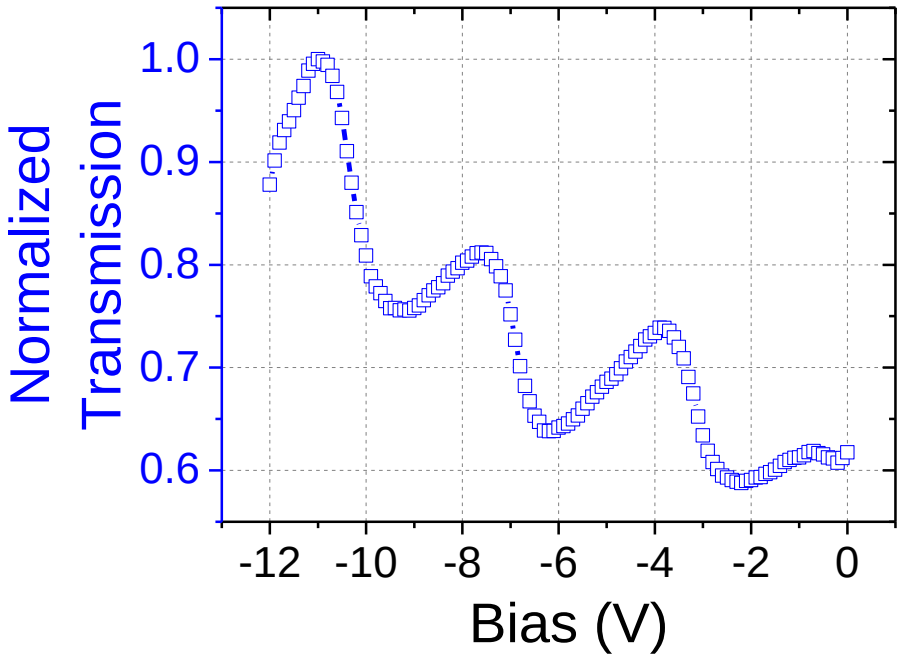

Figure 14 Normalized transfer function and the current through a 5.5 mm long phase modulator at 1.55 µm as a function of applied voltage when coupled input power is 35 mW

Transfer function of this phase modulator is as expected and the voltage span between two adjacent peaks corresponds to a π phase shift. Hence, this voltage is the same as V_π of an MZM under single arm drive. In this case V_π=3.78 V which corresponds to a $V_\pi L$ product of 2 V-cm under single arm and 1 V-cm under push pull drive. This agrees with the result discussed earlier. The current voltage characteristics of a 6 mm long phase modulator when input power is increased is shown in Figure 15. There is some evidence of increased absorption as input power increases, especially when the electric field is the highest. Increased

absorption increases the device current due to photo detected current. However, even when the coupled input power is 160 mW, increase of the current due to absorption in the desired operation region of less than 10 V bias is less than 5 μA. This indicates minimal absorption at high input optical powers demonstrating the suitability of the device for high optical power handling.

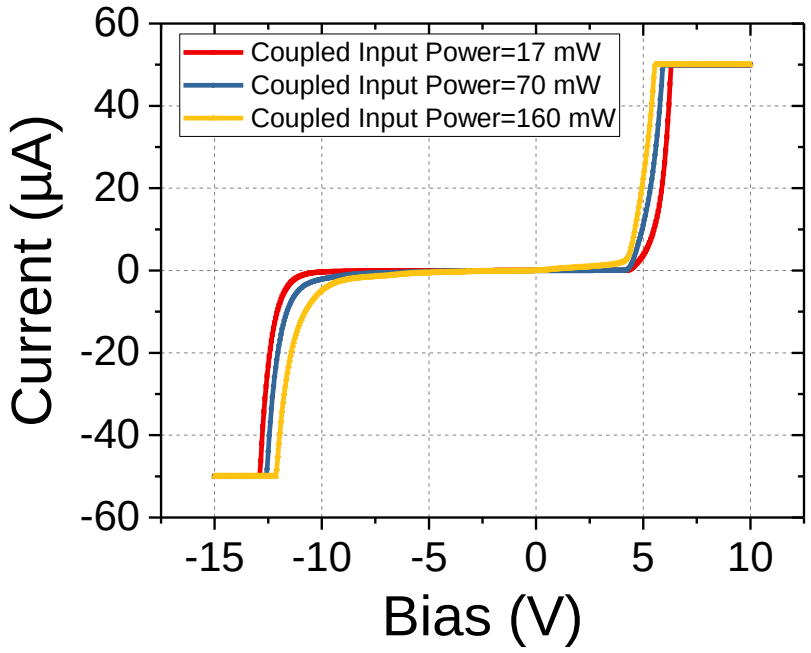

Figure 15 Current as a function of voltage applied at different input power excitations for a 6 mm long phase modulator

2.6 Results-Silicon Substrate

Silicon substrate was 750 μm thick and it was near to impossible to cleave manually. Polishing the facet resulted in more than expected junk near the facet. Depending on the perfection involved in polishing, both the facets may not be parallel to each other and could be tilted. Because of these issues, silicon substrate was lapped down to 200 μm in thickness and then manually cleaved by hand. Even though this approach had some issues related to fragility of thin substrate, this approach was giving reasonably acceptable optical facets.

Optimum final thickness should be between 180-230 μm to balance fragility issue and to get decent cleaving. Cleaved facet is shown in Figure 16.

Applying a positive voltage to top n^+ GaAs reverse biases the NP diode and a negative voltage reverse biases the bottom PIN diode. Current and capacitance result of 5 mm electrode device is shown in the Figure **17**. Current is only in the range of 0.1 μA until the break down point which also indicates good quality epitaxial layers.

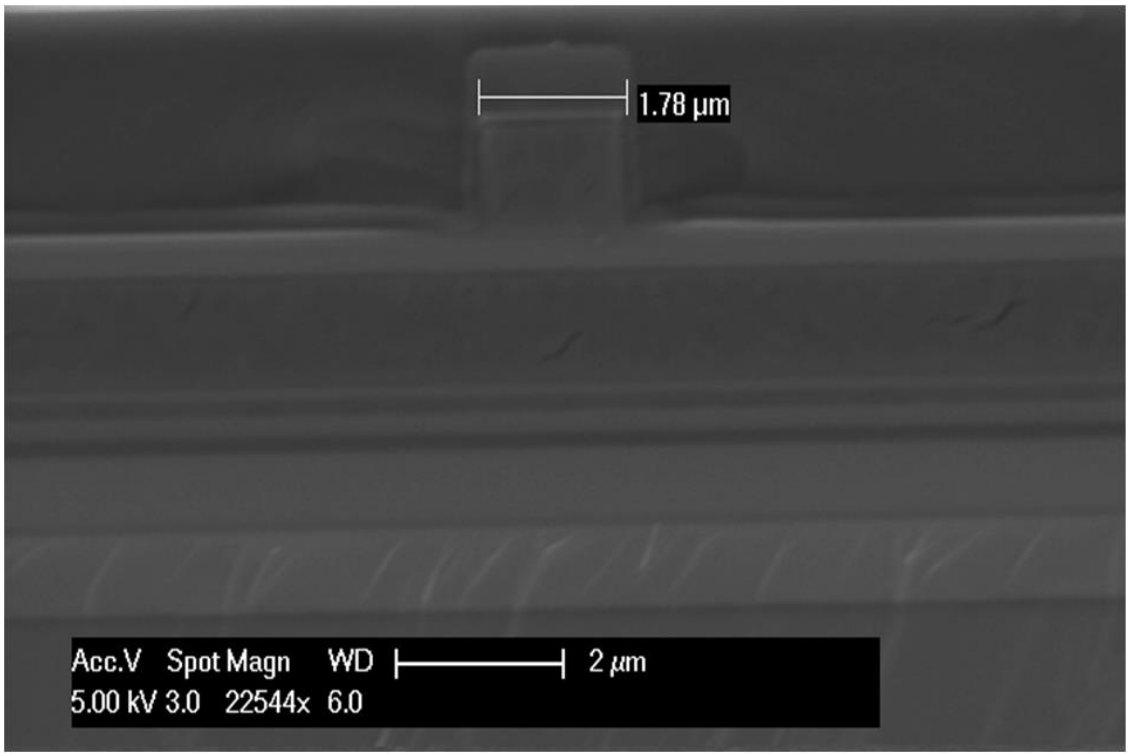

Figure 16 GaAs on Silicon-Facet

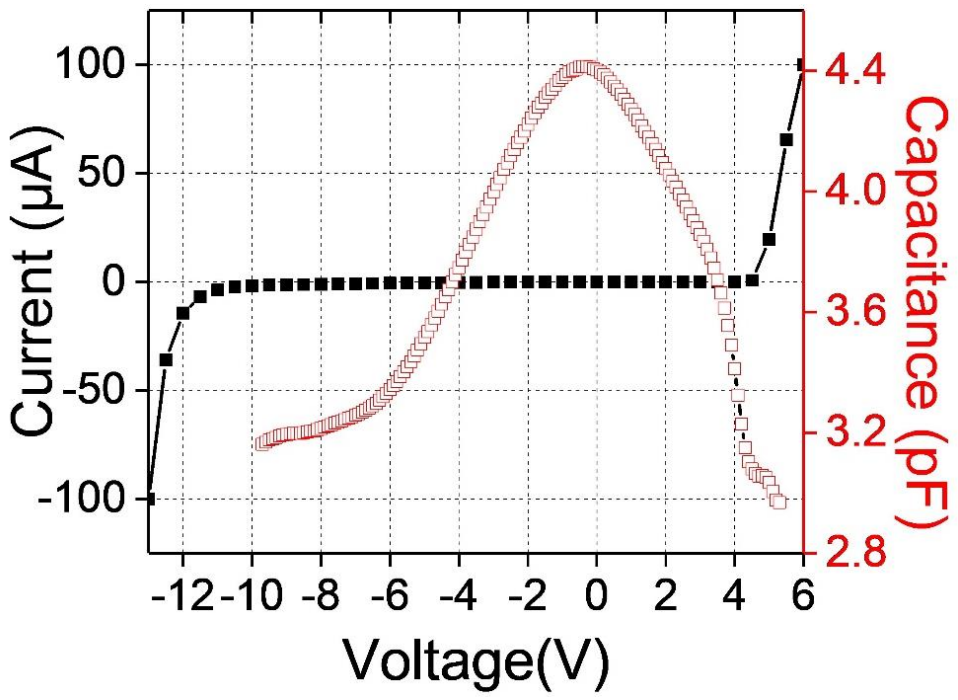

Figure 17 GaAs on Silicon-5mm CV and IV

As explained in GaAs substrate section, capacitance contribution comes from wider mesas in some section and narrow waveguide width in some sections due to etch rate non-uniformity. Capacitance decreases rapidly for both diodes as reverse bias increases. This indicates depletion of p and n layers as well as the sweep out of charge due to unintentional dopants in the I-region of pin diode. Capacitance of the pin diode starts to flatten out after 6 V reverse bias. This indicates full depletion of the I-region and any further reduction is due to depletion of *p* and *n* layers. Furthermore, there is depletion of the *p* layer in the core, which helps to reduce the free carrier absorption. In case of high-speed operation with travelling wave electrodes, device operation in flat capacitance region is needed for velocity matching between the microwave and optical signal. Background doping is higher in epi-layer grown on silicon than on GaAs substrate.

IV characteristics and optical transfer function of an intensity modulator with 4 mm long electrodes is shown in Figure 18. IV behavior is very similar to the data presented in

Figure **17**. In the optical transfer function dots are the data points and the continuous curve is a curve fit. Based on this curve fitting, when the device is biased at -5 V, the drive voltage under single arm and push pull operation is 7.4 V and 3.6 V respectively. V_π shows bias dependence. It is observed that modulation becomes more efficient as reverse bias increases as evidenced by decreased V_π in the higher reverse bias region. This is due to sweep out of the unintentional charge in the I-region. Under lower reverse bias V_π is higher. This is related to unintentional doping as evidenced in the CV data under lower reverse biases. At lower reverse biases, this charge screens the electric field as well as reducing the overlap of the field with the optical mode. These two effects increase V_π. Very negligible current indicates no index change due to device heating or carrier injection.

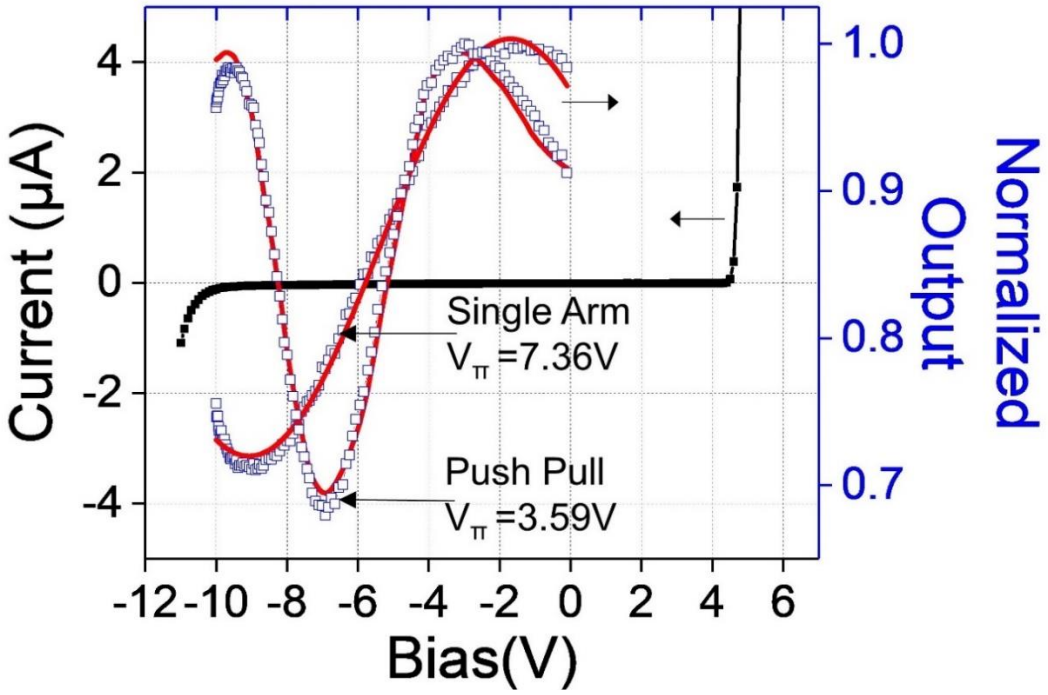

Figure 18 IV characteristics and optical transfer function of an MZM for 4 mm electrode at 1.55 μm

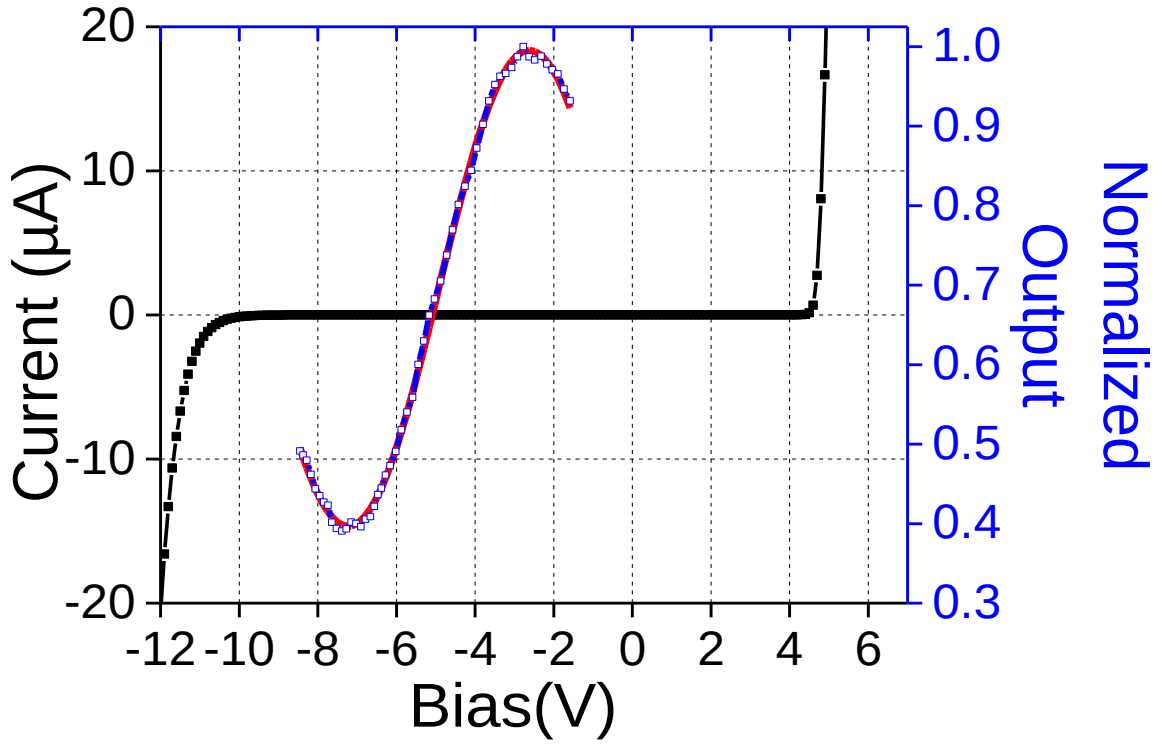

Figure 19 IV characteristics and normalized optical transmission of a 7 mm long Fabry-Perot modulator with 7 mm long electrodes at 1.55 μm

Figure 19 shows the normalized transmission of a Fabry-Perot modulator along with the IV characteristics. Fabry-Perot modulator is formed between the input and output facets of a straight waveguide. In this case, both the length of the modulator and the electrode are 7 mm. Points show the data taken at 1.55 μm and continuous curve is the fit. Under 5 V reverse bias V_π is 4.6 V. A push pull driven MZM using this phase modulator in the arms would have a V_π of 2.3 V. This corresponds to a drive voltage-length product ($V_\pi L$) of 1.5±0.1 V-cm. This data also indicates on chip propagation loss of less than 1 dB/cm assuming regular GaAs facet

reflectivity. This is an estimate due to presence of mesa modes, which affect the fringe contrast, but shows a very favorable propagation loss.

2.7 Summary

In this chapter, optical transmission and electrical results based on first experimental demonstration of electro-optic phase modulators in GaAs/AlGaAs epitaxial layers grown on Silicon substrates was presented. V_π of 4 mm MZM under single arm and push pull scheme was 7.4 V and 3.6 V. This corresponds to 1.5±0.1 V.cm modulation efficiency. Data on 7 mm long electrode Fabry-Perot phase modulators indicate 2.3 V Mach-Zehnder modulators are possible. This data also indicates less than 1 dB/cm on chip propagation loss under 5 V reverse bias. These results are comparable to the best-reported results in bulk GaAs/AlGaAs modulators. Devices grown on GaAs substrates had better results in terms of the drive voltage. Modulators with 1 cm long electrodes have 1 V V_π. The lowest bandgap in the device is larger than twice the photon energy at 1.55 μm. This eliminates material absorption including two-photon absorption. Modulator performance remains unchanged under coupled input optical powers approaching 160 mW.

2.8 References

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3. Microstrip Electrodes for Electro-Optic Modulators on Silicon Substrates

3.1. High Frequency Device Design

In the previous chapter, low frequency operation of GaAs/AlGaAs modulator directly grown on silicon substrate was discussed and results were explained. In this chapter, various criteria for high frequency modulator design will be discussed along with experimental results. An electro-optic modulator's operation is electrically equivalent to a diode operating in reverse bias. Electric field along the reverse bias creates a refractive index change based on Pockel's effect which in turn is converted to an intensity modulation using Mach-Zehnder modulator (MZM). A diode could be modelled as a RC circuit as shown in Figure 20 where C is the capacitance of the diode and R is the resistance associated with contacts and semiconductor doped layers. In low frequency operation, all the applied voltage drops across the reverse biased diode because of its high resistance. However, as the frequency increases, capacitive impedance decreases resulting in an overall impedance reduction.

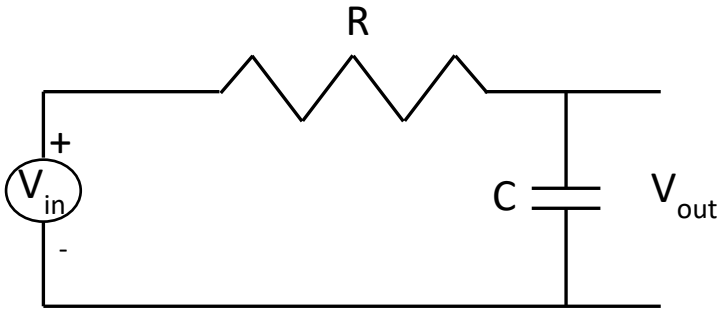

Figure 20 RC circuit

The above circuit acts like a low pass filter. At low frequencies, input voltage appears across the capacitor because of its high resistance and at high frequency, voltage drop across the resistance increases, thus acting like a filter. Impedance of the above RC circuit is given by

$$Z = \sqrt{R^2 + X_C^2}$$

Where $X_c = \frac{1}{2\pi f C}$

$$V_{out} = V_{in} * \frac{X_c}{\sqrt{R^2 + X_C^2}}$$

At high frequencies, for the applied voltage to be dropped across the capacitor, R << X_c. This cut-off frequency is given by $f_c = \frac{1}{2\pi RC}$. This frequency defines the intrinsic device band width of the modulator.

In case of lumped modulators such as Electro-Absorption Modulator (EAM), active modulation length is much less than the electrical wavelength, so that the applied voltage is considered to be uniform across the transmission line [1]. However, for longer devices, this is not the case. Travelling wave electrodes are used in case of electro-optic modulators where the modulation length is at the order of millimeters [2]. Unloaded transmission line, usually a coplanar electrode runs parallel along the optical waveguide with its microwave velocity greater than the optical group velocity and its line impedance greater than 50 ohms. Modulator diode sections are electrically isolated in short lengths and are periodically connected to the unloaded line as capacitive loading thereby reducing its impedance and velocity. Since these are periodic structures, it creates a bragg cut off frequency given by $f = \frac{V_{ph}}{2l}$ where v_{ph} is the phase velocity and l is the length of periodic diode sections [3, 4]. For frequencies less than

the cut-off frequency, transmission line would be less dispersive. Isolation of diode sections also ensures that the microwave axial current doesn't flow along the waveguide direction and are carried out by the unloaded line. With proper design of epitaxial layer, it's possible to simultaneously achieve both velocity and impedance matching [5]. When the velocity is matched, electro-optic bandwidth is limited by the electrodes microwave loss.

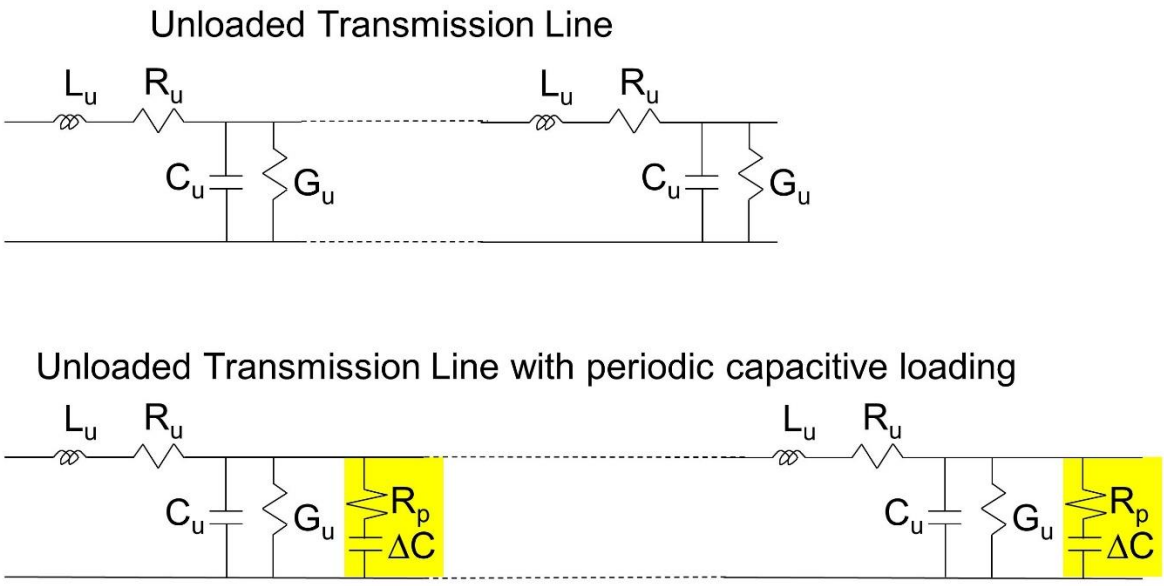

Figure 21 Transmission line equivalent circuit

Equivalent circuit of both unloaded and loaded transmission lines are shown in Figure 21. L_u, R_u, C_u and G_u are inductance, resistance, capacitance and the conductance per unit length of unloaded transmission line. R_p and ΔC are resistance and capacitance associate with the diode section. Contribution to R_p comes mainly from the doped semiconductor layers and the contact resistances. The above circuit with diode section and unloaded line could be converted in terms of impedance and admittance as shown in Figure 22. It could be solved to yield the loss and the propagation constant of the effective transmission line circuit.

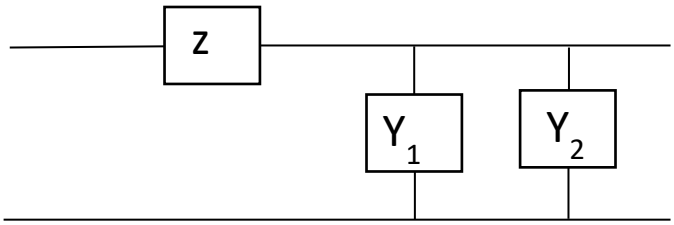

Figure 22 Impedance and Admittance model

$Z = R_u + j\omega L_u$

$Y_1 = G_u + j\omega C_u$

$Y_2 = \frac{1}{R_P + \frac{1}{j\omega \Delta C}} = G_l + j\omega C_l$

$where\ G_l = \frac{(\omega \Delta C)^2 R_P}{1 + (R_p \omega \Delta C)^2}$

$C_l = \frac{\Delta C}{1 + (R_p \omega \Delta C)^2}$

$\alpha + j\beta = \sqrt{ZY_0}$

$Y_0 = Y_1 + Y_2$

$G = G_l + G_u$

$C = C_l + C_u$

$\alpha + j\beta = j\omega\sqrt{L_u C}\sqrt{1 - j\left(\frac{R_u}{\omega L_u} + \frac{G}{\omega C}\right) - \left(\frac{R_u G}{\omega^2 L_u C}\right)}$

Let's assume

$R_u = R_p = 0.3\ \Omega/\text{cm}$

$f = 40\ GHz$

$L_u = 5.3\ nH/cm$

$C_u = 0.4\ pF/cm$

$\Delta C = 2\ pF/cm$

$\frac{R_u G}{\omega^2 L_u C}$<<1, so

$$\alpha + j\beta \approx j\omega\sqrt{L_u C}\sqrt{1 - j\left(\frac{R_u}{\omega L_u} + \frac{G}{\omega C}\right)}$$

$$\alpha = \frac{1}{2}\left(\frac{R_u}{Z_0}\right) + \frac{1}{2}(GZ_0)$$

Let's define

$\alpha_c = \frac{1}{2}\left(\frac{R_u}{Z_0}\right)$ as loss due to the conductor

$$\alpha_{diode} = \frac{1}{2}(GZ_0)$$

$$= \frac{Z_0}{2}\left(G_u + \frac{(\omega\Delta C)^2 R_P}{1+(R_p\omega\Delta C)^2}\right)$$

where $Z_0 = \sqrt{\frac{R_u + j\omega L_u}{G + j\omega C}} \approx \sqrt{\frac{L_u}{C}}$

Loss in the capacitively loaded transmission line depends on the square of loaded device capacitance (ΔC), frequency and has a linear dependence with the resistance of the semiconductor doped layers. When the arms of the interferometer are connected in parallel, total capacitance loaded will be doubled and resistance would be halved and when connected in series, capacitance would be halved, and resistance would be doubled.

3.2. Transmission line losses

The two main sources of loss in a transmission line arises due to the dielectric loss and the skin effect loss. The electric field polarizes the atoms of the material to induce electric dipole moments and as frequency increases, these dipole moments cannot react instantaneously to the applied electric field. This damping of vibrating dipole moments results in loss on the medium in the form of heat and is represented by the imaginary part of the dielectric constant. [6]. Loss tangent and the dielectric constant is given by

$$tan\delta = \frac{\omega\epsilon'' + \sigma}{\omega\epsilon'}$$

$$\epsilon = \epsilon'(1 - jtan\delta)$$

Overall dielectric loss comes both from the damping and the finite conductivity of the material. In case of semiconductors such as GaAs which are available in semi-insulating quality, resistivity of the substrate could be very high resulting in damping loss, only major contributor to the overall loss. In case of silicon substrates which has a finite conductivity, conductor loss could be the major contributor and with a coplanar waveguide design on a finite conductivity substrate, there could be spurious RF modes propagating through the silicon substrate. With low resistivity, silicon substrate could support slow wave modes at certain frequency ranges resulting in significant reduction in microwave phase velocity. Recently, high resistivity silicon wafer (~ 6 KΩ.cm) are available in the market, still much lower than the semi-insulating GaAs(>10^4 KΩ.cm).

Next main loss is the skin effect loss which arises due to the current being forced to flow near the edges of the conductor as the frequency increases. Effective resistance increases thereby increasing the loss of the transmission line.

3.3. Coplanar electrode design

Coplanar electrodes were simulated using Ansys HFSS to extract the propagation loss, epsilon and the characteristic impedance of the transmission line. Silicon substrate along with the GaP buffer layers were purchased from an outside vendor. From the manufacturer's spec sheet, substrate is mentioned to be p doped and the resistivity is about 8-12 ohm.cm. For simulations, value of 10 ohm.cm was used corresponding to a conductivity of 10 Siemens/m. Previous users in the lab had their coplanar mask layers fabricated for their process and was used to fabricate the coplanar lines on silicon substrate. Dimensions of the electrode which

was simulated is shown in Figure 23. BCB planarization was decided to be used as part of high-speed device and so simulations were carried out by varying its thickness. Loss tangent of BCB from manufacturer's spec sheet is 0.002 @ 20 GHz. However, in a publication [7], extracted loss tangent of BCB seems to increase as the frequency increases and so a worst case value of 0.009 was assumed for all the frequencies of interest. Signal and ground lines were 30 µm and 170 µm wide and were separated by 35 µm. Thickness of the metal lines were 1.5 µm. Thickness of the BCB was varied to simulate the effect of field lines penetration into the silicon substrate and results are shown in Figure 24 and Figure 25.

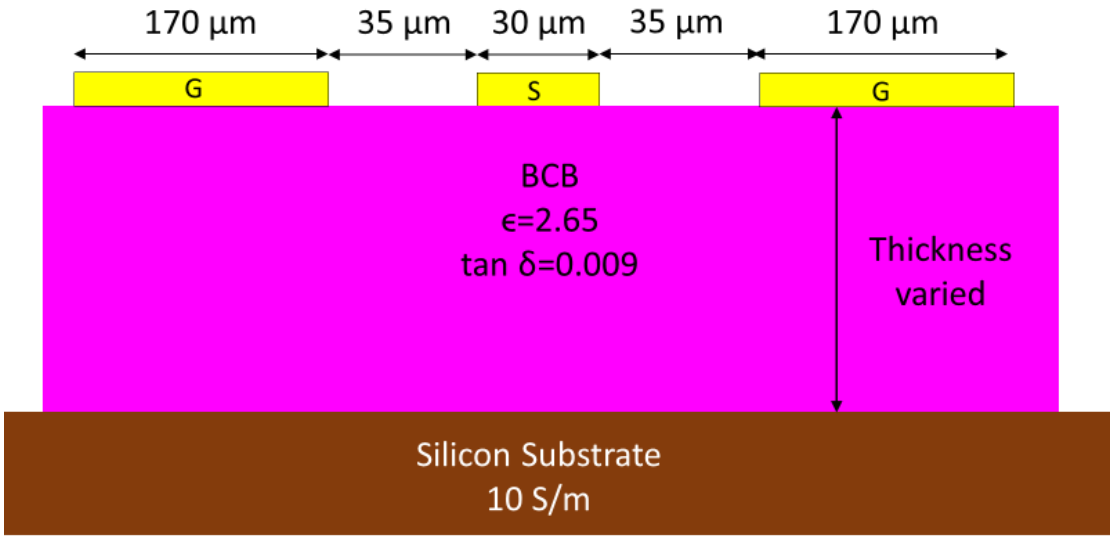

Figure 23 Coplanar electrode used for simulations

Simulations were carried out at a constant frequency of 67 GHz since that's the maximum frequency that could be tested in our lab. Epsilon of BCB was used as 2.65 from manufacturer's data sheet and epsilon of silicon was set to be 11.9. As thickness increases, electric field lines penetration into substrate decreases with more overlap with BCB layers resulting in decrease of epsilon from 5.4 with no BCB to 2.75 @ 15 µm thickness. Propagation loss decreases from 24 dB/cm to approximately 7.7 dB/cm at 15 µm BCB. Even at 15 µm

thickness, there is a slight penetration of the field lines into the silicon substrate as evident from higher loss and epsilon values (2.75 > 2.65).

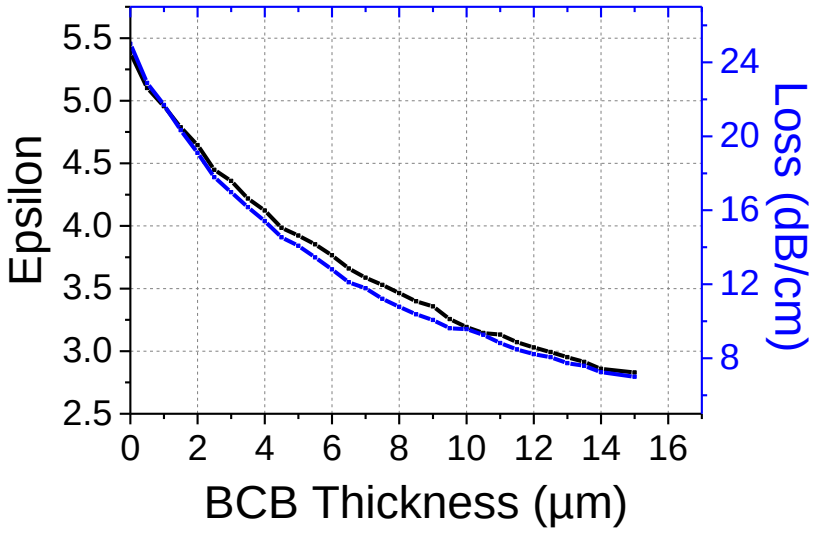

Figure 24 HFSS Simulation of Coplanar lines on silicon substrates for varying BCB thickness

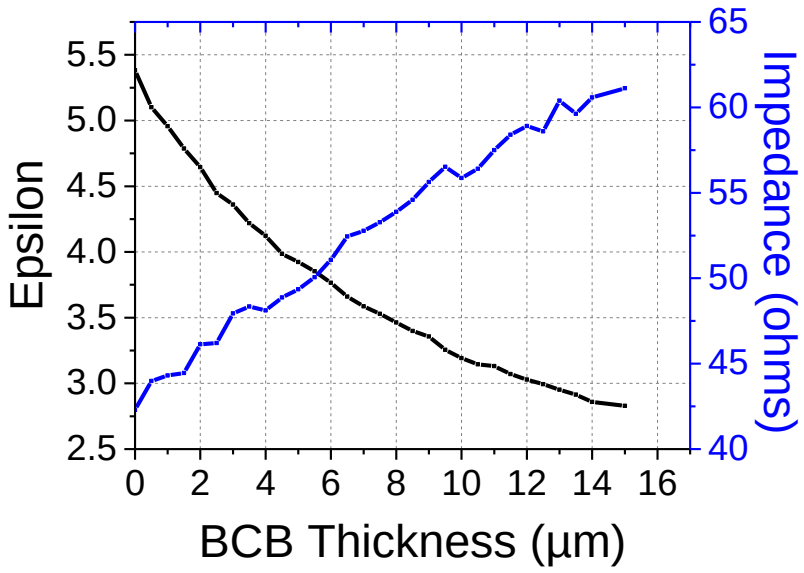

Figure 25 Epsilon and Impedance of coplanar lines on silicon substrate for varying BCB thickness

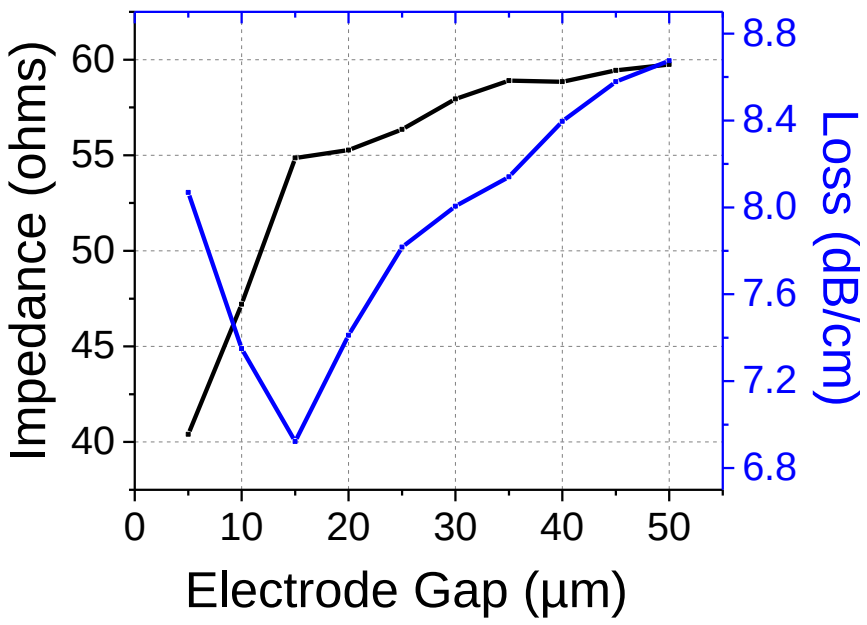

Figure 26 Coplanar line impedance and loss as the electrode gap is varied, BCB thickness= 12 µm

As BCB thickness increases, line impedance increases because of the decrease in the capacitance of the transmission line attributing to increase in overlap of field lines with BCB as shown in Figure 25. Overlap of the field lines with the silicon substrate could be decreased by reducing the gap between the coplanar electrodes at the expense of reduced impedance. Simulations were performed for varying electrode gap at a constant BCB thickness of 12 µm and results are shown above in Figure 26. As the electrode gap is decreased, minimum loss of 7 dB/cm @ 67 GHz could be achieved at a gap of 15 µm. But as the gap further decreases, loss due to increased charge accumulation between the electrodes dominates the loss of silicon substrate and hence the loss continues to increase. When the modulators are integrated with these transmission lines, impedance of overall line will be reduced based on the capacitive loading of the modulator active section. Even though reducing the electrode gap appears to be

a viable option to reduce the loss, it will be challenging to achieve an overall 50 Ω line and velocity matching simultaneously with this approach.

Even though coplanar electrodes are easy to fabricate, integrating with electro-optic modulators of several millimeters' length will severely degrade the electrical performance of the device at high frequencies. High resistivity silicon substrates are available in market but are yet to be made compatible for III-V material growth on that. In the present-day silicon modulators on high resistivity substrates, 2 μm or thicker bottom oxide helps to reduce the overlap of field lines with the substrate, but this approach is not possible for III-V epitaxial growth on silicon. One cannot grow a low epsilon III-V material epitaxially on silicon except for oxidized AlGaAs layers, but this approach is yet to be fine-tuned. Without a low epsilon material, amount of capacitance that could be loaded from modulator sections could be reduced thereby increasing the drive voltage of the modulator. Bonding III-V to SOI wafer could help to partially alleviate the problem, but it counteracts the whole goal of easy-integration of III-V on silicon and using the bigger silicon substrates for epitaxial growth. In conclusion, modified transmission lines must be used to improve the electrical performance of III-V electro-optic modulators on silicon substrates.

3.4. Microstrip electrode design

As discussed in the previous section, in case of coplanar electrodes on silicon, RF propagation loss would be unsuitable for III-V electro-optic modulators. Transmission line design must be modified to prevent the field lines interact with the silicon substrate. We decided to use microstrip transmission line design for the high-speed modulator. Unlike the coplanar electrode, in a microstrip line, signal electrode is at a certain gap above the ground electrode and hence would provide a better isolation to the field lines. Choice of the microstrip

dielectric is crucial for low RF loss and hence BCB with its low loss tangent [7] and planarizing capabilities was chosen as the dielectric material. Simultaneous achievement of an impedance of 50 ohms and a velocity match between the optical and microwave signal is possible if the device is designed based on the following equations [5].

$$\Delta C = \frac{n_{wg}^2 - n_u^2}{cZ_0 n_{wg}}$$

$$L_u = \frac{n_{wg} Z_0}{c}$$

$$C_u = \frac{n_{wg}}{cZ_0} - \Delta C$$

where n_{wg} and n_u are optical group velocity and microwave phase velocity, Z_o is overall line impedance, C_u and ΔC are unloaded and loaded capacitance, L_u is the unloaded line inductance and c is the velocity of light. Epilayer will be periodically isolated electrically along the waveguide direction forcing the microwave current to primarily flow along the unloaded transmission line and hence the overall line inductance changes marginally from the unloaded line inductance. Using a group index of 3.488 and microwave index of 1.398 (BCB dielectric), L_u, C_u and ΔC required for a 50 ohms line and velocity matching are 5.81 nH/cm, 0.374 pF/cm and 1.95 pF/cm respectively.

3.4.1. Microstrip Simulations

Microstrip structure simulated in HFSS is shown in Figure 27. Thickness of signal and ground electrodes were chosen to be 1.5 μm with gold as the metal. Signal and ground electrode widths were chosen to be 5 μm and 70 μm and thickness of the BCB was varied to calculate the transmission line parameters at a constant frequency of 67 GHz. Top material was chosen to be air. Impedance and loss values as BCB thickness is varied is shown

in Figure 28 and inductance and capacitance of the line is shown in Figure 29. Inductance and the capacitance values are extracted from the impedance and epsilon results obtained from the simulation.

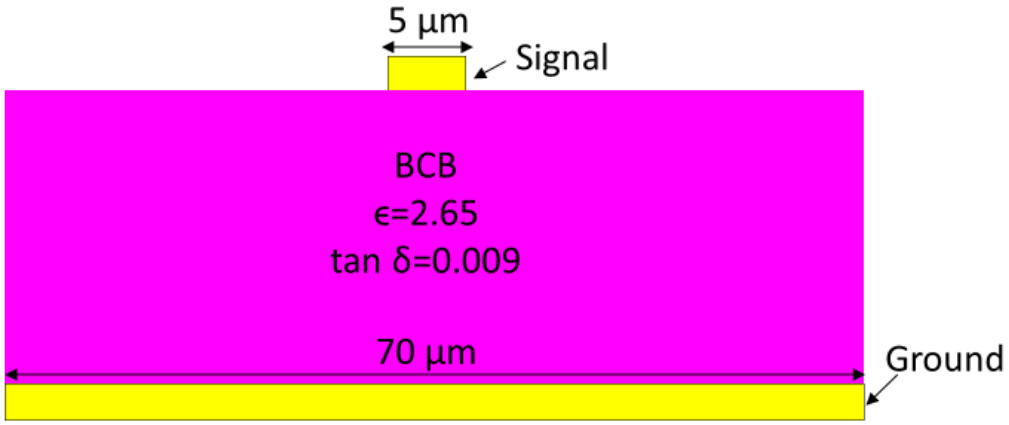

Figure 27 Simulated Microstrip Transmission Line

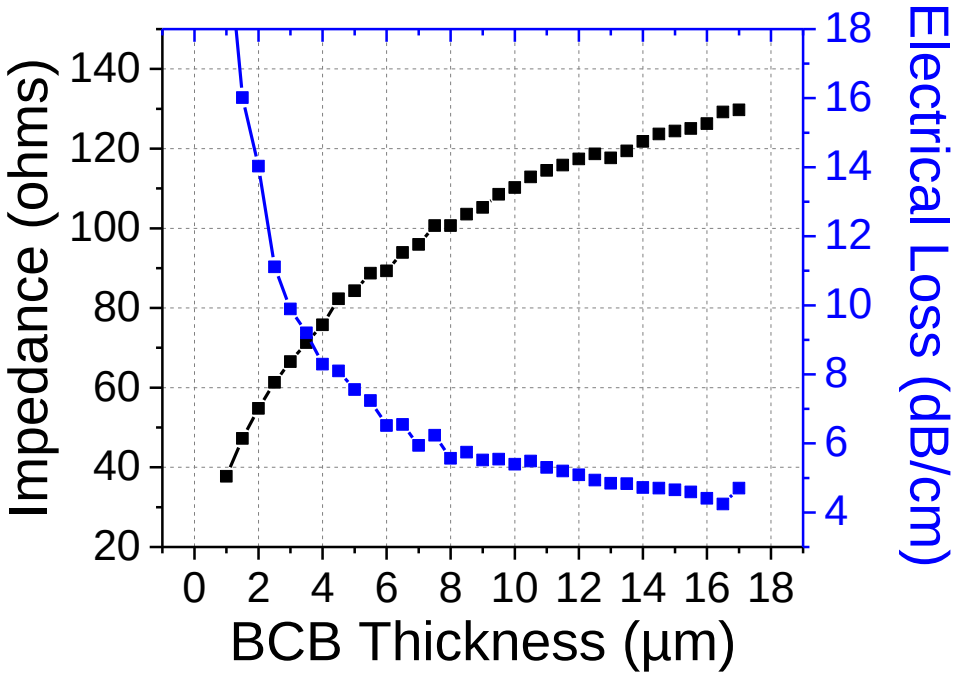

Figure 28 HFSS Simulation of Microstrip Line @ 67 GHz, Signal width= 5µm

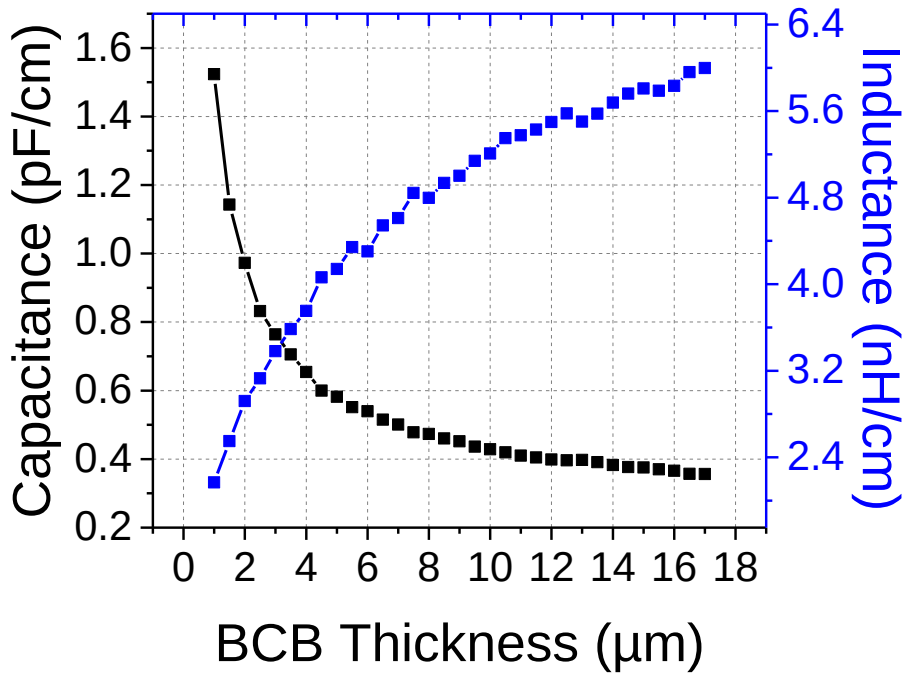

Figure 29 HFSS Simulation- Transmission line Parameters @ 67 GHz, Signal width= 5µm

Required values of inductance and capacitance could be achieved for BCB thickness greater than 14 µm as shown in Figure 29. In case of a microstrip, loss and the inductance of the line are predominantly determined by the width of the signal line since the ground electrodes are much wider than the signal electrode. Electrode gap in a coplanar and BCB thickness in a microstrip share the same purpose in terms of properties of the transmission line. Loss of the transmission significantly decreases as the thickness of the BCB increases as shown in Figure 28. Increased loss at thinner BCB is due to charge accumulation at electrodes due to high electric field. Impedance of the lines are also suitably high so that enough capacitive loading could be included to achieve an overall 50 ohms line. Width of the line was kept at 5 µm as increased width reduced the inductance of line.

3.5. Microstrip Fabrication

Before integrating the microstrip line with the modulator, unloaded line was fabricated to check its loss and fabrication compatibility. Initially, photo BCB was planned to be used as the dielectric. It's a negative photo resist which could be exposed using stepper to create patterns. It could also be exposed multiple times to get a thicker BCB with a very smooth sidewall profile as shown in Figure 30. With a smooth profile, it could be easier to run metal along the sidewall.

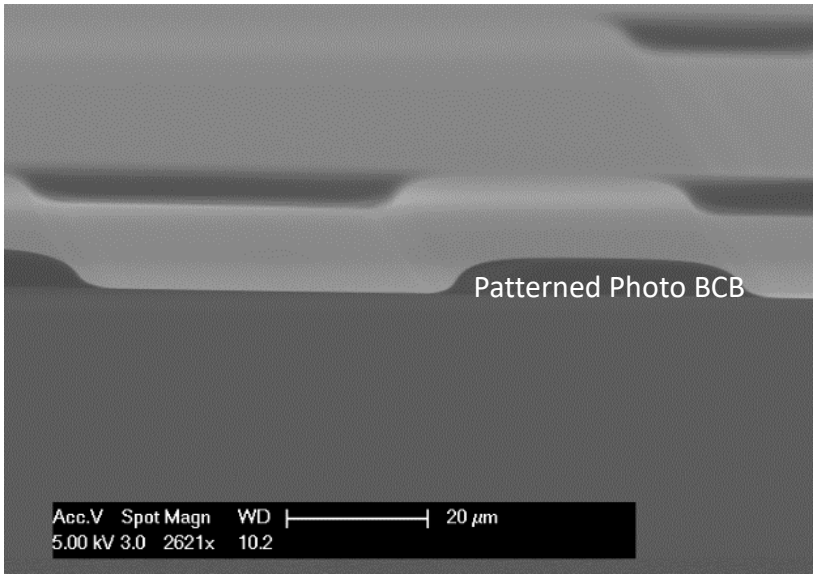

Figure 30 Patterned Photo BCB on silicon substrate

Photo BCB in our lab had expired two years back and from previous user's experience, expired BCB had higher loss tangent. Also, photo BCB doesn't planarize like regular BCB and could be challenging to integrate with the modulator and instead regular BCB was decided to be used for the fabrication. Since the RF probes must land on a planar surface, contact to the bottom ground electrode must be brought up along with the signal line. Etching vias in BCB which are greater than 10 μm thick and lifting off metal contacts will be extremely challenging and so it was decided to plate the metal posts to bring the contacts from ground

line to top of BCB. It's possible to selectively plate gold by patterning using photo resist and connecting the sample to plating electrodes. There must be a continuous metal layer on the sample so that plating electrodes could make a contact to the sample near its edge. It's usually called as a seed layer and is very thin. Once the patterns are plated, photo resist is stripped off and seed layer is removed using wet etching with plated electrode as a mask. Usually the seed layer is gold owing to its low resistance. From previous experience of clean room users, negative photoresist didn't adhere with the plating solution and so a positive resist (AZP 4620) was used for plating. It has an excellent adhesion directly on gold which is challenging even among other positive resists. Multiple coatings leading to a thicker resist is possible without any cracking. I was able to test as thick as 35 μm without any cracking. A soft bake of 80 C for 1 minute is required in between successive spinning of the photo resist.

Entire fabrication process is shown in Figure 31. Fabrication was started with depositing a thin oxide layer on silicon substrate using PECVD followed by electron beam evaporation of Cr/Au, each 25 nm thickness as seed layer. Using AZP 4620, patterns were developed to plate the gold electrodes. Before plating, edge of the sample was cleaned using acetone with cotton swab to open contact areas for plating electrodes. Sample was plated for 30 minutes resulting in a gold thickness of 2 μm. Photoresist was stripped off using acetone. For metal post, two coats of AZP 4620 was spun and plated for 2 hours resulting in a gold thickness of 19 μm. Plated thickness was slightly higher than the resist thickness leading to sideway plating. There was a slight widening of patterns and was not a major concern. After stripping of the resist, seed layer was etched using gold etchant for 5 seconds. Etch stops on chrome and was followed by chrome etchant for 5 seconds leading to complete removal of seed layer. In the process, 400 nm of plated ground electrode was etched. Gold etchant has a

very fast etch rate and care must be taken while etching the patterns. Both gold and chrome etchants doesn't attack silicon dioxide.

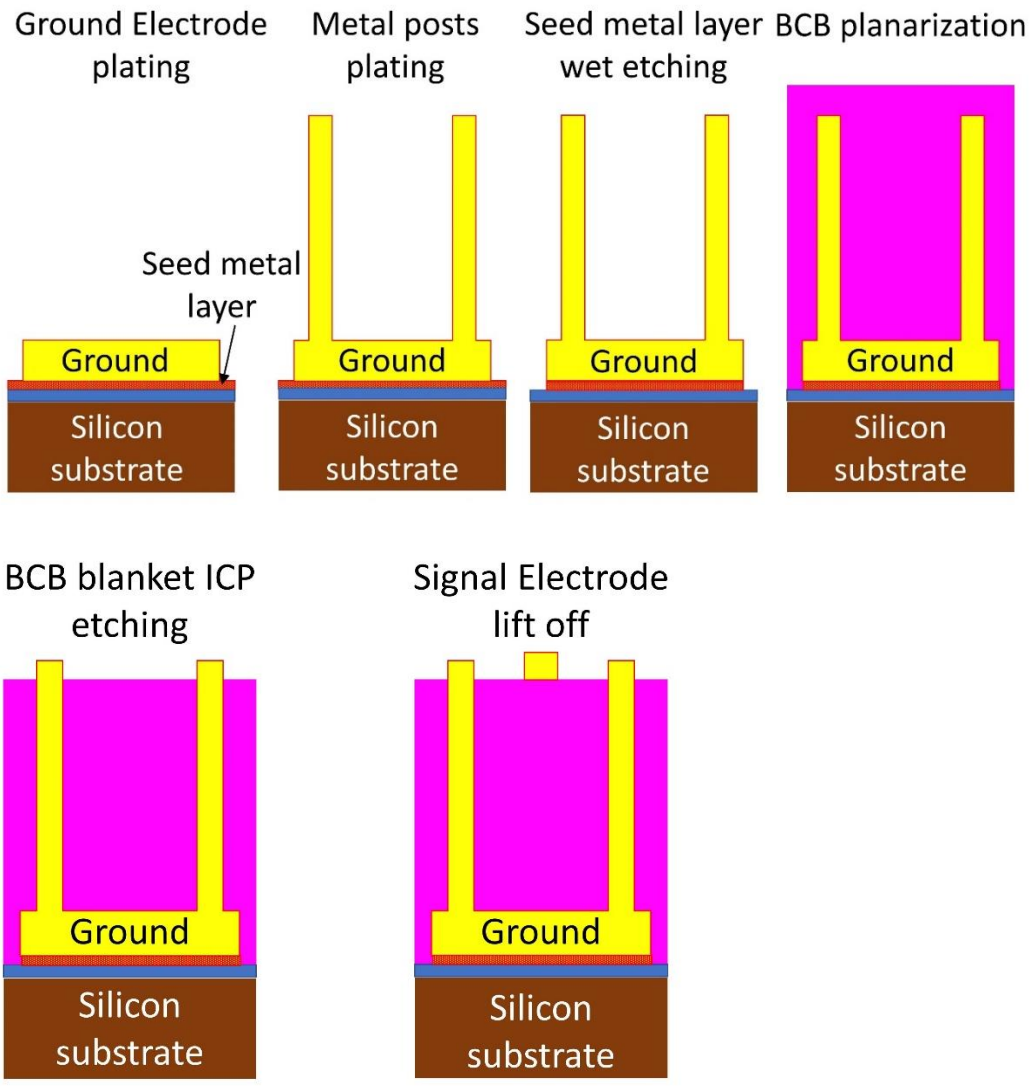

Figure 31 Microstrip Line Fabrication Process

After the seed layer removal, 150 nm silicon nitride was deposited at 300 C. Silicon dioxide doesn't adhere well on to gold and so it's must to have silicon nitride before spinning BCB. Moreover, BCB has good adhesion with silicon nitride. Three schedules of BCB planarization was carried out. First two schedules were soft cured at 210 C and third schedule was hard cured at 250 C. BCB was blanket etched in ICP until the contacts were reached.

Final BCB thickness was between 9 to 10 μm. BCB wasn't completely planar after the hard cure. BCB was thicker on top of plated gold and thinner elsewhere. Blanket etching of BCB resulted in non-uniform final BCB thickness. One more schedule of BCB curing would have made the sample planar. SEM of cleaved section of microstrip line is shown in Figure 32 and thick metal posts are shown in Figure 33.

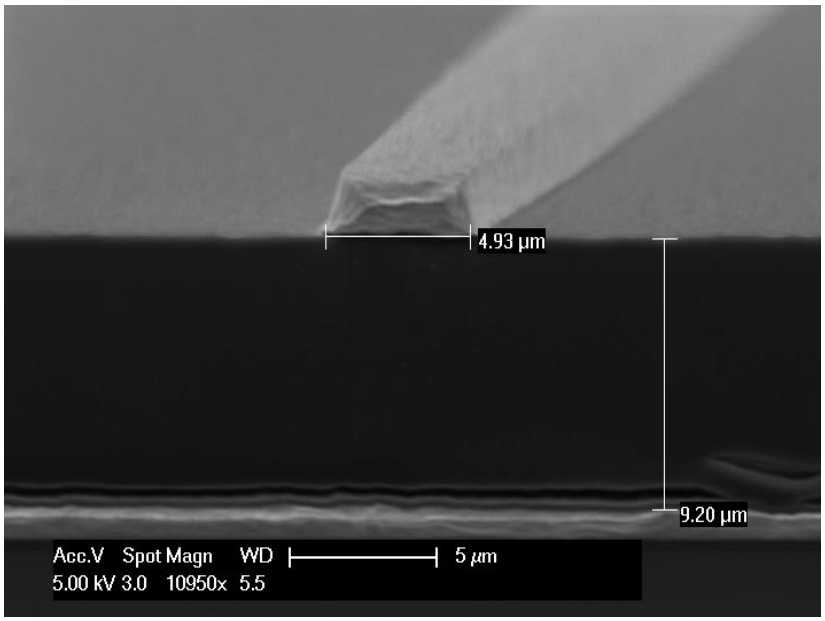

Figure 32 SEM-microstrip line

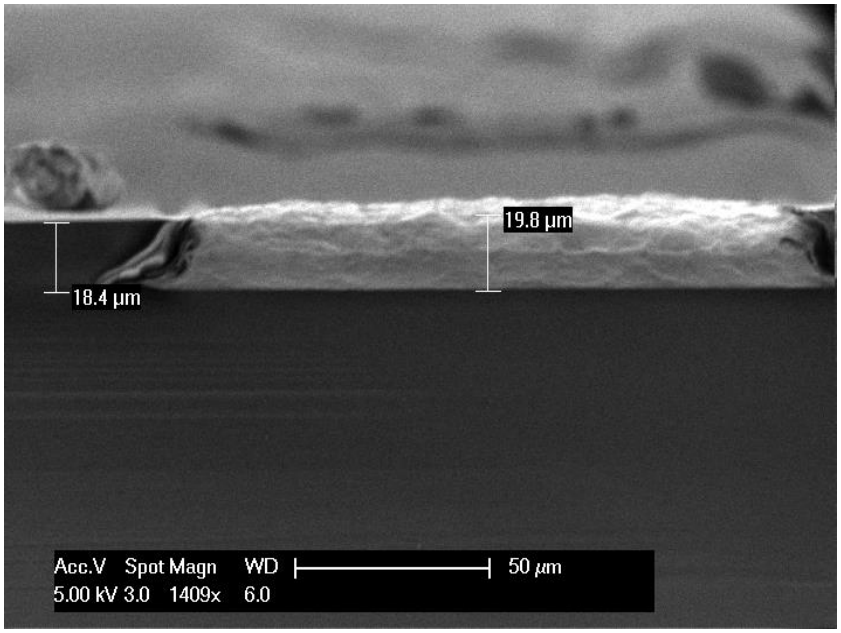

Figure 33 SEM-plated metal posts

3.6. Probe Pads

As said before, to prevent damage to RF probes, they must land on a flat smooth surface. Near the probing section, grounded coplanar electrode with GSG configuration was used as shown in Figure 34.

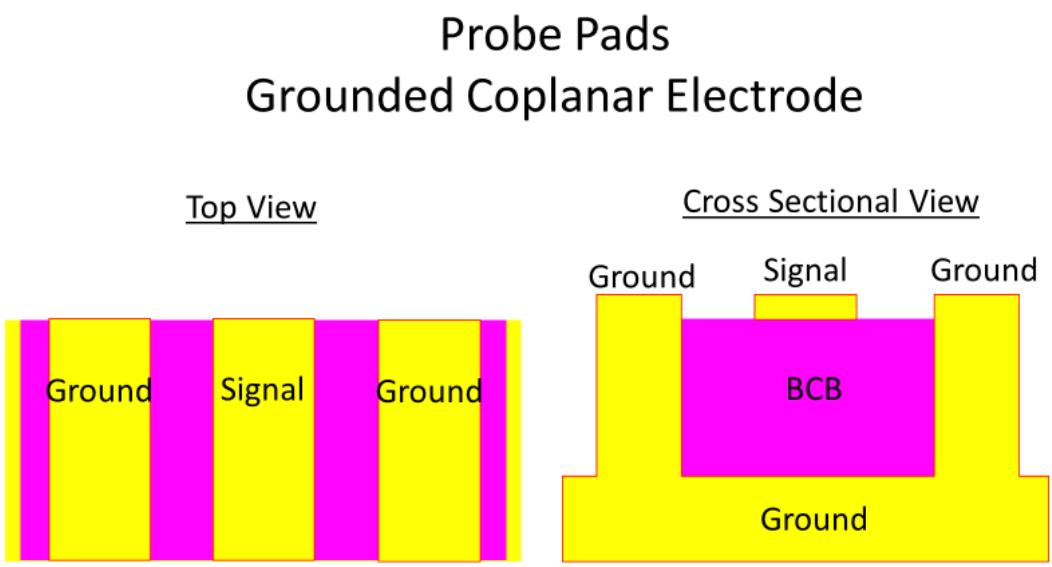

Figure 34 Grounded Coplanar-Top and Cross-Sectional view

Both the ground electrodes are shorted unlike the usual coplanar electrodes where the ground electrodes are floating. However, there could be additional capacitance due to the electrode gap horizontally between the signal and ground lines. A transition from grounded coplanar to microstrip electrode is designed as show in Figure 35. Gap between the electrodes is much higher than BCB thickness and so the impedance changes negligibly across the transition. Microscope picture of the probe pads is shown in Figure 36. Pads are bended so that they are not in the way of fiber used for coupling light and hence could be visible under microscope. Ground electrodes were 470 μm wide in probing section and 80 μm wide in the microstrip section

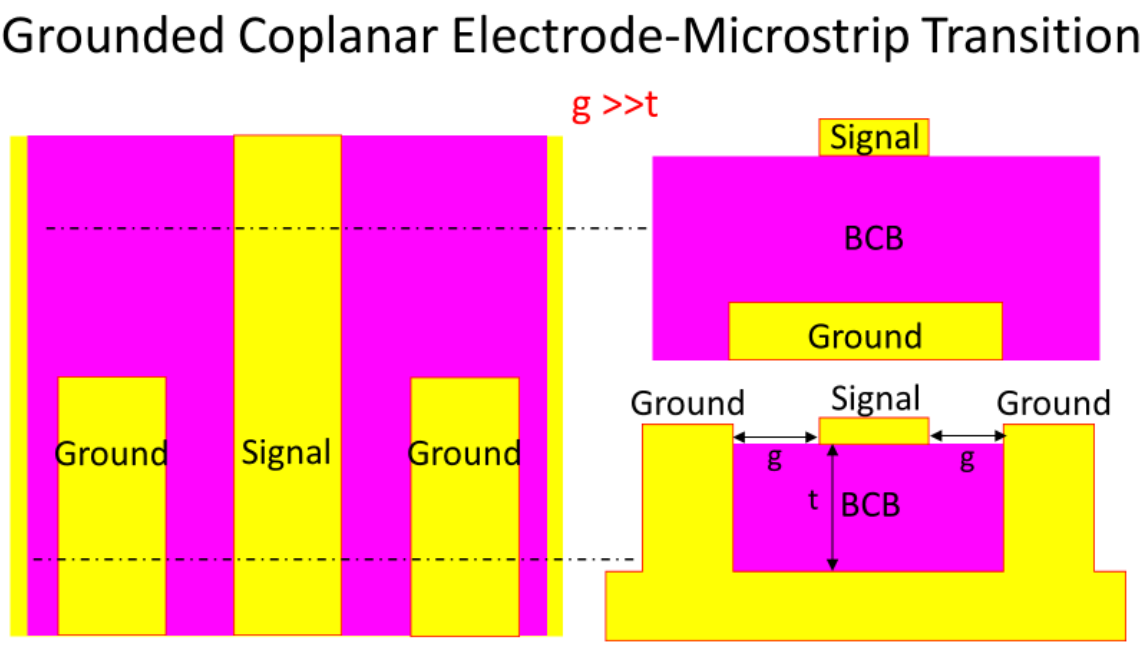

Figure 35 Grounded coplanar- Microstrip transition in Probe Pads

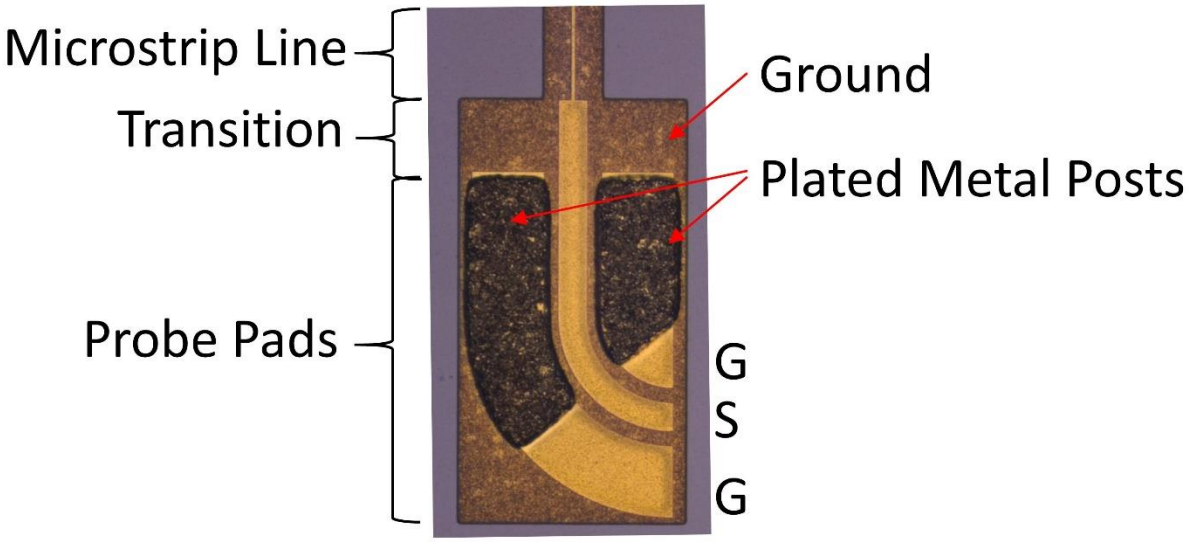

Figure 36 Microscope picture of probe pads

3.7. Results

Two sets of transmission lines were fabricated. One with a microstrip design and next with a coplanar design. For coplanar electrode, a small piece of III-V epi layer grown on silicon was used. Sample was flipped down, and electrodes were fabricated on the polished back side. As mentioned in the simulation section, sample was planarized with 12 μm BCB before lifting off the electrodes and dimensions were same as the one mentioned in simulations. Small signal measurements were carried out using Agilent E8361 PNA. 67 GHz GSG probe from GGB Industries was used for the measurements. Probes were calibrated using on chip TRL patterns. For Line measurements, four different lengths covering frequencies between 2-150 GHz were used with overlap between frequencies in each measurement. Agilent software automatically computes the calibrated line's parameters. Measured loss and epsilon values are shown in Figure 37.

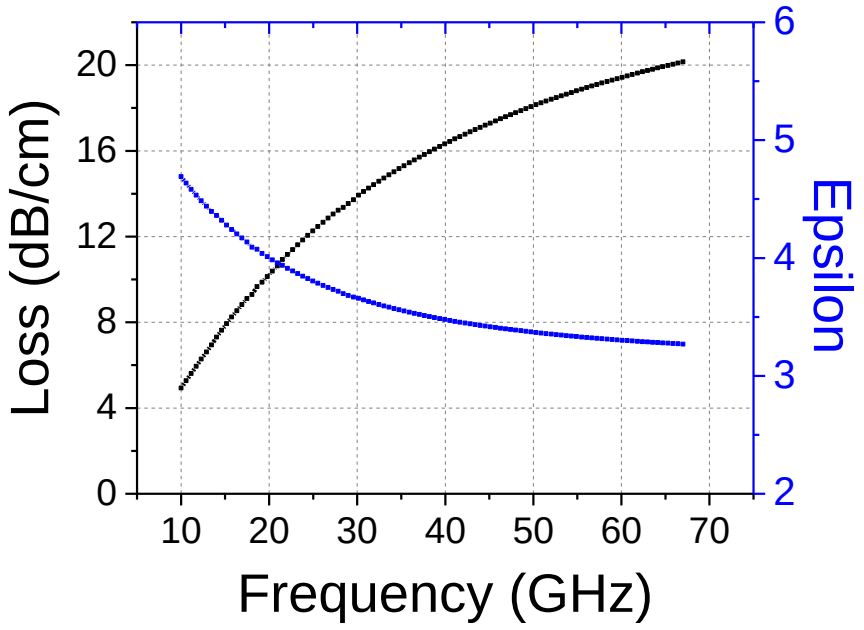

Figure 37 Coplanar Electrode Measurements on Silicon Substrates

It appears that loss of the coplanar line is significantly higher than expected. From simulations, loss is expected to be around 8 dB/cm @ 67 GHz while the measured loss value is around 20 dB/cm @ 67 GHz. Finite conductivity silicon substrates have different modes of propagation such has quasi-dielectric TEM mode, skin-effect mode and slow wave mode based on the conductivity and the frequency of the operation [8]. As the frequency change, transition occurs between the modes with slow wave behavior dominating the low frequency range and quasi TEM dominating the high frequency region. Skin effect mode dominates the intermediate frequency region and loss depends on the field penetration in the silicon. At high frequencies, epsilon approaches an approximate value of weighted average of BCB and silicon (~3.5) indicating the quasi TEM propagation. In Figure 37, only the skin effect and quasi TEM mode of propagation dominates. These effects also result in dispersive transmission line which is not suitable for achieving velocity matching in a traveling wave design.

Similar measurements were carried out on the microstrip electrode design. Epsilon and impedance measurements are shown in Figure 38 and loss measurements are shown in Figure 39. Impedance was calculated from the capacitance and epsilon value measured. Probe pads capacitance was measured to be 0.44 pF and 5 μm line capacitance was measured to be 0.603 pF/cm. Loss value at 67 GHz was around 7 dB/cm as opposed to 20 dB/cm for coplanar electrodes on silicon. From the plot shown in Figure 29, simulated capacitance for 9 μm BCB thickness is around 0.45 pF/cm, while the measured value is 0.6 pF/cm. BCB thickness variation alone can't be responsible for higher capacitance. Dielectric constant of 2.65 as quoted in manufacturer's data sheet was used in the simulation. It appears that the actual dielectric constant could be greater than 3 in order to have such a high capacitance. Higher dielectric constant could be a result of multiple BCB soft cures and this needs to be further

investigated. Higher capacitance also explains the higher loss as a result of reduced line impedance.

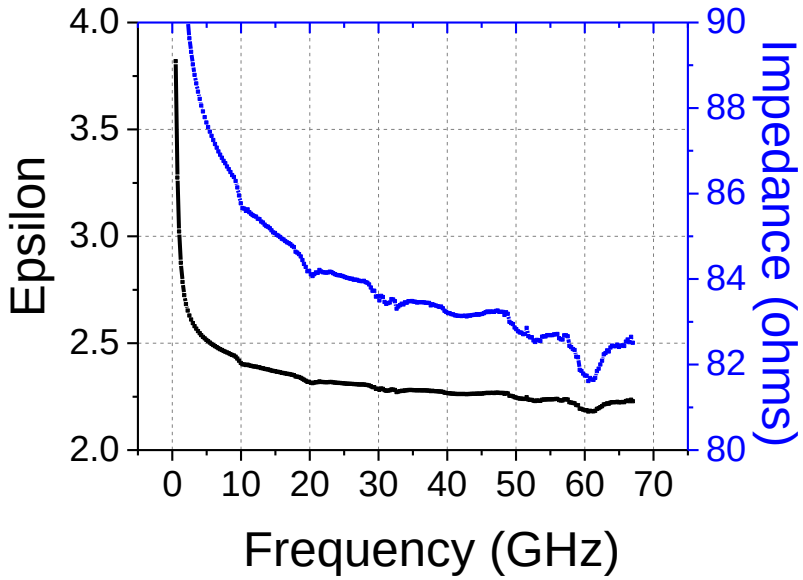

Figure 38 Microstrip electrode epsilon and Impedance measurements

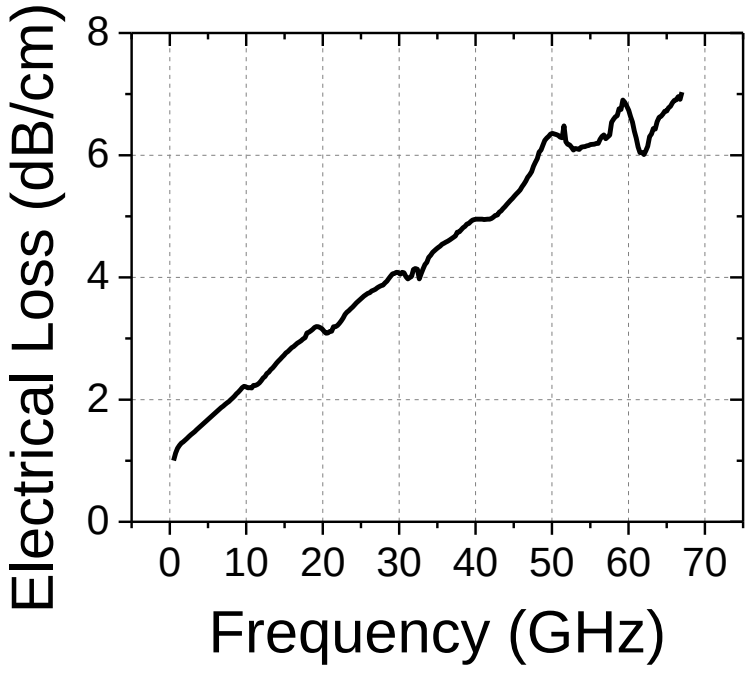

Figure 39 Microstrip electrode loss measurements

3.8. Summary

In this chapter, on chip microstrip electrodes for III-V electro optic modulators was designed and fabricated. Loss of microstrip electrodes was around 7 dB/cm @ 67 GHz, significant improvement over the coplanar electrodes (20 dB/cm @ 67 GHz) on silicon substrates. With slightly increasing the BCB thickness, it's possible to improve the loss of microstrip electrode to less than 5.5 dB/cm @ 67 GHz, approaching closer in number to coplanar electrodes on semi insulating GaAs substrates with similar impedance. These types of electrodes could also be integrated on SOI based modulators without needing to thin down the high resistive silicon substrate for improving the loss or other doped substrates such as InP, GaAs and lithium niobate.

3.9. References

1. Li, X., et al., *Single-drive high-speed lumped depletion-type modulators toward 10 fJ/bit energy consumption.* Photonics Research, 2017. **5**(2): p. 134-142.
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4 High Speed GaAs/AlGaAs MZM on Silicon substrate

4.1 Introduction

As discussed in previous chapter, use of coplanar electrodes on silicon substrates will result in high electrical loss combined with a dispersive transmission line. Since these devices are several millimeters long, velocity matching would be an issue as a result of dispersion. A modified microstrip based electrodes was proposed and loss of those lines was around 7 dB/cm @ 67 GHz. With slightly increasing the BCB thickness, that number could approach around 5 dB/cm. In this chapter, integration of microstrip line with NPIN modulator design is discussed. Chapter begins with design, fabrication details of the high speed NPIN MZM followed by the results. In the second half of the chapter, modified modulator design to improve the electrical bandwidth is discussed and the preliminary results on the optical loss and drive voltage are presented.

4.2 NPIN High Speed Design

Epitaxial layer design for reference is again shown in Figure 40. At high frequencies, displacement current flows through the doped semiconductor layers. Assuming velocity is matched between electrical and the optical signal, modulator bandwidth is limited by the loss associated with the resistance of the doped semiconductor layers and the capacitance that is loaded. Since the skin depth of the doped semiconductor layers are very high, in low frequency region, it could be assumed to have the microwave current flow uniformly throughout the doped semiconductor layers. Mobility of N $Al_{0.9}GaAs$ with a doping of $2.3*10^{18}$ cm^{-3} was measured experimentally by the MBE growers to be around 80. In the design shown in

Figure 40, doping is $1*10^{17}$ cm^{-3} for N $Al_{0.9}GaAs$ layers and mobility increases with decreased doping. For simulation,

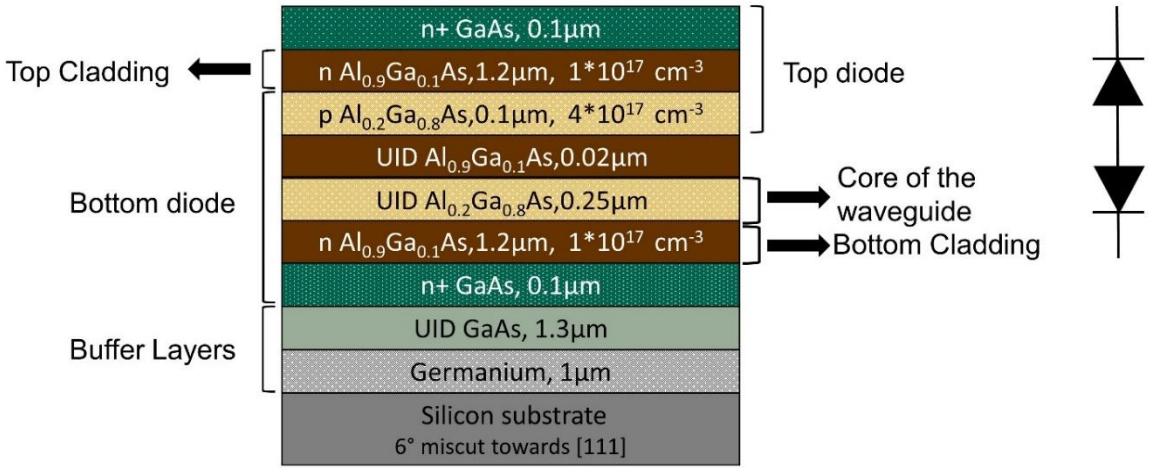


Figure 40 Epitaxial Layer Stack

a worst-case value of 80 was assumed since mobility at lower doping wasn't measured. Mobility of N GaAs at $7*10^{18}$ cm^{-3} was measured to be 2500 and was used for calculating the resistance. For high speed design, rib waveguide width was chosen to be 1.5 µm and etch depth was increased to 1.4 µm. Increase in etch depth is to etch the P $Al_{0.2}GaAs$ layer to reduce the capacitance. Cross section of the active modulator waveguide without the metal contacts is shown in Figure 41.

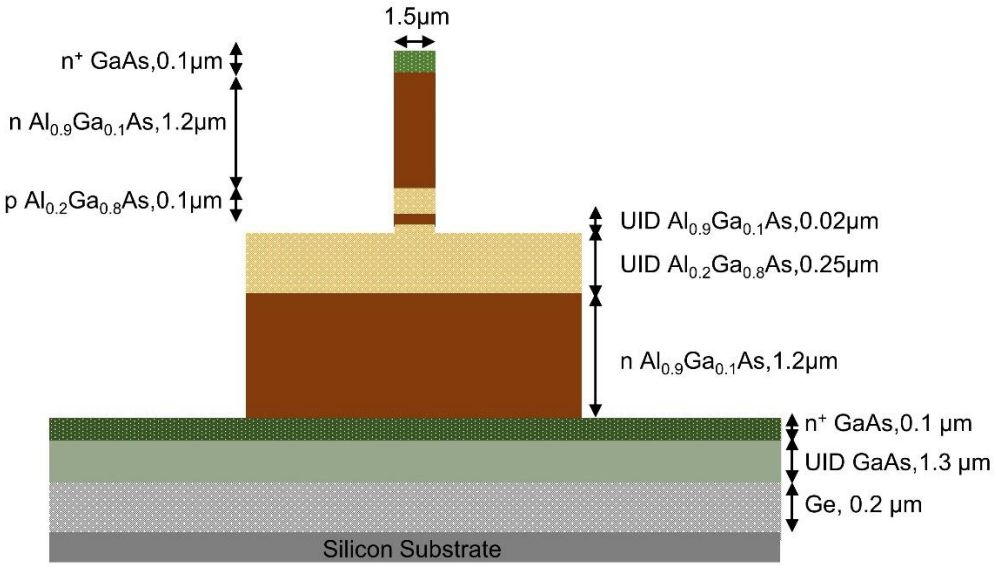


Figure 41 Cross section High Speed Modulator Waveguide

Microwave current will only flow vertically across the rib waveguide if the diode is electrically isolated along the waveguide propagation direction. In both the top and bottom N $Al_{0.9}GaAs$ layers, thickness of the layers for calculating the resistance was 1 μm assuming a depletion width of 0.2 μm. For the bottom N GaAs, microwave current will flow 4 μm laterally. Calculated resistances are shown below. R_{n1} and R_{n2} denotes N $Al_{0.9}GaAs$ resistance in top NP and bottom PIN diode respectively. R_p denotes the resistance of P $Al_{0.2}GaAs$ layer and R_{GaAs} denotes the resistance of bottom N GaAs layer. Resistances associated with other layers are negligible. With this design, intrinsic device bandwidth is around 78 GHz. So, for frequency even at 40 GHz, almost 90 % of applied AC signal will drop across the modulator diode. Reverse leakage current even at high optical input powers didn't exceed 5 μA at bias of -10 V. So electrical loss associated due to the leaky conductance path is also negligible.

$$R_{n1} = \frac{1\ \mu m}{1.5\ \mu m * 1\ cm * 1.6 * 10^{-19} * 1 * 10^{17} * 80\ \frac{cm^2}{v.s}} = 0.5208\ \Omega\ (\text{N } Al_{0.9}GaAs \text{ resistance})$$

$$R_{p} = \frac{0.05\ \mu m}{1.5\ \mu m * 1\ cm * 1.6 * 10^{-19} * 4 * 10^{17} * 300\ \frac{cm^2}{v.s}} = 1.736 * 10^{-3}\ \Omega\ (\text{P } Al_{0.2}GaAs \text{ resistance})$$

$$R_{n2} = \frac{1\ \mu m}{8\ \mu m * 1\ cm * 1.6 * 10^{-19} * 10^{17} * 80\ \frac{cm^2}{v.s}} = 0.097\ \Omega\ (\text{bottom N } Al_{0.9}GaAs \text{ resistance})$$

$$R_{GaAs} = \frac{4\ \mu m}{0.1\ \mu m * 1\ cm * 1.6 * 10^{-19} * 10^{18} * 2500\ \frac{cm^2}{v.s}} = 0.1\ \Omega\ (\text{bottom N GaAs resistance})$$

$$R_{eq} = 0.7178\Omega$$

C_{eq}=2.82 pF (1.5 μm width)

$$f_c = \frac{1}{2\pi R_{eq} C_{eq}} = 78.71\ \text{GHz}$$

$$V_{diode} = V_{in} * \frac{X_C}{\sqrt{R^2 + X_C^2}}$$

At f=40 GHz, Vin=1 V

$V_{diode} = 0.89\ V_{in}$

Before fabricating the actual modulator, unloaded microstrip transmission line was fabricated and tested on a silicon substrate with a slightly thicker BCB value of 12 μm. Signal and ground widths were kept at 5 and 70 μm respectively. Four different lengths of 535 μm, 1535 μm, 4419 μm and 10606 μm was used for calibration and measured capacitance vs length is shown in Figure 42. Slope of line is 0.57 pF which is the capacitance per unit length and the intercept gives the pad capacitance which is 0.44 pF. Measurements were carried out at 1 MHz.

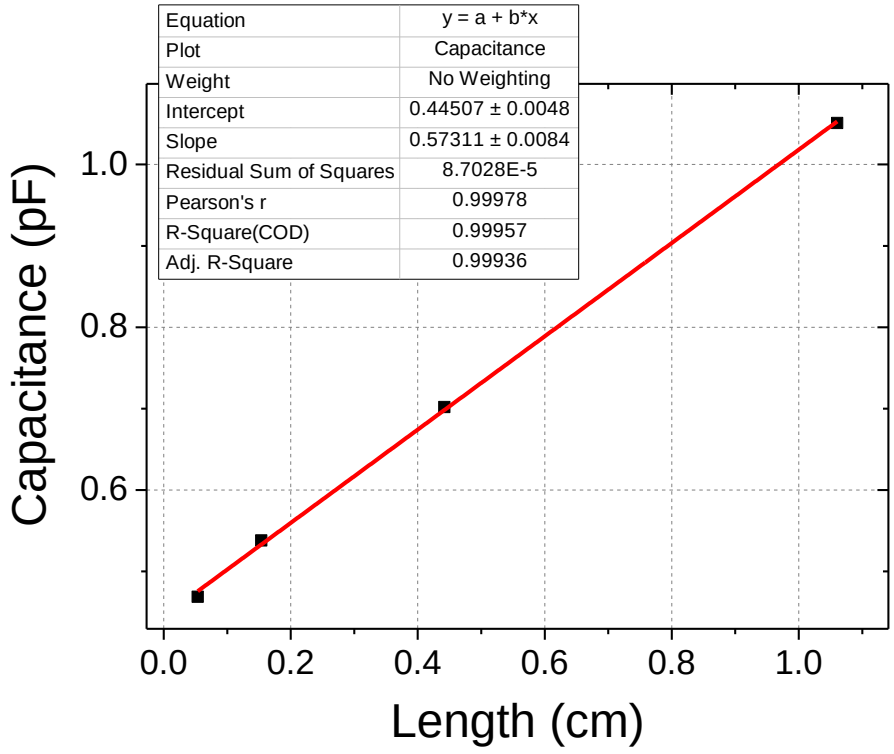


Figure 42 Capacitance vs Length- Unloaded Transmission Line

Measured electrical loss and epsilon values for microstrip unloaded line with BCB thickness of 12 μm is shown in Figure 43. Loss is around 5 dB/cm @ 67 GHz in this measurement. However, measurement across the other structures had a slight variation in electrical loss and could be approximated around 5.5±0.5 dB/cm @ 67 GHz. From the measured values of capacitance (0.57 pF/cm) and epsilon, impedance and inductance of the line is estimated to be 86.72±1.58 Ω and 4.286±0.154 nH/cm.

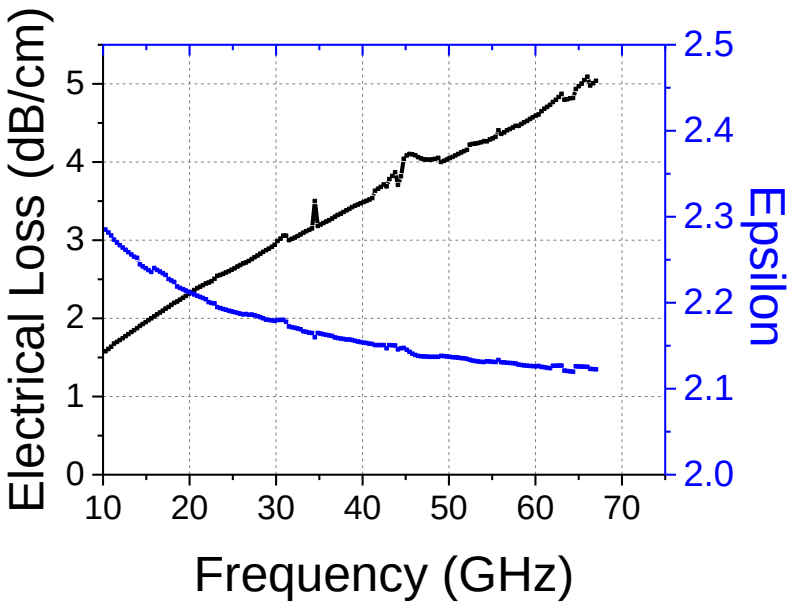


Figure 43 Measured Loss and Epsilon for Microstrip with BCB thickness of 12 µm

Using the above values for the unloaded transmission line along with a device capacitance of 2.82 pF/cm and another ~0.5 pF/cm for T-rails, expected velocity and impedance of the overall line is 33.87 Ω and 7.66 cm/ns. This would result in ~10.5 % velocity mismatch which would reduce modulator EO bandwidth. Parasitic capacitance must be decreased further to increase the impedance and to improve velocity matching. T-rail fill factor was 95 % with 100 µm period length.

4.3 Fabrication

Fabrication of the high speed MZM is mostly like that of the device as explained in chapter 2. Additional steps for microstrip fabrication will be explained in this chapter. Processing flow is shown in Figure 44. Numbers denote the lithography steps. First four steps involve metal contacts for top and bottom N GaAs along with waveguide and mesa etching. Ni/Ge/Au/Ni/Au contacts were used for ohmic contacts.

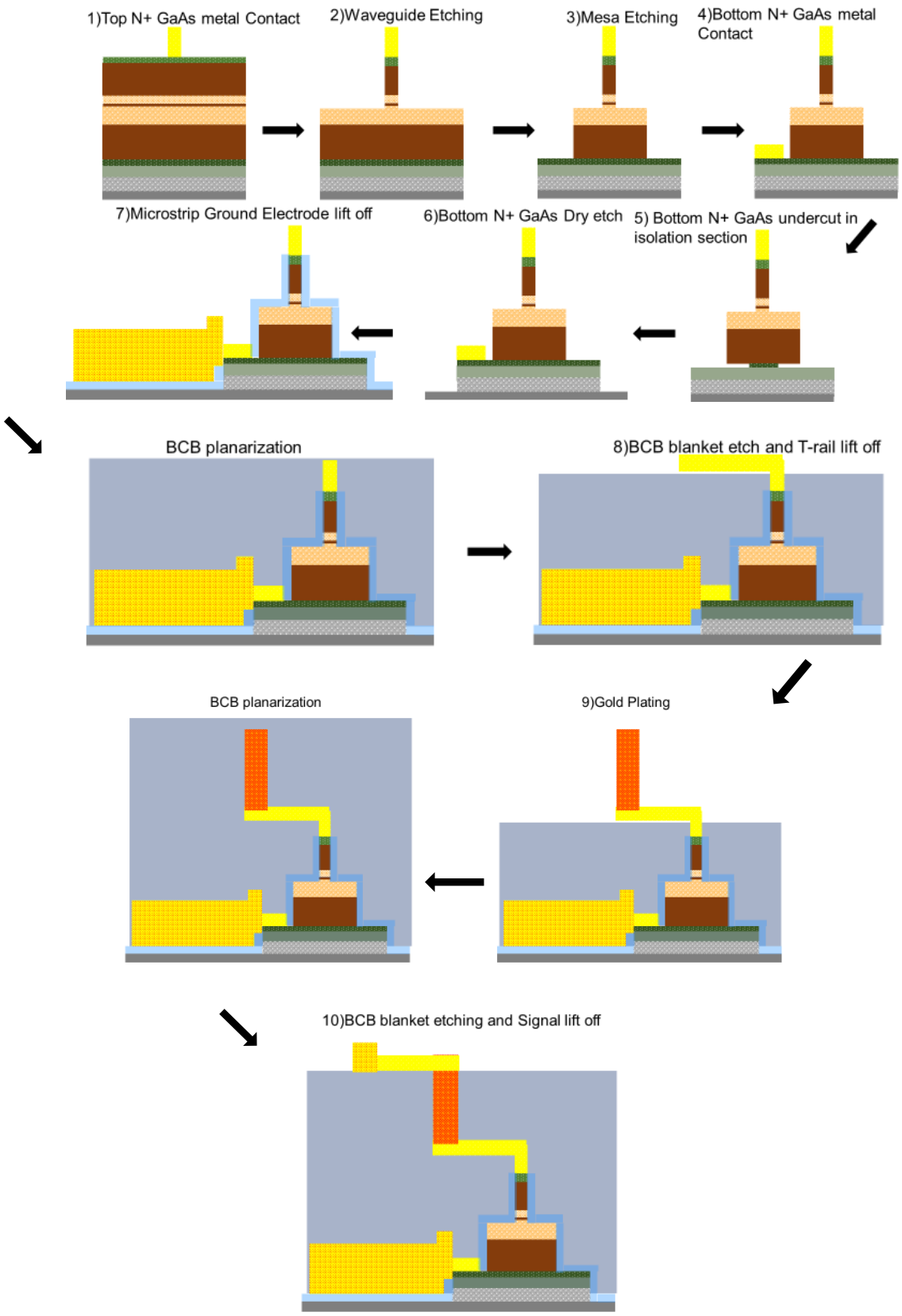


Figure 44 High speed MZM processing steps

After lifting off metal contacts for bottom N GaAs, both the contacts were annealed @ 430 C. To achieve electrical isolation for bottom N GaAs, in the 5 μm isolation section, using $NH_4OH:H_2O_2$:1:30, bottom N GaAs was wet etched by undercutting laterally from either side. Microscope picture of the undercut is shown in Figure 45. Etch rate is greater than 10 μm/minute and because of AlAs etch stop layer underneath, etch proceeds laterally.

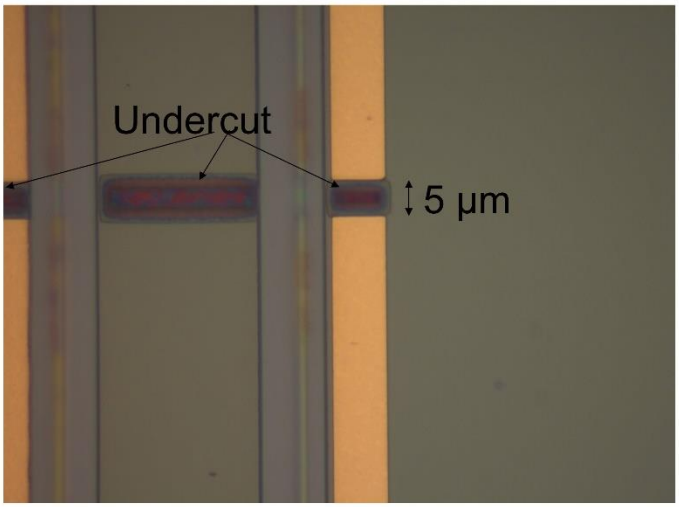


Figure 45 Microscope picture of bottom N GaAs undercutting

Bottom N GaAs is then dry etched in remaining areas until it reaches the bottom UID layers. Ground electrodes (1.3 μm) are then lifted off connecting the modulator through metal strips. Device was then planarized with BCB and blanket etched until the top metal contacts show up. T-rail are then patterned by combination of lift off and plating. Seed layer for plating for Ni/Au 25/60 nm. During plating, patterns was over plated and got widened. After this step, thick 10 μm gold structures were plated using AZP 4620 as plating resist. After plating, seed layer is removed by gold wet etchant for 5 seconds and nickel wet etchant for 2 minutes. Nickel wet etchant doesn't start etching at room temperature and requires heating @ 40 C for 2 minutes. Gold etchant etches nickel very slowly at room temperature and nickel etchant doesn't attack gold. Device is again planarized with thicker BCB in multiple coats and blanket etched using CF_4/CHF_3 plasma. Finally, RF electrodes are lifted with Ni/Au stack. Nickels

sticks better than Ti when directly deposited on BCB. Cross section of the final processed structure is shown in Figure 46 and the microscope picture of processed device is shown in Figure 47.

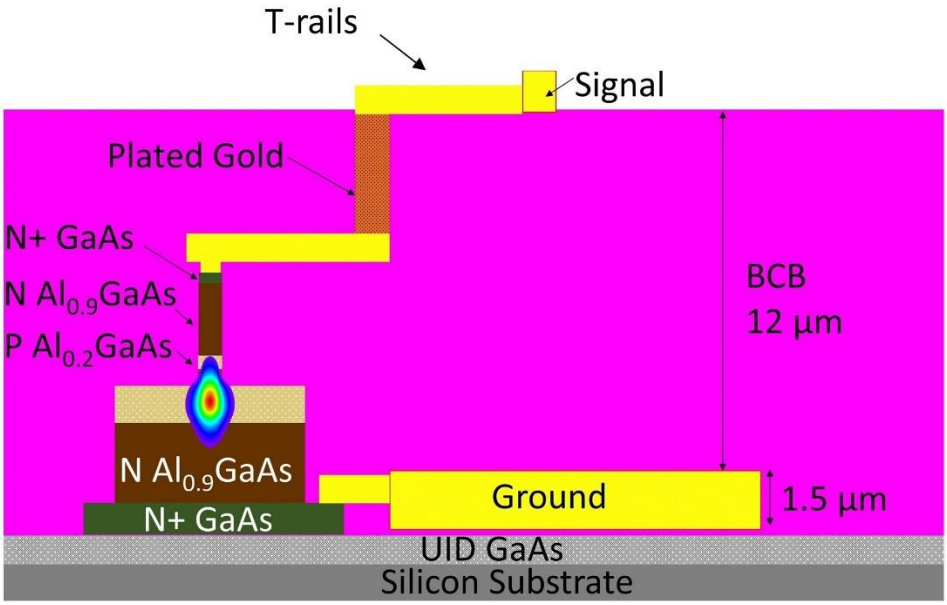


Figure 46 Cross section of final processed structure

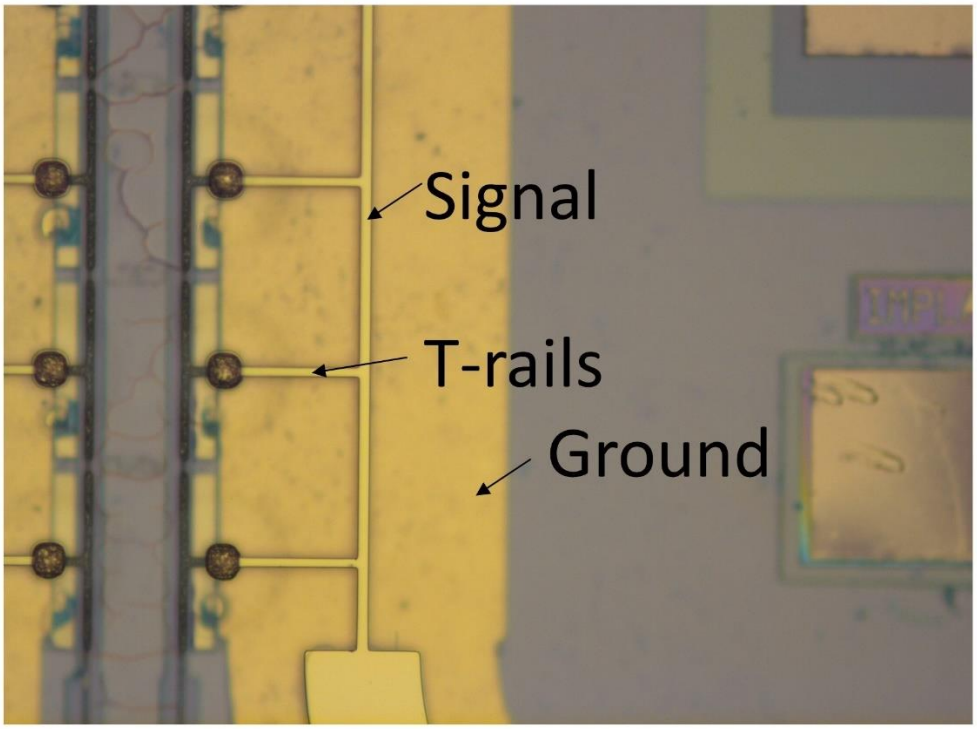


Figure 47 Microscope picture of processed device

4.4 Results

MZM with different lengths (0.5 mm, 1.5 mm, 4 mm, 7 mm, 10 mm) were fabricated. T-rail period was 100 µm with 95 µm active length and 5 µm isolation section. Electrical isolation for top NP contacts was achieved by using the low mobility of doped N $Al_{0.9}GaAs$ layer. In the 5 µm section, top N+ GaAs was wet etched. So, the resistance across 1.5 µm wide and 1.4 µm deep etched rib with N $Al_{0.9}GaAs$ layer over a length of 5 µm is around 26 kΩ which is much higher than the overall line impedance which would be less than 50 Ω, forcing the microwave current to flow only along the unloaded line. For the bottom N contact, as discussed before, N+ GaAs was undercut. However, capacitance measurements were carried out only at 1 MHz and so the measured value would be that of 100 % fill factor and not for 95 %. At 1 MHz, N $Al_{0.9}GaAs$ will still act as a good conductor. Measured capacitance as the

length is varied is shown in Figure 48. Overall capacitance measured is 4.23 pF/cm. Expected value was around 3.88 pF/cm and increase in number could be due to widening of T-rails during plating.

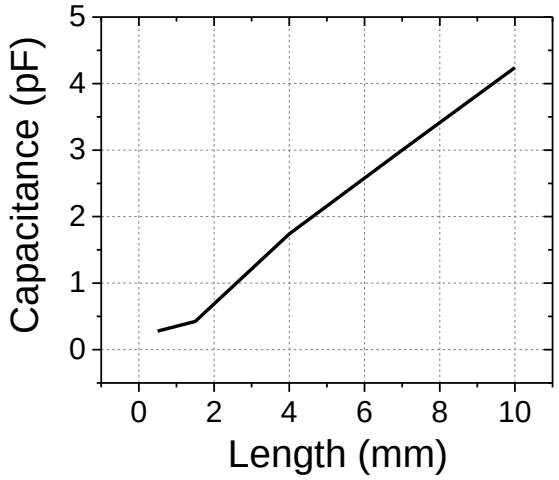
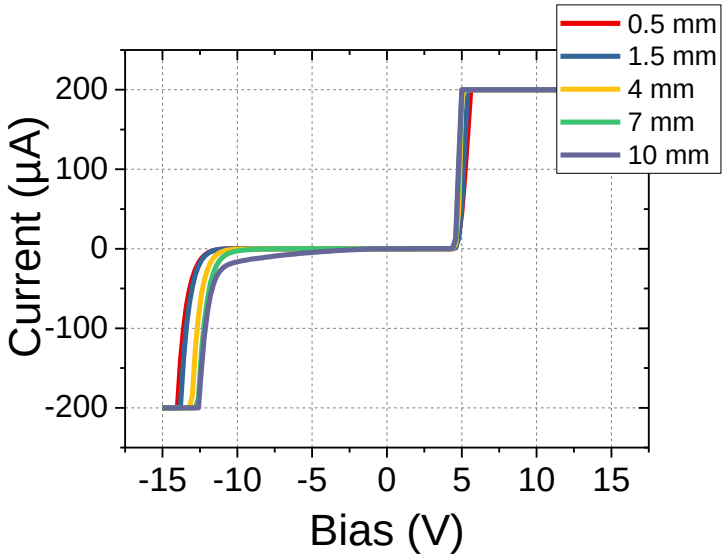
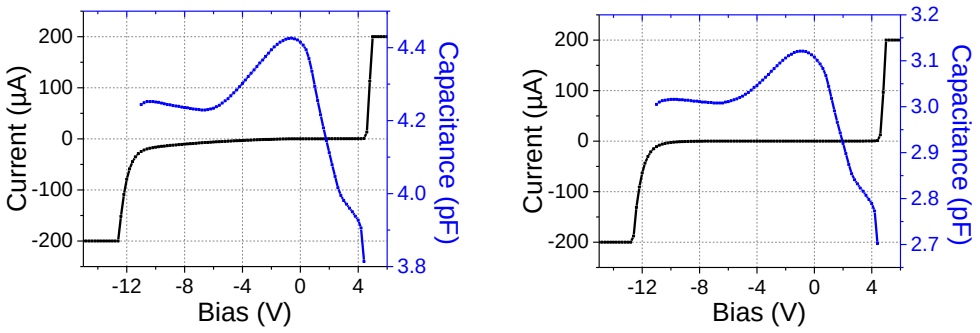


Figure 48 Measured Capacitance vs MZM active length



(a)



(b) **(c)**

Figure 49 Measured IV and CV. (a) Current vs Bias (b) 10 mm MZM CV and IV (b) 7 mm MZM CV and IV

In Figure 49 (a), current vs bias for different MZM lengths are shown. Apart from 10 mm, all other devices had negligible device leakage current and didn't breakdown until -11 V. 10 mm MZM has a slight increase in reverse current and could be processing related issue as 10 mm in other dies didn't breakdown until -11 V. Capacitance as shown by the blue curve appears to have some back ground doping initially. As the bias increases, capacitance becomes flat after the field swept away the background charges. Only one arm of the MZM was designed with RF electrodes. In order to operate the high-speed modulator in push pull scheme, bottom N layer must be electrically isolated from each arms of the interferometer. If that's not possible, then two independent RF sources are needed, and bottom N layer could be used as a common ground. If a single RF sources is used, then a BALUN based design is needed for inverting the RF signal across both arms of interferometer.

Measured phase velocity and impedance results for 4 mm electrode is shown in Figure 50. Measured electrical loss and modulator EO bandwidth is shown in Figure 51 and Figure 52 respectively. S parameters were converted to ABCD parameters, from which the phase velocity and loss was extracted using well known equations. Capacitance was already measured and with the phase velocity measurement, impedance and the inductance of the line

was extracted. Using the measured phase velocity and loss data, modulator bandwidth including the velocity mismatch is plotted in Figure 52.

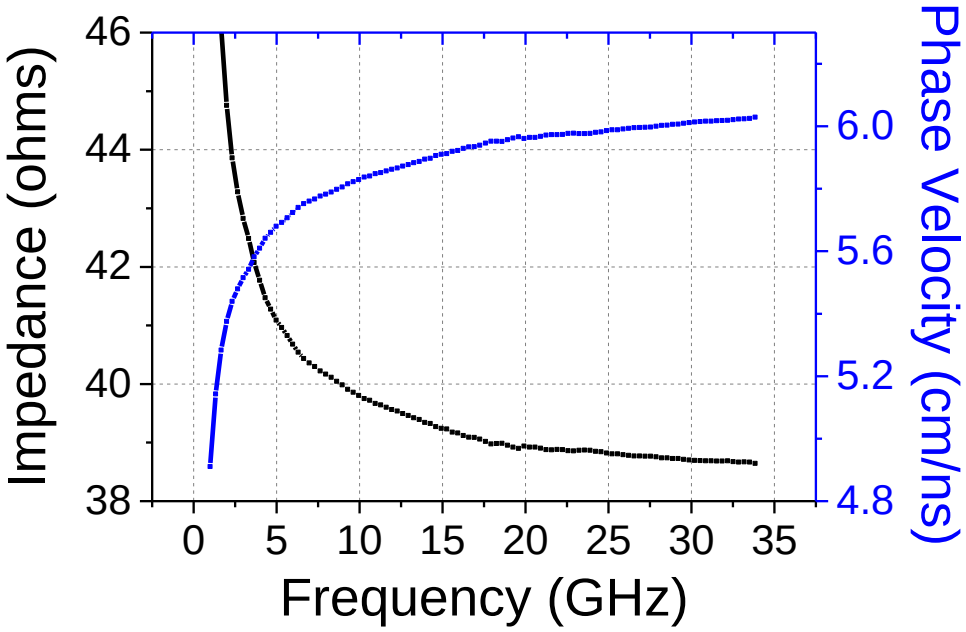


Figure 50 Measurement 4 mm MZM- Impedance and Phase Velocity

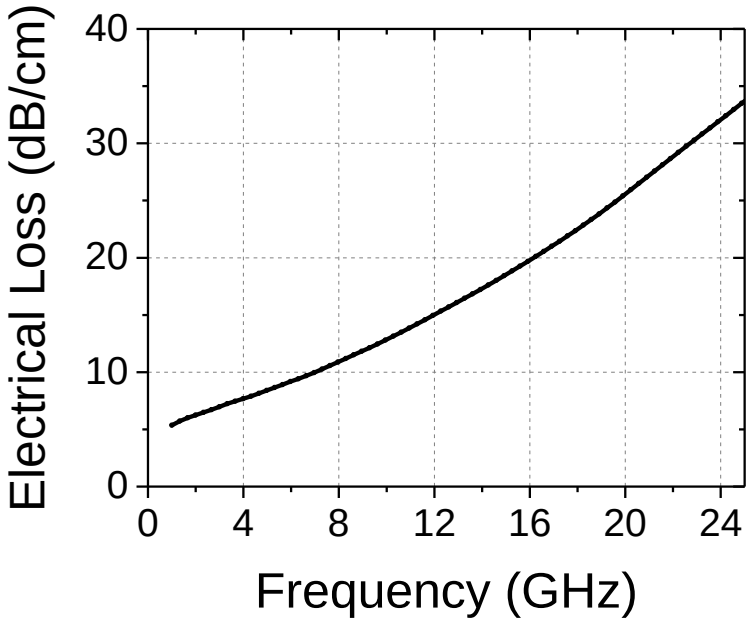


Figure 51 Measurement 4 mm MZM- Electrical Loss

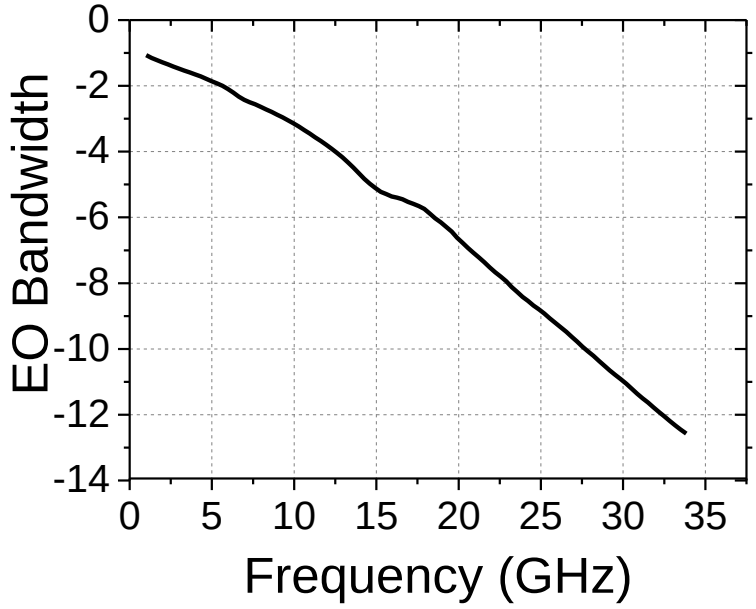


Figure 52 Measurement 4 mm MZM - Modulator EO Bandwidth

Phase velocity measured is around 6 cm/ns and is lower than the expected value of 8.5 cm/ns. Extracted value of inductance is 6.12 nH/cm. This value is higher than the unloaded line inductance indicating the fact that the microwave current is flowing through the doped semiconductor layers. N+ GaAs in bottom diode has lower resistance and wet etch undercutting was used to isolate the modulator section. It's very hard to check whether N+ GaAs was completely undercut without cleaving the device. Metal pads were small enough for it to be probed to check the isolation. Overall impedance of the line was around 37 ohms. 3 dB and 6 dB EO bandwidth was 9.6 GHz and 18.5 GHz respectively. Phase velocity mismatch also contributed to the reduction of the modulator EO bandwidth.

4.5 Simulation

In order to analyze the electrical loss contribution, the above device was simulated based on Figure 53. Capacitance and inductance of the unloaded line was set to be 0.55 pF/cm and 4.4 nH/cm and resistance and capacitance of the loaded modulators were set to be 3.69 pF/cm and 0.71 Ω/cm. Resistance and the conductance of the unloaded line was set to vary based on the frequency. It was assumed that the modulator was electrically isolated so that the current doesn't flow along the longitudinal section. It's a conservative estimate but would enable to analyze the main contributors to the electrical loss. Simulated results are shown in Figure 54.

Figure 53 Electrical Loss simulation equivalent circuit

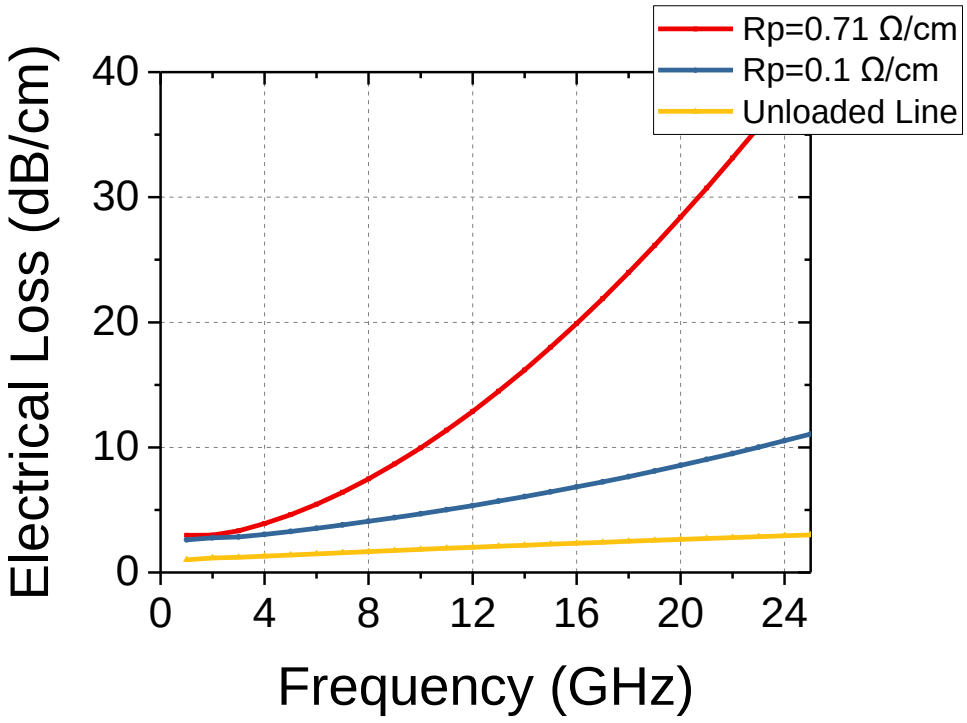


Figure 54 Electrical loss simulation with modulator

As resistance decreases, electrical loss improves significantly as seen from Figure 54. From chapter 3, electrical loss with the modulator section is given by the following expression $\alpha_{diode} = \frac{1}{2}(GZ_0) = \frac{Z_0}{2}\left(G_u + \frac{(\omega\Delta C)^2 R_P}{1+(R_p\omega\Delta C)^2}\right)$. First term inside the bracket represents the dielectric loss of unloaded transmission line and second term represents the loss due to the resistance and the capacitance of modulator section. Both the resistance and the capacitance have a significant impact on the overall loss. Using the above values, without including the second modulator term, $\alpha_{diode} = 0.0027$ @ 30 GHz while including the modulator parameters, $\alpha_{diode} = 0.1237$ @ 30 GHz, approximately 45 times higher than the unloaded line. With the microstrip based design, controlling the capacitance is challenging. A

reasonable number of around 3.2±0.2 pF/cm is possible by carefully controlling the lithography, BCB thickness and the modulator design. So, the resistance associated with the doped $Al_{0.9}GaAs$ layer should be reduced to improve the modulator bandwidth. It was initially planned to use another epitaxial design for high speed modulator. During fabrication, that chip was damaged in thermal annealing and the entire chip was shorted. Temperature during annealing ramped up high resulting in melting of gold contacts. In the next section, modified epitaxial design with some of preliminary experimental results is presented.

4.6 Modified Epitaxial Design

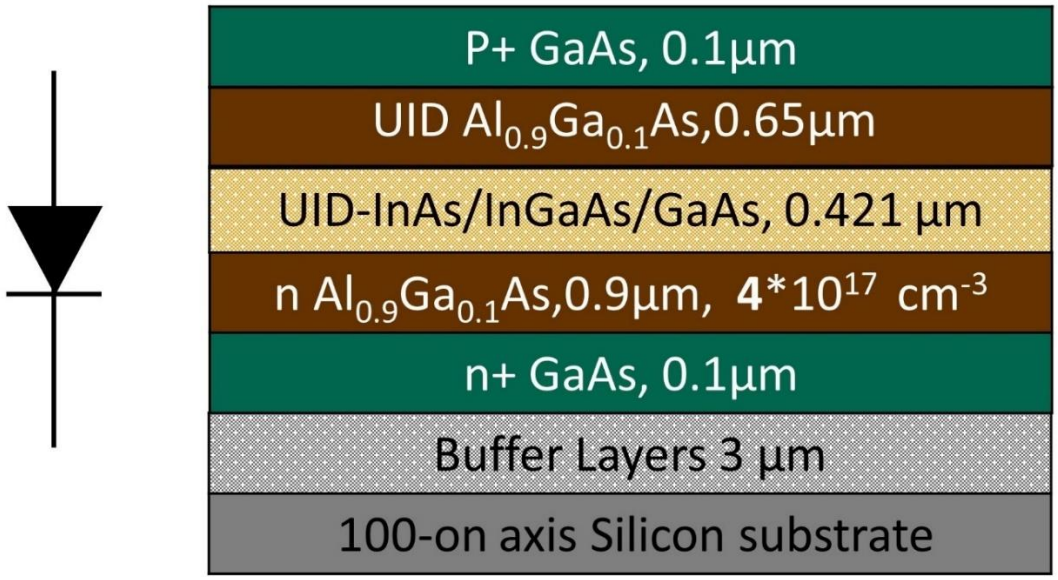


Figure 55 Modified Epitaxial Design

The proposed modulator design is shown above in Figure 55. It's a PIN diode with quantum dot core (PL peak @ 1.3 µm) which is 0.421 µm thick. Each QD layer consists of 7 nm InGaAs well with 46 nm GaAs as barrier. At 1.55 µm operation, absorption due to quantum dot layers will be negligible. The top cladding is designed to be UID $Al_{0.9}GaAs$ 0.65 µm, and the bottom cladding is designed to be N $Al_{0.9}GaAs$ which is 0.9 µm thick. Overall thickness of the intrinsic region is around 1.071 µm. This increases in thickness would

increase the drive voltage of the modulator, but the simultaneous increases in overlap of the optical mode and increased electro-optic coefficients owing to the quantum dot core could reduce the drive voltage of the modulator. Top waveguide cladding is kept undoped which would reduce the overall resistance associated with $Al_{0.9}GaAs$ layer leading to improvement in modulator bandwidth. Cross section of the passive rib waveguide is shown in Figure 56. It's a rib waveguide which 1.9 µm wide and 0.6 µm deep etched. 0.05 µm UID $Al_{0.9}GaAs$ is left unetched. It would help to reduce the propagation loss of the device and maintain single mode optical condition. Overlap of the optical mode in top 0.65 µm $Al_{0.9}GaAs$, 0.421 µm core and bottom 0.9 µm $Al_{0.9}GaAs$ is 7.82 %, 82.646 % and 9.52 % respectively. Overlap of the optical mode under the 1.9 µm rib in the above layers is 7.28 %, 71.388 % and 8.07 % respectively. Mode overlap with heavily doped p^+ and n^+ GaAs contact layers at the top and bottom is negligible. Only doping in the waveguide is *n* doping in the bottom $Al_{0.9}Ga_{0.1}As$ cladding and it contributes less than 0.4 dB/cm free carrier absorption loss.

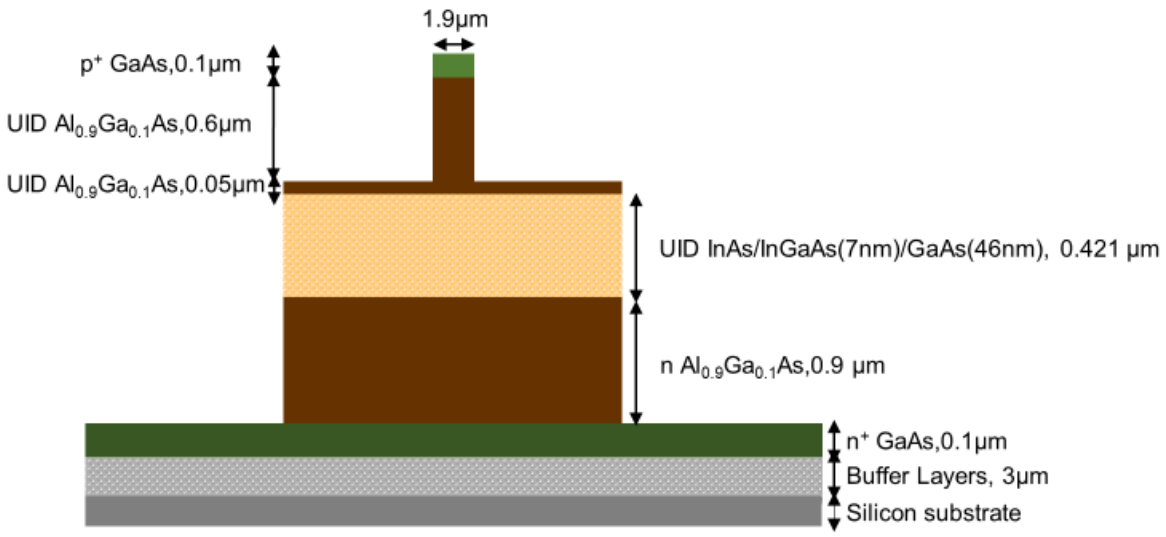


Figure 56 Cross section of Rib Waveguide in proposed design

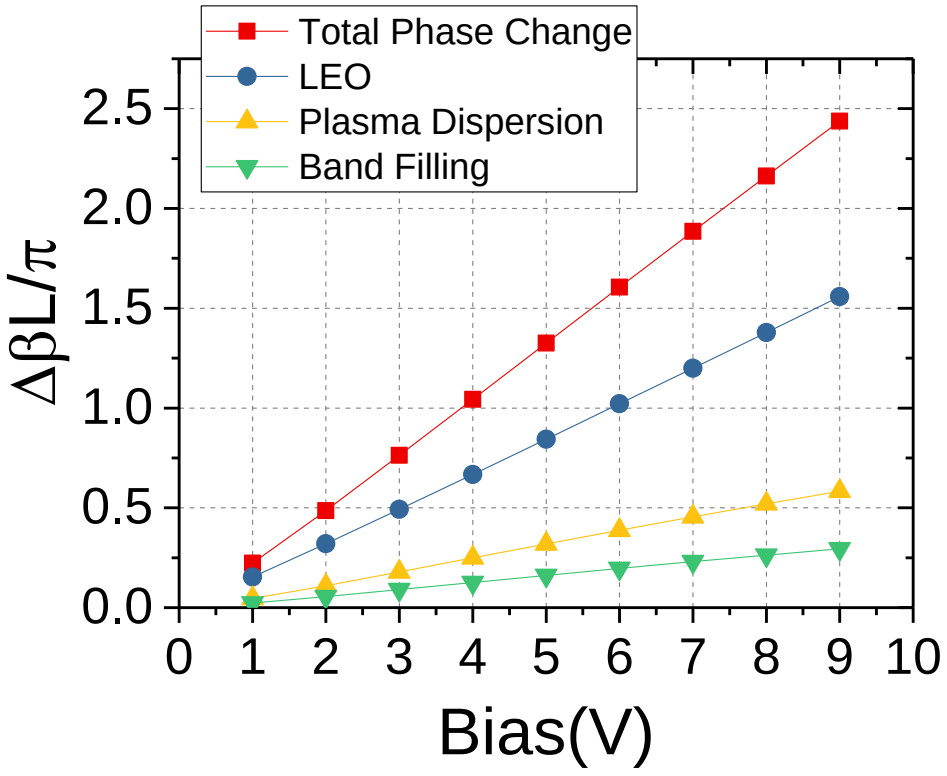


Figure 57 Simulated Phase Change vs Bias for 1 cm Electrode

For the above optical structure, using r_{41}=1.6 pm/V for both GaAs and the quantum dot, phase change vs applied bias was simulated for a length of 1 cm and is shown in Figure 57. Along the positive sweep, device was reverse biased in the simulation. Drive voltage at a bias of 2 V will be 4 V and as bias increases, drive voltage drops to 3.55 V. Initially, there is a 2DEG near the bottom n $Al_{0.9}GaAs$ which reduces the overlap of the mode with applied field resulting in an increase in the drive voltage. As the bias increases, 2DEG charges are swept away resulting in LEO being the major contributor. So, with this design under push pull operation, for a 1 cm long electrode, it's possible to get a drive voltage of 1.77 V. Even for high speed operation, the overall resistance associated with doped $Al_{0.9}GaAs$ and GaAs is only about 0.1024 Ω/cm. For the above design, calculated capacitance assuming a

parallel plate structure with a waveguide width of 1 μm is 0.933 pF/cm. So, for a 1.9 μm waveguide width, expected capacitance from device for a single arm is 1.77 pF/cm and for a push pull device, it will be twice the above value equal to ~3.55 pF/cm. Including the parasitic and unloaded capacitance and with a 100 % fill factor, for a single arm, around 2.5 pF/cm and for a push pull around 4.6 pF/cm is possible. Reducing the fill factor will decrease the capacitance at the expense of the increased drive voltage. From simulation in Figure 54, with this design, a 3 dB EO bandwidth of ~ 15 GHz with a drive voltage of ~ 3.5 V $V\pi$ is possible for a 1 cm device.

4.7 Optical Transmission Results

A very similar design was grown, fabricated and tested optically. Only change was a thicker bottom N+ GaAs and doping gradient in bottom N $Al_{0.9}GaAs$. Doping in bottom N $Al_{0.9}GaAs$ was graded from $2.3*10^{18}$ cm^{-3} near the N GaAs to $4*10^{17}$ cm^{-3} closer to the core. This doping gradient wouldn't change the optical transmission results. Fabrication was the same as to the device described in chapter 2 with BCB planarization. Cleaved devices were excited by a 2 μm spot size fiber at the input. Optical output was measured using an InGaAs photodetector after a 40x microscope objective lens. For push pull operation, arms of the interferometer are electrically isolated by etching the p^+ layer outside the electrode. Maximum current flow between the arms is less than a few μA. Bottom $n+$ GaAs layer was kept at ground potential during measurements making the *n* layers at the same potential for both arms. Current and normalized transmission for a 10 mm MZM as voltage is varied is shown in Figure 58. For positive voltages, device turns on and demonstrates diode behavior. The forward current is low due to thick *i*-layer. In the reverse direction, there is very low reverse current, and this shows that a large electric field that produces modulation is available in the

QD core. Drive voltage under single arm operation was 3.56 V corresponding to $V_\pi L$=1.78 V.cm under push pull. Blue curve is the measured data and red is fit with MZM transfer function. Because of the loss imbalance between the arms of the interferometer, there is a slight reduction in the amplitude of the on state as the bias increases.

Extinction ratio is mainly limited by the excitation of mesa modes during input coupling. For an 8 mm MZM as shown in Figure 59, V_π is 4.5 V and 2.2 V under single arm and push pull drive respectively corresponding to 1.76 V.cm modulation efficiency and for a 6 mm MZM under single arm, V_π is 5.70 V as shown in Figure 60 corresponding to 1.71 V.cm which agrees closely with 1.78 V-cm modulation efficiency measured for 10 mm electrode. Strong modulation is seen only after a reverse bias of -3 V as shown in Figure 58, when background doping has been depleted. On-chip propagation loss is estimated around 3 dB/cm based on the Fabry-Perot fringe contrast as shown in Figure 61. This is a worst-case estimate due to mesa modes, which are not modulated and reduce the fringe contrast. From measurements, $V_\pi L$ product could be estimated to be 1.745±0.035 V.cm. These results along with low propagation loss and low reverse leakage current confirm the excellent quality and uniformity of the material grown on on-axis Silicon wafer.

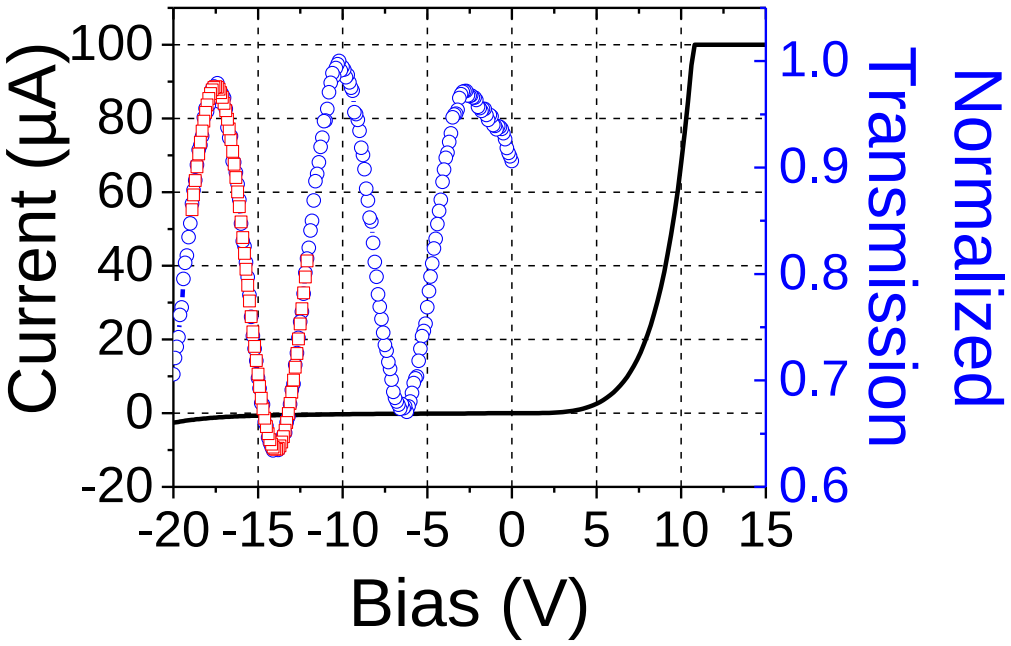


Figure 58 Measured optical MZM results for 10 mm electrode- Single Arm, Vπ=3.563 V.

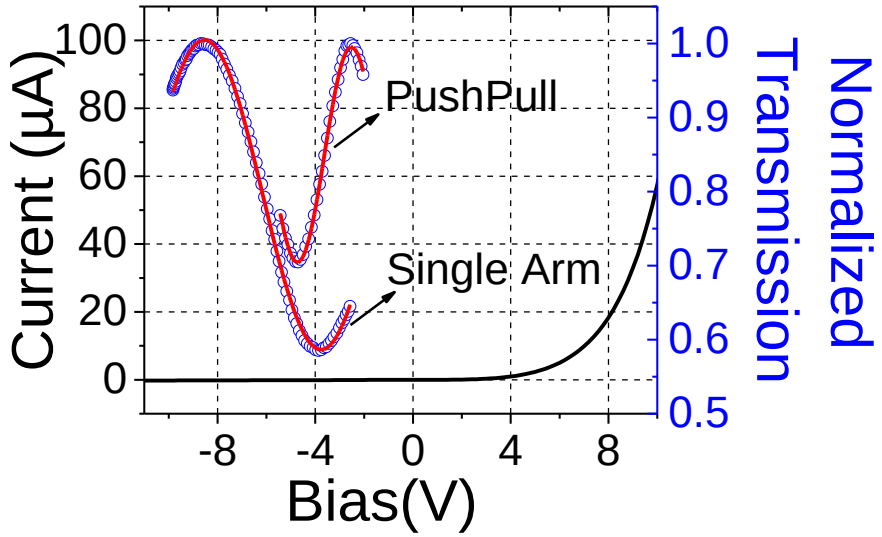


Figure 59 Measured optical MZM results for 8 mm electrode-

Single Arm Vπ=4.5 V and Push pull Vπ=2.2 V

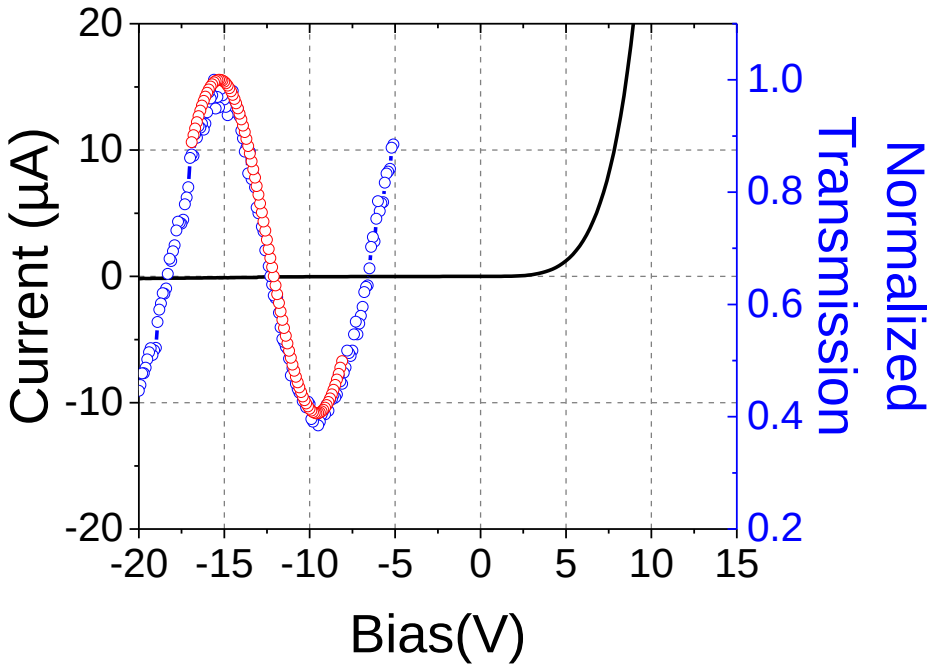


Figure 60 Measured optical MZM results for 6 mm electrode- Single Arm, Vπ=5.70 V

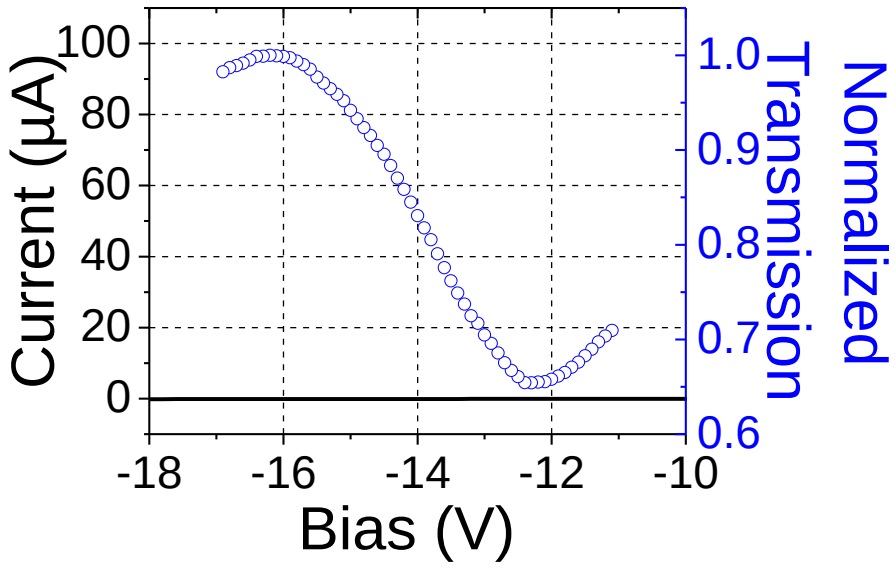


Figure 61 Measured transmission of a Fabry-Perot modulator with 1 cm long electrode

From the results, contribution of the quantum dots to drive voltage reduction seems negligible. However, one should fabricate a similar structure without quantum dot and using a bulk GaAs to confirm the actual contribution to drive voltage. It may be possible to use these devices as an electro-absorption modulator @ 1.3 μm and could be a possible future work. In any wavelength of operation, microstrip based design can be used to achieve high speed versions of these modulators. Capacitance data was also flat in reverse bias indicating minimal background doping in the intrinsic region. SEM of the cleaved rib waveguide is shown in Figure 62. Use of on-axis silicon wafer helped significantly in obtaining a good quality cleave. This modified design is capable of simultaneously achieving low drive voltage and low propagation loss while improving the electrical bandwidth. If perfect electrical isolation is achieved for bottom N+ GaAs, even in high speed operation, push pull scheme could be implemented with a single RF source and without the need of BALUN design thereby reducing the drive voltage of the device to 1.77 V.

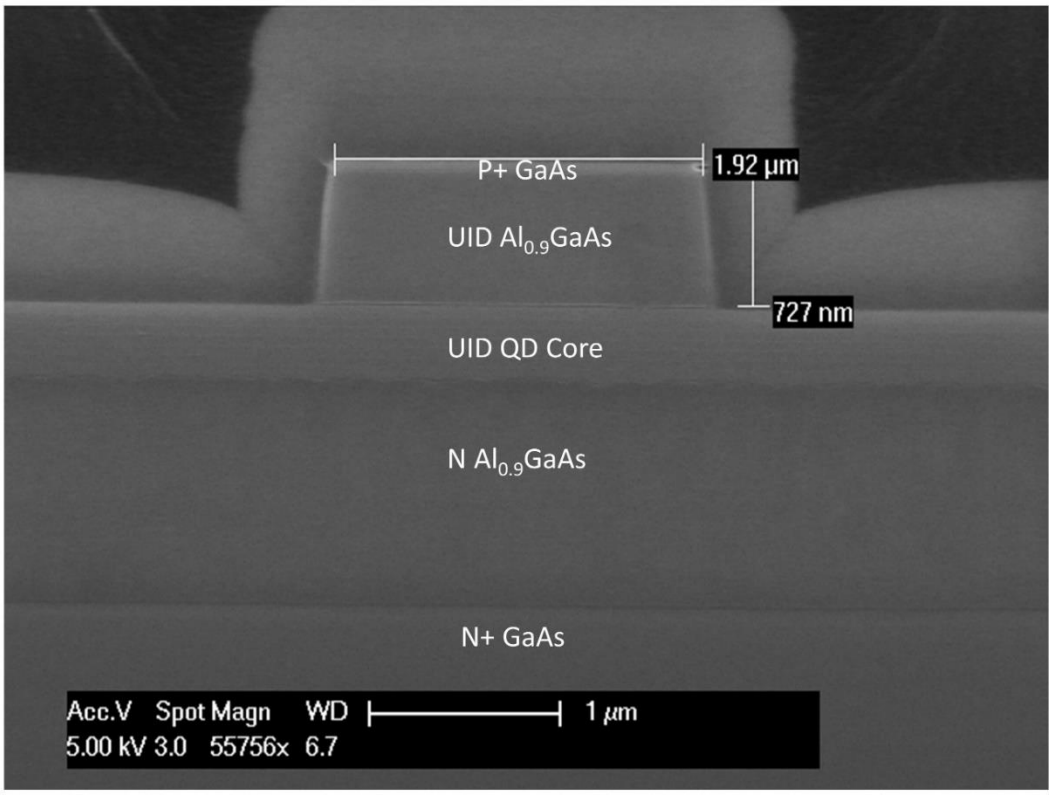


Figure 62 SEM of cleaved optical facet

4.8 Summary

This chapter reported on the design and fabrication of GaAs/AlGaAs based travelling wave MZM's using microstrip based unloaded electrode design. 3 dB and 6 dB EO bandwidth of 4 mm MZM were 9.6 GHz and 18.5 GHz respectively. A modified modulator design was proposed to improve the electrical bandwidth of the modulator along with simulation results. Preliminary experimental results on the drive voltage and propagation loss of the modified design on on-axis silicon wafer was presented. Device demonstrated a $V_\pi L$ product of 1.745±0.035 V.cm and propagation loss of less than 3 dB/cm. 8 mm MZM demonstrated a low drive voltage of 2.2 V under push pull. Modified design can achieve a 3 dB EO bandwidth of ~15 GHz for 1cm long device.

5 Compact GaAs Waveguides on Silicon substrate by AlGaAs Oxidation

5.1 Introduction

Popularity of silicon photonics is attributed to the low cost of silicon substrate and its mature processing technology. 220 nm crystalline silicon (SOI) with a 2 μm thermal oxide would result in single mode condition for certain channel widths leading to a very tightly confined optical waveguide. Low loss compact passive SOI waveguides have been demonstrated. However, in case of III-V material system, limitations on the refractive index contrast between the core and the cladding doesn't permit very tightly confined waveguides. Since III-V based devices are mostly fabricated on the substrate, decreasing the thickness of the core might result in optical mode leaking into the substrate. With a quantum dot laser [1] and a modulator [2] being demonstrated on silicon, having a compact III-V waveguide would enable simpler homogenous integration of active and passive photonic component.

Selective oxidation of high aluminum content layers in GaAs/ AlGaAs epitaxy has been used for several years in GaAs based VCSEL's and GaAs based electronic devices. Oxidation rate of $Al_xGa_{1-x}As$ layers are significant for values of x greater than 0.9. There have been work [3] conducted in our group before, studying the oxidation rates of $Al_xGa_{1-x}As$ layers grown on silicon substrates. $Al_xGa_{1-x}As$ oxidation is performed in water vapor atmosphere. In [3], 0.6 μm $Al_{0.98}Ga_{0.02}As$ was etched as a rib with metal contacts on top of it. Measuring the waveguide loss before and after the oxidation showed clearly a reduction in the propagation loss confirming that the layer has been oxidized. In [3], refractive index of oxidized $Al_{0.98}Ga_{0.02}As$ was estimated to be 1.66 @ 1.55 μm. This approach was used in this work to develop compact GaAs based waveguides on silicon substrate. In the first part of this chapter,

fabrication of compact GaAs waveguide by selective oxidation is explained. In the second half, selective dopant implantation in GaAs waveguide is discussed and possible future work combining the compact waveguide and selective implantation is proposed.

5.2 Device Design

Epitaxial layers were grown on Si substrates. These substrates were obtained from $NA_SP_{III/V}$, GmbH and have a 45 nm GaP layer on them. First, a 100 nm GaAs layer was grown at 500ºC at a very low growth rate, followed by a 1.5 μm GaAs layer grown at 580ºC with a growth rate of 1 μm/hour. This is followed by four cycles of thermal annealing between 400ºC and 700ºC. This step induces thermal stress and promotes dislocation motion. Next, 10 periods of InGaAs (10 nm)/GaAs (10 nm) super-lattice, with 10% In concentration were grown as dislocation filter layers. The buffer structure is finalized with 800 nm GaAs layer. 0.15 μm unintentionally doped (UID) GaAs layer is grown on top of the buffer layers before the waveguide structure is grown. Growth rate of device layers was kept at 1.8 Å/s for both Ga and Al, and the growth temperature was 580ºC. The composition grading was achieved using a digital alloy consisting of alternating GaAs/AlAs super-lattice.

Core of the optical waveguide was designed to be 0.29 μm GaAs. Under the core, $Al_{0.98}Ga_{0.02}As$ layer is graded to GaAs over a thickness of 0.02 μm. For simulations, core GaAs thickness was used as 0.3 μm to take the graded layer thickness into account. Simulations were carried out to find the optimum bottom $Al_{0.98}Ga_{0.02}As$ layer thickness. Cross section of the structure simulated is shown in Figure 63. Design was a rib waveguide with 0.8 μm width and 0.05 μm etch depth. A metallic layer was used under oxide layer to determine the influence of oxide thickness. From simulation, propagation loss increases rapidly for thickness under 0.2 μm and decreases gradually for thickness above. A value of 0.55 μm was

chosen for the epitaxial growth. Buffer layers under the $Al_{0.98}GaAs$ do not contribute to light guiding in oxidized samples. The refractive index of the oxidized AlGaAs layers at 1.55 μm was obtained from [3] as 1.66. With the current epitaxial design, there would not be any guided wave solution without the $Al_{0.98}GaAs$ oxidation since light intended to be guided in the GaAs core would leak into buffer layers and Si substrate.

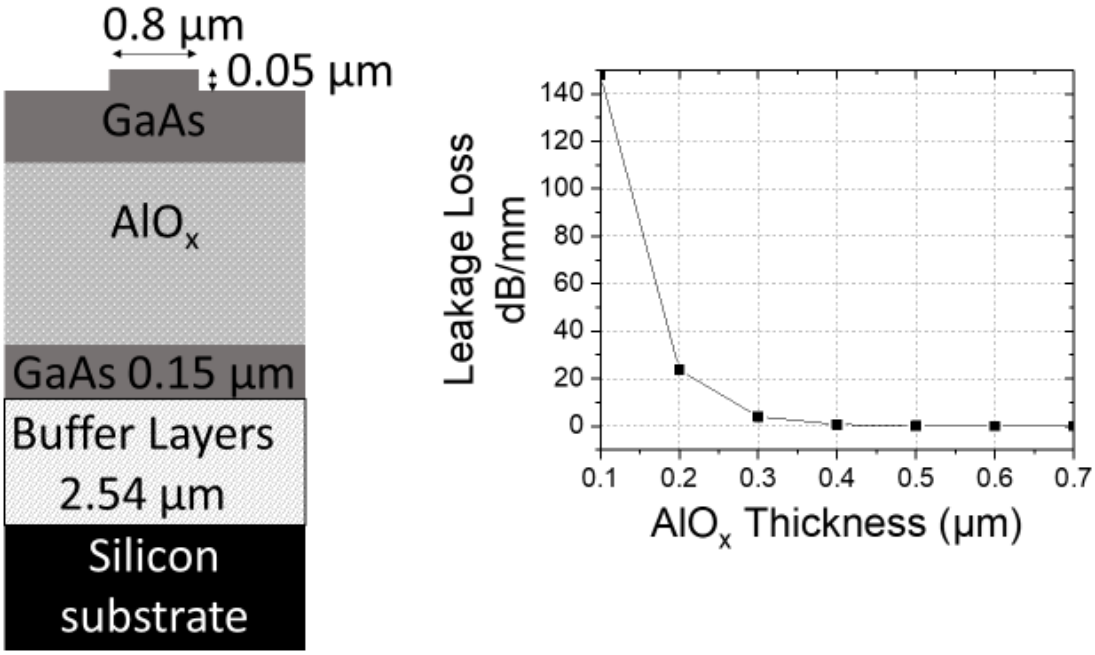


Figure 63 Cross Section of Simulated Waveguide Structure

5.3 Fabrication

Layer structure and fabrication steps are shown in Figure 64. During fabrication, a silicon nitride hard mask was defined for waveguide etching using lithography and CF_4/CHF_3 plasma. 0.8 μm wide and 50 nm deep rib waveguide was then etched in GaAs using Cl_2/N_2 plasma. This was followed by 100 nm more silicon nitride deposition and a 2 μm deep and 10

μm wide mesa etch. Finally, $Al_{0.98}GaAs$ layers were oxidized. $Al_{0.98}GaAs$ layer oxidation was performed laterally in water vapor atmosphere at 420ºC for 20 minutes.

Oxidation rate was calibrated using a test sample on GaAs substrate. Because of significant refractive index change, oxidized and un oxidized layers are distinguishable as shown in Figure 65. Mesas were etched using nitride hard mask and oxidation rate was calibrated. As seen in the figure, it has oxidized close to 21 μm in 40 minutes. Samples were then heated on a hot plate at 100ºC. Then the temperature was ramped to 270ºC over two minutes before depositing 200 nm PECVD oxide layer at 250ºC. No cracks were observed during the entire process.

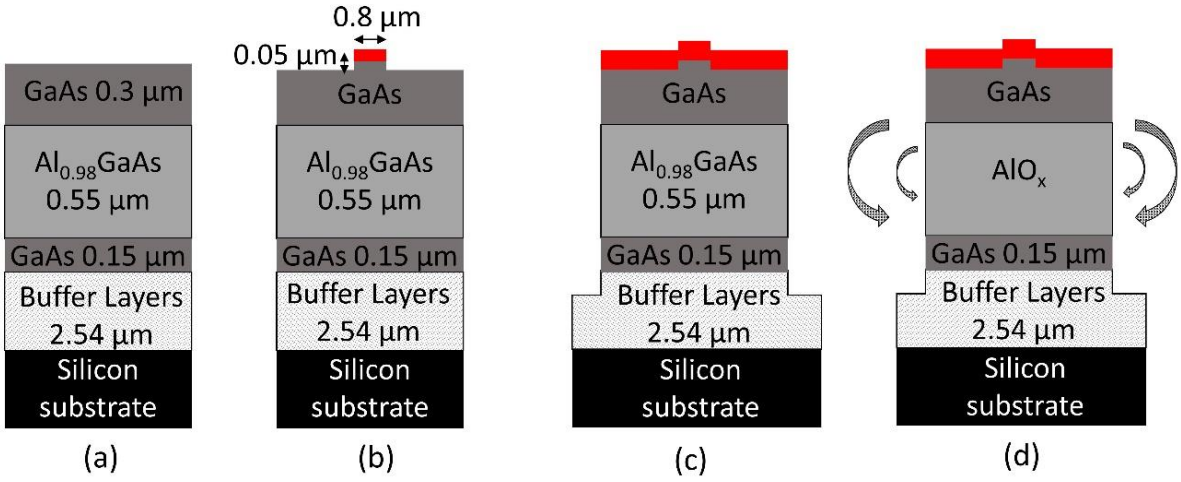


Figure 64 Fabrication Steps

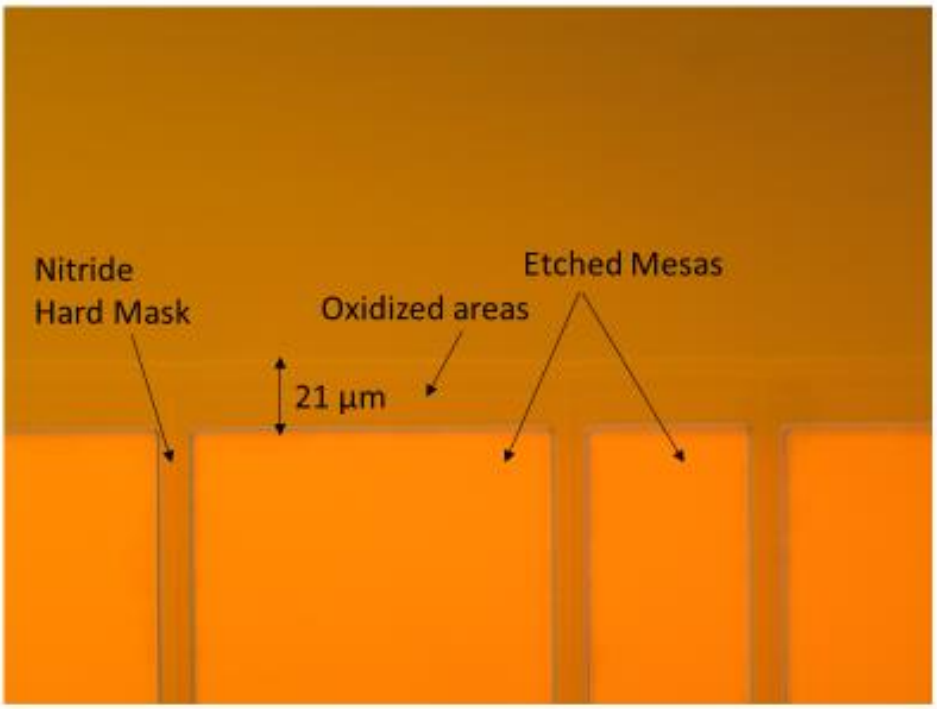


Figure 65 Microscope Picture of Calibration sample after Oxidation

5.4 Results

For facet formation, Si substrate was half-way diced from the back side and manually hand cleaved to a length of 4 mm. SEM picture of a facet is shown in Figure 66. Although facet quality of the buffer layers and Si substrate looks excellent, there were striations in the oxidized $Al_{0.98}GaAs$ and GaAs layers indicating the presence of strain. This may reduce facet reflectivity but is not expected to be a problem for coupling if gratings or mode transformers are used. The effect of strain on device performance needs to be further investigated. The calculated mode shape of a waveguide is shown in Figure 67. Mode is clearly tightly confined in the vertical direction. The resulting waveguide is very similar in both dimension and index wise to a SOI waveguide used in Silicon photonics.

During measurements, waveguides were excited at the input side using a 2.5 μm spot size fiber using a tunable laser around 1.5 μm. The output was coupled into an InGaAs photo detector using a 20 X objective lens. Two different rib waveguide structures with and without oxidized $Al_{0.98}GaAs$ layers were tested. Excited modes were examined using an infrared camera. It was not possible to excite guided modes in structures without $Al_{0.98}GaAs$ oxidation. Oxidized samples provided guided modes confirming the oxidized layer as the bottom cladding. The propagation loss of these waveguides was calculated using Fabry-Perot method. A typical fringe is shown in Figure 68. From the fringe visibility and using a facet reflectivity of 0.23, propagation loss was calculated to be around 4 dB/cm. With further processing improvements and better lithography tools, it might be possible to reduce the loss under 2 dB/cm. This approach would result in ultra-compact devices such as rings and channel waveguide with GaAs core. Transition between the quantum dot laser to these waveguides should be comparatively easier than the heterogenous approach since it doesn't involve bonding.

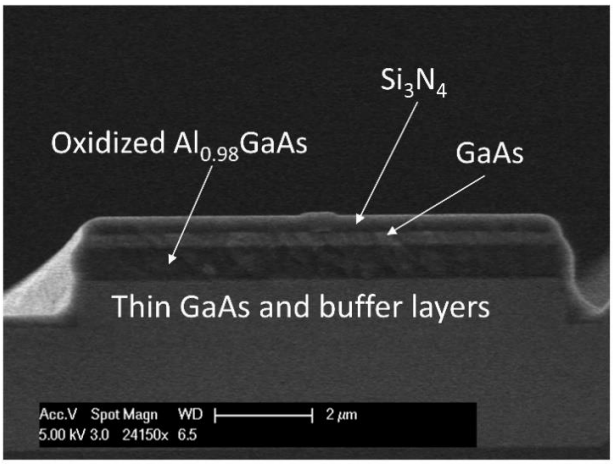


Figure 66 SEM of cleaved facet

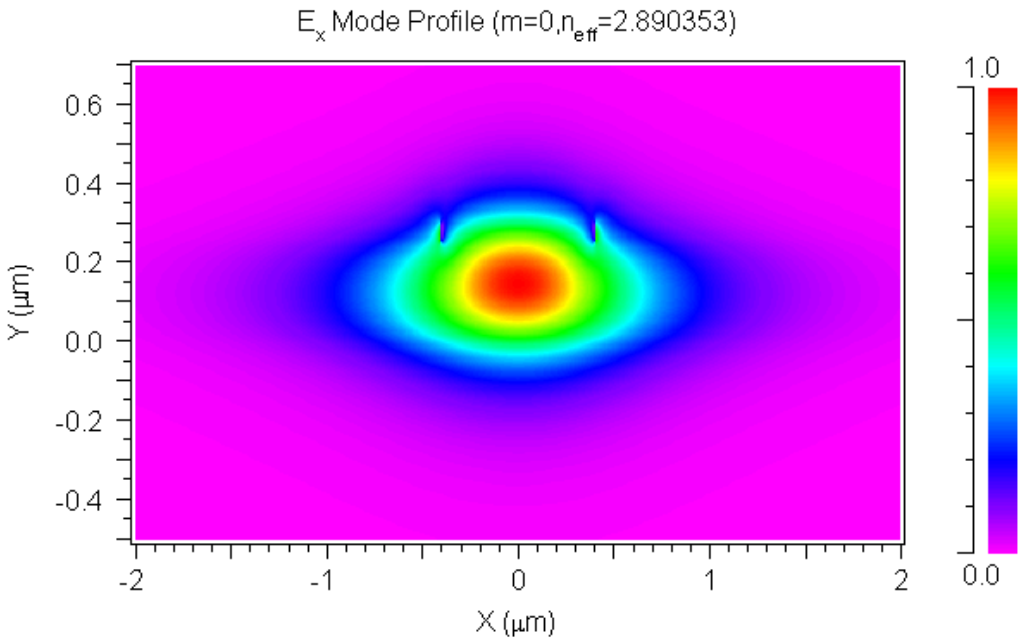


Figure 67 Simulated Mode Profile

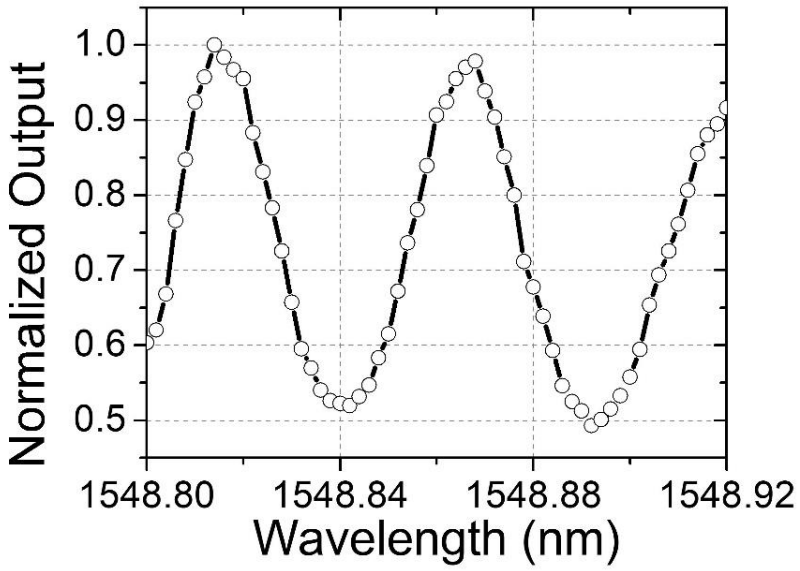


Figure 68 Fabry-perot Normalized transmission as a function of wavelength

5.5 Future Work-Selective Implantation of GaAs waveguides

In case of SOI based modulators [4], core of the waveguide is selectively doped with P and N dopants to create a lateral PN junction. Depletion region thickness is varied laterally to create a refractive index change along the arms of the interferometer. A GSG coplanar electrode periodically connects the active modulator section. Selective implantation helps to ensure that the microwave current runs laterally into the coplanar electrode and not along the waveguide propagation direction. Selective implantation could also result in low loss waveguides in y branches or other passive sections in a modulator. This selective dopant implantation has been in silicon technology for several years. Wafer typically requires an activation step at ~1000 C before making alloyed ohmic contacts. Silicon being a stable material doesn't have much of an issue during this activation step.

Since a very similar tightly confined waveguide has been demonstrated in GaAs on Silicon platform, we decided to test selective implantation and activation of dopants in GaAs waveguides. Selective implanted modulators on GaAs core should yield lower drive voltage modulators. Refractive index change due to free carrier plasma effect is inversely proportional to effective mass. Since the effective mass of electrons are lower in GaAs than silicon, for the same doping concentration, refractive index change should be higher. In addition to these, additional effects such as Pockel's effect and quantum confined stark effect in III-V will also yield lower drive voltages. Subsequent section briefly discusses the implantation and dopant activation procedure.

1.2 μm U-$Al_{0.9}$GaAs and 5 nm GaAs grown on SI GaAs was selectively patterned with a 50 nm oxide layer. A blanket SI GaAs without any epitaxial layer was also subjected to silicon implantation. Both these samples were annealed at 850 C for 15 seconds. Silicon

dopants energy was 130 keV with a dose of 6.6 e13 ions/cm^2. After the samples arrived, oxide was stripped and microscope pictures of sample with $Al_{0.9}GaAs$ after this step and before annealing is shown in Figure 69. Microscope picture after annealing is shown in Figure 70. Sample was significantly damaged after annealing and by looking under the microscope, there were some bright spots. It was the first time to try at selective implantation GaAs in our group. Main reason for sample damage appears to be from the oxide hard mask [5]. Oxide hard mask induces out diffusion of Gallium atoms resulting in a vacancy which would be eventually filled with Aluminum from underneath layers. This level of sample damage was not observed in SI GaAs substrate without any $Al_{0.9}GaAs$ layers. Better dielectric encapsulation was required in order to have this approach feasible.

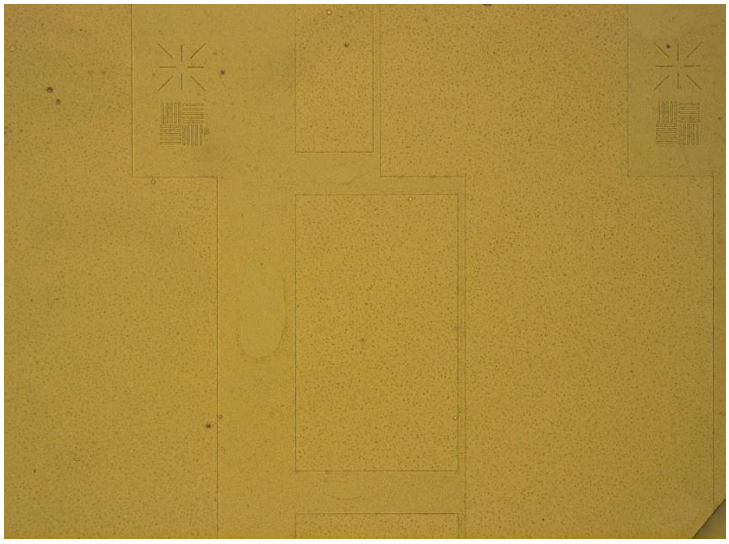


Figure 69 Silicon implanted sample before annealing

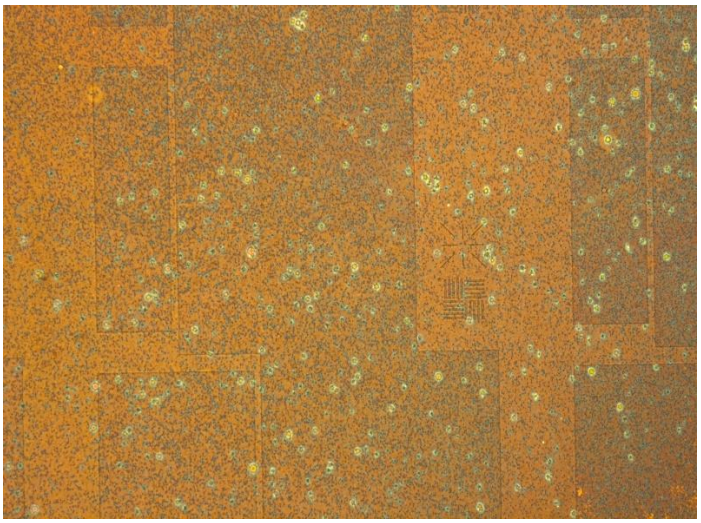


Figure 70 Implanted sample after 850 C annealing

PECVD deposited silicon nitride had slightly better result with respect to protecting the surface during annealing but was not able to achieve the results repeatably. Experiment was repeated with a slightly different epitaxial structure. Modified epi-layer details are shown

in Figure 71. Idea was to implant the 50 nm GaAs layer and after annealing, remove the 100 nm GaAs and 20 nm $Al_{0.9}GaAs$ layers.

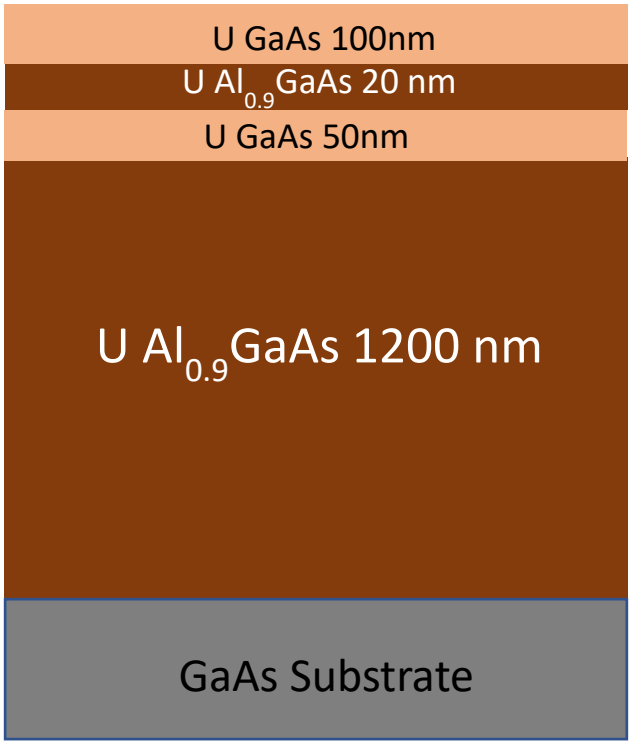
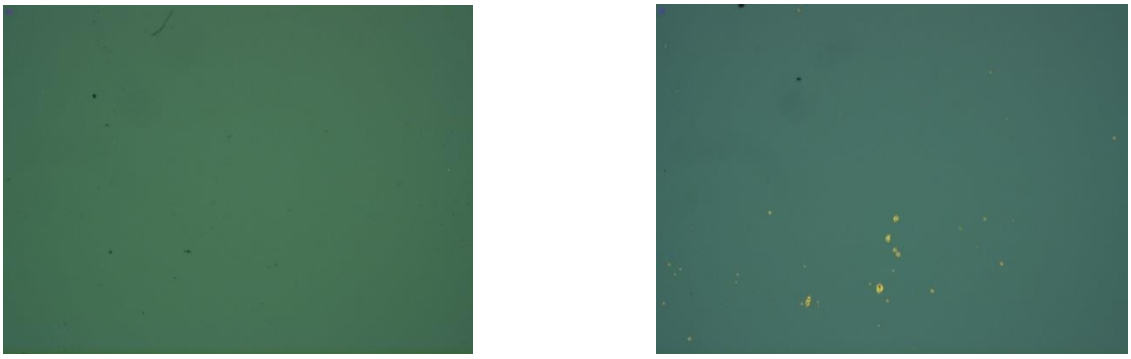


Figure 71 Modified epitaxial design for implantation testing

Reason for PECVD nitride not working as expected could be due to the presence of oxygen during its deposition. Nitride was deposited in our lab using silane (SiH_4) and N_2O. There is a slight chance that the film might be contaminated with oxygen. Silicon nitride deposited using sputtering techniques only involve silicon target and nitrogen plasma. Sputtering approach could be a better option for encapsulation of GaAs surface. Epilayer was implanted with silicon using a thin oxide mask. After implantation, oxide was stripped off using BHF. Before nitride sputter deposition, native oxide was removed using ammonium hydroxide. Inside the sputter chamber, sample surface was cleaned with Argon for 5 minutes before starting the nitride deposition. Argon clean helps to remove thin oxide layers.

This approach was first tested on a SI GaAs substrate without any AlGaAs layers. Microscope picture after 10 seconds of annealing at 800 C is shown in Figure 72. There weren't any visible adhesion issues with sputtered nitride on SI GaAs substrate after annealing. Sputtered nitride was then tested on sample with AlGaAs layers and microscope pictures before and after annealing is shown in Figure 73.

Figure 72 SI GaAs after annealing at 800 C with sputtered nitride as encapsulant



(a) **(b)**

Figure 73 Epilayer with sputtered nitride (a) Before Annealing (b) After Annealing

This approach resulted in significantly better surface when compared with either using PECVD oxide or nitride. Sputtered films are also denser when compared with PECVD films. After annealing, this sputtered film was next to impossible to be removed by BHF. ICP etch

removed the film, but at a slower etch rate. There was still 10-15 % surface damage after annealing on a quarter of 2-inch wafer with this approach.

5.6 PN Junction formation using selective implantation

PN junction could be created by implanting beryllium and silicon as dopants. Pockel's effect in GaAs grown on 100 wafer orientation for TE mode is possible only for electric fields applied in vertical direction. Creating a vertical PN junction is far more challenging than a lateral junction, one used in SOI based modulator. But, even with a lateral PN junction in GaAs, one could use free carrier and quantum confined effect and develop modulators with low drive voltages. Beryllium, because of its low mass number penetrates deeper than silicon. Proposed idea is to first implant with beryllium selectively and then with silicon to form a lateral junction. Cross section of processing flow is shown in Figure 74. Cross section of the intended modulator design is shown in Figure 75. Waveguide rib is designed to be a-Si. It has higher refractive index and could provide better mode confinement in lateral direction. Once the dopants are activated, metal contacts could be lifted off away from the rib to form ohmic contacts. AlGaAs oxidation should be after activating the dopant implants. Stress in oxidized AlGaAs layers is very high and sample shouldn't be exposed to temperatures higher than 300 C after oxidation. Mobilities of electrons in GaAs is higher when compared with that of silicon. For high frequency design, one of the limitations for electrical bandwidth is the resistance of the doped semiconductor layers. Having a GaAs based modulator should also help in improving the electrical bandwidth because of its higher mobility. Influence of selective implantation on mobility of charge carriers is yet to be investigated.

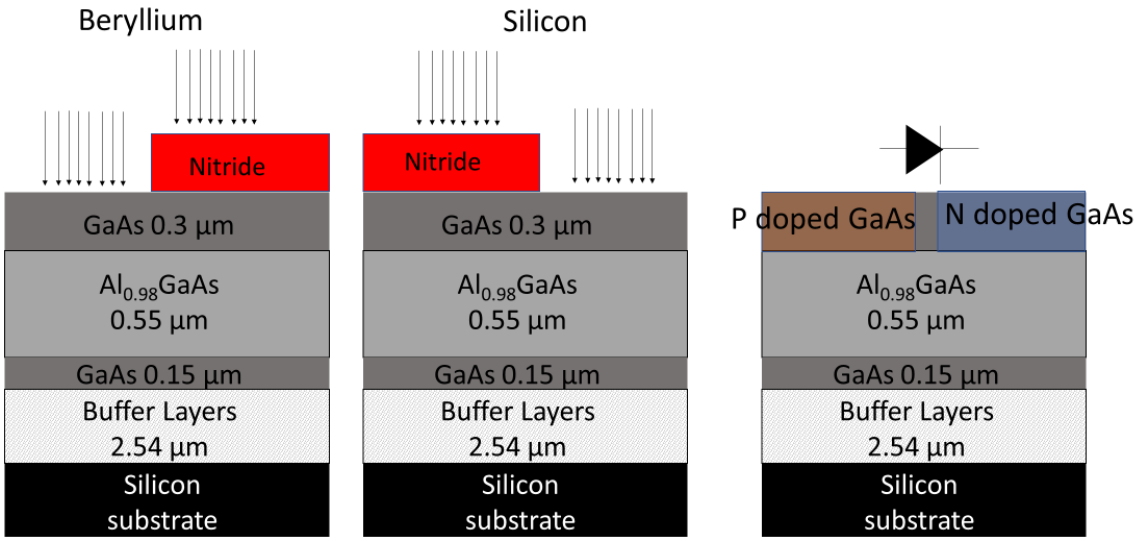


Figure 74 PN junction process flow

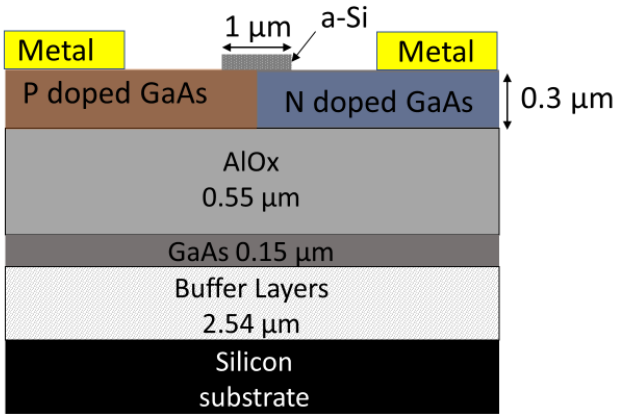


Figure 75 Selective Implanted GaAs based Modulator

5.7 Summary

This chapter explained the procedure for fabricating very tightly confined GaAs based waveguide. First the optical waveguide design was explained followed by the fabrication steps and the measured loss data. Propagation loss was around 4 dB/cm which is at an acceptable level and is expected to further improve with fabrication adjustments. With this approach, very tightly confined channel waveguides are also possible with GaAs core. Oxidized AlGaAs layers could also acts an etch layer when etching these channel waveguides.

Next, a detailed fabrication approach for developing very tightly confined GaAs based modulators on Silicon substrate was presented. Challenges such as surface decomposition of GaAs at high temperature dopant activation was solved using sputtered nitride as encapsulation. More than 80 % yield across a quarter of 2-inch wafer was achieved after activating the N type silicon implants. Active modulator design was discussed explaining the advantages and fabrication ways for this new approach. With this new GaAs on oxidized AlGaAs layers approach, it’s possible to develop efficient photonic devices on much bigger silicon wafer.

5.8 References

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6 Active-Passive Integration using amorphous Silicon Waveguides for substrate removed InP MQW MZM

6.1 Introduction

This chapter focuses on the design of mode transformers for substrate removed InP MQW modulator. This part of the thesis is different from the previous chapters. Modulator was grown on N doped InP substrate. Goal of the project was to reduce the coupling loss and the passive propagation loss.

Drive voltage length product of an electro-optic modulator is directly and inversely proportional to the thickness of intrinsic (I) region and optical confinement respectively. Lattice matched layers grown on InP substrate, at 1.55 μm have maximum index difference between the substrate and core of waveguide at the order of 0.3-0.4. With that index contrast, core of the optical waveguide must be at least 1 μm above the growth substrate to prevent optical mode leaking into substrate. It is not possible to simultaneously increase the confinement and decrease the thickness of the I region for substrate on devices. Removing the growth substrate could offer increased optical confinement with dielectric top and bottom claddings. Processed devices are bonded on to a transfer substrate such as Semi-Insulating (SI) GaAs using BCB as the bonding material. Growth substrate and the subsequent etch stop layers are removed using wet etching. It offers added flexibility of processing on both sides of epi layer. In case of active devices, contacts which were fabricated before bonding would be buried in BCB and can be reached by subsequent processing after substrate removal. For high speed modulators, removing the doped growth substrate and bonding with SI GaAs substrate improves microwave performance.

Coupling into tightly confined waveguides have always been challenging. Tapered lensed fibers have helped in improving the coupling loss, but the minimum spot size available is only 2 μm. Most of the silicon and substrate removed III-V Waveguides are under 0.5 μm in thickness which results in high modal mismatch loss. Suitable mode transformers are needed to couple light more efficiently from the fiber into these waveguides.

Doped layers near the core of the waveguide result in increased propagation loss in addition to losses associated with sidewall scattering. Passive section can be replaced with low loss waveguides such as Silicon Nitride waveguides to reduce the passive loss. To couple the light from III-V into nitride waveguide, width of the III-V waveguide must be tapered down to 150 nm. ICP plasma etching of III-V materials involves predominantly chlorine. Due to the non-volatility of Indium chloride by products at room temperature, etching is carried out at temperatures greater than 200 C. ICP etchers are very sensitive to chamber conditions. A slight variation could result in poor etched sidewall. As the width of III-V gets narrower, mode overlap increases with the sidewall and in turn requires an extremely smooth etching. It is challenging to etch MQW and the entire epi layer stack in a single step to a smooth narrow width. Rather than etching the entire III-V epi, it is possible to taper individual layers. But it increases the number of processing steps and tip at each transition must be narrow to reduce reflection.

Heterogenous integration of III-V and Silicon involves processing of III-V epilayer after bonding to Silicon On Insulator (SOI) [1]. Processed III-V wafers when bonded to SOI, requires very high degree of alignment accuracy since the silicon waveguides are defined first on SOI wafer. Bonding of unprocessed III-V epilayer onto SOI wafer reduces the flexibility of processing on both the sides of epi layer.

To process on both sides of epi layer and to use the robust processing of silicon, amorphous silicon (a-Si) was deposited on top of III-V substrate using PECVD. Oxide was used as an adhesion layer between the III-V and a-Si. PECVD growth of a-Si on III-V has many advantages as shown in Figure 76 such as

1) III-V surface necessarily doesn't need to be planar. It can be deposited over wide variety of surfaces since its PECVD.

2) It can be deposited at low temperatures (@250C)

3) Refractive Index of a-Si (3.545@1.55μm) is high enough to enable better coupling of light from III-V into a-Si.

4) Amorphous silicon could be simultaneously used as the passive section as well as a hard mask to etch III-V waveguides which makes the process completely self-aligned between both the material system.

5) Material loss of a-Si @1.55 μm is low [2, 3].

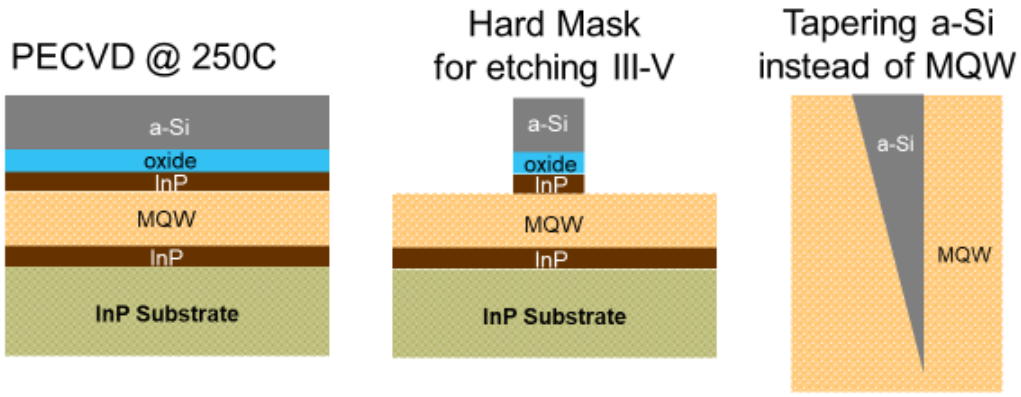


Figure 76 Amorphous Silicon on III-V

In this work, suitable mode transformers were designed and fabricated on a-Si waveguides to couple light out of III-V with more than 95% simulation efficiency. Another self-aligned mode transformer was designed to reduce the coupling loss.

6.2 Epi-Layer Details

Electro-optic effects require strong electric field to change the refractive index. Substrate removal enables strong optical confinement with very thin I region. In case of a rib waveguide, with a thinner I-region, optical mode could overlap with metal contacts. If the metal contacts are placed farther away from rib, it leads to additional capacitance. So, staircase waveguide design [4] was used where overlap between the doped layers and overlap of optical mode with metal contacts are reduced as shown below. Cross section of rib and staircase waveguide is shown in Figure 77.

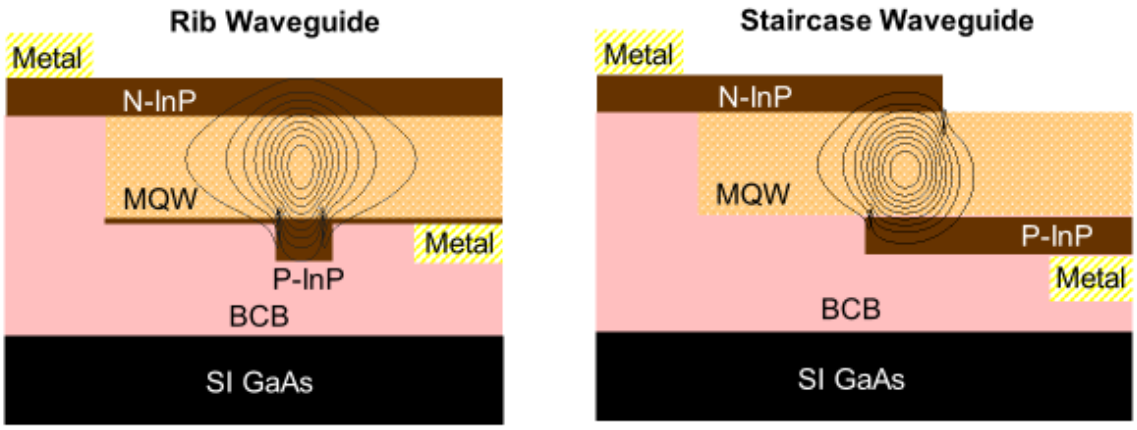


Figure 77 Rib and Staircase Waveguide

Epi-Layer consists of back to back diodes. NIPIN is used instead of PIN to reduce the microwave loss due to p doped layer. I-region in one of the diodes is much thicker than the other, so that for high speed operation, effective capacitance is the capacitance of thicker I region. In DC operation, one diode is always forward biased and other one is reverse biased. If the biasing is such a way that the bottom thicker diode is reverse biased, most of the voltage would be applied across the MQW region. Epi design starts with growing set of etch stop layers on S doped InP substrate for substrate removal. Thicker diode consists of

$In_{0.53}Al_{0.08}Ga_{0.39}As/In_{0.52}Al_{0.48}As$ MQW as I-region to make use of quantum confined stark effect in addition to linear electro optic effect. Photo luminescence peak of the MQW was set to be 1370nm, 180nm away from the desired wavelength of operation to reduce absorption. 400nm n-InGaAs is used to form non-alloyed ohmic contacts to the bottom thicker diode. $In_{0.52}Al_{0.48}As$ is used as barrier on either side of quantum well. Finally, other diode is formed with InP as I-region followed by n-InGaAs for non-alloyed ohmic contacts. Epi-layer design without amorphous silicon was completed by previous lab member.

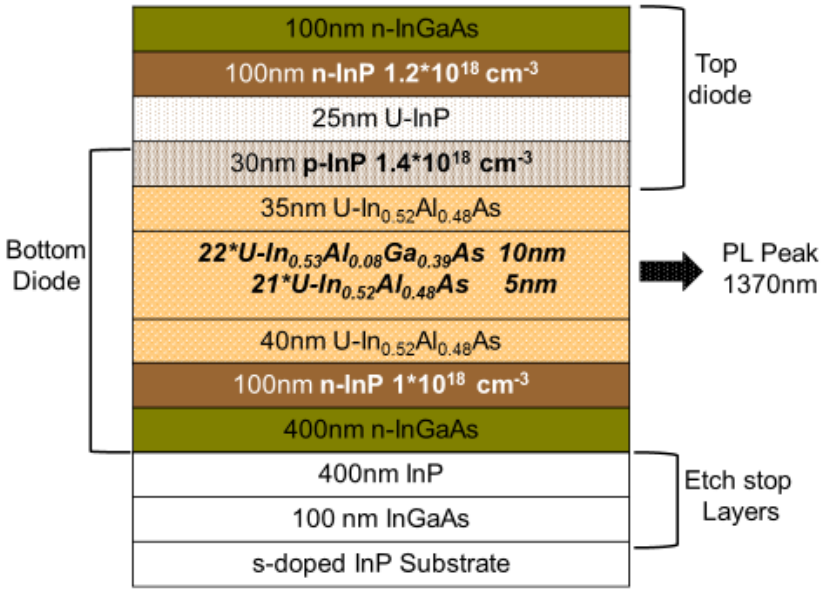


Figure 78 Epitaxial layer

6.3 Passive Design

To reduce the coupling loss, optical mode profile and the effective index of the waveguide at the facet must be closely matched with that of the coupling fiber. Polymers such as Su-8, BCB can be spun thick and lithographically defined to a waveguide to match its mode profile with the coupling fiber. But, to efficiently transition from tightly confined III-V or

Silicon to polymer waveguide, taper lengths must be sufficiently long, and the semiconductor taper tip must be under 100 nm. In that sufficiently long taper, side walls must be very smooth since it will be deeply etched. So rather than having a polymer waveguide at facet, reducing the thickness and width of the semiconductor waveguide would also result in weakly confined optical mode, easy to couple with tapered fiber.

Passive section was designed to be 40 nm thick a-Si waveguide. Effective index of such waveguide could be changed between 1.58-1.68 by tapering its width between 0.6-1.6 μm. Width corresponding to lower limit of the effective index could be used to easily couple into fiber and higher limit could be used in Y branches for increased confinement. Cross section of proposed waveguide and simulated modal mismatch loss for varying widths is shown in Figure 79.

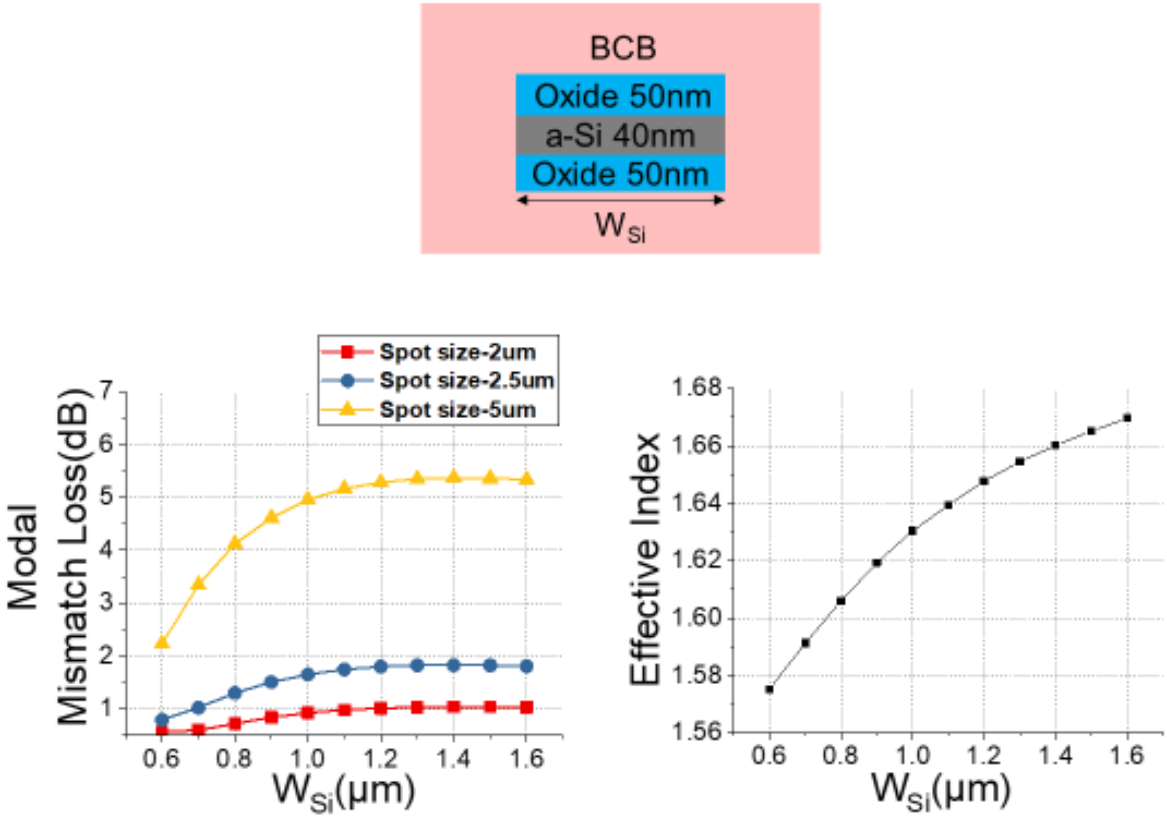


Figure 79 Thin Silicon waveguide-coupling loss vs width

For widths under 1 μm, modal mismatch loss under 1 dB/facet is possible with a 2 μm spot size fiber. As width increases, modal confinement increases, and hence modal mismatch loss increases. Tapering the width of the above waveguide between 1.5 to 0.6 μm can be easily fabricated over a very short length.

6.4 Index Matching to III-V

Thickness of a-Si must be greater than 40 nm to couple light out of the III-V fundamental mode (neff-3.207). 3D BPM simulations were performed to calculate effective index of fundamental mode for the composite cross-sectional structure shown in Figure 80. It's a cross sectional view of staircase waveguide with amorphous silicon layers. First 50 nm

oxide layer in a-Si stack is used for adhesion purpose. Second oxide layer is used as an etch stop for etching the top thick a-Si layer. Staircase waveguide is formed by etching InP rib of 155 nm and 100 nm thickness, before and after substrate removal. a-Si layers will be processed before bonding to SI GaAs.

Silicon width was chosen to be 1.5 μm to have maximum taper efficiency from III-V. For thickness under 325nm, silicon film provides only a slight index perturbation to the III-V fundamental mode. Thickness of the silicon must be greater than 325nm for index matching and was chosen to be 380nm. After 325 nm, optical mode is evanescent in MQW waveguide.

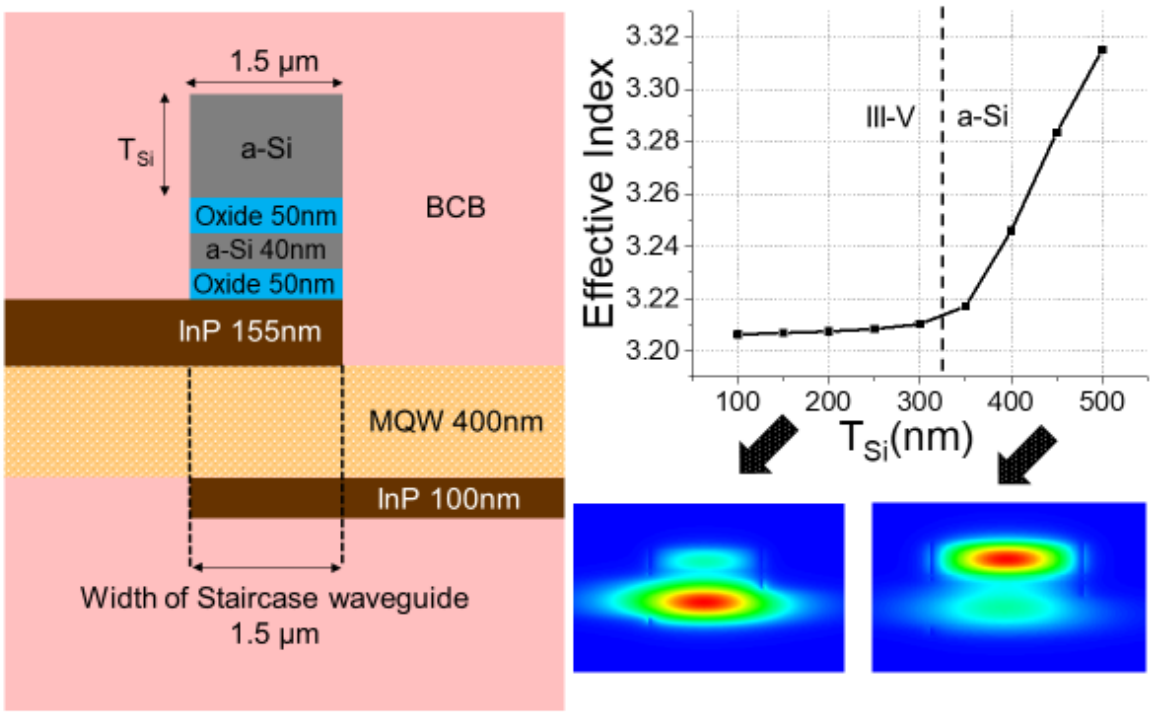


Figure 80 Index matching to III-V

6.5 III-V to amorphous silicon transition:

Effective index of the composite silicon waveguide with width 1.5 μm is higher than the III-V optical waveguide. Tapering the a-Si waveguide width would adiabatically couple the mode in and out of III-V. Transition involves two sections as shown in Figure 82.

1) Coupling from III-V into a-Si waveguide as a hybrid mode
    a. Depending on the taper length, there is 10-20% optical power still in III-V. Optical mode is evanescent in III-V waveguide after this transition.
2) Transition from hybrid silicon mode into composite silicon waveguide.
    a. Instead of tapering the MQW into a narrow tip, entire MQW section was linearly tapered as shown in Figure 82. III-V section just crosses the Silicon waveguide. Since this step involves etching III-V section underneath silicon waveguide, this step is fabricated after substrate removal. There is no challenging MQW tip to be fabricated in this design. Section 2 is necessary to reduce reflections as the optical mode transitions completely into the composite silicon waveguide

Process is completely self-aligned. Same design could be applied for transition from III-V to rib waveguide. One edge of the staircase waveguide will be etched using a-Si as the hard mask. Assuming a width of 1.5um, III-V to a-Si taper efficiency for varying lengths was simulated for section 1 and is shown in Figure 81. Transition length from hybrid silicon to silicon mode was simulated and chosen to be 80 μm. Tip width was assumed to be 100 nm in the simulation. Simulation was carried by launching staircase waveguide fundamental mode and computing the overlap of silicon fundamental mode at the output composite silicon waveguide. Simulation efficiency for section 1 was 98.4% for a taper length of 180 μm. Width

of the staircase waveguide was set to be 1.5 μm in the mask layout. Assuming a 0.5 μm misalignment, width of the staircase waveguide could be either 1 μm or 2 μm depending on which way misalignment goes during lithography. Simulations were carried out for three different widths by launching their respective fundamental mode and their efficiency were greater than 98%. As shown in Figure 82, taper etch involves only the top 380 nm silicon and the remaining 40 nm a-Si along with oxide layers are still present on top of staircase waveguide. It doesn't perturb the mode profile of staircase waveguide.

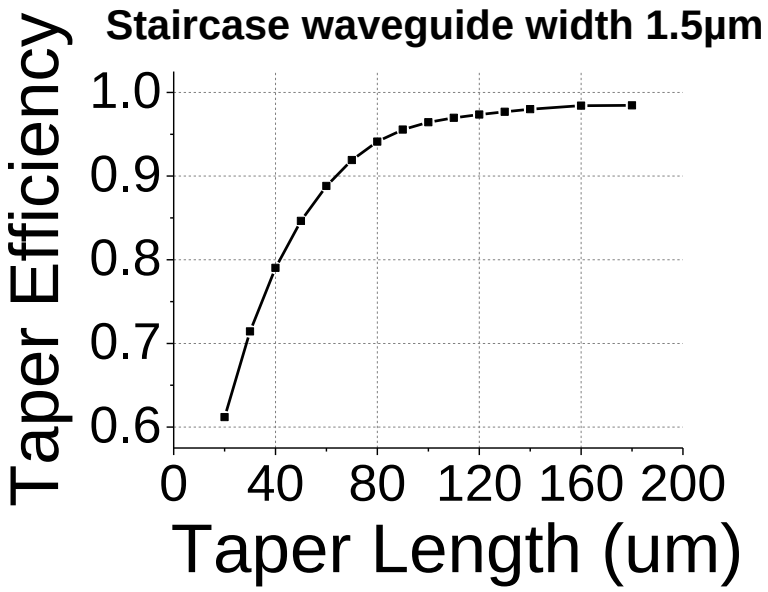
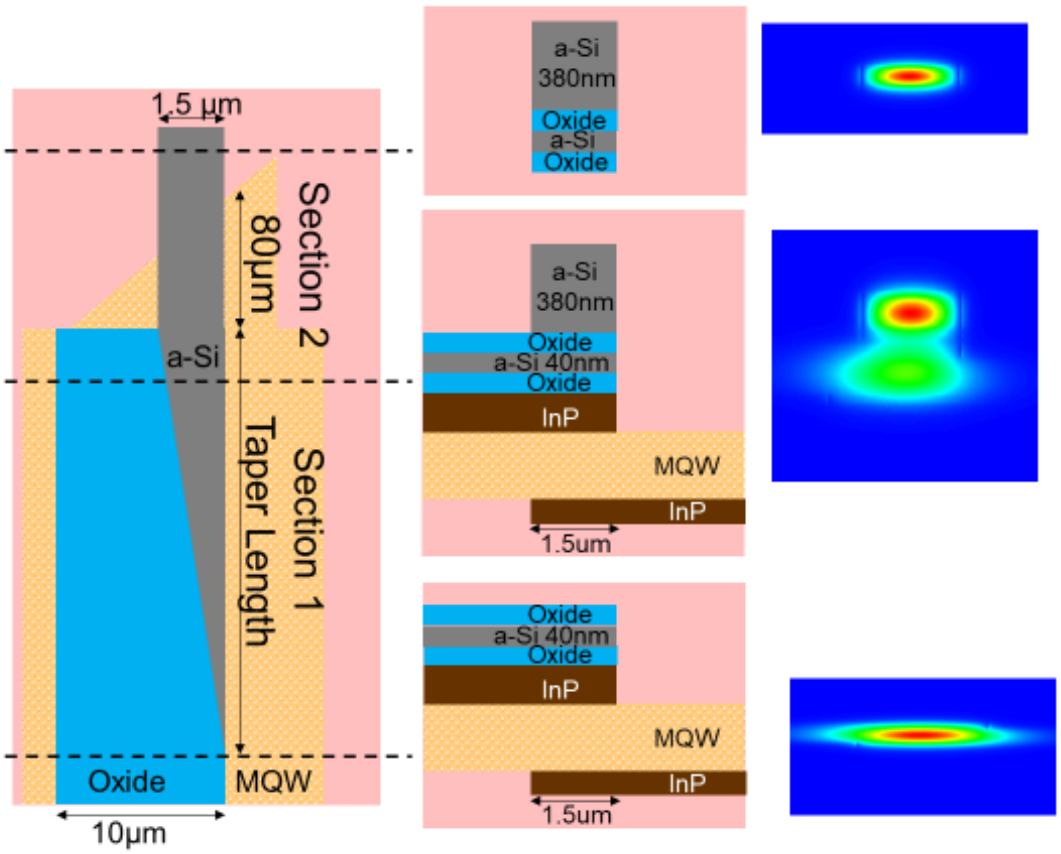


Figure 81 III-V to a-Si waveguide transition simulation

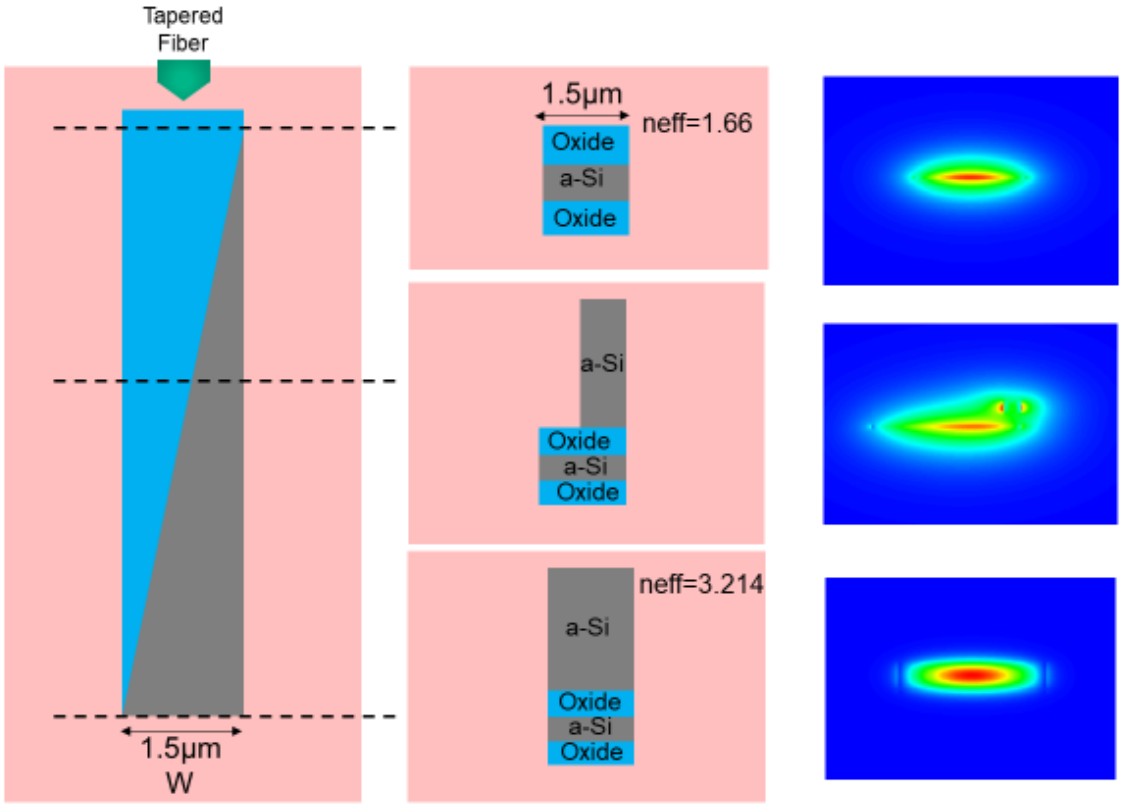


(a) Top View **(b) Cross Sectional View** **(c) Corresponding Mode Profiles**

Figure 82 III-V to a-Si Taper,

6.6 Thin to Thick Silicon waveguide transition

Self-Aligned mode transformer from thin silicon waveguide to composite thick silicon waveguide was also designed. In Figure 83, top, cross section and the corresponding mode profiles of transition from tapered fiber to composite thick silicon waveguide is shown. As discussed in previous section, only the top 380 nm silicon's width is gradually varied. If the III-V epilayer is removed near the y branches, it's possible to fabricated weakly confined 40 nm thin silicon waveguide near the facet



(a) Top View **(b) Cross Sectional View** **(c) Corresponding Mode Profiles**

Figure 83 Thin to thick silicon waveguide transition

Width(W) of composite silicon waveguide determines the following factors

1) Single mode condition of thin silicon waveguide since the process is self-aligned
2) Taper tip width tolerance for transition from composite silicon waveguide into thin silicon waveguide as the effective index of thin silicon waveguide increases with width (W) and hence the tip tolerance improves.
3) Coupling efficiency from III-V into composite silicon waveguide.

Optimum width of 1.5 μm was chosen after considering all the above three factors. 3D BPM simulation were performed to find the optimum taper length and taper tip. Fundamental mode of composite silicon waveguide was calculated and used as the launch field. Since BCB (n-1.535) is used for bonding, it becomes one of the optical cladding. Photo

BCB (n-1.543) is used as the other optical cladding since it could be lithographically defined to open the buried electrical contacts. Assuming a taper tip of 100 nm, taper length greater than 150 μm results in more than 95% taper efficiency as shown in Figure 84. Assuming a taper length of 250 μm, taper tip must be under 150 nm for greater than 80% efficiency. Width of the thin silicon waveguide in y branches could be 1.5 μm to improve the confinement and the width could be tapered down to 0.8 μm at the facet. Width of 0.8 μm was chosen keeping in mind the repeatable resolution limit of stepper in our clean room.

Top view of the overall transition is shown in Figure 85. Tapered fiber excites the weakly confined thin silicon mode. A linear taper gradually varies the width of 380 nm thick silicon layer thereby coupling the light from thin silicon waveguide to staircase waveguide. In a single lithography, it's possible to achieve both these transitions.

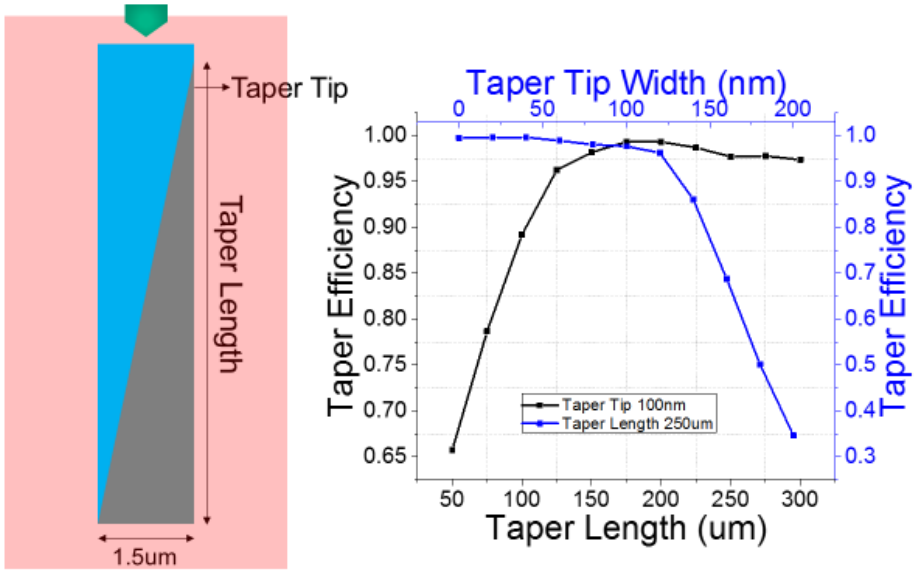


Figure 84 Thin to thick silicon waveguide BPM simulation

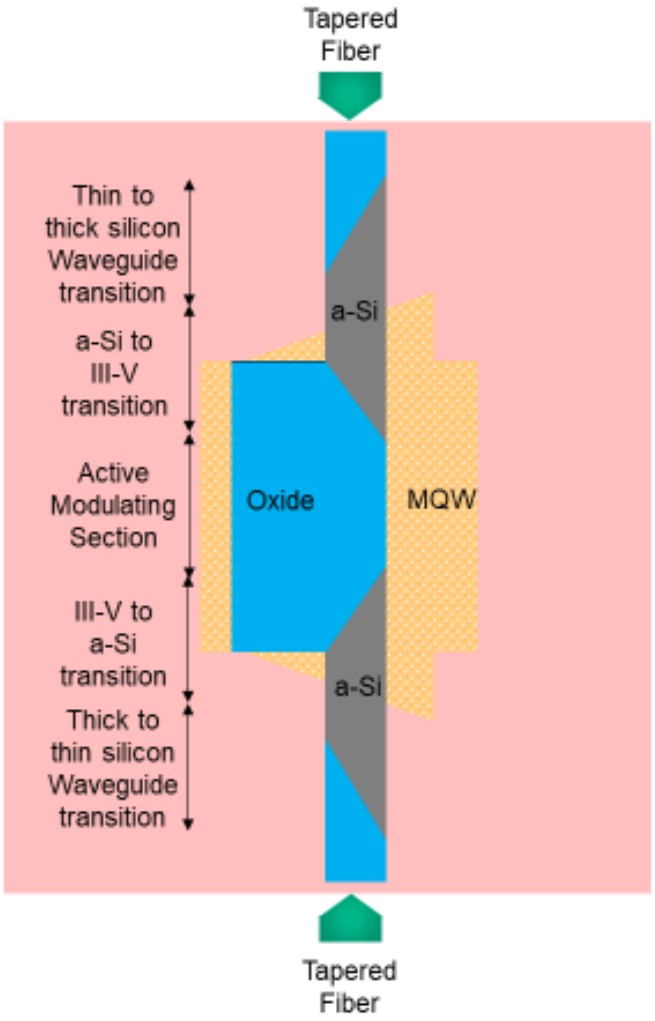


Figure 85 Top View of Overall Transition

6.7 Fabrication Details:

Metal contacts (Ni/Au/Ni 40/30/40nm) were lifted off from the top InGaAs surface. Before evaporating the metals, native oxide was removed using HCL:DI:1:20 wet etching for 30 seconds. Contacts are thin at this step to reduce stress issues after silicon deposition. After the lift off, InGaAs was wet etched (H_3PO_4:H_2O_2:H_2O:5:5:190) using metal as the hard mask. InGaAs wet etching is selective to InP. Before depositing the silicon stack, n-InP surface was wet cleaned with NH_4OH for 30 seconds to remove native oxide. Failure to do this step results

in a-Si film buckling from the surface. Alternate stacks of silicon and oxide were grown using PECVD at 250C. PECVD chamber was cleaned using SF_6 plasma for 45 minutes before each layer deposition. Cross sectional view of processing steps is shown in Figure 86 ,13 and 14.

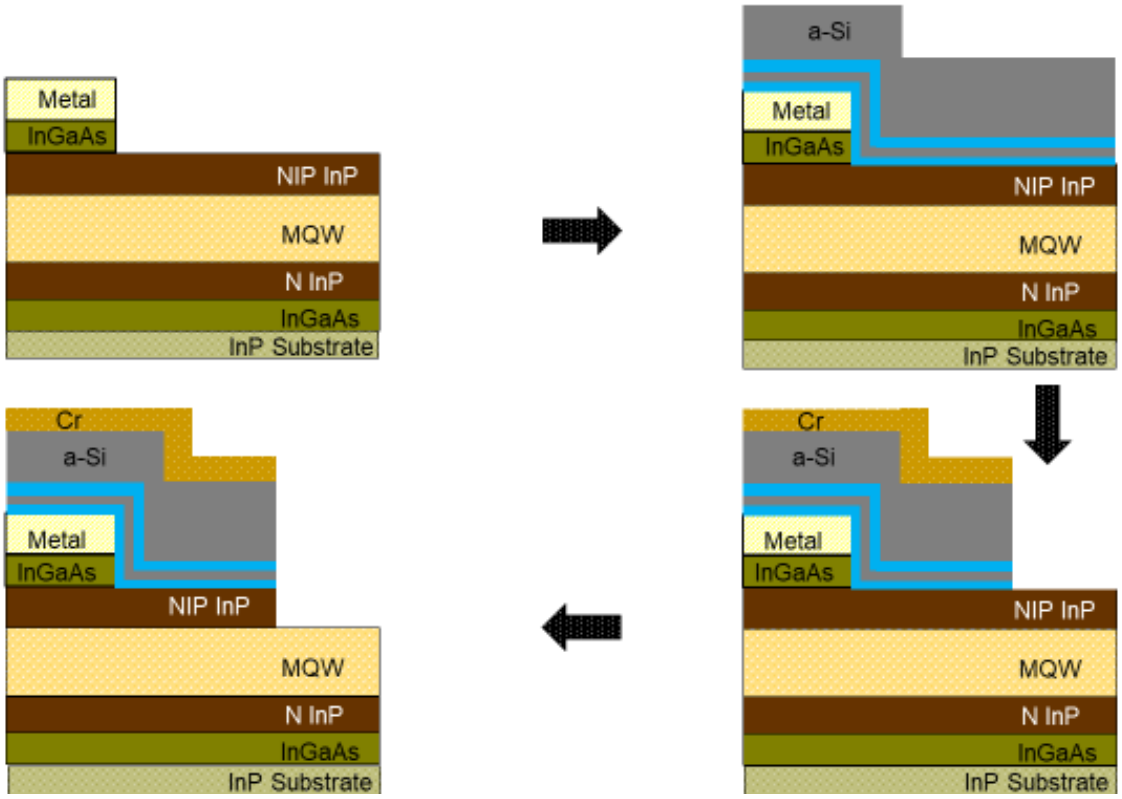


Figure 86 Cross sectional view of device fabrication

One edge of staircase waveguide was defined using chrome hard mask. 60nm chrome was evaporated and patterned using photo resists as hard mask. Cl_2/O_2 plasma was used to etch chrome and stop on amorphous silicon. After removing the photo resist using acetone, silicon stack is etched in CF_4/CHF_3 plasma using chrome hard mask and stop on InP. To define taper tip, patterns were designed such that it cuts the chrome hard mask. Taper formation steps are shown in Figure 87. First row represents the top view and second row represents the cross-sectional view. Only one half of the transition is shown.

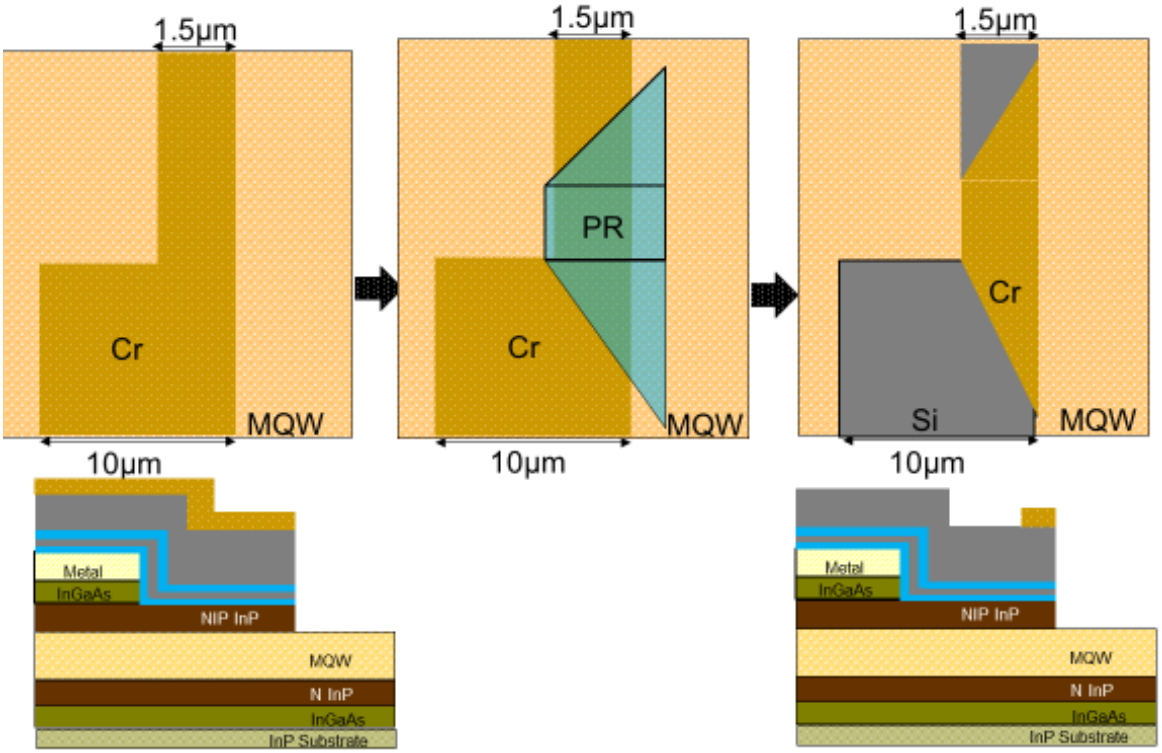


Figure 87 Taper tip formation

Absolute resolution limit of the stepper in our clean room is 400nm and defining the taper by this way helps in overcoming it. While etching the chrome at this step, it doesn't damage the InP surface significantly. NIP InP is then etched using $CH_4/H_2/Ar$ plasma. Etch stops on InAlAs. To etch the silicon taper, sidewall of deeply etched silicon stack was passivated with 350 nm oxide. CF_4/CHF_3 plasma is physical in nature and doesn't etch from sideways. Oxide passivation helps in protecting the sidewall of thin silicon waveguide from getting damaged. Taper etch was timed and stopped on buffer oxide layer. After this step, entire silicon stack will be defined only in transition regions. Y branches would be made of remaining thin silicon. Thus, in a single lithography, both the transitions would be defined, and process becomes completely self-aligned. After etching the chrome hard mask, mesa was etched to define alignment marks for backside processing. Mesa was etched all the way down till 400 nm InP etch stop layers. After passivating the n-InP with 200nm oxide, contacts on

top of n-InGaAs were opened and thicker metal pads were lifted off. Epi was bonded on to GaAs SI transfer substrate using BCB as bonding material. InP substrate was etched using HCL:DI(3:1) for 60 minutes. Etch stop layers were removed subsequently and stopped on 400nm n-InGaAs.

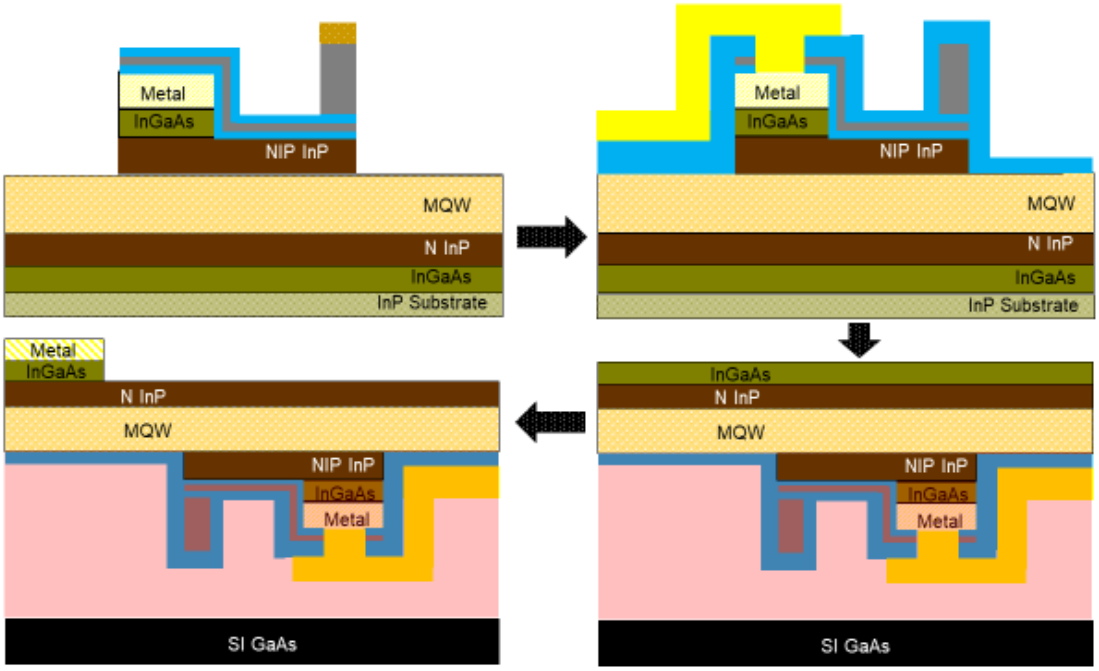


Figure 88 Cross sectional view of device fabrication-continued

Non-alloyed ohmic Contacts (Ni/Au/Ni 30/220/35nm) were made on InGaAs. Other side of the staircase waveguide was etched using an oxide hard mask. To convert the hybrid silicon mode into the silicon mode, MQW section and bottom NIP InP was tapered in such a way it crosses the buried silicon waveguide. Both MQW and InP was wet etched. This step also opens the buried contacts processed on the front side. Finally, photo BCB was lithography defined and opened where the contacts were buried.

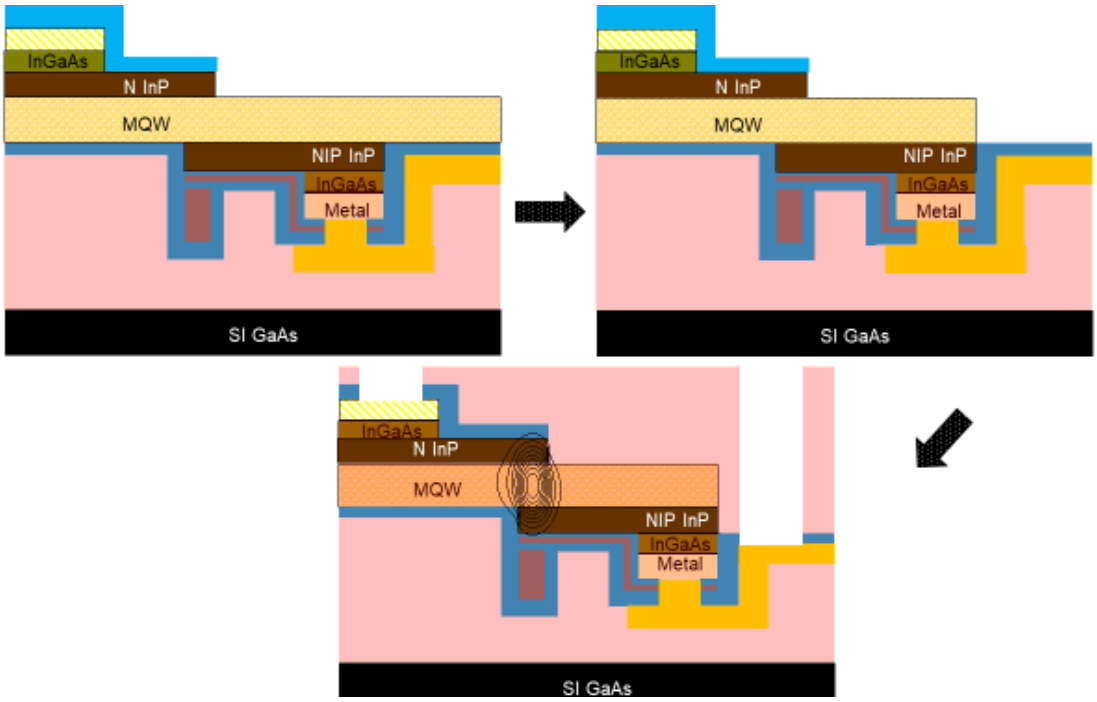


Figure 89 Cross sectional view of device fabrication-continued

6.8 aSi Deposition and Optical Loss Characterization:

Amorphous Silicon was deposited using Vision 310 Advanced Vacuum PECVD using a 2% SiH_4 source. An oxide layer is necessary to improve the adhesion of the silicon film grown. Because of the vertical coupling between III-V and a-Si waveguide, taper length depends upon the thickness of this oxide layer. Adhesion was further improved by removing the native oxide on InP surface using NH_4OH dip for 40 seconds before the oxide deposition. Stress in amorphous silicon is usually compressive in nature. There is a maximum film thickness above which amorphous silicon buckles up from the surface. Deposition parameters were 2% SiH_4 1580 sccm, 30W and 580 mt.

ICP etching of silicon and oxide involves fluorine containing gases. CF_4/CHF_3 plasma has a selectivity more than 30 with respect to InP and GaAs surfaces while it sputters InAlAs. InP could be etched using $CH_4/H_2/Ar$ (MHA) plasma. Simultaneous deposition and etching of polymer on sidewall and planar surface respectively ensure very vertical side wall angle

using MHA. Polymer deposition on InAlAs surface is much higher than other InP surfaces and hence the etch stops. Metal masks such as chrome has selectivity more than 25 with respect to silicon etching. Chrome can be etched using low power Cl_2/O_2 plasma and stop on silicon. Low temperature deposition, process compatibility and high etch selectivity across different materials makes amorphous silicon a promising solution for passive section alternative.

To check the optical loss @1.55 μm, amorphous silicon was deposited on s doped InP substrate and a rib waveguide was etched. Two sets of alternating layers of oxide and silicon with thickness of 55 nm, 40 nm, 55 nm and 440 nm were deposited. 0.8 μm wide rib waveguide with 60 nm etch depth was etched. Waveguide was etched shallow to have maximum modal overlap within the amorphous silicon and minimize the scattering loss. SEM of the cleaved optical facet and simulated mode profile is shown in Figure 90and Figure 91 respectively.

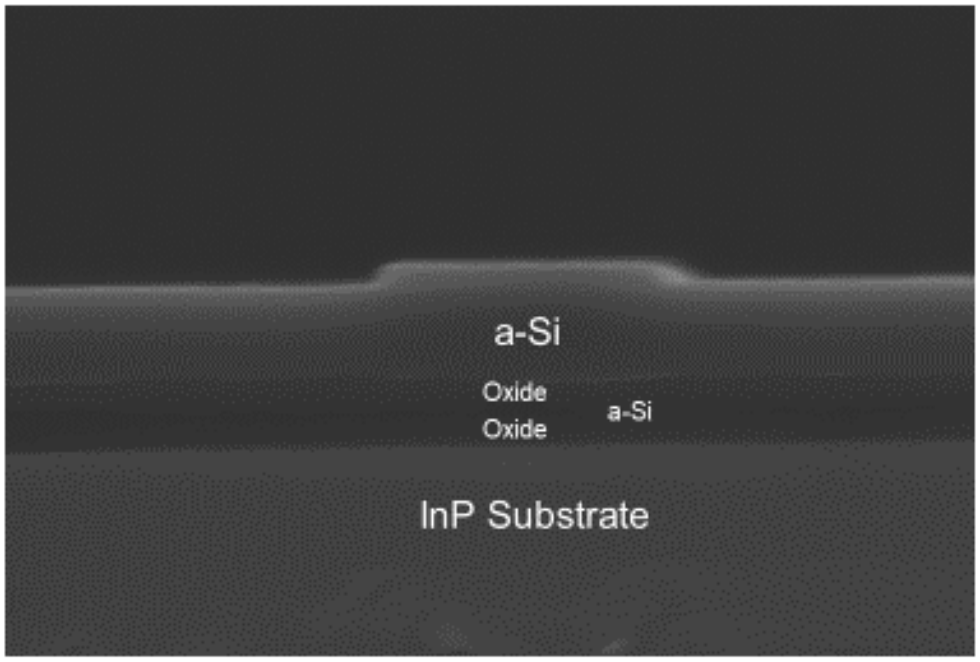


Figure 90 SEM of cleaved facet of a-Si rib waveguide on InP Substrate

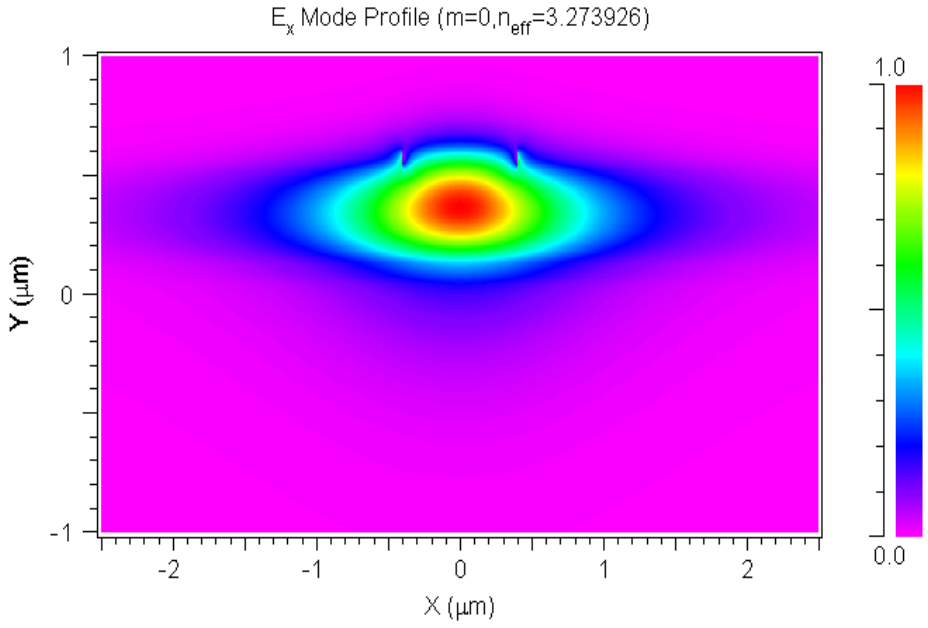


Figure 91 Simulated mode profile

Waveguides were excited by 2.5 μm spot size fiber. For a input power of 1.1 mW, total insertion loss was 17.29 dB. Propagation loss was calculated by sweeping the wavelength. From the fringe visibility across different dies, propagation loss is estimated to be under a dB/cm. Fabry- perot measurement data is shown in Figure 92. Out of 17.29 dB insertion loss, most of the loss was due to modal mismatch. Loss data confirmed that amorphous silicon deposited had low optical loss @1.55 μm.

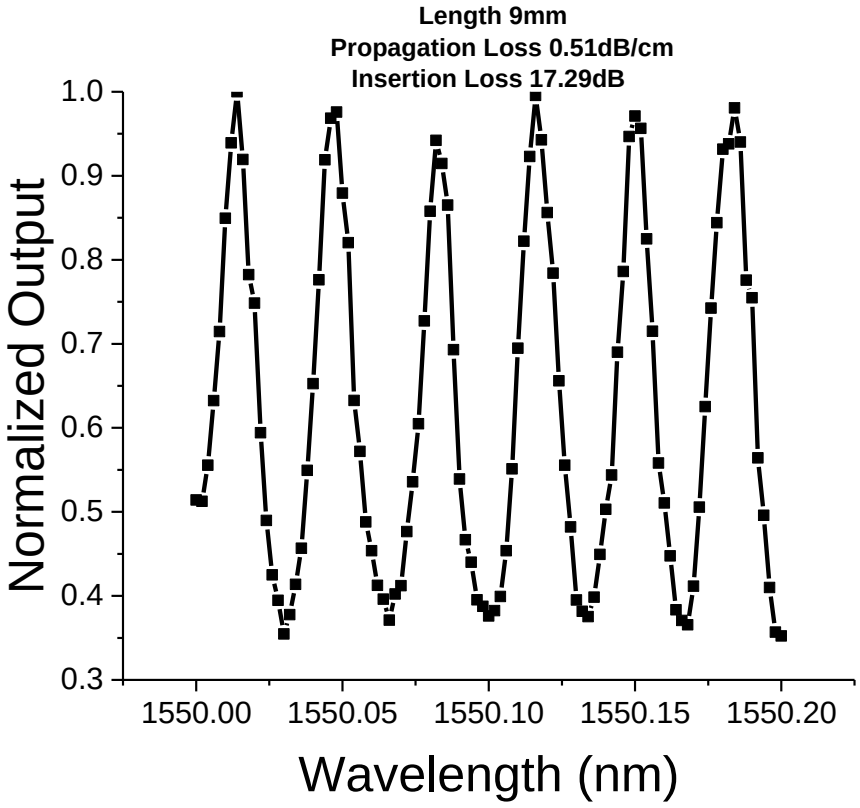
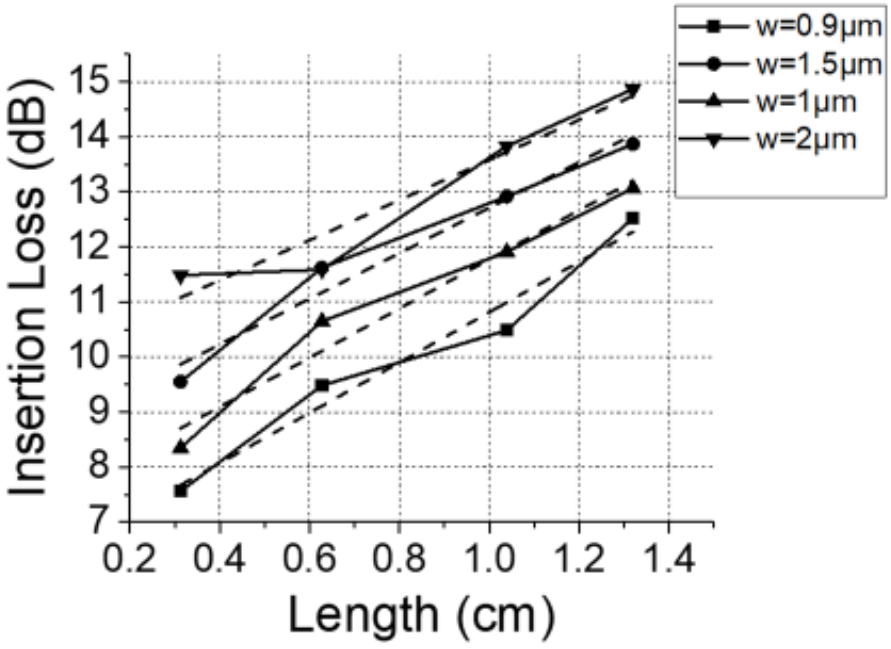


Figure 92 Fabry perot measurement

To check the coupling loss of thin silicon waveguide, 38 nm a-Si was deposited on InP substrate with 3 μm bottom oxide. Thick bottom oxide was deposited on InP substrate to prevent optical mode leaking into substrate. 38nm thick a-Si was deposited and patterned using photoresist mask. BCB was not used since a-Si deposited on BCB had some stress issues

in that past. Using oxide as cladding will increase the optical confinement slightly. After etching a-Si in ICP, photo resist was stripped using acetone and top oxide cladding (~2 μm) was again deposited using PECVD. Because of its low effective index, cut back method was used to measure the propagation and the coupling loss with a 5 μm spot size fiber.



Width (μm)	Propagation Loss (dB/cm)	Coupling Loss (dB)/facet
0.9	4.56	3.12
1	4.46	3.65
1.5	4.14	4.29
2	3.64	4.97

Figure 93 Coupling loss of thin silicon waveguide by cut back measurement

Various widths were tested. Coupling and propagation loss values are shown in Figure 93. As the width increase, propagation loss decreases and coupling loss increases. Coupling loss for a 0.9 μm width was around 3 dB/ facet. Its further possible to improve the coupling loss by decreasing the width of the waveguide and exciting with smaller spot size tapered

fiber. Width of 1.5 μm with 4.1 dB/cm propagation loss could be used in y branches and narrower widths could be used near the facet to reduce coupling loss. Challenge on depositing thick bottom cladding limits decreasing the width of the waveguide.

6.9 Results

MZMs were cleaved at both ends and excited by a 2.5 μm spot size fiber at the input. Optical output was measured using an InGaAs photodetector after a 20x microscope objective lens. Sinusoidal signal and a bias were applied such that the *pin* diode with MQW core is reverse biased. The transfer function of the MZM under single arm drive is shown in Figure 94. V_π for 3 mm long electrode was 1.1 V under 4 V bias, which indicates 0.55 V V_π under push pull operation. Device had tapers on both input and output side. Near the facet, thin silicon waveguide width was 1.5 μm. Thin silicon was tapered from 1.5 μm to 0.8 μm near the facet. But, because of issues with bonding, there were air bubbles leading to void and patterns collapsing near the facet which led to the cleaving of the sample to protect the rest of the device. Picture of sample with BCB void is shown in Figure 95. Air bubbles were also an issue in the device section which led to only single arm measurement. Width of the staircase waveguide as measured from SEM was 0.8 μm. Widths varied between 0.8 to 1.1 μm across the dies.

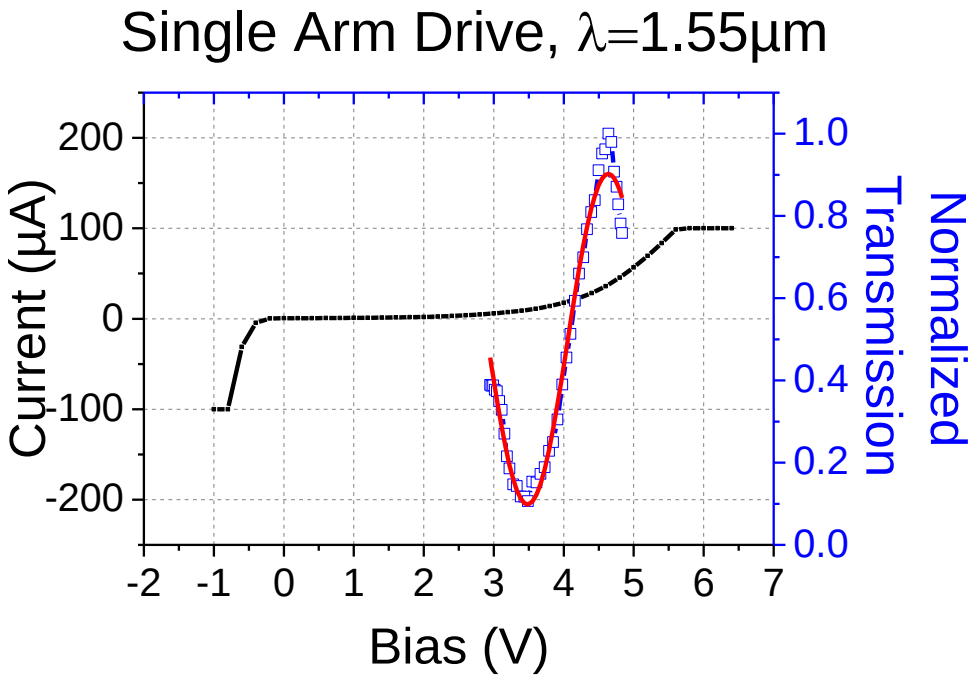


Figure 94 Single arm measurement of MZM

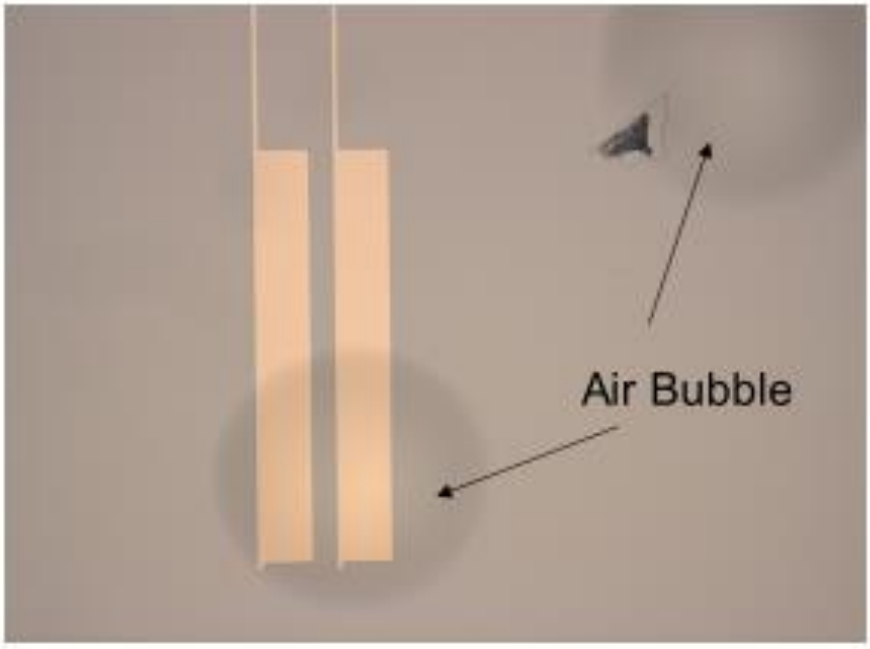


Figure 95 Air bubble after substrate removal

6.9.1 Taper Measurements

Propagation loss of thin silicon waveguide was measured using fabry-perot method. Its effective index was around 1.68 which resulted in reflection suitable for measurement. Cut back method wasn't used since it will destroy the active modulator. Measured data is shown in

Figure 96. From the fringe visibility, propagation loss was estimated to be 7 dB/cm. Loss value was higher than what was quoted in Figure 93. Reason for higher loss is because of the procedure by which these thin silicon waveguides were fabricated. In Figure 93, waveguide was fabricated in a single step. However, during complete device fabrication, thin silicon waveguide is defined after removing the 380 nm silicon layer. A chrome mask was used to define the taper and etch 380 nm silicon and stop on 50 nm oxide layer. In this process, bottom 40 nm silicon sidewall is exposed to ICP etch twice leading to slightly increased propagation loss.

First, transition loss between thin silicon waveguide to composite thick silicon waveguide was characterized. To measure this loss, two structures were defined as shown in Figure 97. Structure 1 is straight passive waveguide made of 40 nm thick a-Si and 1.5 μm width. Structure 2 is like structure 1 except that it has transitions to composite thick silicon waveguide.

In structure 2, there is a 50 μm straight section of composite thick waveguide. By calculating the difference between the insertion loss of two structures, it is possible to get the transition loss assuming the structures have the same coupling loss.

$$IL_1 - IL_2 = 2\alpha_T + \alpha_{Si}$$

$$IL_1 - \text{Total Insertion Loss of structure 1}$$
$$IL_2 - \text{Total Insertion Loss of structure 2}$$
$$\alpha_T - \text{Loss per transition}$$

α_{Si} – Propagation loss of 50µm straigt section

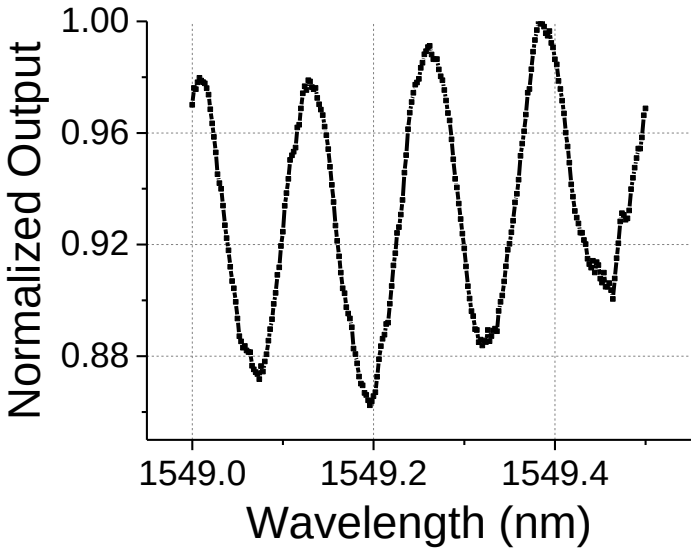


Figure 96 Thin Silicon waveguide propagation loss measurement

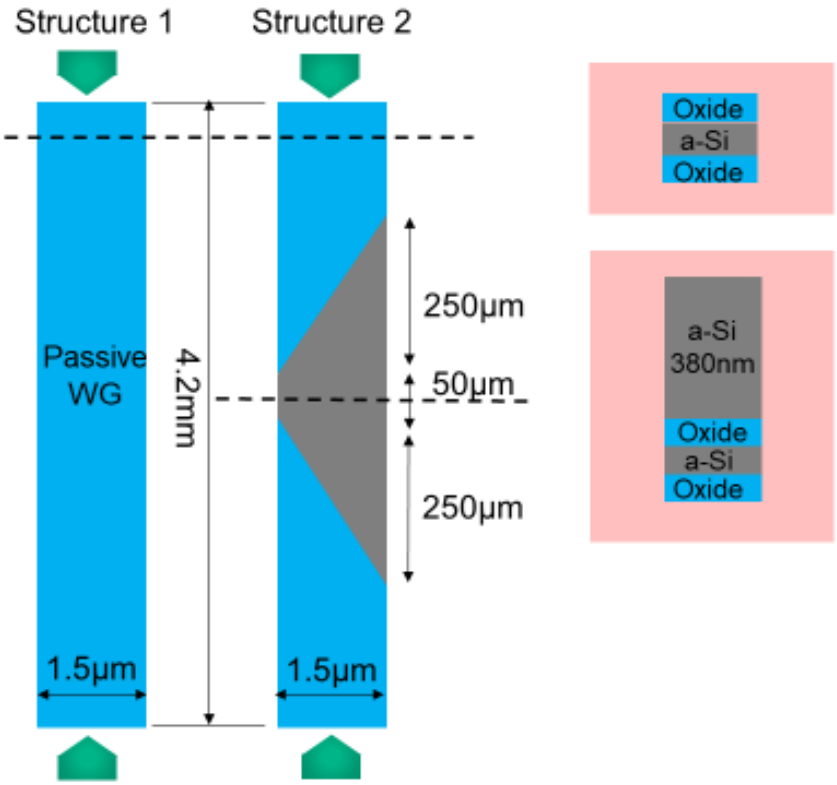


Figure 97 Transition loss test structures. Top view on left and cross-sectional view on right

The total insertion loss of structure 1 was 11 dB and that of structure 2 was 11.8 dB. Neglecting the propagation loss of the 50 μm straight section, loss per transition was 0.4 dB. Propagation loss of straight passive section in structure 1 was measured to be 7 dB/cm using fabry-perot measurement. So out of 11 dB insertion loss from structure 1, 2.94 dB comes from propagation loss and remaining 8 dB accounts for the coupling loss.

Propagation loss of staircase waveguide was also measured using fabry-perot method and measured data for 4.2 mm phase modulator without transitions is shown in Figure 98. From the fringe visibility, propagation loss is estimated to be around 17.6 dB/cm. Total insertion loss was 31.1 dB which leads to a coupling loss of 11.8 dB/facet. Active device length in modulator was 3 mm which corresponds to an on-chip propagation loss 5.28 dB. Out of 17.6 dB/cm, loss associated with overlap of optical mode with p doped layer is around 4.5 dB/cm calculated from simulation. The propagation loss of staircase waveguide was higher than expected because of the misalignment after substrate removal. After bonding and substrate removal, surface is not flat as one would expect. BCB curing leads to wafer bow. Because of that, alignment marks no longer appear to be at the position as defined in the mask plate which resulted in misalignment. Having even more tolerance while designing the mask would help to reduce the loss due to overlap with metal contacts. For high speed modulator design, placing metal contacts far away from optical mode would result in increased microwave loss and so there is a tradeoff while designing the metal contacts distance. SEM of cleaved facet is shown in Figure 99.

Transition loss between III-V and silicon waveguide was measured by exciting a 1 mm phase modulator with transitions at both input and output sides. Having known the propagation losses of individual waveguides and their lengths, transition loss could be

estimated by calculating the difference from the overall insertion loss. Top view of the test structure with corresponding loss numbers is shown in Figure 101.

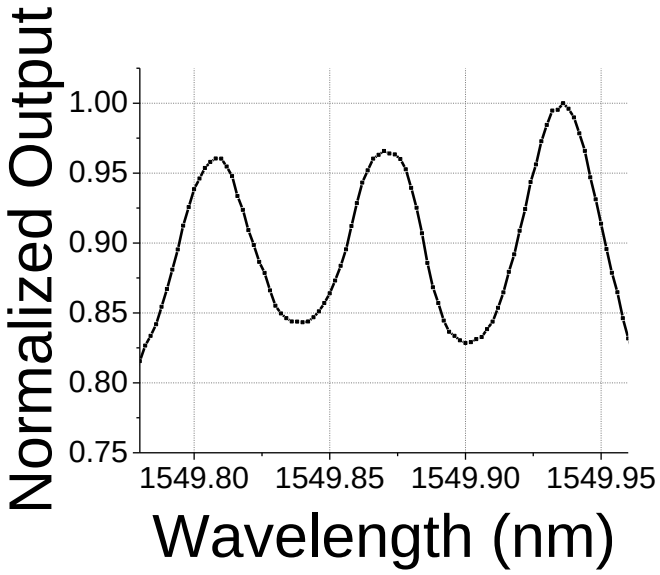


Figure 98 Staircase waveguide loss measurement

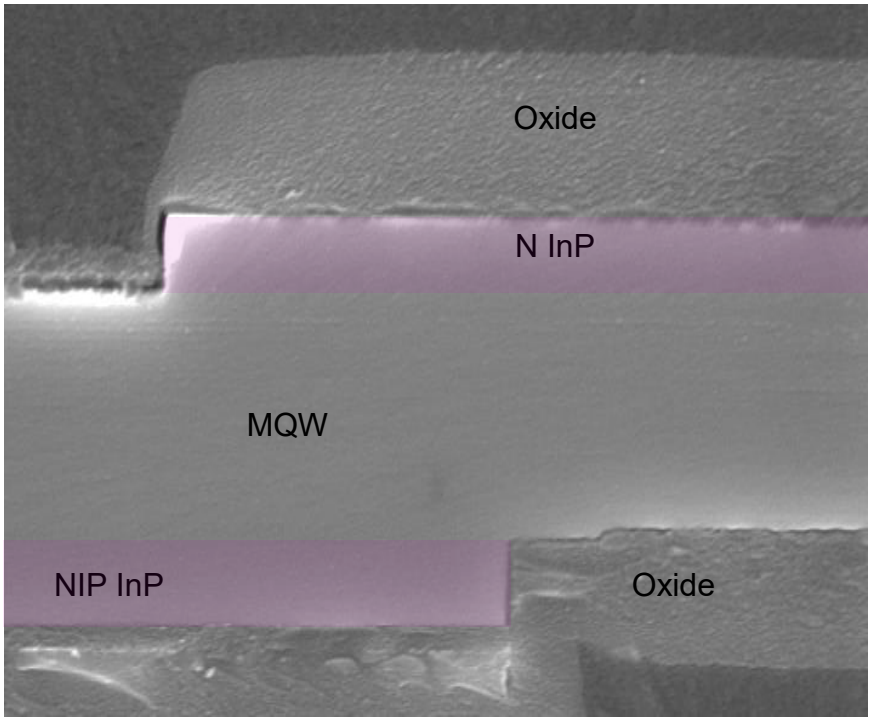
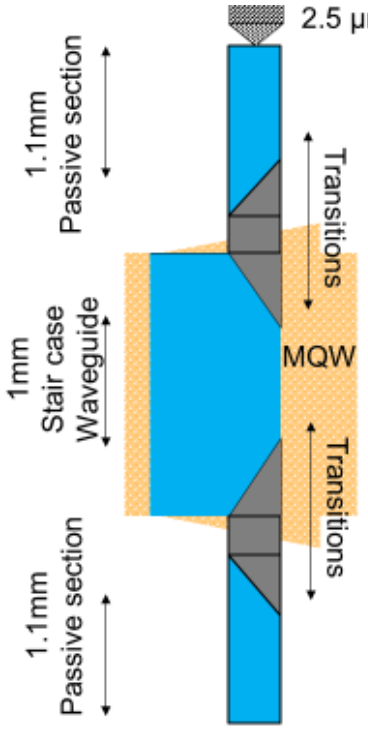


Figure 99 SEM of stair case waveguide cleaved facet



	Loss (dB)
Insertion Loss	18.2
Thin Silicon straight section	1.45
Coupling Loss	7.4
Thick to Thin Silicon transition	0.85
III-V Straight section	1.85
III-V to Silicon Taper	3.3dB/transition

Figure 101 Test structure for III-V to silicon transition loss measurement. Top view on left and loss split up on right.

From the overall insertion loss measurement of 18.2 dB, transition loss was estimated to be 3.3 dB/ transition. MQW taper (Section 2) as discussed in Figure 82 was performed using wet etching after substrate removal. This step should be replaced with an ICP dry etching to improve on the loss. With processing improvements, this number could be further cut down to 2 dB/transition.

6.10 Summary

New way of active passive integration of low loss a-Si waveguides and substrate removed III-V waveguides in electro-optic modulator applications was developed and fabricated. This approach eliminates fabrication of precise tapers in III-V material, additional loss due to III-V waveguides in passive parts of the device and provides electrical isolation between the arms of the interferometer. a-Si could be deposited on wide variety of surfaces using PECVD which would also enable active passive integration in other material systems. Its refractive index could be easily tuned from 3 to 3.7 by varying the deposition parameters which increases design flexibility across different systems. Required tapers are defined in a-Si waveguides. Furthermore, thin a-Si waveguides could provide low loss coupling to fibers. MZM with 0.165 V-cm efficiency under push pull was demonstrated. Preliminary results indicate more than 95 % simulation efficiency and 3.5±0.2 dB fabricated transition loss, which is expected to improve with processing adjustments.

6.11 References

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3. Zhu, S., G.Q. Lo, and D.L. Kwong, *Low-loss amorphous silicon wire waveguide for integrated photonics: effect of fabrication process and the thermal stability.* Optics Express, 2010. **18**(24): p. 25283-25291.
4. Dogru, S., J.H. Shin, and N. Dagli, *Traveling Wave Electrodes for Substrate Removed Electro-Optic Modulators With Buried Doped Semiconductor Electrodes.* IEEE Journal of Quantum Electronics, 2013. **49**(7): p. 599-606.

1 Appendix

GaAs on Silicon Modulator (Chapter 2- Fabrication Details)

Mask Plate: DCASMZM3A, DCASMZM3B

Stepper Ppt file: DCASMZM3_mask_layout_UCSB_Nak_Ki_Kim

Ledit file name: DCASMZM3

Step 1: Waveguide Metal

a) Stepper Lithography
   - Spin LOL 2000-1000rpm, 45s
   - Soft bake : hotplate, 170C, 2min
   - Spin LOL 1000rpm, 45s
   - Soft bake : hotplate, 170C, 2min
   - Spin LOL 1000rpm, 45s
   - Soft bake : hotplate, 170C, 2 min
   - Spin LOL 1000rpm, 45s
   - Soft bake : hotplate, 170C, 5 min
   - Spin SPR0.9-3000rpm
   - Soft bake : hotplate, 95C, 60s
   - Expose sample: 0.35s, focus offset: 0
   - Post bake: hotplate, 110C, 60s
   - Develop : AZ300 MIF, 60s / DI rinse, 3min / blow dry
   - No Descum

b) Ebeam Evaporation
   - Native oxide etch: HCL:DI:1:10, 1 min / DI rinse, 3min / blow dry
   - Evaporate : Ni/Ge/Au/Ni/Au (5/18/132/20/900 nm)
   - Metal liftoff in AZ NMP : Overnight

Step 2: Waveguide etching

a) PECVD Oxide
   - 30 min Std clean
   - 450nm oxide deposition

b) Stepper Lithography
   - Spin HMDS : 3000rpm, 30s
   - Spin SPR220-3 : 2500rpm, 30s
   - Soft bake : hotplate, 115 C, 90s
   - Expose: 0.72s, focus offset:0
   - Post bake: hotplate, 115 C, 90s
   - Develop : AZ300MIF, 60s / DI rinse, 3min / blow dry
   - Inspect pattern under microscope

c) Oxide Etch-ICP2

- CF4/CHF3 30/10
- 900/50 W, 0.5Pa
- Remove PR
- Descum 1 minute

d) GaAs Etch-ICP2
- Cl2/N2 27/10 sccm, 0.2 Pa
- 900/75 W,
- 1’35” etch
- Rinse in Water immediately after chlorine etch
- Descum 1 minute

e) PECVD Nitride
- 30 min Std clean
- 40nm nitride deposition

Step 3: Mesa Etching

a) Stepper Lithography
- Spin HMDS : 3000rpm, 30s
- Spin SPR220-3 : 2500rpm, 30s
- Soft bake : hotplate, 115 C, 90s
- Expose: 0.72s, focus offset:0
- Post bake: hotplate, 115 C, 90s
- Develop : AZ300MIF, 60s / DI rinse, 3min / blow dry
- Inspect pattern under microscope

b) Nitride Etch-ICP2
- CF4/CHF3 30/10
- 900/50 W, 0.5Pa
- 30 seconds etch

c) GaAs Etch-ICP2
- Cl2/N2 15/10 sccm, 0.2 Pa
- 900/75 W,
- 2’10” etch
- Rinse in Water immediately after chlorine etch

d) Wet etching
- BHF- 25 seconds
- Strip PR- Acetone

e) PECVD Nitride
- 30 min Std clean
- 40nm nitride deposition

Step 4: Bottom GaAs Metal Pad

a) Stepper Lithography
- Dehydrate @ 200 C for 5 minutes before spinning SF
- Spin SF11 : 2000rpm, 30s
- Soft bake : hotplate, 200C, 2 min
- Spin SPR220-3 2500rpm

- Soft bake : hotplate, 115C, 90s
- Expose sample: 0.72s, focus offset: 0
- No Post bake with thick SF
- Develop : AZ300 MIF, 60s / DI rinse, 3min / blow dry
- Expose and develop SF using SAL 101
- Descum: O2 plasma, 300mTorr / 100W, 30s

b) Ebeam Evaporation
- BHF 90 seconds
- Evaporate : Ni/Ge/Au/Ni/Au (5/18/132/20/900 nm)
- Metal liftoff in AZ NMP : Overnight

Step 5: Annealing

a) RTA 430C, 30 seconds, FG
- Check the contacts

Step 6: Implant

a) Stepper Lithography
- Spin SF11-2000 rpm
- Soft bake : hotplate, 200C, 2'
- Spin AZ4620-2500 RPM
- Soft bake : hotplate, 95C, 95"
- Expose sample: 1.8s, focus offset: -4
- Develop : AZ400 1:4 60s / DI rinse, 3min / blow dry
- Descum: O2 plasma, 300mTorr / 100W, 30s
- PR Stripping AZ NMP: 4 hours

Step 7: Bottom GaAs Isolation

a) Stepper Lithography
- Spin HMDS : 3000rpm, 30s
- Spin SPR220-3 : 2500rpm, 30s
- Soft bake : hotplate, 115 C, 90s
- Expose: 0.82s, focus offset:0
- Post bake: hotplate, 115 C, 90s
- Develop : AZ300MIF, 60s / DI rinse, 3min / blow dry
- Inspect pattern under microscope

b) Wet etching
- BHF- 1 minute

c) GaAs Etch-ICP2
- Cl2/N2 15/10 sccm, 0.2 Pa
- 900/75 W,
- 45" etch
- Rinse in Water immediately after chlorine etch
- Strip PR-acetone

Step 8: BCB planarization and blanket etch

a) Spin BCB @1000 rpm

- Blue Oven, Overnight cure, Recipe 7

b) BCB blanket Etch-ICP2
   - CF4/CHF3 30/10
   - 900/50 W, 0.5Pa
   - ~130-140 nm/min etch rate
   - Etch until top metal is reached

Step 9: N-metal Pad

a) Stepper Lithography
   - Dehydrate @ 200 C for 5 minutes before spinning SF
   - Spin SF11 : 2000rpm, 30s
   - Soft bake : hotplate, 200C, 2 min
   - Spin SPR220-3 2500rpm
   - Soft bake : hotplate, 115C, 90s
   - Expose sample: 0.72s, focus offset: 0
   - No Post bake with thick SF
   - Develop : AZ300 MIF, 60s / DI rinse, 3min / blow dry
   - Expose and develop SF using SAL 101
   - Descum: O2 plasma, 300mTorr / 100W, 30s

b) Ebeam Evaporation-Ebeam 3
   - Evaporate : Ni/Au(50/500 nm)
   - Metal liftoff in AZ NMP : Overnight

Step 10: BCB Opening

a) Stepper Lithography
   - Spin AZ4620-4000 RPM
   - Soft bake : hotplate, 95C, 95s
   - Expose sample: 1.7s, focus offset: -4
   - Develop : AZ400 1:4 60s / DI rinse, 3min / blow dry
   - Descum: O2 plasma, 300mTorr / 100W, 30s

b) BCB blanket Etch-ICP2
   - CF4/CHF3 30/10
   - 900/50 W, 0.5Pa
   - Etch until bottom metal is reached
   - Strip PR

Microstrip Fabrication (Chapter 3 -Fabrication Details)

Mask Plate: Plated-Microstrip

Stepper Ppt file: microstrip_stepper

Ledit file name: microstrip_sep2018

Step 1: Seed Metal Blanket Deposition

c) PECVD Oxide
    - 30 min Std clean
    - 40 nm oxide deposition
d) Ebeam-4 Evaporation
    - Evaporate: Cr/Au 25nm /25 nm
    - Don't use sputtering for seed metal. Gold wet etchant etches sputtered gold very slow

Step 2: Ground Electrode Plating

f) Stepper Lithography
    - No HMDS
    - Spin AZP 4620 : 4000rpm, 30s
    - Soft bake : hotplate, 95 C, 95s
    - Expose: 1.7s, focus offset:0
    - No Post bake
    - Develop : AZ400MIF:DI (1:4), 60s / DI rinse, 3min / blow dry
    - Inspect pattern under microscope
    - Using cotton swab with acetone, clean the photoresist near the edges for plating contacts
    - Using a similar size sample, calibrate the plating rate
    - Plate to get 2 μm thickness
    - Strip the photo resist using acetone

Step 3: Thick Metal post Plating

f) Stepper Lithography
    - No HMDS
    - Spin AZP 4620 : 4000rpm, 30s
    - Soft bake : hotplate, 80 C, 60s
    - Spin AZP 4620 : 4000rpm, 30s
    - Soft bake : hotplate, 95 C, 95s
    - Expose: 5s, focus offset:0
    - Develop : AZ400MIF:DI (1:4), 60s / DI rinse, 3min / blow dry
    - Inspect pattern under microscope
    - Using cotton swab, clean the photoresist near the edges for plating contacts
    - Using a similar size sample, calibrate the plating rate
    - Plate to get 19 μm thickness
    - Strip the photo resist using acetone

g) Seed layer removal
    - Use gold wet etchant to etch gold for 5 seconds. Etch stops on gold.
    - Use chrome wet etchant to etch chrome for 5 seconds.
    - 30 seconds etch

Step 4: BCB planarization and blanket etch

c) PECVD-2 Nitride @ 300 C
    - 150 nm Nitride deposition
    - Gold doesn't stick well with nitride deposited using PECVD 1

d) Spin BCB @1000 rpm for 3 times. First two schedules were soft cured @ 210 C
    - Blue Oven, Overnight cure, Recipe 7

e) BCB blanket Etch-ICP2
    - CF4/CHF3 30/10
    - 900/50 W, 0.5Pa
    - Etch until top metal is reached

Step 5: Signal metal Pad

c) Stepper Lithography
    - Dehydrate @ 200 C for 5 minutes before spinning SF
    - Spin SF15 : 4000rpm, 30s
    - Soft bake : hotplate, 200C, 2 min
    - Spin SPR-0.9 3000rpm
    - Soft bake : hotplate, 95C, 60s
    - Expose sample: 0.35s, focus offset: 0
    - No Post bake with thick SF
    - Develop : AZ300 MIF, 60s / DI rinse, 3min / blow dry
    - Expose and develop SF using SAL 101
    - Descum: O2 plasma, 300mTorr / 100W, 30s

d) Ebeam Evaporation-Ebeam 4
    - Evaporate : Ni/Au(50/1300 nm)
    - Don't use Ti on BCB. It doesn't stick good on BCB
    - Metal liftoff in AZ NMP : Overnight