UNIVERSITY OF CALIFORNIA, SAN DIEGO

Characterization and Modeling of III-V MOS Capacitors: Interface States and Bulk Oxide Traps

A dissertation submitted in partial satisfaction of

the requirements for the degree Doctor of Philosophy

in

Electrical Engineering (Nanoscale Devices and Systems)

by

Han-Ping Chen

Committee in charge:

Professor Yuan Taur, Chair
Professor Jie Xiang, Co-Chair
Professor Peter Asbeck
Professor Chung-Kuan Cheng
Professor Andrew Kummel

2014

The dissertation of Han-Ping Chen is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Co-Chair

_____

Chair

University of California, San Diego

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Dedication

This dissertation is dedicated to my family.

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The text of Chapter 4, in part, is a reprint of the material as it appears in "On the effect and extraction of series resistance in Al_2O_3-InGaAs MOS with bulk-oxide trap" by Bo Yu, Yu Yuan, Han-Ping Chen, and Yuan Taur, Electronics Letter, Mar., 2013. The dissertation author was a co-author of this paper.

The text of Chapter 5, in part, is a reprint of the material as it appears in "Effects of Oxide Thickness and Temperature on Dispersions in InGaAs MOS C-V Characteristics" by Han-Ping Chen, Jaesoo Ahn, Paul C. McIntyre, and Yuan Taur, Journal of Vacuum Science & Technology B, Mar., 2014. The dissertation author was the primary investigator and author of this paper.

The text of Chapter 6, in part, is a reprint of the material as it appears in "Modeling illumination effects on n- and p-type InGaAs MOS at room and low temperatures" by Han-Ping Chen, Dmitry Veksler, Gennadi Bersuker, and Yuan Taur, to be published by IEEE Transaction on Electron Devices. The dissertation author was the primary investigator and author of this paper.

VITA

2007	B.S. in Electronics Engineering National Chiao Tung University, Hsinchu, Taiwan
2011	M.S. in Electrical and Computer Engineering University of California, San Diego
2014	Ph.D. in Electrical and Computer Engineering University of California, San Diego

PUBLICATIONS

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ABSTRACT OF THE DISSERTATION

Characterization and Modeling of III-V MOS Capacitors: Interface States and Bulk Oxide Traps

by

Han-Ping Chen

Doctor of Philosophy in Electrical Engineering

University of California, San Diego, 2014

Professor Yuan Taur, Chair

Professor Jie Xiang, Co-Chair

As the Silicon based MOSFET scaling is close to an end, high mobility III-V MOSFET is considered one of the most promising candidates in continuing Moore's Law. By replacing the channel from Silicon to III-V high mobility materials, it is expected that the on-current can be further increased, or the same on-current level can be achieved with decreased V_{DS}, which lowers power consumption. However, the high interface and bulk-

oxide trap densities are still major issues. These two kinds of trap states deteriorate device performance by lowering device on-current, increasing inverse subthreshold slope, and causing hysteresis (history effect). Fabricating high quality dielectric with low defect density on the interface and inside high-*k* dielectric is still a critical challenge which needs to be overcome.

In this dissertation, two trap models are introduced to simulate the MOS capacitor C-V and G-V dispersions: full interface state model and distributed bulk-oxide trap model. One major application of the models is extracting the interface and bulk-oxide trap densities. Therefore, they can be applied to assist the researchers in the field monitoring the results after certain fabrication procedures. Furthermore, the models can be used to interpret the measuring data, such as the linear capacitance dispersion in accumulation region from bulk-oxide traps, the high-low capacitance dispersion in depletion from interface traps, and the C-V humps in n-type InGaAs MOS from depletion to inversion from the combination effect of increasing interface trap densities and majority carrier time constants. Such "know why" is the key of success in all the field of scientific study assisting the "know how" of engineering work.

Furthermore, the insulator thickness effect, temperature effect, and light illumination effect on MOS C-V dispersions are also studied. It is shown that the data in all the conditions can be satisfactorily explained by the frame work of the small signal models with the same trap density. Other trap extraction methods and models, such as Terman method and conductance method for interface traps, and lumped circuit model, including Hasegawa model, for bulk-oxide traps, are also reviewed and commented in the dissertation.

Chapter 1

Introduction

1.1 A Brief Review on the Scaling of CMOS Technology

In the past few decades, the whole IC industry evolution has significantly changed our lives owing to the success of CMOS scaling. From personal computer (PC) with microprocessor chip to mobile devices with SoC, the very-large-scale-integration (VLSI) technology has been driven by the scaling of MOSFET, which provides higher circuit density, higher computing speed, and lower power consumption. Since early 70's, such scaling has followed the famous "Moore's Law" that the number of transistor on a chip

doubles every two years [1]. Figure 1.1 shows the technology trend for microprocessor unit (MPU) functions per chip versus the Moore's Law from International Technology Roadmap for Semiconductor (ITRS) 2011 [2]. The success of the Moore's Law is clearly presented, and it is very likely to continue in the near future.

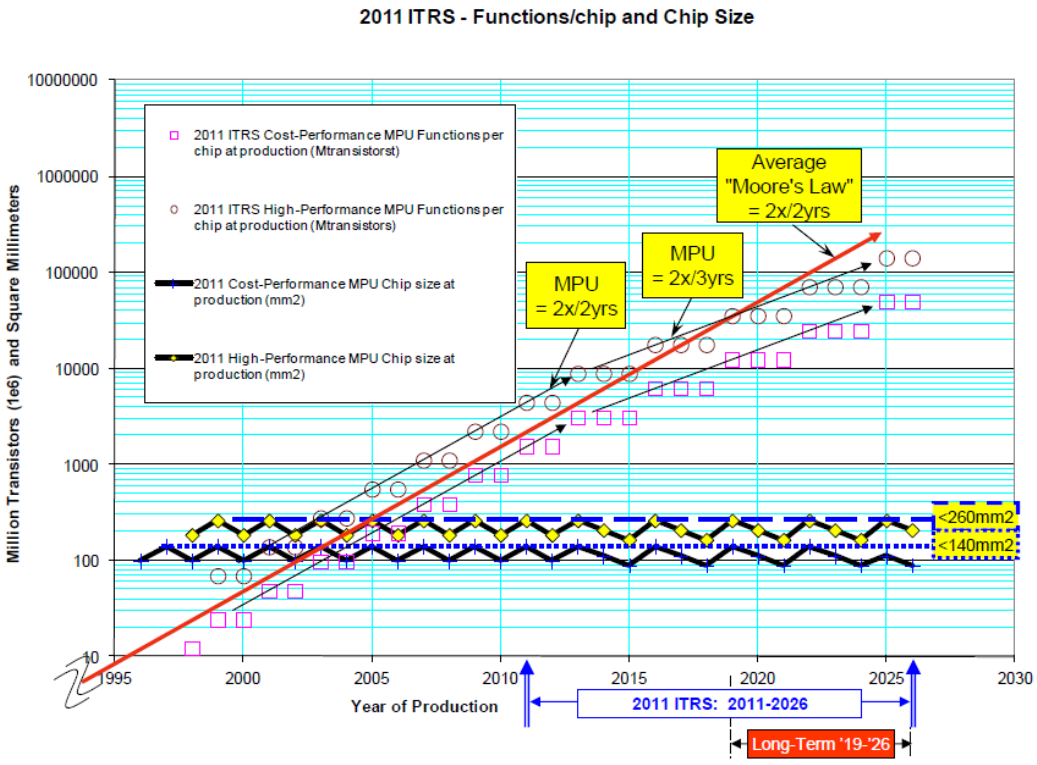

Figure 1.1: 2011 ITRS roadmap on MPU functions per chip comparing to the average of "Moore's Law" [2].

The traditional MOSFET scaling described by Dennard [3], namely scaling by shrinking the channel length, the oxide thickness and the supply voltage, had gradually ended in the early 2000s. In Intel 90 nm process node (Fig. 1.2), the SiO_2 layer thickness is only 1.2 nm, which causes severe oxide leakage, and the oxide thickness could not be further scaled down. The technology was still able to improve because of the

development of strained Silicon technology [4-7], such as the compressive strain from SiGe S/D in PMOS and the tensile strain from SiN cap layer in NMOS, which increase the mobility of silicon channel and device performance. The loss from the non-scaling oxide thickness was then compensated.

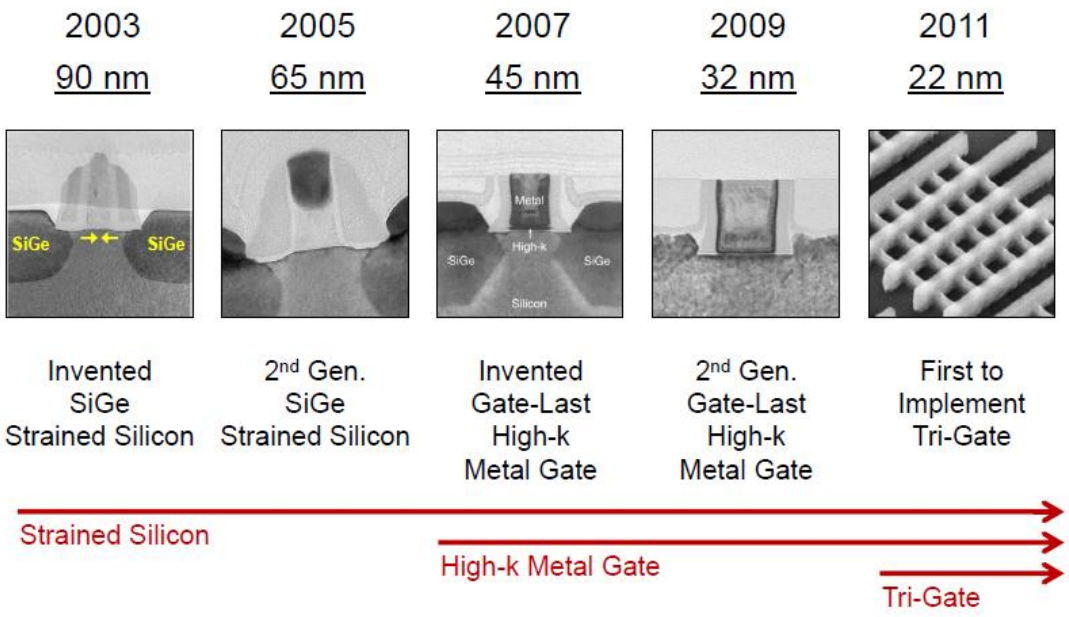

Figure 1.2: The roadmap of Intel CMOS scaling in the past decade [8].

The high-*k* metal gate process was first adopted in Intel 45 nm node (see Fig. 1.2) by replacing the SiO_2 layer by a hafnium based dielectric. The high-*k* dielectric provides a higher oxide capacitance with larger physical thickness, effectively suppressing gate leakage and boosting on-current (I_{on}). More importantly, it was the start of the "heterogeneous era" that not only the size is shrinking, new materials and new structures are also introduced [9]. A more recent breakthrough happened in 2011, when the first Tri-

gate MOSFET (or 3-D FET, FinFET) microchip was announced by Intel in their 22 nm technology node [8]. The transistors with multi-fin structure (Fig. 1.3) were adopted to replace the traditional 2-D bulk devices. The first advantage of the fin structure is the ability for the channel length scaling since the gate has better electrostatic control on the channel potential with the additional dimension. On the other hand, the channel is fully-depleted and the whole region is limited by the both sides of the gate. The high-doping density in bulk MOSFET is then not necessary. With low channel doping, the carrier mobility is enhanced with less impurity scattering; the random dopant fluctuation effect is also minimized. Furthermore, the inverse subthreshold slope (S.S.) and drain-induced barrier-lowering (DIBL) are reduced, improving the scalability of FinFETs. With all these performance improvements, Moore's Law is able to be continued. "What's after FinFET?" is then a big question for the industry.

As it has been pointed out by ITRS, one of the promising direction is to replace the channel with high mobility materials, such as III-V materials with high electron mobility and germanium (Ge) with high hole mobility. It's predicted that the technology would be ready for 7 nm node by 2018 [2]. In fact, III-V/Ge have been applied in other transistors such as BJTs, high electron mobility transistors (HEMTs), and Hetero-Bipolar transistors (HBTs) for decades. They have not been used in CMOS technology mainly because of the defective insulator/semiconductor interface comparing to the near perfect Si/SiO_2. As the Si based scaling is close to an end, these materials again draw the attentions [10, 11].

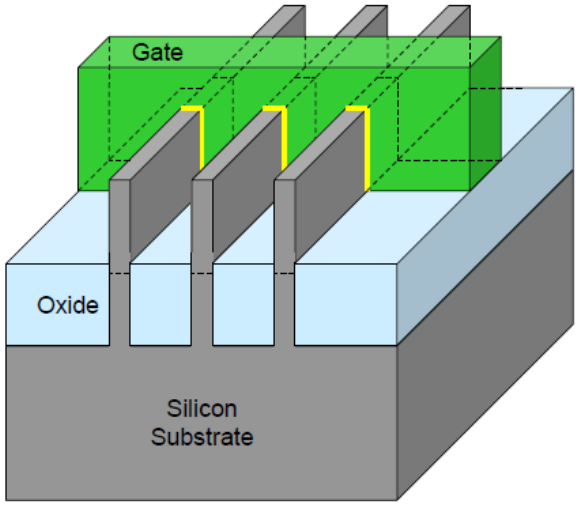

Figure 1.3: The roadmap of Intel CMOS scaling in the past decade [8].

Although high mobility is the indication of high current, the associated low effective mass may cause drawbacks. The first issue is the strong quantum-mechanical effect, which results in a higher threshold voltage (V_{th}), increasing the process difficulties. The small inversion capacitance from the intrinsic low density of states (DOS) is another latent issue. Inversion capacitance is composed of two capacitances in series: oxide capacitance and semiconductor inversion layer capacitance. In Silicon, the latter is much larger, and oxide capacitance is dominant. With low DOS materials, the inversion capacitance becomes smaller which decreases the inversion charge density and I_{on}.

Besides the issue mentioned above, another, and also the biggest challenge is to reduce the defect density on both interface state traps and bulk-oxide traps [12]. Different from interface traps, the bulk-oxide traps interact with semiconductor substrate through tunneling. This gives rise to a wide range of time constants due to the spreading of traps through the dielectric and generates large C-V dispersions [13-15]. The trap states are

undesired since they significantly deteriorate device performance. For example, with slow device switching, both trap states act as additional capacitances to be charged/discharged during the switching behavior. Such additional capacitances increase the total capacitance but do not contribute to the current, making it hard to modulate the surface potential inside semiconductor; therefore, the off state current (I_{off}) becomes larger and I_{on} becomes smaller. In another case with transient switching, the rising/falling time in state-of-the-art logic circuits is on the order of pico-seconds [2]. It is so fast that the traps cannot respond properly, hence they are unable to affect the switching curves; however, they can cause severe hysteresis, depending on how long the device stays in certain states. Such type of historical effects is akin to the threshold voltage (V_{th}) shifting in flash memory, but it is unintentional and hard to control. As a rough estimate, the interface state density should be on or below the order of $10^{11}eV^{-1}cm^{-2}$ and the bulk oxide trap density should be on or below the order of 10^{18} $ev^{-1}cm^{-3}$ in order to have tolerable V_{th} variation.

Despite the potential drawbacks above, the proof of concept has been demonstrated. It has been shown that III-V MOSFET has improved carrier injection speed compared with strained silicon at low V_{DS} [16], and the improved electrostatic control at short channel with FinFET structure has also been presented [17] (Fig. 1.4). In 2013, IMEC also announced the first III-V FinFET monolithic integrated on 300 mm Silicon wafer [18], which provides not only a promising way for CMOS scaling but also an opportunity in CMOS-RF integration.

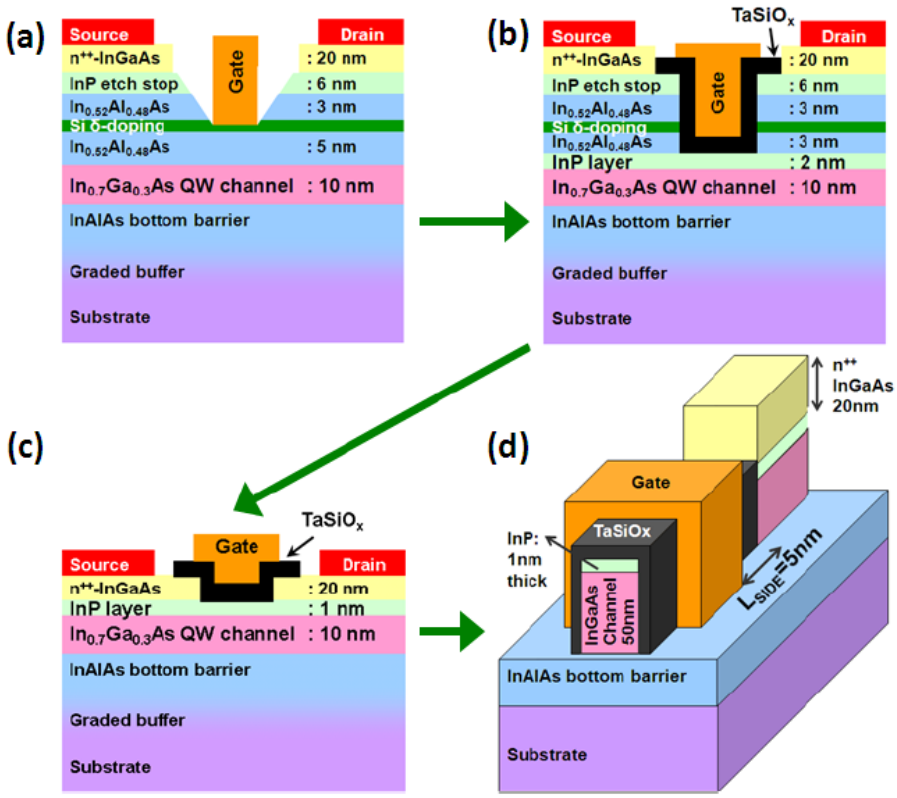

Figure 1.4: Intel InGaAs MOSFET evolution chart, from planar to multi-gate FET [17].

1.2 Objective and Organization of the Dissertation

This dissertation is aimed at the modeling and characterization of high-k/ III-V MOS capacitors. The theory basis for both bulk-oxide trap and interface model will be introduced; the examples on the electrical characterization in multiple conditions will also be included. The objective of this work is to explain and analyze the frequently observed capacitance-voltage (C-V) and conductance-voltage (G-V) dispersions in high-k/ III-V MOS capacitors. It is expected that this work will provide useful information to assist the researchers in this field to analyze and interpret experimental data qualitatively and quantitatively. Although Al_2O_3/InGaAs capacitors are used as examples in the

dissertation, the models and the methodologies can be applied to other MOS capacitors with high defect densities.

In Chapter 1, the CMOS scaling history is briefly reviewed, which includes the strained Silicon technology, the high-*k* metal gate, and the Tri-Gate FET. Furthermore, the potential of high mobility materials such as III-V and Ge MOSFET is introduced. The motivation and objective of the dissertation are stated.

In Chapter 2, two most widely used interface trap density (D_{it}) extraction methods, conductance method and Terman method, are introduced and re-examined. It is shown that they may not be suitable or may be misapplied in certain cases. It is suggested that both capacitive and conductive data components should be examined to avoid possible incorrect interpretation of data.

The full-D_{it} model and its application are introduced in Chapter 3. Both C-V and G-V dispersion data on Al_2O_3/n-InGaAs capacitors are fitted and explained in detail by the full D_{it} model, from depletion to inversion region. The reason for the observed C-V humps is also explained.

In Chapter 4, the distributed bulk-oxide trap (N_{bt}) model is introduced. Starting from the theory background, the model is applied to explain the capacitance and conductance dispersion data in accumulation region. The model with added series resistance and the comparison to the "lumped circuit model" are also presented.

In Chapter 5, insulator thickness and temperature effects are addressed by applying the D_{it} and N_{bt} models presented in Chapters 3 and 4. The models indicate that for the same trap density, the normalized C-V dispersion due to border traps increases toward thinner oxides, whereas that due to interface states behaves oppositely, exactly as

observed in the data. For the temperature effect, the dispersion in C-V from interface states diminishes at low temperatures, while that from oxide traps changes little to none. Those trends are shown to be driven by a temperature dependent trap time constant, not trap density.

Chapter 6 further extends the model in explaining the light illumination effect on C-V dispersions. The difference between p- and n-type data can be explained by including an additional diffusion conductance "G_d", which represents the minority carrier generation in the semiconductor substrate. It is shown that the asymmetric D_{it} distribution inside the bandgap is responsible for the differences.

The last chapter summarizes the entire dissertation.

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Chapter 2

Re-examination of the Extraction of MOS Interface State Density by C-V Stretchout and Conductance Methods

In this chapter, both extraction methods using model generated C-V and G-V characteristics are examined with a preprogrammed amount of D_{it}. Realistic, bias-dependent trap time constants are assumed. The interface-state densities are then played back by applying either Terman method or the conductance method to the model data. Among the factors investigated are the robustness of the conductance method subject to errors in C_{ox} estimation and its extendibility into the weak inversion region.

2. 1 C-V Stretchout (Terman) Method

Extraction of interface-state density by the stretchout of high frequency C-V curve was first proposed by L.M. Terman in 1962 [1], hence also known as Terman method. It is assumed that the small signal frequency is high enough that the total measured capacitance at that frequency has no interface-state component. The only effect of the interface states is then to cause a stretchout of the C-V curve along the gate voltage (V_g) axis given by

$$\Delta V_g = \Delta \psi_s \left(1 + \frac{C_s + C_{it}}{C_{ox}} \right) \tag{2.1}$$

where ψ_s is the surface potential, C_{ox} is the gate oxide capacitance, C_s is the intrinsic semiconductor capacitance, and $C_{it} = qD_{it}$ is the interface-state capacitance. An example is shown in Fig. 2.1 with the dashed curve being the ideal C-V (D_{it} = 0) simulated by *Sentaurus* [2]. The thin solid curve is generated from the ideal C-V by adding a constant $D_{it} = 5\times10^{12}$ $cm^{-2}eV^{-1}$ using Eq. (2.1) and the interface-state model in Fig. 2.2(a). The crossover point of the two curves is arbitrarily set to be V_g = 0.1 V. Note that a constant V_g shift of one entire curve has no effect as far as Terman method is concerned. If the interface-state contribution to the capacitance in the solid curve is negligible, then the total capacitance C_{tot} equals the serial combination of C_{ox} and C_s for both the ideal C-V and the stretched-out C-V. Therefore, the same C_{tot} between the two curves means the same C_s hence the same ψ_s. D_{it} can then be extracted by

$$D_{it} = \frac{1}{q}\left[\frac{(\partial C/\partial V_g)_{sim}}{(\partial C/\partial V_g)_{data}} - 1\right](C_d + C_{ox}) \tag{2.2}$$

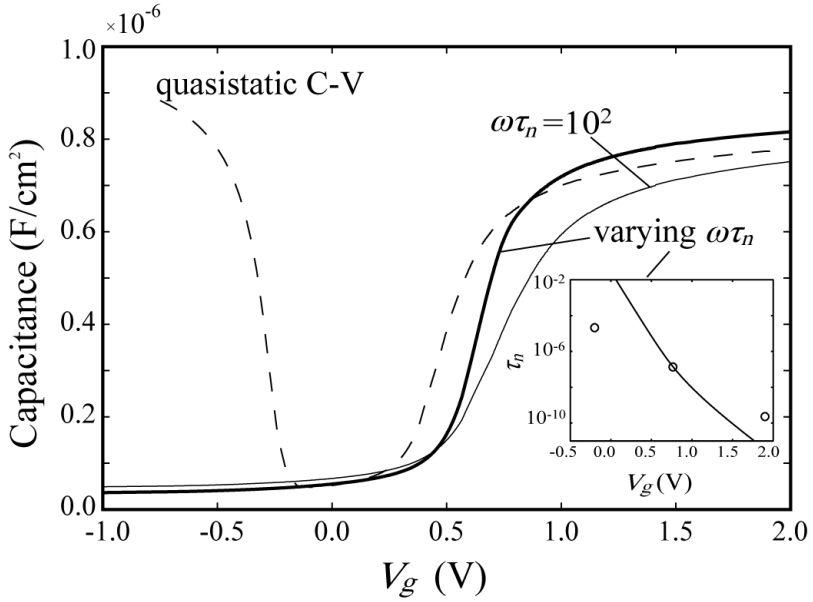

Figure 2.1: Dashed curve is simulated quasistatic C-V with no D_{it}. Solid curves are 1 MHz C-V generated from the full D_{it} model with D_{it}=5×10^{12} eV^{-1}cm^{-2}. The varying τ_n profile is given in the inset (line), along with published data points (circles). The substrate is $In_{0.53}Ga_{0.47}As$ with an n-type doping of 1.0×10^{16} cm^{-3}. C_{ox}=1.1×10^{-6} F/cm^2.

A key parameter not yet mentioned is the trap time constant τ_n. Here we assume an n-type substrate so electrons play the major role in depletion. In fact, there are two time constants, τ_n and τ_p, in the full interface-state model shown in Fig. 2.2(a). The intrinsic semiconductor capacitances are C_d (depletion capacitance) and C_i (inversion capacitance). They are provided from the *Sentaurus* run as functions of ψ_s or V_g. The interface-state components C_{Tn}, C_{Tp}, G_{gr} are complex functions of D_{it}, τ_n, τ_p, and frequency ω (a thorough introduction to full interface-state model is in Chapter 3) [4]. In the depletion and accumulation region where Terman method is applied, $\tau_n << \tau_p$, the full circuit can be simplified to that of Fig. 2.2(b) with [4]

$$C_p = C_d + C_{it}(\omega\tau_n)^{-1}\tan^{-1}(\omega\tau_n) \tag{2.3}$$

$$G_p/\omega = C_{it}(2\omega\tau_n)^{-1}\ln[1+(\omega\tau_n)^2] \tag{2.4}$$

The interface-state capacitance term in Eq. (2.3) decreases slowly with ω when $\omega\tau_n >> 1$. The thin solid C-V curve in Fig. 2.1 mentioned earlier assumes $\omega\tau_n = 100$ throughout the bias range. Even with that, the extracted D_{it} by Terman method played back in Fig. 2.3 contains some error in the region of low C_{tot}. In practice, 1 MHz frequency is not nearly high enough to satisfy $\omega\tau_n > 100$ as it requires $\tau_n > 2\times10^{-5}$ s up to accumulation. Typically, in InGaAs MOS for example, τ_n varies from 10^{-5} s in deep depletion [3] to 10^{-10} s in strong accumulation [5], as shown in the inset to Fig. 2.1. The bias dependence arises mainly from the fact that τ_n is inversely proportional to the electron volume density at the surface. This has the effect of steepening up the C-V slope because as C_{tot} increases, $\omega\tau_n$ becomes smaller thus adding more C_{it} contribution to C_{tot}. Such a case is shown in Fig. 2.1 as the thick solid C-V curve, with the input $\tau_n(V_g)$ given in the inset. Fig. 2.3 shows that the D_{it} extracted by Terman method is severely underestimated, even going negative over a wide range of V_g including and beyond the point of the steepest slope. Note that this starts to happen at $C_{tot} \sim 2\times10^{-7}$ F/cm^2, despite $\omega\tau_n > 1$ in that region.

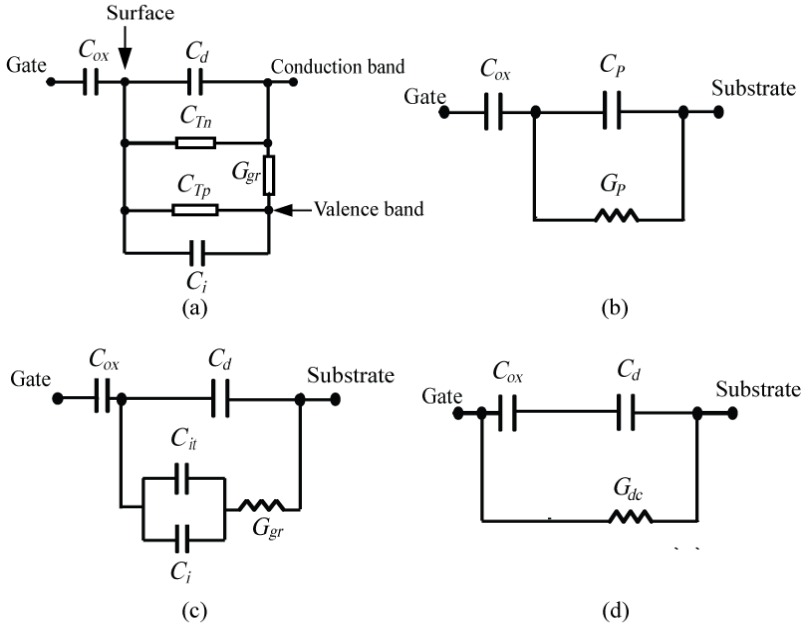

Figure 2.2: (a) Equivalent circuit of full interface-state (D_{it}) MOS model (n-type substrate) [4]. (b) Equivalent circuit by lumping the semiconductor components into admittance $G_p+j\omega C_p$. (c) Simplified equivalent circuit in inversion at low frequencies. (d) Equivalent circuit with tunneling leakage (G_{dc}), no D_{it}.

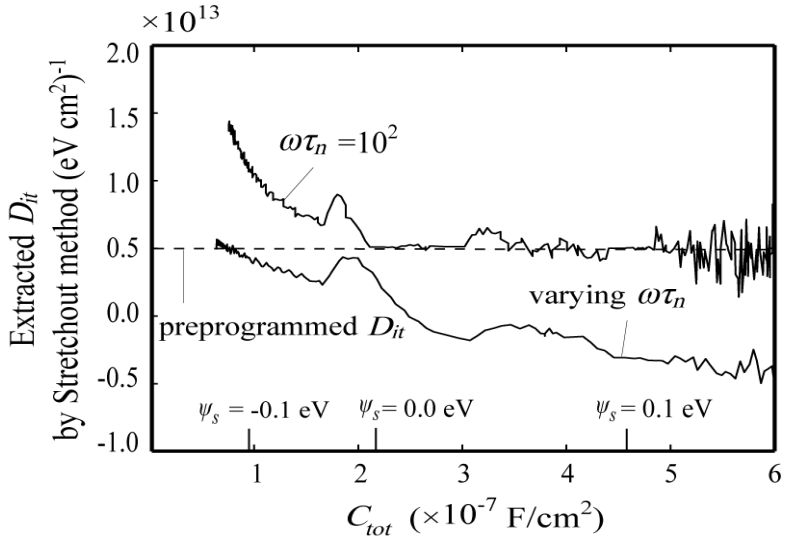

Figure 2.3: Extracted D_{it} by Terman method versus C_{tot} for the two $\omega\tau_n$ cases in Fig. 2.1. Surface potential (ψ_s) values are labeled at several bias points.

A different type of error occurs in applying Terman method when the stretchout

of C-V is caused by bulk oxide traps, not by D_{it}. Stretchout by bulk oxide traps (N_{bt}, in units of $cm^{-3}eV^{-1}$) takes an entirely different mathematical form [6]. Applying Eq. (2.2) to C-V data would not yield meaningful results.

2. 2 Conductance Method

The conductance method is based on Eq. (2.4), valid in depletion. The G_p/ω versus ω plot exhibits a peak value of $0.4C_{it}$ at $\omega\tau_n = 1.98$, from which D_{it} is determined. Note that G_p is computed from the total measured MOS admittance $G_{tot} + j\omega C_{tot}$ using $[G_p + j\omega C_p]^{-1} = [G_{tot} + j\omega C_{tot}]^{-1} - (j\omega C_{ox})^{-1}$. So an estimated value of C_{ox} is needed for the conductance method.

For G_p/ω peaks played back from the model generated dispersions, Fig. 2.4(a) shows that reasonably accurate D_{it} is obtained by the conductance method, even with a ±10% error on C_{ox}. The peak moves to lower frequencies as τ_n increases toward deeper depletion. It becomes unobservable when below the low end of the measured frequency range, typically 1 kHz.

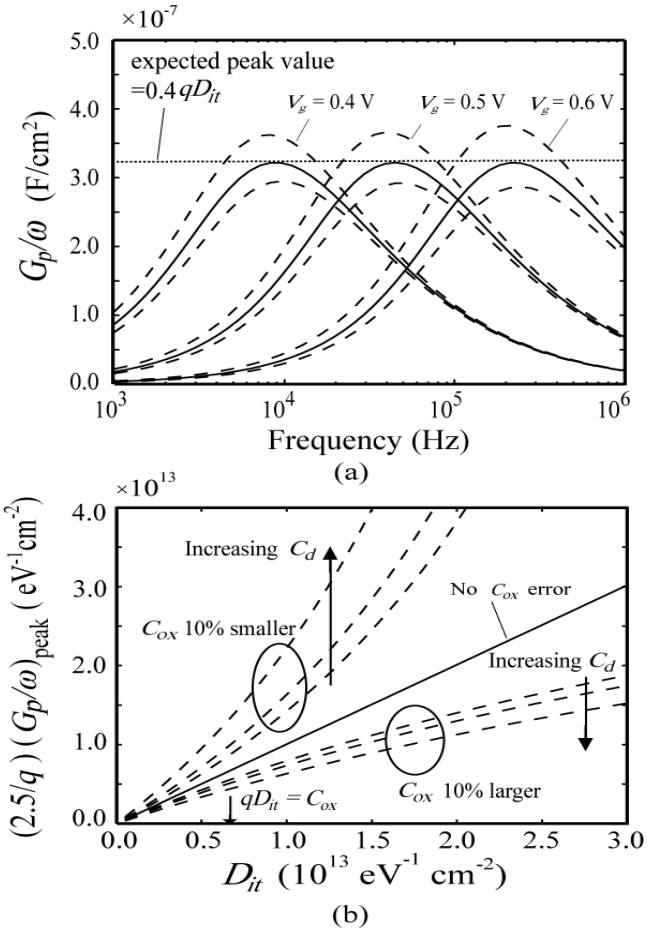

Figure 2.4: (a) G_p/ω versus frequency for several V_g biases in depletion. Solid curves are obtained by subtracting the exact $(j\omega C_{ox})^{-1}$ from the model $[G_{tot} + j\omega C_{tot}]^{-1}$. The dashed curves are obtained similarly, but with ±10% error in C_{ox}. (b) D_{it} extracted by the conductance method versus the true D_{it} preprogrammed in the model. Solid line uses the correct C_{ox}. Dashed curves are extracted with ±10% C_{ox} error. Each dashed group consists of three C_d values: 5×10^{-7}, 1×10^{-6}, and 2×10^{-6} F/cm^2.

In previously published literatures [7, 8], it has been pointed out that D_{it} extraction based on conductance method lost the sensitivity when $qD_{it} > C_{ox}$. This conclusion is actually based on the D_{it} extraction from G_{tot}/ω peak, not G_p/ω peak applied in conductance method. Mathematically, from the notation in Fig. 2.2 (b), the two are related by the equation

$$\frac{G_{tot}}{\omega} = \frac{C_{ox}^{\ 2}(G_p/\omega)}{(G_p/\omega)^2 + (C_{ox} + C_p)^2} \tag{2.5}$$

In the cases of low D_{it}, G_p/ω is negligible compared to C_{ox} + C_p in the denominator, and Eq. (xx) can be rewritten as

$$\frac{G_{tot}}{\omega} \approx \frac{G_p/\omega}{(1 + C_p/C_{ox})^2} \tag{2.6}$$

G_{tot}/ω and G_p/ω are related by a frequency independent but bias dependent factor, $(1+ C_p/C_{ox})^{-2}$, which contains both C_{it} and C_d components and goes down as C_d increases toward accumulation region. It is not straightforward to extract D_{it} in this manner since C_d should be extracted in advance. On the other hand, if G_p/ω is not negligible comparing to C_{ox} + C_p in the denominator (which is a common case in high-k/ III-V MOS capacitor), there is no simple correlation between G/ω and G_p/ω, and Eq. (2.3) and (2.4) have to be applied in relating the two. In general, we believe that the D_{it} extraction from G_{tot}/ω is not applicable and misleading. In contrast to the G_{tot}/ω peak, the G_p/ω peak always yields the correct D_{it} value even if $qD_{it} >> C_{ox}$, as long as there is no error in C_{ox}. Fig. 2.4(b) shows the D_{it} extracted by the conductance method as a function of the true D_{it}. When $qD_{it} >> C_{ox}$, errors in the extracted D_{it} increases with C_{ox} errors, especially if C_{ox} is underestimated. In that case, D_{it} can be overestimated by a large factor if C_d is large, i.e., toward upper half of the C-V. It is far safer to overestimate C_{ox} than underestimate it.

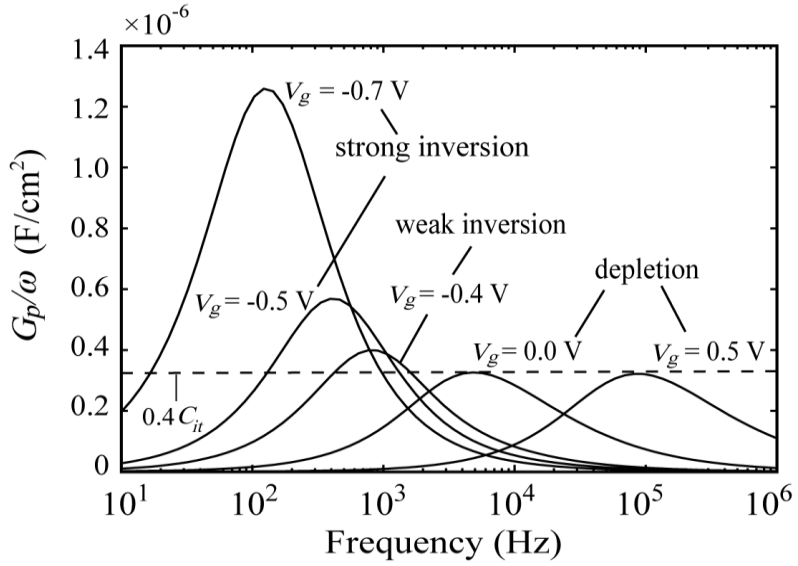

Figure 2.5: G_p/ω versus frequency from depletion to inversion. C_{ox} = 1.1×10^{-6} F/cm^2. From V_g = 0.5 V to -0.7 V, C_d varies from 1.59×10^{-7} F/cm^2 to 3.95×10^{-8} F/cm^2, τ_n varies from 3.72×10^{-6} s to 2.0×10^{-3} s. C_i is negligible except V_g = -0.5 V where C_i = 3.54×10^{-7} F/cm^2 and V_g = -0.7 V where C_i = 1.72×10^{-6} F/cm^2. In weak inversion, the peak value is $0.5C_{it}$. In strong inversion, the peak is $0.5(C_i + C_{it})$.

If the MOS C-V measurement is extended to below 1 kHz, e.g., to 100 Hz, the G_p/ω peak will persist into weak inversion and even strong inversion. Since $\tau_p < \tau_n$, the simplified circuit in Fig. 2.2(b) no longer applies. The full interface-state model in Fig. 2.2(a) must be used. Fig. 2.5 plots model generated G_p/ω versus ω over a wide range of V_g bias from depletion to strong inversion. A realistic bias dependence of τ_n, τ_p like that of an InGaAs MOS is assumed [3]. At low frequencies where the peak is located in inversion, the MOS equivalent circuit can be approximated by that of Fig. 2.2(c). The parameter $G_{gr} = (C_{it}/\tau_n)\ln(\tau_n/\tau_p)$ represents minority carrier generation and recombination via interface states [4]. The peak of G_p/ω is then $0.5(C_i + C_{it})$ at $\omega = G_{gr}/(C_i + C_{it})$. In weak inversion, C_i is negligible, interpreting the peak value the same as $0.4C_{it}$ in

depletion introduces only a slight error in D_{it}. In strong inversion, however, D_{it} can be significantly overestimated if the entire peak value is taken to be from C_{it} [6], [9]. Note in Fig. 2.5 that the peak continues to shift to lower frequencies as G_{gr} decreases and C_i increases toward stronger inversion.

2. 3 False G_p/ω peak

A factor often overlooked in the conductance method is C_p of Eq. (2.3) [10]. If G_p/ω peaks are indeed due to D_{it}, C_p should behave accordingly, namely, decreasing from $C_d + C_{it}$ at low frequencies ($\omega\tau_n << 1$) to C_d at high frequencies ($\omega\tau_n >> 1$). In two examples given below, false G_p/ω peaks can arise from non-D_{it} factors. Examination of C_p is the key to tell them apart.

The first example of false G_p/ω peak is caused by tunneling leakage through the gate insulator. It can be represented by a shunt conductance G_{dc} between the gate and the substrate as in Fig. 2.2(d) ($D_{it} = 0$ is assumed in this case). The measured MOS admittance is then $G_{tot} = G_{dc}$ and $C_{tot} = C_{ox}C_d/(C_{ox} + C_d)$. Applying $[G_p + j\omega C_p]^{-1} = [G_{tot} + j\omega C_{tot}]^{-1} - (j\omega C_{ox})^{-1}$ as before, we obtain

$$\frac{G_p}{\omega} = \frac{\omega C_{ox}^{\ 2}(C_{ox} + C_d)^2 G_{dc}}{\omega^2 C_{ox}^{\ 4} + (C_{ox} + C_d)^2 G_{dc}^{\ 2}} \tag{2.7}$$

which happens to exhibit a peak value of $(C_{ox} + C_d)/2$ at $\omega = (1 + C_d/C_{ox})G_{dc}/C_{ox}$. As plotted in Fig. 2.6(a) for different magnitudes of G_{dc}, the false G_p/ω peaks are

indistinguishable from those due to D_{it}. Examination of C_p in Fig. 2.6(b), however, reveals that it does not have the correct behavior. In fact, C_p turns negative at low frequencies.

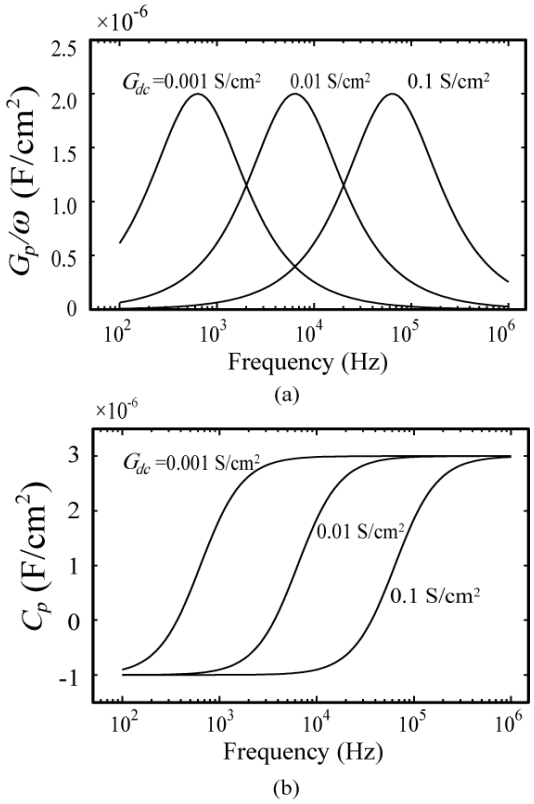

Figure 2.6: (a) False G_p/ω peaks due to G_{dc} (three values). (b) Corresponding C_p versus ω. Here, C_{ox}=1.0×10^{-6} F/cm^2, C_d = 3.0×10^{-6} F/cm^2, and τ_n = 1.0×10^{-8} s.

The second case of false G_p/ω peak is associated with bulk-oxide traps N_{bt} in units of cm^{-3}eV^{-1}. Normally, no G_p/ω peak is observed when the dispersion is caused by bulk-oxide traps [5]. However, when N_{bt} is high enough, it is possible that C_{tot} in accumulation becomes larger than C_{ox} below certain frequency. G_p/ω is then maximized at the frequency C_{tot} crosses over C_{ox}. This is shown in Fig. 2.7(a). Again, C_p in Fig. 2.7(b) reveals that the G_p/ω peak is false as it goes negative at low frequencies. Note that at low

N_{bt} levels, the false G_p/ω peak moves to below the frequency range of measurement. For even lower levels (5×10^{18} $eV^{-1}cm^{-3}$), the peak may not exist at all.

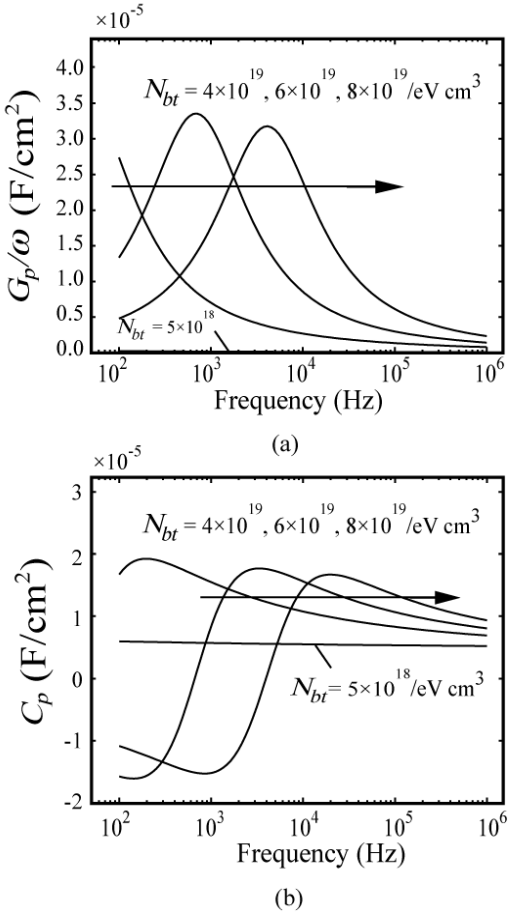

Figure 2.7: (a) False G_p/ω peaks due to large N_{bt} (three values). (b) Corresponding C_p versus ω. Here, C_{ox}=1.0×10^{-6} F/cm^2, C_d = 5.0×10^{-6} F/cm^2, τ_n = 1.0×10^{-10} s, and attenuation coefficient κ=4×10^7 cm^{-1}. The MOS is biased in strong accumulation.

The text of Chapter 2, in part, is a reprint of the material as it appears in "Re-examination of the Extraction of MOS Interface State Density by C-V Stretchout and Conductance Methods" by Han-Ping Chen, Yu Yuan, Bo Yu, Chih-Sheng Chang, Clement Wann, and Yuan Taur, Semiconductor Science Technology, 2013. The dissertation author was the primary investigator and author of this paper.

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Chapter 3

Interface Traps in High-*k* III-V MOS Capacitors

This chapter presents a detailed analysis of the multifrequency capacitance–voltage and conductance–voltage data of Al_2O_3/n-InGaAs MOS capacitors from depletion to inversion. It is shown that the widely varied frequency dependence of the data in this region can be fitted to various regional equivalent circuits derived from the full interface-state model. By calibrating the model with experimental data, the interface-state density and the trap time constants are extracted as functions of energy in the bandgap, from which the stretch-out of gate voltage is determined. It is concluded that the

commonly observed decrease of the 1-kHz capacitance toward stronger inversion is due to the increasing time constant for traps to capture majority carriers at the inverted surface.

3. 1 Overview of the Capacitance and Conductance Data and Modeling Approach

Fig. 3.1 shows the multiple frequency C-V and G-V data measured from a $Pt/Al_2O_3/n\text{-}In_{0.53}Ga_{0.47}As$ MOS capacitor. It is fabricated under similar processing procedures as in Ref. [1]. The semiconductor layer structure is 1 μm $2\times10^{16}cm^{-3}$ doped n-$In_{0.53}Ga_{0.47}As$ on 100 nm $5\times10^{18}cm^{-3}$ doped n-$In_{0.53}Ga_{0.47}As$ on n^+ InP substrate. The Al_2O_3 film is prepared by 50 cycles of atomic layer deposition (ALD) with trimethyl aluminum precursor and water vapor oxidant. The sample is then annealed in forming gas for 30 minutes at 400°C.

Superimposed in Fig. 3.1(a) is an ideal quasistatic C-V simulated by *Sentaurus* without any traps. The simulation parameters are $C_{ox} = 1.06\times10^{-6}$ F/cm^2, doping density = 3.7×10^{16} /cm^3, and a gate work function such that the simulated curve crosses over the 1 MHz data at $V_g = 0.2$ V. Labeled on the simulated curve are E_c, E_i, and E_v at gate voltages where the surface potential crosses these energies. It will be shown in Chapter. 4 that the dispersions in accumulation, $V_g > 0.2$ V, are due to bulk-oxide traps [2], [3]. The dispersions in depletion and inversion, $V_g < 0.2$ V, i.e., the hump region, however, do not exhibit the same frequency dependence expected of bulk-oxide traps. The low-frequency

C-V humps start at V_g ~ 0.1 V where the inversion charge capacitance is negligible, hence they are due to interface states.

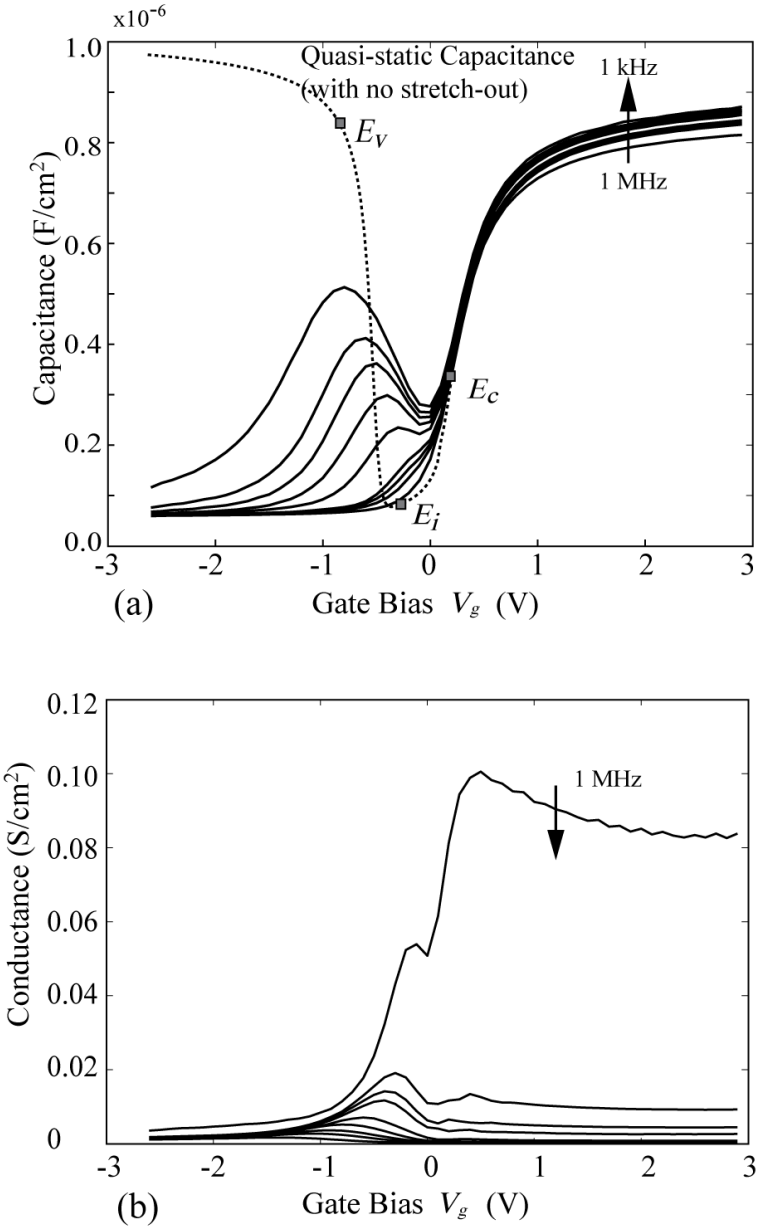

Figure 3.1: Experimental (a) C-V and (b) G-V measured at 1 kHz, 2 kHz, 3 kHz, 5 kHZ, 10 kHZ, 30 kHz, 50 kHz, 100 kHz and 1 MHz.

In the classic interface state theory [4], a single-level trap is represented by an Y-equivalent circuit consisting of a capacitance C_T and two conductances G_n, G_p connected

among the surface, the conduction band, and the valence band. Each of the three elements is proportional to the trap density per area and is dependent on the energy of the trap through the Fermi-Dirac distribution function. In practice, there is a continuous distribution of traps as a function of their energy, characterized by D_{it}, the interface-state trap density per area per energy. To integrate the trap contributions for all energies, the Y-equivalent circuit must first be converted to a Δ-equivalent circuit. The resulting circuit is shown in Fig. 3.2, where the intrinsic elements are the oxide capacitance C_{ox}, the depletion charge capacitance C_d, the inversion charge capacitance C_i, and a conductance G_d representing generation and recombination in the bulk. At room temperature, and for a small-signal frequency of 1 kHz, G_d is usually negligible so that the intrinsic C-V exhibits high-frequency-like characteristics.

The interface-state components are C_{Tn}, C_{Tp}, and G_{gr} in Fig. 3.2. They are given by [4]:

$$C_{Tn} = qD_{it}\tau_n^{-1}\int_0^1 df(1-f)[j\omega f(1-f) + f\tau_p^{-1} + (1-f)f\tau_n^{-1}]^{-1} \tag{3.1}$$

$$C_{Tp} = qD_{it}\tau_p^{-1}\int_0^1 df(1-f)[j\omega f(1-f) + f\tau_n^{-1} + (1-f)f\tau_p^{-1}]^{-1} \tag{3.2}$$

$$G_{gr} = qD_{it}\tau_p^{-1}\tau_n^{-1}\int_0^1 df[j\omega f(1-f) + f\tau_p^{-1} + (1-f)f\tau_n^{-1}]^{-1} \tag{3.3}$$

where

$$\tau_n = (\sigma_n v_{th}^{\ n} n_s)^{-1} \tag{3.4}$$

and

$$\tau_p = (\sigma_p v_{th}^{\ p} p_s)^{-1} \tag{3.5}$$

σ_n and σ_p are the electron and hole capture cross sections of the traps, v_{th}^{n} and v_{th}^{p} are the carrier thermal velocities, n_s and p_s are the electron and hole densities at the semiconductor surface. Note that in general, C_{Tn}, C_{Tp}, and G_{gr} are all complex functions of frequency ω. At every gate bias or surface potential (ψ_s), they are completely specified by three parameters, D_{it}, τ_n, and τ_p, which are chosen in our procedure to fit both the $C_{tot}(\omega)$ and $G_{tot}(\omega)$ data at that point.

At 1 MHz, the measured C_{tot} is nearly frequency independent, implying no contribution from the traps. The depletion-charge capacitance C_d is therefore chosen such that the serial combination of C_{ox} and C_d matches the 1 MHz C_{tot} at every gate bias. The inversion charge capacitance C_i is given by the quasi-static C-V simulation (Fig. 3.1) as a function of ψ_s. To estimate C_i at a given gate voltage V_g, the stretch-out $V_g(\psi_s)$ of the experimental C-V by the DC effect of D_{it} must first be worked out, as described later.

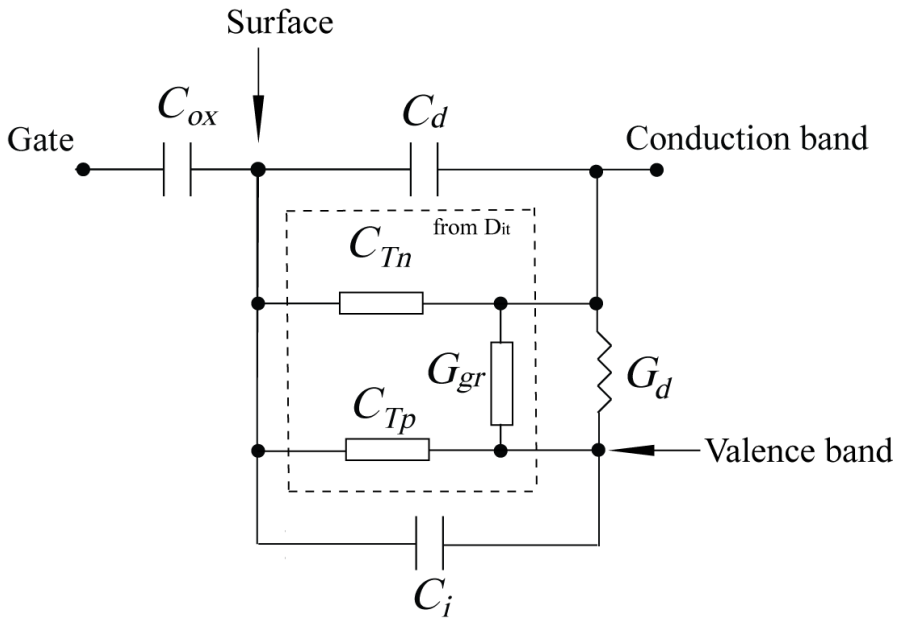

Figure 3.2: Equivalent circuit model of MOS (n-type substrate) capacitance with interface state (D_{it}) [4].

3. 2 Regional Fitting of Data to the Interface-State Model

A numerical program is set up to compute $C_{tot}(\omega)$ and $G_{tot}(\omega)$ based on Fig. 3.2 and Eqs. (3.1)-(3.3). To gain physical insight to the model, it helps to make regional approximations to reduce the model to simple, analytical forms. The measured C_{tot} and G_{tot} data are often converted to C_p and G_p defined in Fig. 3.3 for correlation with analytic models.

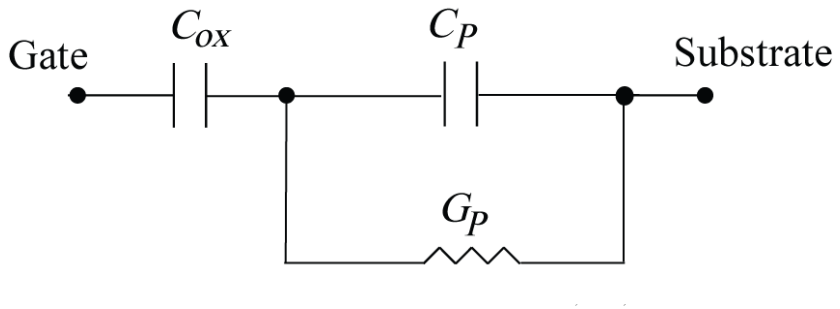

Figure 3.3: MOS equivalent circuit by lumping the semiconductor components in Fig.3.2 into admittance $G_p + j\omega C_p$.

3.2.1 Depletion region and Midgap

In the depletion region, $V_g \sim 0$, $\tau_n << \tau_p$, the only significant component from the interface states is C_{Tn}. It is an admittance in parallel with C_d such that [4]

$$C_p = C_d + C_{it}(\omega\tau_n)^{-1}\tan^{-1}(\omega\tau_n) \qquad \text{depletion} \qquad (3.6)$$

$$G_p/\omega = C_{it}(2\omega\tau_n)^{-1}\ln[1+(\omega\tau_n)^2] \qquad \text{depletion} \qquad (3.7)$$

Here, $C_{it} \equiv qD_{it}$ (with D_{it} in units of $cm^{-2}eV^{-1}$) is the interface-state capacitance. This is the well-known "Conductance Method," in which D_{it} is extracted by plotting G_p/ω versus ω and reading the peak, $0.4C_{it}$ at $\omega\tau_n = 1.98$. Fig. 3.4 shows the G_p/ω versus ω plots for several V_g biases de-embedded from the $C_{tot}(\omega)$ and $G_{tot}(\omega)$ data using $C_{ox} = 1.06\times10^{-6}$ F/cm^2. At $V_g = -0.2$ V, a D_{it} of 2.1×10^{12} $cm^{-2}eV^{-1}$ and τ_n of 2.8×10^{-5} s are extracted from the fitting. As V_g becomes more negative, both D_{it} and τ_n increase. The latter is due to further depletion of the electron density at the surface. For V_g more negative than –0.6 V, the G_p/ω peak shifts to a frequency below 1 kHz.

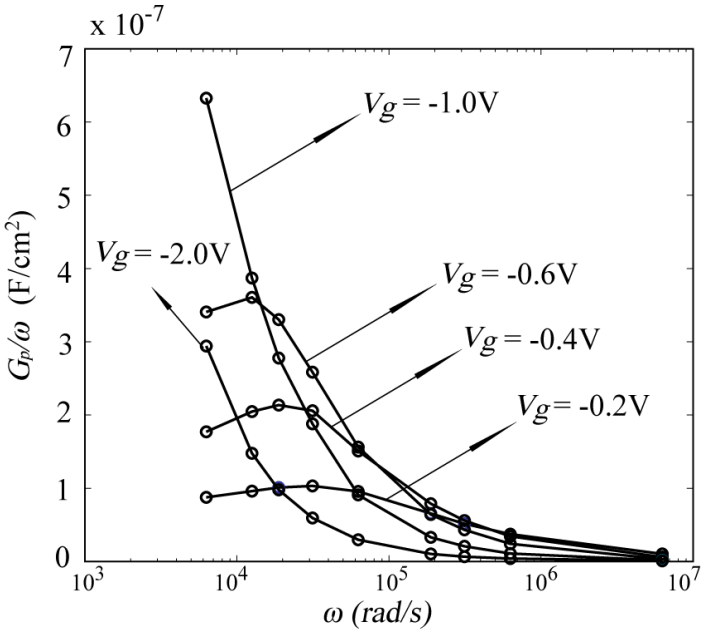

Figure 3.4: Extracted G_p/ω data versus ω for different gate biases.

A particular bias point in depletion is when the Fermi level crosses the midgap potential where $\tau_n = \tau_p = \tau$. For most of the frequency range, $\omega\tau > 1$, and Eq. (3.7) can be approximated as [4]

$$G_p = \frac{C_{it}}{\tau}\ln(\omega\tau_n) \qquad \text{midgap} \qquad (3.8)$$

By plotting G_p versus $\ln(\omega)$ for a wide range of V_g in Fig. 3.5, it is determined that the midgap position is reached near $V_g = -0.4$ V where $\tau_n \approx \tau_p \approx 10^{-4}$ s and $D_{it} \approx 3.9\times10^{12}$ $cm^{-2}eV^{-1}$.

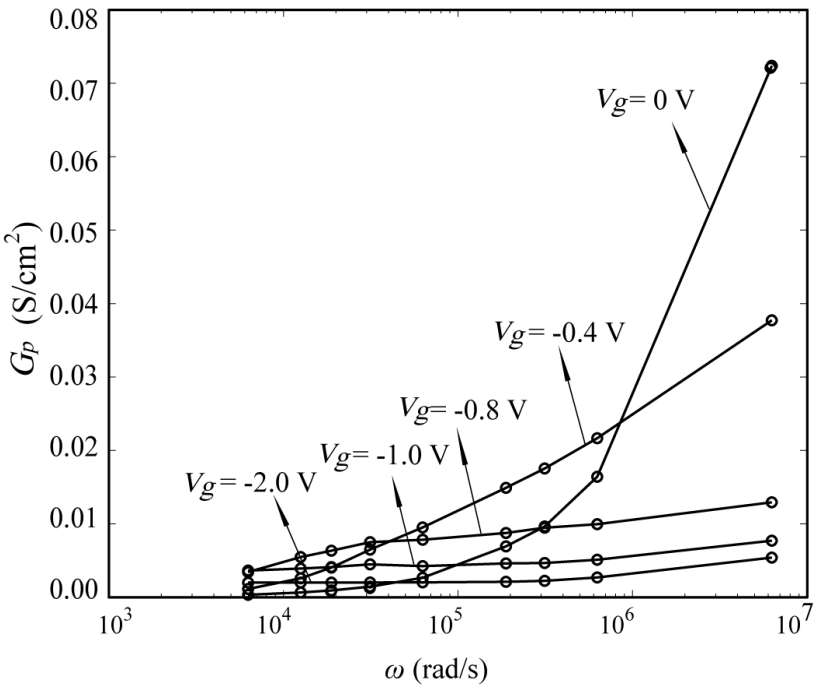

Figure 3.5: Extracted G_p data versus ω for different gate biases.

3.2.2 Weak Inversion Region

In the weak inversion region (-1.0 V $\le V_g \le -0.4$ V), $\tau_p < \tau_n$. While $\omega\tau_n > 1$ for the entire frequency range, $\omega\tau_p > 1$ at 1 MHz but $\omega\tau_p < 1$ at 1 kHz. There is no single analytic circuit valid for the entire range. At high frequencies, $\omega C_{Tp} >> G_{gr}$, the interface-state admittance can be considered as $j\omega C_{Tn}$ in parallel with G_{gr}, with $j\omega C_{Tn}$ dominating. It has been shown to yield [4]

$$C_p = C_d + \frac{\tau_p}{\tau_n} C_{it} (\omega\tau_p)^{-1} \tan^{-1}(\omega\tau_p) \quad \text{weak inversion, } \omega\tau_p > 1 \tag{3.9}$$

$$G_p = \frac{C_{it}}{2\tau_n} \ln[(\frac{\tau_n}{\tau_p})^2 + (\omega\tau_n)^2] \quad \text{weak inversion, } \omega\tau_p > 1 \tag{3.10}$$

for the components defined in Fig. 3.3. At low frequencies, the interface-state contribution is dominated by $j\omega C_{Tp}$ in series with G_{gr} (C_i is negligible in weak inversion), but $j\omega C_{Tn}$ is not completely negligible. For $\omega\tau_p << 1$, $C_{Tp} \approx C_{it}$, and $G_{gr} \approx (C_{it}/\tau_n)\ln(\tau_n/\tau_p)$. The equivalent circuit and C_p, G_p expressions are similar to the strong inversion case below.

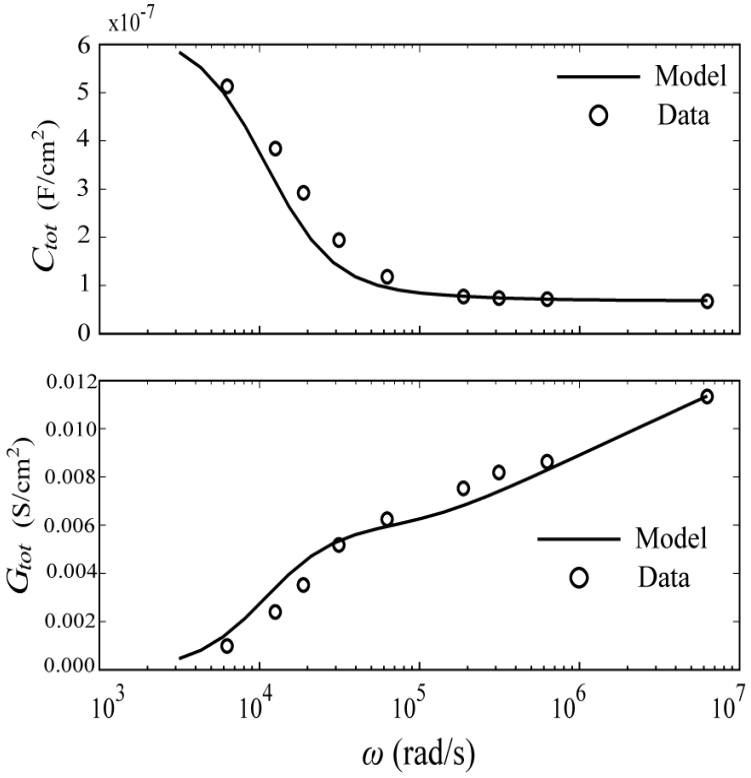

Figure 3.6: Model fitting of C&G data at V_g= -0.8 V. Model parameters are C_{it} = 1.312×10^{-6} F/cm^2, C_i= 1.45×10^{-7} F/cm^2, C_d= 7.3×10^{-8} F/cm^2, τ_n= 8.7×10^{-4} s, τ_p= 1.1×10^{-5} s.

At V_g = -0.8 V near the peak of the hump, parameters C_{it}, τ_n, and τ_p are chosen to fit both the $C_{tot}(\omega)$ and $G_{tot}(\omega)$ data (Fig. 3.6) using the full numerical program.

3.2.3 Strong Inversion Region

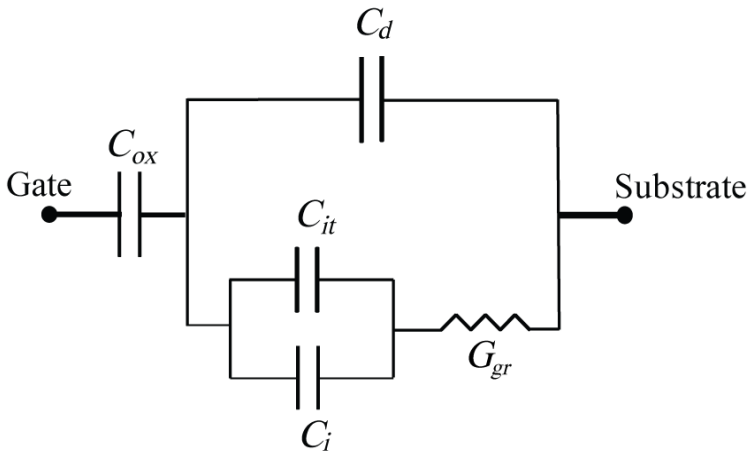

Figure 3.7: Simplified MOS equivalent circuit in strong inversion.

In strong inversion, $V_g < -1$ V, $\tau_p << \tau_n$, C_{Tn} is negligible. Also, $C_{Tp} \approx C_{it}$, and C_i becomes appreciable. The equivalent circuit is shown in Fig. 3.7, where

$$G_{gr} = \frac{C_{it}}{\tau_n} \ln\left(\frac{\tau_n}{\tau_p}\right) \qquad \text{strong inversion} \qquad (3.11)$$

For this circuit, C_p and G_p are

$$C_p = \frac{(C_i + C_{it}) G_{gr}^{\ 2}}{\omega^2 (C_i + C_{it})^2 + G_{gr}^{\ 2}} + C_d \qquad \text{strong inversion} \qquad (3.12)$$

$$G_p = \frac{\omega^2 (C_i + C_{it})^2 G_{gr}}{\omega^2 (C_i + C_{it})^2 + G_{gr}^{\ 2}} \qquad \text{strong inversion} \qquad (3.13)$$

Fig. 3.8 plots the $G_p(\omega)$ data for several V_g biases in strong inversion. For frequencies in the low kHz range, G_p is independent of frequency, implying that $\omega(C_i +$

C_{it}) >> G_{gr}, and $G_p = G_{gr} = (C_{it}/\tau_n)\ln(\tau_n/\tau_p)$. G_p or G_{gr} decreases as V_g becomes more negative. This is a reflection of the longer τ_n as the MOS is biased into stronger inversion. Physically, the surface electron density in the conduction band becomes so low that it takes much longer for a trap to capture an electron. The increase of G_p toward 1 MHz cannot be explained by the interface-state model alone. It will be addressed in a later section.

Under the above condition, $\omega(C_i + C_{it}) >> G_{gr}$, the interface-state contribution to C_p in Eq. (3.12) is $(G_{gr}/\omega)^2/(C_i + C_{it})$, inversely proportional to $C_i + C_{it}$. It is counter-intuitive that in this regime, C_p actually goes down as the inversion capacitance C_i goes up. The combination of decreasing G_{gr} and increasing C_i accounts for the observed drop of the 1 kHz C_{tot} beyond the peak of the hump. Note that the drop of C_{tot} does not imply that C_{it} (or D_{it}) is decreasing toward more negative V_g.

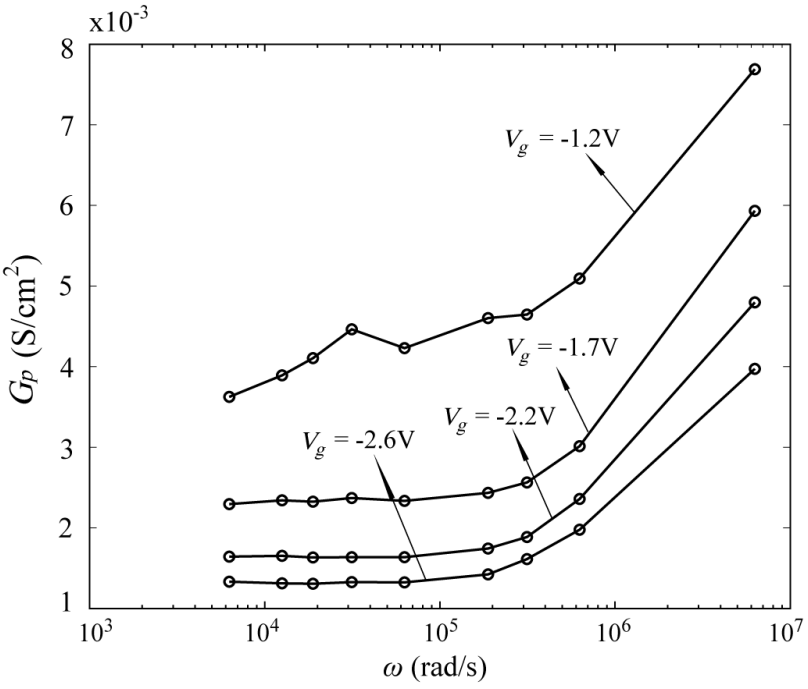

Figure 3.8: Extracted G_p data versus ω for different gate biases in inversion.

3. 3 Overall Model Fitting With Gate Voltage Stretch-out

From the quasi-static simulation (Fig. 3.1(a)), the intrinsic capacitance C_i can be extracted as a function of surface potential ψ_s. To apply it to the model for a given V_g, ψ_s needs to be determined, taking the stretch-out of V_g by the DC effect of D_{it} into account. The starting point is V_g = 0.2 V where the surface potential is obtained by matching the measured 1 MHz capacitance to the simulated capacitance. As V_g goes negative, the incremental stretch-out is calculated by

$$\Delta V_g = \Delta \psi_s \times \left(\frac{C_{ox} + C_{it} + C_i + C_d}{C_{ox}}\right) \tag{3.14}$$

point by point, where C_{it} is interface-state capacitance extracted from the dispersion at that point. In other words, the increment of surface potential of the next bias point is calculated from the ΔV_g step using the above equation. A ψ_s-V_g relation with stretch-out is then generated by integrating the C_{it} contribution of all previous bias points.

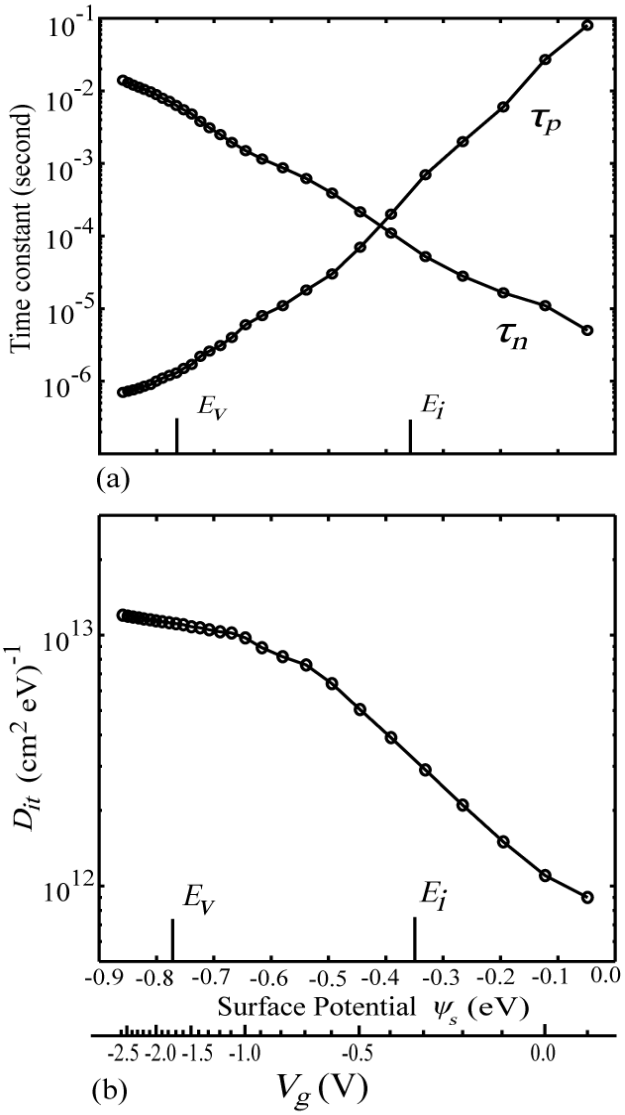

Figure 3.9: (a) Extracted τ_n and τ_p versus surface potential ψ_s and V_g (bottom x-axis). (b) Extracted interface state density (D_{it}) versus surface potential ψ_s and V_g (bottom x-axis).

The extraction results of D_{it}, τ_n, τ_p for the range of $-2.6\ \text{V} \le V_g \le 0.2\ \text{V}$ are summarized in Fig. 3.9 versus ψ_s. D_{it} rises from ~10^{12} cm^{-2}eV^{-1} near the flatband to ~10^{13} cm^{-2}eV^{-1} into the valence band. Its value on the far left of the range is estimated since only the ratio C_{it}/τ_n can be accurately determined from the G_{gr} data. τ_n and τ_p exhibit the expected trend reflecting several orders-of-magnitude change in the electron and hole

densities at the surface. While they by and large vary exponentially with ψ_s, the slopes are much slower than $\exp(\pm q\psi_s/kT)$.

The overall fitting of the multiple-frequency C_{tot}-V_g and G_{tot}-V_g data by the full interface-state model with the extracted parameters of Fig. 3.9 is shown in Fig. 3.10. Also plotted in Fig. 3.10(a) is the inversion layer capacitance C_i based on the stretched out ψ_s-V_g relation mentioned earlier. Beyond the peak of the hump toward more negative V_g, the 1 kHz C_{tot} decreases while C_i increases sharply and C_{it} stays more or less flat. The fall of the C_{tot} is attributed to the increasing τ_n, as stated before.

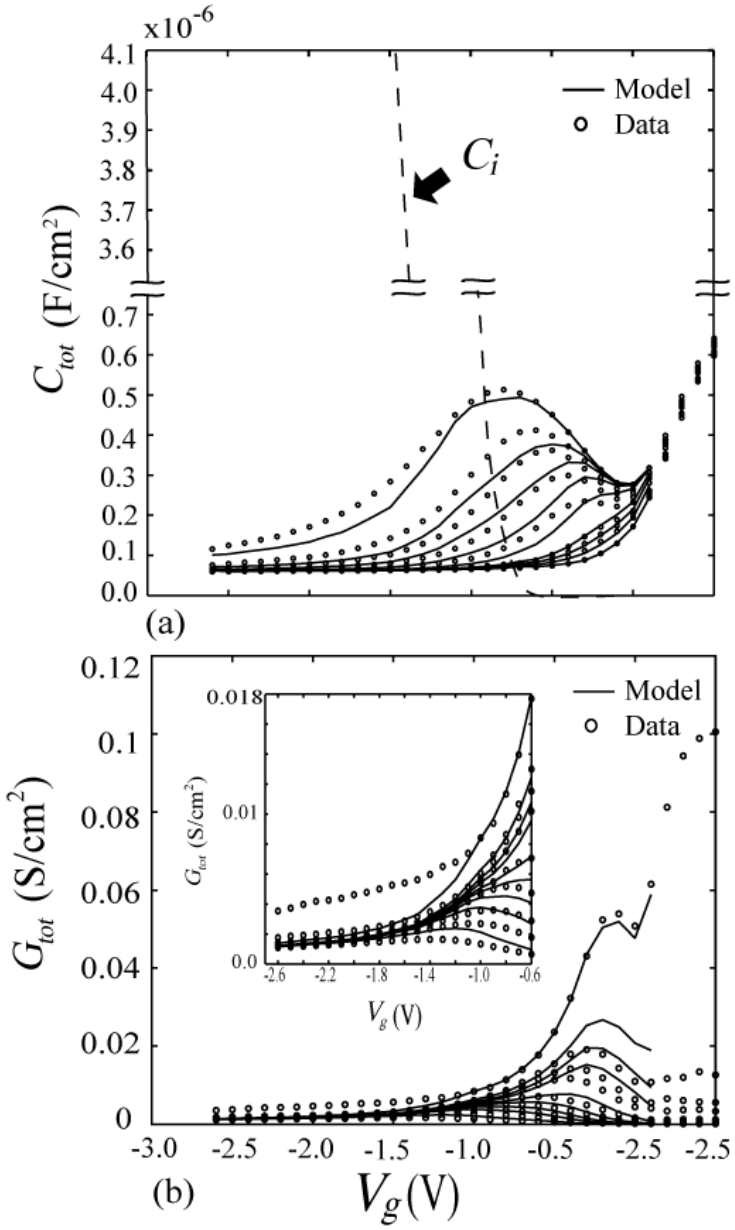

Figure 3.10: Overall model fitting of experimental (a) C_{tot}-V_g and (b) G_{tot}-V_g data.

It is informative to use the model to find out how the C-V changes from the high-frequency to the low-frequency or quasi-static characteristics, either by intrinsic generation and recombination in the bulk or by interface states. Consider the strong inversion circuit in Fig. 3.7 with $C_i > C_{ox} > C_d$. In the high frequency limit, $\omega C_d >> G_{gr}$,

C_{tot} equals C_{ox} in series with C_d. In the low frequency limit, $\omega C_i << G_{gr}$, $C_{tot} \approx C_{ox}$. For intermediate frequencies, $G_{gr}/C_i << \omega << G_{gr}/C_d$, C_{tot} is approximately the capacitive component of the serial combination of C_{ox} and G_{gr}, i.e.,

$$C_{tot} = \frac{C_{ox} G_{gr}^{\ 2}}{\omega^2 C_{ox}^{\ 2} + G_{gr}^{\ 2}} \tag{3.15}$$

Fig. 3.11 shows two sets of model generated C_{tot}-V_g plots in the intermediate frequency range. The solid curves use the D_{it} parameters in Fig. 3.9 and extend the frequency to below 1 kHz. The dashed curves are for an intrinsic MOS with $C_{it} = 0$ but at elevated temperature, for which we assume a constant $G_d = 0.002$ S/cm^2 replacing G_{gr} in Fig. 3.7. Basically, the slope of the C_{tot}-V_g curves reflects the dependence of G_{gr} or G_d on V_g. The conductance G_d from generation and recombination in the bulk is independent of V_g, hence the intrinsic C_{tot}-V_g curves (dashed) are flat. On the other hand, C_{tot} of the D_{it} case (solid) decreases toward stronger inversion because G_{gr} decreases in that direction. A positive then negative going slope of C_{tot}-V_g characteristics in inversion is thus a telltale sign of interface states.

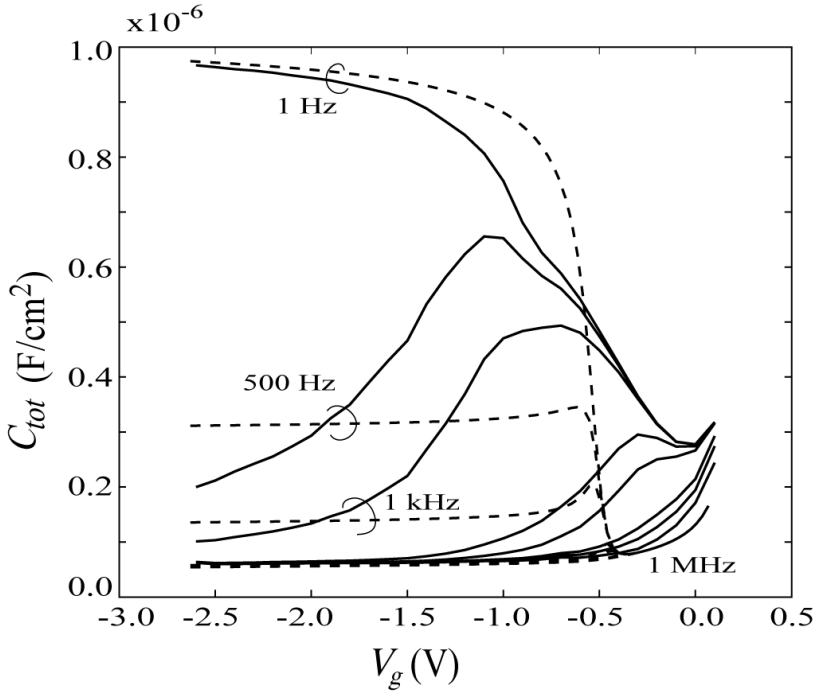

Figure 3.11: Model extension of C-V to low frequencies. Solid curves assume $G_d = 0$ and use the τ_n, τ_p and D_{it} parameters in Fig. 3.9. Dashed curves assume $D_{it} = 0$ and $G_d = 0.002$ S/cm^2.

The text of Chapter 3, in part, is a reprint of the material as it appears in "Interface-State Modeling of Al_2O_3-InGaAs MOS from Depletion to Inversion" by Han-Ping Chen, Yu Yuan, Bo Yu, Jaesoo Ahn, Paul C. McIntyre, Peter M. Asbeck, Mark J. Rodwell, and Yuan Taur, IEEE Transaction on Electron Devices, Sep., 2012. The dissertation author was the primary investigator and author of this paper.

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[3] Y. Yuan, "Non-Classical MOSFETs: Design, Modeling, and Characterization," Ph.D. dissertation in Electrical Engineering (Applied Physics), University of California, San Diego, 2012.

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Chapter 4

Bulk-Oxide Trap in High-*k* III-V MOS Capacitor

Distributed circuit model is applied in this chapter to explain the C-V and G-V dispersion of the Al_2O_3/n-InGaAs MOS capacitor in accumulation region and characterize the bulk-oxide trap density. The series resistance effect is also introduced by adding an additional resistance component to the model, explaining the well-observed upturning G_{tot} at high frequency. Other models such as distributed-transcunductance model, lumped circuit model, as well as Hasegawa model, are further examined and commented by comparing to the experimental data.

4.1 Distributed Bulk-Oxide Trap Model

4.1.1 Theoretical Basis [1, 2]

The Full-interface state model described in Chapter 3 has single τ_n and τ_p at given bias, which leads to a high-low type of transition in capacitance dispersion from low to high frequency. It cannot explain the uniform capacitance dispersion data in accumulation. Instead, such uniform dispersion has been explained by the bulk-oxide trap effect [1]. Different from interface traps, bulk-oxide traps are in the bulk dielectrics, and they exchange charges with mobile carriers in the semiconductor through tunneling; therefore, it has relatively large and wide-spreading time constants. The tunneling process in n-type MOS capacitor is schematically illustrated in Fig. 4.1.

In the static picture, consider single-level oxide traps of density N_t (cm^{-3}) at energy E_t, shown schematically in Fig. 4.2. In equilibrium, the occupation percentage is given by the Fermi-Dirac function,

$$f = \frac{1}{1+e^{(E_t - E_f)/kT}} \tag{4.1}$$

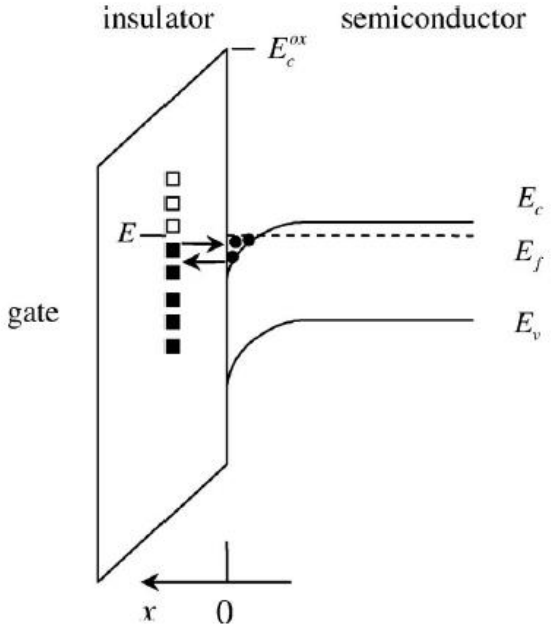

Figure 4.1: Schematic of tunneling between bulk-oxide traps in the gate insulator and conductance band of the semiconductor [1].

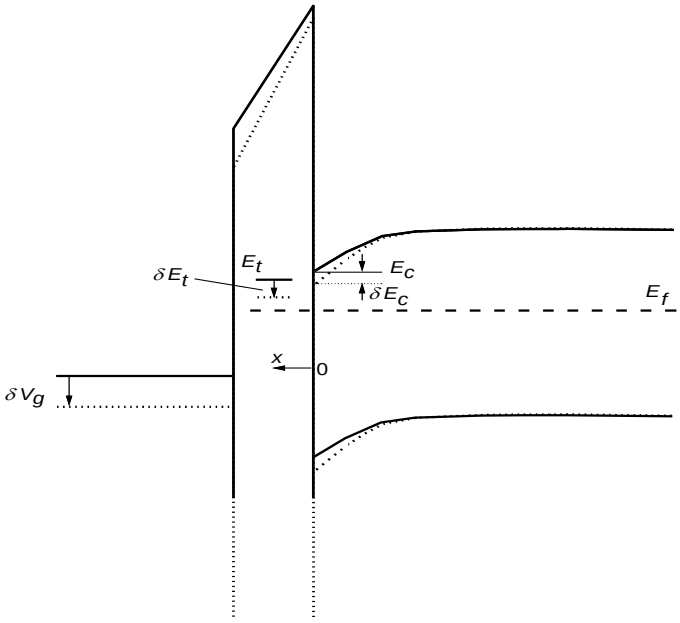

Figure 4.2: Band diagram of MOS capacitor with oxide traps at E_t and x. The dotted lines show how the bands change with a slight increase of gate voltage [2].

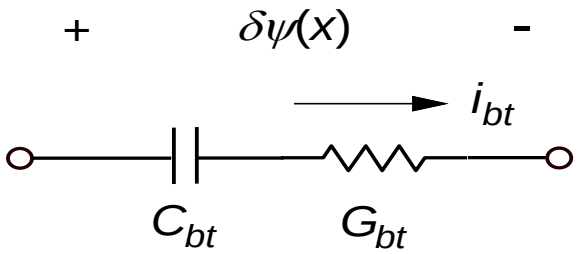

Figure 4.3: Serial circuit representation of a single-level trap element. C_{bt} and G_{bt} are capacitance and conductance per volume.

When a slow, incremental gate voltage changes the local potential at x by $\delta\psi$ (x), E_t changes by $\delta E_t = -q\delta\psi$ (x), and the trapped charge per volume changes by $\delta Q_t = qN_t(df/dE_t)\delta E_t = (q^2/kT)N_t f (1 - f) \delta\psi(x)$. Note that δQ_t is proportional to the local potential change, $\delta\psi(x)$, not the surface potential change $\delta\psi_s$ at $x = 0$. The static effect of the traps is then equivalent to a capacitance (Fig. 4.3)

$$C_{bt} = \frac{q^2}{kT} f(1-f)N_t \tag{4.2}$$

Based on Shockley-Read-Hall theory [3] applied to border traps, the capture rate for traps at x is

$$r_c = c_n n e^{-2\kappa x} N_t (1-f) \tag{4.3}$$

where n is the conduction band electron density at the semiconductor surface, e-2κx is the attenuation factor from tunneling, and cn is the capture probability in cm3/s often expressed as σvth where σ is the trap cross-section area and vth is the electron thermal velocity. κ is the attenuation coefficient for an electron wave function of energy E decaying under an energy barrier E_C^{ox} > E

$$\kappa = \sqrt{2m^*(E_C^{OX} - E)}/\hbar \tag{4.4}$$

m^* is the electron effective mass in the dielectric film and E_C^{ox} is the energy of the top of the dielectric barrier, as indicated in Fig. 4.1. The emission rate is

$$r_e = e_n N_t f \tag{4.5}$$

where en is the emission probability in s^{-1}. In equilibrium, $r_c = r_e$, therefore,

$$\frac{e_n}{c_n n e^{-2\kappa x}} = \frac{1-f}{f} = e^{(E_t - E_f)/kT} \tag{4.6}$$

n can be expressed in terms of the conduction band effective density of states N_c as

$$n = N_c e^{-(E_c - E_f)/kT} \tag{4.7}$$

Substituting $c_n = \sigma v_{th}$ and Eq. (4.6) into Eq. (4.5) yields

$$\frac{e_n}{\sigma v_{th} e^{-2\kappa x}} = N_c e^{-(E_c - E_t)/kT} \tag{4.8}$$

The right side is simply the Boltzmann factor for the probability of electron emission from energy E_t to energy E_c. In Appendix I of Nicollian and Brews [3], e_n is

treated as a constant because for interface state traps at x = 0, $E_c - E_t$ is fixed. For oxide traps at x, however, $\delta E_t \neq \delta E_c$ (Fig. 4.1), the change of en must be taken into account.

Consider a sudden step δV_g that changes the E_t of oxide traps at x by δE_t and E_c by δE_c. From Eqs. (4.7) and (4.8),

$$\delta n / n = -\delta E_c / kT \tag{4.9}$$

and

$$\delta e_n / e_n = -(\delta E_c - \delta E_t) / kT \tag{4.10}$$

These give rise to instantaneous changes in Eqs. (4.3) and (4.5). Note that the trap occupancy factor f has not changed yet and remains at the value prior to the step. For the case shown in Fig. 1, $\delta E_t < \delta E_c < 0$, the capture rate r_c increases and the emission rate re decreases instantaneously. The net charging current is

$$\begin{aligned} i_{bt} &= q(\delta r_c - \delta r_e) = q c_n N_t (1 - f) e^{-2\kappa x} \delta n - q N_t f \delta e_n \\ &= q N_t f e_n (\delta n / n - \delta e_n / e_n) = -q N_t f e_n \delta E_t / kT \end{aligned} \tag{4.11}$$

The middle step made use of the relation $r_c = r_e$ before the voltage step. The instantaneous drop of local potential $\delta\psi(x) = -\delta E_t/q$ is entirely over G_{bt} in Fig. 4.3. So $G_{bt} = i_{bt}/ \delta\psi$ (x) is a simple conductance,

$$G_{bt} = (q^2 / kT) N_t f e_n \tag{4.12}$$

Alternatively, $G_{bt} = \sigma v_{th} n e^{-2\kappa x}(q^2/kT)N_t(1-f)$, and C_{bt} and G_{bt} are related by time constant $\tau(x)$ [4],[5]

$$\tau(x) = C_{bt}/G_{bt} = f\tau_0 e^{2\kappa x} \tag{4.13}$$

, which is a function of depth x. Here, $\tau_0 = (n_s \sigma v_{\text{th}})^{-1}$ is the time constant of the traps at the interface x=0. Note that here a time-domain approach to derive C_{bt} and G_{bt} is used. It is simpler and more physical than the frequency-domain approach in Appendix I of Nicollian and Brews [3] in arriving at the same results.

If the density per volume per energy of bulk-oxide traps is N_{bt} in units of $\text{cm}^{-3}\text{Joule}^{-1}$, then C_{bt} is re-written to ΔC_{bt} as [3, 4]

$$\Delta \text{C}_{\text{bt}}(E,x) = \frac{f_0(1-f_0)q^2 N_{bt}}{kT}\Delta E \Delta x \tag{4.14}$$

and

$$\Delta \text{C}_{\text{bt}}(E,x)/\Delta \text{G}_{\text{bt}}(E,x) = \tau(x) = f_0\tau_0 e^{2\kappa x} \tag{4.15}$$

To integrate for a continuous energy distribution of bulk-oxide traps, the serial connection of $\Delta C_{\text{bt}}(E, x)$ and $\Delta G_{\text{bt}}(E, x)$ at a given x must be first converted to a parallel combination of incremental admittance. Because the factor $f_0(1 - f_0)$ is sharply peaked at $E = E_f$, κ in (4.4) is set to be a constant with $E = E_f$ in the integration. The total incremental admittance at x is then

$$\Delta Y_{bt}(x) = \int_E \frac{1}{\frac{1}{j\omega \Delta C_{bt}(E,x)} + \frac{1}{\Delta G_{bt}(E,x)}} = \frac{q^2 N_{bt} \ln(1 + j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}} \Delta x \tag{4.16}$$

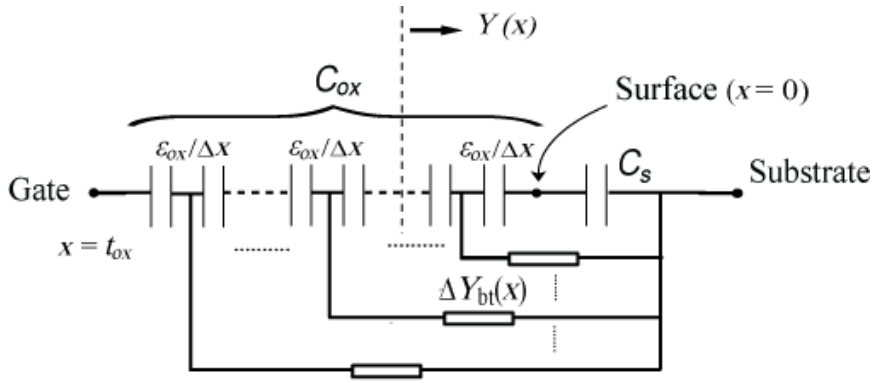

Figure 4.4: Equivalent circuit for bulk-oxide traps distributed over the depth of the insulator [1].

If we define $Y(x)$ to be the equivalent admittance at a point x looking into the semiconductor in Fig. 4.4, the recursive nature of the distributed circuit gives the admittance of the next point $x+\Delta x$ as

$$Y(x + \Delta x) = \Delta Y_{bt} + \frac{1}{\frac{\Delta x}{j\omega\varepsilon_{ox}} + \frac{1}{Y(x)}} \tag{4.17}$$

Substituting (4.17) for $\Delta Y_{bt}(x)$, the first-order terms in Δx then yield a differential equation for $Y(x)$

$$\frac{dY}{dx} = \frac{-Y^2}{j\omega\varepsilon_{ox}} + \frac{q^2 N_{bt} \ln(1 + j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}} \tag{4.18}$$

The boundary condition is Y (x = 0) = $j\omega C_s$. Eq. (4.18) is numerically solved to obtain the total admittance seen by the gate:

$$Y(x=t_{ox}) \equiv G_{tot} + j\omega C_{tot} \tag{4.19}$$

4.1.2 Correlations of the Model with the C-V and G-V Dispersion Data

A typical example of the solutions C_{tot} versus ln ω and G_{tot} versus ω is given in Fig. 4.3. In the high frequency limit, $\omega\tau_0 \geq 1$, none of the bulk-oxide traps respond to the ac signal and C_{tot} is equal to C_{ox} in series with C_s as expected. For the measurement frequencies of 1 kHz–1 MHz, $1.4 \times 10^{-6} < \omega\tau_0 < 1.4 \times 10^{-3}$, C_{tot} linearly varies with ln(1/ω), and G_{tot} linearly varies with ω, i.e., $G_{\text{tot}}/\omega \approx$ constant. Both are consistent with the data trends in Fig. 4.1. Constant G_{tot}/ω reflects the fact that, for a given gate bias, response of bulk-oxide traps spans a wide spectrum of frequencies due to their depth distribution, i.e., a clear distinction from conventional interface traps [3]. For a given frequency of $\omega < 1/\tau_0$, the depth of traps that respond to the small signal can be estimated by letting the factor $\omega\tau_0 e^{2\kappa x}$ in (18) equal unity, i.e., $x \sim (2\kappa)^{-1} \ln(1/\omega\tau_0)$. This is typically in the range of 0.1–1 nm.

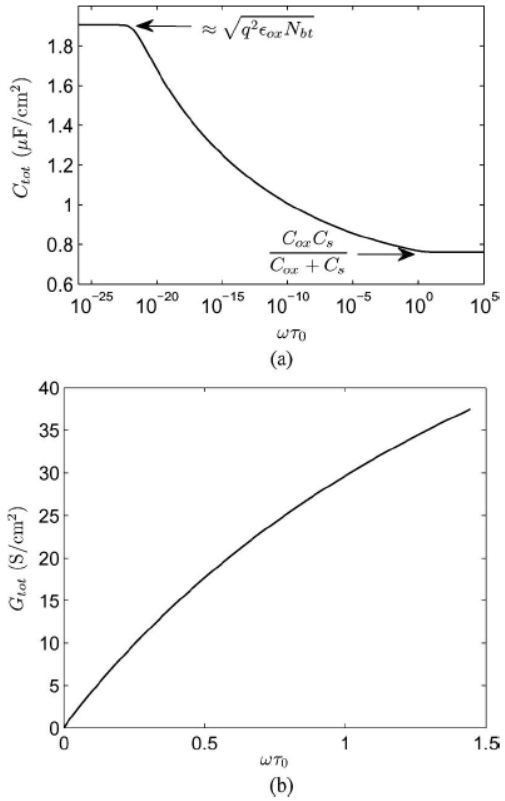

Figure 4.5: Example of numerical solution to (18): (a) real and (b) imaginary parts of Y ($x = t_{ox}$) versus $\omega\tau_0$ with $N_{bt} = 4.2 \times 10^{19}$ cm^{-3} eV^{-1} and $\tau_0 = 2.3 \times 10^{-10}$ s [1].

In Fig. 4.6, the experimental capacitance and conductance versus frequency data in strong accumulation in Fig. 3.1 (Al_2O_3/n-InGaAs at V_g = 2.9 V) are compared with model calculations. For model parameters, semiconductor capacitance C_s is chosen such that the serial combination of C_{ox} and C_s gives C_{tot} slightly below the measured 1-MHz capacitance at V_g = 2.9 V. κ is calculated from (4.2) with $m* = 0.5m0$ and $E_C^{ox} - E = 1.99$ eV. Both the slopes of Ctot versus ln(1/ω) and Gtot versus ω are sensitive to bulk-oxide trap density N_{bt}. By choosing a single fitting parameter, uniform $N_{bt} = 4.2 \times 10^{19}$ cm^{-3} eV^{-1}, good agreement is achieved between the model and the measured C_{tot} and G_{tot} data from 1 kHz to 1 MHz in Fig. 4.6(a) and (b). Parameter τ_0 is chosen so that C_{tot} is consistent with $C_{ox}C_s/(C_{ox} + C_s)$ at a frequency $\omega\tau_0 \rightarrow 1$, where the traps have no effect

[see lower right of Figs. 4.5(a)]. For an assessment of sensitivity to the fitting parameters, Fig. 4.6 also shows two curves (dashed) calculated with 10% variation of N_{bt} for best fitting. A more detailed discussion can be found in the original paper by Yu et al. [1].

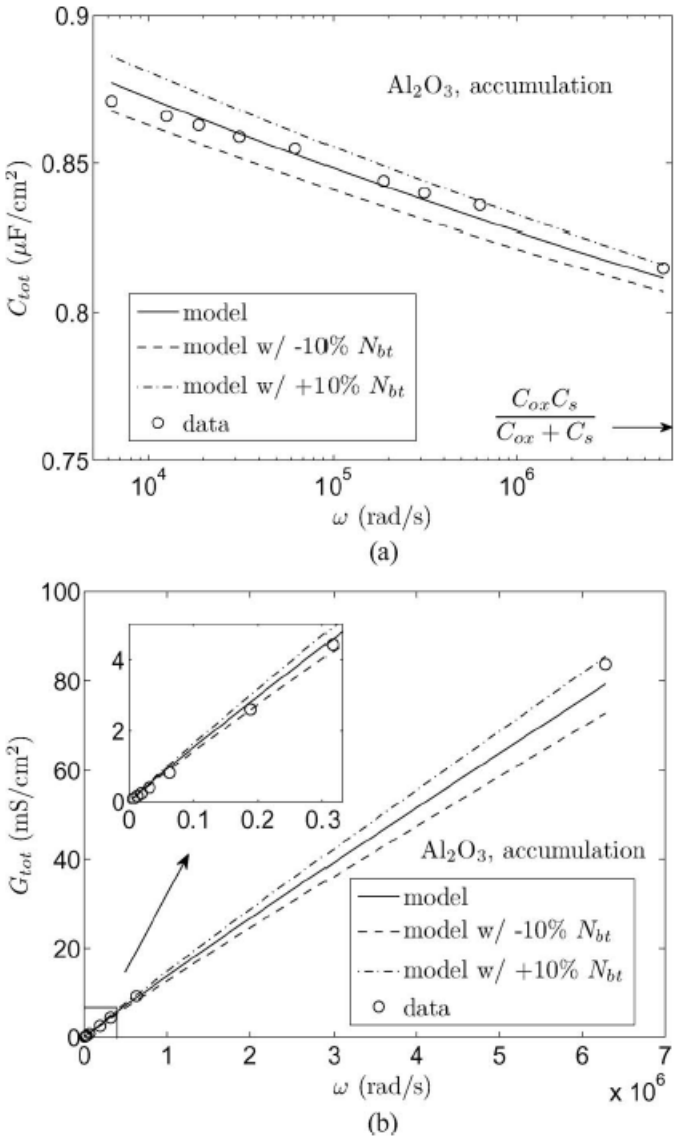

Figure 4.6: Al_2O_3 MOS experimental (a) $C_{tot}(\omega)$ and (b) $G_{tot}(\omega)$ dispersion data (open circles) at V_g = 2.9 V in Fig. 3.1 compared with those calculated from the distributed bulk-oxide trap model (solid lines). A single bulk-oxide trap density N_{bt} = 4.2 × 10^{19} cm^{-3} eV^{-1} is assumed in both $C_{tot}(\omega)$ and $G_{tot}(\omega)$ calculations. The rest of the model parameters are C_{ox} = 1.06 μF/cm^2, t_{ox} = 5 nm, C_s = 2.7 μF/cm2, κ = 5.1 nm^{-1}, and τ_0 = 2.3 × 10^{-10} s [1].

Another "Distributive-Transconductance Model" has been proposed in a recent publication [6] for bulk-oxide trap modeling. The authors derived a distributed transconductance g_m for the equivalent circuit of oxide traps in an MOS capacitor. The border trap elements at x are represented as dependent current sources, $g_m \Delta x \delta\psi_s$, where $\delta\psi_s$ is the small-signal modulation of the surface potential at $x = 0$, instead of the local potential in the original admittance-based model. The omission of δe_n in [6] led its authors to the erroneous transconductance model that i_{bt} in Eq. (4.11) only comes from δn, and therefore is proportional to δE_c or $\delta\psi_s$. In practice, the transconductance model produces very different results from the admittance model in [1], as seen in the example in Fig. 4.7. The transconductance model not surprisingly yields lower C_{tot} and dispersion than the admittance model. The errors are significant even at high frequencies ($\omega\tau_0 \geq 10^{-5}$) where the dispersion comes from border traps within 1 nm of the interface. The discrepancy grew worse with a higher semiconductor capacitance C_s. An odd consequence of the transconductance model is that there is a crossover frequency below which C_{tot} goes down as C_s goes up. In the limit of $C_s \rightarrow \infty$, $\delta\psi_s = 0$, the dispersion from the transconductance model disappears altogether and C_{tot} becomes a flat line at C_{ox}. The admittance model [1], on the other hand, displays none of such unreasonable behavior.

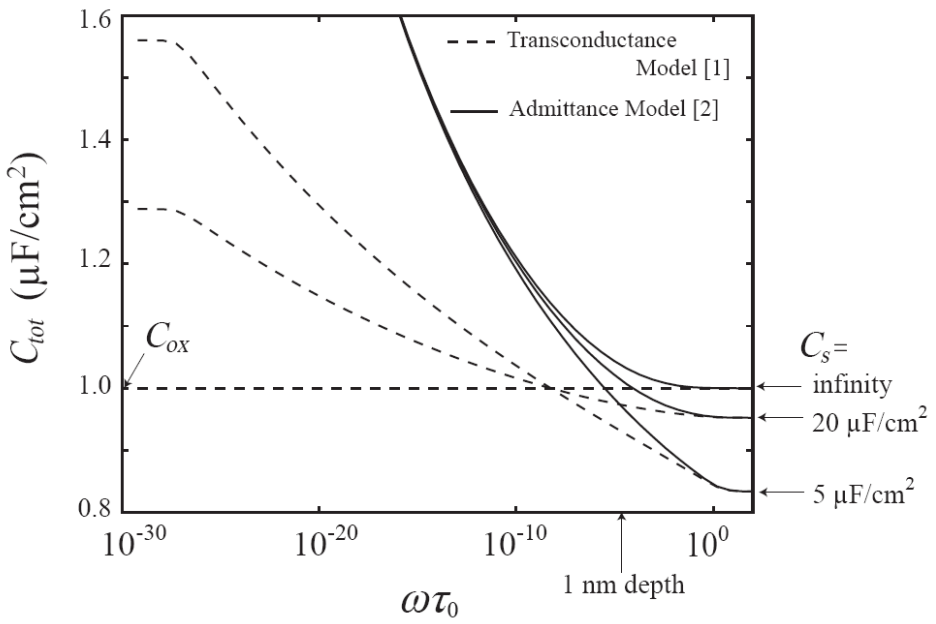

Figure 4.7: Comparison between the transconductance model and admittance model. The common parameters are C_{ox} = 1 μF/cm^2, κ = 5.1 nm^{-1}, $\varepsilon_{ox}/\varepsilon_0$ = 7, N_{bt} = 2×10^{20} cm^{-3}eV^{-1}. Three C_s values are used as indicated to the right. The 1 nm border trap depth is estimated from $x \sim (2\kappa)^{-1}\ln(1/\omega\tau_0)$ [1].

4.1.3. Combination of the Interface Trap and the Bulk-Oxide trap models

While the C_{tot}-V_g and G_{tot}-V_g data in Chapter. 2 for most of the −2.6 V ≤ V_g ≤ 0.2 V range are fitted rather well by the interface-state model, the fitting at either end of the range can be further improved by incorporating bulk-oxide traps in the interface-state model. Low frequency C_{tot} near V_g = 0.2 V fits better by adding electron bulk-oxide traps, and high frequency G_{tot} near V_g = −2.6 V fits better by adding hole bulk-oxide traps [10].

The combined bulk-oxide trap and interface-state equivalent circuits are shown in Fig. 4.8. The distributed electron traps in the bulk oxide are connected to the n-type substrate in Fig. 4.8 (a). The distributed hole traps in the bulk oxide are connected through G_{gr}, along with C_i in Fig. 4.8 (b). The incremental trap elements ΔY_{bt} are

described in eq. (4.16). Similar expression applies for hole bulk-oxide traps by replacing τ_n with τ_p and the electron barrier height with the hole barrier height. The distributed circuit in Fig. 4.8 (a) can be solved numerically by alternating serial and parallel combinations. The circuit in Fig. 4.8 (b) can be solved numerically by successive □-to-Y impedance transformations. The Matlab codes for both circuit model are in the Appendix.

The solid curves in Fig. 4.9 are fittings of the C_{tot} and G_{tot} data at $V_g = 0$ with only the interface-state model. The D_{it} was chosen for the model to match the 1 kHz C_{tot}, which left significant discrepancies with the next few points. By incorporating electron bulk-oxide traps in the interface-state model, much improved fitting is achieved for the entire frequency range (dashed curves). As noted in the caption, a D_{it} lower than that of the interface-state only model is used in the combined model. As V_g becomes more negative, D_{it} increases while the contribution from bulk-oxide traps diminishes due to increasing τ_n. The data can be well fitted with interface states only.

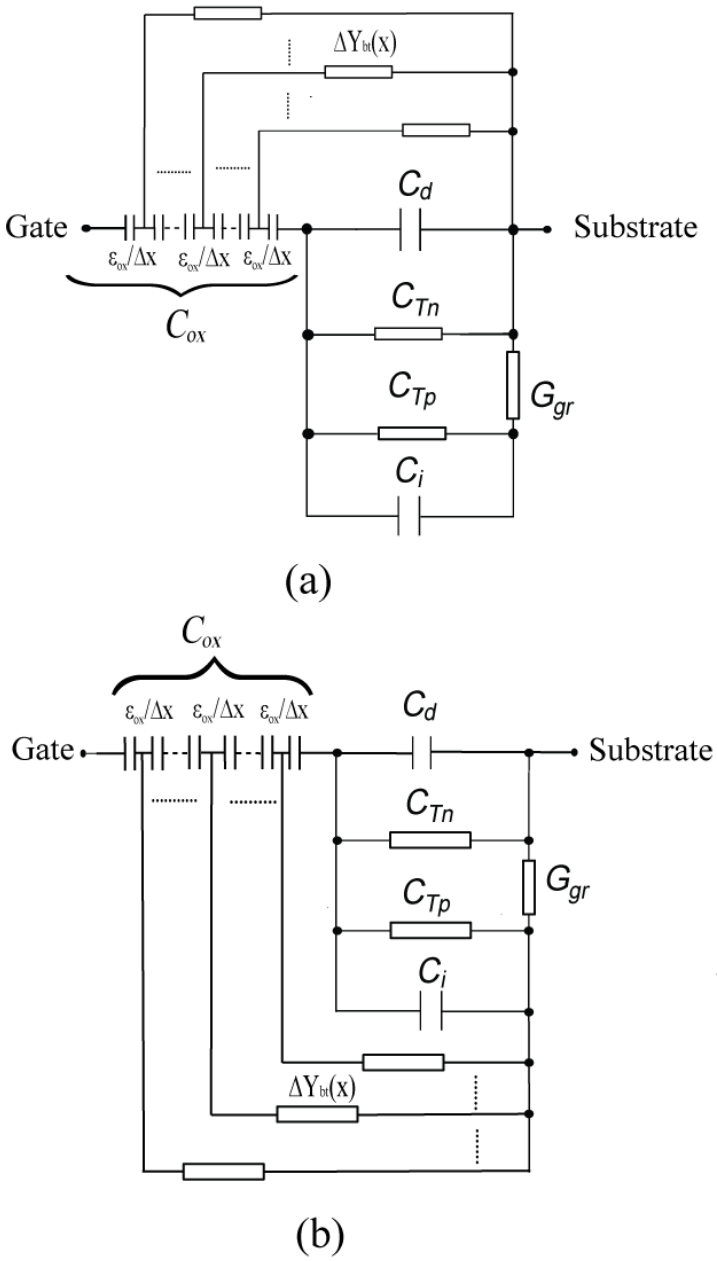

Figure 4.8: Equivalent circuits with (a) the bulk-oxide electron trap full interface state model and (b) the bulk-oxide hole trap full interface state model [10].

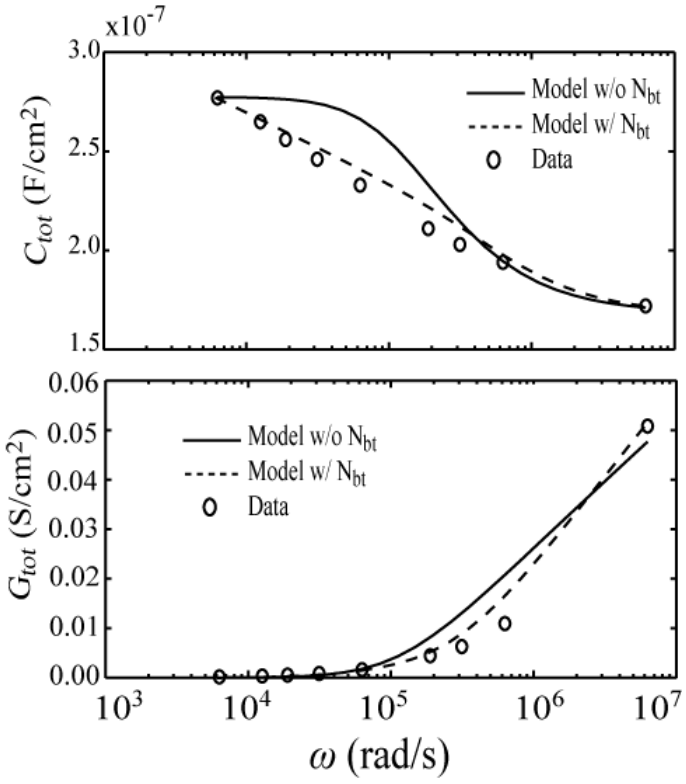

Figure 4.9: C_{tot} and G_{tot} fitting at V_g = 0V with and without bulk-oxide electron traps. For solid lines without bulk-oxide traps, C_{it} = 1.76×10^{-7} F/cm^2 C_i = 9.00×10^{-15} F/cm^2, C_d = 2.0×10^{-7} F/cm^2, τ_n = 1.1×10^{-5} s and τ_p = 2.7×10^{-2} s. For dashed lines with bulk-oxide traps, C_{it} = 4.00×10^{-8} F/cm^2, C_i= 9.30×10^{-15} F/cm^2, C_d = 2.0×10^{-7} F/cm^2, τ_n = 3.0×10^{-6} s, τ_p = 2.7×10^{-2} s, N_{bt} = 2×10^{19} cm^{-3} and κ = 6.4×10^{7} cm^{-1}.

The discrepancy of G_{tot}(1 MHz) from the D_{it}-only model at large negative V_g [inset of Fig. 3. 10(b) in Chapter 3] is much more difficult to explain. Fig. 4.10 shows that inclusion of bulk-oxide hole traps in the interface-state model [Fig. 4.8(b)] tends to move G_{tot}(1 MHz) up in the right direction. However, to fully account for the observed data, unreasonably low valence band barrier and high hole trap density would have to be assumed in the model.

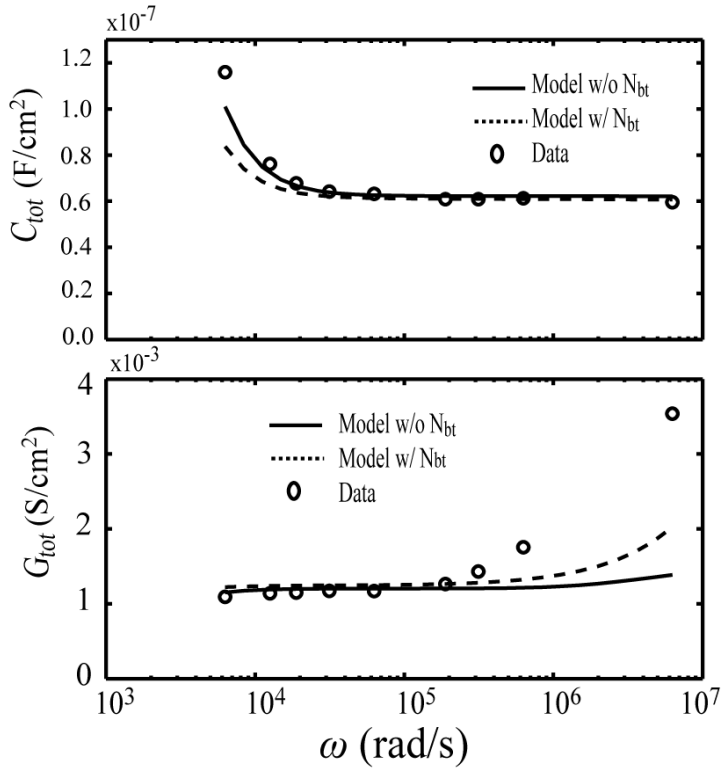

Figure 4.10: C_{tot} and G_{tot} fitting at V_g = -2.6 V with and without bulk-oxide hole traps. For solid lines without bulk-oxide traps, $C_{it} = 1.92\times10^{-6}$ F/cm^2 $C_i = 8.80\times10^{-6}$ F/cm^2, $C_d = 6.4\times10^{-8}$ F/cm^2, $\tau_n = 1.4\times10^{-2}$ s and $\tau_p = 7.0\times10^{-7}$ s. For dashed lines with bulk-oxide traps, $C_{it} = 1.92\times10^{-6}$ F/cm^2, $C_i = 4.50\times10^{-6}$ F/cm^2, $C_d = 6.4\times10^{-8}$ F/cm^2, $\tau_n = 2.8\times10^{-2}$ s, $\tau_p = 1.0\times10^{-10}$ s, $N_{bt} = 5\times10^{20}$ cm^{-3} and $\kappa = 3.0\times10^{7}$ cm^{-1}.

4.1.4. Distributed Model with Series Resistance

Although the distributed model works very well in the previous sections, there are cases that the conductance data is higher than model prediction [11]. An example is shown in Fig. 4.11, from a MOS capacitor with 7 nm Al_2O_3 and n-type InGaAs (the full C-V curves can be found in Fig. 5.1). The figure indicates that the distributed model cannot capture the G-V dispersion accurately at high frequency end, where the measured

data exhibit a roll-up away from the linear trend. Such effect is explained by the series resistance in this section.

For the purpose of extracting series resistance, the accumulation region is emphasized. Fig. 4.12 shows the equivalent model of distributed model with series resistance R_s without considering oxide leakage.

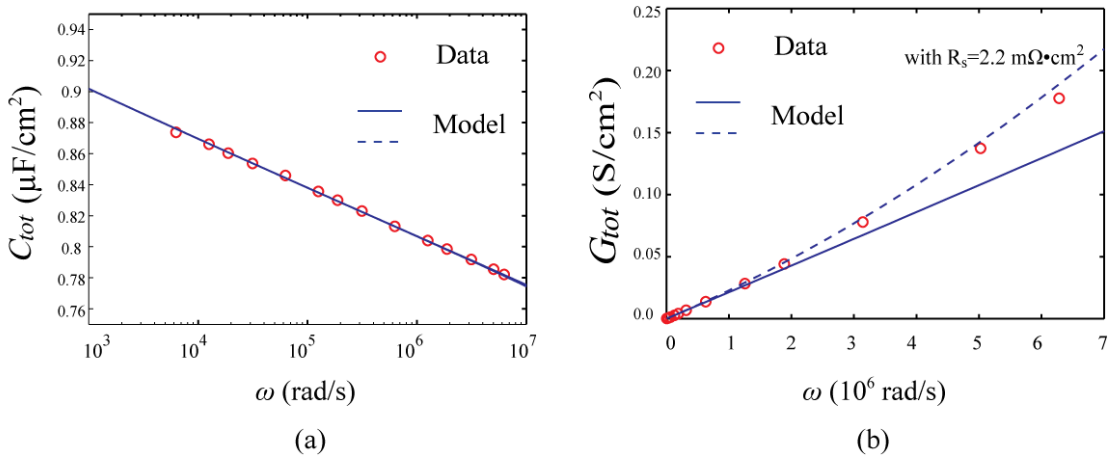

Figure 4.11: (a) $C_{tot}(\omega)$ and (b) $G_{tot}(\omega)$ dispersion data (open circles) at V_g = 2.5 V in Fig. 5.1 compared with those calculated from the distributed bulk-oxide trap model (solid lines). A single bulk-oxide trap density N_{bt} = 6.6 × 10^{19} cm^{-3} eV^{-1} is assumed in both $C_{tot}(\omega)$ and $G_{tot}(\omega)$ calculations. The rest of the model parameters are C_{ox} = 0.94 μF/cm^2, t_{ox} = 7 nm, C_s = 2.8 μF/cm2, κ = 3.8 nm^{-1}, and τ_0 = 1.7 × 10^{-10} s. The dashed curve is with R_s= 2.2 mΩ·cm^2.

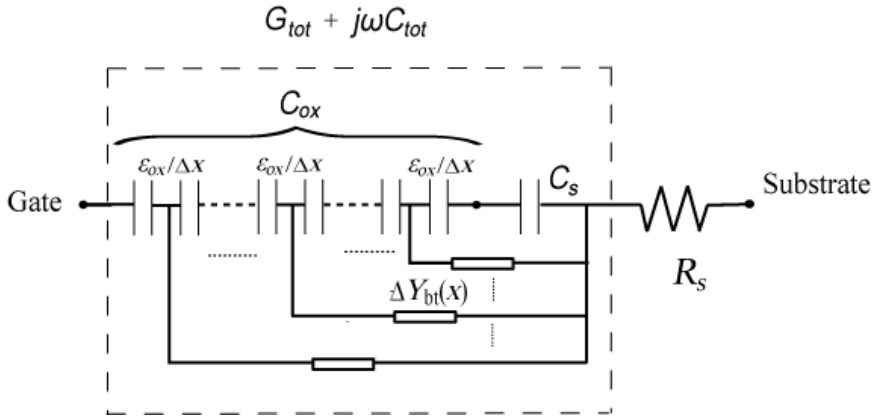

Figure 4.12: Equivalent distributed circuit model with series resistance.

If we define $G_{tot} + j\omega C_{tot}$ as the admittance of intrinsic MOS with the distributed bulk-oxide trap, i.e. the part enclosed by the dashed box in Fig. 4.12, then the equivalent circuit yields the expression for the total admittance $G_m + j\omega C_m$ measured between gate and substrate nodes:

$$G_m = \frac{G_{tot}(1 + R_s G_{tot}) + \omega^2 C_{tot}^{\ 2} R_s}{(1 + R_s G_{tot})^2 + \omega^2 C_{tot}^{\ 2} R_s^{\ 2}} \tag{4.20}$$

$$C_m = \frac{C_{tot}}{(1 + R_s G_{tot})^2 + \omega^2 C_{tot}^{\ 2} R_s^{\ 2}} \tag{4.21}$$

Within the general frequency range for C-V measurement, $R_s G_{tot} << 1$ and $\omega C_{tot} R_s << 1$ are valid assumptions for the III-V MOS device with normal to low bulk-oxide trap density, and series resistance. With these two assumptions, C_m can be simplified to $C_m \simeq C_{tot}$, and

$$G_m = G_{tot} + \omega^2 C_m^{\ 2} R_s \tag{4.22}$$

It is known that in the presence of bulk-oxide trap, G_{tot} varies linearly with ω, Eq. (4.22) then consists of one term proportional to ω and a term proportional to ω^2. The R_s term can be appreciable at 1 MHz if $\omega C_m R_s$, although $<<1$, becomes comparable to $G_{tot}/(\omega C_m)$ which is also $\ll 1$. This explains the upturn of Gm against ω in Fig. 4.11(b). One can then extract R_s as the slope of the $G_m/(\omega C_m^2)$ against ω curve.

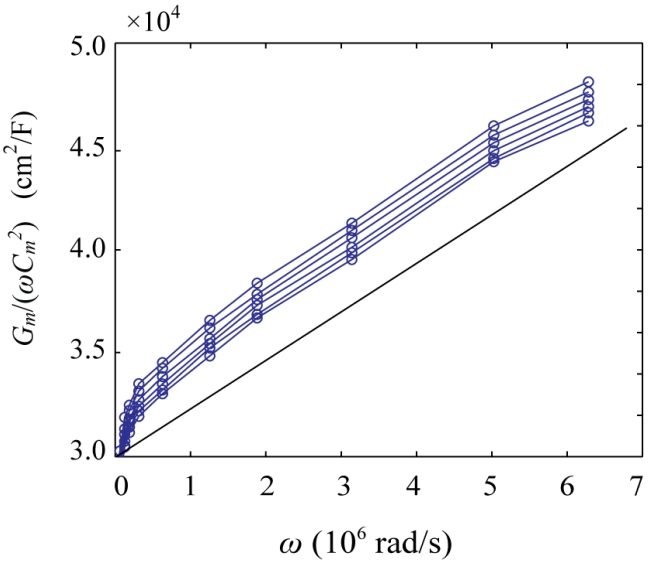

Figure 4.13: $G_m/(\omega C_m^2)$ against ω for R_s extraction: thick solid line represents slope of 2.2 mΩ·cm^2.

In Fig. 4.13, the measured data are coverted to $G_m/(\omega C_m^2)$ and plotted against ω in the linear scale in accumulation, for V_g from 2.0 V to 2.5 V in accumulation. It can be seen that the curves have strong frequency dependence, indicating that the parasitic series resistnace is large enough to be extracted. Besides, they exhibit almost linear characteristics for the high frequency end as predicted by Eq. (4.22). Most importantly, the slope is bias independent in accumulation, which is consistant with the series resistance assumption.

The thick solid line with as slope of 2.2×10^{-3} Ω·cm^2 in Fig. 4.13 is to estimate the series resistance. The dashed curves in Fig. 4. 11 are the fittings with R_s being considered. It can be seen that the upturning of G_m is captured by the model, while C_m remain unaffected. In Eq. (4.21), if R_s is further larger, $\omega C_{tot} R_s$ can be greater than unity, and C_m can also be affected that it drops at high frequency. It becomes a well-known effect explained by a simple R-C branch circuit.

4.2 Comparison of Bulk-Oxide Trap Models: Lumped Versus Distributed Circuit

4. 2. 1 Model Formulation

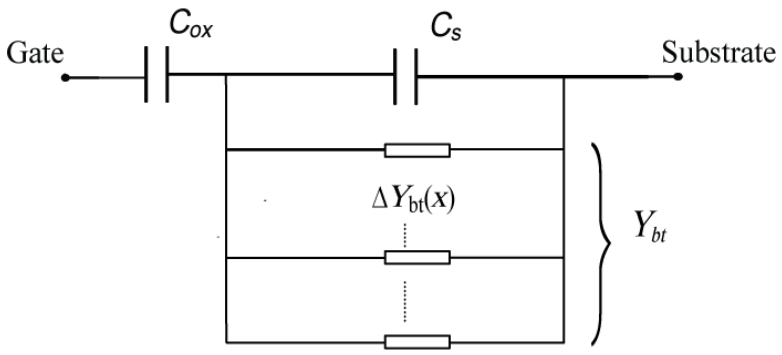

Figure 4.14: Lumped Bulk-Oxide trap model

Besides the distributed circuit model in the previous sections, another type of bulk-oxide trap models has been employed in the community: lumped circuit model. It is also based on charging and discharging of traps at varying depths from the interface by tunneling to and from the semiconductor. In the lumped-circuit model, originally proposed by Heiman and Warfield [4] and then by Preier [5], all the trap admittances are connected at the interface in parallel with the semiconductor capacitance [Fig. 4.14]. Later, Hasegawa and Sawada [7] considered a special case of Preier's model: that with an exponential distribution of trap density decaying away from the interface. The traps were attributed to a thin disordered layer at the semiconductor-oxide interface. In the distributed model [1], the physical location of the oxide trap is taken into account by

connecting each admittance element of the traps to the interface through a partitioned oxide capacitance [Fig. 4.3]

For the lumped circuit model in Fig. 4.14, one simply integrate ΔY_{bt} in Eq. (4.16) over x to obtain [12]

$$Y_{bt} = \int_0^{t_{ox}} \frac{q^2 N_{bt} \ln(1 + j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}} dx \tag{4.23}$$

where t_{ox} is the oxide thickness. The total MOS admittance is then the serial combination of $j\omega C_{ox}$ and $Y_{bt} + j\omega C_s$ from Fig. 4.13. It is different from distributed circuit model based on eq. (4.18).

It should first be pointed out that the lumped-circuit model is inherently inconsistent as it on one hand assumes carriers tunneling into traps at $x \neq 0$, while on the other hand places all the trap admittance at $x = 0$. In contrast, the distributed-circuit model is physically consistent in that regard.

Fig. 4.15 compares the $C_{tot}(\omega)$ and $G_{tot}(\omega)$ (inset) computed from the two models for a typical set of parameters listed in the caption. At $\omega\tau_0 > 1$, both models give an intrinsic $C_{tot} = C_{ox}C_s/(C_{ox}+C_s)$ with no trap contribution. G_{tot} versus ω from the two models are only slightly different. The key difference between the models is in C_{tot} below $\omega\tau_0 \sim 10^{-2}$. In the lumped-circuit model, C_{tot} can never exceed C_{ox} because all the trapped charge is placed at the interface, at distance tox from the gate. In the distributed-circuit model, however, C_{tot} can exceed C_{ox} because the trapped charge is distributed in the oxide, less than tox away from the gate. Note that the curvatures of C_{tot} versus log ω are

very different between the two models below $\omega\tau_0 \sim 10^{-2}$, a key distinction further stressed later.

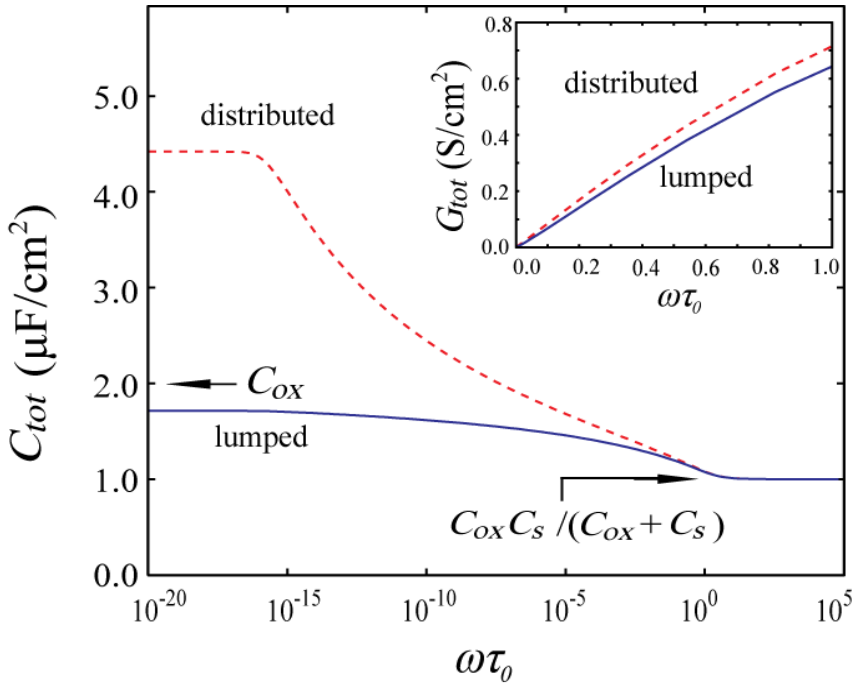

Figure 4.15: C_{tot} and G_{tot} (inset) dispersion computed from the lumped circuit model (solid) and the distributed circuit model (dashed). The parameters are $N_{bt} = 2\times10^{20}$ cm^{-3}eV^{-1}, $C_{ox} = C_s = 2$ μF/cm2, $\tau_0 = 10^{-7}$ s, $\varepsilon_{ox} = 7\varepsilon_0$, and $\kappa = 6\times10^7$ cm^{-1} for both models

4. 2. 2 Comparison of the Lumped Model to the Distributed Circuit Model

Fig. 4.16 shows the multiple frequency C-V curves measured from a Pd/Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOS capacitor. It is fabricated under similar processing procedures as in Ref. [8]. The epitaxial 0.5 μm p-$In_{0.53}Ga_{0.47}As$ with Be doping (1×10^{17}cm^{-3}) grown on p+InP substrate was initially covered with a protective amorphous As2 layer to protect the channel surface from oxidation. The As2 layer was thermally desorbed at 460°C in-situ in a high vacuum atomic layer deposition (ALD) chamber prior to oxide deposition.

The 45 cycles of ALD-Al_2O_3 was deposited at a substrate temperature of 270°C, using trimethylaluminum precursor and water vapor oxidant. Afterwards, 50nm palladium gate metal was deposited by thermal evaporation through a shadow mask. The sample was annealed in forming gas for 30 minutes at 400°C after the gate metal deposition.

Also plotted in Fig. 4.15 are ideal, Sentaurus simulated quasistatic C-Vs with quantum effects [9] for three C_{ox} values. Both the heavy and the light hole bands in $In_{0.53}Ga_{0.47}As$ are considered in the Schrödinger solver ($m_{hh} = 0.46m_0$, mlh = $0.05m_0$). These are for later discussions. As it is discussed in Chapter 3, the C-V humps near V_g = 0.75 V are due to interface states [10], not bulk-oxide traps.

It is often observed that for Al_2O_3/InGaAs MOS, p-type C-V exhibits more border trap dispersion in accumulation than n-type C-V [1]. This is indication of a higher density of hole oxide traps at the valence band energy than electron oxide traps at the conduction band energy.

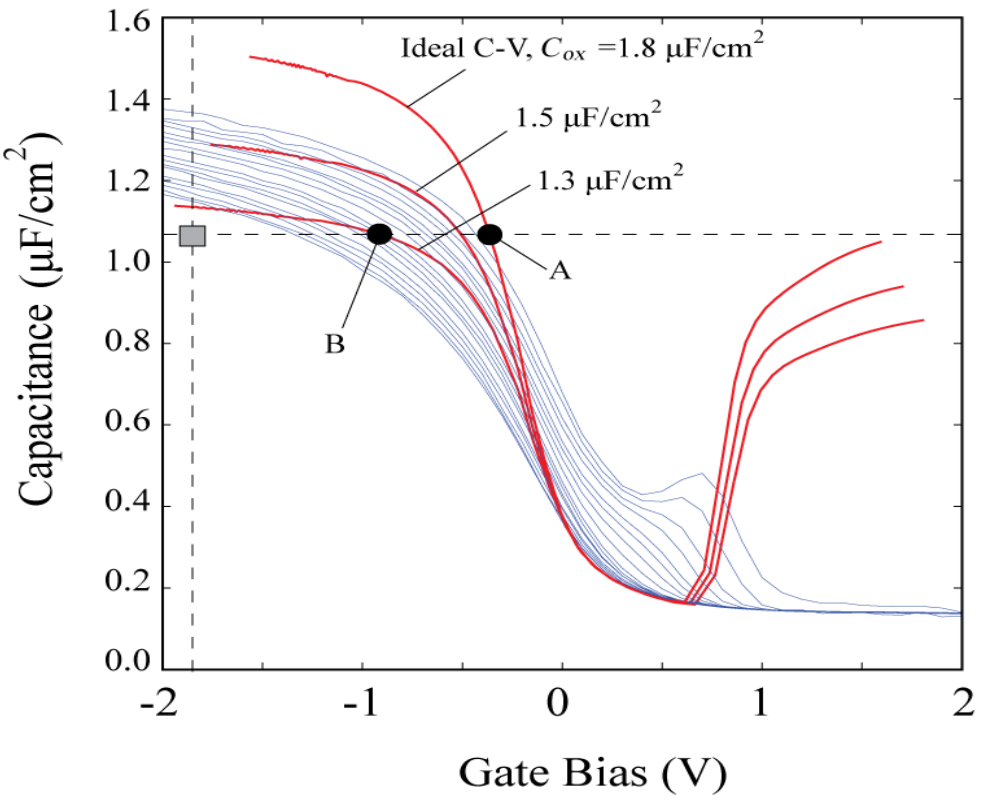

Figure 4.16: Experimental C−V data of an Al_2O_3/p-InGaAs MOSCAP taken at 17 frequencies from 100 Hz to 1 MHz. The dark curves are ideal, quasistatic C-Vs simulated by Sentaurus for three Cox values with $\varepsilon_{ox} = 7\varepsilon_0$.

In Fig. 4.17, C- and G-dispersion data at V_g= -1.8 V in accumulation are focused. With an assumed C_{ox} = 1.5 μF/cm2 in Fig. 4.11(a), the C_{tot} versus log ω curves generated by the lumped circuit model have too much curvature to fit the entire region of data. Adjusting τ_0 or N_{bt} only shifts the curve horizontally or vertically with little effect on the curvature. To reduce the curvature to an extent not too far deviated from the data trend, a large C_{ox} = 1.8 μF/cm^2 needs to be assumed [Fig. 4. 16(b)]. However, such a large C_{ox} would mean that the bias point Vg= -1.8 V was stretched out from point A in Fig. 3 on the ideal Sentaurus C-V for C_{ox} = 1.8 μF/cm^2. Point A was determined by the estimated intrinsic $C_{tot} = C_{ox}C_s/ (C_{ox} + C_s)$ at V_g= -1.8 V somewhat below the 1 MHz data point

(gray rectangle in Fig. 4.16). This is unreasonable because the slope dC/dV_g at point A is nearly as steep as the highest slope of that curve, hence it cannot be in accumulation. On the other hand, the slope dC/dV_g at V_g = -1.8 V of the 1 MHz C-V is only 1/5 of the steepest slope of the 1 MHz curve, inferring that it is in accumulation.

On the contrary, the nearly linear C_{tot} versus log ω data points are readily fitted by the distributed circuit model with a C_{ox} = 1.3 μF/cm^2 [dashed curve in Fig. 4.17(b)]. Note that the C_{tot} data at 100 Hz exceeds C_{ox} —an outcome allowed in the distributed circuit model but not in the lumped model. With the lower C_{ox}, the stretchout from point B on the ideal C-V to the intrinsic C_{tot} at V_g = -1.8 V (gray rectangle in Fig. 4.16) makes much more sense from the relative slope point of view (both in accumulation). The conductance data G_{tot} (ω) are also better fitted by the distributed model, as shown in Fig. 4.17(c). The 1 MHz G_{tot} point can be explained by adding series resistance to the model, as it is addressed in the previous section. It should be stressed that for the C_{ox} and N_{bt} values of the lumped model that best fitted the C_{tot} data in Fig. 4. 17(b), the G_{tot} vs. ω slope in Fig. 4.17(c) is 25% higher than the data. The distributed model, on the other hand, achieves best fittings of both C_{tot} and G_{tot} at the same time. While nonuniform Nbt can be accommodated in the distributed model, all the MOS dispersion data can be satisfactorily accounted for with a single, uniform N_{bt} fitting parameter (for a given V_g bias).

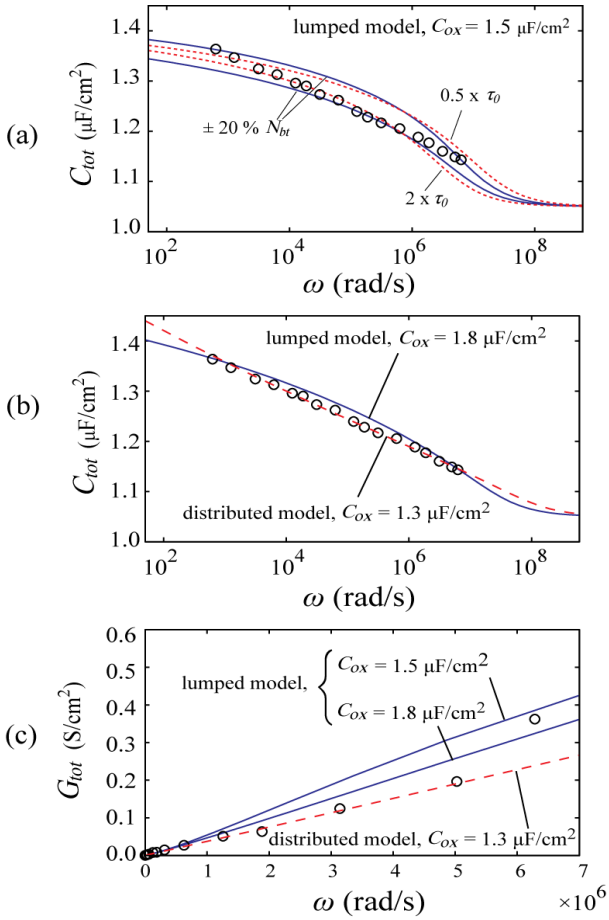

Figure 4.17: Model fitting of C_{tot} dispersion data (open circles) at V_g = -1.8 V. ε_{ox} is set to 7 ε_0, κ is set to 6×10^7 cm-1, and C_s is selected such that C_{ox} in series with C_s is 1.05 μF/cm² in all cases. (a) Lumped circuit model with C_{ox} = 1.5 μF/cm². Solid curves: N_{bt} = 7.0×10^{20} $cm^{-3}eV$-1±20%, τ_0 = 2.0×10^{-7} s. Dotted curves: 2× variation in τ0. (b) Lumped circuit model (solid) with C_{ox} = 1.8 μF/cm², N_{bt} = 2.05×10^{20} $cm^{-3}eV^{-1}$, τ0 = 5.0×10^{-8} s. Distributed circuit model (dashed) with C_{ox} = 1.3 μF/cm², N_{bt} = 6.0×10^{20} $cm^{-3}eV^{-1}$, τ_0 = 1.7×10^{-8} s. (c) G_{tot} fitting results.

Fig. 4.18 provides additional experimental evidence that the lumped-circuit model is inconsistent with measured dispersions. The MOSCAP here is an Al_2O_3 on n-type InGaAs with the oxide thickness calibrated by TEM measurements. The dielectric constant is extracted from the slope of $1/C_{max}$ versus tox plot consisting of several different thicknesses [14]. With the C_{ox} known, the uncertainty in the p-type case in Figs.

4.16 and 4.17 is removed. Fig. 4.18(a) compares the fitting of lumped and distributed models to the dispersion data in accumulation (data the same as that in Fig. 4.11, and the full C-V is in Fig. 5.1). The same curvature problem exists with the lumped model. Fig. 4.18 (b) shows that the slope $dC_{tot}/d(\log \omega)$ of the lumped model (best case in Fig. 4.18 (a)) is far off the data trend while the distributed model is consistent with the data trend. Fig. 4.18 (c) shows the mean (rms) percentage error of each model with Nbt as a fitting parameter. For G_{tot}, the error is defined as $\delta G_{tot}/G_{tot}$, where δG_{tot} is the deviation of model from the data point. For C_{tot}, the deviation is normalized by the dispersion measured from $C_{tot}(N_{bt} = 0) = C_{ox}C_s/(C_{ox} + C_s)$ to the C_{tot} (ω) of that point. The best fitting of both Ctot and G_{tot} occurs at the same $N_{bt} = 1.23\times10^{20}$ $cm^{-3}eV^{-1}$ for the distributed model. The lumped model not only has significantly larger errors in both C_{tot} and G_{tot} than the distributed model, but the best fitting of C_{tot} and G_{tot} also takes place at different N_{bt}. Note that in general G_{tot} errors are larger than those of C_{tot} because G_{tot} spans three orders of magnitude over the frequency range, much wider than C_{tot}.

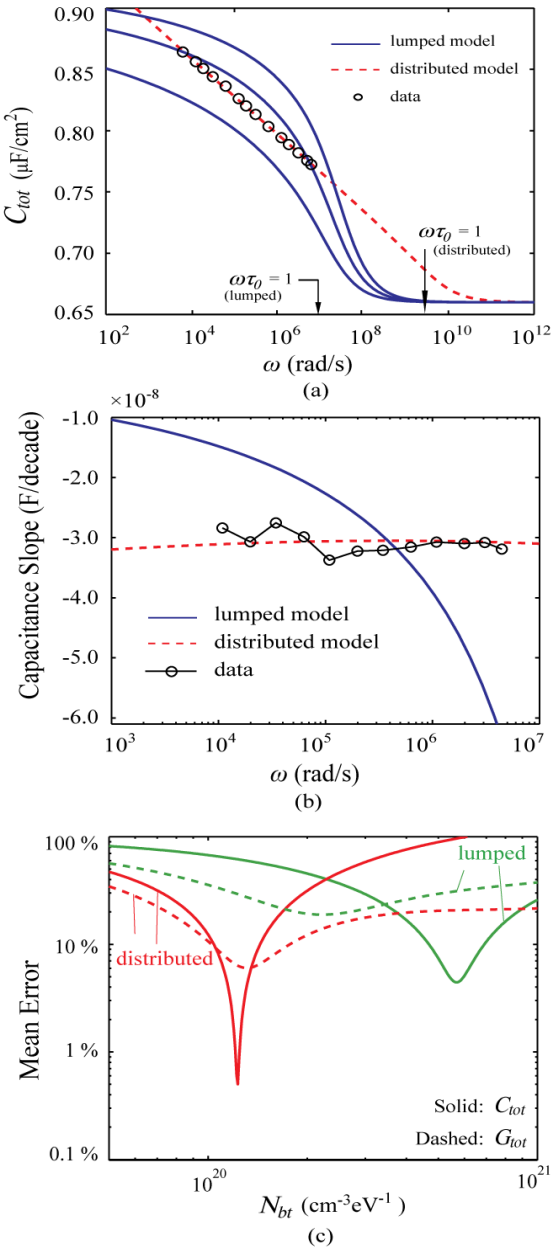

Figure 4.18: Model fitting of n-type InGaAs MOS data, with Al_2O_3 thickness of 7 nm and $\varepsilon_{ox} = 7.4\ \varepsilon_0$. Common model parameters are C_s = 2.2 μF/cm2 and κ = 5.1 nm^{-1}. In (a), Nbt = 1.23×10^{20} cm^{-3}eV^{-1} for distributed, 3.5, 6.5, 10×10^{20} cm^{-3}eV^{-1} for lumped. Arrows show τ_0 for each model. (b) dC_{tot}/d(log ω) vs. log ω (c) Fitting errors of C_{tot} and G_{tot} versus N_{bt} for lumped and distributed models.

4. 2. 3 Hasegawa Model

In a special case of the lumped-circuit model, Hasegawa and Sawada [7] considered an exponentially decaying trap density, $N_{bt} \propto \exp(-\alpha x)$, where α is in cm^{-1}. Fig. 4.19 shows that such a profile produces even more curvature in the Ctot versus log ω curve than the uniform N_{bt} lumped model. In other words, there is more C_{tot} dispersion per log ω at high frequency than at low frequency. While such data characteristics may have been the case with [7], they have never been observed in any of the samples we analyzed thus far. In fact, the opposite was observed in some published Al_2O_3/InP data [13], suggesting that N_{bt} might be going up farther away from the interface, not down. The best fitting in Fig. 4.18 is obtained with small α, or α = 0, back to the case of uniform trap density. In an earlier work on GaAs MOS [15], Hasegawa and Sawada's model was applied to explain the large C-V dispersion observed in accumulation. No detailed fitting of both the C_{tot} and the G_{tot} data with the same trap density was given.

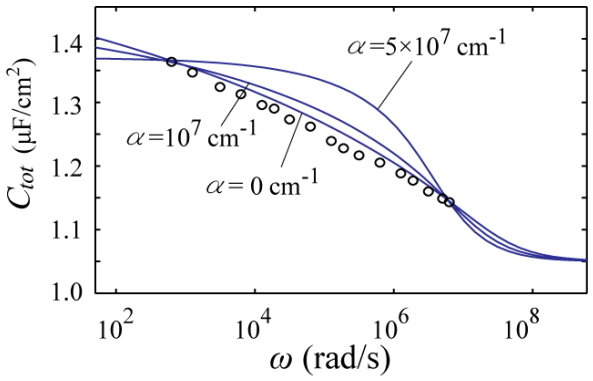

Figure 4.19: Fitting of the same data with Hasegawa and Sawada's model (C_{ox} = 1.8 μF/cm^2). N_{bt} and τ_0 are adjusted for best fitting as α is varied.

The text of Chapter 4, in part, is a reprint of the material as it appears in "Comparison of Bulk-Oxide Trap Models: Lumped versus Distributed Circuit" by Han-

Ping Chen, Jaesoo Ahn, Paul C. McIntyre, and Yuan Taur, IEEE Transaction on Electron Devices, Nov., 2013. The dissertation author was the primary investigator and author of this paper.

The text of Chapter 4, in part, is a reprint of the material as it appears in "Comments to "A Distributive-Transconductance Model for Border Traps in III-V/High-k MOS Capacitors" by Yuan Taur, Han-Ping Chen, Yu Yuan, and Bo Yu, IEEE Electron Device Letter, Oct., 2013. The dissertation author was a co-author of this paper.

The text of Chapter 4, in part, is a reprint of the material as it appears in "Comments to "On the effect and extraction of series resistance in Al_2O_3-InGaAs MOS with bulk-oxide trap" by Bo Yu, Yu Yuan, Han-Ping Chen, and Yuan Taur, Electronics Letter, Mar., 2013. The dissertation author was a co-author of this paper.

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Chapter 5

Thickness and Temperature Effects on C-V Dispersions of High-*k* III-V MOS Capacitors

The C-V dispersion data on Al_2O_3/ n-InGaAs MOS capacitors with different insulator thicknesses are shown in Fig. 5.1. As it is explained in the previous chapters, the uniform dispersions in the accumulation regions and near the flatband are due to electron traps in the oxide that communicate with conduction band electrons by tunneling [1]. The humps or high-low dispersions in the depletion and inversion regions are due to conventional interface states [2]. As the oxide thickness increases, the normalized dispersions of oxide traps decrease while those of the interface states increase. In this

chapter, the two model described in previous chapters are applied to address the question: should the C-V data be interpreted such that the oxide trap density goes down while the surface state density goes up for thicker oxides?

Also addressed is the temperature effect on observed C-V dispersions. In the example in Fig. 5.2, the interface state humps largely subside at low temperatures. On the other hand, the dispersion from oxide traps only changes slightly with temperature. Both the interface state model and the oxide trap model are used to explain such behavior.

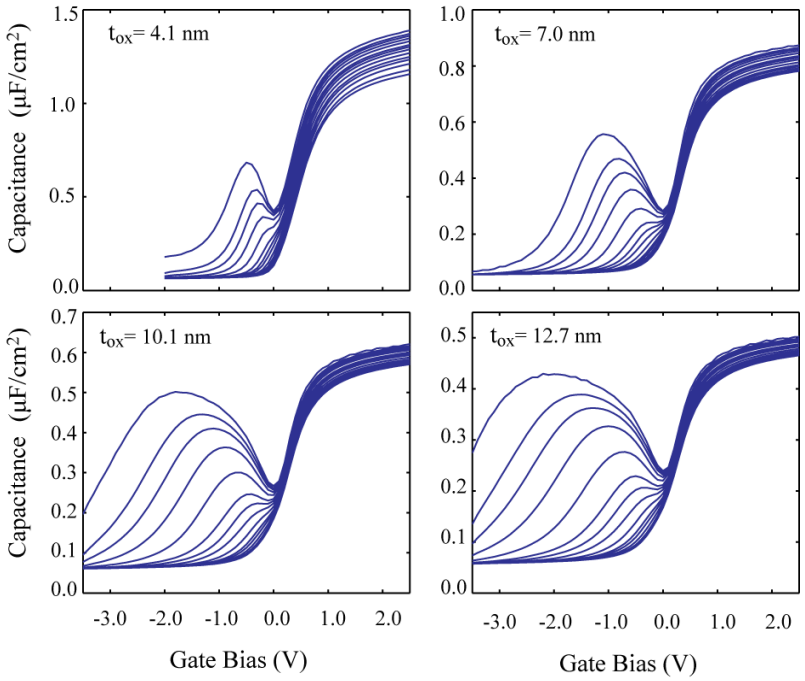

Figure 5.1: Measured C-V characteristics of Pt/Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS capacitors with four different oxide thicknesses. The small signal frequencies are from 1 kHz to 1 MHz with 1, 2, 3, 5, 10 steps plus an added frequency at 800 kHz. The samples were fabricated under processing conditions similar to those in Kim *et al*. [3]

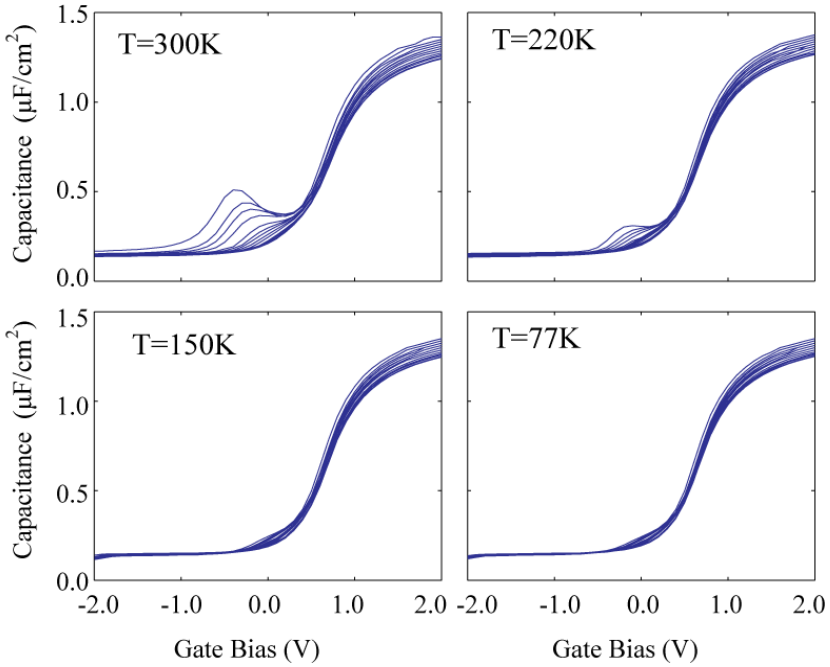

Figure 5.2: Measured C-V data of Al_2O_3/n-$In_{0.53}Ga_{0.47}As$ MOS at four different temperatures. The frequencies are the same as in Fig. 5.1. The samples were prepared under experimental conditions similar to those in Ahn *et al*. [4]

5. 1 Thickness Effect on Dispersions Due to Bulk-Oxide Traps

The distributed oxide trap model [1] described in Ch. 4 is applied to examine the effect of oxide thickness on the dispersions in accumulation. The C_{tot} dispersion data of Fig. 5.1 at V_g = 2.0 V are plotted in Fig. 5.3 (circles). The linear dependence on log(ω) is a characteristic of bulk-oxide traps for which the time constant is an exponential function of thickness. The solid curves in Fig. 5.3 show that with one set of oxide trap and semiconductor parameters: $C_s = 2\times10^{-6}$ F/cm^2, $\tau_0 = 3\times10^{-10}$ s, $\kappa = 3.8\times10^{7}$ cm^{-1}, and $N_{bt} = 6.6\times10^{19}$ cm^{-3}eV^{-1}, the dispersion data of all four oxide thicknesses can be fitted satisfactorily. The parameter κ above for electron tunneling was calculated from a barrier height of 2.0 eV and an effective mass of $0.28m_0$ [5]. The oxide parameters applied are ε_{ox}

= $7.4\varepsilon_0$ and t_{ox} = 4.1 nm, 7.0 nm, 10.1 nm, and 12.7 nm, consistent with the number of ALD cycles for each film. The slight drop of capacitance at the 1 MHz end of the 4.1 nm data can be explained by adding a small series resistance of 0.02 Ω-cm^2 to the model. The fitting with a single N_{bt} proves that the trap density is not higher in thin oxides despite their apparently larger dispersion in accumulation.

For an analytic insight of why the same trap density produces larger normalized C-V dispersion in thin oxides, we consider a lumped circuit approximation of the border trap model. Without any oxide traps, or at a high enough frequency where no trap can respond, $C_{tot}^{-1} = C_{ox}^{-1} + C_s^{-1}$. A small added trap capacitance near the semiconductor-oxide interface can be approximated as δC_{bt} in parallel with C_s. It gives rise to a dispersion of δC_{tot} in C_{tot}. We can write

$$\frac{1}{C_{tot}+\delta C_{tot}} = \frac{1}{C_{ox}} + \frac{1}{C_s+\delta C_{bt}} \tag{5.1}$$

Equating the first order terms of the power series expansion on both sides then gives:

$$\frac{\delta C_{tot}}{C_{tot}} = \frac{C_{tot}}{C_s^{\,2}}\delta C_{bt} \tag{5.2}$$

So for a given δC_{bt}, the normalized C_{tot} dispersion due to border traps grows with the larger C_{tot} in thin oxides.

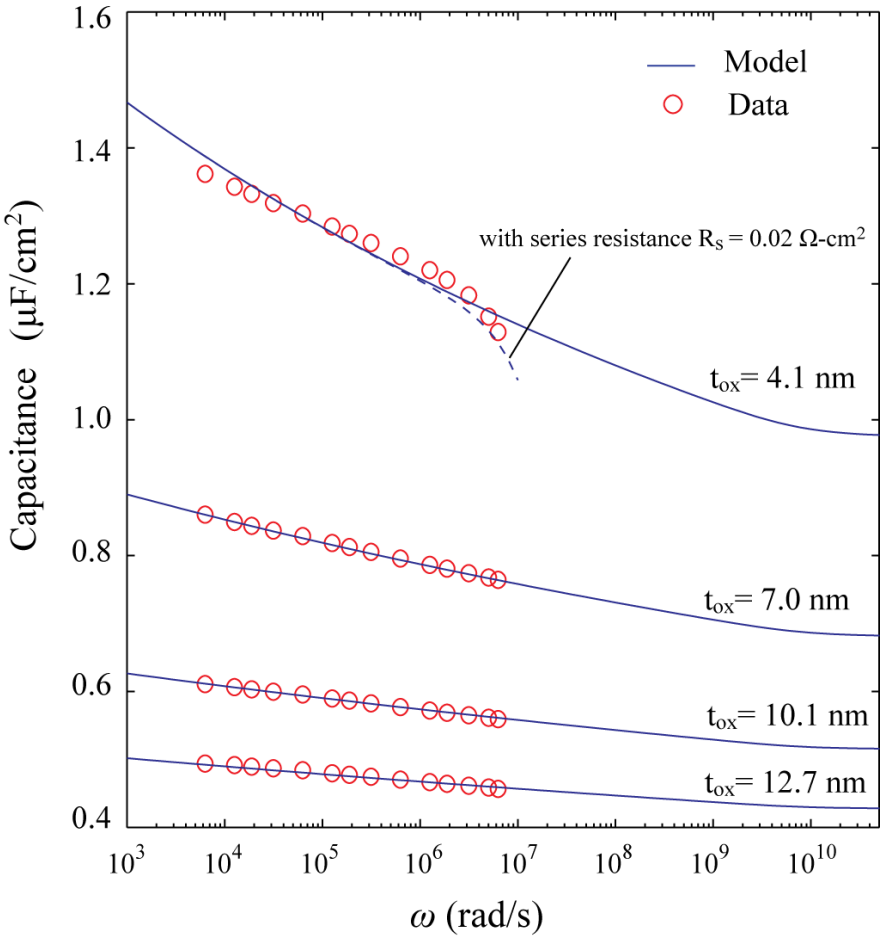

Figure 5.3: Model fitting of the C_{tot} dispersion at V_g = 2 V in Fig. 5.1. The parameters are N_{bt} = 6.6×10^{19} eV^{-1}cm^{-3}, ε_{ox} = 7.4ε_0, κ = 3.8×10^7 cm^{-1}, τ_0 = 3×10^{-10} s, and C_s = 2.5 μF/cm^2 for all four cases.

5. 2 Thickness Effect on Dispersions Due to Interface Traps

In Fig. 5.1, as the oxide thickness increases, the hump of the 1 kHz capacitance in the negative V_g range becomes broader and moves further negative. Also, the height of the hump relative to the capacitance in accumulation increases from about 50% for t_{ox} = 4.1 nm to nearly 100% for t_{ox} = 12.7 nm. To explain the observation, we apply the full interface state model described in chapter 3 with the equivalent circuit in Fig. 5.4(a).

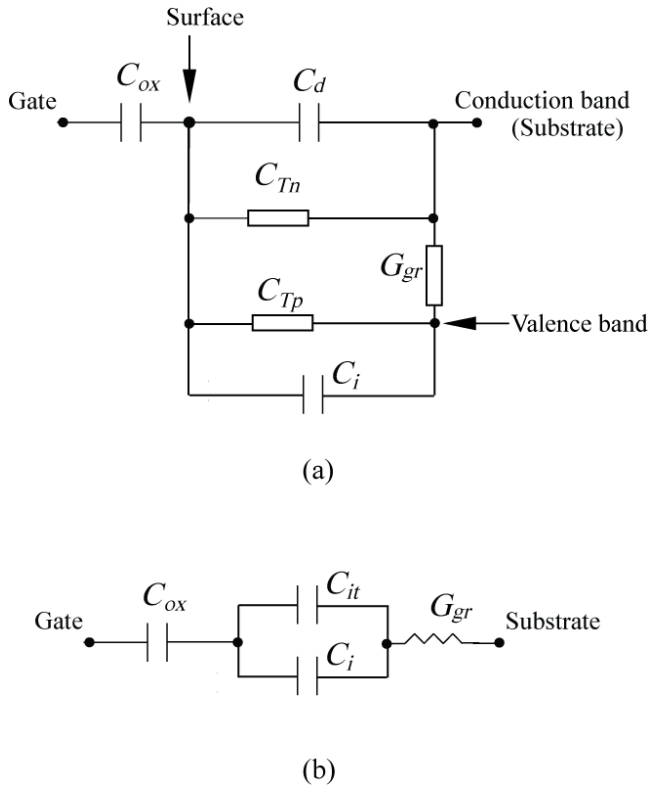

Figure 5.4: (a) Equivalent circuit model of an MOS capacitor on n-type substrate with interface state elements C_{Tn}, C_{Tp}, G_{gr}. (b) Approximate equivalent circuit in weak and strong inversion.

Here, C_d is the majority carrier depletion capacitance and C_i is the inversion layer capacitance per area. The latter rises steeply to much larger than C_{ox} in strong inversion. Interface states are represented by the Π-circuit consisting of frequency dependent complex admittances $j\omega C_{Tn}$, $j\omega C_{Tp}$, and G_{gr} [6]. They are functions of the interface state capacitance C_{it} ($\equiv qD_{\mathrm{it}}$, with D_{it} the interface state density in $\mathrm{cm}^{-2}\mathrm{eV}^{-1}$), the electron capture time τ_n, and the hole capture time τ_p [6]. τ_n and τ_p are inversely proportional to the electron and hole concentrations at the MOS surface, respectively. In an n-type material, τ_n increases by orders of magnitude from accumulation to inversion.

When biased in weak inversion and beyond, $\tau_p < \tau_n$, $C_{Tn} \rightarrow 0$ and $C_{Tp} \rightarrow C_{it}$. It can be shown that G_{gr} is a conductance with mostly real part and that for $\omega\tau_p << 1$,79

$$G_{gr} \approx \frac{C_{it}}{\tau_n} \ln\left(\frac{\tau_n}{\tau_p}\right) \tag{5.3}$$

independent of frequency. At 1 kHz and near the peak of the hump, C_d can be neglected. The MOS equivalent circuit is then approximated by the serial connection of C_{ox}, $C_i + C_{it}$, and G_{gr}, shown in Fig. 5.4(b). The total capacitance is

$$C_{tot} \approx \frac{C_{ox}^{-1} + (C_i + C_{it})^{-1}}{(\omega G_{gr}^{-1})^2 + \left[C_{ox}^{-1} + (C_i + C_{it})^{-1}\right]^2} \tag{5.4}$$

This approximation works better when the surface potential is 0.1 V or more further negative than the midgap point. The hump is a result of two opposing effects. When V_g moves in the negative direction, C_i and C_{it} increases, but G_{gr} decreases because τ_n increases much faster than C_{it}. Physically, a much longer time is needed for electron capture when the surface is severely depleted of electrons toward stronger inversion. Going from thin oxides to thick oxides, C_{ox}^{-1} becomes the dominant term in Eq. (5.4), much larger than both $(C_i + C_{it})^{-1}$ and ωG_{gr}^{-1}. The trend for the peak of the hump is then $C_{tot} \rightarrow C_{ox}$. At the same time, the width of the hump broadens in thick oxides because the variation of $C_i + C_{it}$ and G_{gr} has less effect on C_{tot}.

To explain the shifting of the peak with oxide thickness, consider a small change in the surface potential, $\delta\psi_s$. It gives rise to changes δG_{gr} and $\delta(C_i + C_{it})$, and therefore a change in C_{tot}:

$$\delta C_{tot} = Z^2 \left\{ \frac{\delta(C_i + C_{it})}{(C_i + C_{it})^2} - \frac{\delta(\omega G_{gr}^{-1})^2}{C_{ox}^{-1} + (C_i + C_{it})^{-1}} - \frac{(\omega G_{gr}^{-1})^2 \delta(C_i + C_{it})}{\left[1 + (C_i + C_{it}) C_{ox}^{-1}\right]^2} \right\} \qquad (5.5)$$

Here, Z^2 is some positive expression of the parameters. Given a certain D_{it} distribution, C_{it}, C_i, τ_n, and G_{gr} are fixed functions of the surface potential, ψ_s. For $\delta\psi_s < 0$, $\delta(C_i + C_{it}) > 0$ and $\delta(\omega G_{gr}^{-1})^2 > 0$. The sign of δC_{tot} depends on the three terms in the bracket: one positive, two negative. At the peak of the hump, $\delta C_{tot} = 0$. Before the peak (on the right side), $\delta C_{tot} > 0$. After the peak (on the left side), $\delta C_{tot} < 0$. At a fixed ψ_s, the positive term is fixed, while the magnitudes of both negative terms decrease with the increasing C_{ox}^{-1} of thick oxides. This means that at the ψ_s value where $\delta C_{tot} = 0$ for the thin oxide, $\delta C_{tot} > 0$ for the thick oxide. In other words, the peak of the hump shifts to a more negative ψ_s in thicker oxides. Along the same line, the magnitudes of the two negative terms also decrease with decreasing frequency, which explains the shifting of lower frequency humps toward negative bias for a given oxide thickness.

In converting ψ_s to V_g, there is an additional factor that further shifts and broadens the humps in thicker oxides: the static stretchout factor,

$$\frac{\delta V_g}{\delta \psi_s} = 1 + \frac{C_{it} + C_i + C_d}{C_{ox}} \quad . \tag{5.6}$$

It goes up with oxide thickness. A much larger V_g swing is needed in the 12.7 nm case than in the 4.1 nm case to arrive at the same surface potential.

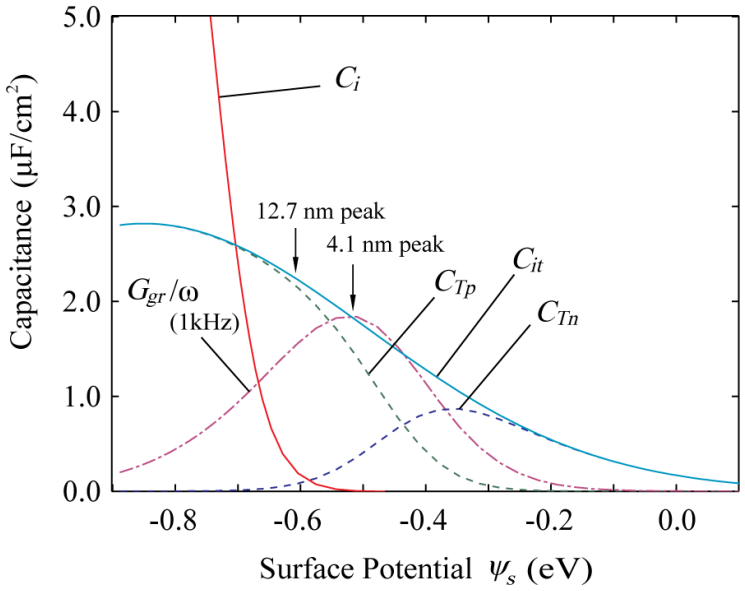

Figure 5.5: The input distribution of interface states, $C_{it}(\psi_s)$, to the model behind Fig. 5.6. $C_i(\psi_s)$ is from a Poisson solver. C_{Tn}, C_{Tp}, and G_{gr}/ω are the derived interface state components (dominated by the real parts) at 1 kHz. The vertical arrows indicate the ψ_s values at the corresponding peaks of the 1 kHz hump in Fig. 5.6.

For a more quantitative proof that the various hump sizes and shapes in Fig. 5.1 are manifestations of the same interface state distribution, the full model of Fig. 5.4(a) is used, in conjunction with the stretchout factor above, to generate C-V curves for different oxide thicknesses. The starting point for the input parameters to the model, $D_{it}(\psi_s)$, $\tau_n(\psi_s)$, $\tau_p(\psi_s)$, is taken from those in [2], which were obtained following an elaborate point-by-

point fitting of the capacitance and conductance dispersion data. To best fit the current set of data, the original $D_{it}(\psi_s)$ is adjusted upward by some 50-100%, depending on the ψ_s bias. The resultant interface-state distribution and the corresponding 1 kHz components are shown in Fig. 5.5. In strong inversion, C_{it} and C_i are in parallel hence cannot be separately determined through fitting of the data. The C_i curve in Fig. 5.5 is that expected from device simulations. Fig. 5.6 displays the model generated multiple-frequency C-V curves for two oxide thicknesses over the data from Fig. 5.1. All the previously noted features of the humps from the 4.1 nm and the 12.7 nm data are reproduced by the model. Note in Fig. 5.6(a) that strong inversion, or the steep rise of C_i, occurs on the falling side of the 1 kHz peak. Based on Eq. (5.5), for the C_{tot} in the 4.1 nm case to reach $\approx C_{ox}$ in strong inversion, the frequency needs to be much lower than $G_{gr}/(2\pi C_{ox}) \sim 250$ Hz where $G_{gr} \approx 2.5$ mS/cm^2 is the value at $\psi_s = -0.8$ V from Fig. 5.5.

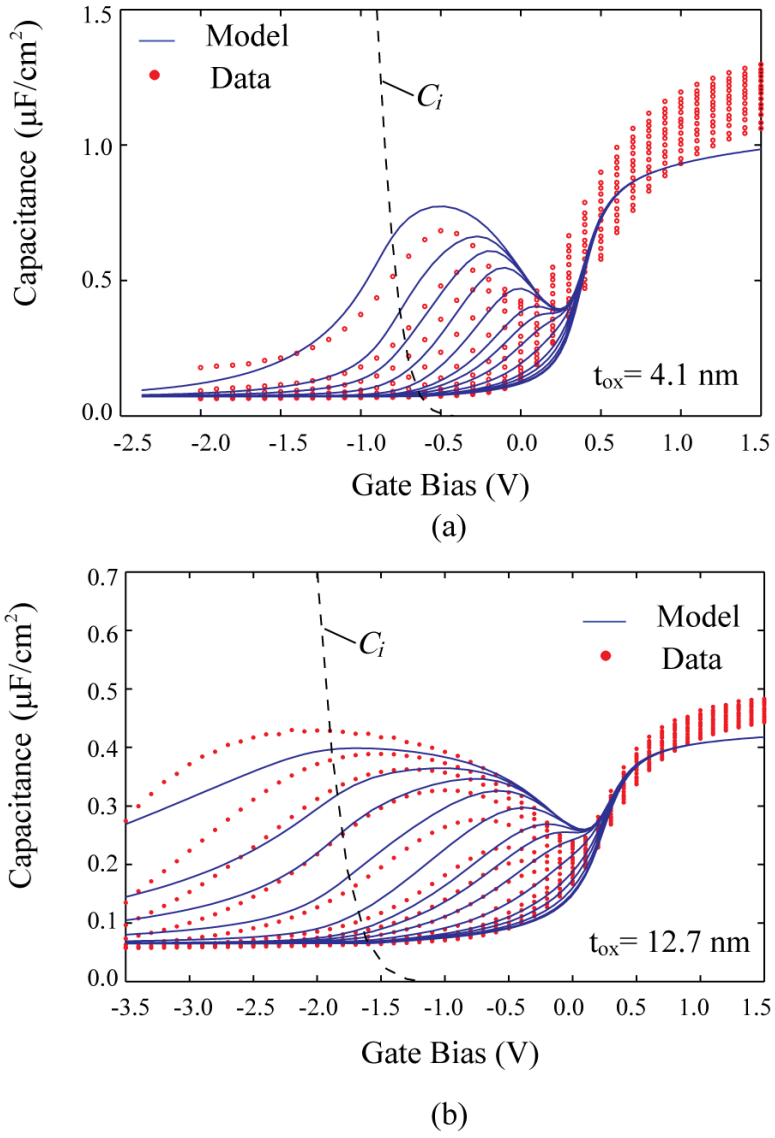

Figure 5.6: Comparison of model generated C-V to the data of Fig. 5.1. The same interface state parameters shown in Fig. 5.5 are applied to both (a) t_{ox} = 4.1 nm and (b) t_{ox} = 12.7 nm cases.

5. 3 Temperature Effect on Dispersions Due to Bulk-Oxide Traps

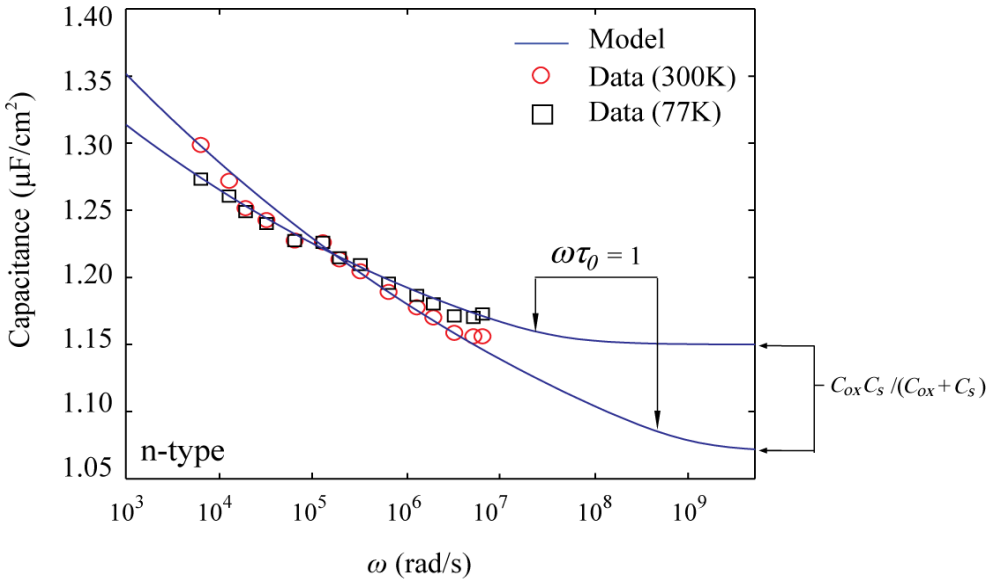

Figure 5.7: Model fitting of the C_{tot} dispersion in accumulation (V_g = 1.5 V) at 300 K and 77 K in Fig. 5.2. Parameters common to both temperatures are: uniform N_{bt} = 4.85×10^{19} $eV^{-1}cm^{-3}$, C_{ox} = 1.6 μF/cm², and κ = 3.8×10^{7} cm^{-1}. For 300 K, τ_0 = 2×10^{-9} s and C_s = 3.23 μF/cm². For 77 K, τ_0 = 5×10^{-8} s and C_s = 4.09 μF/cm²

Fig. 5.2 showed that the dispersion in accumulation due to oxide or border traps changes very little with temperature. In the oxide trap model discussed in Section 5.1, the parameter most sensitive to temperature is $\tau_0 = (n_s\sigma v_{th})^{-1}$, the trap time constant at x = 0. τ_0 goes up from room temperature to low temperature because carrier thermal velocity and trap cross-section go down. Model fitting of the C_{tot} dispersion data at V_g = 1.5 V is shown in Fig. 5.7. A uniform trap density of 4.85×10^{19} $cm^{-3}eV^{-1}$ is assumed for both 300 and 77 K. Note that for a fixed set of model parameters, the dispersion slope, $|dC_{tot}/d(\log \omega)|$, decreases slightly from $\omega\tau_0 << 1$ toward $\omega\tau_0 \approx 1$. The ~10 times increase of $\omega\tau_0$ for the frequencies 1 kHz-1 MHz from 300 to 77 K explains the slight reduction of

dispersion in that range. Another factor that contributes to the decrease of dispersion is a moderate increase of the semiconductor capacitance C_s at low temperatures. It raises $C_{ox}C_s/(C_{ox} + C_s)$, the floor of C_{tot} at $\omega\tau_0 > 1$.

Fig. 5.8 shows the C-V data of a p-type InGaAs MOS sample processed under similar conditions as those in Ahn *et al.* [4]. The dispersions in accumulation in this case can be due to tunneling of holes below the bottom of the valence band barrier, or due to tunneling of valence band electrons over the top of the conduction band barrier. As mentioned before, the conduction band offset between $In_{0.53}Ga_{0.47}As$ and Al_2O_3 is 2.0 eV. Since the bandgap of $In_{0.53}Ga_{0.47}As$ is 0.75 eV and the bandgap of Al_2O_3 is 6.6 eV, the barrier height for tunneling of valence band electrons from the top, 2.75 eV, is significantly lower than the barrier height for hole tunneling from the bottom. For the same $m^* = 0.28m_0$ as before, κ is determined to be 4.5×10^7 cm^{-1} for p-type. The model fitting in Fig. 5.9 for p-type parallels that of n-type. The same density of oxide traps, $N_{bt} = 2.9\times10^{20}$ $cm^{-3}eV^{-1}$, is assumed for both 300 and 77 K. The reduction of dispersion at the low temperature results from a longer trap time constant and a higher semiconductor capacitance.

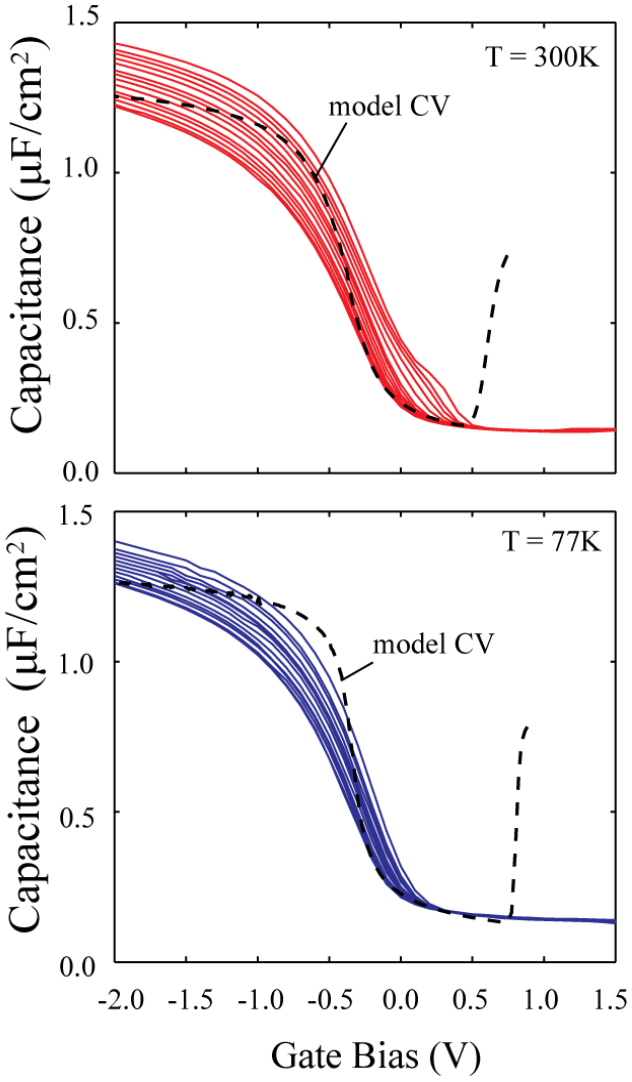

Figure 5.8: C-V data of Al_2O_3/p-$In_{0.53}Ga_{0.47}As$ MOS measured at 300 K and 77 K. The frequencies are the same as those in Fig. 5.1. Dashed curves are simulated ideal C-V with C_{ox} = 1.45 μF/cm^2 and p-type doping of 1.9×10^{17} cm^{-3}.

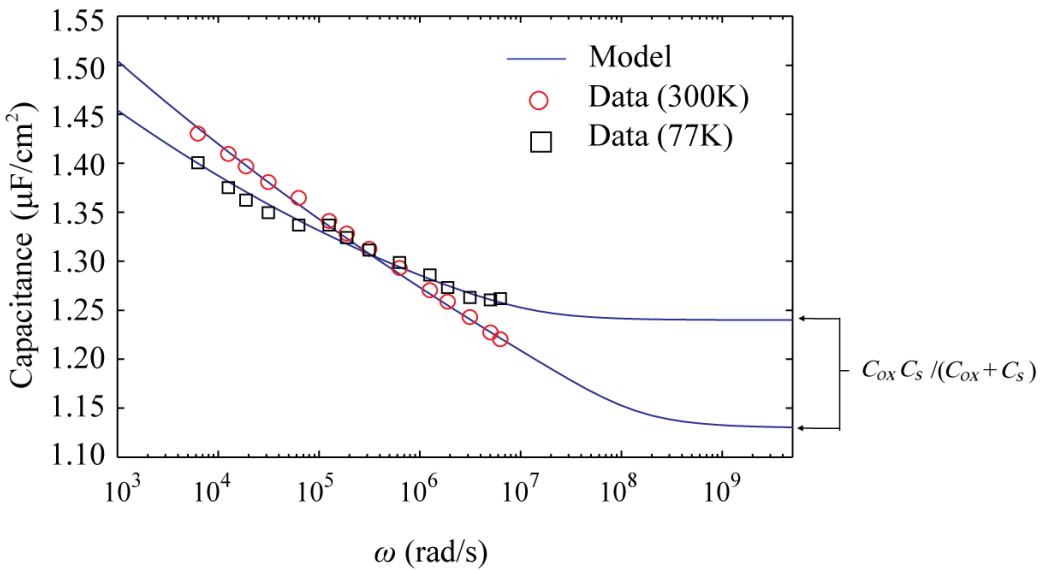

Figure 5.9: Model fitting of the C_{tot} dispersion in accumulation (V_g = –2.0 V) at 300 K and 77 K in Fig. 5.8. Parameters common to both temperatures are: uniform N_{bt} = 2.9×10^{20} $eV^{-1}cm^{-3}$, C_{ox} = 1.45 μF/cm^2, and κ = 4.5×10^{7} cm^{-1}. For 300 K, τ_0 = 1.8×10^{-8} s and C_s = 5.12 μF/cm^2. For 77 K, τ_0 = 1.5×10^{-7} s and C_s = 8.56 μF/cm^2.

While the data covered in this paper on dispersion from oxide traps show little change with temperature, changes by 2-3 times from 300 K to 77 K have been reported in the literature [7-9]. Such a large reduction cannot be explained by τ_0 and C_s with a uniform N_{bt} as was done in Figs. 8 and 10. Dou *et al*. [9] recently came up with a temperature independent, but nonuniform $N_{bt}(x)$ to fit their dispersion data at all temperatures. The key idea is based the oxide trap model:

$$\Delta Y_{bt}(x) = \frac{q^2 N_{bt} \ln(1 + j\omega\tau_0 e^{2\kappa x})}{\tau_0 e^{2\kappa x}} \Delta x \qquad (5.7)$$

that the capacitive component of $\Delta Y_{bt}(x)$ or, $\mathrm{Im}[\Delta Y_{bt}(x)]/\omega$, decreases rapidly with x when $\omega\tau_0 e^{2\kappa x} > 1$. In other words, the traps contributing to the capacitance measured at frequency ω reside at a depth between $x = 0$ and

$$x \approx \frac{1}{2\kappa}\ln\left(\frac{1}{\omega\tau_0}\right) \tag{5.8}$$

Because τ_0 increases at low temperatures, the oxide traps responsible for the dispersion between 1 kHz and 1 MHz at 77 K are shallower than those responsible for the dispersion at 300 K. A nonuniform trap distribution with the trap density increasing deeper into the oxide then explains the relatively large increase of dispersion at higher temperatures.

Note that while the border traps at the valence band energy give rise to dispersion in accumulation of p-type C-V, they do not have a significant effect on n-type C-V in inversion. This is because in the latter case, the trap elements are connected to the valence band in Fig. 5.4(a), then via G_{gr} to the substrate (conduction band) contact. Physically, it means that for the n-type contact to supply or take away valence band electrons or holes, a generation and recombination process assisted by the surface states is involved. With the rapidly decreasing G_{gr} in strong inversion (Fig. 5.5), border traps at the valence band energy cannot respond fast enough to contribute to the 1 kHz capacitance [2].

5. 4 Temperature Effect on Dispersions Due to Interface Traps

In contrast to the insensitivity of oxide-trap generated dispersions to temperature, temperature has a dramatic effect on the dispersion from interface states in the depletion and inversion regions (V_g < 0.4 V) in Fig. 5.2. The full interface state model in Fig. 5.4(a) is applied to analyze, for example, the capacitance dispersion data at V_g = –0.3 V in Fig. 5.2. This bias condition is near the midgap and the trap time constants are very different from the time constant for capture of majority carriers in accumulation. First, both τ_n and τ_p are much longer because of the low carrier densities at the surface. Second, the carrier densities and therefore τ_n and τ_p are more sensitive to temperature under the nondegenerate condition. Fig. 5.10 shows model fitting of the data of all four temperatures, with one interface state density, D_{it} = 4.0×10^{12} $eV^{-1}cm^{-2}$. All model curves are of the high-low type. At low frequencies, all the surface states respond to the small signal and the capacitance is C_{ox} in series with (C_s + C_{it}). At high frequencies, no states respond and the capacitance is C_{ox} in series with C_s. The high-low transition shifts with the temperature through the time constants. At 150 K and below, the transition has shifted to far below 1 kHz so only a very small fraction of the dispersion is observed in the measured range.

The text of Chapter 5, in part, is a reprint of the material as it appears in “Effects of Oxide Thickness and Temperature on Dispersions in InGaAs MOS C-V Characteristics” by Han-Ping Chen, Jaesoo Ahn, Paul C. McIntyre, and Yuan Taur, Journal of Vacuum Science & Technology B, Mar., 2014. The dissertation author was the primary investigator and author of this paper.

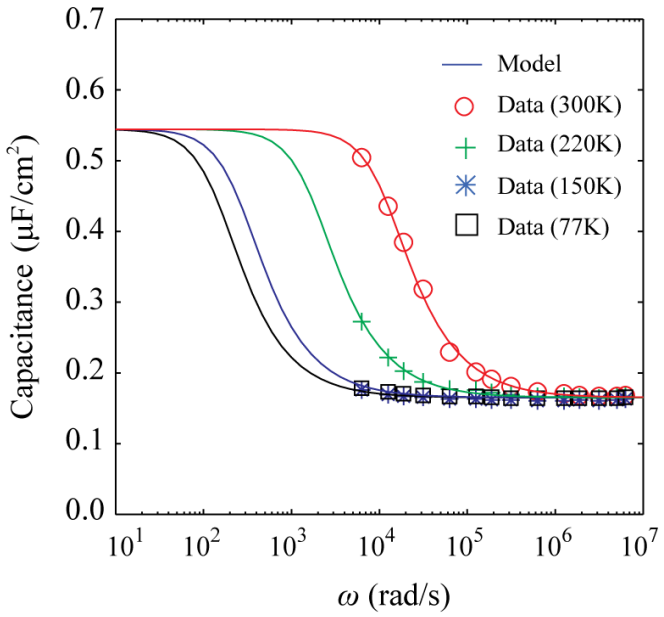

Figure 5.10: Model fitting of C_{tot} dispersion data of Fig. 5.2 at V_g = –0.3 V. For all temperatures, D_{it} = 4.0×10^{12} $eV^{-1}cm^{-2}$, C_{ox} = 1.6 μF/cm², and C_d = 0.18 μF/cm². Temperature specific parameters are $\tau_n = \tau_p$ = 1.6×10^{-4} s, 1.1×10^{-3} s, 8.0×10^{-3} s, and 1.5×10^{-2} s from 300 K to 77 K.

.

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Chapter 6

Light Illumination Effect on High-*k* III-V MOS Capacitors

InGaAs MOS C-V and G-V characteristics are measured under illumination to identify regions of strong minority carrier response related to surface inversion. For the MOS structure with n-type substrate biased in inversion, a high density of surface states in the proximity of the valence band edge is present that masks the response of light generated minority carriers at room temperature. Much stronger effect of illumination is

observed at low temperature where the surface-state response is suppressed due to carrier freeze out. On the other hand, for the MOS structure with p-type substrate, strong minority carrier response under illumination is readily observed in inversion even at room temperature, reflecting that the density of surface states near the edge of conduction band is negligible. All the data can be explained in the framework of small-signal equivalent circuit, by modeling the minority carrier generation with a light-dependent conductance plugged in between the conduction band and the valence band. The model is validated against the measured MOS conductance with and without light in inversion.

6. 1 Sample Fabrication

The samples used in the study were based on MBE grown 150 nm thick $In_{0.53}Ga_{0.47}As$ n-type (doped with Si) or p-type (doped with Be) layer on top of heavily doped buffer on a heavily doped InP substrate. Doping level of 10^{17} cm^{-3} was reached for both n-type and p-type layers. After a surface pre-cleaned by HF, a 2 nm Al_2O_3 layer followed by a 5 nm ZrO_2 layer formed the gate dielectric stack. H_2O based atomic layer deposition technique (ALD) was used to deposit both dielectrics, with tri-methyl aluminum (TMA) and Zirconium tert-butoxide (ZTB) precursors, respectively. The sample was then annealed in nitrogen at 500° C. TaN, gate metal, was deposited using physical vapor deposition (PVD). The metal was patterned to form individual capacitors with the area ranging from 2.5×10^{-5} cm^2 to 1.86×10^{-4} cm^2. Backside contact was formed by Au/Ge/Ni/Au for n-type, and Cr/Au for p-type substrate. Green laser with 5 mW output power was utilized in the experiment as the light source.

6. 2 Model Description

The equivalent circuit of the MOS model is described in Chapter 3 and shown here again in Fig. 1(a). C_{ox} and C_d are the oxide capacitance and majority carrier depletion capacitance per area, respectively. C_i is the inversion layer capacitance per area which rises steeply to >> C_{ox} in strong inversion. Interface states are represented by the Δ-circuit consisting of frequency dependent complex admittances C_{Tn}, C_{Tp}, and G_{gr} [1]. The conductance, G_d, connected between the conduction band and the valence band is related with generation and recombination of minority carriers in the bulk semiconductor. In the absence of interface states, the frequency dependence of the MOS capacitance in strong inversion hinges on the magnitude of G_d [2].

In an n-type semiconductor, G_d represents the diffusion of thermally generated holes from the bulk of the substrate to the interface, and is given by [1]

$$G_d = \frac{q\mu_p n_i^2}{L_p N_d}, \tag{6.1}$$

where q is the electron charge, n_i is the intrinsic carrier concentration, N_d is the doping density, μ_p is the hole mobility, and L_p is the hole diffusion length. Note, the factor n_i^2/N_d in Eq. (1) represents the concentration of thermally generated minority carriers in the bulk semiconductor. Under illumination, the minority carrier generation rate in the substrate is increased to $\mathcal{G}_l$ (in $cm^{-3}s^{-1}$), in proportion to the light intensity. The n_i^2/N_d factor in Eq. (1) is then replaced by the light enhanced minority carrier concentration, $\mathcal{G}_l \tau_p$, where τ_p is the minority carrier lifetime. L_p and τ_p are related by $L_p = [(kT/q)\mu_p \tau_p]^{1/2}$.

Substituting this expression into Eq. (1), the conductance between the conduction band and valence band under illumination is expressed as

$$G_{dL} = q\mathcal{G}_{\mathcal{H}}\sqrt{\frac{q\mu_p \boldsymbol{t}_{\boldsymbol{p}}}{kT}} \tag{6.2}$$

As it is described in chapter 3, when biased in strong inversion, $\tau_p << \tau_n$, C_{Tn} is negligible and $C_{Tp} \approx C_{it}$. The equivalent circuit is then reduced to that of Fig. 2(b). It can be shown that G_{gr} is a real conductance and that for $\omega\tau_p << 1$,

$$G_{gr} \approx \frac{C_{it}}{\tau_n}\ln\left(\frac{\tau_n}{\tau_p}\right), \tag{6.3}$$

independent of frequency.

All the circuit elements associated with the semiconductor and its interface can be lumped into an admittance, $G_p + j\omega C_p$, as shown in Fig. 2(c). $C_p(\omega)$ and $G_p(\omega)$ can be extracted from the measured MOS admittance once an estimate is made on C_{ox}. For frequencies $\omega >> (G_{gr} + G_d)/(C_{it} + C_i)$, $G_p \approx G_{gr} + G_d$. Without light, the intrinsic G_d of Eq. (1) is negligible, and does not practically contribute into the conductance G_p, which in this case is determined by G_{gr} only. With light input, G_{dL} of Eq. (2) is combined with G_{gr} to constitute G_p:

$$G_p = \frac{C_{it}}{\tau_n}\ln\left(\frac{\tau_n}{\tau_p}\right) + G_{dL} \tag{6.4}$$

.

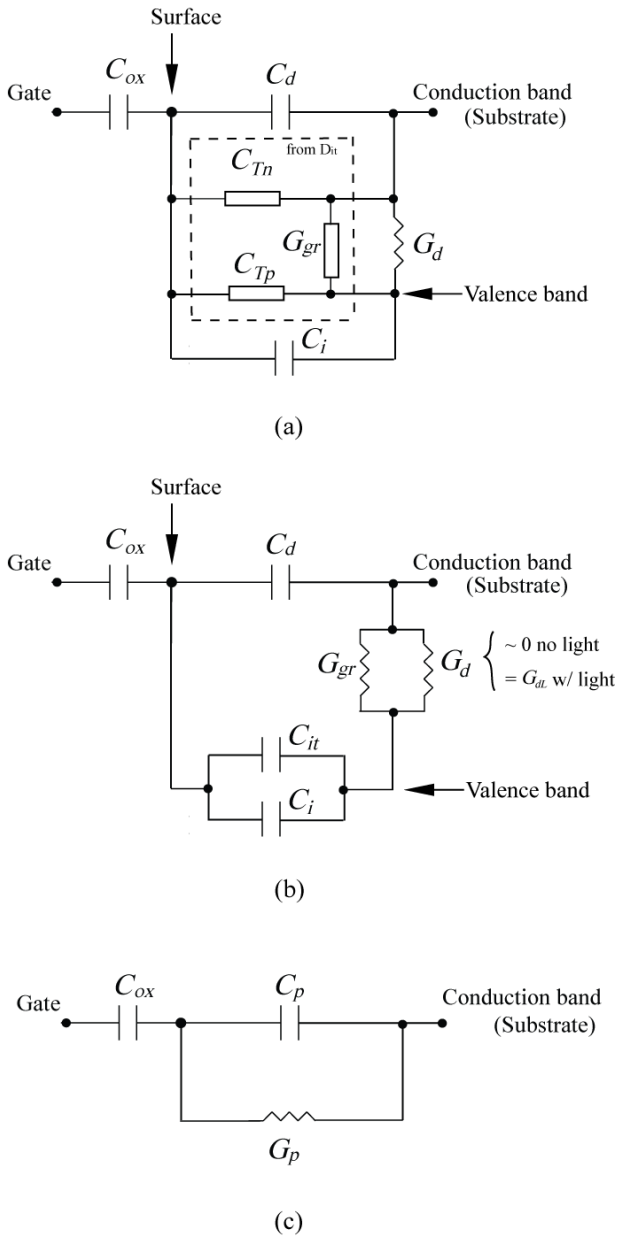
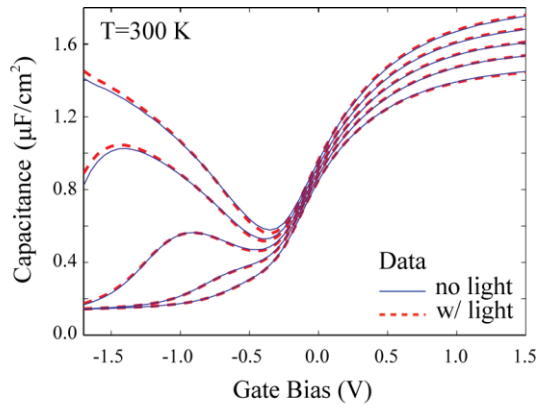


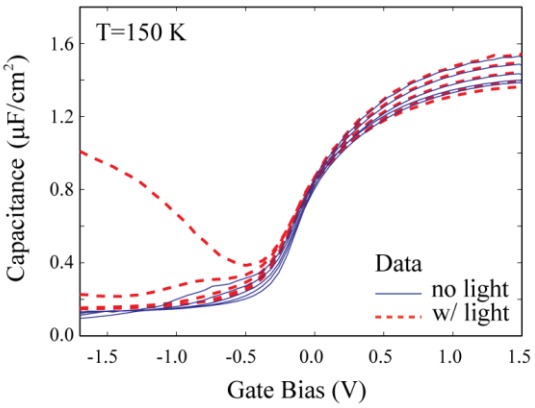
Figure 6.1: (a) Equivalent circuit model of an MOS capacitor (n-type substrate). The dashed rectangle encloses the interface state elements [1]. (b) Simplified equivalent circuit in strong inversion. (c) Circuit that defines $G_p(\omega)$ and $C_p(\omega)$.

6. 3 Data and Model for n-type MOS

Fig. 6.2(a) shows the C-V data measured with and without light at 300 K. Very small modification of the C-V characteristics in the negative gate voltage range was observed. When the MOS was cooled to 150 K, however, the humps from the interface states subside and large increase of measured capacitance induced by light was observed in the same voltage range [Fig. 6.2(b)].



(a)



(b)

Figure 6.2: Measured C-V characteristics of n-$In_{0.53}Ga_{0.47}As$ MOS with and without light illumination at (a) 300 K and (b) 150 K. The frequencies are 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz.

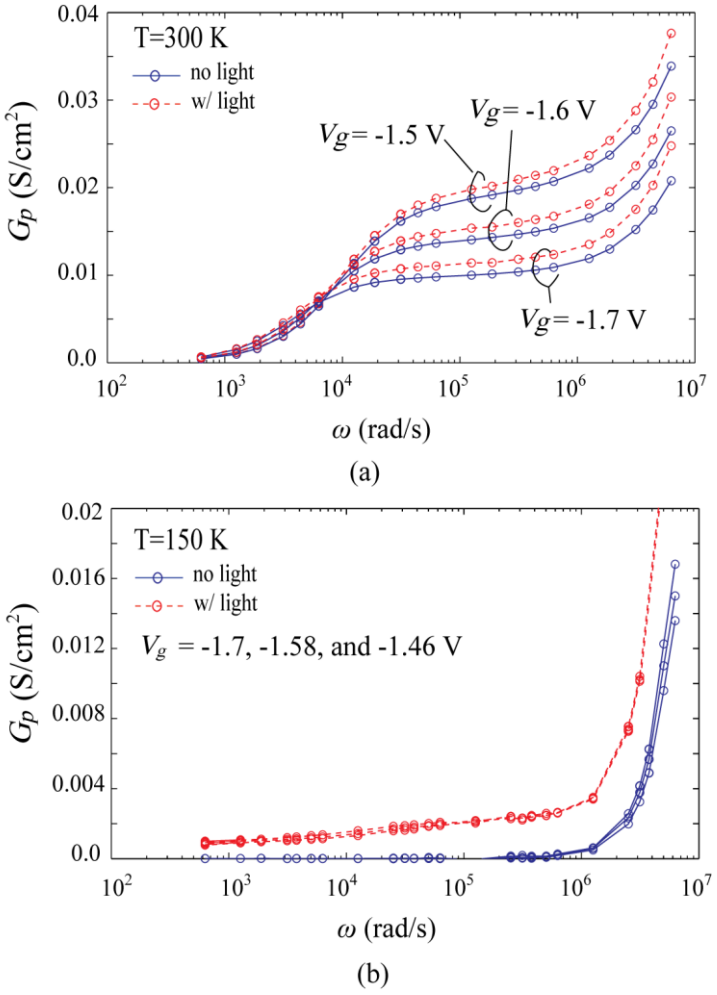


Figure 6.3: G_p versus ω data with and without light for three V_g biases in inversion (n-type substrate) at (a) 300 K and (b) 150 K. C_{ox} = 2.4 μF/cm^2 is assumed to de-embed G_p from MOS data.

Fig. 6.3(a) shows the G_p versus ω data at 300 K for three gate voltages in inversion with and without light. The plateau in the intermediate frequency range is clearly seen. The incremental ΔG_p caused by illumination has an average value of $G_{dL} \approx$ 0.0013 S/cm^2. The dependence of G_{gr} (no light) on bias voltage reflects the increase of τ_n due to depletion of majority carriers going toward stronger inversion. Because of the G_{gr}, which is associated with generation/recombination of the charge carriers through the

interface states and is sufficiently large at room temperature, the effect of light is rather small and constitutes only ~10% of G_p. This is consistent with the relatively little illumination effect observed in Fig. 6.2(a).

To model the light effect in Fig. 6.2(a) in more detail, we focus on the interface state region from the midgap to strong inversion, i.e., at $V_g < -0.2$ V. The border trap dominated region of higher gate biases is not modeled. C-V humps similar to those observed in Fig. 6.2(a) without light have been modeled quantitatively earlier in [2]. To fit the current data set, the interface-state parameters C_{it}, τ_n, and τ_p, as well as the MOS structure parameters C_{ox}, C_d, have been adjusted to the values shown in Fig. 6.4 and caption. The model C-Vs generated with these parameters are shown in Fig. 6.5(a), labeled 'no light'. They generally mimic the data without light in Fig. 6.2(a). Note from Fig. 6.1(b) that in strong inversion, C_{it} and C_i are in parallel hence cannot be separately determined through fitting of the data. The dashed curve in Fig. 6.4(a) represents the expected C_i with a presumed degree of V_g stretchout. It is consistent with the trend of the $C_{it} + C_i$ curve extracted from the fitting. The C-Vs with illumination are then generated by adding the average $G_{dL} \approx 0.0013$ S/cm^2 of the ΔG_p in Fig. 6.3(a) to the G_{gr} of the interface state model. The simulated light effect in Fig. 6.5(a) reproduces what was observed experimentally in Fig. 6.2(a).

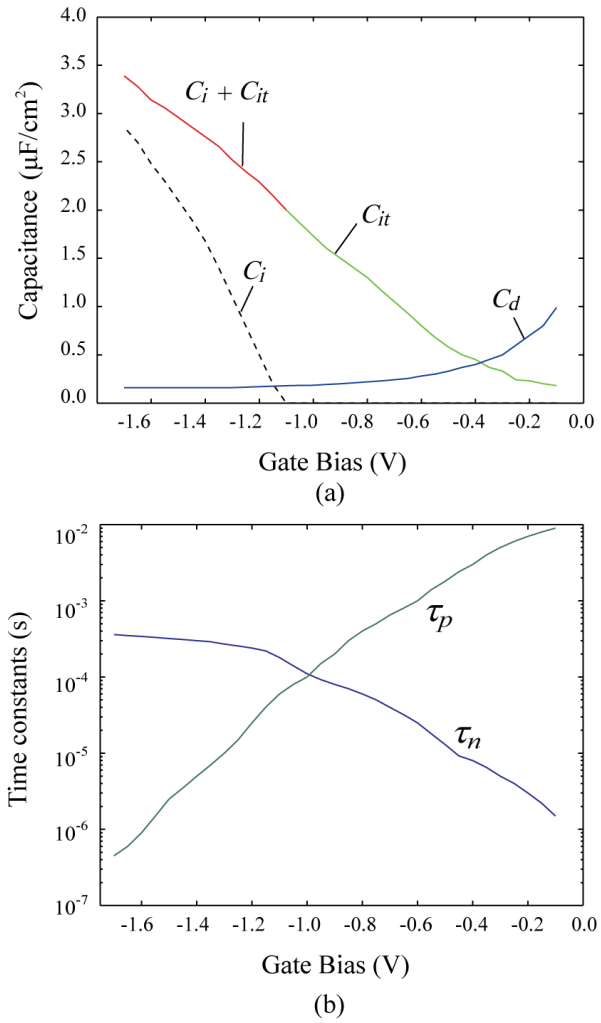


Figure 6.4: Parameters for the 300 K interface state model: (a) C_{it}, C_i, C_d and (b) τ_n, τ_p. C_{ox} is 2.4 μF/cm^2.

Fig. 6.2(b) demonstrates that at 150 K and without illumination in the experiment, the interface state induced C-V humps diminish. This is because at 150 K, τ_n further increases by orders of magnitude due to severe depletion of majority carriers in inversion [$n_s \sim \exp(-q|\psi_s|/kT)$]. Fig. 6.5(b) shows the simulated C-V characteristics without light, which are generated from the 300 K model by multiplying the time constants τ_n by 800 and τ_p by 50 while keeping C_{it} the same. With the humps largely subsided, the C-V data

are not sensitive to the exact choice of τ_n and τ_p. To account for the temperature effect on the inversion threshold, the $C_i(V_g)$ in Fig. 4(a) for 300 K is shifted ≈ 0.15 V further negative in the 150 K model. The conductance data G_p in Fig. 3(b) are essentially zero without light and ≈ 0.001-0.002 S/cm^2 with light. The G_{dL} extracted from the 100 Hz data at –1.7 V is 0.00125 S/cm^2. By adding this value to the model at 150 K, Fig. 6.5(b) reproduces the strong C-V response to light in Fig. 6.2(b). Two points are noteworthy. First, the rise of the 100 Hz capacitance at $V_g > -1.2$ V is due to interface states, not inversion capacitance. Second, even though C_i may be rising steeply after $V_g \approx -1.2$ V, the capacitance measured at 100 Hz is limited by the serial G_{dL}. If we neglect the small C_d in the equivalent circuit of Fig. 6.1(b), the total capacitance is given by the serial combination of C_{ox}, $C_{it} + C_i$, and G_{dL}, or

$$C_{tot} = \frac{C_{ox}^{-1} + (C_i + C_{it})^{-1}}{(\omega G_{dL}^{-1})^2 + \left[C_{ox}^{-1} + (C_i + C_{it})^{-1}\right]^2} \tag{6.5}$$

The above expression has a maximum value of $G_{dL}/2\omega$, which equals 1.0 μF/cm^2 at 100 Hz in our case. As C_{tot} approaches this value, its rate of increase with V_g through C_i slows down as observed in Fig. 6.2(b) and modeled in Fig. 6.5(b).

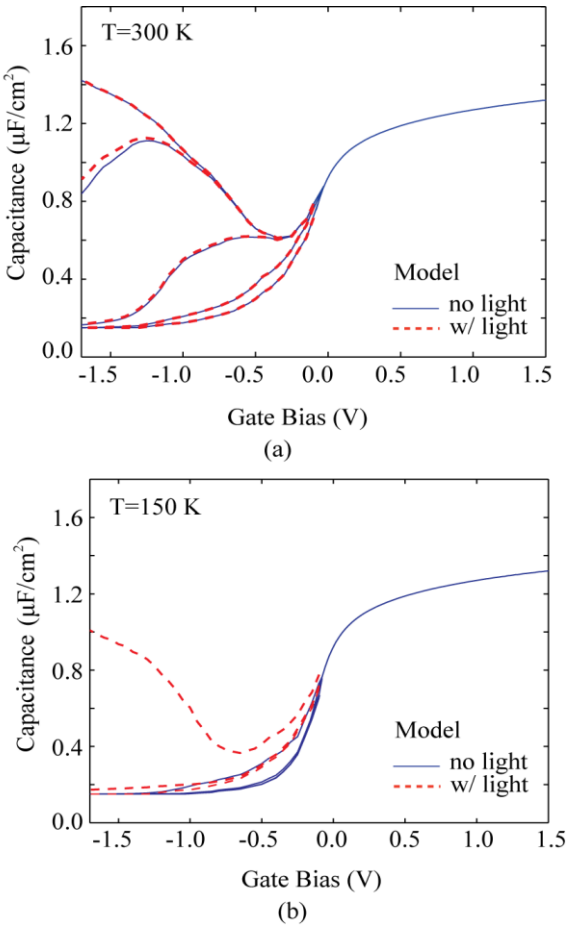


Figure 6.5: Model generated C-V with and without light for (a) 300 K and (b) 150 K. Same frequencies as those in Fig. 6.2 are used.

6. 4 Data and Model for p-type MOS

The C-V characteristics measured at 300 K on an MOS structure with p-type substrate are shown in Fig. 6.6(a). These characteristics show strong frequency dispersions in the accumulation due to border traps near the valence band edge [3], analogous to the border traps near the conduction band edge in the case of n-type substrate. On the other hand, contrary to n-type, no humps in the inversion region of the C-V characteristics are observed. Again, leaving the border traps out of the scope of the

study, we focus on the contrast of surface states between n-type and p-type substrates. With no surface states near the conduction band edge, illumination readily produced strong inversion C-V characteristics at positive gate biases in Fig. 6.6(a). In this case, the 100 Hz capacitance increases more steeply with V_g, indicating very little stretchout. As expected, G_p without light is low and insensitive to gate voltage [Fig. 6.6(b)]. With light, G_p is enhanced by $G_{dL} \approx 0.00133$ S/cm^2, comparable to that in the n-type case.

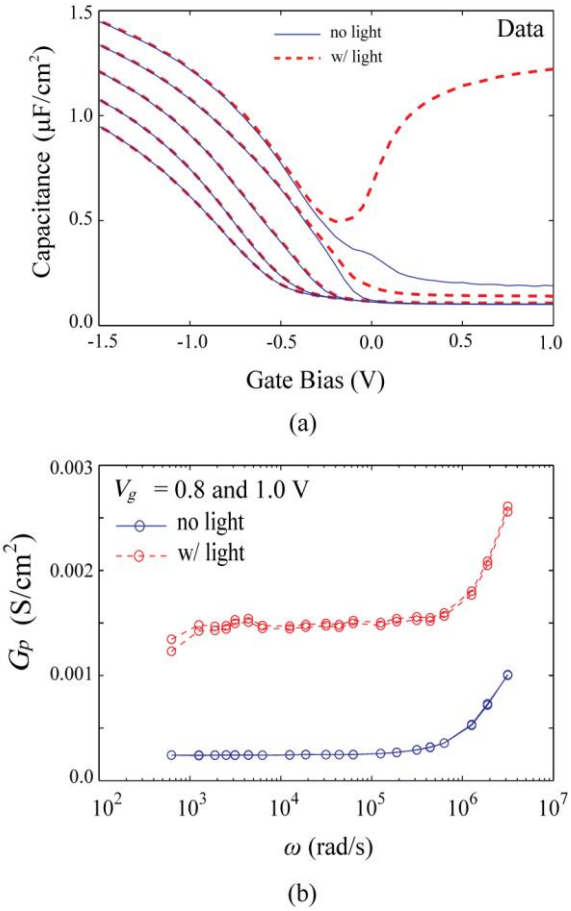


Figure 6.6: (a) C-V data of a p-type InGaAs MOSCAP with and without light at 300 K. The frequencies are 100 Hz, 1 kHz, 10 kHz, 100 kHz, and 1 MHz. (b) G_p versus ω data for two different gate voltages in inversion.

The capacitance and conductance dispersion data at V_g = 1.0 V with and without

light are modeled in Fig. 6.7 assuming frequency independent G_d with no C_{it}. The upturn of G_{tot} above 100 kHz can be explained by series resistance [4].

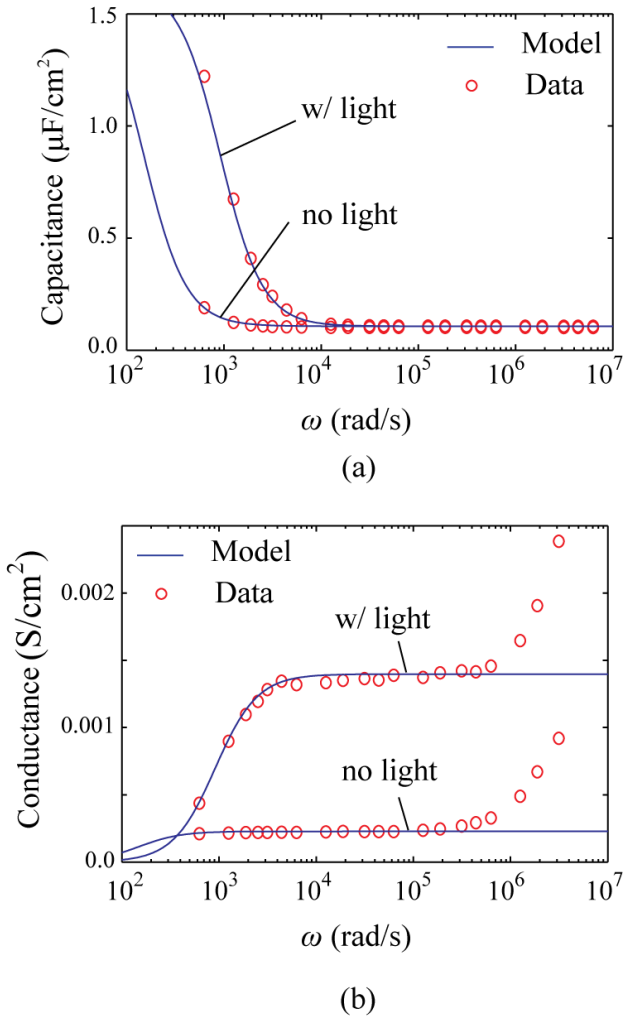


Figure 6.7: Model fitting of (a) capacitance and (b) conductance dispersion data of the MOSCAP in Fig. 6 at V_g = 1 V. Parameters used are C_{ox} = 2.4 μF/cm^2, C_d = 0.12 μF/cm^2, C_i = 5.0 μF/cm^2, and G_d values consistent with Fig. 6(b), namely, 0.00025 S/cm^2 without light, 0.00153 S/cm^2 with light.

In sum, minority carrier response to light illumination is used to identify strong inversion and interface states in $In_{0.53}Ga_{0.47}As$ MOS characteristics. The asymmetric

responses with n-type and p-type substrates verify the significant presence of interface states only in the lower half of the bandgap. It is shown that the conductance data hold the key to the modeling of illumination effect. All the experimental data, n-type and p-type, 300 K and 150 K, with and without light, are satisfactorily explained by adding a light dependent conductance between the conduction band and the valence band to the full interface state model.

The text of Chapter 6, in part, is a reprint of the material as it appears in "Modeling illumination effects on n- and p-type InGaAs MOS at room and low temperatures" by Han-Ping Chen, Dmitry Veksler, Gennadi Bersuker, and Yuan Taur, to be published by IEEE Transaction on Electron Devices. The dissertation author was the primary investigator and author of this paper

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Chapter 7

Conclusion

A comprehensive study on the electrical modeling and characterization of high-*k* / III-V MOS capacitors is presented in this dissertation. Interface traps and bulk-oxide traps effects are explained and simulated in detail by the full D_{it} model and distributed N_{bt} model correspondingly. It is also shown that the two models can be combined in applying to all the bias range and with the existing of both kinds of trap states.

The drawbacks of the previously existing D_{it} extraction methods are addressed. For example, the commonly used 1 MHz frequency in Terman method is not high enough for the measuring capacitance excluding D_{it} effect from flatband to accumulation regions.

On the other hand, the conductance method, which is the most widely applied D_{it} extraction method, is actually a special case of the full D_{it} model. It can be misapplied in the wrong bias region and gives rise to an overestimated D_{it} by mixing with the inversion charge response or N_{bt} response. Besides, there are cases that the false G_p/ω peaks are generated by oxide leakage or high bulk-oxide density when C_{tot} is larger than C_{ox}. Therefore, it is advisable to examine both capacitive and conductive components to rule out the possibility of false G_p/ω peak. It is another fundamental reason why full D_{it} model excels: both capacitive and conductive components are fitted at the same bias. After the overall D_{it} fitting with both capacitance and conductance data, it is revealed that the rise of the low-frequency C-V humps in depletion is due to the increasing D_{it}, while the fall of the humps in inversion is due to the increased time constant for electron capture. The C-V humps then are taken as the signal of D_{it} response.

Similar examinations have been done with the distributed N_{bt} model. It differs from the D_{it} model since the trap states are in the dielectric, and they communicate with semiconductor substrate through tunneling, leading to a broad range and depth dependent time constants. The broad range of time constants correspond to a wide frequency spectrum and result in the observed linear capacitance dispersion. The fitting examples are illustrated in the chapters in extracting the bulk-oxide trap density. It is also shown that the observed upturning $G_{tot}(\omega)$ can be explained by adding series resistance in the model, whereas it has no effect on $C_{tot}(\omega)$. Comparing to the previously existed "lumped circuit model", which produces a curvature in the capacitance versus $\log(\omega)$ plot thus inconsistent with the experimental data, the distributed circuit model is more physical since the locations of the traps are considered. Another problem with the lumped model

is that the trap density that best fits $C_{tot}(\omega)$ data is different from the trap density that best fits $G_{tot}(\omega)$ data. For the distributed model, a single, uniform oxide trap density can fit both $C_{tot}(\omega)$ and $G_{tot}(\omega)$ data at the same time.

The models are also applied and validated in different circumstances. We have shown by model analysis that the observed variations of C-V dispersion with oxide thickness and temperature are consistent with a thickness and temperature independent trap density, whether the dispersion is caused by oxide traps or by interface states. In the case of oxide traps, the normalized dispersion is amplified by the oxide capacitance and is relatively insensitive to changes of time constant due to temperature. For interface states, the humps of dispersion widen and their peaks nearly reach C_{ox} in thick oxides in which $1/(\omega C_{ox})$ is the dominating impedance in the serial circuit. The high-low dispersion of interface states diminishes at low temperatures where the time constant is too long for the traps to follow even the lowest frequency of the measurement. Lastly, the asymmetric responses with n-type and p-type substrates verify the significant presence of interface states only in the lower half of the bandgap. It is shown that the conductance data hold the key to the modeling of illumination effect. All the experimental data, n-type and p-type, 300 K and 150 K, with and without light, are satisfactorily explained by adding a light dependent conductance between the conduction band and the valence band to the full interface state model

Appendix

A. Matlab Code for bulk-oxide electron trap full-interface state model in n-type substrate (Fig. 4.8 (a))

```
%%%%
% This program simulates the total capacitance and conductance as functions
% of freqency in n-substrate MOS structure. Both interface states density
%(Dit) and bulk-oxide trap electron (Nbt) effect are included. Set Nbt=0 as Dit only
% model and Dit=0 as Nbt only model.
%%%%

clear all

q=1.6E-19; % the charge of electron
Cox=1.06e-6; % F/cm^2, oxide capacitance
k0=3.8e7;  % cm-1, kappa - decay factor
t0=1e-9; % second, tau_0 - trap time contant at interface
tox=5e-7; % cm, oxide physical thickness
epslonox= Cox*tox; % oxide permitivity (F/cm)
w=logspace(1,8,100)*2*pi; % rad/s, frequency range
Nox=2000;% mesh number in the oxide
Coxn=Cox*Nox; % incremental oxide capacitance
Nbt=2e19; % cm^-3, bulk-oxide trap density
Cd=2e-6;  % F/cm^2, majority carrier capacitance
Ci=1e-10; % F/cm^2, minority carrier capacitance
Dit=1e12; % cm^-2 eV^-1, interface state density
tn=t0;    % second, trap time constant interacting with CB (n-type substrate)
tp=1e-3;  % second, trap time constant interacting with VB (n-type substrate)
Gd=0;  % S/cm^2, generation and recombination in the bulk
Gdc=0; % S/cm^2, oxide leakage conductance
Gs=1e8; % S/cm^2, series conductance (1/series resistance)

for i=1:length(w)

% CTn, CTp, Ggr and Ybt defined in Chapters 3 and 4
F = @(f)(1-f)./(j*w(i)*f.*(1-f)+f./tp+(1-f)./tn);
[Hcn, errbnd] = quadgk(F,0,1,'RelTol',1e-10);
CTn=q*Dit*Hcn/tn;
F = @(f)f./(j*w(i)*f.*(1-f)+f./tp+(1-f)./tn);
[Hcp, errbnd] = quadgk(F,0,1,'RelTol',1e-10);
CTp=q*Dit*Hcp/tp;
F = @(f)1./(j*w(i)*f.*(1-f)+f./tp+(1-f)./tn);
[Hg, errbnd] = quadgk(F,0,1,'RelTol',1e-10);
Ggr=q*Dit/tn/tp*Hg+Gd;
Y=j*w(i)*(Cd+CTn)+j*w(i)*(Ci+CTp)*(Ggr)*(j*w(i)*(Ci+CTp)+Ggr)^-1;

  for n=1:Nox
      Cpbt=q/w(i)/t0*(Nbt*atan(w(i)*t0*exp(2*k0*tox/Nox*(n-1)))/exp(2*k0*tox/Nox*(n-1))+...
         Nbt*atan(w(i)*t0*exp(2*k0*tox/Nox*(n)))/exp(2*k0*tox/Nox*(n)))*tox/Nox/2;
      Gpbt=q/2/t0*(Nbt*log(1+w(i)^2*t0^2*exp(4*k0*tox/Nox*(n-1)))/exp(2*k0*tox/Nox*(n-1))+...
```

```
        Nbt*log(1+w(i)^2*t0^2*exp(4*k0*tox/Nox*(n)))/exp(2*k0*tox/Nox*(n)))*tox/Nox/2;
    Ypbt=j*w(i)*Cpbt+Gpbt;
    Y=j*w(i)*Coxn*Y./(j*w(i)*Coxn+Y)+Ypbt;
  end

  Y=Y+Gdc;
  Y=Y*Gs/(Y+Gs);
  G_tot(i,:)=real(Y);
  C_tot(i,:)=imag(Y)/w(i);

end

% plot out Ctot and Gtot dispersion simulation results
subplot(2,1,1)
semilogx(w,C_tot,'b');
xlim([1e2 1e6]*2*pi);
xlabel('\omega (rad/s) ');ylabel('Ctot (F/cm^2)');
hold on

subplot(2,1,2)
plot(w,G_tot,'b');
xlim([1e2 1e6]*2*pi);
xlabel('\omega (rad/s) ');ylabel('Gtot (S/cm^2)');
hold on
```

B. Matlab Code for bulk-oxide hole trap full-interface state model in n-type substrate (Fig. 4.8 (b))

```
%%%%
% This program simulates the total capacitance and conductance as functions
% of freqency in n-substrate MOS structure. Both interface states density
%(Dit) and bulk-oxide hole trap (Nbt)effect are included. Set Nbt=0 as Dit only
% model and Dit=0 as Nbt only model.
%%%%

clear all

q=1.6E-19; % the charge of electron
Cox=1.06e-6; % F/cm^2, oxide capacitance
k0=4.5e7;  % cm-1, kappa - decay factor
t0=1e-9; % second, tau_0 - trap time contant at interface
tox=5e-7; % cm, oxide physical thickness
epslonox= Cox*tox; % oxide permitivity (F/cm)
w=logspace(1,8,100)*2*pi; % rad/s, frequency range
Nox=2000;% mesh number in the oxide
deltx=tox/Nox; % incremental x
Coxn=Cox*Nox; % incremental oxide capacitance
Nbt=0e19; % cm^-3, bulk-oxide trap density
Cd=2e-7;  % F/cm^2, majority carrier capacitance
Ci=2e-6; % F/cm^2, minority carrier capacitance
Dit=5e12; % cm^-2 eV^-1, interface state density
tn=1e-3;    % second, trap time constant interacting with CB (n-type substrate)
tp=t0;  % second, trap time constant interacting with VB (n-type substrate)
```

```
Gd=0;  % S/cm^2, generation and recombination in the bulk
Gdc=0; % S/cm^2, oxide leakage conductance
Gs=1e8; % S/cm^2, series conductance (1/series resistance)


for i=1:length(w)

F = @(f)(1-f)./(j*w(i)*f.*(1-f)+f./tp+(1-f)./tn);
Hcn = quadgk(F,0,1);
CTn=q*Dit*Hcn/tn;
F = @(f)f./(j*w(i)*f.*(1-f)+f./tp+(1-f)./tn);
Hcp = quadgk(F,0,1);
CTp=q*Dit*Hcp/tp;
F = @(f)1./(j*w(i)*f.*(1-f)+f./tp+(1-f)./tn);
Hg = quadgk(F,0,1);
Ggr=q*Dit/tn/tp*Hg+Gd;

% Δ-Y circuit transform
C1=CTn+Cd;
C2=CTp+Ci;
R1=((Ggr))/((j*w(i)*C1)*(j*w(i)*C2)+(j*w(i)*C1)*Ggr+(j*w(i)*C2)*Ggr);
R2=((j*w(i)*C2))/((j*w(i)*C1)*(j*w(i)*C2)+(j*w(i)*C1)*Ggr+(j*w(i)*C2)*Ggr);
R3=((j*w(i)*C1))/((j*w(i)*C1)*(j*w(i)*C2)+(j*w(i)*C1)*Ggr+(j*w(i)*C2)*Ggr);

for nn=1:tox/deltx;

 x=nn*deltx;
 if x<1E-7
 R1=R1+(j*w(i)*epslonox/deltx)^-1;
 if k0*x > 300
    delt_Ybt=0;
 else
 delt_Ybt=q*Nbt*log(1+j*w(i)*t0*exp(2*k0*x))*deltx/(t0*exp(2*k0*x));
 end
 else
    delt_Ybt=0;
 end
 R_bt=1/delt_Ybt;
 R1=R1/(R1/R_bt+R3/R_bt+1);
 R2=R1*R3/(R1+R_bt+R3)+R2;
 R3=R3/(R1/R_bt+R3/R_bt+1);
end
Rtot=R1+R2;
Ytot=1/Rtot;
Ytot=Ytot+Gdc;
Ytot=Ytot*Gs/(Ytot+Gs);
C_tot(i)=imag(Ytot)/w(i);
G_tot(i)=real(Ytot);
end

% plot out Ctot and Gtot dispersion simulation results

subplot(2,1,1)
semilogx(w,C_tot,'b');
```

```
xlim([1e2 1e6]*2*pi);
xlabel('\omega (rad/s) ');ylabel('Ctot (F/cm^2)');
hold on

subplot(2,1,2)
plot(w,G_tot,'b');
xlim([1e2 1e6]*2*pi);
xlabel('\omega (rad/s) ');ylabel('Gtot (S/cm^2)');
hold on
```