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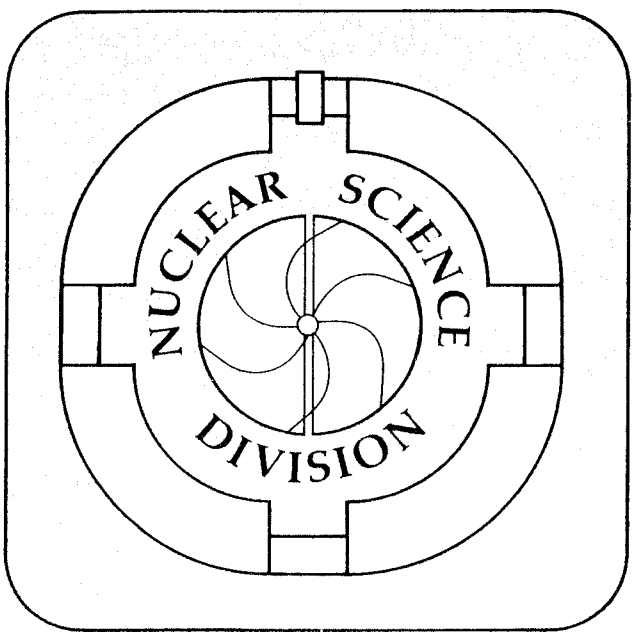

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Quad Fourfold (4x4) Logic Unit (LBL #21X6421 P-1)*

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Abstract

A quad fourfold (4x4) logic unit has been designed and packaged in a single-width NIM module for use in nuclear and atomic physics experiments. The four inputs of each unit are combined internally to perform logical AND, OR, and VETO functions. A set of eight DIP switches on the front panel select either the input signal or its complement, trigger slope, output pulse duration, and positive or negative logic on the overlap signal. A one-shot multivibrator may be triggered on either the positive or negative-going slope of the overlap signal to form the shaped output. The output width can be adjusted between ~50 ns and 50 μsec with two coarse ranges and a twenty-turn potentiometer. An LED attached to the one-shot gives a visual indication of the output rate.

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1. Introduction:

Most modern experiments in nuclear and atomic physics involve several detectors, and besides data from individual detectors (singles), one typically wants to restrict data to events where more than one detector fired within a given time window (coincidences). While it is desirable to take relatively unrestricted event-by-event data on magnetic tape and put in restrictions during the off-line analysis, often these rates would be too high and some triggering conditions are needed to filter out most of the unwanted data. Electronic logic modules, such as this 4x4 logic module, set hardware conditions such as AND, OR, and VETO to determine the accepted and rejected data. Considering the number of channels in modern detector arrays, typically tens to hundreds, compactness is important. Thus, we have tried to standardize on "quad" modules that pack four units into a single NIM module. The quad fourfold (4x4) logic module described herein and depicted in figure 1 allows one to easily perform the common AND, OR, and VETO functions. The unit generates an overlap output, a positive TTL output, and two negative NIM logic outputs of adjustable duration.

2. Operation:

The four-fold logic module accepts up to four negative NIM logic inputs and combines them to form an **X** (overlap) signal. When this signal changes state, either from LOW (L) to HIGH (H) or from HIGH to LOW, a one-shot multivibrator circuit is triggered to form a negative NIM output of adjustable duration. The operation of the four-fold logic module is governed by the input signals and the switch settings on the front panel (Figure 2). In this paper, the connectors are referred to in the **bold** letters **A, B, C, D, X,** and **Y.** The top four switches labeled A, $\underline{A}$; B, $\underline{B}$; C, $\underline{C}$; and D, $\underline{D}$ control the inputs and therefore the logic functions. Note than on the module front panel, there is a "bar" on top of the letter, but in this paper it is easier to show it as an _ . The next two switches, labeled X, + and $\underline{X}$, + affect the X (overlap) and $\underline{X}$ (overlap complement) outputs and add +700 mV to those signals to provide positive fast logic outputs. This also interchanges the **X** and $\underline{X}$ outputs. The next switch is labeled $\uparrow$ and $\downarrow$ to indicate which slope of the **X** (overlap) signal the one-shot output will trigger on. One will normally trigger on the $\uparrow$ slope for OR functions and the $\downarrow$ slope for AND functions to set the timing on the leading edge of the overlap pulse. The bottom switch, labeled S and L, denotes short (~50 ns to 1.1 μsec) or long (~0.9 μsec to 50μsec) duration of the **Y** (output) pulse.

The operation of this module is based on a rather elegant combination of the MC10113 and MC10198 Motorola Emitter Coupled Logic (MECL) chips shown schematically in figure 3. The MC10113 is an exclusive OR (XOR) gate and its operation is governed by the following set of rules (truth table 1):

		INPUT 1	
	XOR	L	H
	L	L	H
INPUT 2			OUTPUTS
	H	H	L

Each input consists of two parts XORed together: one part is the external signal and the other is an internal level set by the A,A etc. switches. The outputs of the XORs are wire ORed together. This means that if any one or more of the XOR outputs are in the HIGH state, the output will be HIGH. Only if all outputs are in the LOW state will the output be LOW. This operation is governed by the following set of rules (truth table 2):

	A	L	H	O	O	O
INPUTS	B	L	O	H	O	O
	C	L	O	O	H	O
	D	L	O	O	O	H
OVERLAP	X	L	H	H	H	H

Where the O represents either the LOW or HIGH state, and the result is independent of which state it is in. Figure 3 shows the four XORs ORed together to form the **X** (overlap) signal which triggers the MC10198 one-shot multivibrator. This unit can trigger on either a positive- or negative-going **X** (overlap) pulse depending on an external setting (the trigger slope switch on the front panel). **Before proceeding, one should become very familiar with the schematic (figure 3) and the front panel connectors and controls (figure 2).**

Associated with each input to the XOR, (**A,B,C,** and **D**); there is an additional internal input associated with the position of the A,A, etc. switches. In the quiescent state, that is with no external input signal, the external input is resting in a HIGH state. The internal input may be HIGH or LOW depending on the position of the switches A,A, etc. The XOR outputs depend on the inputs according to truth table 1. The XORs for each of the four inputs are ORed together to form the **X** (overlap) signal. Note that if any one or more of the XOR circuit outputs is in the HIGH state, the output is also in the HIGH state as shown in truth table 2. Only if all XOR outputs are in the LOW state is the output in the LOW state. Note also that the **X** signal can change either from LOW to HIGH or HIGH to LOW, and the slope of the trigger may be set to time off either the leading edge or the trailing edge of the overlap signal. Normally, one will time off the

leading edge of the overlap signal. As a practical matter, only if all A, B, C, and D are in the _ position (regular OR function) should one use the ↑ slope on the trigger. One should examine the **X** output with an oscilloscope and set the trigger slope to match the leading edge of the overlap. **CAUTION: Any time one changes the logic function of the module, they should make sure they are still timing off the desired slope of the overlap signal; otherwise the timing of the output may be adversely affected and the rest of the circuit may not function properly.**

To understand the functioning of the logic module, we will study three examples. First, we will consider the use of the four-fold logic module as a simple OR. To do this, all switches A, B, C, and D should be in the _ position and the trigger slope should be set for ↑. Because the input switches are in the _ position, the internal side of each XOR gate will be set in the HIGH state, the same as the quiescent external inputs. Thus, the quiescent outputs of the XORs will be LOW according to truth table 1 and as shown in figure 3. The overlap **X** signal will be resting LOW also. A negative NIM input to any one of the inputs **A**, **B**, **C**, or **D** will drive that input LOW, and the output of that XOR HIGH and therefore the **X** signal HIGH as determined from truth table 2 and shown in figure 3. Since the trigger slope is set for ↑, an output will be generated from the leading edge of the overlap signal.

As a second example, we consider a simple AND between the **A** and **B** inputs. Here the A and B switches are set in the normal position and the C and D switches are in the _ position. If the C and/or D switches were also in the normal position, they would be included in the AND. As shown in figure 4a, the quiescent outputs of the XORs for C and D are LOW since both their internal and external inputs are in the HIGH state . The quiescent outputs of the XORs associated with A and B are, on the other hand, in the HIGH state since the A,$\underline{A}$ and B,$\underline{B}$ switches are in the normal position. Thus, as shown in figure 4a, the quiescent **X** (overlap) signal is HIGH since at least one XOR output signal is HIGH. An input to either **A** or **B** will drive the A or B XOR output LOW, but since the other will remain HIGH, no output will be triggered. If, however, both **A** and **B** inputs are driven LOW together, ALL XOR output signals go LOW, and the **X** signal changes from HIGH to LOW. With the trigger set on the ↓ position, an output will be generated from the leading edge of the overlap signal.

As a third and final example, consider the same situation as above, except that a negative NIM logic signal comes into the **C** input preceding and of longer duration than the **A** and **B** signals. This is shown in figure 4b. Remember that the quiescent output of the C XOR was LOW (as is D), and that a negative NIM input to **C** will drive it HIGH. Now, even when the **A** and **B** inputs arrive in time, driving both their XOR outputs low, the C XOR output will remain HIGH, and no output will be triggered since there will be no signal level change at the input to the one-shot. This is an application of the VETO function.

3. Summary:

This manual describes the operation of the LBL #21X-6421 P-1 quad fourfold (4x4) logic unit. Functions such as AND, OR, and VETO may be selected by the proper combination of the input and trigger-slope switches. Because of the emitter-coupled logic (ECL) circuitry used, the module will accept high rates. The overlap of all inputs generates a **X** (overlap) signal which triggers a shaped one-shot multivibrator to provide a **Y** (output) signal having a time duration of between ~50 ns and 50 μsec.

4. Specifications:

Inputs: Four each, fast negative NIM logic, internally terminated with 50Ω.
Maximum input frequency = ~1 / output pulse width

Outputs: **X** (overlap) and $\underline{X}$ (overlap complement): Negative NIM logic.
Y (one-shot shaped output, ~50 ns to ~50 μsec.) : Two NIM, one TTL.

Latency: ~5 ns between the input and the leading edge of the **X** signal, and ~5 ns between the **X** signal and the leading edge of the **Y** outputs

Operating Modes: Logic functions, including AND, OR, and VETO.

Indicator lights: A LED on the output indicates the rate.

Power: +6 (200 mA), -6 (900 mA)

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Figure Captions

Figure 1. Picture of the 4x4 Logic module from the front (left picture) and from the back and side (right picture). One cover is removed to show the details of construction.

Figure 2. Illustration of the front panel and description of the controls and connectors. The eight DIP switches control the inputs, outputs, and logic functions.

Figure 3. Illustration of the 4x4 logic module configured as a simple OR gate with one input. The **bold** letters **A, B, C,** and **D** represent the inputs and **X** and **Y** represent the outputs. The letters A, B, etc, represent the switch positions for the input / complement switches. H and L are for HIGH and LOW respectively, and represent the quiescent state of the signals. The signals shown schematically represent changes to the quiescent signals. On the right is a timing diagram showing the inputs, the XOR outputs, and the **X** and **Y** outputs. Again, H and L represent the quiescent states.

Figure 4. a) Illustration of the 4x4 logic module used for the AND function.
b) Illustration of the 4x4 logic module used for the AND function with an additional VETO signal on the C input.

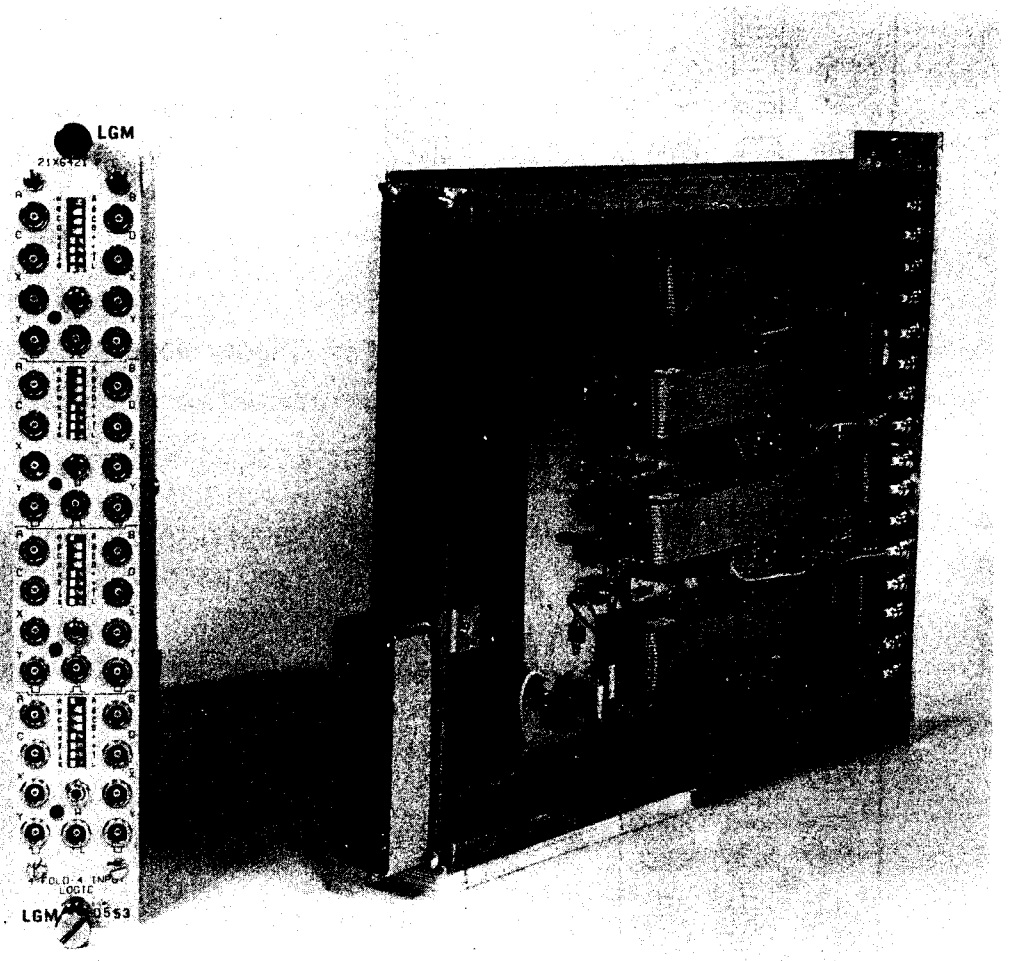

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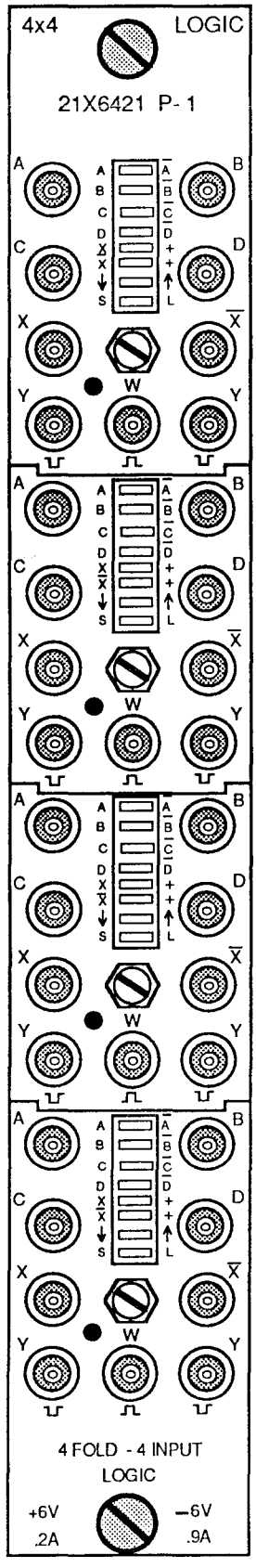
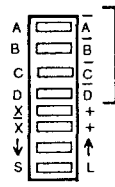
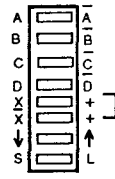
Figure 1

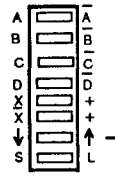




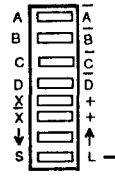
Selects normal or complement (Low or High) internal inputs



Add 700 mV to X and $\underline{X}$ for positive logic



Trigger slope



Short (<50 ns) and Long (<50 µsec) output width

← Input Connectors **A, B, C, D**

← **X** and $\overline{\mathbf{X}}$ (overlap) connectors

← **Y** shaped outputs
(2 NIM, 1 TTL)

← **Y** output width fine adjust

← Input rate LED

Figure 2

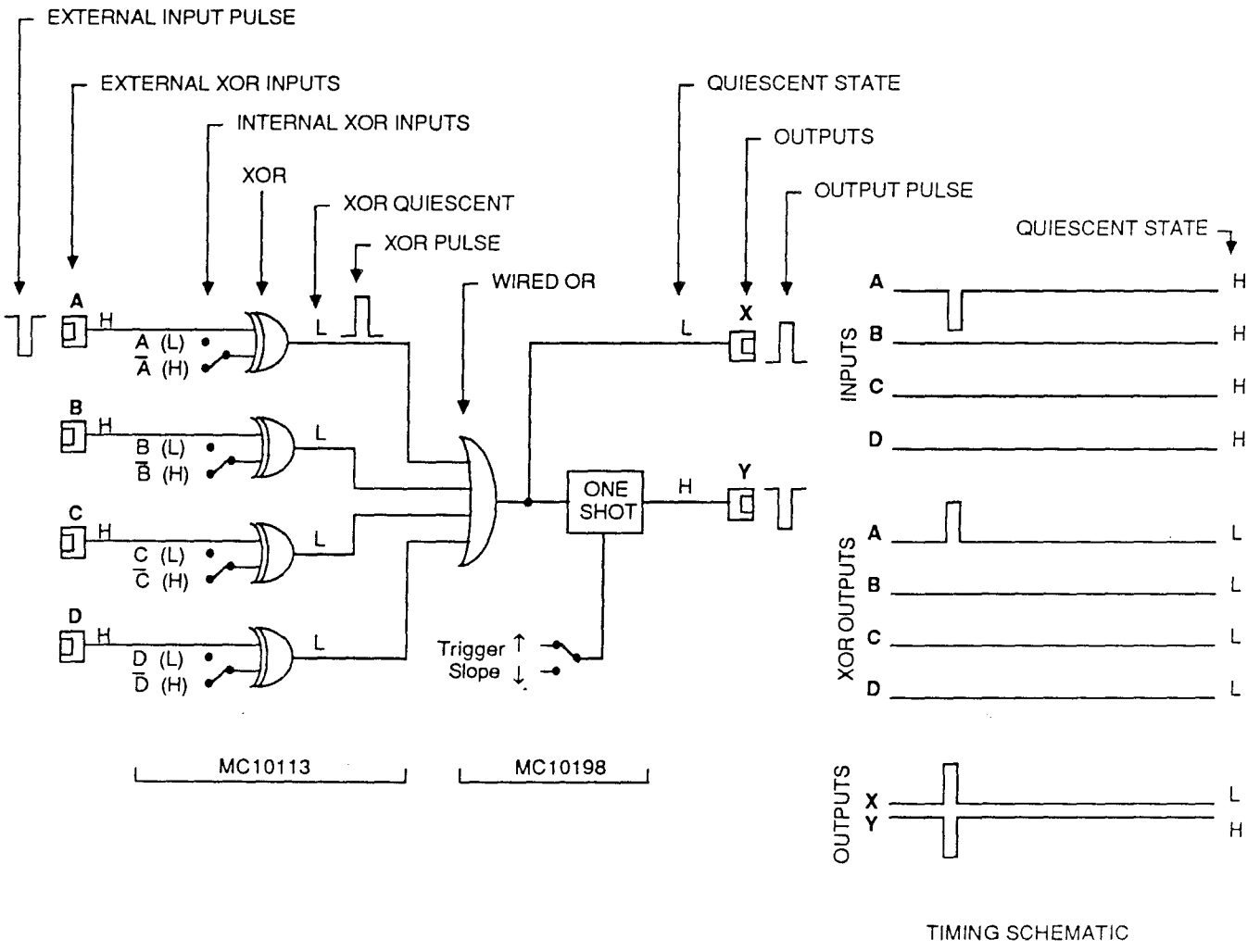

EXTERNAL INPUT PULSE
EXTERNAL XOR INPUTS
INTERNAL XOR INPUTS
XOR
XOR QUIESCENT
XOR PULSE
WIRED OR
QUIESCENT STATE
OUTPUTS
OUTPUT PULSE
A
B
C
D
H
L
A (L)
Ā (H)
B (L)
B̄ (H)
C (L)
C̄ (H)
D (L)
D̄ (H)
ONE SHOT
X
Y
Trigger ↑
Slope ↓
MC10113
MC10198
QUIESCENT STATE
INPUTS
XOR OUTPUTS
OUTPUTS
TIMING SCHEMATIC

Figure 3

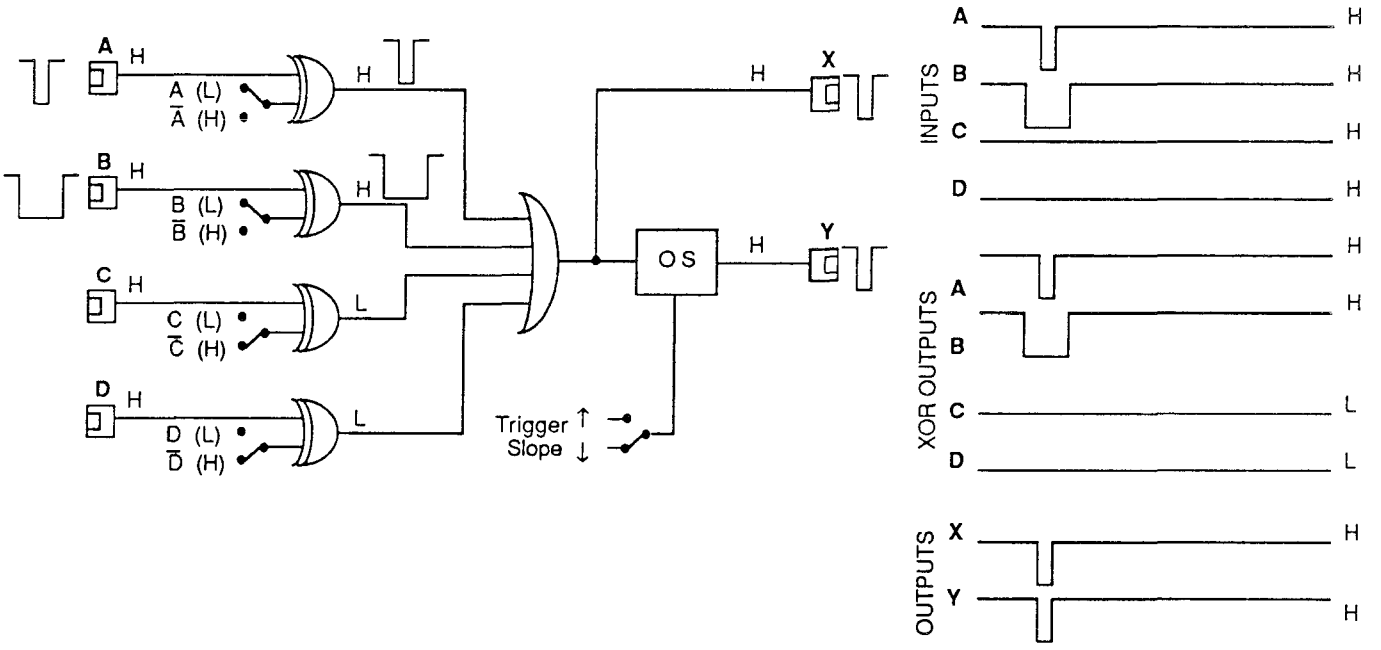


Figure 4a

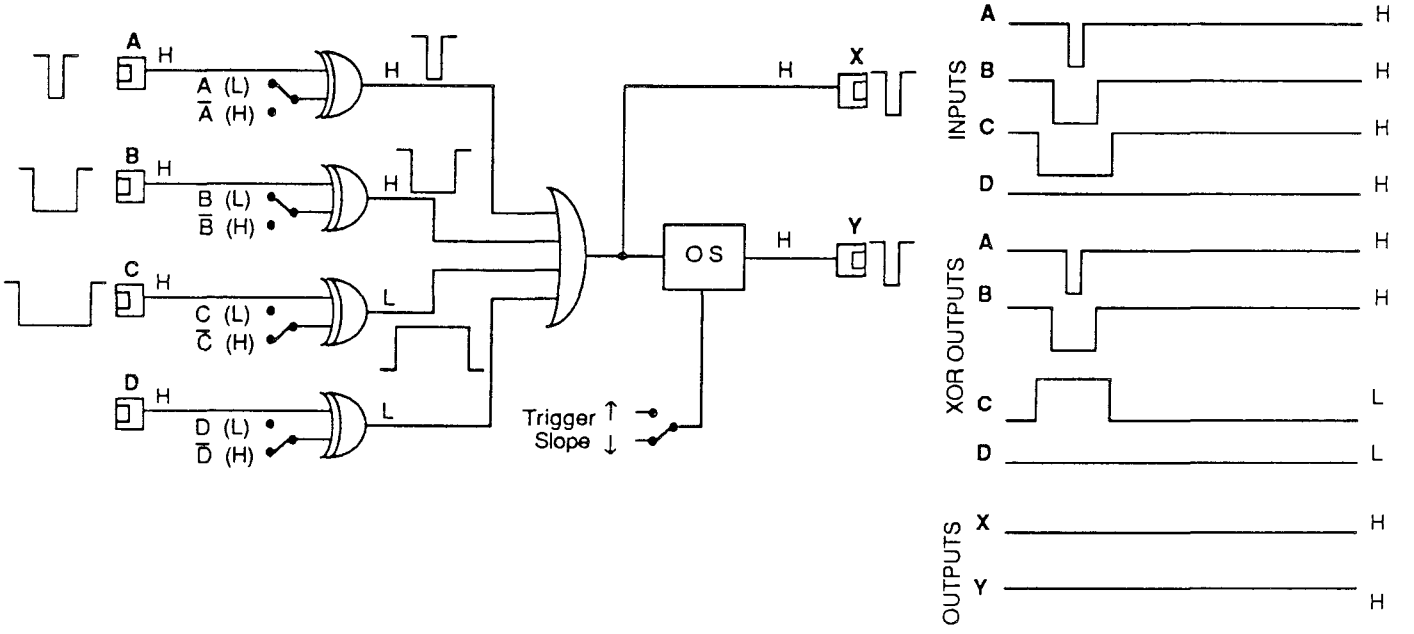


Figure 4b