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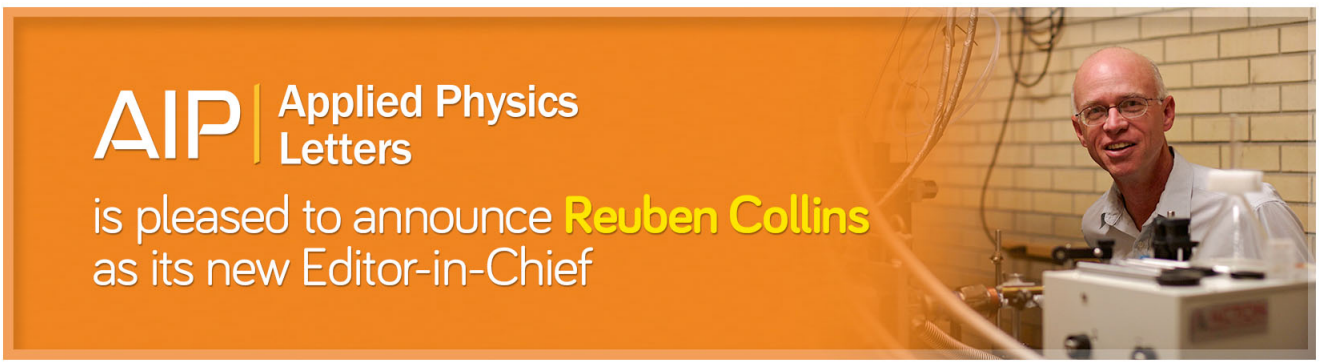

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Extremely scaled high-*k*/$In_{0.53}Ga_{0.47}As$ gate stacks with low leakage and low interface trap densities

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Highly scaled gate dielectric stacks with low leakage and low interface trap densities are required for complementary metal-oxide-semiconductor technology with III-V semiconductor channels. Here, we show that a novel pre-deposition technique, consisting of alternating cycles of nitrogen plasma and tetrakis(dimethylamino)titanium, allows for HfO_2 and ZrO_2 gate stacks with extremely high accumulation capacitance densities of more than 5 $\mu F/cm^2$ at 1 MHz, low leakage current, low frequency dispersion, and low midgap interface trap densities ($10^{12}\,cm^{-2}eV^{-1}$ range). Using x-ray photoelectron spectroscopy, we show that the interface contains TiO_2 and small quantities of In_2O_3, but no detectable Ga- or As-oxides, or As-As bonding. The results allow for insights into the microscopic mechanisms that control leakage and frequency dispersion in high-k/III-V gate stacks.
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I. INTRODUCTION

III-V semiconductors have much lower carrier effective masses than Si, which allows for high velocities. They are currently under active investigation to replace Si as the channel in large-scale integrated digital circuits.[1,2] The advantage of a low carrier mass is, however, offset by a low density of conduction band states, which limits achievable carrier densities and thus negatively affects the transistor transconductance. This issue has become known as the "density of states bottleneck."[3,4] To allow for device scaling to nm-dimensions, gate dielectrics with very high dielectric constants (k) are required for large capacitance densities, low tunneling leakage, and to mitigate the density of states bottleneck.[3]

To date, significant efforts have focused on optimizing the interface quality of high-*k*/III-V interfaces, with remarkable success. For example, the midgap trap densities (D_{it}) for gate stacks with high-*k* HfO_2 and ZrO_2 dielectrics, which can achieve sub-nm equivalent oxide thickness (EOT), are now in the $10^{12}\,cm^{-2}eV^{-1}$ range.[5–8] Such interfaces allow for excellent transistor performance, including subthreshold slopes of 61 mV/dec and record transconductance.[9,10] Near-ideal subthreshold slopes indicate that the interface is not degraded by interface traps. A common attribute of nearly all high quality high-*k*/III-V interfaces is the presence of an Al-oxide interface layer, which is either deposited intentionally, or forms during a pre-deposition cleaning process.[5–7,11–13] For example, high-performance HfO_2 and ZrO_2 dielectrics use an *in-situ*, cyclic, pre-deposition tri-methylaluminum (TMA)/nitrogen plasma cleaning process that leads to the formation of a thin Al_2O_3 layer at the interface.[6,11,14] The presence of Al_2O_3 severely limits capacitance (or EOT) scaling, because the interface layer is connected in series with the high-*k* dielectric and Al_2O_3 has a very low dielectric constant (~8). EOT scaling will therefore require either significantly thinning this layer, or replacing it with one that has a higher capacitance density. Furthermore, this must be achieved without degrading other key properties, in particular, interface trap density and leakage.

TiO_2 has the highest dielectric constant among all binary oxides.[15] Unlike the case for Si,[16] TiO_2 is thermally stable in contact with III-V semiconductors.[17,18] Furthermore, Ti has excellent oxygen gettering properties,[19] which aids in the reduction of native III-V oxides that can be responsible for high D_{it}.[20–23] Abrupt $TiO_2/In_{0.53}Ga_{0.47}As$ interfaces are possible.[17] Here, we report on a method to replace the low-*k* Al-oxide interface layer with a higher-*k* Ti-oxide. We show that this can be achieved without degrading the interface quality. In combination with ZrO_2 and HfO_2 dielectrics, Ti-oxide-based interface passivation layers allow for extremely high capacitance densities that exceed the highest reported values by almost a factor of two, while maintaining low D_{it}. Crystalline TiO_2 has a negligible conduction band offset with $In_{0.53}Ga_{0.47}As$, and one may thus predict a large increase in leakage for n-type channels, compared to wide-band gap, Al-oxide based interlayers.[17,24] Contrary to this, we show that gate stacks with Ti-oxide based interface layers show *low* leakage, similar to what is found for gate stacks with Al_2O_3 interface layers. Furthermore, the frequency dispersion in accumulation, a known problem of high-k/III-V interfaces,[25] is lower than that of aggressively scaled stacks with Al_2O_3 interface layers.

II. EXPERIMENTAL

MOSCAP structures were fabricated on 300-nm-thick, *n*-type $In_{0.53}Ga_{0.47}As$ (Si: $1 \times 10^{17}\,cm^{-3}$) epitaxial layers grown by molecular beam epitaxy on (001) n^+-InP (IntelliEpi, Richardson, Texas). Surfaces were cleaned in buffered HF for 3 min before they were transferred to the atomic layer deposition (ALD) reactor (Oxford Instruments FlexAL ALD). The ALD substrate temperature was set at 300 °C. Samples were heated in hydrogen atmosphere for 3 min. The $In_{0.53}Ga_{0.47}As$ channel surface preparation was carried out *in-*

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situ in the ALD system by exposing the surface to cycles consisting of alternating exposures to nitrogen plasma and pulses of tetrakis(dimethylamino)titanium (TDMAT), which is a common ALD precursor for Ti-based layers. This process is very similar to one that uses nitrogen or hydrogen plasma and TMA, reported previously,[6,11,14,26] except that here the TMA was replaced with TDMAT. Each of these cycles consisted of a nitrogen gas set-up step (3 s, 20 mTorr, 20 sccm), a nitrogen plasma pulse (2 s, 20 mTorr, 100 W inductively coupled plasma forward power), a pump step (2 s), a TDMAT dose (500 ms, 200 mTorr, Ar bubbler 100 sccm), a hold step (1 s), followed by purge (3 s) and pump (2 s). The deposition chamber was isolated from the plasma chamber during TDMAT dose to avoid contamination to the plasma chamber. Additional nitrogen plasma and pump steps were added to the end of these cycles. After a fixed number of these cycles, HfO_2 and/or ZrO_2 dielectrics were deposited. The hafnium and zirconium precursors were TEMAHf (tetrakis[ethylmethylamino]hafnium) and TEMAZr (tetrakis[ethylmethylamino]zirconium), respectively. Details of the high-k dielectric deposition are described elsewhere.[6,11,14] Variable angle spectroscopic ellipsometry was used to determine the oxide thicknesses on Si pieces, and thickness were also confirmed using STEM. After ALD, plasma-enhanced chemical vapor deposition was used to deposit 500 nm of SiO_2 on the sample backside to protect the InP substrate. The samples were annealed at 400 °C for 15 min in a tube furnace in forming gas (95% N_2 and 5% H_2). A thermal evaporator was used to deposit metal contacts. 80-nm-thick Ni top contacts (7.8×10^{-5} cm^2) were evaporated through a shadow mask. The back Ohmic contact, consisting of Cr (20 nm)/Au (100 nm), was deposited after SiO_2 removal.

Frequency-dependent capacitance-voltage (CV) and conductance-voltage measurements were carried out in the dark from 1 kHz to 1 MHz using an impedance analyzer (Agilent 4294 A). A 300 kV field-emission transmission electron microscope (FEI Titan 80–300) was used for obtaining high-angle annular dark-field scanning transmission electron microscopy (HAADF/STEM) images.

The interface chemistry was investigated using X-ray photoelectron spectroscopy (XPS) (Kratos Axis Ultra DLD). Scans were run using monochromatic Al Kα radiation at a pass energy of 20 eV. The energy scales were calibrated by setting the surface aliphatic hydrocarbon peak to 285.0 eV. For quantification, no attempt was made to correct for the fact that layers have different distances to the surface. The relative sensitivity factors used were: Ti $2p = 7.8$ and In $3d = 35$ (In $3d^{5/2} = 21$). Scofield's values were modified in some cases by results on standards that can be related back to carbon. For Ti, results on a TiC standard (using high-resolution fits to uniquely identify the carbide peaks) showed that no changes were needed to the Scofield value of 7.8. For In, InN was used, with another standard being used to relate N to C.

III. RESULTS

Figure 1 shows In 3d and Ti 2p XPS data for two samples with sufficiently thin (~1 nm) ZrO_2 dielectrics to allow for significant signal from the interface. The ZrO_2 dielectric avoids the issue of Hf peaks overlapping with In, Ga, and As peaks, as is the case for HfO_2.[6,11] The surfaces were subjected to 9 and 4 nitrogen plasma/TDMAT cycles, respectively, prior to the dielectric ALD. The thin lines are fits to the experimental data. The fits to the In $3d^{5/2}$ peaks, at 444.3 eV, are consistent with InGaAs.[27] Because of the overlap with As Auger and In loss signals, Ti 2p peaks were extracted by subtracting the signal from an ~1 nm Al_2O_3/$In_{0.53}Ga_{0.47}As$ sample without Ti. This background subtraction removed the low-intensity peaks at 461 and 468 eV, associated with As Auger. The Ti $2p^{3/2}$ peaks appear at 458.7 eV, consistent with TiO_2 bonding. We note, however, that sufficient uncertainty exists in the fitting of the Ti peak that it could also be fitted with similar confidence by including an additional set of peaks at 457.1 eV and 463.3 eV, corresponding to Ti^{3+}, which could be associated with a suboxide and/or some Ti-N or Ti-O-N bonding. In such a fit, these peaks are about 20% as large as the TiO_2 peaks, therefore possibly equating to something like a monolayer within a 5-atom thick Ti layer. Detecting N directly is difficult in these XPS studies because of the N 1s-Ga Auger interference. Comparison of the results for the two samples shows that the sample with 9 cycles of the pretreatment contained a greater amount of Ti than the interface subjected to 4 cycles, as the ratio of Ti:In increases from 0.65 to 0.92. A higher binding energy component (shaded area) of In $3d^{5/2}$ is detected at 445.3 eV, indicating the presence of In_2O_3.[28]

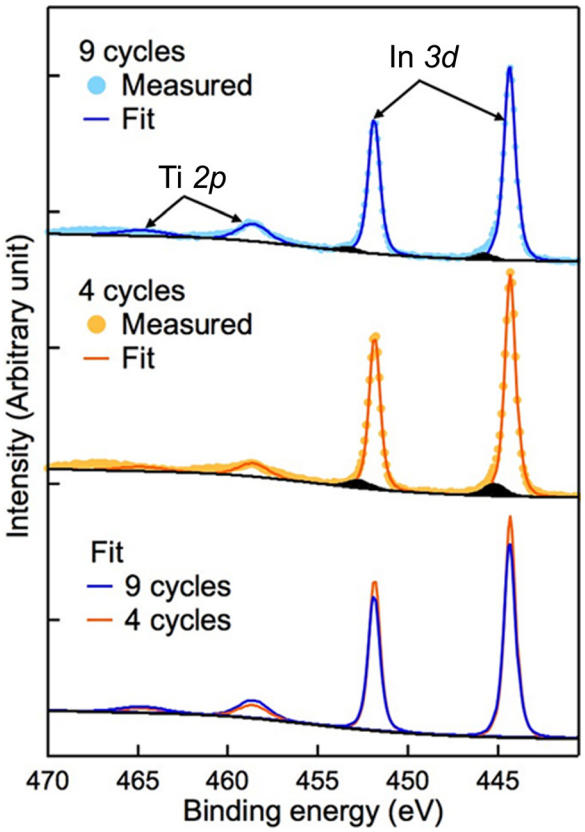

FIG. 1. Ti 2p and In 3d XPS of ~1 nm ZrO_2/$In_{0.53}Ga_{0.47}As$ samples subjected to 9 cycles and 4 cycles of nitrogen plasma/TDMAT pre-treatment. Both samples were annealed in forming gas anneal at 400 °C after ZrO_2 deposition. The black shaded areas indicate peaks associated with In_2O_3. The lines are fits to the experimental data.

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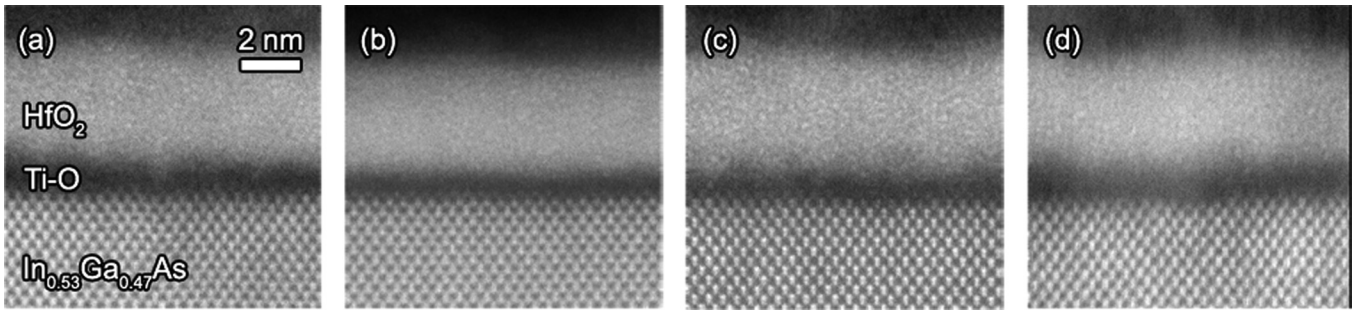

FIG. 2. HAADF/STEM cross-section images of $HfO_2/In_{0.53}Ga_{0.47}As$ interfaces, subjected to (a) 9 cycles; (b) 6 cycles; (c) 4 cycles; and (d) 2 cycles of the nitrogen plasma/TDMAT pre-deposition treatment. All samples were annealed in forming gas at 400 °C after HfO_2 deposition. The TEM foil in (b) is thicker, so the contrast was adjusted for better comparison with the thinner foils.

Quantification from the survey scans (not shown) and the high-resolution peaks suggest that the amount of In_2O_3 is approximately 0.3–0.4 at. % of the overall interface region. Considering only the In peak, about 5% of it appeared oxidized, which is likely sufficient to account for an oxidized surface layer (a more accurate estimate is difficult because the XPS signal decreases exponentially as a function of depth, and the oxidized In is closest to the top surface, and therefore disproportionately strong compared to the rest of the In signal). No signatures associated with Ga-oxide, As-oxide, As suboxide, or As-As bonding could be detected. We conclude that the interface layer is mostly TiO_2 with a small amount of In_2O_3 and possibly some nitrogen,[6] and we will refer to it as Ti-O layer in the following.

Figure 2 shows STEM images taken in HAADF mode of four samples with ~4-nm HfO_2 dielectrics, subjected to the postdeposition anneal at 400 °C. The samples were exposed to different number of cycles (9, 6, 4, and 2, respectively) of nitrogen plasma/TDMAT. A low-atomic-number amorphous layer that is ~1 nm thick is visible at the interface between HfO_2 and $In_{0.53}Ga_{0.47}As$, and thus likely corresponds to the Ti-O layer detected in XPS (Ti has a lower atomic number than Hf, causing the Ti-O layer to appear dark in HAADF imaging mode). While the HfO_2 contains small crystallites as a result of the anneal (visible as wormlike contrast in these images), the interface layer remains amorphous, mostly likely due to its small thickness, which affects the crystallization kinetics.[29] The thickness of the amorphous Ti-O layer appears to be relatively independent of the number of pre-deposition cycles. This indicates that its thickness is self-limiting. One explanation is that the first few cycles of the water in the ALD process are the likely to be the source of oxidation. The increase of the interfacial layer thickness is terminated after the high-k layer completely covers the surface. If the thickness of the interfacial layer is approximately constant across the series, one would expect that the capacitance density of the stack increases with increasing number of cycles due to the increase in Ti content detected in XPS (or, alternatively, a reduction in the amount of lower permittivity In-O), which is indeed observed, as described next.

Figure 3 shows frequency-dependent CV characteristics of MOSCAPs from the four different samples for which the STEM images were shown in Fig. 2. The capacitance density in accumulation (large positive gate bias) systematically increases with the number of pre-deposition cycles, and reaches about 4.5 $\mu F/cm^2$ at 1 MHz for the sample exposed to 9 cycles of nitrogen plasma/TDMAT (Fig. 3(a)). Even higher capacitance densities can be achieved by optimizing the high-k stack. For example, HfO_2/ZrO_2 bilayers give excellent results. Figure 4(a) shows the CV characteristics of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ~1 nm HfO_2/~3 nm ZrO_2 subjected to 6 cycles of the nitrogen plasma/TDMAT pre-treatment. The accumulation capacitance density is 5.3 $\mu F/cm^2$ at 1 MHz and 2 V, almost twice that of other gate stacks reported in the literature, which are less than 3 $\mu F/cm^2$ at 1 MHz.[5–7,14] This sample had an interface layer that was only about 0.5 nm thick (see STEM image in Fig. 4(b)), which is 50% thinner than that of the samples shown in Fig. 3, and contributes to the higher capacitance density. In general, for n-type $In_{0.53}Ga_{0.47}As$, the oxide capacitance density (C_{OX}) should be higher than the accumulation capacitance density (C_{acc}), due to the low conduction band density of

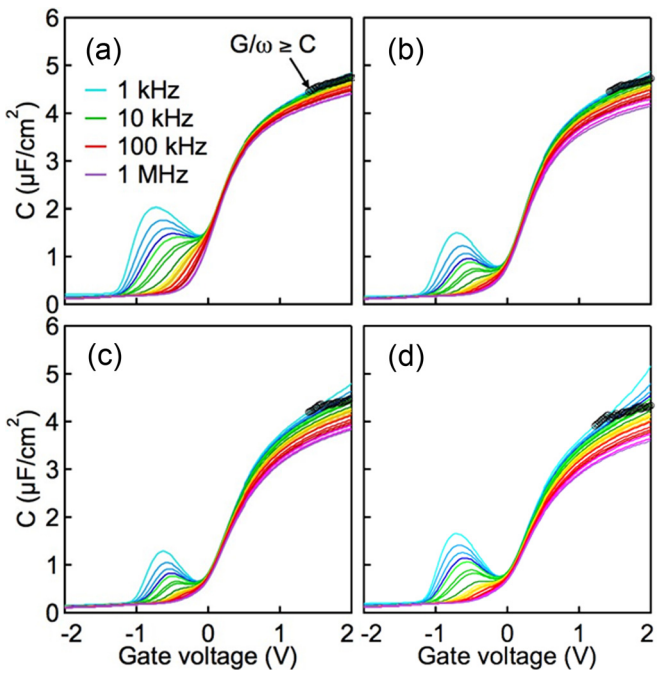

FIG. 3. CV characteristics of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ~4 nm HfO_2 subjected to (a) 9 cycles; (b) 6 cycles; (c) 4 cycles; and (d) 2 cycles of nitrogen plasma/TDMAT pre-treatment. The black markers indicate where $G/\omega \geq C$.

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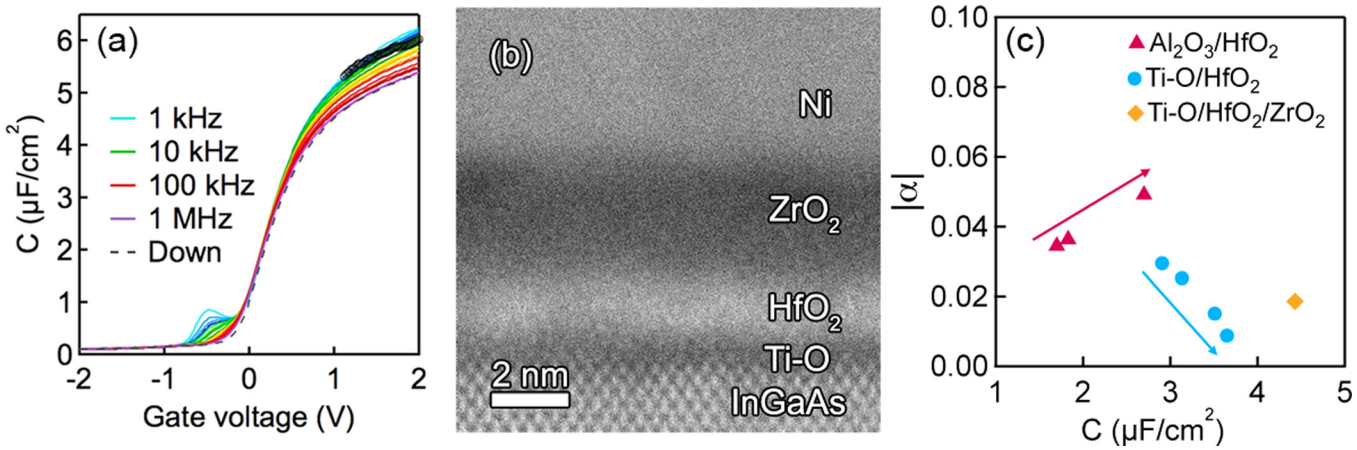

FIG. 4. (a) CV characteristics as a function of frequency and (b) HAADF/STEM cross-section image of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ~3 nm ZrO_2/~1 nm HfO_2 subjected to 6 cycles of nitrogen plasma/TDMAT pre-treatment. The dashed line in (a) shows downward (positive to negative voltage) sweep at 1 MHz. The black markers indicate where $G/\omega \geq C$. (c) Power law coefficient α of a power law fit of the frequency dispersion ($C_{acc} = Af^{\alpha}$) at +1 V from flatband for $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with nitrogen plasma/TMA pre-treatment, and $HfO_2/In_{0.53}Ga_{0.47}As$ and $ZrO_2/HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs with nitrogen plasma/TDMAT pre-treatment as a function of the 1 MHz accumulation capacitance density at +1 V from flatband.

states, which adds a semiconductor capacitance in series with the oxide capacitance. The dielectric constant for amorphous TiO_2 can be as high as 40 (Ref. 30), while the dielectric constants for HfO_2 and ZrO_2 depend on their crystalline phase. The dielectric constant of tetragonal ZrO_2, which is kinetically stabilized in thin dielectrics,[31] can be as high as 35–50 (Ref. 32). HfO_2 is typically monoclinic, with a low dielectric constant of about 18. If these three dielectrics are in series, C_{OX} of this MOSCAP could approach values of 6 μF/cm^2, which is higher than the measured C_{acc}. While the contribution of the semiconductor capacitance to the accumulation capacitance can, in principle, be calculated,[33] accurate modeling of C_{acc} is currently not possible, as discussed below. At low frequencies, the measured accumulation capacitance may also suffer from artifacts from leakage. The black markers in the CV data in Figs. 3 and 4(a) indicate where $C \geq G/\omega$, where G is the measured conductance and ω is the frequency. Values above this line are not a measure of the true capacitance density.

The CV characteristics indicate very high quality interfaces. For example, the ideal depletion capacitance value of 0.119 μF/cm^2 is reached, before entering deep depletion, as can be seen from the finite slope at negative gate biases. Deep depletion is one of the best indicators that the Fermi level is unpinned and moves into the lower half of the band gap.[34,35] The CV hysteresis is very small. The dashed line in Fig. 4(a) indicates a hysteresis of ~0.06 V around flatband at 1 MHz. By sweeping to a smaller bias range, the hysteresis is reduced. This indicates that charge trapping in the oxide is small. The hysteresis may also have other origins such as generation of minority carriers in the semiconductor, if the CV is swept to high voltages. All CV show a steep slope in the transition to the accumulation. Furthermore, the frequency dispersion at negative biases (hump), which is now well established as being due to midgap D_{it} response,[34,36] is small. It increases with increasing number of pre-treatment cycles. Midgap D_{it} is typically due to damage (defects) of the semiconductor.[14,37] The results indicate that too many plasma cycles cause damage to the III-V surface.

In addition to the high capacitance density, the samples show remarkably low frequency dispersion in accumulation. All high-k/$In_{0.53}Ga_{0.47}As$ MOSCAPs, with the exception of those that employ a Si interfacial layer,[5] show such frequency dispersion, and its origins are currently debated in the literature.[25,38,39] The frequency dispersion is fairly modest for thick Al_2O_3 dielectrics, but increases significantly as the capacitance density is scaled.[40] Figure 4(c) shows a measure of the frequency dispersion in accumulation, expressed in terms of the coefficient α of a power law fit of the frequency dispersion ($C_{acc} = Af^{\alpha}$, where C_{acc} is the accumulation capacitance density at +1 V from flatband, A is a constant, and f is the frequency). Figure 4(c) compares α for HfO_2 dielectrics and the bilayer MOSCAP, with Al_2O_3 and Ti-O interface layers, respectively, as a function of the maximum capacitance density at 1 MHz. For the Al_2O_3 interface layers, α increases with decreasing HfO_2 thickness and increasing C_{OX}. In contrast, for the Ti-O interface layers, increasing the number of nitrogen plasma/TDMAT cycles (from 2 to 9), results in an increased capacitance density and Ti-content of the interface layer, but decreases the frequency dispersion in accumulation, as can also be seen from Fig. 3. Note that the ZrO_2/HfO_2 bilayer stack, which has the highest capacitance density, was exposed to 6 cycles nitrogen plasma/TDMAT, and has a similar α as the 6 cycle HfO_2 MOSCAP with nitrogen plasma/TDMAT. We discuss the mechanisms below.

A complete theoretical description of the CV of high-k/III-V interfaces is still lacking. In particular, at least for n-type channels, the contribution of D_{it} to the capacitance in accumulation appears to be non-negligible,[41] even at 1 MHz, due to the fast response of traps near or in the conduction band, as described by

$$\frac{1}{C_{acc}} = \frac{1}{C_{OX}} + \frac{1}{C_{Dit} + C_S}, \quad (1)$$

where C_S and C_{Dit} are the semiconductor and interface state capacitances, respectively. It is believed that the D_{it} in the conduction band can be high.[42] This precludes determination

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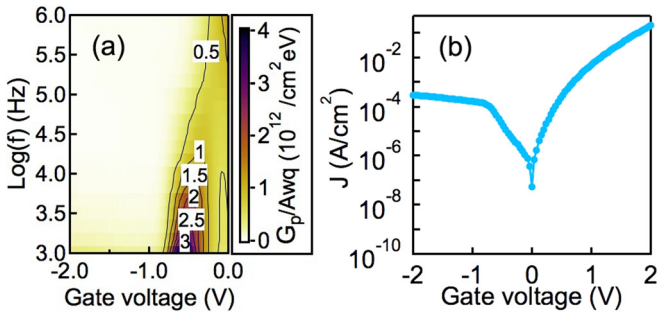

FIG. 5. Conductance map and leakage of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ~1 nm HfO_2/~3 nm ZrO_2 subjected to 6 cycles of nitrogen plasma/TDMAT pre-treatment. (a) Normalized parallel conductance maps, showing $(G_p/A\omega q)_{max}$ as a function of gate voltage and frequency. (b) Current-voltage characteristics between −2 V and 2 V. All measurements are at room temperature.

of the D_{it} from CV-based methods, which assume that the only contribution of D_{it} to the high-frequency CV is a stretch-out. Reliable values for the D_{it} near midgap can be obtained from the conductance method,[34,41] as described next.

To provide a quantitative measure of D_{it}, Figure 5(a) shows the normalized parallel conductance peak values, $(G_p/A\omega q)_{max}$, where G_p is the parallel conductance, A the capacitor area, ω the frequency, and q the elemental charge, as a function of voltage and ω, for the sample for which the CV was shown in Fig. 4(a). The D_{it} can be estimated by multiplying $(G_p/A\omega q)_{max}$ with a factor of ~2.5.[43] Near midgap, the D_{it} values are in the $10^{12}\,cm^{-2}eV^{-1}$ range, very similar to what is obtained for the best interfaces with Al-O interlayers.[11] Conductance maps also provide a measure of the efficiency of the Fermi level movement in the band gap.[44,45] The $(G_p/A\omega q)_{max}$ peak shifts more than two orders of magnitude in frequency as the gate bias is changed between −0.25 and −0.75 V, which indicates a large band bending in response to a change in gate bias.

Figure 5(b) shows the leakage current of the same MOSCAP as a function of gate voltage. The leakage current density is 5 mA/cm^2 at 1 V gate bias, which is below the limit specified by the international technology roadmap for semiconductors. Figure 6(a) shows that the leakage current density barely differs from that of HfO_2 MOSCAPs with Al_2O_3 interface layers and is lower than that of ZrO_2 MOSCAPs with Al_2O_3 interface layers. The leakage is at least an order of magnitude lower than that of other scaled III-V MOSCAPs.[5] As shown in Fig. 6(b), the leakage data are well described by direct tunneling:[46,47]

$$J = \frac{q^3}{16\pi^2\hbar\phi_{OX,eff}}E^2 \times \exp\left(-\frac{4\sqrt{2m^*}\phi_{OX,eff}^{3/2}}{3\hbar q}E\left(1-\left(1-\frac{V}{\phi_{OX,eff}}\right)^{3/2}\right)\right), \quad (2)$$

where q, $\hbar$, and E are the elementary charge, the reduced Planck's constant, and the electric field, respectively. The fit parameters were the effective barrier height $\phi_{OX,eff}$ and the effective mass m^*. The image-force-induced barrier lowering was included according to

$$\Delta\phi = \sqrt{\frac{Eq^3}{4\pi\varepsilon_0\varepsilon_{OX}}}, \quad (3)$$

where the effective dielectric permittivity, ε_{OX}, was estimated to be ~40 for amorphous Ti-O and the fitting range was between 0 and +0.7 V. As shown in Fig. 6(b) for the sample with 4 nm HfO_2 and 9 cycles of pre-treatment, the direct tunneling model describes the leakage data well. Shown in Fig. 6(c) are extracted parameters $\phi_{OX,eff}$ and m^* for the HfO_2 dielectrics with different number of nitrogen plasma/TDMAT cycles. As the number of cycles increases, $\phi_{OX,eff}$ decreases from 2.06 to 1.93 and m^* increases from 0.17 to 0.2. Since the effects of barrier lowering and the increasing mass offset each other, the leakage current density remains fairly constant. Furthermore, the changes in both parameters are small, and the leakage current density barely differs from that of MOSCAPs with Al_2O_3 interface layers (Fig. 6(a)). This is a surprising result, because the conductance band offset between crystalline TiO_2 and $In_{0.53}Ga_{0.47}As$ is much smaller than between Al_2O_3 and $In_{0.53}Ga_{0.47}As$ and a much large leakage current density would have been expected. The leakage data suggest that the effective barrier height is close to 2 eV, whereas the conduction band offset between TiO_2 and $In_{0.53}Ga_{0.47}As$ is, at most, 0.6 eV.[17,24]

IV. DISCUSSION

In addition to demonstrating a route to high-*k*/III-V interfaces with unprecedented high capacitance densities, low leakage, and low D_{it}, the results shown here are also relevant for several aspects of high-*k*/III-V interfaces that have been discussed extensively in the literature. The first relates to the origin of the large frequency dispersion that is seen in accumulation, which has been attributed to border traps,[25] near interface traps in the semiconductor,[39,40] and leakage.[38] The precise origins of this frequency dispersion are important because they may negatively affect transistor parameters such as channel mobility or reliability. In general, the frequency dispersion in accumulation increases with the capacitance density, which can be understood from the simple lumped circuit model of the MOSCAP, expressed in Eq. (1): as C_{OX} increases, the frequency dispersion caused by C_{Dit} increases. Although Eq. (1) refers to the effect of the interface state capacitance, C_{Dit}, the lumped circuit models for border traps are basically similar, with the border trap capacitance replacing C_{Dit}. It is therefore very important that gate stacks of the same C_{OX} are compared when comparing the amount of frequency dispersion.

The results here are contrary to the trend expected from Eq. (1), namely, increasing C_{OX} by adding Ti to the interface layer *decreases* the dispersion. In particular, given the high C_{OX}, the low frequency dispersion is remarkable. The results show that modifying the chemistry of the interface, in particular replacing the ubiquitously employed Al-O, can lower the frequency dispersion. The results furthermore show that a region very near the interface, confined to no more than the

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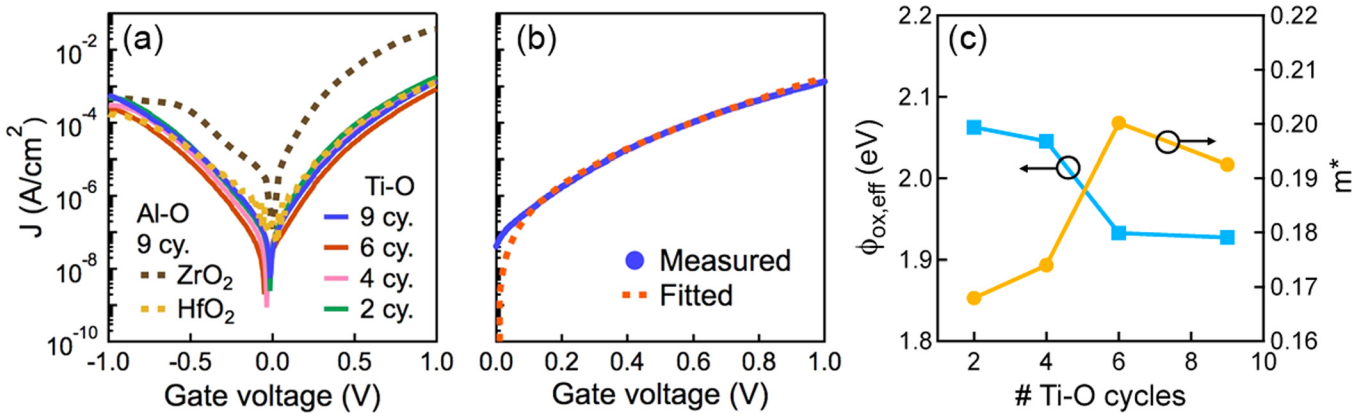

FIG. 6. (a) Current-voltage characteristics of $In_{0.53}Ga_{0.47}As$ MOSCAPs with either ~4 nm HfO_2 or ~4 nm ZrO_2 dielectrics subjected to 9 cycles of nitrogen plasma/TMA pre-treatment and ~4 nm HfO_2 samples subjected to 9, 6, 4, and 2 cycles of nitrogen plasma/TDMAT pre-treatment. (b) Comparison of measured (solid) and fitted (dashed) current-voltage characteristics between 0 V and 1 V of $In_{0.53}Ga_{0.47}As$ MOSCAPs with ~4 nm HfO_2 sample subjected to 9 cycles nitrogen plasma/TDMAT pre-treatment. (c) Effective barrier height ϕ_{OX} and the effective mass m^* as a function of the number of nitrogen plasma/TDMAT pre-treatment cycles.

thickness of the interfacial layer itself, is key to the microscopic origin of the frequency dispersion. The high-*k* dielectrics and ALD process are the same in all samples and they should thus contain the same density of defects. This is in keeping with results from modeling of the frequency dispersion.[39] It is interesting to note that the main difference in the chemistry of the interface layers in this study and previously used Al-oxide layers is that Al is replaced with Ti—the amounts of In-oxide are the same as is the lack As-oxides and As-As bonding, at least within the detection limit of XPS. Thus, the study eliminates at least these defects as the origin of large frequency dispersion in accumulation.

The second question relates to what controls the leakage current density in high-*k*/III-V MOSCAPs. In particular, here, we obtain a counterintuitive result, namely that inserting a low band gap, Ti-O layer at the interface does not change the leakage density from MOSCAPs containing a wide-band gap Al-oxide interface layer. We argue that interface dipoles may largely control the leakage properties of these interfaces. Evidence for such dipoles can be found in shifts in the flat-band voltage (V_{FB}), according to:[48]

$$\frac{V_{FB}}{q} = \phi_M - \chi_S - \phi_F - \frac{Q_f}{qC_{OX}} + \phi_D, \tag{4}$$

where ϕ_M is the effective workfunction of the metal, χ_S the affinity of the semiconductor, ϕ_D the potential drop due to a dipole layer, C_{OX} the oxide capacitance, and ϕ_F is the Fermi energy, given by

$$\phi_F = \frac{E_g}{2} - k_B T \ln\left(\frac{N_D}{n_i}\right), \tag{5}$$

where E_g the band gap, k_B is the Boltzmann constant, T the absolute temperature, and N_D and n_i the doping and intrinsic concentrations. In this system, $\phi_M = 5.15$ eV (Ref. 49), $\chi_S = 4.5$ eV, and $\phi_F = 0.06$ eV at 300 K, which gives $(\phi_M - \chi_S - \phi_F) = 0.59$ eV. The fixed charge at the interface, Q_f, can be determined from slope of a plot of V_{FB} versus thickness, t, and an estimate for ε_{OX}, as shown in Fig. 7(a). The positive fixed charge density is estimated to be 1×10^{13} cm^{-2}, which is about an order of magnitude higher than the fixed charge at the HfO_2/SiO_2 interface.[50] The linear dependence of V_{FB} on thickness indicates that the influence of oxide fixed charge is small. The intercept, which is smaller than $(\phi_M - \chi_S - \phi_F)$, indicates the presence of a large *negative* dipole (the positive end of the dipole points to the semiconductor). The extracted dipole

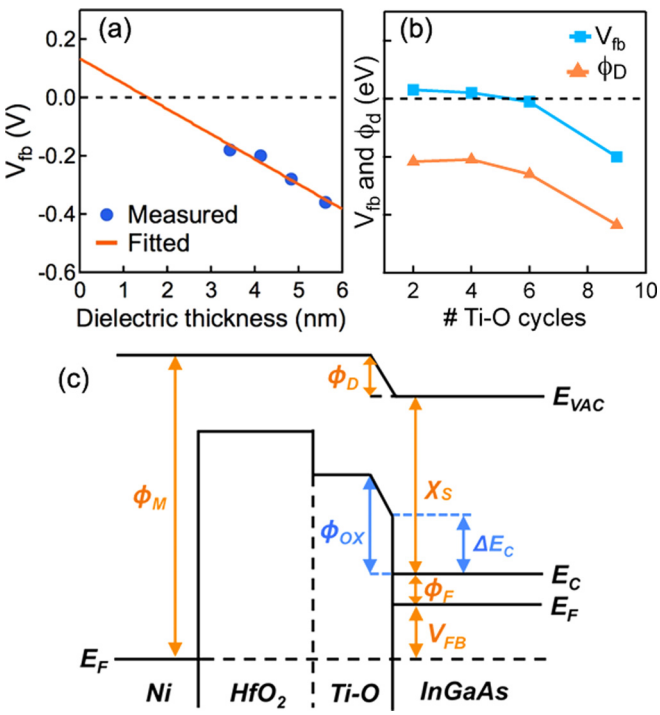

FIG. 7. (a) Flat band voltage as function of HfO_2 thickness of $In_{0.53}Ga_{0.47}As$ MOSCAPs subjected to 9 cycles of nitrogen plasma/TDMAT pre-treatment. The line represents is a linear fit to the data. (b) Flat band voltage and calculated dipole value as a function of the number of cycles of nitrogen plasma/TDMAT pre-treatment for ~4 nm $HfO_2/In_{0.53}Ga_{0.47}As$ MOSCAPs. (c) Schematic energy band diagram at flat band of MOSCAP with HfO_2/Ti-O/$In_{0.53}Ga_{0.47}As$ dielectrics showing the effect of an interface dipole on the effective barrier height. The fixed charge is not shown.

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values and the flatband voltage for the samples with 2, 4, 6, and 9 cycles of pre-treatment are shown in Fig. 7(b). V_{FB} shifts to more negative bias as the Ti content in the interface layer is increased, and ϕ_D becomes more negative. A negative dipole serves to increase the effective barrier height,[51,52] as shown in the band diagram in Fig. 7(c). This results in a lower leakage than what would be expected from the band alignments alone. The results in Fig. 6(c), a decreasing band offset by 0.13 eV with increasing Ti-content, show that increasingly negative interface dipole does not quite offset the change in band alignments.

V. CONCLUSIONS

In summary, we have shown that by exposing $In_{0.53}Ga_{0.47}As$ surfaces to a nitrogen plasma/TDMAT pre-treatment, extremely high capacitance densities can be achieved, through a combination of increasing the permittivity of the interfacial passivation layer with a highly polarizable Ti-oxide, and reducing its thickness to below what is currently possible with the commonly employed Al-oxide interface layers. The extreme increase in capacitance density was achieved without comprising the other key properties, namely D_{it} and leakage density, which are both similar to those of the best III-V MOSCAPs with Al-oxide interlayers. Similar to previously employed nitrogen plasma/TMA pre-treatments, interfaces are free of Ga-oxides, As-oxides, and As-As bonds, which can be a cause of high D_{it}.[21–23] Such dielectric stacks should enable extremely scaled III-V transistors for logic devices.

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