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An 11-bit 20MS/s Pipelined Analog-to-Digital Converter with Op Amp Sharing

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An 11-bit 20MS/s Pipelined Analog-to-Digital Converter with Op Amp Sharing

A thesis submitted in partial satisfaction

of the requirements for the degree Master of Science

in Electrical Engineering

by

Long Kong

2013

ABSTRACT OF THE THESIS

An 11-bit 20MS/s Pipelined Analog-to-Digital Converter with Op Amp Sharing

by

Long Kong

Master of Science in Electrical Engineering

University of California, Los Angeles, 2013

Professor Mau-Chung Frank Chang, Chair

In today's System-on-Chip (SoC) design, both analog and digital circuits play important role. Digital circuits are fully used to build memory and signal processing blocks. With technology scaling, speed of digital circuits has been boosted a lot in deep submicron technologies. Being the interface between real world and digital block, Analog-to-Digital Converter (ADC) is now very critical. Since high speed and high precision is required, ADC has now become a bottleneck in SoC design. Especially when integrated with digital circuits, ADC has to maintain its performance in noisy environment. Therefore, effort is deserved to develop high resolution, low power ADC designs.

In this thesis, an 11-bit Pipelined ADC with Op Amp sharing technique is presented. The post-layout simulation shows an SNDR of 59.46dB and SFDR of 69.00dB. Current consumption is around 11mA from 2.5V power supply.

The thesis of Long Kong is approved.

Kung Yao

Sudhakar Pamarti

Mau-Chung Frank Chang, Committee Chair

University of California, Los Angeles

2013

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I would like to thank my advisor, Professor Frank Chang first. He gave me the chance to do circuit design in High Speed Electronic Laboratory (HSEL) and helped me to figure out problems during the design process. I would also thank Hao Wu and Yen-Hsiang Wang, who are senior PHD students in HSEL. Hao Wu helped me a lot when I first came to this lab. He assisted me to set up the simulation environment and even taught me how to utilize different tools in the lab. Without him, I would not be able to do any circuit design. Yen-Hsiang Wang, who had several years' experience in Pipelined Analog-to-Digital Converter Design, really gave me good suggestions on my design. Meanwhile, he gave me great help on PCB design and chip testing. Furthermore, I need to thank TSMC for tape out. I started to work on this project the third quarter in UCLA. It was the perfect academic environment and friendly alumni that made me well prepared for circuit area. I think the knowledge as well as the altitude I leaned here will benefit my whole career in Electrical Engineering.

Finally, I would like to thank my family. They supported me and gave me confidence throughout my life.

CHAPTER 1

Introduction

1.1 Motivation

With the rapid growth in digital electronic technology, various digital equipment, especially computer are widely used. Computer can process digital signal and gives digital results. However, all the variables are continuous time signal when it's used in real world. These continuous analog quantities must be transferred to voltage or current quantity and then quantized to digital bit streams before processing. The process to transfer analog information into digital bits is called Analog-to-Digital Converting, and the circuit used to perform this task is called Analog-to-Digital Converter (ADC).

Till now, a variety of ADCs have been proposed which can be easily integrated with other analog or digital circuits. There're ADCs for high speed, low-resolution application. And there're also ADCs for low speed, high-resolution application. For example, good audio equipment requires around 15 bits resolution of ADC [1]. A fast growing branch in circuit area is the Radio Frequency (RF) design. In most kinds of transceivers, DAC is needed to transfer data into analog quantity in transmitter side while ADC is needed to derive digital information for baseband processing in receiver side. Nowadays, high speed ADC is used in software defined radio [2]. In some wideband communication systems, an extremely high speed ADC [3] is used in front to direct sampling the received signal. At this scenario, the linearity, resolution and speed requirement is so demanding.

In all of these applications, today's SoC design has encountered great challenge due to the process and temperature variation. Taking the wireless receiver for instance. When temperature varies, center frequency of Phase Locked Loop (PLL) will change, which impacts the radio performance. As a result, certain temperature sensors are proposed to measure the on chip temperature. Due to stability consideration, digital control bits derived from temperature sensor are desired to control the PLL. Therefore, an ADC usually follows the sensor to quantize the analog information [4]. After that, the temperature sensing result can be utilized to change bias current and operation mode in other part of circuit. For this kind of application, we need low power high resolution ADC to act as the interface. And Pipelined ADC is a good candidate as presented later in this thesis.

1.2 Organization of Thesis

In Chapter 2, performance metrics and different architectures of ADC are illustrated. Chapter 3 will highlight the proposed Pipelined architecture and its building blocks. Furthermore, the non-idealities are analyzed in detail. In Chapter 4, the main emphasize is placed on circuit design. After that, layout design is briefly presented. Finally, Chapter 5 shows simulation results under different corners and makes a conclusion.

CHAPTER 2

Fundamentals of Analog-to-Digital Converter

This chapter will introduce a list of metrics that measure the performance of Analog-to-Digital Converter. For each metric, definition will be given as well as the way to characterize it. Later, the thesis will show different kinds of ADC architectures and will give a brief idea of how specific ADC works and what are the advantages and disadvantages. This paves the path to understand why Pipelined ADC is chosen for temperature sensing application.

2.1 ADC Performance Metrics

Quantization Error: the difference between input and quantized output [5]. As shown in Figure 2.1, the quantization error always lie within $[-\frac{\Delta}{2}, +\frac{\Delta}{2}]$, where Δ denotes the value of Least Significant Bit (LSB). And it can be treated as a uniformly distributed random variable. Therefore, the quantization noise power is:

$$P_{noise} = \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q^2 \cdot \frac{1}{\Delta} dq = \frac{\Delta^2}{12}$$

Signal-to-Noise Ratio (SNR): ratio of signal power and noise power [5]. For a full-scale sinusoid input $V_{in} = V_{ref} \sin \omega t$. The signal power is $\frac{{V_{ref}}^2}{2}$. And $\Delta = \frac{2V_{ref}}{2^N}$, where N denotes the number of bits. Thus, SNR is derived:

$$SNR = \frac{P_{signal}}{P_{noise}} = 6 \cdot 4^{N-1} = 6.02N + 1.76\ dB$$

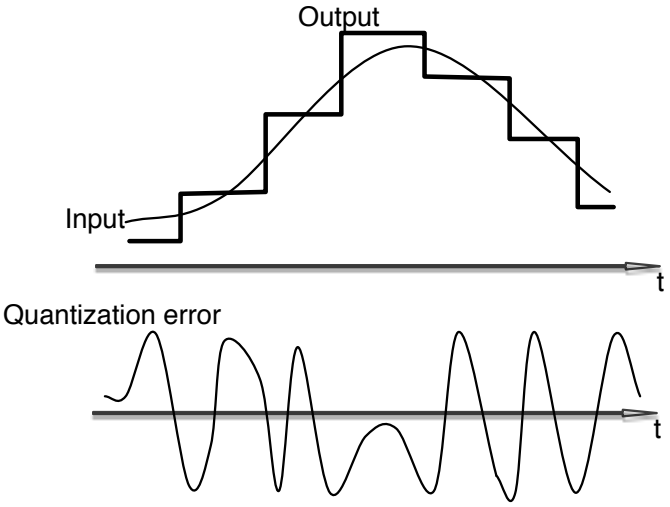

Figure 2.1 Amplitude quantization on a time domain waveform

Differential Nonlinearity (DNL): the deviation in the difference between two consecutive code transition points on the input from the ideal value of one LSB [5].

Integral Nonlinearity (INL): the deviation between input /output characteristic and the straight line connecting its start and end point. It's quite obvious that INL is the integration of DNL. Meanwhile, both INL and DNL reflect an ADC's static nonlinear behavior. In the sense of dynamic nonlinearity, INL and DNL contribute to harmonic distortion.

Spurious Free Dynamic Range (SFDR): the ratio between amplitude of fundamental and the level of largest harmonic or spur [5]. SFDR depends on the input signal level. To capture the true performance, input needs to reach full scale.

Signal-to-Noise and Distortion Ratio (SNDR): ratio between signal power and noise plus harmonic power at output [5]. Since harmonic and spur are also taken into consideration, SNDR is smaller than SNR, but it's an accurate criterion to measure ADC's performance.

Effective Number of Bits (ENOB): relates to the peak SNDR [5] by:

$$ENOB = \frac{SNDR_p - 1.76}{6.02}$$

2.2 Architectures of Analog-to Digital Converter

This section discusses different ADC architectures. In general, ADC can be calssified into two types: Nyquist ADC and Oversampling ADC. As Nyquist sampling rule requires, sampling frequency must be at least two times the bandwidth of input signal. And Nyquisst frequency is $2f_B$. Oversampling ADC works at a much higher sampling frequency than Nyquist frequency which helps to reduce the inband quantizaion noise. The most typical oversampling ADC is Sigma-Delta ADC. While on the other hand, Nyquist ADC works at a frequency comparable with Nyquist frequency. The common type is Flash ADC, Two-Step ADC, Successive Approximation ADC (SAR ADC) and Pipelined ADC. The following paragraphs discuss these ADCs repectively.

2.2.1 Sigma-Delta ADC

In Sigma-Delta ADC, the higher sampling rate means quantization noise is spread into a wider bandwidth. Therefore the total in-band noise is reduced. This is called oversampling. Next, certain feedback loop is implemented to achieve high pass effect for

noise while low pass effect for signal. This is called noise shaping. It moves in-band noise into much higher frequency band. Therefore, high SNR is achieved after filtering output signal. An important building block for Sigma-Delta ADC is integrator. Figure 2.2 shows the architecture of delaying integrator and non-delaying integrator.

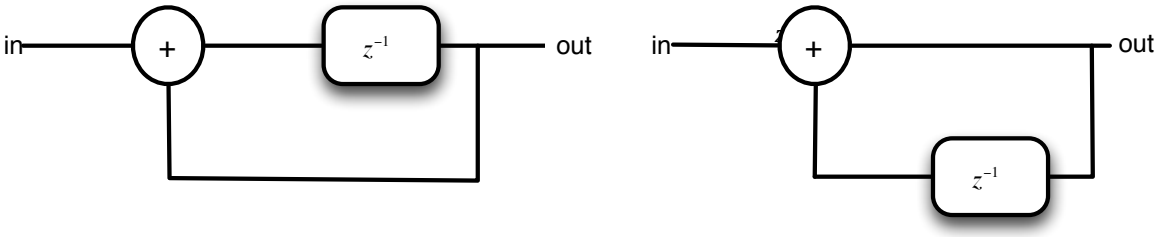

Figure 2.2 Delaying integrator (left) and non-delaying integrator (right)

With these integrators, it's easy to build Sigma-Delta modulator. Figure 2.3 shows a second order modulator, which consists of a non-delaying integrator and a delaying one. The higher the order, the better noise shaping will be. However, higher order loop suffers from stability problem.

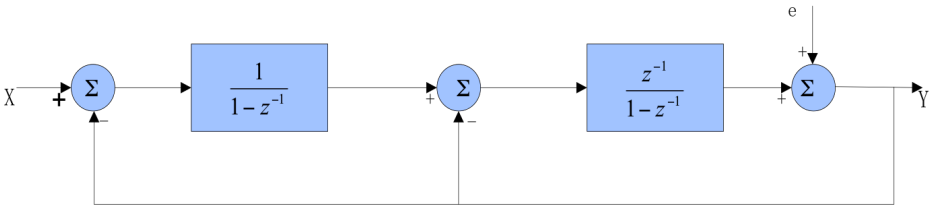

Figure 2.3 Second order Sigma-Delta modulator

Nowadays, cascading architectures are been widely used in order to maintain stability while achieving high order noise shaping at the same time.

2.2.2 Flash ADC

Flash ADC compares the input signal with different threshold level in one clock cycle. A simple architecture is shown in Figure 2.4.

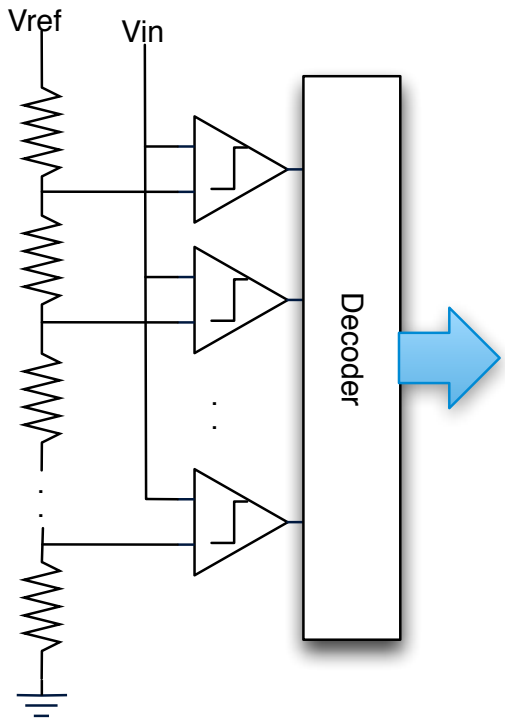

Figure 2.4 Flash ADC architecture

The main advantage of Flash ADC is fast speed because it finishes quantization in one clock cycle. But the power and area consumption increase dramatically if number of bits is large. This results from the fact that an N bits Flash ADC uses 2^N-1 comparators. Thus, Flash ADC is suitable for high speed, low-resolution application.

2.2.3 Two-Step ADC

Revealing the fact that Flash ADC is fast but cannot afford high resolution due to the exponentially dependency on number of comparators, it's better to achieve high resolution in two steps. The first step gets MSB while the second step gets LSB.

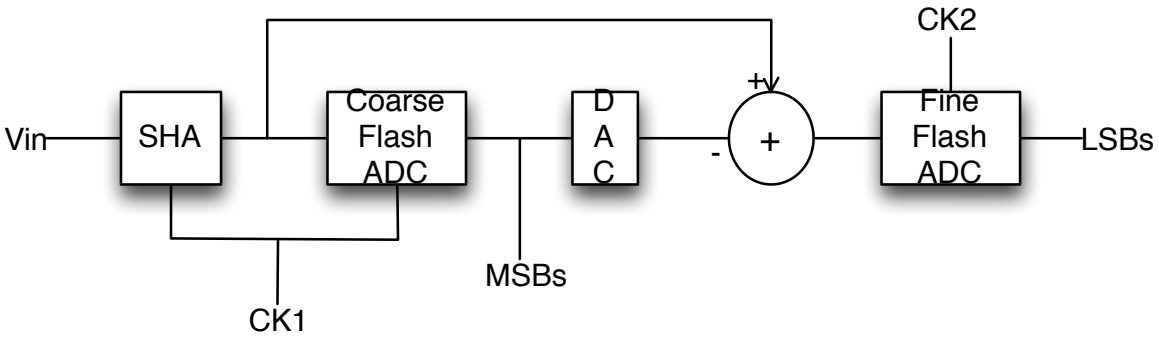

Figure 2.5 Two-Step ADC architecture

Shown in Figure 2.5, after deriving MSBs, subtracter calculates redundancy and gives result to second stage. Through this way, the power and area consumption of Flash ADC is greatly reduced.

2.2.4 SAR ADC

SAR ADC utilizes the successive approximation idea, it continuously doing logic shifting, comparison and D/A converting.

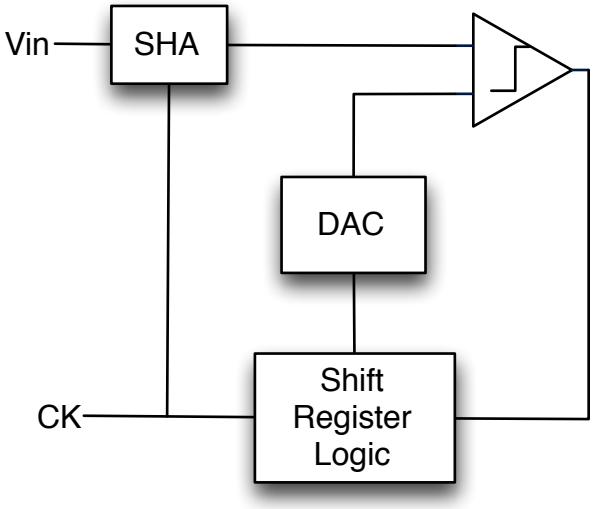

Figure 2.6 Simplified architecture of SAR ADC

Shown in Figure 2.6, the shift register logic goes from MSB to LSB. Also, the decision logic inside the shift register block tells whether each bit is 0 or 1. A very good advantage of SAR ADC is the low power consumption. Since comparator can be implemented with no static power and DAC can be implemented with switched capacitor circuit, the total power consumption is very small. Therefore, SAR ADC is suitable for low power application.

2.2.5 Pipelined ADC

The idea of pipeline comes from real life. When processing a number of toys in a factory. Different work stations charge for different parts of a toy. When first station is processing, the second station is working on the previous processed one. Through this way, every station is used fully and speed is determined by the slowest station, not the time to process a whole toy. Figure 2.7 shows the architecture of Pipelined ADC.

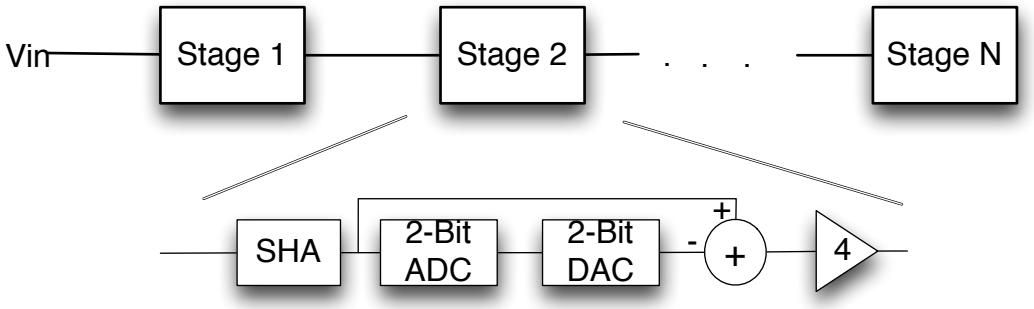

Figure 2.7 Pipelined ADC architecture (2 bits/stage)

Each stage of Pipelined ADC is the same. And within a stage, the architecture is like Two-Step ADC. Shown in Figure 2.7 is a Pipelined ADC with 2 bits per stage. To release resolution requirement for the following stage, redundancy is amplified by a factor of

four. Therefore, the input signal range for each stage remains same. The speed of ADC is determined by a single stage. It's obvious that cascading more stages will increase resolution, however, offset and linearity requirement is so demanding at higher resolution. As a result, redundant bits are usually added to each stage. Today, Pipelined ADC is widely used in high speed, moderate resolution applications.

CHAPTER 3

Pipelined Analog-to-Digital Converter Design

3.1 Proposed Architecture for Pipelined ADC

As illustrated in Chapter 2, Pipelined ADC suits well for moderate resolution applications. Now, the proposed Pipelined ADC is designed for temperature sensing, which requires around 60dB SNDR at 20MS/s and the physical bits is 11. This section presents the proposed architecture for the Pipelined ADC.

In traditional Pipelined architecture, 1.5 bits per stage is used. This results form the loop gain consideration. Since $A_{loop} = A_{open} \cdot \beta$, where β denotes the feedback factor. If more bits pre stage is used, feedback factor will be smaller, resulting in smaller loop gain. Thus, gain error will be larger as will be discussed in later sections. Thus, 1.5 bits per stage is preferred in typical scenario. At the same time, 0.5 bit redundancy greatly reduces the design effort placed on comparator and amplifier because it makes the ADC more tolerable to offset. Shown in Figure 3.1 is the architecture for traditional 11 bits Pipelined ADC.

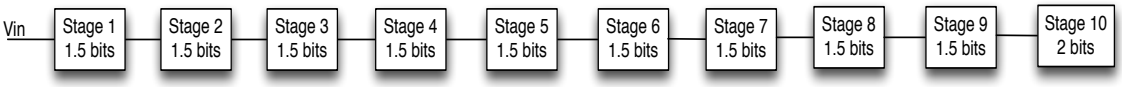

Figure 3.1 Architecture for traditional 11 bits Pipelined ADC

The first 9 stages resolve 9 bits while the last 2-bit Flash ADC gives another 2 bits. However, this architecture is not power efficient.

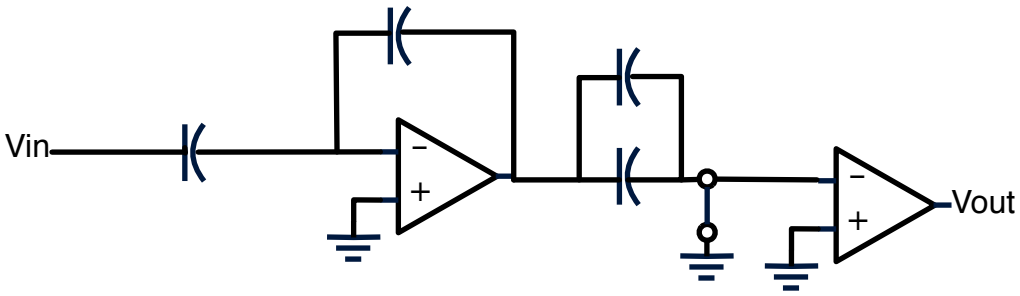

Figure 3.2 Amplification and sampling in traditional Pipelined ADC

Shown in Figure 3.2, when one stage is in amplification phase, the following stage is in sampling phase. Then the first stage goes to sampling phase while the following stage starts to amplify. It's obvious that the amplifier in each stage is used in half clock cycle. The other half cycle is actually resetting error on amplifier. The proposed idea is to do Op Amp sharing [6]. When first stage is amplifying, the second stage won't need Op Amp. When second stage is amplifying, it uses the previous amplifier because the first stage won't need it in this half cycle. Figure 3.3 illustrates this idea.

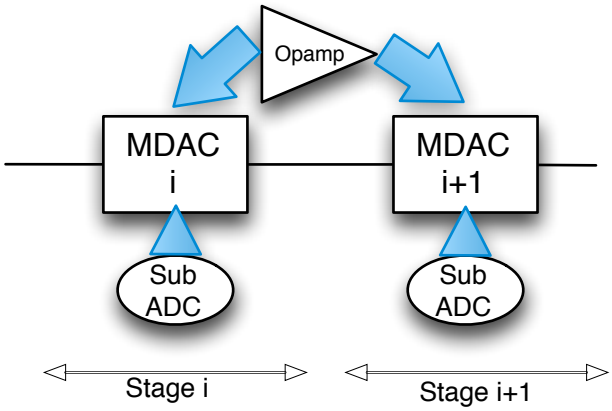

Figure 3.3 Op Amp sharing idea between pipelined stages

Due to Op Amp sharing, power consumption can be reduced by a factor of two, however, the trade off is resolution. Since there's no reset phase, error charge at input of Op Amp will directly influent the amplified redundancy. Therefore, additional technique should be adopted to solve this problem. Here's the proposed architecture.

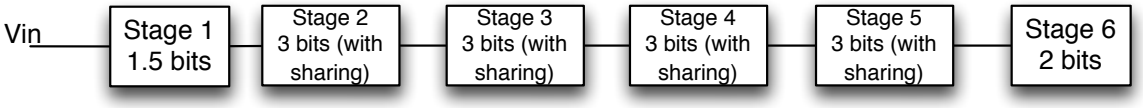

Figure 3.4 Proposed architecture for 11 bits Pipelined ADC

As shown in Figure 3.4, the first stage uses one Op Amp without sharing because resolution requirement is as high as 11 bits for the first stage. Stage 2~5 use Op Amp sharing technique. Actually each of them consists of two 1.5 bits' stages. Stage 6 is a 2 bits Flash ADC.

3.2 KT/C noise and Stage Scaling in Pipelined ADC

For high resolution ADC, the dominant noise source is usually KT/C noise. It comes form the sampling switch at front.

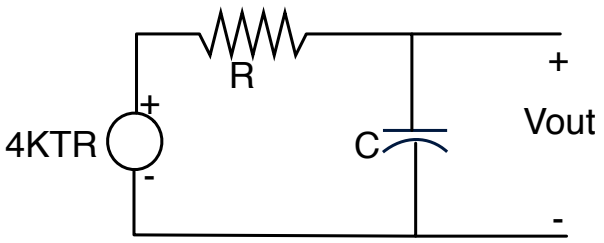

Figure 3.5 KT/C noise calculation model

As shown in Figure 3.5, sampling transistor can be approximated by a resistor, which has 4KTR (V^2/Hz) thermal noise associated with it. Since this is a linear time invariant circuit, the output mean square noise voltage can be calculated as:

$$\overline{V_{out}^2} = \int_{-\infty}^{\infty} |H(f)|^2 \cdot 4KTR \cdot df = \int_{-\infty}^{\infty} \frac{4KTR}{1 + (2\pi fRC)^2} df = \frac{KT}{C}$$

So the noise voltage at output has no relationship with the value of resistance. That's because the bandwidth decreases if power spectral density of input noise increases. Therefore, noise voltage can be reduced to a small amount only when capacitor is large enough. Since resolution requirement is the tightest at first stage, capacitor size is largest at first stage's input. For the following stage, capacitor can be sized down due to a smaller resolution requirement. With capacitor scaling, the Op Amp driving it need not maintain that large bandwidth as first stage. As a result, the whole stage scales down. This is called stage scaling. In 1.5-bits/stage architecture, scaling factor can be approximated to be 2 [7]. In order to reduce labor in designing different Op Amp for each stage, the proposed Pipelined ADC uses a scaled version for both stage 2 and 3. And a further scaled version for both stage 4 and 5 as shown in Figure 3.6.

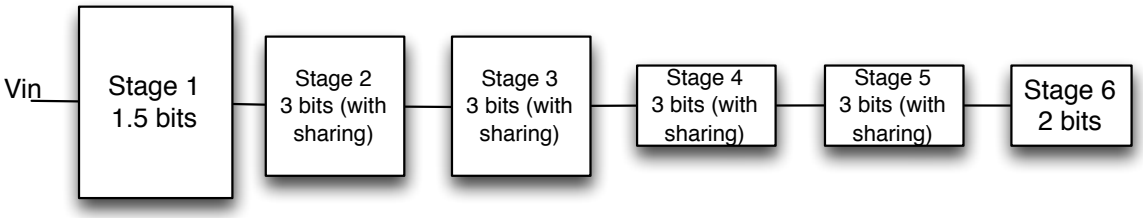

Figure 3.6 Op Amp sharing and stage scaling for 11 bits Pipelined ADC

3.3 Basic Building Blocks

3.3.1 Multiplying Digital-to-Analog Converter (MDAC)

In general, there're two kinds of MDACs: flip-over and non-flip-over. The proposed design utilizes flip-over architecture. In sampling phase, amplifier can be either input reset or unity gain feedback constructed. Since unity gain feedback limits use of telescopic amplifier, the proposed ADC adopts input resetting. Figure 3.7 shows the architecture of MDAC.

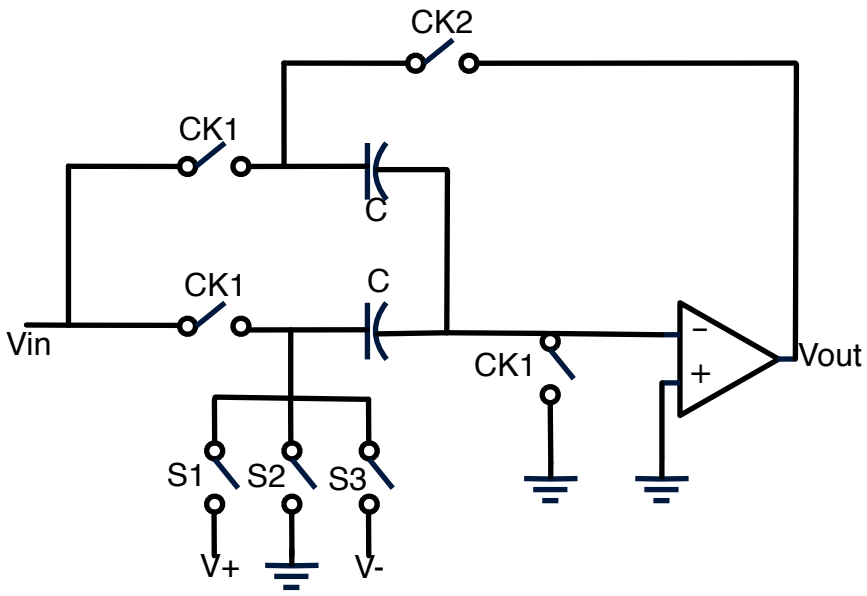

Figure 3.7 MDAC architecture in single-ended form

At CK1, two capacitors sample input signal, and Op Amp is in reset phase. At CK2, one capacitor is connected to either V+, V_{com} or V- depends on sub-ADC's output. At the same time, the other capacitor is flipped around the amplifier. In actual differential form, V+ is chosen to be V_{ref} and V- to be $-V_{ref}$. Amplified results are shown below:

$$V_{out} = \begin{cases} 2V_{in} - V_{ref}, if\ \frac{V_{ref}}{4} < V_{in} < V_{ref} \\ 2V_{in}, \quad if\ \frac{-V_{ref}}{4} < V_{in} < \frac{V_{ref}}{4} \\ 2V_{in} + V_{ref}, -V_{ref} < V_{in} < \frac{-V_{ref}}{4} \end{cases}$$

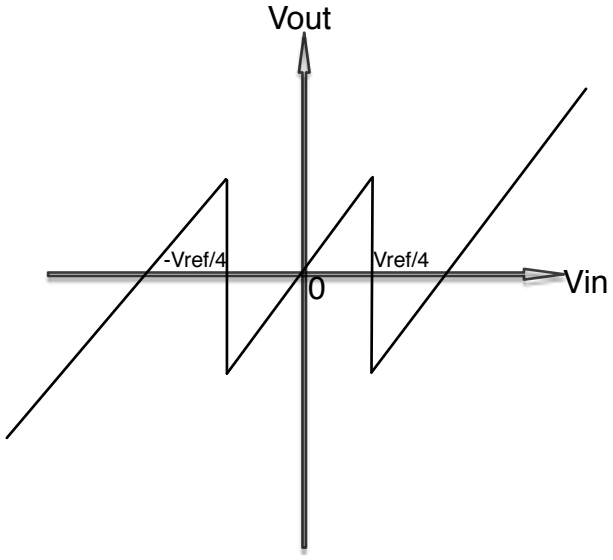

Figure 3.8 Residue plot of MDAC

Figure 3.8 shows the residue plot of MDAC. As will be discussed later, the redundancy introduced here has greatly reduced offset requirement.

3.3.2 Sub-ADC

The function of Sub-ADC is to quantize input of each stage, and produce corresponding selection bits for MDAC. Meanwhile, the digital codes of each stage come from this Sub-ADC. Shown in Figure 3.9, two comparators compare input with $\frac{-V_{ref}}{4}$ and $\frac{V_{ref}}{4}$. The two output bits will be 00, 01 or 10. Then, encoder produces selection signal

according to the rule in table 3.1. Also, S1, S2, S3 should be synchronized to CK2 to guarantee the correct operation in amplification mode.

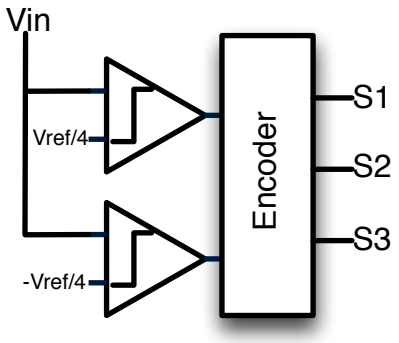

Figure 3.9 Sub-ADC architecture

2 Bits	00	01	10
S1	0	0	1
S2	0	1	0
S3	1	0	0

Table 3.1 Encoder output of Sub-ADC

3.3.3. Operational Amplifier

Shown in Figure 3.10 is a two-stage amplifier. This fully differential amplifier will need common mode feedback circuitry to stabilize the common mode level. The single ended version will be used as buffer in bias circuits. DC gain is the product of two gains.

$$A_{DC} = g_{m2}(r_{o2}//r_{o4}) \cdot g_{m8}(r_{o6}//r_{o8})$$

Since there're two dominant poles in this amplifier: one at the output of first stage and another at the output of second stage, phase margin is usually not enough to guarantee stability. Therefore, miller compensation is applied to split pole locations. Due to the increased loading at output of first stage, pole is shifted closer to origin. And the compensation capacitor also reduces the output impedance of second stage by making M8 and M9 like diode connected devices. The result is shown in Table 3.2.

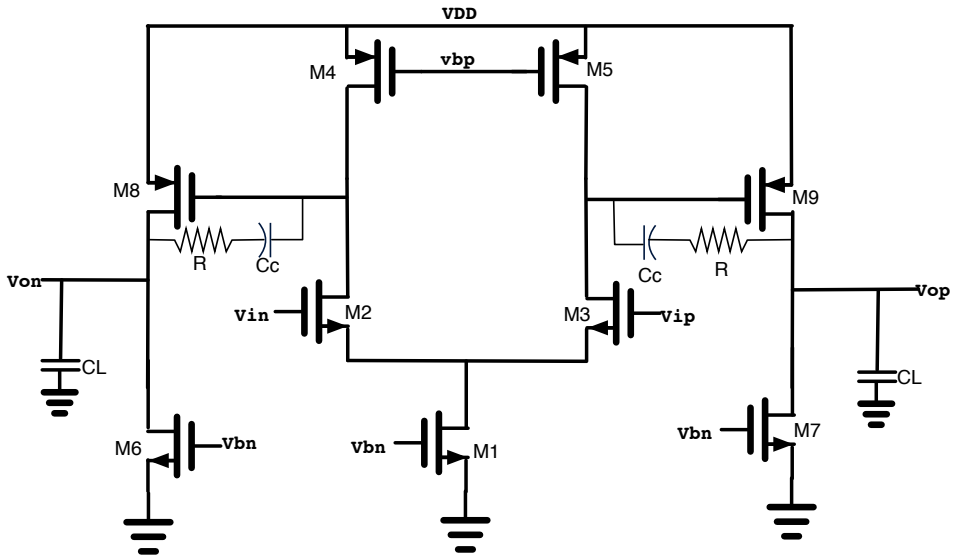

Figure 3.10 Two-stage amplifier

	Before Compensation	After Compensation
First Pole Location	$-\frac{1}{C_p(r_{o2}//r_{o4})}$	$-\frac{1}{g_{m8}(r_{o8}//r_{o6})C_c(r_{o2}//r_{o4})}$
Second Pole Location	$-\frac{1}{C_L(r_{o2}//r_{o4})}$	$-\frac{g_{m8}}{C_L+C_c}$

Table 3.2 Pole locations for two-stage Op Amp

Also, the unity gain bandwidth is approximately $\frac{g_{m2}}{C_c}$ given that unity gain frequency is much larger than first pole frequency while much smaller than the second pole frequency.

Shown in Figure 3.11 is a telescopic amplifier. The differential pair is loaded with cascade current source. Therefore, the output impedance is increased to:

$$R_{out} \backsimeq (g_{m4}r_{o4}r_{o2})//(g_{m6}r_{o6}r_{o8})$$

Since trans-conductance is still g_{m2}, DC gain can be found to be:

$$A = g_{m2}[(g_{m4}r_{o4}r_{o2})//(g_{m6}r_{o6}r_{o8})]$$

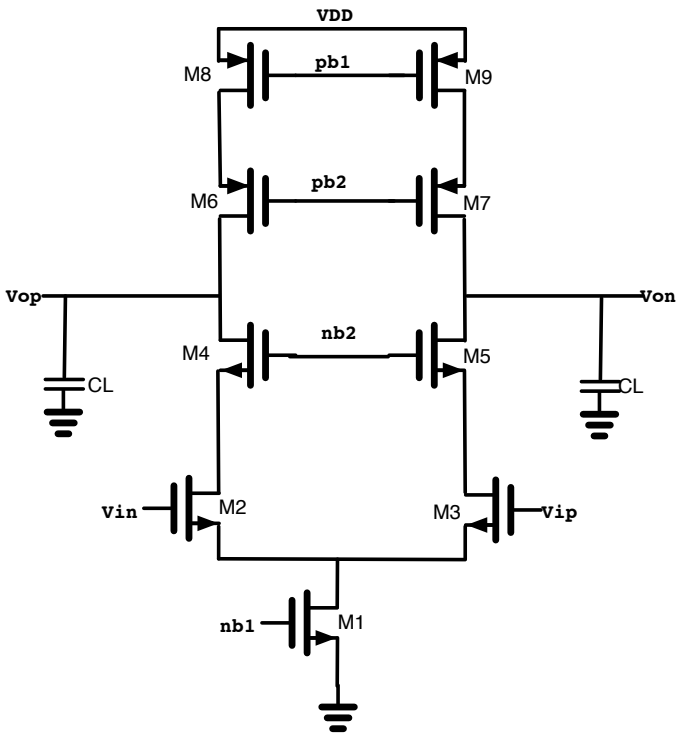

Figure 3.11 Telescopic amplifier

Since dominant pole frequency is at output, given by $\frac{1}{R_{out}C_L}$, the unity gain bandwidth is approximately $\frac{g_{m2}}{C_L}$. And slewing rate is simply $\frac{I_1}{C_L}$. This kind of amplifier will be used in MDAC, but the open loop gain is far from enough to maintain small close loop gain error. Thus, gain-boosting technique is utilized in the proposed amplifier architecture as shown in Figure 3.12.

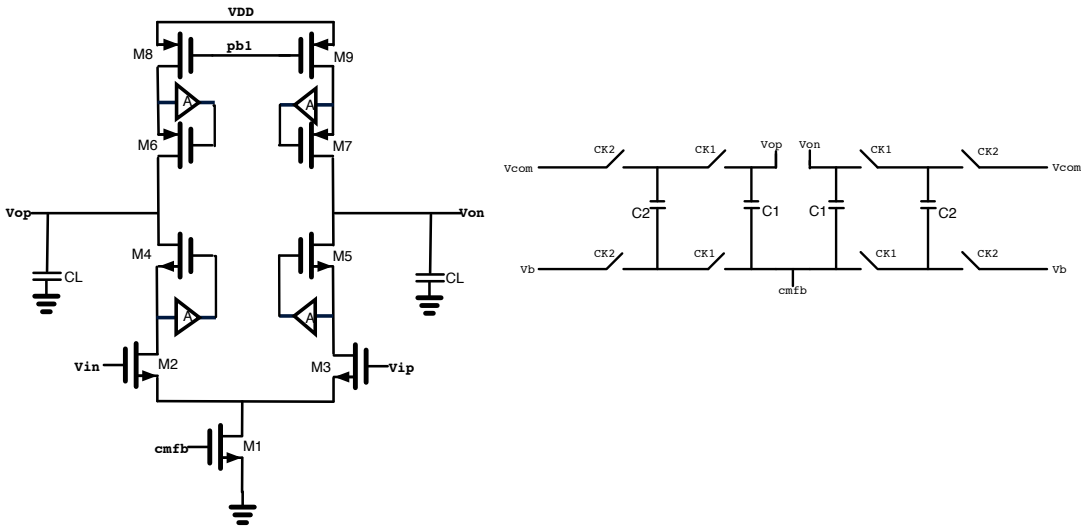

Figure 3.12 Gain-boosted telescopic amplifier with common mode feedback

Now, the open loop gain is approximately:

$$A_{open} = g_{m2}[(A \cdot g_{m4}r_{o4}r_{o2})//(A \cdot g_{m6}r_{o6}r_{o8})]$$

If the auxiliary amplifier has moderate DC gain, then telescopic amplifier will probably have enough gain. Meanwhile, stability won't be affected since gain boosting is not on main signal path. Bandwidth of auxiliary amplifier should be large enough [8] to avoid slowing down the main stage. And common mode feedback is implemented with switched capacitor circuitry [9]. The advantage is little static power consumption.

3.3.4 Comparator

Comparator is the most essential block to quantize an analog signal because it provides digital information with respect to the analog input. Comparator needs to provide high gain but the circuit doesn't have to be linear. And phase margin is not important because it doesn't use negative feedback. A simple plot is shown in Figure 3.13.

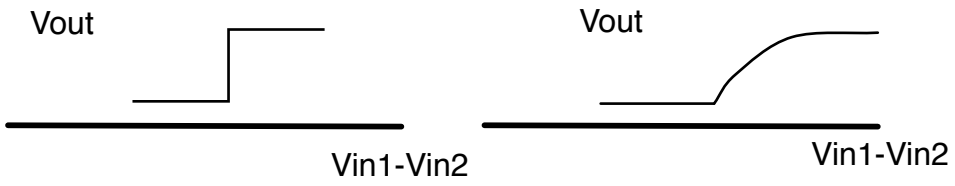

Figure 3.13 Characteristic of comparator in ideal (left) and practical (right) cases

As shown above, ideal comparator resolves the correct result even from infinitely small input difference. But in practical condition, comparator takes very long time to resolve when input difference is very small. This can be understood by the inherent time constant of a comparator. Since latch is usually a key block in comparator, it's useful to evaluate the behavior of latch. Figure 3.14 shows the model of cross-coupled inverters.

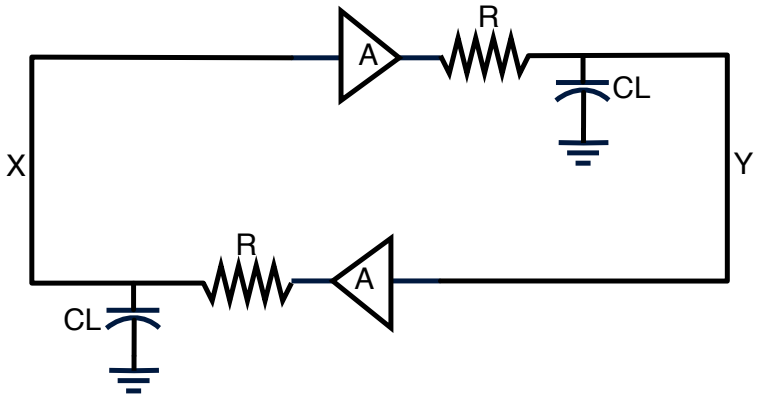

Figure 3.14 Model of cross-coupled inverters

Equations for X and Y are:

$$RC_L \frac{dV_X}{dt} + V_X = AV_Y$$

$$RC_L \frac{dV_Y}{dt} + V_Y = AV_X$$

Therefore, voltage difference between X and Y is:

$$V_{XY} = V_{XY0} e^{\frac{t}{\tau}}, where\ \tau = \frac{RC_L}{-A-1} = \frac{RC_L}{g_m R - 1}$$

If gain is larger than one, time constant is positive. Thus, exponential increase can be found in the characteristic of latch. However, for infinite small initial voltage difference, the resolving time for latch will be infinite large [16]. Since comparator is clocked in ADC scenario, the resolving time must be smaller than one clock cycle. So the input voltage resulting in very large resolving time defines meta-stability region. Below is an example of well-designed Strong-Arm comparator [10].

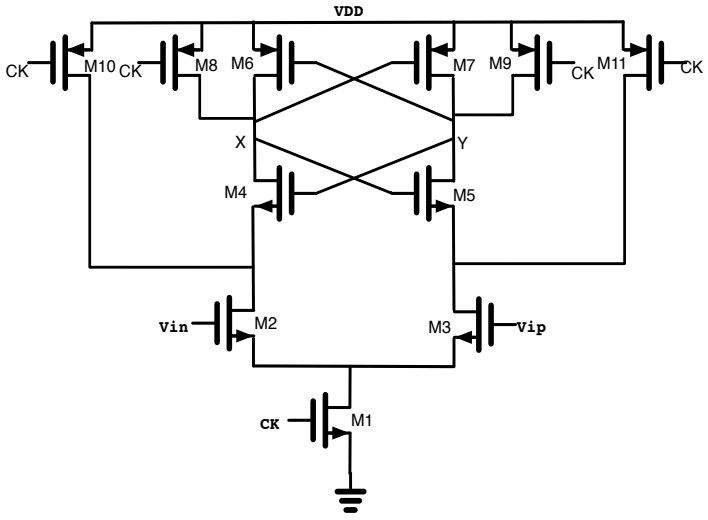

Figure 3.15 Strong-Arm comparator

When CK is low, M8~11 is on, which reset internal nodes. When CK is high, input difference will bring voltage difference in node X and Y. Finally, regeneration happens for X and Y to give effective logical level. As discussed before, meta-stability region is not desired, so high gain is necessary in comparator. The problem associated with this is the input offset. Since a small offset will be regenerated due to high gain, there comes trade off between gain and mismatch requirement. To release this effect, comparator usually consists of a pre-amplifier as shown in Figure 3.16.

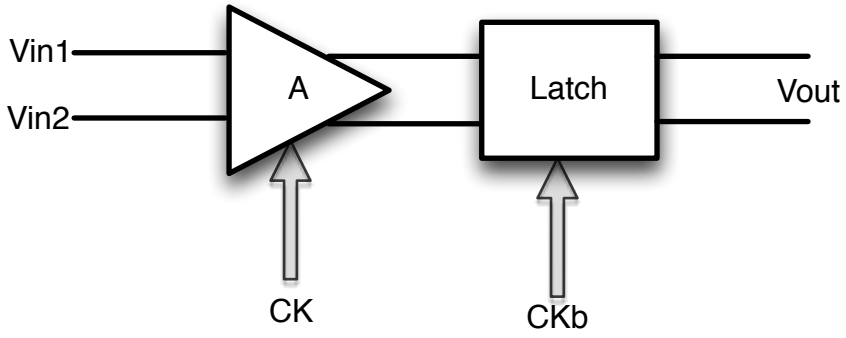

Figure 3.16 Proposed comparator architecture

When CK is high, amplifier will amplifier the input voltage difference and latch is not triggered. When CKb is high, latch will regenerate the voltage to digital level. Due to the existence of pre-amplifier, gain of latch need not be very high, thus the offset requirement is released.

3.4 Non-ideal sources in Pipelined ADC

3.4.1 Offset

Offset comes from device mismatch, temperature and process variation. It can shift the decision threshold of Sub-ADC, therefore the residue curve will shift.

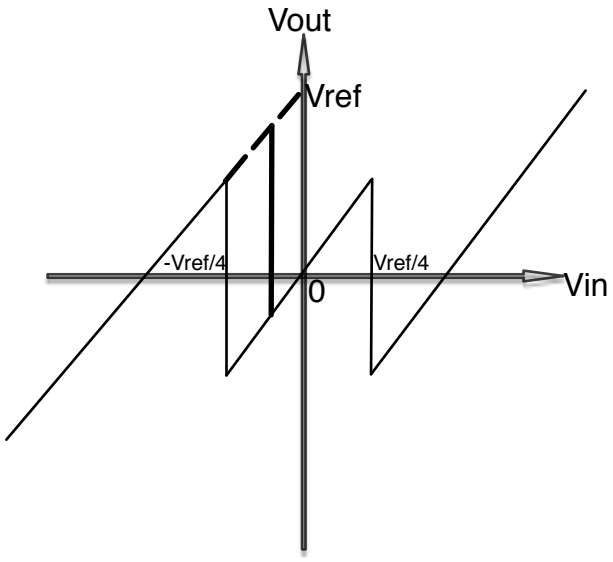

Figure 3.17 Residue plot with offset

Figure 3.17 shows the effect of offset on residue plot. If offset is smaller than $\frac{V_{ref}}{4}$, output redundancy is still within full scale, meaning that the following stage is capable to quantize and amplifier it. Once offset rises larger than $\frac{V_{ref}}{4}$, output redundancy will be greater than full scale, therefore, the following stage will saturate. In conclusion, offset requirement of Pipelined ADC is:

$$\left|V_{offset}\right| < \frac{V_{ref}}{4}$$

This includes amplifier and comparator offset, which is quite relaxed for circuit design. Here, the advantage of redundancy is very clear. If no redundancy is addressed, offset voltage must remain much smaller than 1LSB.

3.4.2 Switches

Sampling switch is usually implemented with complementary transistors as shown in Figure 3.18. But there're several issues relate to it.

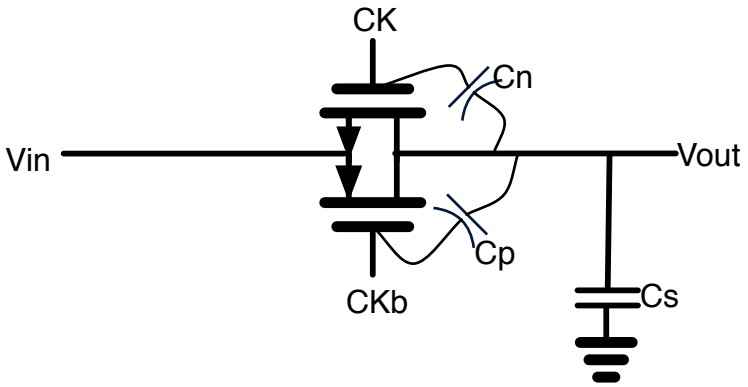

Figure 3.18 Sampling circuit

The first issue is clock feed-through. Since gate drain parasitic capacitances are different for NMOS and PMOS. The voltage variation due to capacitive coupling cannot cancel each other at output. If CK switches from V_{DD} to 0 and CKb switches from 0 to V_{DD}. The variation at V_{out} is:

$$\Delta V_{out} = \Delta V_{+} - \Delta V_{-} = \frac{C_p - C_n}{C_n + C_p + C_s} V_{DD}$$

From the calculation, it's straightforward to find that clock feed-through contributes to offset. And it can be removed by differential signaling.

The second issue is charge injection. While NMOS transistor is on, the channel charge is:

$$Q = WLC_{ox}(V_{DD} - V_{in} - V_{th})$$

$$where\ V_{th} = V_{th0} + \gamma(\sqrt{V_{SB} + 2\varphi_F} - \sqrt{2\varphi_F})$$

Suppose channel charge all injects into the sampling capacitor, V_{out} will be:

$$V_{out} = \left(1 - \frac{WLC_{ox}}{C_s}\right)V_{in} - \frac{WLC_{ox}}{C_s}\left(V_{DD} - V_{th0} + \gamma\sqrt{2\varphi_F}\right) + \frac{WLC_{ox}\gamma}{C_s}\sqrt{V_{in} + 2\varphi_F}$$

The first term denotes gain error, the second term denotes offset while the last term denotes nonlinearity. Injected holes by PMOS will reduce the voltage variation, but they cannot cancel each other. Fortunately, proper arrangement of clock sequence in MDAC will reduce the effect of this error.

The third issue is nonlinearity of on-resistance. When both NMOS and PMOS work in linear region, the on resistance can be found as follows:

$$R_{on} = \frac{1}{u_n C_{ox}\frac{W_n}{L_n}(V_{DD} - V_{in} - V_{thn})}$$

$$R_{op} = \frac{1}{u_p C_{ox}\frac{W_p}{L_p}\left(V_{in} - |V_{thp}|\right)}$$

Resistance versus input voltage is plotted in Figure 3.19.

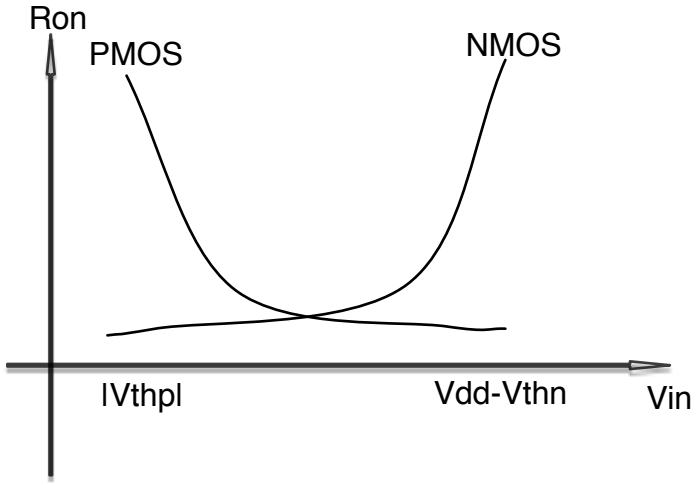

Figure 3.19 On-resistance for NMOS and PMOS switches [11]

The on-resistance for complementary switch is the parallel of these two resistances, which is shown in Figure 3.20.

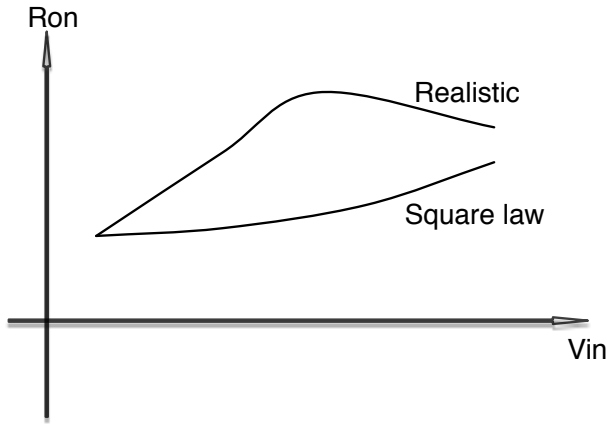

Figure 3.20 On-resistance of complementary switch

It can be found that on-resistance varies with input voltage and the relationship is not linear, which results in harmonic distortion at output. This phenomena is quite undesirable because it adds nonlinearity directly to input signal even before it's quantized. The way to address this is the bootstrap switch. The basic idea is to make gate source voltage constant.

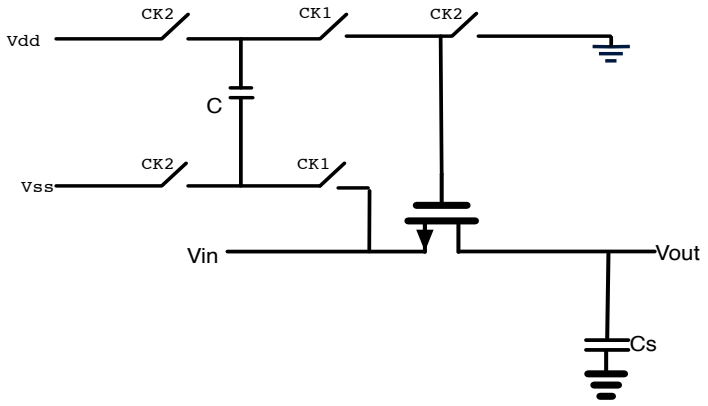

Figure 3.21 Architecture of bootstrap switch

As shown in figure 3.21, when CK2 is high, voltage between capacitor is Vdd, and sampling switch is off. When CK1 is high, bottom side of capacitor is connected to input signal, while the top is connected to gate, with a voltage Vdd+Vin, and sampling switch is on. Through this way, gate source voltage is maintained constant [17]. And it eliminates nonlinearity of on-resistance. The actual circuit implementation must take care of high voltage. Typically, cascade devices are used to protect MOSFET.

3.4.3 Gain Error

Due to finite DC gain of operational amplifier, MDAC will always have gain error. Figure 3.22 shows a single ended version for MDAC in amplification mode.

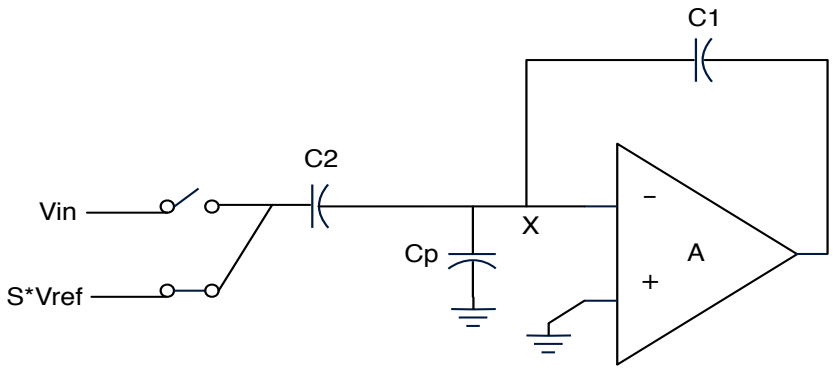

Figure 3.22 Amplification mode of MDAC

In Figure 3.22, capacitor Cp denotes the parasitic capacitance at amplifier's input. This comes from the parasitic capacitance of switches and input MOS transistors. According to charge conservation at node X,

$$V_{in}(C_1 + C_2) = (S \cdot V_{ref} - V_x)C_2 + (0 - V_x)C_p + (V_{out} - V_x)C_1$$

And gain of amplifier, $A = -V_{out}/V_x$

Combing two equations, $V_{out} = \frac{V_{in}(C_1+C_2)-S\cdot V_{ref}\cdot C_2}{\frac{C_2+C_p+C_1}{A}+C_1}$

Suppose $C_2 = (1+a)C_1$, $\beta = \frac{C_1}{C_1+C_2+C_p}$

Thus, $V_{out} = \left(1-\frac{1}{A\beta}\right)[(2+a)V_{in} - (1+a)S\cdot V_{ref}]$

Term 'a' denotes capacitor mismatch and β [12] denotes feedback factor including the effect of parasitic capacitance. From the equation, it's easy to find that larger open loop gain and smaller capacitor mismatch will reduce gain error. For DC gain, one can enlarge open loop gain of amplifier. While for capacitor mismatch, there're several ways to address it. One effective way is capacitor averaging.

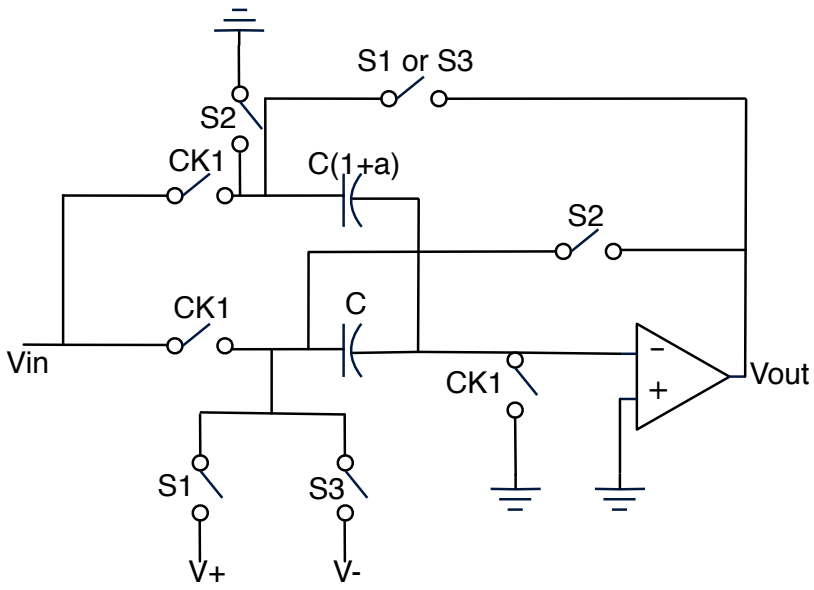

Figure 3.23 Single ended MDAC with capacitor averaging

As shown in Figure 3.23, when S1 or S3 is high, the larger capacitor is flipped around amplifier. When S2 is high, the smaller capacitor is flipped around amplifier. Suppose infinite gain of amplifier, output signal can be derived as:

$$V_{out} = \begin{cases} \frac{2+a}{1+a}V_{in} + \frac{V_{ref}}{1+a}, if\ -V_{ref} < V_{in} < \frac{-V_{ref}}{4} \\ (2+a)V_{in}, \frac{-V_{ref}}{4} < V_{in} < \frac{V_{ref}}{4} \\ \frac{2+a}{1+a}V_{in} - \frac{V_{ref}}{1+a}, if\ \frac{V_{ref}}{4} < V_{in} < V_{ref} \end{cases}$$

The first part and last part has smaller slope while the second part has larger slope as illustrated in Figure 3.24.

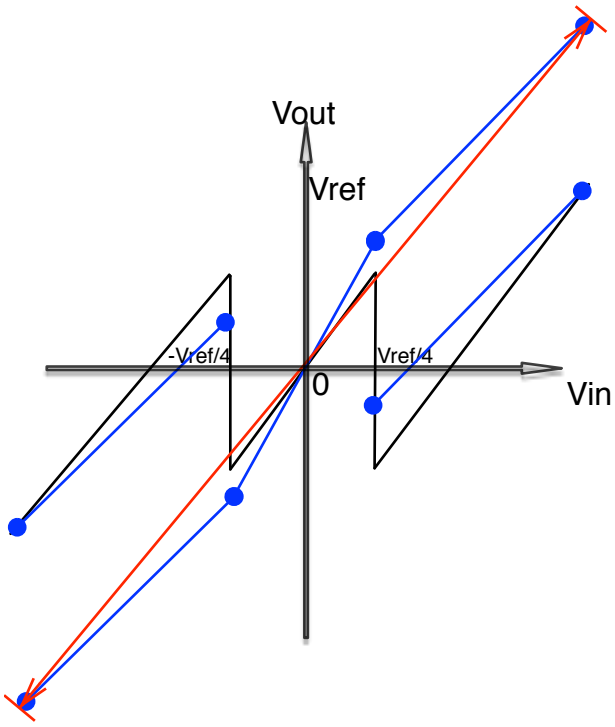

Figure 3.24 Residue plot with capacitor averaging

After averaging, the final slope is larger than the smallest slope while smaller than the largest slope as drawn in red curve. Therefore, the gain error is reduced.

3.4.4 Finite Bandwidth

In amplification mode of MDAC, time constant of Op Amp and switches will never be infinitely small. This results in the settling behavior of output residue. Using single pole approximation, the redundancy can be found as below, where ω_{3dB} is the 3dB bandwidth of amplifier:

$$V_{out} = \left(1 - \frac{1}{A\beta}\right)(1 - e^{-\omega_{3dB} \cdot t})\left[(2 + a)V_{in} - (1 + a)S \cdot V_{ref}\right]$$

And nonlinearity can be found in residue plot:

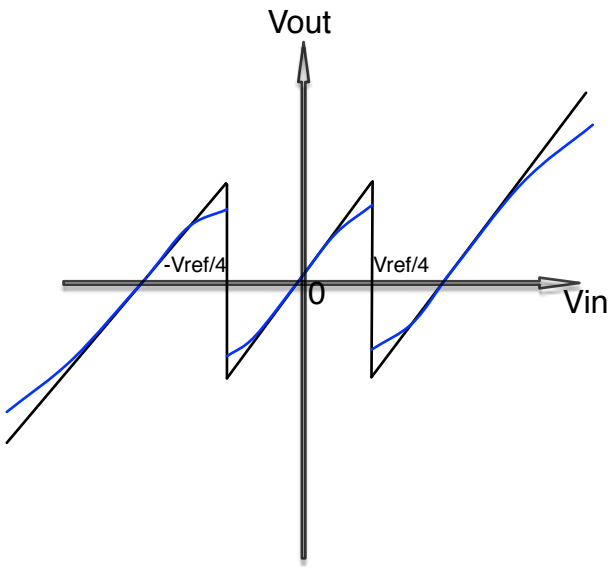

Figure 3.25 Residue plot with effect of finite bandwidth

As shown in Figure 3.25, blue curve qualitatively reflects effect of finite bandwidth. At the start and end point, settling is never complete, but the largest error must be remained below certain level.

CHAPTER 4

Design of Prototype ADC

4.1 Operational Amplifier

Operational amplifier is a critical building block for MDAC. It's gain and bandwidth must be large enough to minimize gain error and nonlinearity. First we need to calculate the capacitive loading of the first stage amplifier. Given capacitor size C at input of first stage, the second and third sharing stages employ $\frac{C}{2}$ while fourth and fifth sharing stages employ $\frac{C}{4}$. Total input referred mean square noise is:

$$\overline{V_{in}^2} = \frac{4KT}{C} + \frac{1}{4}\cdot\frac{4KT}{\frac{C}{2}} + \frac{1}{16}\cdot\frac{4KT}{\frac{C}{2}} + \frac{1}{64}\cdot\frac{4KT}{\frac{C}{2}} + \frac{1}{256}\cdot\frac{4KT}{\frac{C}{2}} + \frac{1}{1024}\cdot\frac{4KT}{\frac{C}{4}} +$$

$$\frac{1}{4096}\cdot\frac{4KT}{\frac{C}{4}} + \frac{1}{16384}\cdot\frac{4KT}{\frac{C}{4}} + \frac{1}{65536}\cdot\frac{4KT}{\frac{C}{4}} \simeq \frac{20\mathrm{KT}}{3\mathrm{C}}$$

Full scale is chosen to be 1V, therefore 1LSB is $1/2^{11}$=0.48828mV. Making input referred thermal noise voltage to be less than $\frac{1}{4}LSB$, capacitor should be larger than 1.85pF. Finally, capacitor C is chosen to be 2pF for 11 bits resolution. That's to say, the loading for first stage amplifier will be at least 3pF. From chapter 3, the residue voltage is:

$$\mathrm{V_{out}} = \left(1 - \frac{1}{\mathrm{A\beta}}\right)(1 - \mathrm{e}^{-\omega_{3\mathrm{dB}}\cdot\mathrm{t}})[(2+\mathrm{a})\mathrm{V_{in}} - (1+\mathrm{a})\mathrm{S}\cdot\mathrm{V_{ref}}]\ [13]$$

With 2pF capacitor and averaging technique, mismatch is supposed to be very small. The largest error happens when Vin=Vref, S=1:

$$V_{ref}\sqrt{(\frac{1}{A\beta})^2 + (e^{-\omega_{3dB}t})^2}$$

To make largest error smaller than $\frac{1}{4}LSB$,

$$A \geq \frac{2^{13}}{\beta}, \omega_{3dB} = \beta\omega_{UGB} \geq \frac{13\ln 2}{t_{amp}}$$

Since $\beta = 0.5$ and $t_{amp} = 22ns$ (considering non-overlap clocks),

$$A \geq 84dB, f_{UGB} \geq \frac{13\ln 2}{\beta \cdot 2\pi \cdot t_{amp}} = 130MHz$$

The above calculation roughly gives amplifier's specs. However, some second order effect and non-idealities have not been taken into account. As a result, the designed amplifier shown in Figure 4.1 needs to have a larger gain and bandwidth than the calculated value.

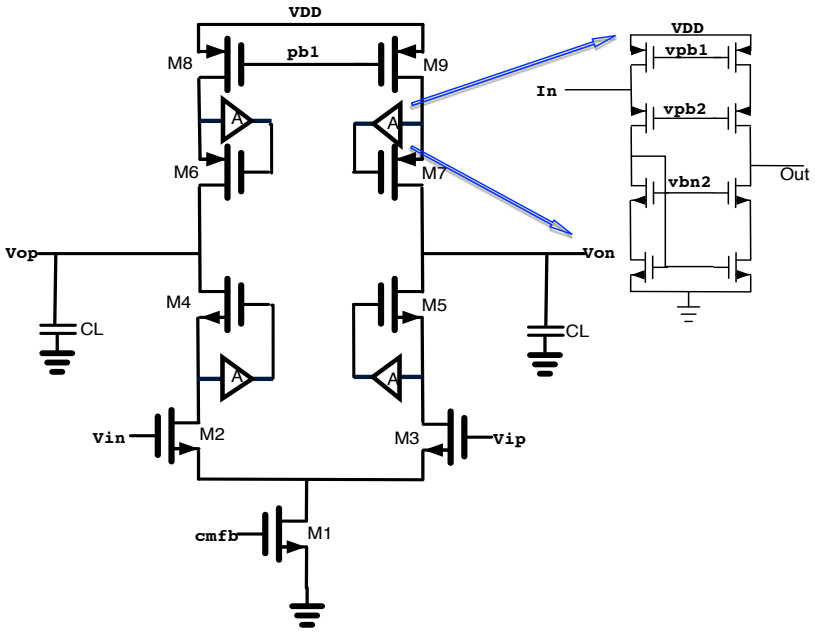

Figure 4.1 Telescopic amplifier with gain-boosting

Transistor sizing in main amplifier is shown in Table 4.1.

Transistor	M1	M2	M3	M4	M5	M6	M7	M8	M9
$\frac{W\ (um)}{L\ (um)}$	$\frac{320}{0.6}$	$\frac{160}{0.06}$	$\frac{160}{0.06}$	$\frac{240}{0.28}$	$\frac{240}{0.28}$	$\frac{240}{0.28}$	$\frac{240}{0.28}$	$\frac{240}{0.6}$	$\frac{240}{0.6}$

Table 4.1 Transistor sizing of telescopic amplifier

Since power supply is 2.5V, all transistors are thick oxide devices in TSMC 65nm technology except input pair. Since voltage across input transistors is not large, so they're typical devices in 65nm process. Therefore, the threshold voltage is smaller for input pair, which gives a larger trans-conductance. When loading with 4pF capacitor on each side, the simulated responses are:

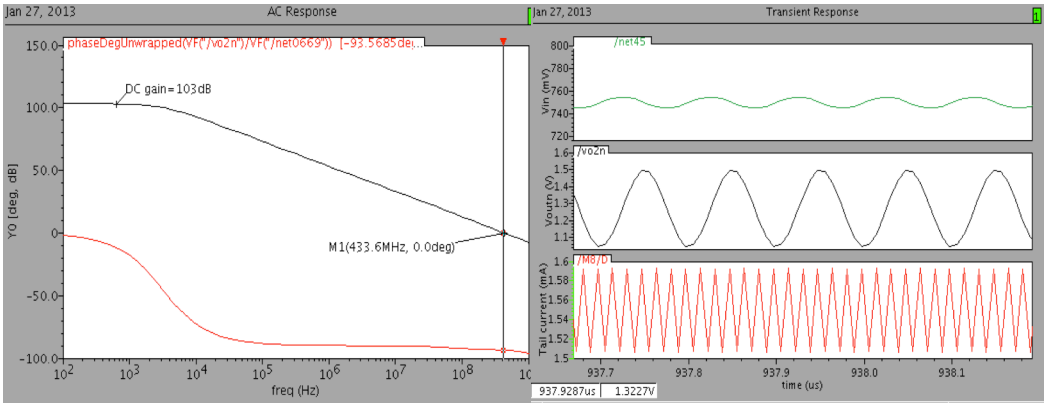

Figure 4.2 AC and Transient response of telescopic amplifier

As shown in Figure 4.2, input sinusoidal has a frequency of 10 MHz and amplitude of 10mV. Current consumption is measured at tail current source. At the same time, a little amount of current needs to be allocate to DC bias circuits.

Performance specs are concluded in Table 4.2.

Power supply	Current consumption	DC gain	Unity gain bandwidth	Phase margin	Output swing
2.5V	1.6mA	103dB	433MHz	86 degree	1.2V

Table 4.2 Amplifier specs

Amplifier used in the following stages will be scaled down. But since it's used in Op Amp sharing stages, dual input telescopic amplifier [14] is adopted to alleviate error charge issue.

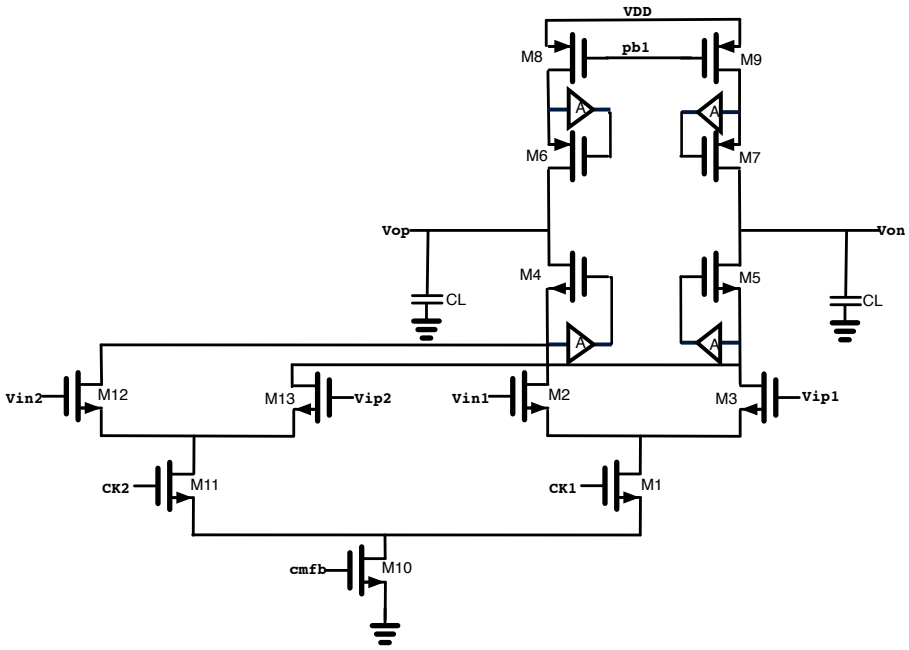

Figure 4.3 Dual input telescopic amplifier

Figure 4.3 shows the dual input amplifier. It's based on the current steering idea. And total current consumption scales with capacitor scaling to save power.

4.2 Multiplying Digital-to-Analog Converter

The function of MDAC is to do subtraction and amplification. This switched capacitor circuit also encompasses the capacitor averaging idea. MDAC for the first stage is shown in Figure 4.4.

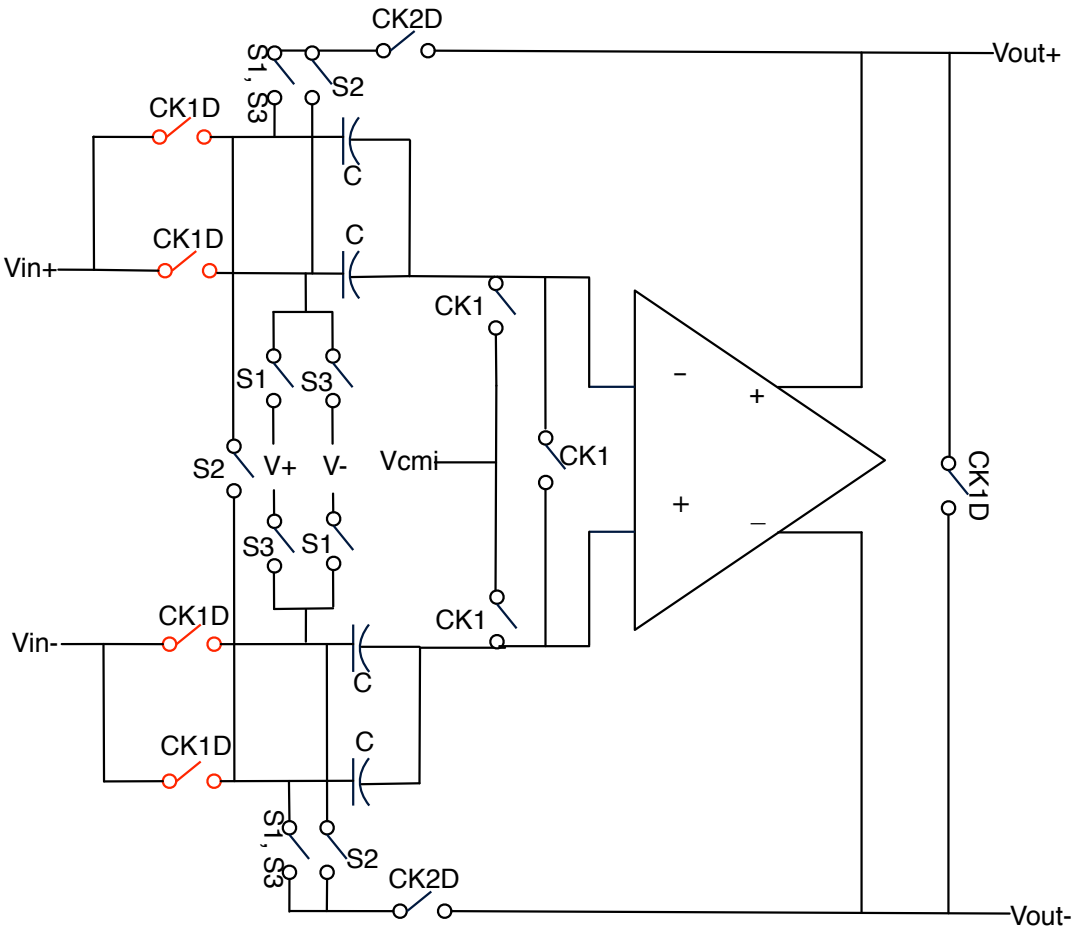

Figure 4.4 MDAC for the first stage

As shown in Figure 4.4, the implementation is in fully differential from which increases the immunity of common noise and offset. The red sampling switches are bootstrap switches to reduce nonlinearity. Other switches are all made of complementary transistors,

but the sizing is critical. And capacitor is 2pF Mimcap. In clock phase 1, sampling occurs and both input and output of Op Amp are in reset phase to make sure there's no error charge. In clock phase 2, Sub-ADC selects corresponding reference voltage and amplification occurs. Depends on selection pattern, capacitor average happens by swapping the flip over capacitor [15]. Here is the simulated result of this MDAC.

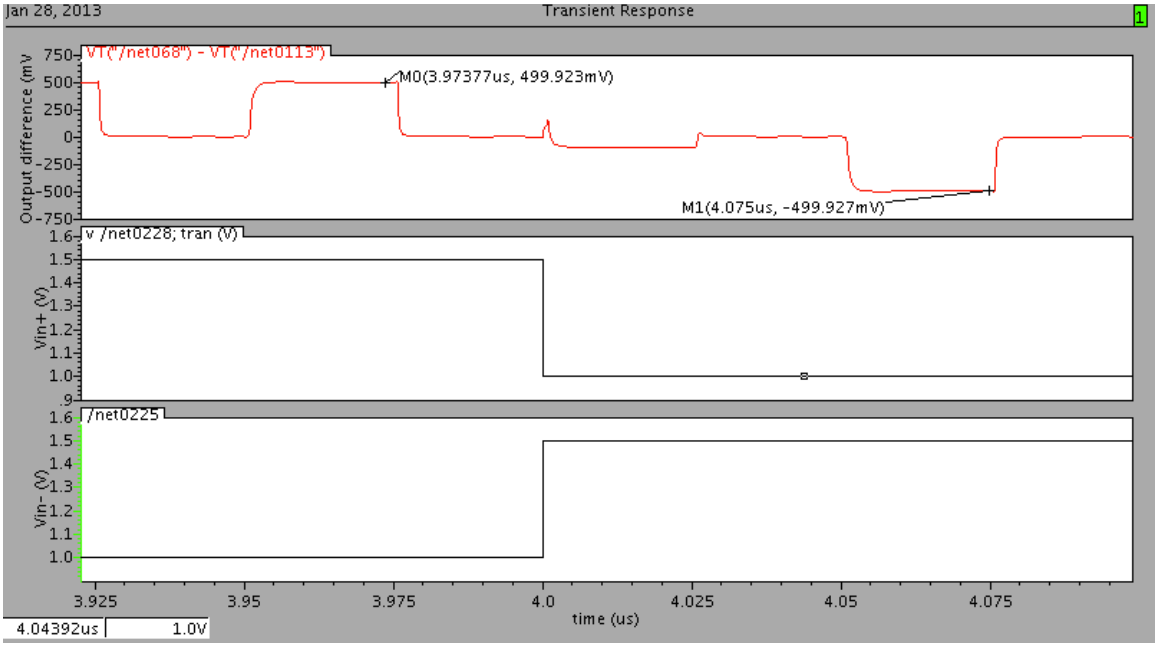

Figure 4.5 Simulation result of MDAC with full-scale input

As shown in Figure 4.5, when 1V full-scale voltage is applied as input, output voltage of MDAC is within [-499.927mV, 499.923mV]. Thus, error voltage is around 0.077mV, which is less than $\frac{1}{6}LSB$. The following stages use Op Amp sharing technique, and MDAC actually contains two sets of sampling circuitry. As shown in Figure 4.6, dual input operational amplifier is used in these MDACs. Selection bits S1~3 is synchronized to clock phase 2 while S1'~3' is synchronized to clock phase 1.

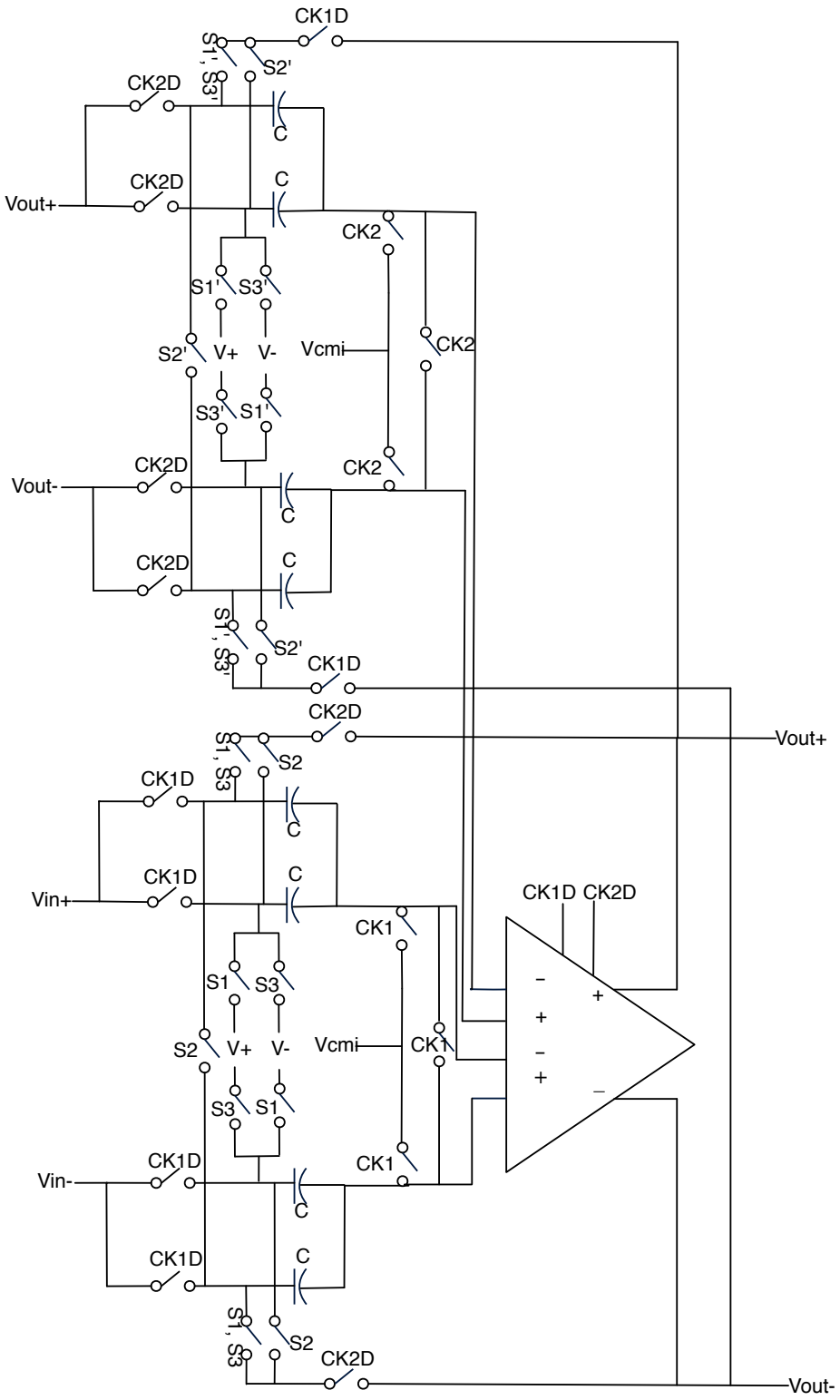

Figure 4.6 MDAC for Op Amp sharing stages

In clock phase 1, bottom part is in sampling phase, and top part uses Op Amp to do amplification, the result is sampled by following stage. In clock phase 2, bottom part is amplifying, while the top part samples the amplified output. Due to the separation of inputs, error charge of each part is reset in every clock cycle.

4.3 Comparator and Sub-ADC Design

In chapter 3, comparator architecture is discussed in detail. And circuit implementation do uses a pre-amplifier cascading with a clocked latch.

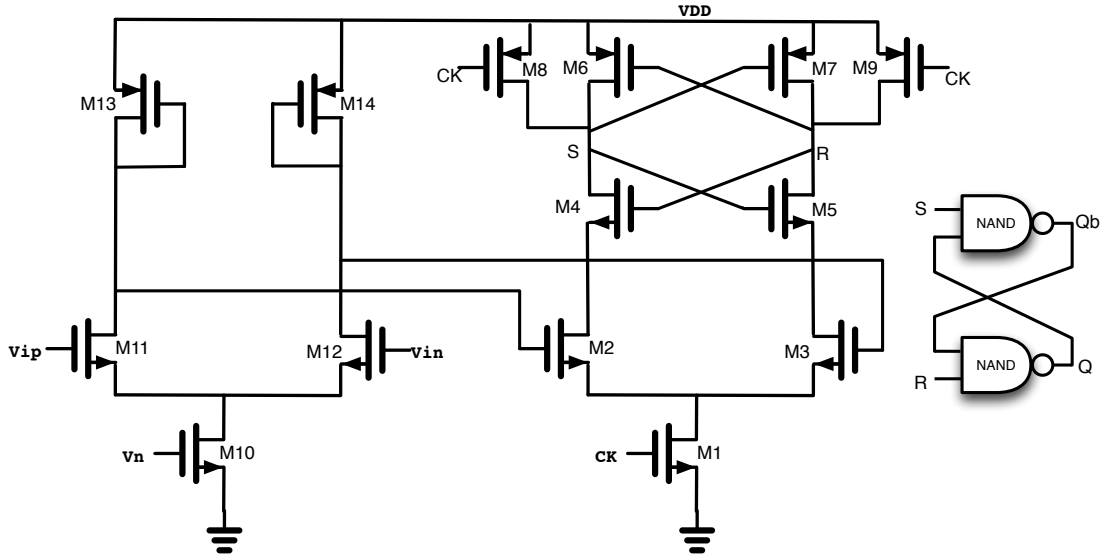

Figure 4.7 Comparator circuit

As shown in Figure 4.7, the first stage is simply an amplifier with diode-connected load. It provides gain of $\frac{g_{m11}}{g_{m13}}$. The second stage is clocked latch, which regenerates the output of first stage. Input transistors M11, M12 are sized to be $\frac{5um}{0.28um}$ to make sure that offset is well below $\frac{V_{ref}}{4}$ (125mV).

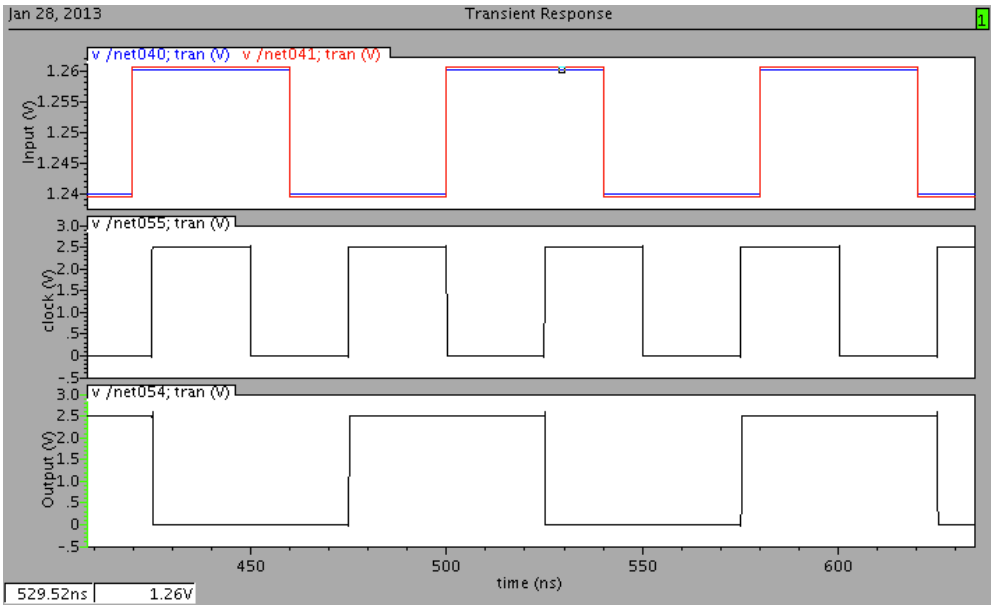

Figure 4.8 Transient simulation of comparator

Figure 4.8 shows the simulation results of comparator. When input toggles with $\pm 1LSB$ difference, comparator still works correctly. In fully differential circuit, comparator should be able to compare two groups of differential voltages. Combined with the discrete time nature in MDAC, dynamic comparator [18] is designed.

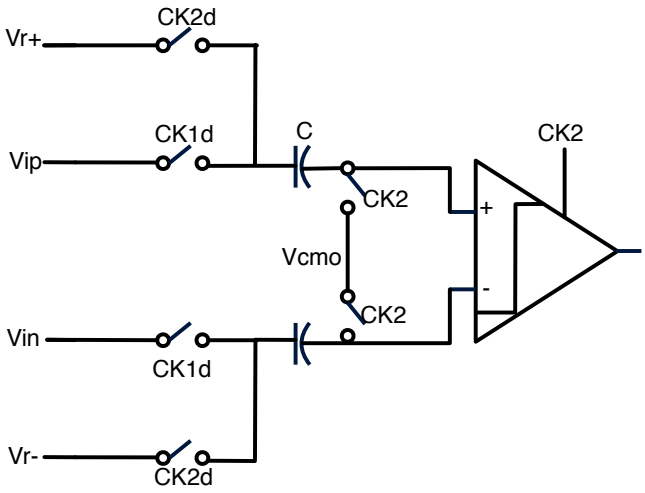

Figure 4.9 Dynamic comparator circuit

As shown in Figure 4.9, in clock phase 2, latch is in reset mode and capacitors store voltage information of V_{r+}, V_{r-} respectively. In clock phase 1, positive input at comparator becomes $V_{ip} - V_{r+}$ and negative input becomes $V_{in} - V_{r-}$. So it compares the differential difference:

$$V_{ip} - V_{r+} - (V_{in} - V_{r-}) = (V_{ip} - V_{in}) - (V_{r+} - V_{r-})$$

At the same time, latch is triggered and regenerates the difference. With this dynamic comparator, Sub-ADC can be implemented as below:

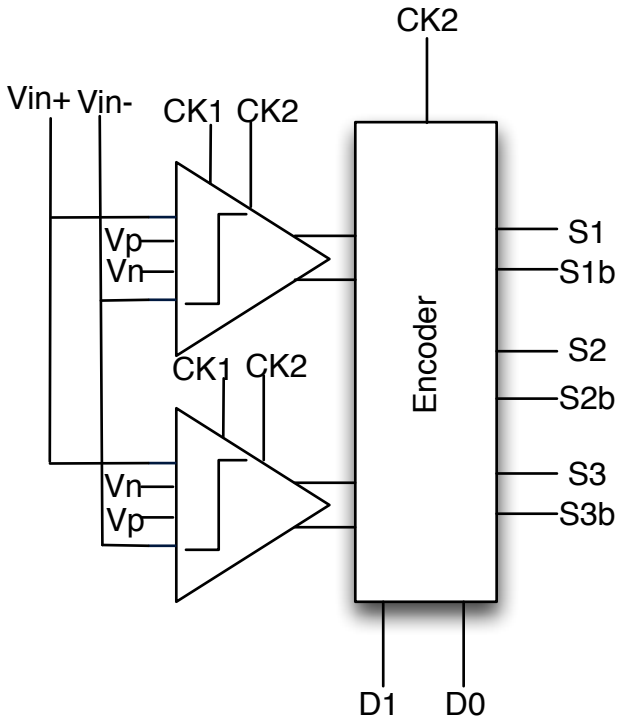

Figure 4.10 Sub-ADC with dynamic comparators

As shown in Figure 4.10, the decision threshold is determined by the difference of reference voltage. Thus, the top comparator compares input difference with $V_p - V_n =$

$\frac{V_{ref}}{4}$ while the bottom comparator compares input difference with $V_n - V_p = -\frac{V_{ref}}{4}$. Encoder output is synchronized to clock signal to give proper selection bits for MDAC.

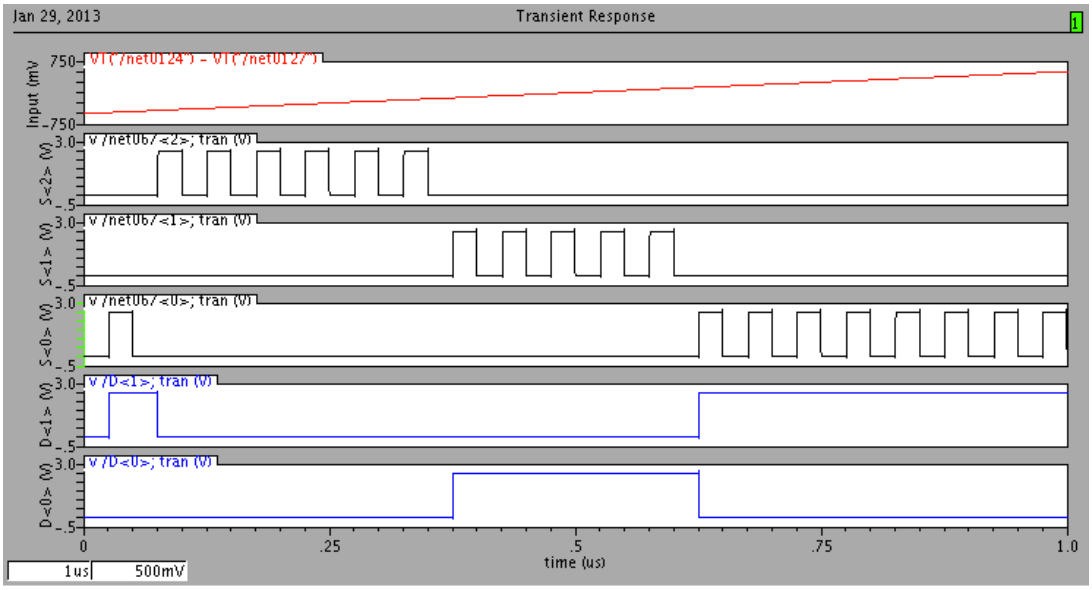

Figure 4.11 Transient simulation of Sub-ADC

As shown in Figure 4.11, when input is less than $-\frac{V_{ref}}{4}$, selection bits S are 100 and output bits are 00. When input is greater than $-\frac{V_{ref}}{4}$ and less than $\frac{V_{ref}}{4}$, selection bits S are 010 and output bits are 01. When input is greater than $\frac{V_{ref}}{4}$, selection bits S are 001 and output bits are 10. The behavior matches residue plot perfectly.

4.4 Non-overlapping Clock Generation

Non-overlapping clocks and their delayed version are frequently used in MDAC. Allocating proper clock sequence in sampling circuitry will reduce the effect of charge injection, clock feed-through and so on.

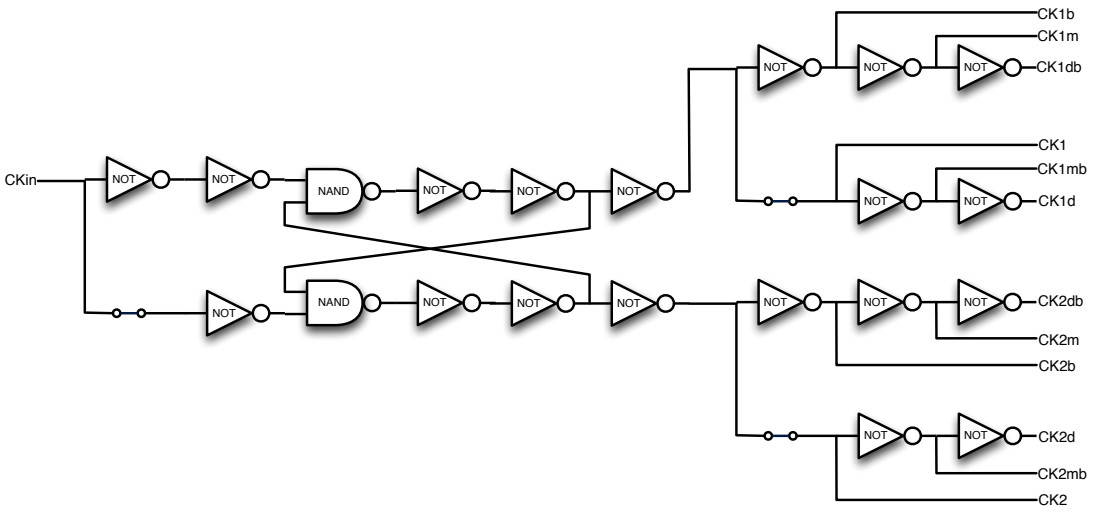

Figure 4.12 Non-overlapping clock generation circuitry

As shown in Figure 4.12, the circuitry generates non-overlapping clock phases and their delayed version. Transmission gates are used to match inverter delay. And some of intermediate inverter buffers are omitted in the figure. Cross-coupled circuit is the key part to generate non-overlapping phases. Below are the simulation results.

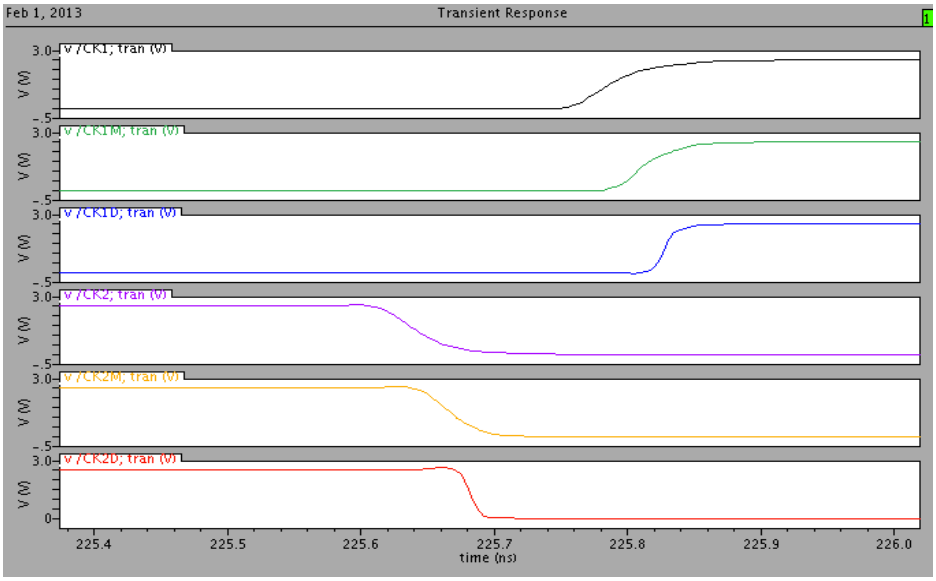

Figure 4.13 Simulation results of non-overlapping clock generator

As shown in Figure 4.13, CK1D is delayed version of CK1, while CK1M locates between CK1D and CK1. The same holds for CK2, CK2D and CK2M. Moreover, clock phase 1 is non-overlapping with clock phase 2 for 0.14ns duration.

4.5 Stage Design

The MDAC, sub-ADC and clock generator have been demonstrated above. Pipelined stage can be built form these blocks. Shown in Figure 4.14 is the diagram of first stage.

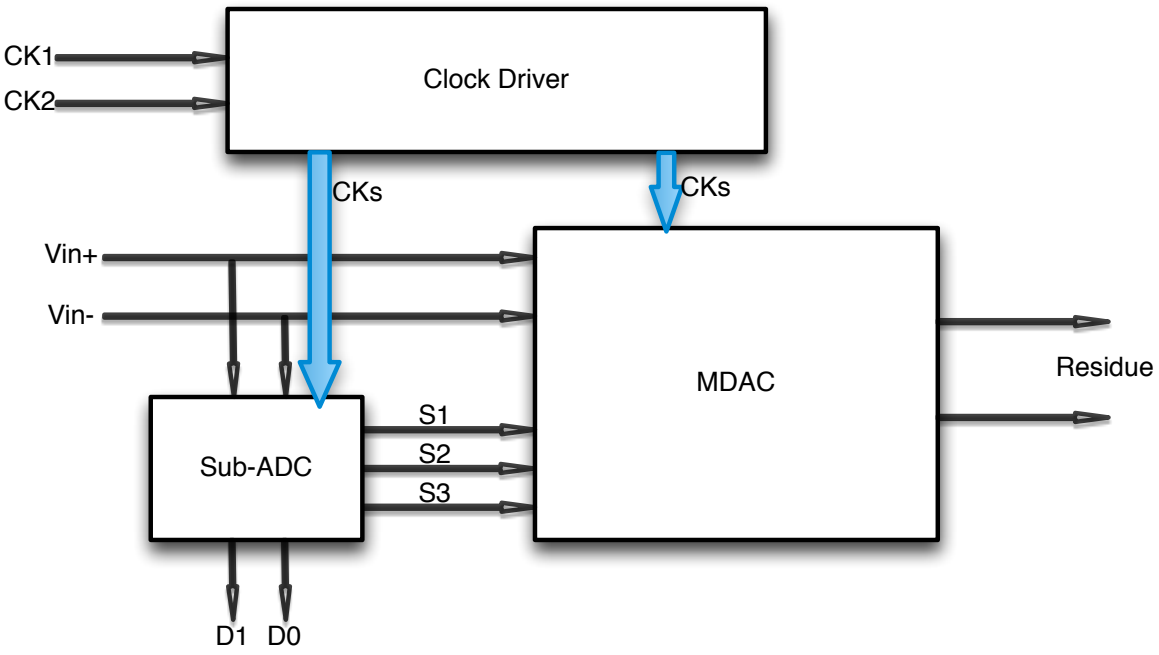

Figure 4.14 Architecture of first stage

Shown in Figure 4.14 is a traditional architecture of pipelined stage. Clock driver gives all clock signals to sub-ADC and MDAC. Selection bits and digital codes are generated from sub-ADC. Finally, MDAC outputs residue signal. Simulation results are shown in Figure 4.15. Input sine wave has 0.9V fully differential swing and frequency of 1.35MHz. And output matches well with the results calculated from residue plot.

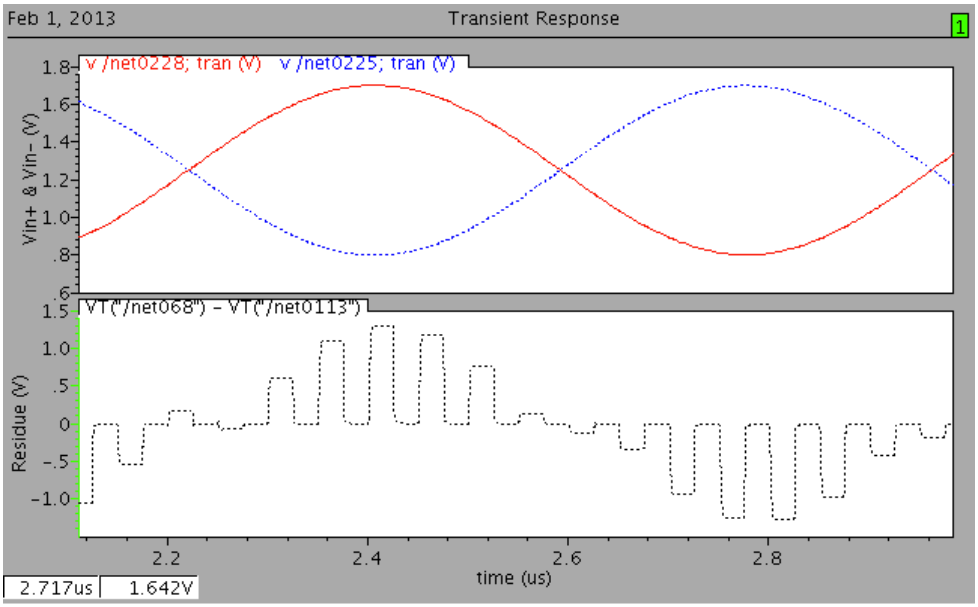

Figure 4.15 Simulation results of first stage

For the following stages, Op Amp sharing MDAC is used. And two sub-ADCs are necessary to generate 4 digital codes. The architecture is shown in Figure 4.16.

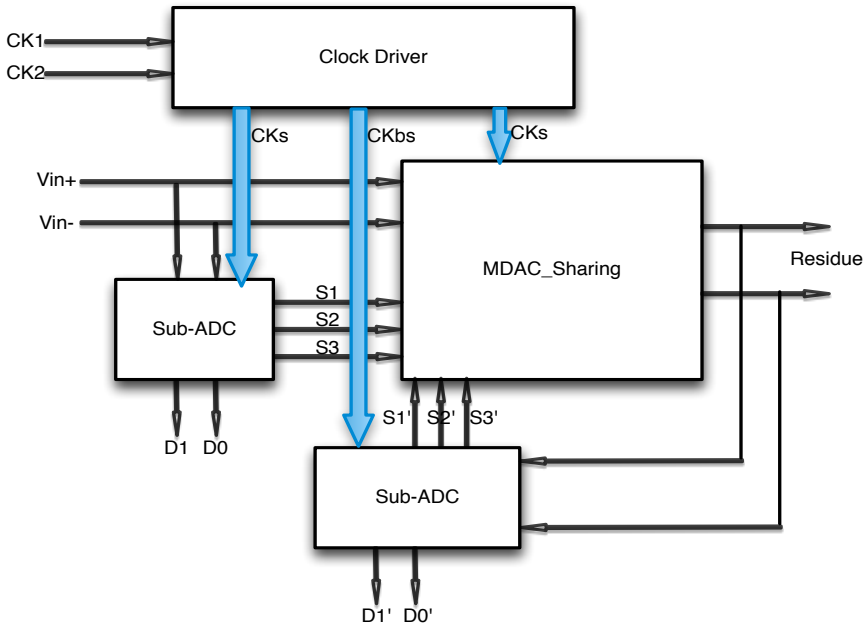

Figure 4.16 Architecture of Op Amp sharing stages

As shown in Figure 4.16, two sub-ADCs work at inverted clock phases. The first one takes input signal and generates corresponding digital codes. The second one takes Op Amp output as input and generates the other digital codes.

4.6 Bias Circuits

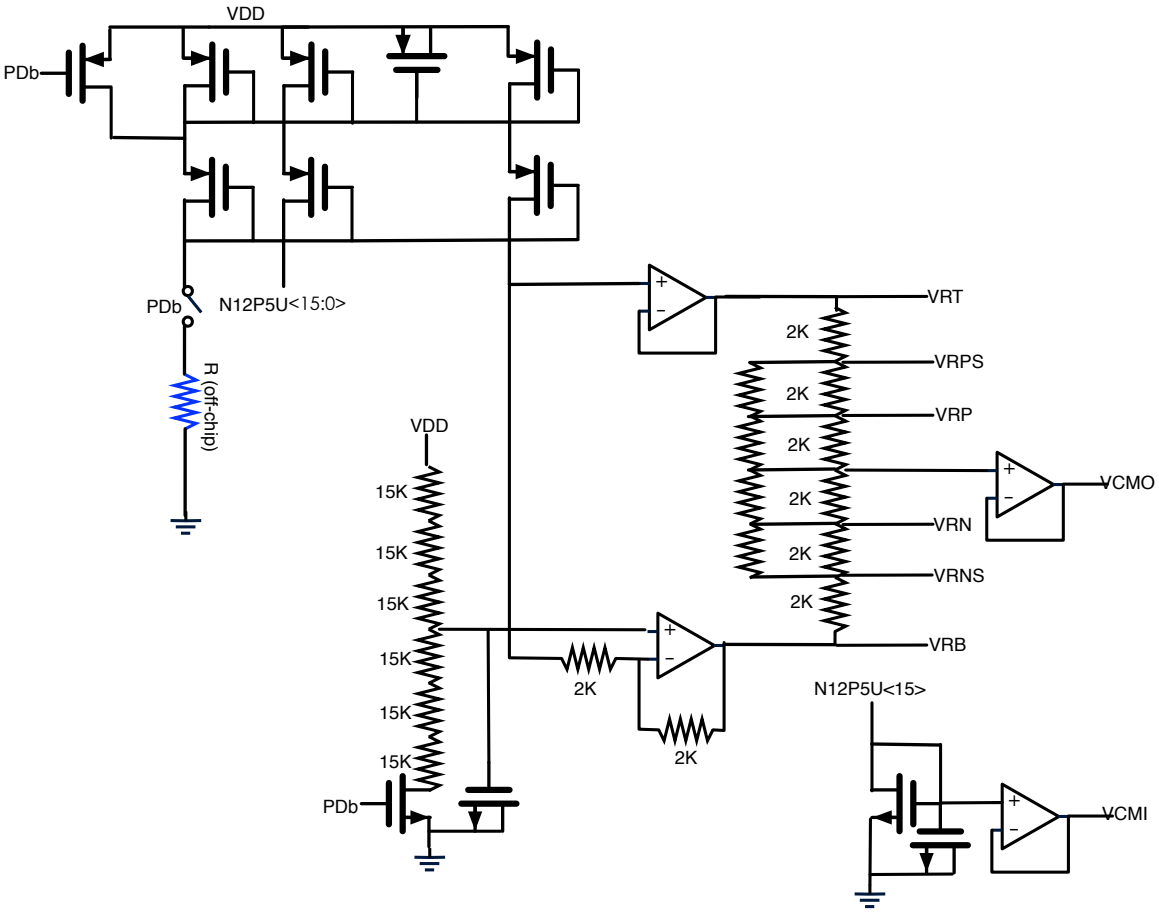

Figure 4.17 Bias circuits

As shown in Figure 4.17, bias circuits uses an on board tunable resistor to define 20uA current. And it generates copies of 12.5uA current for pipelined stages. Meanwhile, it defines reference voltage for MDAC and sub-ADC. Reference voltages need to provide

transient currents to charge or discharge capacitors, therefore, unity gain buffers are used to drive them. These buffering Op Amps are two stage amplifiers described before. But current consumption should be large enough to minimize the output noise voltage because the noise will directly alter reference levels. Furthermore, to get accurate rational voltage, a resistor train consisting of identical $2K\Omega$ resistors is used. Even with supply and common mode noise, the reference voltages can go up and down together. Figure 4.18 shows the waveform when PD goes from 1 to 0. And Table 4.3 concludes the voltage values.

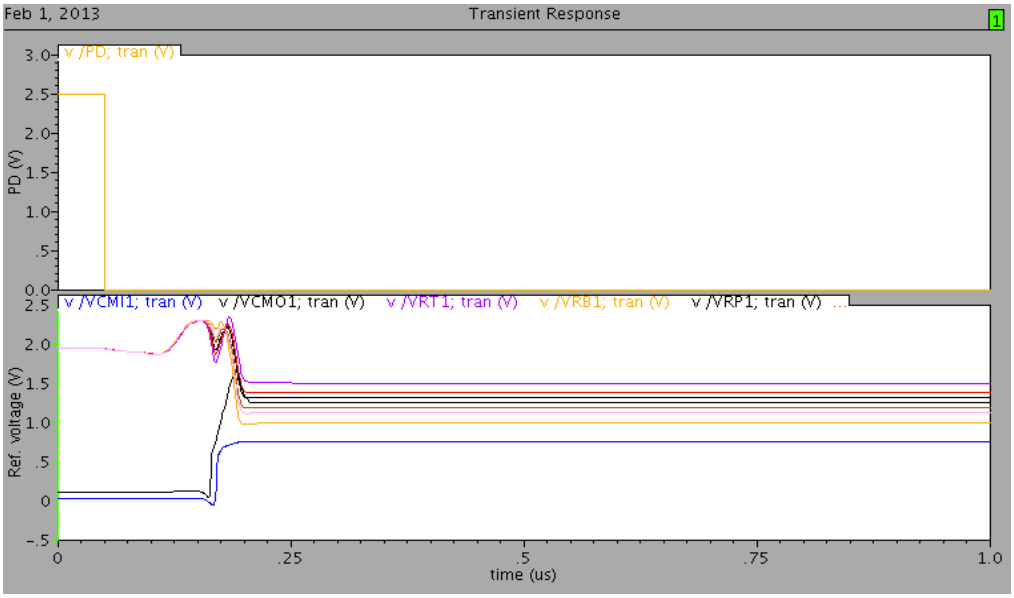

Figure 4.18 Simulation results of bias voltages

VCMO	VCMI	VRT	VRB	VRPS	VRNS	VRP	VRN
1.244V	0.75V	1.498V	0.997V	1.373V	1.122V	1.310V	1.185V

Table 4.3 Reference voltage values

4.7 2-Bit Flash ADC Design

Unlike sub-ADC used in pipelined stages, the last 2-bit Flash needs to provide exactly 2 bits. Therefore, it consists of three comparators as shown in Figure 4.19.

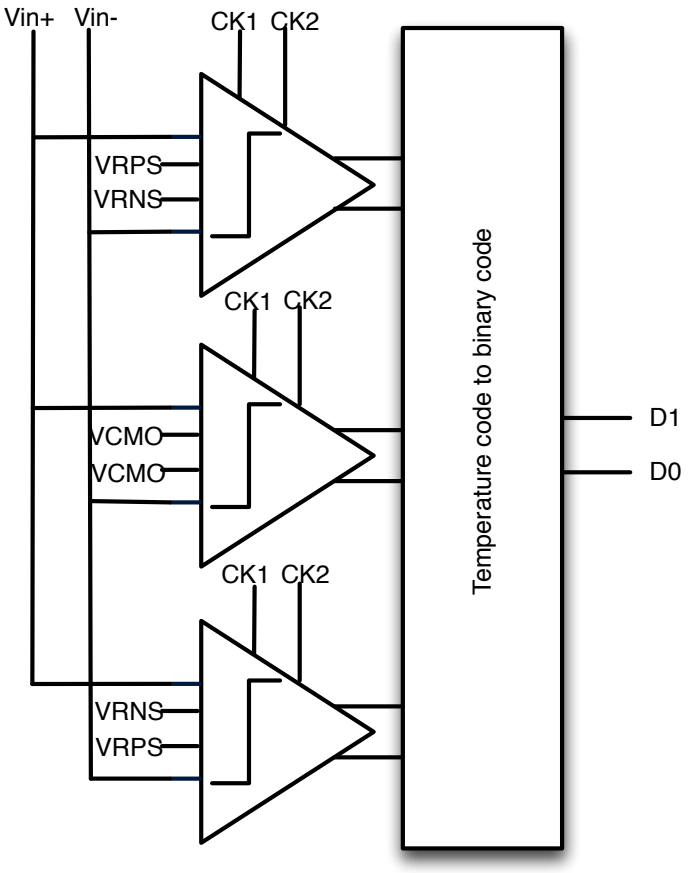

Figure 4.19 2-Bit Flash ADC

As shown in Figure 4.19, the decision threshold is actually $-\frac{V_{ref}}{2}, 0, \frac{V_{ref}}{2}$. And simple logic gates are used to perform temperature code to binary code conversion.

4.8 Digital Error Correction

Digital error correction circuits are shown in Figure 4.20, it delays digital codes of each stage by half clock cycle. Then full adder performs addition to combine the delayed outputs. Through this process, redundancy is omitted. The result codes DO<10:0> are final output of ADC.

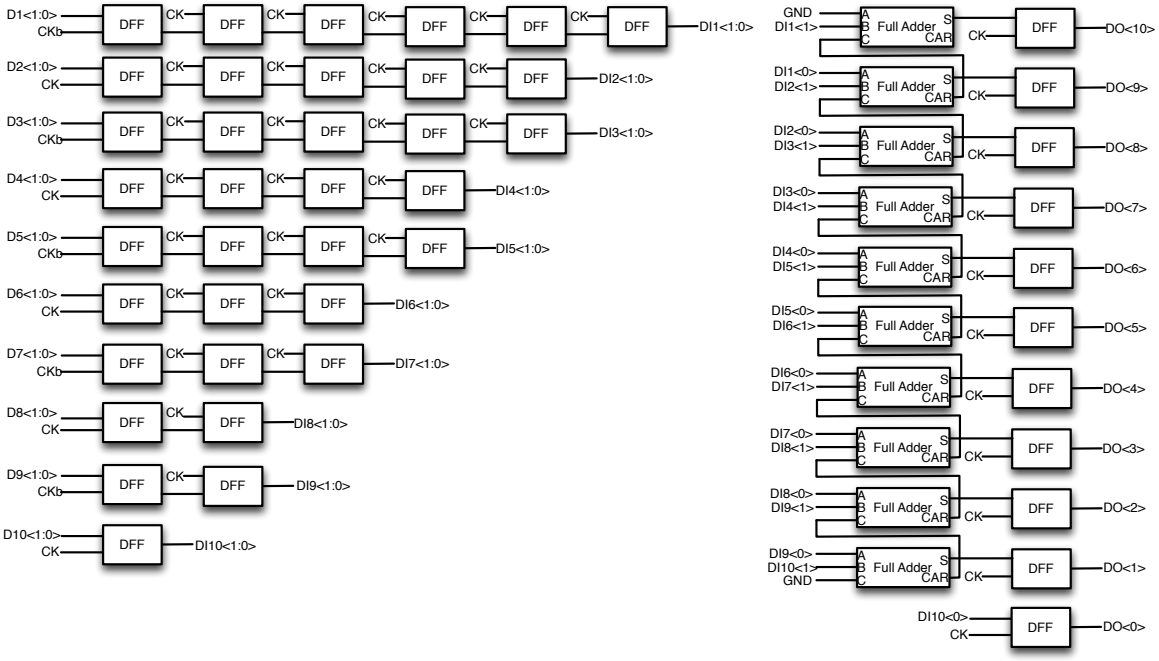

Figure 4.20 Digital error correction circuits

4.9 Layout Design

Layout is very critical in ADC design. Since analog circuits are embedded in quite discrete time environment, switching and digital circuits will have great impact on analog circuitry. The most severe issue is the variation on power supply. Due to bond wire inductance, the core power supply may vary a lot when digital circuits are randomly on and off. So it's a good option to separate analog supply and digital supply when doing layout. Figure 4.21 shows the proposed idea.

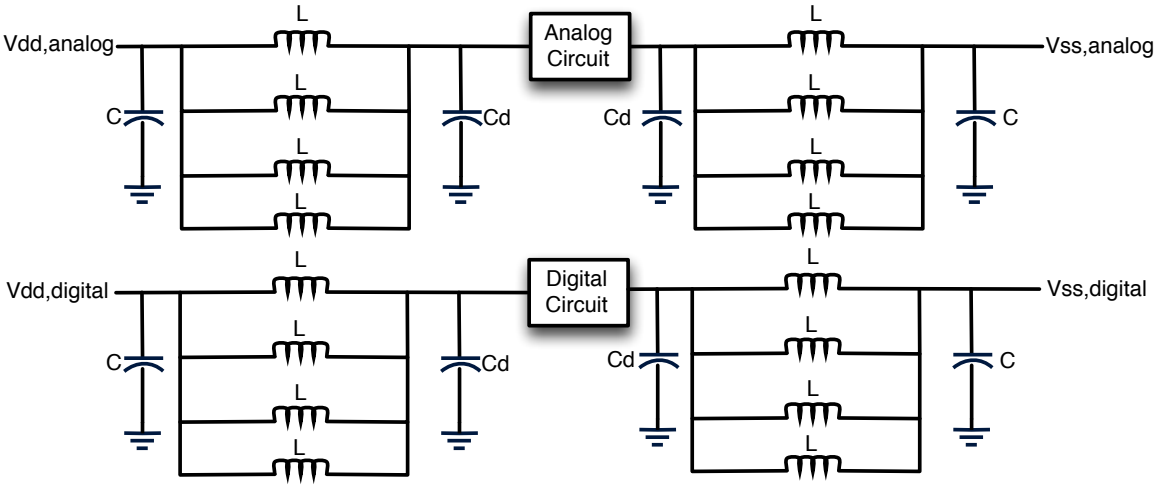

Figure 4.21 Separated power supply for analog and digital circuits

As shown in Figure 4.21, both digital and analog supply contain four pads for Vdd and four pads for Vss, therefore, the bond wire inductances are reduced by a factor of 4. And both on-chip and on-board decoupling capacitors are added to provide transient current. The proposed ADC layout has 33 pads. Figure 4.22 shows the entire layout.

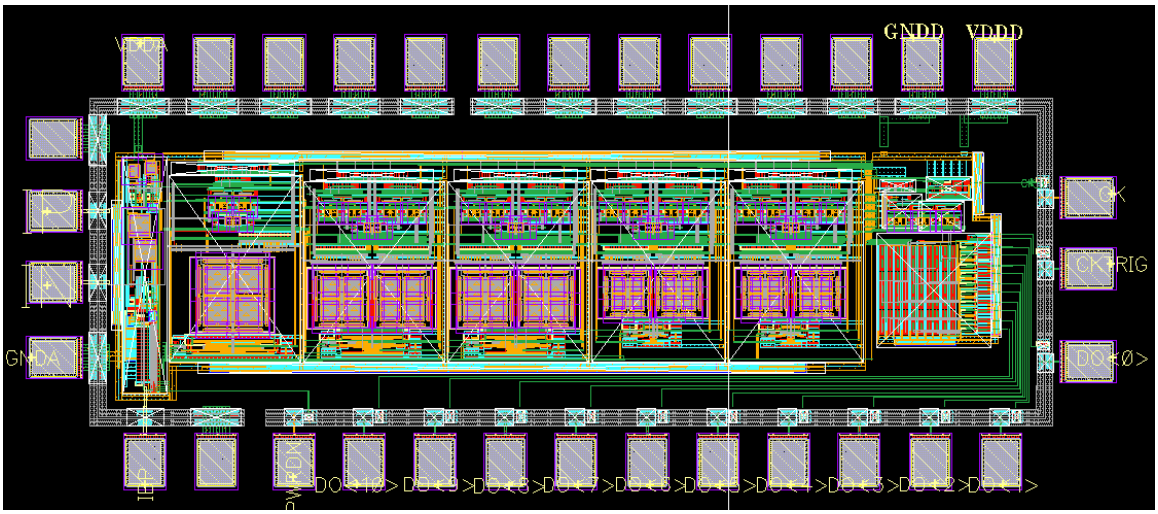

Figure 4.22 Pipelined ADC layout

Shown in Figure 4.22, 33 pads surround the rectangle. In the core layout, the left most part is bias circuits, then it comes the 1st, 2nd, 3rd, 4th and 5th stages. After that, 2-bit Flash ADC is placed on right top of core. And the clock generation circuit is placed right to it. Finally, digital error correction circuits are placed on the bottom right corner. Table 4.4 concludes the pads number and active core size.

Analog Vdd pads	Digital Vdd pads	Analog Vss pads	Digital Vss pads	Analog in/ out pads	Digital in/ out pads	Core size
4	4	4	4	3	14	1250um*310um

Table 4.4 Conclusion on pads number and core size

CHAPTER 5

Results and Conclusions

5.1 11-Bit Pipelined ADC

The test bench of ADC should include bond wire inductance and resistance. Also, parasitic capacitance must be taken into account. Figure 5.1 shows the test bench.

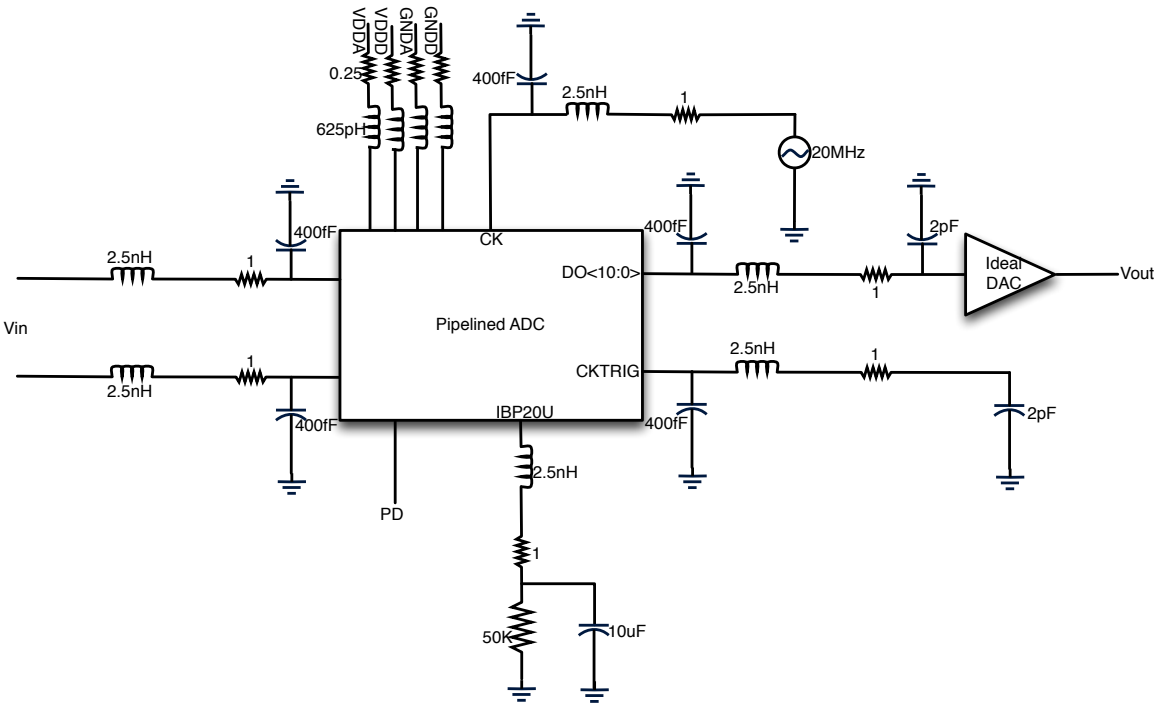

Figure 5.1 Test bench of Pipelined ADC

As shown in Figure 5.1, bond wire model consisting of 1ohm resistor and 2.5nH inductor is used. The bond wire inductance and resistance are reduced to one fourth of original value for power supply because there are 4 pads for each one. 50Kohm off chip resistor defines 20uA current, and 10uF on-board capacitor is used to deal with thermal noise.

400fF capacitors indicate the parasitic of pads. At the same time, CKTRIG and DO<10:0> signals drive 2pF capacitors which model the input terminal of logic analysier. Finally, an idela DAC combines ADC output to waveform. Then, it can be sampled to get DFT results.

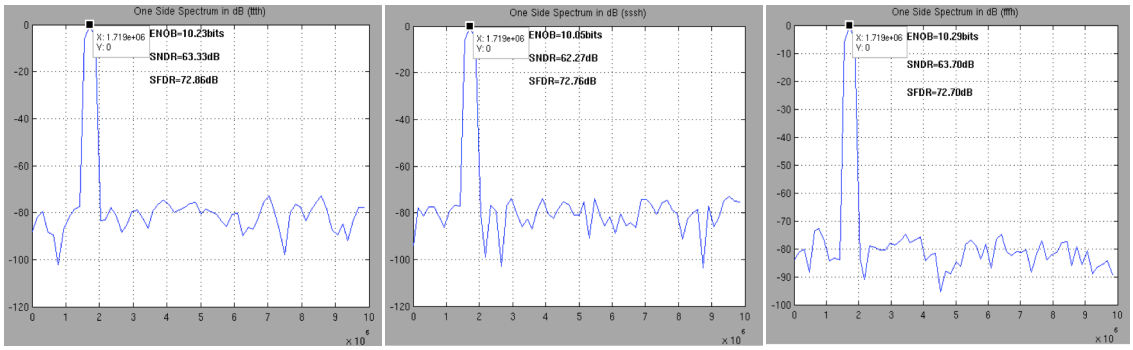

Figure 5.2 DFT results in pre-layout simulation under different corners (ttth, sssh, fffh)

Figure 5.2 shows the simulation results for this Pipelined ADC in 100 ºC with noise included. Input signal is 1.719MHz sine wave and output waveform is analyzed with 128 points DFT. Circuit performs best in fffh corner and worst in sssh corner. In worst condition, SNDR is 62.27dB. In Nyquist sampling condition, SNDR stays the same.

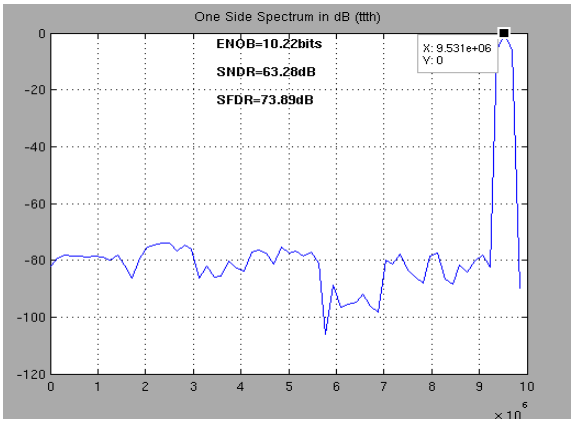

Figure 5.3 DFT result in Nyquist condition under ttth corner

Shown in Figure 5.3 is the DFT result when input frequency is increased to 9.531MHz. SNDR is now 63.28dB under typical corner. Since sssh corner is supposed to be worst, post-layout simulation mainly focuses on ttth and sssh corners.

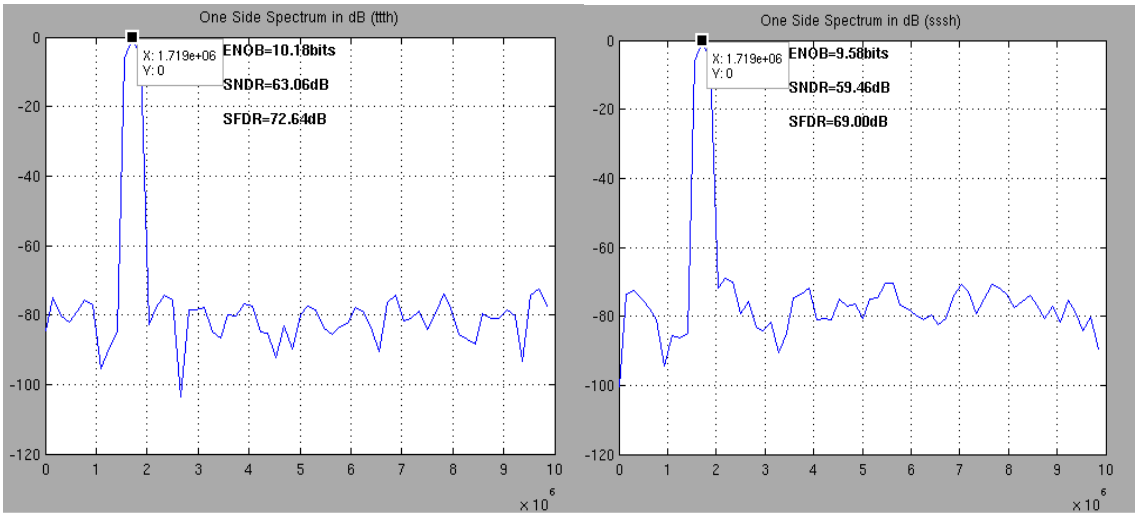

Figure 5.4 Post-layout simulation results under different corners (ttth, sssh)

As shown in Figure 5.4, the worst case happens under sssh corner, and SNDR is 59.46dB. Finally, current consumption is found to be around 11mA as indicates in Figure 5.5.

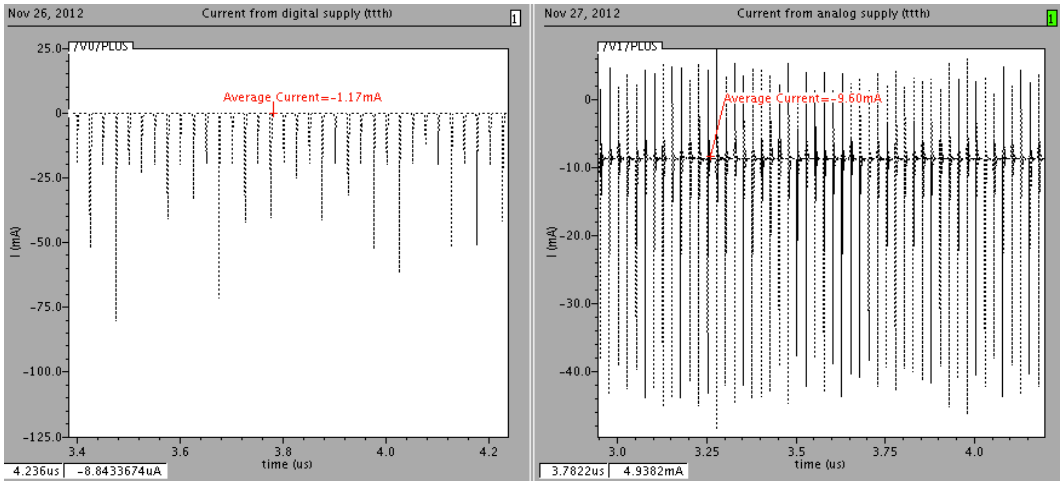

Figure 5.5 Current consumption under ttth corner

Table 5.1 concludes the performance metrics for this Pipelined ADC.

Power consumption	Sampling frequency	SNDR	ENOB	SFDR	@Temperature
27.5mW	20MHz	59.46dB	9.58 bits	69.00dB	100 degree

Table 5.1 Performance metrics of the designed Pipelined ADC

5.2 Conclusions

This Pipelined ADC is submitted to tape out on January 2013. It will be used for linearity, power and temperature sensing. On-chip temperature power and amplitude sensors extract analog information and ADC digitizes it. Then digital codes are used to control other circuits for self-healing. This compensates effects of temperature linearity and power variations on circuit performance. As today's SoC becomes more complex, this idea is more practical to guarantee the performance yield. Moreover, the latency of this Pipelined ADC won't affect stability because it's not used in feedback loop. On the other hand, it can be also used to digitize down converted signals in radio chain for zero or low IF applications, provided the bandwidth is sufficiently narrow.

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