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OPTICAL TIMING RECEIVER FOR THE NASA SPACEBORNE RANGING SYSTEM PART II: HIGH PRECISION EVENT-TIMING DIGITIZER

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August 1978

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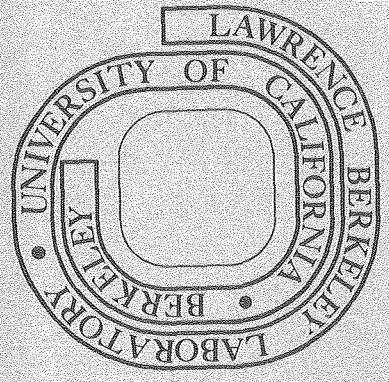

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Optical Timing Receiver for the NASA Spaceborne Ranging System
Part II: High Precision Event-Timing Digitizer

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Abstract

Position-resolution capabilities of the NASA Spaceborne Laser Ranging System are essentially determined by the time-resolution capabilities of its optical timing receiver. The optical timing receiver consists of a fast photoelectric device; (e.g., photomultiplier or an avalanche photodiode detector), a timing discriminator, a high-precision event-timing digitizer, and a signal-processing system. The time-resolution capabilities of the receiver are determined by the photoelectron time spread of the photoelectric device, the time walk and resolution characteristics of the timing discriminator, and the resolution of the event-timing digitizer. It is thus necessary to evaluate available fast photoelectronic devices with respect to their time-resolution capabilities, and to develope a very low time walk timing discriminator and a high-resolution event-timing digitizer to be used in the high-resolution spaceborne laser ranging system receiver.

This part of the report describes the development of a high precision event-timing digitizer. The event-timing digitizer is basically a combination of a very accurate high resolution real time digital clock and an interval timer. The timing digitizer is a high resolution multiple stop clock, counting the time up to 131 days in 19.5 ps increments.

The digitizer also generates several reference frequency markers for the synchronization of all parts of the laser ranging

system throughout the entire range of the mission. Typically, the digitizer measures the time difference between a pair of start-stop events. The start pulse is generated each time the ranging laser is fired and fed to one of the event inputs of the digitizer. The time between the leading edge of the start event and the mission start pulse is digitized and stored. The input of the digitizer is then ready for the next stop event. The time needed for a light pulse to reflect back from the target is approximately known and it is stored into the digitizer range counter prior to laser firing. The absolute accuracy and stability of the digitizer is determined by an external 50 MHz master oscillator, which serves as a standard time marker. Since the digitizer uses a single processing channel for each start/stop event, the thermal drift and tracking problems become negligible even for the largest time ranges. The digitizer is designed to be CAMAC compatible to a data processing system and the dual peak-sensing timing discriminator.

I. Introduction

Satellite laser ranging methods have been used successfully for precise satellite orbit determination, polar motion determination, the measurement of earth tidal parameters, high precision distance measurements between laser sites, and for the calibration of spaceborne radar altimeters (1). More recently, it has been proposed that a high precision laser ranging system be applied to geophysical studies, particularly those concerned with solid earth dynamics measurements and earthquake prediction, using a Laser Geodetic Satellite (LAGEOS) (2), and the Space Shuttle (3). Since pulsed laser ranging systems determine the distance to a target by measuring the time of flight of a short light pulse to a target and back, their position-resolution capabilities are essentially determined by the time-resolution capabilities of their optical timing receiver. An optical timing receiver consists of a fast photoelectric device, primarily a standard or an avalanche photodiode

detector, a timing discriminator, a high-precision event-timing digitizer, and a signal processing system. The time resolution capabilities of the receiver are determined by the time spread of the photoelectric device, the time walk and resolution characteristics of the timing discriminator, and the time resolution of the event timing digitizer. Consequently, to achieve optimum results, it was necessary to evaluate fast photoelectric devices with respect to their time resolution capabilities in order to select the best available, to design a very low time walk high resolution timing discriminator and to develope a high-precision event timing digitizer to be used in this High Resolution Spaceborne Laser Ranging System Receiver.

An evaluation of timing characteristics of the very fast classically designed and static crossed-field photomultipliers was carried out and was reported in Ref. (4)-(9).

The dual peak-sensing timing discriminator with an amplitude dependent time walk of less than ±150 ps for a 100:1 dynamic range of Gaussian-shaped input signals, was designed by the Electronics Research and Development Group of the Lawrence Berkeley Laboratory, (10). As a further step in the development of the spaceborne optical timing receiver, it was necessary to design a high precision event-timing digitizer with a time resolution of approximately 20 ps in a range up to 131 days.

This report describes the design of a high precision event-timing digitizer. The event-timing digitizer is basically a combination of the very accurate high resolution real time digital clock and an interval timer. Typically, the digitizer measures the time difference between a pair of start-stop events. The digitizer is started at the beginning of each mission and like a clock, counts the time in a range of up to 131 days in 19.5 ps increments. The start pulse is generated each time the laser is fired and fed to one of the event inputs of the digitizer. The time between the leading edge of an event and the mission start pulse is digitized in a time shorter than 5.3 μs and stored in the digitizer's buffer register. The time is given in 59-bit

binary words. The input of the digitizer is then ready for the stop event. The time needed for a light pulse to reflect back from the target is approximately known and it is stored into a digitizer range counter prior to the laser firing. Also, the desired aperture width is loaded at the same time into an enable counter.

An accurate built-in 50 MHz clock reference oscillator is adequate for the testing and ranging of shorter distances. However, for long distance ranging and operation over long periods of time, an external clock reference of extremely well defined characteristics should be provided. In this case, the absolute accuracy and stability of the digitizer are determined by the external oscillator, which serves as a standard time marker. Although a number of systems have been devised for subnanosecond time-interval measurements, based on various principles, (16)-(17), our analysis and design experience has shown that an interpolation technique is the best method for the very high resolution requirements, (13)-(14), (18)-(20).

The digitizer uses a single processing channel for each start/stop event. Consequently, the thermal drift and tracking problems become negligible even for the largest time ranges.

The digitizer is a CAMAC compatible modular system, allowing full remote control of all functions. The modules fit any standard CAMAC crate. An appropriate standard crate controller is needed for the communication with the particular computer. Front panel controls and light emitting diode readouts are also provided for manual operation of the digitizer. The maximum total power required by the digitizer, without the display, is approximately 14 W. The events cannot be processed when the Digitizer is in the stand-by mode, but the mission time counting and all vital functions continue without interruption.

The design of the high precision event-timing digitizer, which is an improved version of instruments described in Ref. (18), (19), (20), and (13) is based on the experience acquired

over a number of years by the Electronics Research and Development Group in developing high precision time interval digitizers and very fast timing discriminators for atomic and molecular subnanosecond fluorescence decay time measurements.

2. Description of the High Precision Event Timing Digitizer

The High Precision Event Timing Digitizer (further on reffered to as Digitizer) is basically a fast multiple stop clock. The Digitizer is a part of a space borne laser ranging system where it has to meet extreme requirements on time range and resolution, stability and accuracy, low deadtime and low power dissapation.

Normally, the Digitizer is started at the beginning of each mission and counts the time like a clock, in a range of up to 131 days in 19.5 ps increments. Also, the Digitizer generates several reference frequency markers to assist in the synchronization of all the parts of the laser ranging system throughout the mission. The phase of these marker frequencies (known to about 40 ps) can be locked-in on the mission start pulse (Fig. 1).

The typical application of the Digitizer is the measurement of time difference between a pair of start-stop events. The start pulse is generated each time the laser is fired and is fed to one of the event inputs of the Digitizer. In less than 5.3 μs the time between the leading edge of the start event and the mission start pulse will be digitized and stored in the Digitizer's buffer register. This time is given in a 59-bit binary word, the LSB of which corresponds to a time increment of 20/1024 = 19.53 ps. The input of the Digitizer is then ready for the stop event. The approximate time needed for a light pulse to reflect back from the target is normally known and should be stored into the Digitizer's Range Counter prior to laser firing. Also, the desired aperture width (time range when a stop signal will be accepted) should be loaded at the same time into the Enable Counter.

The Range Counter is started at the same time as the start event is accepted. The event stop input of the Digitizer is

enabled at the end of the range, at which point the enable counter starts. The input remains enabled until the end of enable time counting. The event stop signal can be processed only if entered into the Digitizer during this aperture time. The accepted stop event is digitized in the same way as the start event. The leading edge of the stop pulse is referred to the mission start and the time given in 59-bit words. Also, the stop event is tagged by an additional (60th) bit for easier computer identification.

The stop event remains stored in the Event Register until the start event is cleared from the Buffer Register. The stop event is then automatically shifted into the Buffer Register. The Digitizer is then ready again. Thus, regardless of the readout speed, a single start-stop pair can always be digitized and stored later. Several other modes of operation are also possible. A more detailed description is given in the following sections.

It should be pointed out, that the mission counting is not affected by any event following the mission start, until the mission is cleared or aborted by appropriate commands.

The Digitizer is a CAMAC compatible modular system, allowing full remote control of all functions. The modules fit any standard CAMAC crate. An appropriate standard crate controller is needed for the communication with the particular computer. Front panel controls and LED readouts are also provided for manual operation of the Digitizer. The total power required to run the Digitizer (with the display off) is about 14 watts. In stand-by operation the power can be cut to 7 watts by a remote command. The events connot be processed in the stand-by mode, but the mission time counting and all vital functions continue without interruption.

An accurate built-in 50 MHz clock reference oscillator is adequate for the testing and ranging of shorter distances. However, for long distance ranging and operation over long periods of time, an external clock reference of extremely well defined characteristics should be provided.

3. Operating Principles of the High Precision Event-Timing Digitizer

Digitizing time intervals with incremental resolution of 20 ps by merely counting high frequency clock pulses between start and stop events is presently impossible, since it would require a counting technique in the 50 GHz range. However, various interpolation techniques can be used where the equivalent of count frequencies of up to 100 GHz have been obtained, (18), (19), (13), (14), (15). Interpolation techniques reduce the real counting frequencies to below 50 MHz eliminating the need for power consuming high speed circuits. The penalty is that the processing time per each event increases accordingly. In normal laser ranging the rate of events is generally low, being limited by the laser pulse rate, and processing times of 50 to 100 μs are generally acceptable. In order to measure start-stop time intervals shorter than the processing time, two identical interpolation circuits are needed, one for the start and the other for the stop event, (13), (14). Since the interpolation circuits are basically analog-to-digital converters, they must be identical and perfectly matched for thermal tracking to minimize the timing error.

The Digitizer described here uses a new interpolation technique that results in a tenfold reduction of the processing time yet offering the same incremental resolution as a high frequency clock (12), (14). At 50 MHz clock frequency, it takes less than 5.3 μs to digitize each event in 19.53 ns increments. Therefore, 5.3 μs is the minimum time interval that can be digitized by using the same interpolator circuit for both the start and the stop event. 5.3 μs corresponds to a minimum one-way target distance of less than 0.5 miles, making possible on-site ground ranging tests. A single optical receiver thus can be used to serve all events, making the system virtually self-tracking. Thermal drift also becomes negligible even for the largest time ranges.

Functionally, the Digitizer system consists of three distinct sections, which are conveniently contained in separate CAMAC modules: 1. Clock and Calibrator, 2. Tandem Interpolator (or Stretcher) and 3. Logic (consisting of 3 modules, because of

technical reasons, which function as a single unit). The general block diagram of the Digitizer, including the CAMAC crate and controller, is shown in Fig. 1.

The CAMAC crate provides the housing, power and communication between the modules and the computer. The interconnections between the modules are kept at minimum and are made possible by rear panel 50-ohm terminated connectors carrying fast signals and, where necessary, by the flat edge connectors for the slow (TTL) signals. Front panels have coaxial connectors for communication with the other parts of the ranging system, also LED indicator lights and the controls for manual operation of the Digitizer.

The block diagram in Fig. 1 can be best explained by following the sequence of steps in a typical ranging application. The Digitizer is first initialized by a CAMAC command from the computer, which leaves the latchable parts reset and all the modules under power. The clock is the only unaffected circuits, continually supplying shaped 50 MHz reference signals to the Clock Frequency Divider, Tandem Interpolator and Control Logic. In order to start the mission counting, a Mission Enable Computer command is first received and decoded by the CAMAC Logic, setting the Mission Start Latch in the Control Logic. (See also the basic timing diagram in Fig. 2, lines A and B.) The mission can now be started by the first pulse arriving at the Mission Start input of the Tandem Interpolator.

It is preferable however, to start the mission by the Mission Start output from the Clock Frequency Divider in order to retain a known accurate phase relationship between the Frequency Outputs and any digitized event for the rest of the mission time. In that case, the Mission Start output should be connected externally to the Tandem Interpolator Mission Start input before the Clock Frequency Divider is started by a computer command (lines C and D in Fig. 2). Other options for the mission start are possible, but the one just described gives the most accurate information of the phase relationship between clock mission time and those parts of the laser

ranging system that use the Digitizer's frequency Divider for timing.

Several frequency outputs are derived by the Divider from the 50 MHz reference frequency and are available for external timing of the laser ranging system components. Mission Start outputs are 1 Hz marker pulses which are phase locked to all of the frequency outputs. All first pulses at each frequency output appear simultaneously upon the CAMAC command and remain phase-locked for the rest of the mission time.

The mission is started by the first Mission Start pulse (line E) that appears within one reference clock period (20 ns) after the Frequency Divider Latch was set (line D). It is assumed that the CAMAC command that set the latch was uncorrelated to the reference clock phase. A Mission Start pulse appears each second at the input afterward, for as long as the Frequency Divider is running.

Busy output (line F) appears each time the processing of an event is in progress. The first Busy indicates the Mission has started and no other event can be accepted. Busy time is less than 5.3 μs and the same for any event. A new event, meeting the input conditions, can be processed immediately after the busy output returns to zero.

During the first busy period following the start of the mission, the counting of time in 20 ns increments starts in the Auxiliary Counter after the second reference frequency clock following the mission start pulse. The initial time fraction between the Mission Start pulse and the second following clock pulse is stretched in the Tandem Interpolator and digitized in the "Coarse" Counter and "Fine" Counter in 19.53 ps increments. This information is an important constant, different for each mission start and the reference clock. This constant is used for the computation of the exact time between any subsequent event and the mission start. It remains stored during the mission in the "Coarse" and "Fine" Registers. Also, this information is treated as a

regular event and is temporarily stored in the Event Register after passing the Adder. Event Ready (Fig. 2, line G) signals that the conversion process is completed and that the event has been stored in the Event Register.

The Buffer Register (the second storage stage) was cleared previously when the Digitizer was initialized so the second transfer takes place immediately. The Buffer Register generates the readout request ("Buffer Ready," line H), and the event clear that enables the Digitizer for the acceptance of a new event.

The Digitizer is now ready for the ranging. In space-borne laser ranging, the expected time range between any start and stop pair is computed and the values loaded into the Digitizer before each laser shot. A CAMAC command presets first the Digitizer to the time needed for the return of the light pulse from the target (still referring to Fig. 2 Range time, line M), and another command presets the time aperture (Enable Time, line N). Only during the aperture time will the stop input of the Digitizer be kept open, minimizing the possibility of an error due to spurious stop pulses. The final command is Start Event Enable (line P), setting the Start Event Enable Latch in Control Logic (line R). Event Start input to Tandem Interpolator is now enabled. A fraction of the laser pulse generates the Event Start pulse (line S), and the start event conversion process is set in the Tandem Interpolator. A new Busy signal indicates that the processing is in progress (line F).

During the Busy time the Mission Counter is stopped by switching the mission clock counting temporarily to the Auxiliary Counter. At the same time the "Coarse" Counter and the "Fine" Counter digitize the remaining fraction of the start event time which is smaller than a clock period. The result of the counting is fed to the Adder (Fig. 1), where the exact time difference between the start event and the mission start is computed.

After 256 Auxiliary Counter clock pulses have been counted (5.12 μs), the counting is switched back to the Mission Counter. The time equivalent of the mission 256 counts is also added to

the Mission Counter so that there is no gap left in the mission counting. The start time event is then transferred from the Adder first into the Event Register and then into the Buffer Register provided the latter is free. Event Clear (line K) is then generated. The Event Start Latch in Control Logic is thus cleared so that the event start input can no longer accept a signal. Busy returns to zero indicating that the start event conversion is over.

Range counting that started at the same time the start event was accepted, still continues in 20 ns increments until the preset range time is reached (line T). The Enable Counter starts at this point counting for the duration of the preset enable time (line V). Event Stop input to the Tandem Interpolator is enabled during this time. Only a stop event coincident with the enable time is accepted (line V) and stop event time is digitized. The procedure is identical to the start event conversion. The event stop time is also referred to the mission start and stored first in the Event Register and further transferred automatically when the Buffer Register is free. In order to tag the stop event, the 60th bit is set and stored along with the other 59 time bits.

The three Digitizer event inputs are controlled independently and a number of operation sequences different from the described one, are possible. If only one optical receiver for the laser ranging system is available, the Event Stop input alone can be used for both the start and stop events, and even for the mission start. As mentioned earlier, this mode offers also the most stable and accurate results because all the processed events involve the same circuits.

The Digitizer also comprises an independent calibrator (Fig. 1) for easier test and calibration of time ranges. The Calibrator is a marker pulse generator. The marker pulse trains are obtained by dividing the reference clock input frequency. Ten ranges can be selected by a front panel switch. Each range ($n = 1, 2, 3, \ldots 10$) divides the frequency by the factor $N = 2^{3n-1}$.

For a frequency of 50 MHz and n = 10, the separation between adjacent calibration marker pulses is 10.73 seconds. The marker pulses are phase locked to the reference frequency. The jitter amounts to a few picoseconds, regardless of the range.

The Digitizer's own reference clock output can be used for driving the Calibrator. The marker pulses thus generated are phase locked with all the Digitizer operations. Since the clock frequency is used for both purposes, any difference is thus eliminated. Any small drifts throughout the mission time are thus attributed to the interpolator and can be measured and correlated to the mission start. Calibrator Start and/or Stop output should be externally connected to the appropriate Tandem Interpolator input, depending on which mode of operation is chosen. An additional Calibrator (Sync.) output is also available for external monitoring or oscilloscope synchronization.

4. Dual Interpolation Principle

The counting of the 50 MHz reference clock frequency pulse resolves the time measurement only in 20 ns increments. Time intervals smaller than a clock period have been resolved in picoseconds by employing one or the other interpolation technique (16), (17), (18). In order to achieve 20 ps resolution, the time fractions smaller than the 20 ns clock pulse period can be stretched 1,000 times and digitized by the same clock frequency. However, the conversion of this kind would require up to 60 μs, eliminating thus the possibility of digitizing shorter start-stop time intervals.

This Digitizer employs a new dual interpolation technique (15) that greatly reduces the conversion time but still offers the same resolution of 19.53 ps at the clock frequency of 50 MHz. The conversion deadtime of 5.3 μs is the same for any event, and is more than ten times shorter than the single interpolation conversion time using the same clock frequency.

The principle of dual interpolation is shown in Fig. 3. Mission Start and Event Start pulse (line B) define the time

interval T_{ak} to be digitized. The points a and k at which the two events occur are uncorrelated to the Digitizer's clock pulses (line A). Upon the acceptance of the Mission Start pulse, the Event Busy signal (line C) is generated by the Interpolator. No other event can be accepted until the end of this signal.

Pulse T_1 (line F) is internally generated at the point b, which is coincident with the second clock pulse following the mission start. A second pulse, T_1, will be generated at point 1, coincident with the second clock pulse following the Event Start signal. Three intervals are thus defined, so that

$$T_{ak} = T_{ab} + T_{b1} - T_{k1} \tag{1}$$

T_{b1} is synchronized with the clock and thus can be expressed as a multiple of clock periods T_o. T_{ab} is first made shorter by a fixed delay $T_o/2$ and then expanded by a constant K_c in the "Coarse" Time Stretcher (line D) so that

$$T_{ab} - T_o/2 = (T_{be} - T_{cd})/K_c \tag{2}$$

T_{cd} is a residual time fraction between the end of "Coarse" conversion and the second following clock pulse. T_{be} is thus synchronized with the clock and can be expressed as a multiple of T_o. The excess fraction T_{cd} is expanded once again by a factor K_f in the "Fine" Time Stretcher (line G). $T_o/2$ is subtracted from T_{cd} in order to make the conversion shorter.

$$T_{cd} - T_o/2 = T_{ef}/K_f \tag{3}$$

By substituting (3) into (2) we obtain

$$T_{ab} = (1+1/K_c)T_o/2 + T_{be}/K_c - T_{ef}/K_cK_f \tag{4}$$

Similar procedure follows for the Event Start pulse:

$$T_{k1} = (1+1/K_c)T_o/2 + T_{1o}/K_c - T_{op}/K_cK_f \qquad (5)$$

and (1) becomes

$$T_{ak} = T_{b1} + (T_{be}-T_{1o})/K_c - (T_{ef}-T_{op})/K_cK_f \qquad (6)$$

It can be easily shown (15) that the minimum conversion time is required when $K_c = K_f = \sqrt{K}$, where the total time expansion factor K is the ratio of clock period T_o and the desired incremental resolution T_{oi}. In this case K = 1024 was selected, giving the optimum "coarse" and "fine" interpolation ratio of $K_c = K_f = 32$. The longest conversion time for either the "coarse" or "fine" stretcher takes about 48 clock pulses or 0.96 μs. Less than 2 μs is thus sufficient for a complete conversion of an event to obtain an incremental time resolution of $T_o/K = 20/1024 = 19.53$ ps.

Each event is thus defined only by the pulses T_1, T_2, and T_3 (lines F, K and H) that are precisely correlated with the clock frequency. These pulses are fed to the control Logic (See also Fig. 1), where the coincidence of T_1 and T_2 gives the "coarse" counter gate (line L) and the coincidence of T_2 and T_3 gives the "fine" counter gate (line M). The two gates enable the respective counters. N_{be} clock pulses are thus counted in the "fine" counter (lines T and V). N_{be} and N_{ef} are a constant that remains stored for the rest of the mission time in the "Coarse" and "Fine" Registers (Fig. 1).

During the Event Start conversion, T_1, T_2, and T_3 generate a new pair of "coarse" and "fine" counter gate pulses, that pass N_{1o} clock pulses to the "Coarse" Counter and N_{op} clock pulses to the "Fine" Counter (lines T and U).

In the meantime the main time interval T_{b1} (Eq. 1) was also digitized. The Auxiliary Counter gate (line N) was generated by the Control Logic at point b so that the first $N_{bg} = 256$

mission clock pulses were counted by the Auxiliary Counter (line P). At the point g the counting was switched to the Mission Counter (Mission Counter Gate, line R). N_{g1} counts (line S) were counted at the point 1 where the mission counting was again turned to the Auxiliary Counter. The equivalent of N_{bg} counts has been added to the Mission Counter before the point g so that at 1 the total of mission counts is $N_{b1} = N_{bg} + N_{g1}$. This number is then transferred into the Adder (Fig. 1). Dividing Eq. (1) by T_o we obtain

$$T_{ak}/T_o = N_{b1}+(N_{be}-N_{1o})/K-(N_{ef}-N_{op})/K^2 \qquad (7)$$

which can be transformed into

$$T_{ak}/T_o = N_{b1} + (\overline{N_{be}+N_{1o}})/K+(\overline{N}_{ef} +N_{op})/K^2-C \qquad (8)$$

$$C = 2 + 1/K-1/K^2$$

Eq. (8) gives the normalized time difference between the Event Start and Mission Start. Only summing operations are needed to compute the right hand side of Eq. (8) except for C, which is a system constant. In this manner most of the computing is done by simple counting. The same counters are thus used for the counting, arithmetic operations and data storage. Considerable saving in components and power requirements is thus achieved.

The summing of Eq. (8) is done in the Adder circuit (Fig. 1). The Mission Counter content N_{b1} is ready at the point 1 (Fig. 3). At this point the complement $\overline{N}_{be}$ of the content of "Coarse" Register has been already loaded into the "Coarse" Counter and the complement $\overline{N}_{ef}$ of the "Fine" Register into the "Fine" Counter.

The "coarse" conversion of Event Start results in N_{1o} "coarse" clock pulses (line T in Fig. 3) so that at the point o the "Coarse" Counter contains a sum of $\overline{N}_{be}+N_{1o}$ counts, a complement of which is then fed to the Adder. Likewise, N_{op} "fine" clock pulses (line V) are added to the preloaded $\overline{N}_{ef}$

counts in the "Fine" Counter and their sum $\overline{N}_{ef}+N_{op}$ also fed to the Adder. The sum of $N_{bl}+(\overline{\overline{N}_{be}+N_{lo}})/K+(\overline{N}_{ef}+N_{op})/K^2$ is computed in the Adder, and the total transferred first to the Event Register and then to the Buffer Register.

All this takes place during the counting of N_{lg} pulses in the Auxiliary Counter (line P). In addition, $\overline{N}_{be}$ and $\overline{N}_{ef}$ are loaded again into the "Coarse" and "Fine" Counter in order to prepare them for a future event, and the equivalent of N_{lg}=256 auxiliary counts added to the Mission Counter. At the point q, the Mission Counter resumes again the counting without the loss of any of the mission counts.

Each subsequent event is treated in the same way. Throughout the mission time, an event is always referred to the original Mission Start pulse. The time difference between any two recorded events therefore has to be computed externally. The constant C (Eq. 8) disappears automatically when the difference is computed. It has to be taken into account only if an event is referred to the Mission Start.

5. Discription of the Module Block Diagrams

5a. Clock and Calibrator Module (Fig. 6)

The module consists of three independent sections. The block diagram is shown in Fig. 7.

5aa. Clock. The clock reference frequency is either generated internally by the ICM MOE-10, 50 MHz crystal oscillator or supplied externally. The power to the internal oscillator is turned off when not in use in order to prevent any interference with the external clock. For the same reason, it is advisable to disconnect the external clock signal when the internal reference is used.

The two clock signals are reshaped in the OR gate G1. The leading edge differentiator (G2 and time delay D) produces uniform sharp clock spikes and is buffered in the amplifier-translators

A1 to A3. They provide the "coarse" and "fine" synchronization signal to the Tandem Stretcher Module and the clock to the logic modules through the rear panel connections. The respective propagation delays of these signals are matched and it is important that the lengths of the connecting cables are not altered.

An A4 provides a CLOCK OUT reference terminal on the front panel for monitoring or for driving the input of the calibrator circuit. Another A4 output drives the Frequency Divider circuit internally.

Once selected, the internal or external clock reference must not be interrupted throughout the mission.

5ab. Frequency Divider. Several frequencies can be derived from the basic 50 MHz reference and are available at a rear panel multiple pin connector. The Frequency Divider can be controlled by CAMAC commands. CAMAC Function and Subaddress Decoder respond only to two instructions, F(24) and F(26). The commands F(24)A(0)S1 and ZS1 disable (or initialize) the Divider by clearing the Clock Enable Latch. The enable command F(26)A(0)S1 sets the latch, enabling thus the first, divide-by-five ($f_o/5$) stage. The first following clock pulse starts the frequency division and also appears as the first pulse simultaneously at all the frequency outputs. In other words, all outputs start at the same instant and their phase relationship is thus precisely known during the whole mission.

The frequency output f_{11}=1 Hz in particular is shaped by G6 and A5 into fast, 5 ns wide spikes (MISSION START connector). If the mission is started by this signal, and the event recorded in the computer, any Divider generated frequency phase can be accurately determined in few tens of picoseconds.

The frequencies f_{12}=5 MHz and f_{13}=1.25 MHz are obtained by the $f_1/2$ and $f_1/8$ counter. Seven divide-by-five counters reduce f_1 to f_8=128 Hz and one more stage generates f_9=8 Hz and f_{11}=1 Hz. The outputs are square symmetrical pulses. The exception is f_{11}, which is reshaped by G7 to obtain 20 ns wide pulses. The shaping

by G6 and A5 was described earlier.

5ac. Calibrator. The circuits consist of a divide-by-four counter and ten divide-by-eight counters (Fig. 7). A ten position switch controls the gates G9 to G27, enabling the selection of 10 ranges. Any external reference frequency sources F_o of up to 100 MHz can be used. The $F_o/4$ stage toggles on the negative edge of the next clock pulse. The propagation delay of any subsequent divider thus does not change the phase between the clock frequency and the output of G8. Amplifier A6 translates the output into a double fast NIM signal suitable for driving the inputs of the Tandem Stretcher. The complement output is intended for monitoring or oscilloscope synchronization.

If the internal Digitizer clock reference f_o=50 MHz is used for driving the input of the Calibrator, the following time ranges can be generated (in multiples of the clock period $T_o=1/f_o$=20 ns):

Pos.	Range	n	2^n	$T=2^nT_o$
1.	A	2	4	80 ns
2.	B	5	32	640 ns
3.	C	8	256	5.120 μs
4.	D	11	2048	40.96 μs
5.	E	14	16384	327.68 μs
6.	F	17	131072	2.62144 ms
7.	G	20	1048576	20.97152 ms
8.	H	23	8388608	167.77126 ms
9.	I	26	67108864	1.34217728 s
10.	J	29	536870912	10.73741824 s
11.	K	32	4294967296	85.89934592 s

Range K is optional. It can be obtained by sacrificing one of the ten remaining ranges, since there are only ten selector positions available.

5b. Tandem Stretcher (Fig. 8)

This is the only analog module of the Digitizer. Dual interpolation technique is based on stretching small, less than one clock pulse long, time intervals by a factor of 1,024. The equivalent bandwidth of the time conversion is greatly increased by means of this method. The equivalent digitizing clock frequency is thus increased from 50 MHz to 50 GHz. Tunnel diodes are used in the most critical circuits (Fig. 9) such as Busy Latch and the two synchros.

The Busy Latch is set each time an event is accepted. The status of this latch can be monitored through the front panel BUSY output. The latch is cleared by the Logic Module each time an event is processed and transferred from the Event Register to the Buffer Register. As long as the Event Register is busy, no new event can be accepted.

The latch can be set by any of the signals passing the triple OR-gate G8. The status of the gates G5, G7 and G10 defines which signals will be accepted. G5 controls the mission start events. The mission can be started either by a front panel signal or by an internal CAMAC logic command, passing the OR-gate G2. OR-gate G3 must also be enabled internally by the logic circuits. A coincident Mission Enable front panel pulse is needed to start the mission, unless this condition is eliminated by a Logic command, which will premanently enable the OR-gate G4.

Similar logic applies for the Event Start and Start gate inputs (G6 and G7) and for the Event Stop and Stop Gate inputs. Each function requires a different set of commands, as given in the Specification Section.

Busy Latch opens the gate G11 after a delay of $T_o/2=10$ ns. A constant current source is turned on in the Coarse Stretcher, charging a capacitor with a current I_o. The charging stops when G11 is closed again when the "Coarse" Synchro circuit latched on the leading edge of the second clock pulse following the event that had set the latch.

"Coarse" Synchro is a dual tunnel diode latch. The first clock pulse that passes G14 after the Busy latch is set, locks itself up through the OR-gate G13. Gate G16 is then opened after a delay D1 of about 10 ns, making sure that the leading edge of the second clock pulse latches the synchro through the gate G15. The closing of G11 stops the charging in the "Coarse" Stretcher, and starts the discharge of the memory capacitor by a constant current which is exactly 32 times smaller than the charging current. The "coarse" time conversion is over when the capacitor charge returns to the initial level. A tunnel diode discriminator fires at this point, opening the gate G18 in "Fine" Synchro and starting 10 ns later, the next charging process in the Fine Stretcher. The "Fine" Synchro and Stretcher are identical to the "coarse" ones. Two clock pulses later, the "Fine" Synchro latches and G12 is closed, stopping the charging. The Fine Stretcher discriminator fires when the memory capacitor is discharged to the initial level. The "coarse" time converison is thus defined by the signals T1 and T2, and the "fine" conversion by T2 and T3.

These three signals are brought to the Logic Module and along with the clock signal, used for the digitizing of the event. The few interconnections minimize the interference between the modules.

The Stretcher module contains a CAMAC decoder that recognizes four commands. Two commands are used for turning on and off the module power (for stand-by operation), and one each for the testing and mission start.

5c. Logic 1 Module (Fig. 10)

Logic circuits as shown in the general block diagram (Fig. 1) are distributed among three logic modules. Basic logic functions performed by the Logic 1 Module are shown in Figs. 11, 12, and 13. Control logic (Fig. 11) digitizes an event as defined by the pulses T1, T2 and T3 from the Tandem Stretcher. The first event after the mission clear is interpreted as the mission start

event by setting the Mision Latch. Gate G4 is open to pass the clock to the Mission Counter (Fig. 13). This clock train cannot be interrupted until the end of the entire mission.

T1 sets also the "Coarse" Latch that passes the "coarse" clock pulse train to the "Coarse" Counter (Fig. 12). The arrival of T2 some time later sets the "Fine" Latch, which in turn stops the "coarse" pulse train. At the same time, the "fine" pulse train is started (G9) and counted by the "Fine" Counter (Fig. 12).

The arrival of T3 sets the End-of-Conversion Latch, closing G8. The trailing edge of T3 passes G10, and closes G9, and the "fine" counting.

Each event also generates the Auxiliary Counter Start pulse by opening G7 and closing it by T2. This pulse switches the mission train pulses to the Auxiliary Counter (Fig. 13).

The Mission Counter stays idle during the first 256 counts (5.12 μs). During this period the "coarse" and "fine" counting is completed, some arithmetic operations performed, and data is transferred into the Event Register. The strobe for loading is generated by the gate G4 at the 128th count of the Auxiliary Counter. This pulse is also used as a "carry" signal, adding through the OR-gate G5, an equivalent of 256 missing pulses to the binary No. 19 of the Mission Counter. This occurs immediately after the data is transferred from the Mission Counter into the Event Register, but well before the counting is resumed.

After 256 counts have been completed, G3 and G2 switch the counting from the Auxiliary to the Mission Counter. Not a single mission train pulse is lost and the mission time counting continues as though the counting was not interrupted. The size of the Mission Counter 1 section is the same as the Auxiliary Counter's so that for each 256 mission counts, a carry is generated by G6. This pulse is used as a clock pulse to advance the second part of the Mission Counter through G5.

At the end of auxiliary counting the signal from G2 is passed through the OR-gate G1 to the Logic Module 3, where the transfer of data from the Event Register to the Buffer Register is initiated

and an event clear signal is returned to enable the circuits for the new event.

The first event defining the mission start needs to be recorded for the rest of the mission. The "Coarse" train is counted first and the "Fine" train next. The counting of each takes less than a microsecond. The Auxiliary Counter strobe is generated at 2.56 μs after the counting has started. The Strobe Latch is set at this point, generating the strobe to the Coarse Register and Fine Register (Fig. 12). The Fine Register is then strobed into the Fine Register and the complement of the Coarse Counter is strobed into the Coarse Register. Both registers hold this data until the end of the mission.

The Event Clear pulse, generated at the end of the processing at the mission start event, enables the Digitizer for the acceptance of a new event. It is used also for strobing the content of the Coarse Register into the Coarse Counter and the content of the Fine Register into the Fine Counter. The counters are thus prepared for the new event, where the new "coarse" train will be added to the preset Coarse Register content. Likewise, the new "fine" train will be added to the complement of the Fine Register. The addition, corresponding to Eq. 8, is thus performed by counting.

The summing operation is completed in the Adder (Fig. 13). The lowest 12 data bits are then ready for storage in the first part of the Event Register and the carry (bit 13) is added to the second part of the Event Register. Prior to this, the Mission Counter was stopped for the new event, and its data transferred into the Buffer Register.

Presumably, the Range Counter and the Enable Counter were loaded by CAMAC commands before the start of the mission. When T1 sets the "Coarse" Latch (Fig. 11), the Range Latch is also set and G5 opened to pass clock pulses, to the Range Counter (Fig. 12). Gate G4 is open when the number of clock pulses brings the Range Counter to zero, and the signal used to enable the stop input of the Tandem Stretcher. Also, the Gate G1 is closed and G3 opened so that the clock pulses are diverted to the Enable

Counter. After the preset number of clock pulses, the counter is brought to zero and G4 is closed. No stop event can be accepted after G4 closes. The GATE OUT signal of the same duration as Stop Enabled, is available at the front panel for monitoring or for the control of the constant fraction discriminator in the optical receiver.

The RC/EC Register is also loaded each time along with the loading of the Range and Enable Counters. During the normal ranging, each stop event requires a new pair of data to be loaded into the Counters. If the new information does not arrive in time before the new event, both the Range and the Event Counters are automatically loaded by the last data left in the RC/EC Register. At very high rates of start-stop events, it may not be feasible to reload the counter each time. The circuit will then automatically generate the same stop time range and stop aperture after each start event.

The purpose of the Event Enable Latch (Fig. 11) is to recognize the mission start event from all subsequent events during the mission. G2 opens at the end of the first T1 pulse, setting the Event Enable Latch for the rest of the Mission. The next and all subsequent T1's will pass G2 and G3, resulting in an Event Busy output for all events except the mission start.

5d. Logic 2 Module (Fig. 14)

This module contains the major part of the Mission Counter, Event Register, and Buffer Register (Fig. 13). Also, it contains the circuits for LED display of the remaining 48 bits of data in three selectable 16-bit groups, and the data readout to the CAMAC Controller.

5e. Logic 3 Module (Fig. 15)

This module contains the circuits for the interface of the Digitizer with the CAMAC controller. A number of CAMAC commands

are decoded and stored to control the Digitizer's operations. Typically, an accepted command is stored by setting a latch, that in turn controls the appropriate module via the rear panel interconnection system (Fig. 16).

The complete list of CAMAC functions and their explanation is given in a separate section. In addition, manual control and the external control (other than CAMAC) circuits are also in this module.

6. Digitizer Test Results

Two identical Space-Borne Time Event Digitizers have been completed and tested. The results confirm the expectation for inherent thermal stability, resolution and linearity of time measurement. A built-in Calibrator proved to be a very useful tool for the evaluation of the Digitizer's performance as well as for a quick visual inspection and check-up of many functions, that would otherwise require lengthy computer programming.

Driven by the internal clock reference, the calibrator generates accurately separated time markers that are phase locked with the internal function of the Digitizer. Very small thermal and other drifts attributal to the time interpolation can thus be observed and measured. In Fig. 17 the calibrator was set to divide the 50 MHz clock frequency by 2^8, generating continuous marker pulses separated by 5.12 μs. Mission was started by one of the marker pulses, and each subsequent marker pulse is then accepted and digitized as a valid event. Each event is immediately stored into a 256-channel section of an external digital memory and the Digitizer cleared for another event. The Event Busy is thus equal to the minimum event processing time of about 5.3 μs. In Fig. 17 the marker pulses appear each 5.12 μs. Therefore, only every second marker pulse is accepted as a valid event.

Only the 8 least significant bits of each event were stored in the 256-channel memory. Although the events are actually separated by 10.12 μs, they overlap because the higher order bits are ignored. The resulting distributions are shown in Figs. 18 and 19. The symmetrical peak in Fig. 18 shows that the total phase

jitter of all the recorded events in respect to the mission start is less than 0.1 channel (2 ps). Fig. 19 was taken under the same conditions except that all the recorded events were shifted one half of a channel (10 ps) by a variable delay line after the mission started.

Measurements in Fig. 20 were taken with externally supplied continuous calibrating marker pulses separated by 32.768 μs. They were uncorrelated with the Digitizer's internal clock. The Digitizer was initialized after every second event. Thus every second marker pulse started a new mission, followed by one event exactly 32.768 μs apart. Both mission start and the event were stored in the 2048 channel digital memory. The starts were evenly distributed over 1024 channels. All events, however, were sorted into one single peak, because the time difference between each mission start, and the event that follows, is 32.768 μs.

The events in the peak (Fig. 21) are the accumulation of all the mission starts distributed over 1024 channels. The expanded portion of the peak area is shown in the figure. The two adjacent channels next to the peak contain about a third of events each, indicating the total time jitter of about 10 ps.

Temperature change has negligible effect in time ranges of several seconds. Assuming that the Digitizer's 50 MHz reference clock is ideal, i.e. has zero frequency drift regardless of the temperature and aging, the timing error throughout the mission can then be attributed to the interpolator drift only. Such a condition is closely met when the Digitizer is tested by the Calibrator driven by the same clock standard. When both the Digitizer and the Calibrator use the same reference, the frequency drift is automatically compensated. The Digitizer was set-up under the same conditions used for obtaining Fig. 17. The mission was started and ran continually for 22 days. Mission time and crate temperature were taken several times a day. The results are plotted in Fig. 22. A consistent thermal coefficient of about +20 ps/°C is measured as the room temperature was measured throughout each day (data was not taken during the night or over the weekends).

During the first half of the mission a positive, aging like, drift of several channels occured. However, after about 20 mission days, the drift reversed to return eventually at the end to the initial point. Since other parameters (line voltage, power regulator voltages) were not taken, the drift was not well understood. Since the total 22-day cycle (for a normalized temperature) amounts to about 120 ps, the subject was not considered further.

7. Operating Instructions

The SBET Digitizer is shipped in a Standard Engineering Co. CAMAC Minicrate (Fig. 4). Eight CAMAC stations are occupied by the Digitizer modules. The stations No. 24 and 25 are reserved for a CAMAC Controller Module, not supplied with the Digitizer. The Controller can communicate only with the Calibrator, Tandem Stretcher and Logic 3 Module.

The operation of the Digitizer is either remote (via Controller) or fully manual (only on an event by event basis). In the former case, make sure that proper station numbers N are used in the software.

Preliminary inspection

Check visually for any damage in shipment. All modules and the power supply should be fully in place with front panel thumbscrews tightened. Rear panel interconnections should be in place and the cable connector cap tight. Should any module need to be removed and put on an extender, all the extension cables must be of the same length. Several such cables are shipped with the instrument.

Upon turning the power on, proper voltage readings should be obtained at the test points on the front panel of the power supply. Verify by an oscilloscope that 50 MHz CLOCK OUT signal is present when the switch on the Clock module is in INT position. Connect CLOCK OUT to Calibrator INPUT by a short cable. Calibrator

START OUT and STOP OUT marker pulse rates vary according to the position of the RANGE SWITCH from 12.5 MHz to 0.1 Hz.

Connect START OUT to MISSION START and set RANGE SWITCH to position 9, approximate rate 1 Hz. Put both DISPLAY switches on ON. Set the rear panel switch on Logic 3 Module to TEST. One Calibrator pulse will be interpreted as Mission Start (the BUFFER light goes on) and the next pulse arriving about one second later is treated as an event. Mission clear follows the event so that the next Calibrator pulse will cause a new mission start, and the corresponding new data is displayed. In order to ease the visual inspection, the RANGE position No. 10 can be selected. Each event thus remains displayed 10 seconds and can be inspected easier.

By setting the Logic 3 Module rear panel switch to ENA position, the Digitizer operates as described before, except that the mission does not get cleared. Therefore, each new pulse at the Mission input is treated as an event and its time always referred to the original mission start. Only two events can be accepted, as indicated by the BUFFER and EVENT lights. Each time the BUFFER CLEAR is depressed, the BUFFER light goes off, indicating that the event is cleared. Upon the release of the push button, the contents of the Event Register is transferred into the Buffer Register. The EVENT light then goes off and the BUFFER light on.

The input to the Digitizer is free again and the next Calibrator pulse will be accepted as a new event and stored in the Event Register.

For testing purposes, the Buffer Register can be cleared automatically by shorting the two pins of the small connector sticking out of the Logic Module 3 rear panel connector. Each event it thus dumped as soon as the Register is ready. The rate of accepted events then equals the Calibrator pulse rate. Since an event is always referred to the mission start, the small change in the least significant bits indicates the Dual Stretcher drift due to the temperature change

8. Summary of Specifications

Clock and Calibrator Module

Internal Clock Oscillator: ICM MOE-10

Frequency	50.000000 MHz
Calibration	±1 ppm (25°C)
Stability (-10°C to 60°C)	±0.0005%
External Clock Input (50 ohm terminated)	0.8 V (Fast NIM)
Clock Output (50 ohm terminated)	0.8 V (Fast NIM)
CK1, CK2 (Rear panel interconnections)	Clock to Dual Stretcher
CK3 (Rear panel interconnection)	Clock to Logic Module No. 1.

Frequency Divider Outputs (Rear panel connector, Fig. 7):

f_{12}	(pin 2)	5 MHz (TTL)
f_{13}	(pin 3)	1.25 MHz (TTL)
f_{8}	(pin 4)	128 Hz (TTL)
f_{9}	(pin 5)	64 Hz (TTL)
f_{10}	(pin 6)	8 Hz (TTL)
f_{11}	(pin 7)	1 Hz (TTL)
f_{11S}	(pin 1)	1 Hz (TTL)

The width of f_{11S} is 20 ns. All other outputs have 50% duty cycle.

Mission Start Output (front panel):

Rise Time	0.8 ns
Width	5 ns
Amplitude (50 ohm terminated)	0.8 V

Calibrator:

Reference Clock Input (50 ohm terminated)	0.8 V
Start and Stop Output (Dual bridged NIM)	0.8 V (each)
Sync. Output (int. impedance 10 ohm)	0.3 V (open)

CAMAC Commands:

N_c: Clock and Calibrator Module station number.
N_cF(24)A(0)S1: Disable Frequency Divider and Mission Start Output.
N_cF(26)A(0)S1: Enable Frequency Divider and Mission Start Output.
ZS1: Initialize (Disable Frequency Divider and Mission Start Output).

Tandem Stretcher Module:

Front Panel:

Mission Start Input (50 ohm terminated)	0.8 V
Mission Enable Input (50 ohm terminated)	0.8 V
Event Start Input (50 ohm terminated)	0.8 V
Event Start Gate Input (50 ohm terminated)	0.8 V
Event Stop Input (50 ohm terminated)	0.8 V
Event Stop Gate Input (50 ohm terminated)	0.8 V
Busy Output (TTL, 1.2 kohm int. impedance)	3 V

Align coarse: Front panel potentiometer
Align fine: Front panel potentiometer

Note: Adjust only when following the alignment procedure.

N light (LED) is on only if the module is addressed by the controller.

Rear panel:

CK1, CK2: Reference clock from Clock Module
T1, T2, T3: Outputs to control logic in Logic 1 Module.

CAMAC Commands:

N_I:	Tandem Stretcher Module station number
N_IF(24)A(0)S1:	Reset "Power On" latch.
N_IF(25)A(0):	Enable Mission Start Input.
N_IF(25)A(0)S1:	Start Mission (CAMAC option)
N_IF(26)A(0)S1:	Set "Power On" latch.
N_IF(27)A(0):	Test "Power On" latch status
ZS1:	Initialize (Set "Power On" latch).
X:	Command Accepted (X=1 for all valid commands).
Q:	Response (Q=1) for all valid commands except when "Power On" latch status is tested by F(27)A(0).

Note: When "Power On" latch is reset, the module stand-by power requirement is 0.2 W).

Logic 1 Module

Gate Out (Front panel connector): Level: TTL; Width: 0 to 81.92 μs (CAMAC programmable in 4095, 20 ns wide steps); Delay: 0 to 335.54252 ms in 16777126, 20 ns wide steps.
Display: LED'S display the lowest 16 bits of Buffer Register.
Display on/off switch: (Does not affect the operation of the Digitizer).
CK3: 50 MHz clock from Clock Module (rear panel).
T1, T2, T3: Event signals from Tandem Stretcher (rear panel).
Note: Logic 1 Module does not respond to any direct CAMAC command.

Logic 2 Module:

Display: 16 LED display 3 groups of Buffer Register bits according to the Group Display switch.

Group Display Switch:

Pos. A: Displays bits 17 to 32
Pos. B: Displays bits 33 to 48
Pos. C: Displays bits 49 to 59 and stop tag (bit No. 60)

Display on/off switch does not affect the operation of the Digitizer.

Note: Logic 2 Module does not respond to any direct CAMAC command.

Logic 3 Module:

Front panel:

N (LED) Responds for every address from controller.
BUFFER (LED) On when Buffer Register contains data.
EVENT (LED) On when Event Register contains data.
BUFFER CLEAR: Front panel push-button clears the Buffer Register only.

Rear panel:

EXT. CLEAR connector: $\overline{\text{TTL}}$, (20 ns min.) pusle clears Buffer Register only.
MISSION CLEAR connector: $\overline{\text{TTL}}$ (20 ns min.) pulse clears mission and all registers.

Rear Panel Mode Switch:

ENA position: Keeps Mission Start input continually enabled all the time. Any valid Mission Start pulse will be accepted and interpreted as an event.

TEST position: Keeps Mission Start input enabled as above. In addition, the Digitizer is set in the start-stop mode of operation, i.e. the first pulse starts the mission, the next one is interpreted as a stop event followed by an automatic mission clear. The third and the fourth pulse is a new mission start - event stop pair, etc. The Digitizer thus works as a stop watch.

Note: Make sure that for all other modes of Digitizer operation that the swtich is set in the neutral (center) position.

CAMAC Commands:

N_L	Logic 3 Module station number.
$N_L F(0)A(0)$ $N_L F(2)A(0)$	Read data D1-D16 on Dataway lines R1 to R16.
$N_L F(0)A(1)$ $N_L F(2)A(1)$	Read data D17-D32 on Dataway lines R1 to R16.
$N_L F(0)A(2)$ $N_L F(2)A(2)$	Read data D33-D48 on Dataway lines R1 to R16.
$N_L F(0)A(3)$ $N_L F(2)A(3)$	Read data D49-D59 and Stop Tag D60 on Dataway lines R1 to R12.
$N_L F(2)A(3)S2$	Clear LAM Latch and enable Buffer Register to accept a new event.
$N_L F(2)A(7)S2$	Clear Mission (Clock and Tandem Stretcher Modules are not affected).
ZS2	Initialize all modules (Clear Mission).
$N_L F(8)A(0)$	Test LAM (returns Q=1 if LAM Latch is set, i.e. if Buffer Register is ready and Lam Enable Latch is set).
$N_L F(10)A(0)S2$	Clear LAM Latch and enable Buffer Register to accept a new event.
$N_L F(16)A(0)S1$	Load Range/Enable Register (using W1 to W24 Write Bus-lines).
$N_L F(16)A(0)S2$	Load Range Counter (using W1 to W24 Write Bus-lines).

$N_L F(16)A(1)S1$	Load Range/Enable Register (using W1 to W24 Write Bus-lines).
$N_L F(16)A(1)S2$	Load Enable Counter (using W1 to W12 Write Bus-lines).
$N_L F(24)A(0)S2$	Disable LAM Enable Latch.
$N_L F(26)A(0)S2$	Enable LAM Enable Latch.
$N_L F(24)A(1)S1$	Disable Time Readout Latch.
$N_L F(26)A(1)S1$	Enable Time Readout Latch (Enables Mission Start input in Tandem Stretcher).
$N_L F(24)A(2)S1$	Activate Mission Enable input (in Tandem Stretcher Module).
$N_L F(26)A(2)S1$	Deactivate Mission Start Latch.
$N_L F(24)A(3)S1$	Disable Mission Start Latch.
$N_L F(26)A(3)S1$	Enable Mission Start Latch (Mission Start input in Tandem Stretcher is enabled for acceptance only one pulse).
$N_L F(24)A(4)S1$	Activate Start Gate input (in Tandem Stretcher Module).
$N_L F(26)A(4)S1$	Deactivate Start Gate input (i.e. Start Gate signal in Tandem Stretcher is not needed for Event Start acceptance).
$N_L F(24)A(5)S1$	Disable Event Start Latch
$N_L F(26)A(5)S1$	Enable Event Start Latch (Start input in Tandem Stretcher is enabled for acceptance of only one start pulse).
$N_L F(24)A(6)S1$	Activate Stop Gate input (in Tandem Stretcher Module).
$N_L F(26)A(6)S1$	Deactivate Stop Gate input (i.e. Stop Gate signal in Tandem Stretcher is not needed for Event Stop acceptance).
$N_L F(24)A(7)S1$	Disable Event Stop Latch.
$N_L F(26)A(7)S1$	Enable Event Stop Latch (Stop input in Tandem Stretcher is enabled for acceptance of only one stop pulse). Stop event accepted in this way will not be tagged. Stop tag will be added only to the Stop Input event that is accepted within the aperture time when internally generated by the Enable Counter.
CS2	Clear LAM, Tandem Stretcher and Buffer and Event Register. Mission counting is not affected.
X	Command accepted (X=0 for all valid commands).
Q	Response (Q=0 for all valid commands except when LAM latch status is tested by F(8)A(0)).

Power Requirements:

Clock and Calibrator Module

	Clock		Calibrator	Frequency Divider	Total
+6V	0.12A	0.72W	0.11A 0.66W	0.13A 0.78W	1.44W
-6V			0.11A 0.66W		1.38W
+24V			12mA 0.29W		0.29W
-24V			26mS 0.62W		0.62W
					3.73W

Tandem Stretcher Module

+6V	0.21A	1.26W	20mA	0.18W
-6V	0.16A	0.96W		
+24V	57mA	1.36W	0.6mA	0.014W
-24V	64mA	1.53W	0.6mA	0.014W
Full power:		5.11W	Stand-by power:	0.20W

Logic 1 Module:

+6V	0.65A	3.9W

Logic 2 Module:

+6V	0.17A	1.02W

Logic 3 Module:

+6V	0.13A	0.78W
Total Logic Power:		5.7W

Note: Above data are valid when all LED displays are switched off.

Summary of Power Requirements (without LED display):

Full power	14.5W
Stand-by power (with Calibrator on)	9.63W
Stand-by power (with Calibrator off)	7.34W

Note: Power can be further reduced by approximately 20% if +5V line is used for the logic circuits instead of the standard CAMAC +6V line. The power required by the CAMAC crate controller and the power supply itself is not included.

9. Conclusions

The tests confirmed the Digitizer's excellent stabilty for time interval measurement, due to the employment of the same interpolator for both the start and stop events. The new tandem interpolation technique greatly reduces the event conversion deadtime. The fixed event deadtime is 5.3 μs, which is substantially lower than the originally requested 10 μs deadtime. The incremental resolution of 19.53 ns was not affected by this deadtime reduction.

Further improvements can be made in the next generation of the Digitizer. The event deadtime can be reduced to 1 μs by changes in the logic circuits, again without any reduction in time resolution (no change in the reference clock frequency will be required). Minimum one way ranging distance would thus be reduced to 150 meters. The incremental resolution can also be improved by modifying the tandem interpolator. For instance, it is calculated that a fourfold increase of incremental resolution (to 4.88 ps) can be achieved with conversion times still under 2 μs. By increasing the 50 MHz clock frequency the deadtime can be proportionately decreased. The power consumption would be increased because of the faster circuits required.

With the changes indicated in the preceeding paragraph, a very low deadtime digitizer, capable of resolving time intervals

and phase differences in the femtosecond range, can be designed by utilizing the same principle.

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12. Figure Captions

Fig. 1. General block diagram of the High Precision Event-Timing Digitizer.

Fig. 2. General timing diagram.

Fig. 3. Tandem interpolation timing diagram.

Fig. 4. Front view of the Digitizer.

Fig. 5. Partial rear view of the Digitizer.

Fig. 6a. Clock and Calibrator Module front view.

Fig. 6b. Clock and Calibrator Module rear view.

Fig. 7. Clock, Frequency Divider and Calibrator block diagram.

Fig. 8a. Tandem Stretcher Module front view.

Fig. 8b. Tandem Stretcher Module rear view.

Fig. 9. Tandem Stretcher block diagram.

Fig. 10a. Logic 1 Module front view.

Fig. 10b. Logic 1 Module rear view.

Fig. 11. Logic 1 Module; Control Logic block diagram.

Fig. 12. Logic 1 Module; Range and Enable Counter, Fine Counter, Fine Register, Coarse Counter and Coarse Register block diagram.

Fig. 13. Logic 1 Module; Auxiliary Counter, Mission Counter 1, Adder, Event Register 1, Buffer Register 1 and LED Display block diagram.

Fig. 13. Logic 2 Module; Mission Counter 2, Event Register 2, Buffer Register 2 and LED Display block diagram.

Fig. 14a. Logic 2 Module front view.

Fig. 14b. Logic 2 Module rear view.

Fig. 15a. Logic 3 Module front view.

Fig. 15b. Logic 3 Module rear view.

Fig. 16. Logic 3 Module; CAMAC Logic and Command Memory block diagram.

Fig. 17. Section of mission time during which a continuous 10.24 μs event rate was digitized.

Fig. 18. Distribution of overlapped events from Fig. 17. Each out of approximately 3000 events, accumulated in the peak, is actually separated by 10.24 μs.

Fig. 19. Distribution of overlapped events from Fig. 17, which have been delayed by half a channel (10 ps) with respect to the mission start. Separation between each event is actually 10.24 μs.

Fig. 20. Random phase distribution of mission starts obtained by 32.768 μs input event rate.

Fig. 21. Distribution of random 32.768 μs time intervals in relation to mission start.

Fig. 22. Tandem Stretcher drift as a function of ambient temperature during a 21-day mission.

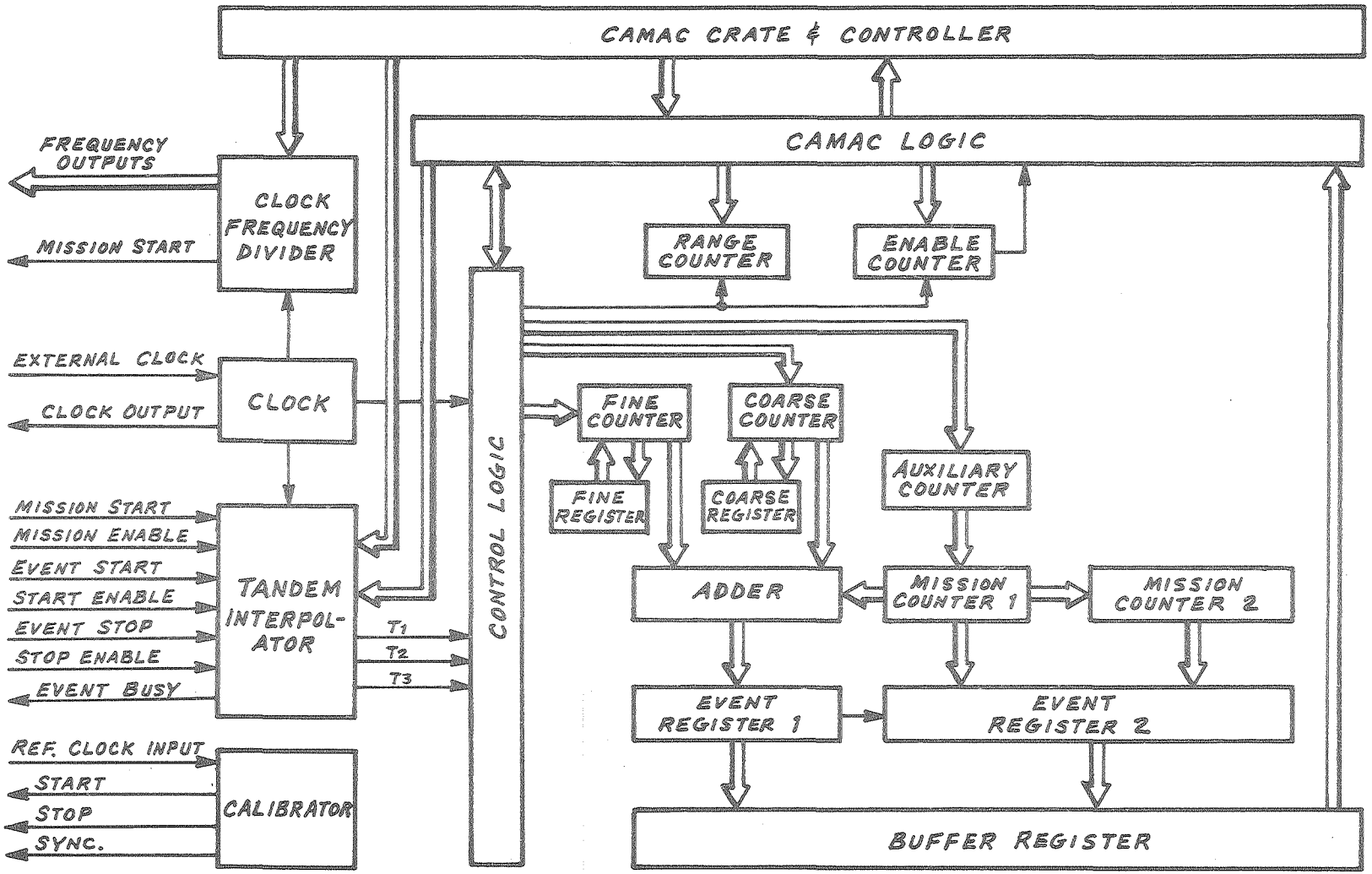
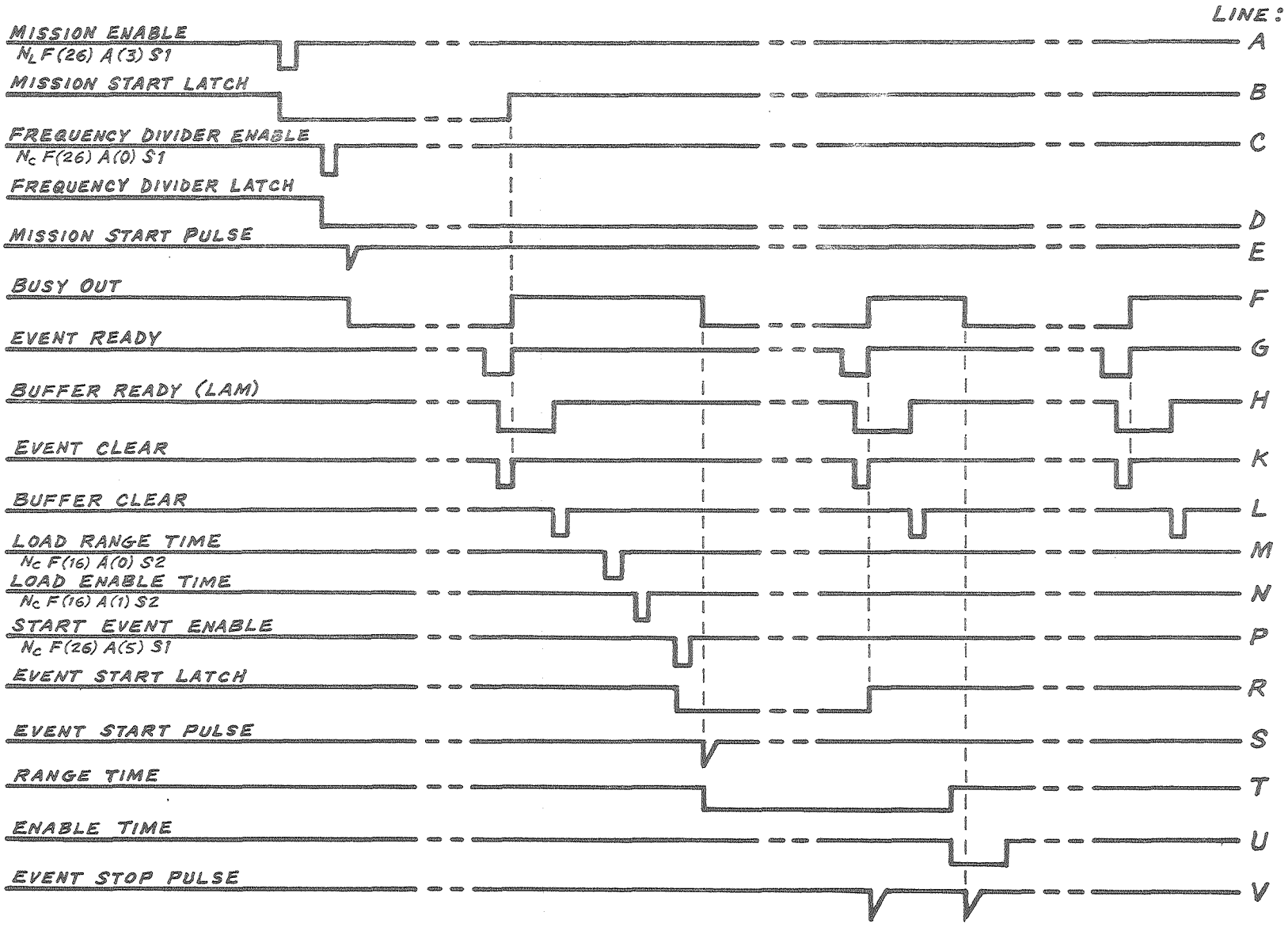


Fig. 1

XBL 791-7778



XBL 791-7779

Fig. 2

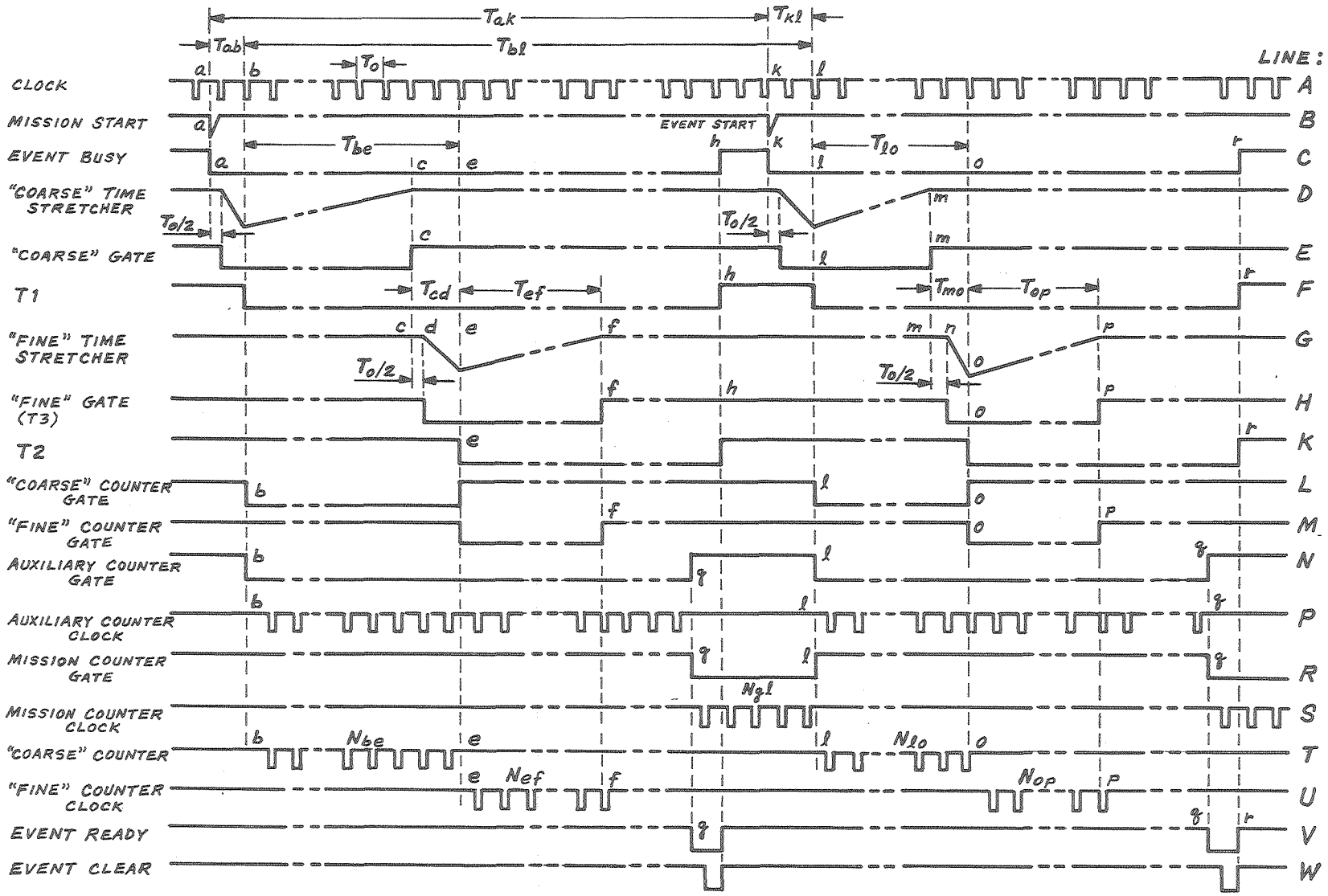
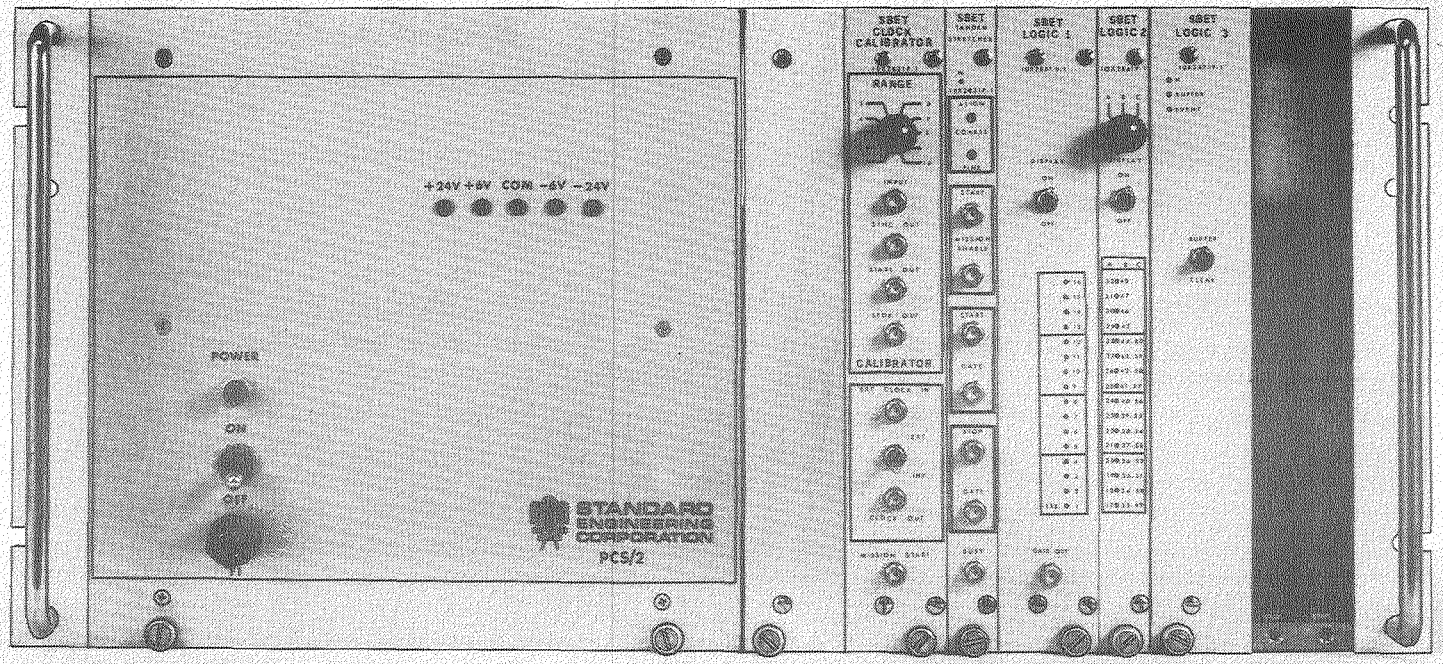


Fig. 3

XBL 791-7780



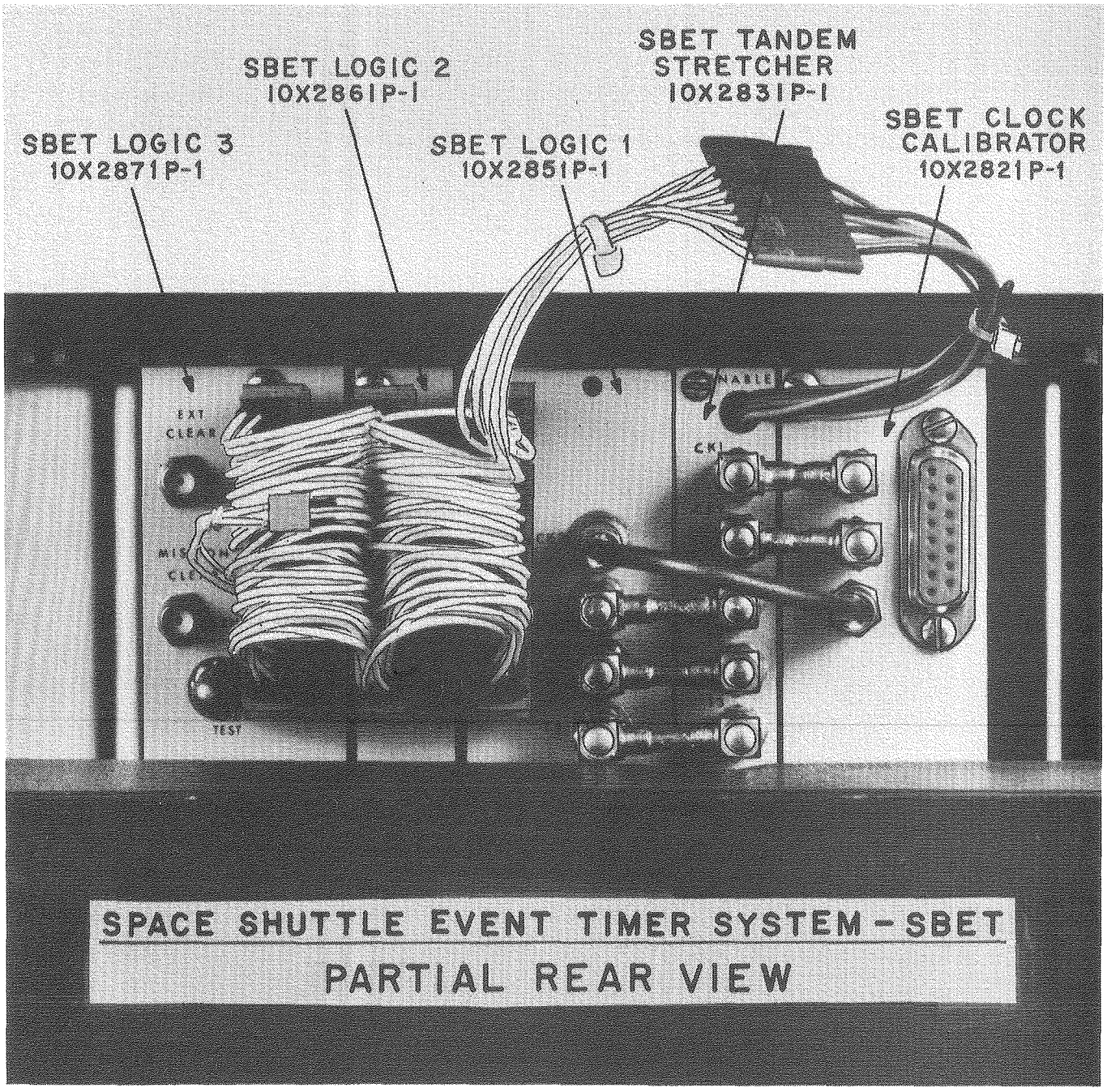
XBB 780-15609

SPACE SHUTTLE EVENT TIMER SYSTEM - SBET

FRONT VIEW

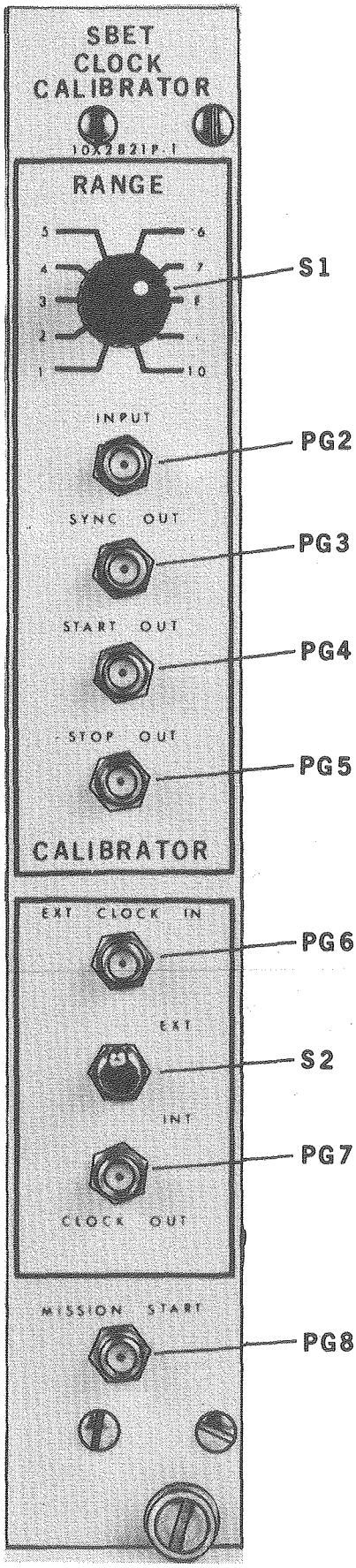
Fig. 4

XBB 780-15609

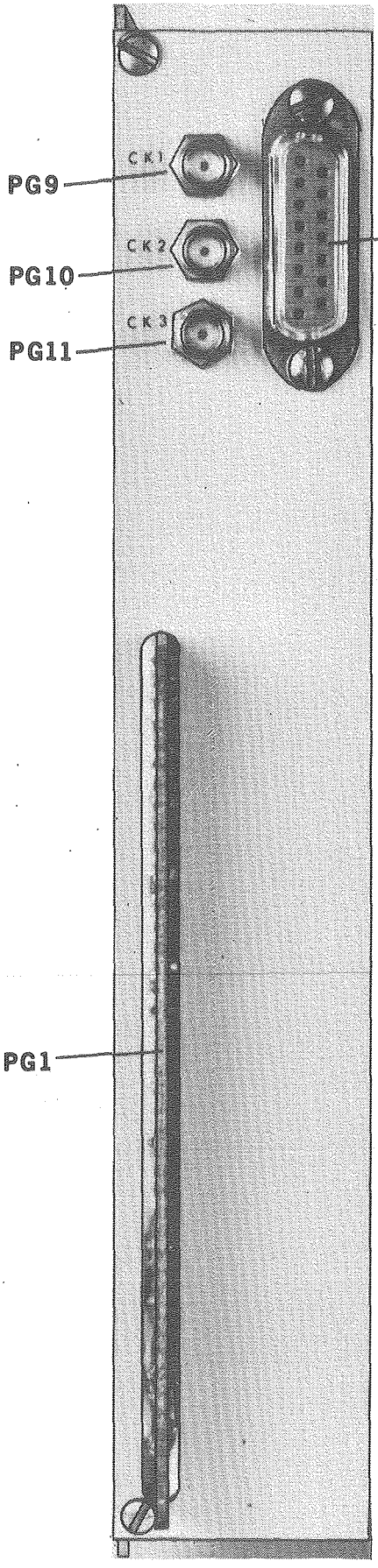


XBB 780-15605A

Fig. 5



FRONT PANEL



REAR PANEL

XBB 780-15614A

Fig. 6a

Fig. 6b

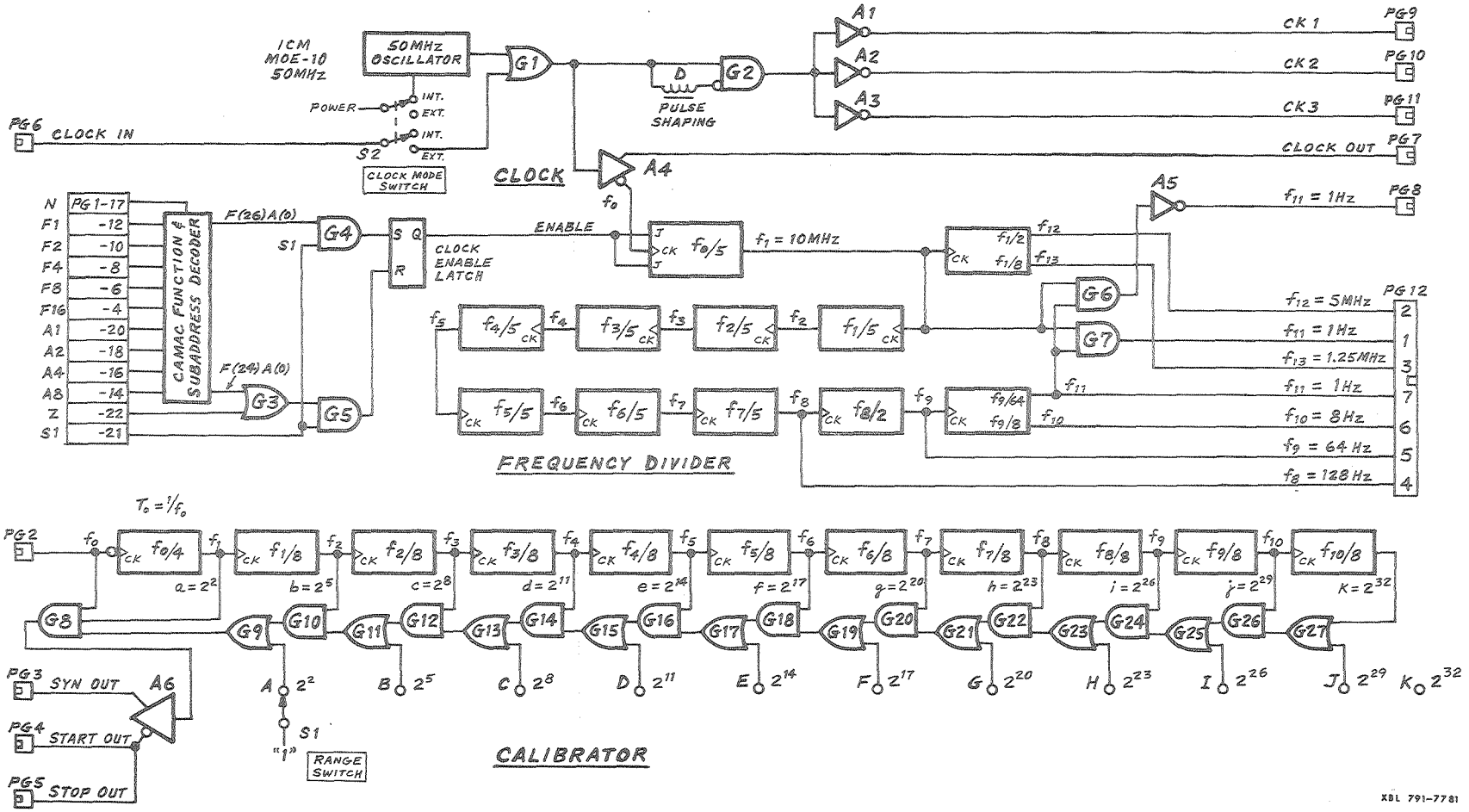
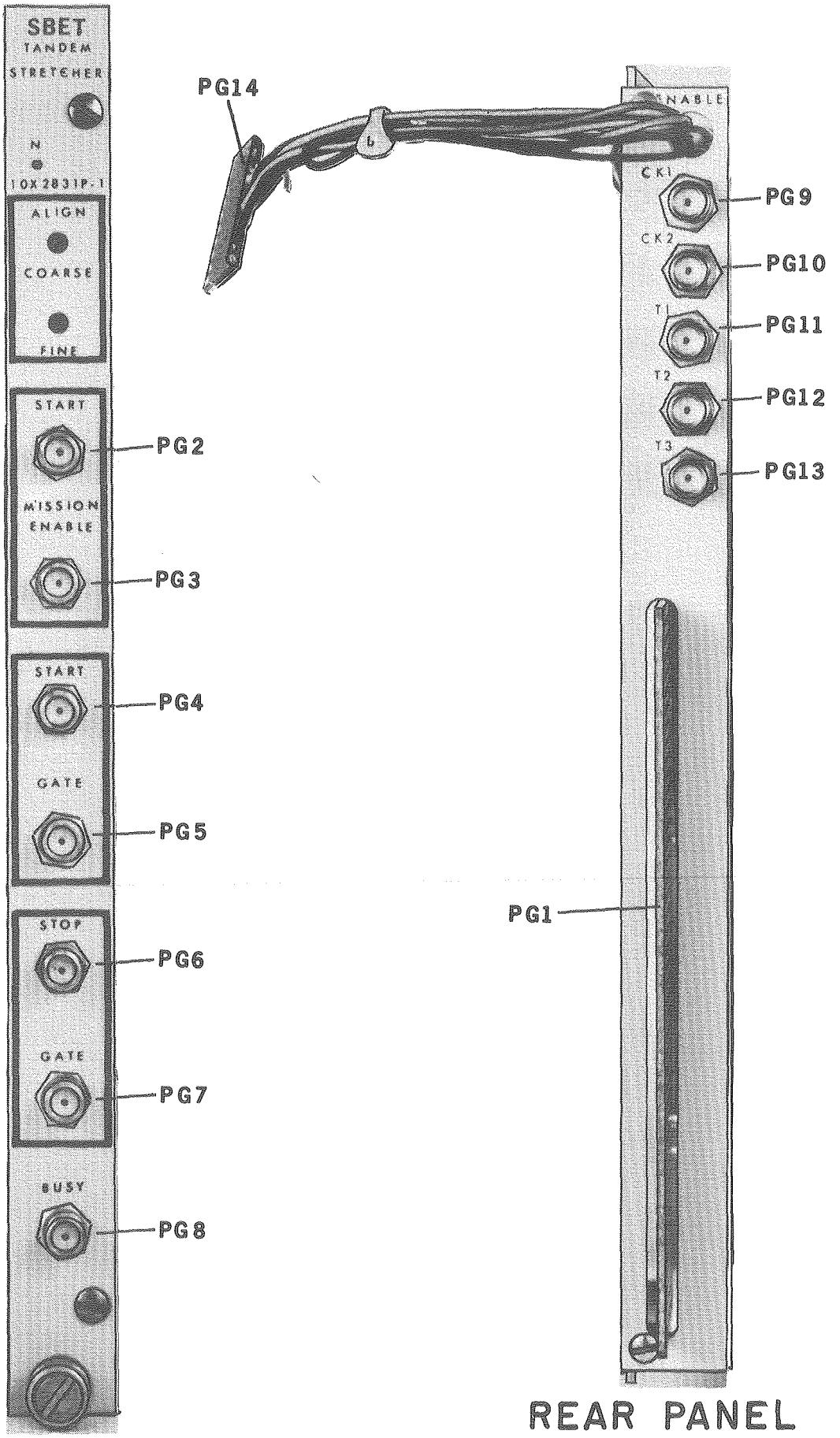

ICM MOE-10 50MHz
50MHz OSCILLATOR
G1
G2
D
PULSE SHAPING
A1
A2
A3
CK 1
CK 2
CK 3
CLOCK OUT
PG9
PG10
PG11
PG7
PG6 CLOCK IN
POWER
INT.
EXT.
INT.
EXT.
S2
CLOCK MODE SWITCH
CLOCK
A4
f_0
A5
f_{11} = 1Hz
PG8
N PG 1-17
F1 -12
F2 -10
F4 -8
F8 -6
F16 -4
A1 -20
A2 -18
A4 -16
A8 -14
Z -22
S1 -21
CAMAC FUNCTION & SUBADDRESS DECODER
F(26)A(0)
F(24)A(0)
S1
G3
G4
G5
S Q
R
CLOCK ENABLE LATCH
ENABLE
$f_0/5$
f_1 = 10MHz
$f_{1/2}$
$f_{1/8}$
f_{12}
f_{13}
G6
G7
f_{12} = 5MHz
f_{11} = 1Hz
f_{13} = 1.25MHz
f_{11} = 1Hz
f_{10} = 8Hz
f_9 = 64 Hz
f_8 = 128 Hz
PG12
f_5 $f_{4/5}$ f_4 $f_{3/5}$ f_3 $f_{2/5}$ f_2 $f_{1/5}$
$f_{5/5}$ f_6 $f_{6/5}$ f_7 $f_{7/5}$ f_8 $f_{8/2}$ f_9 $f_{9/64}$ $f_{9/8}$ f_{10}
FREQUENCY DIVIDER
$T_0 = 1/f_0$
PG2
$f_{0/4}$ $f_{1/8}$ $f_{2/8}$ $f_{3/8}$ $f_{4/8}$ $f_{5/8}$ $f_{6/8}$ $f_{7/8}$ $f_{8/8}$ $f_{9/8}$ $f_{10/8}$
$a = 2^2$ $b = 2^5$ $c = 2^8$ $d = 2^{11}$ $e = 2^{14}$ $f = 2^{17}$ $g = 2^{20}$ $h = 2^{23}$ $i = 2^{26}$ $j = 2^{29}$ $K = 2^{32}$
G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 G25 G26 G27
PG3 SYN OUT
A6
PG4 START OUT
PG5 STOP OUT
A 2^2
B 2^5
C 2^8
D 2^{11}
E 2^{14}
F 2^{17}
G 2^{20}
H 2^{23}
I 2^{26}
J 2^{29}
K 2^{32}
S1
"1"
RANGE SWITCH
CALIBRATOR
XBL 791-7781

Fig. 7



FRONT PANEL

REAR PANEL

XBB 780-15613A

Fig. 8a

Fig. 8b

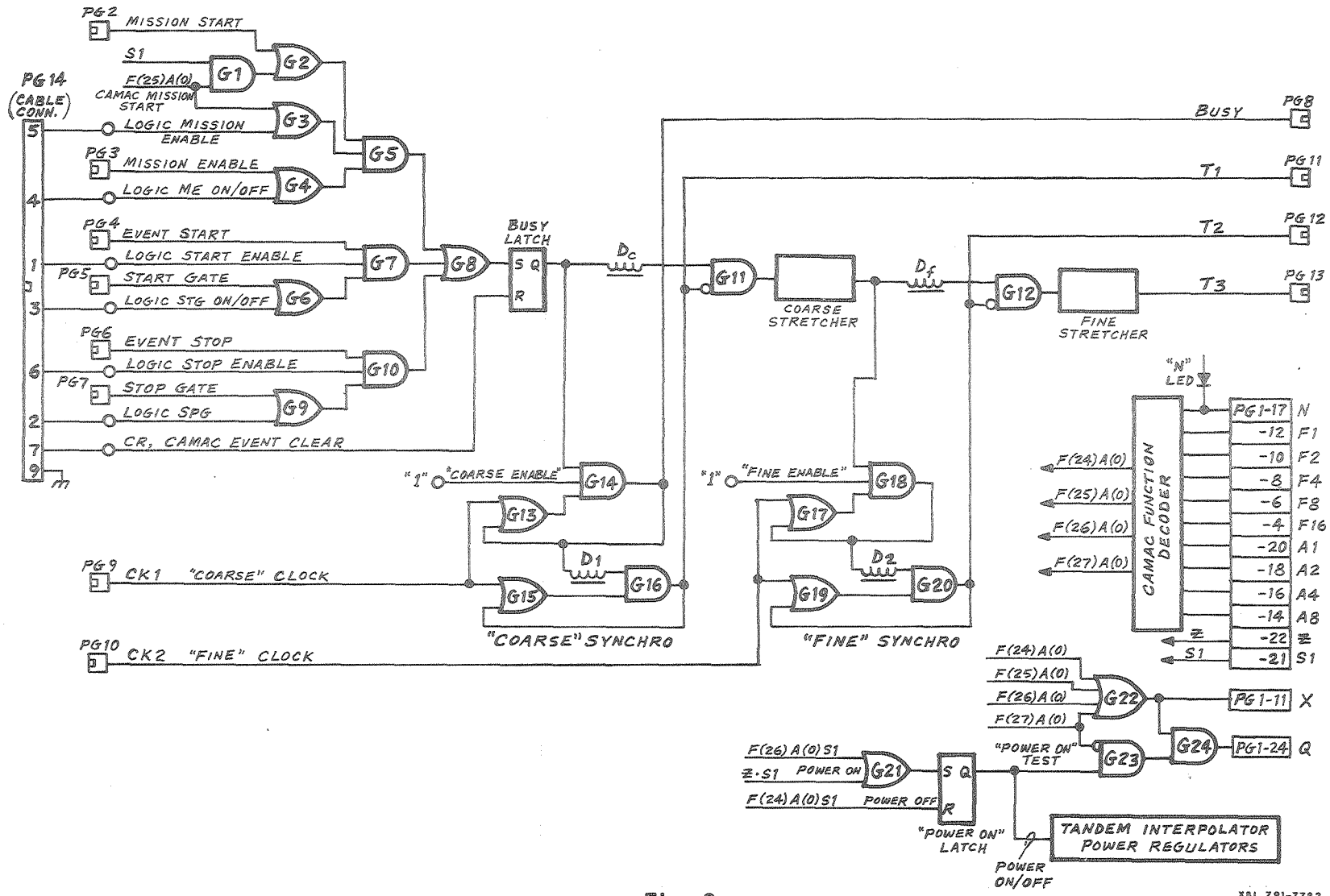
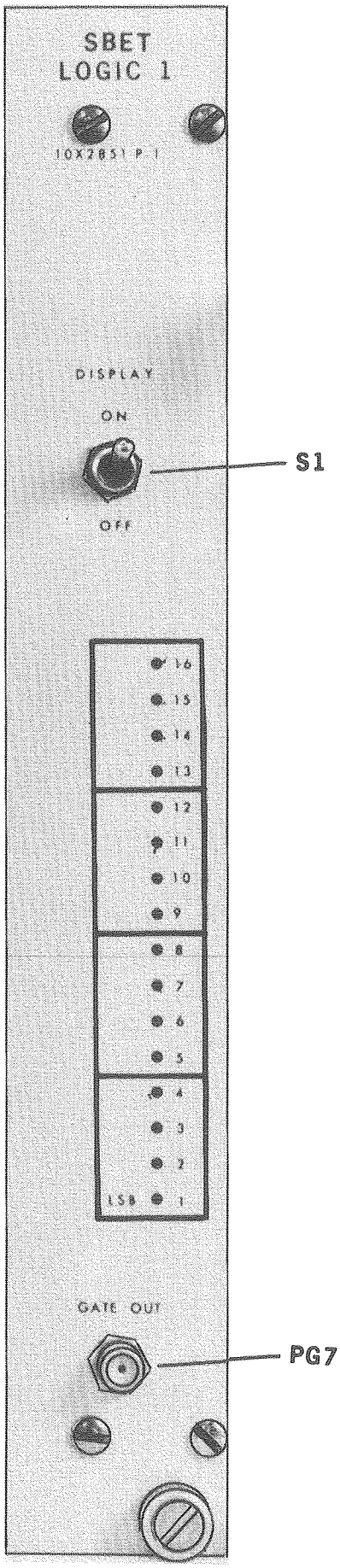


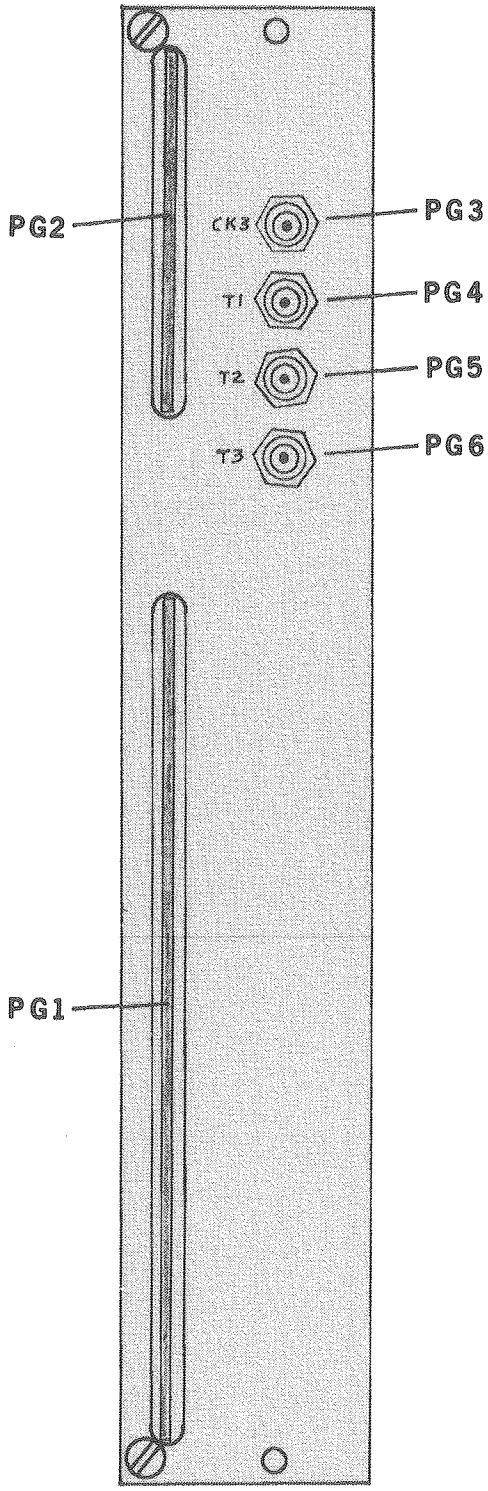
Fig. 9

XBL 791-7782



FRONT PANEL

Fig. 10a



REAR PANEL

XBB 780-15623A

Fig. 10b

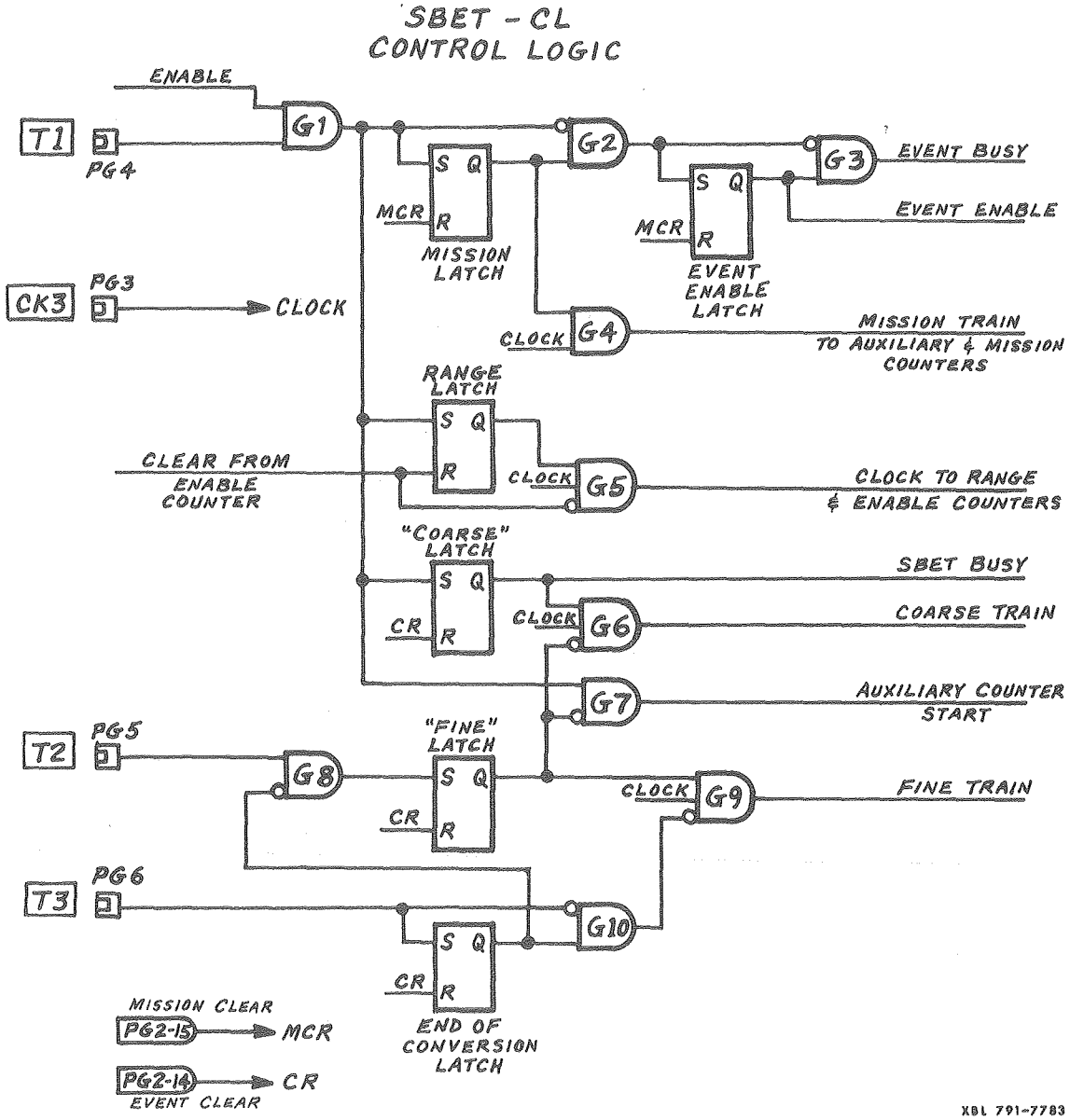

SBET - CL
CONTROL LOGIC
ENABLE
T1
PG4
G1
G2
G3
EVENT BUSY
EVENT ENABLE
S Q
MCR
R
MISSION LATCH
EVENT ENABLE LATCH
CK3
PG3
CLOCK
G4
MISSION TRAIN TO AUXILIARY & MISSION COUNTERS
RANGE LATCH
CLEAR FROM ENABLE COUNTER
G5
CLOCK TO RANGE & ENABLE COUNTERS
"COARSE" LATCH
SBET BUSY
CR
G6
COARSE TRAIN
G7
AUXILIARY COUNTER START
T2
PG5
G8
"FINE" LATCH
G9
FINE TRAIN
T3
PG6
G10
END OF CONVERSION LATCH
MISSION CLEAR
PG2-15
PG2-14
EVENT CLEAR
XBL 791-7783

Fig. 11

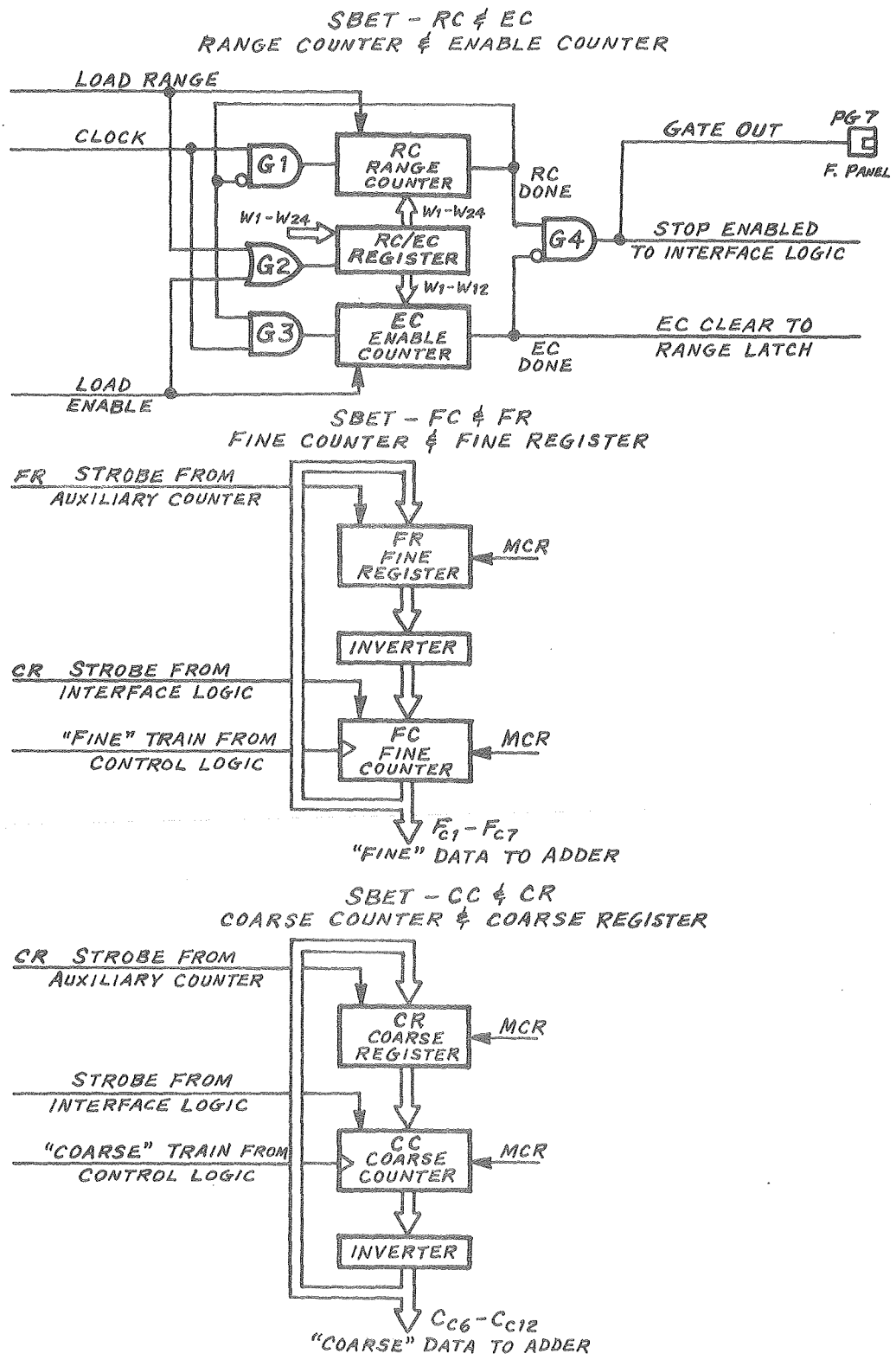
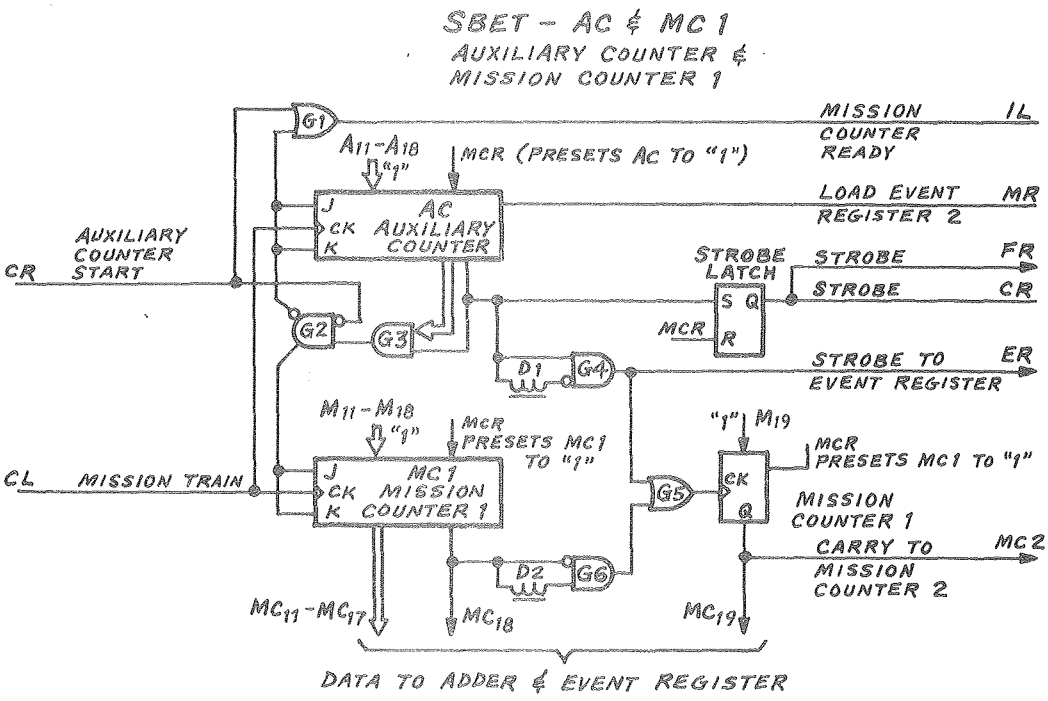

SBET - RC & EC
RANGE COUNTER & ENABLE COUNTER
LOAD RANGE
CLOCK
G1
RC RANGE COUNTER
RC DONE
GATE OUT
PG 7
F. PANEL
W1-W24
W1-W24
RC/EC REGISTER
G4
STOP ENABLED TO INTERFACE LOGIC
G2
W1-W12
G3
EC ENABLE COUNTER
EC DONE
EC CLEAR TO RANGE LATCH
LOAD ENABLE
SBET - FC & FR
FINE COUNTER & FINE REGISTER
FR STROBE FROM AUXILIARY COUNTER
FR FINE REGISTER
MCR
INVERTER
CR STROBE FROM INTERFACE LOGIC
"FINE" TRAIN FROM CONTROL LOGIC
FC FINE COUNTER
MCR
$F_{C1}-F_{C7}$
"FINE" DATA TO ADDER
SBET - CC & CR
COARSE COUNTER & COARSE REGISTER
CR STROBE FROM AUXILIARY COUNTER
CR COARSE REGISTER
MCR
STROBE FROM INTERFACE LOGIC
"COARSE" TRAIN FROM CONTROL LOGIC
CC COARSE COUNTER
MCR
INVERTER
$C_{C6}-C_{C12}$
"COARSE" DATA TO ADDER
XBL 791-7784

Fig. 12


SBET - AC & MC 1
AUXILIARY COUNTER & MISSION COUNTER 1
MISSION COUNTER READY
IL
LOAD EVENT REGISTER 2
MR
AUXILIARY COUNTER START
CR
STROBE LATCH
STROBE
FR
STROBE
CR
MCR
STROBE TO EVENT REGISTER
ER
A11-A18
"1"
MCR (PRESETS AC TO "1")
AC AUXILIARY COUNTER
G1
G2
G3
G4
D1
M11-M18
"1"
MCR PRESETS MC1 TO "1"
"1"
M19
MCR PRESETS MC1 TO "1"
CL
MISSION TRAIN
MC1 MISSION COUNTER 1
G5
G6
D2
MISSION COUNTER 1
CARRY TO MISSION COUNTER 2
MC2
MC11-MC17
MC18
MC19
DATA TO ADDER & EVENT REGISTER

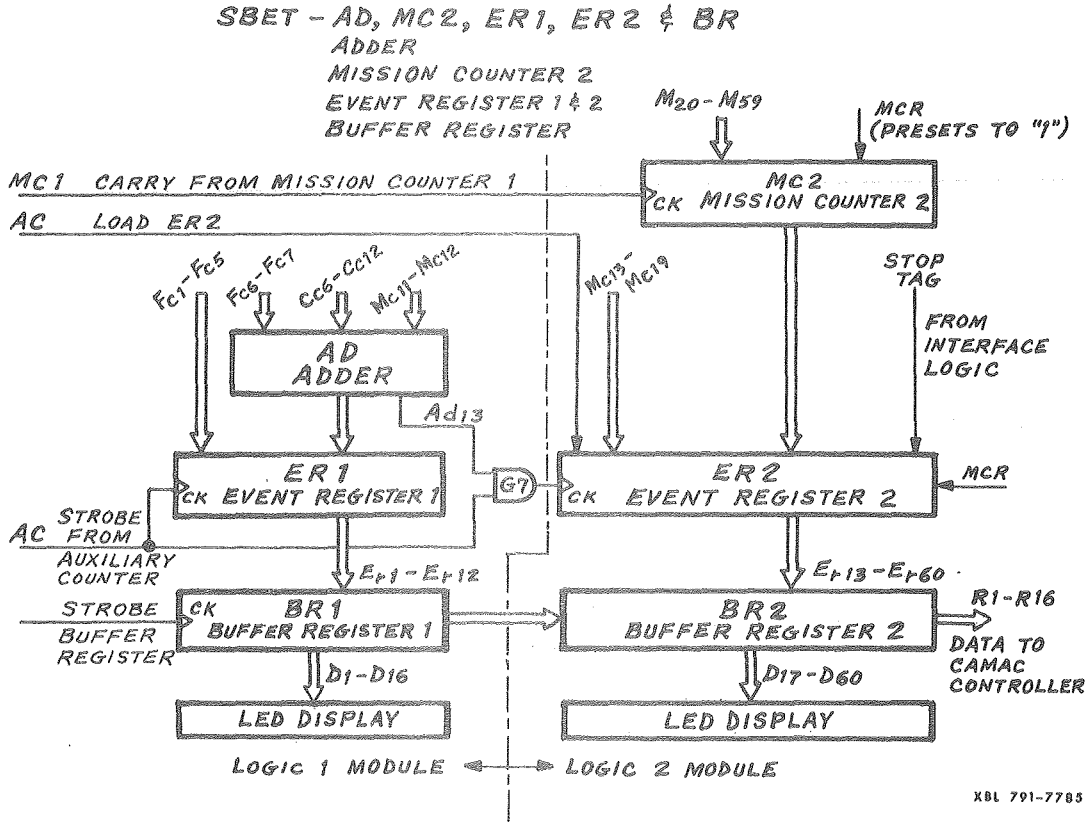
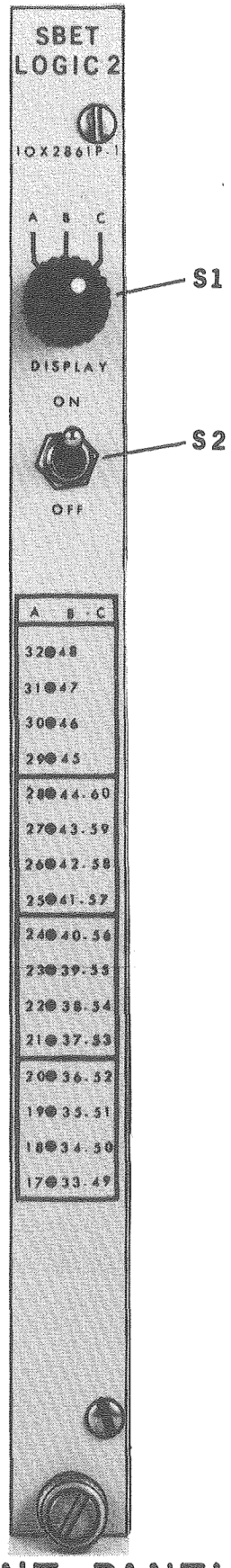
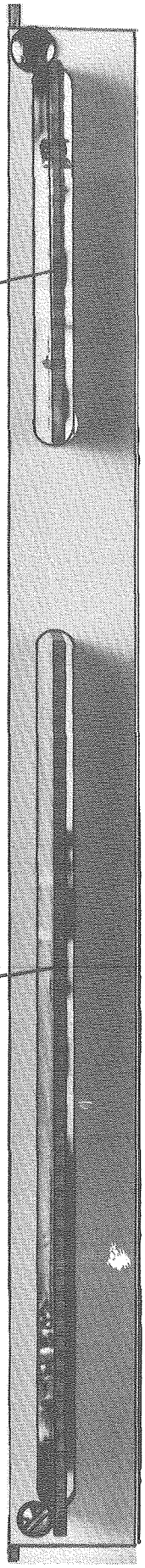

SBET - AD, MC2, ER1, ER2 & BR
ADDER
MISSION COUNTER 2
EVENT REGISTER 1 & 2
BUFFER REGISTER
M20-M59
MCR (PRESETS TO "1")
MC1 CARRY FROM MISSION COUNTER 1
MC2 MISSION COUNTER 2
AC LOAD ER2
FC1-FC5
FC6-FC7
CC6-CC12
MC11-MC12
MC13-MC19
STOP TAG
FROM INTERFACE LOGIC
AD ADDER
AD13
ER1 EVENT REGISTER 1
G7
ER2 EVENT REGISTER 2
MCR
AC STROBE FROM AUXILIARY COUNTER
E1-E12
E13-E60
STROBE BUFFER REGISTER
BR1 BUFFER REGISTER 1
BR2 BUFFER REGISTER 2
R1-R16
DATA TO CAMAC CONTROLLER
D1-D16
D17-D60
LED DISPLAY
LED DISPLAY
LOGIC 1 MODULE
LOGIC 2 MODULE
XBL 791-7785

Fig. 13



FRONT PANEL

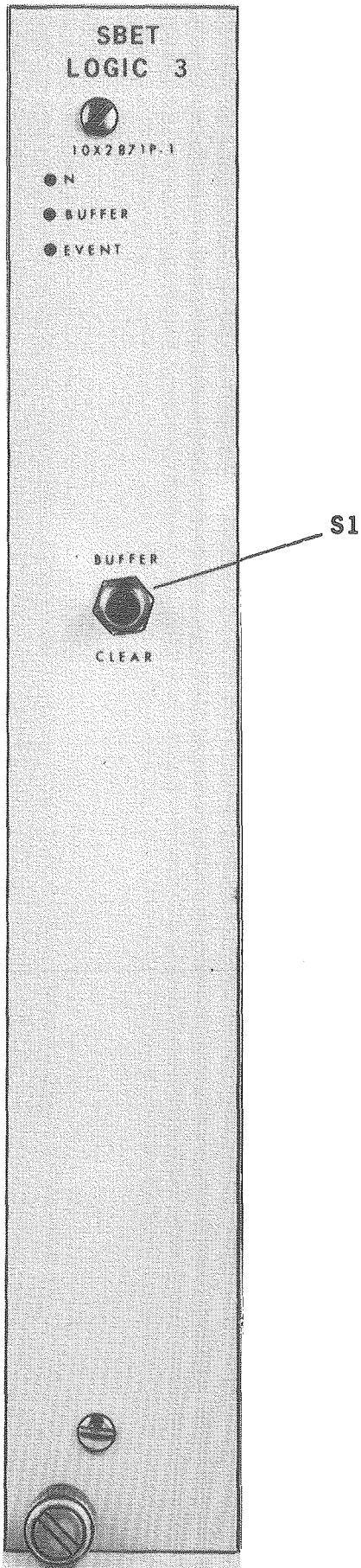
Fig. 14a



REAR PANEL

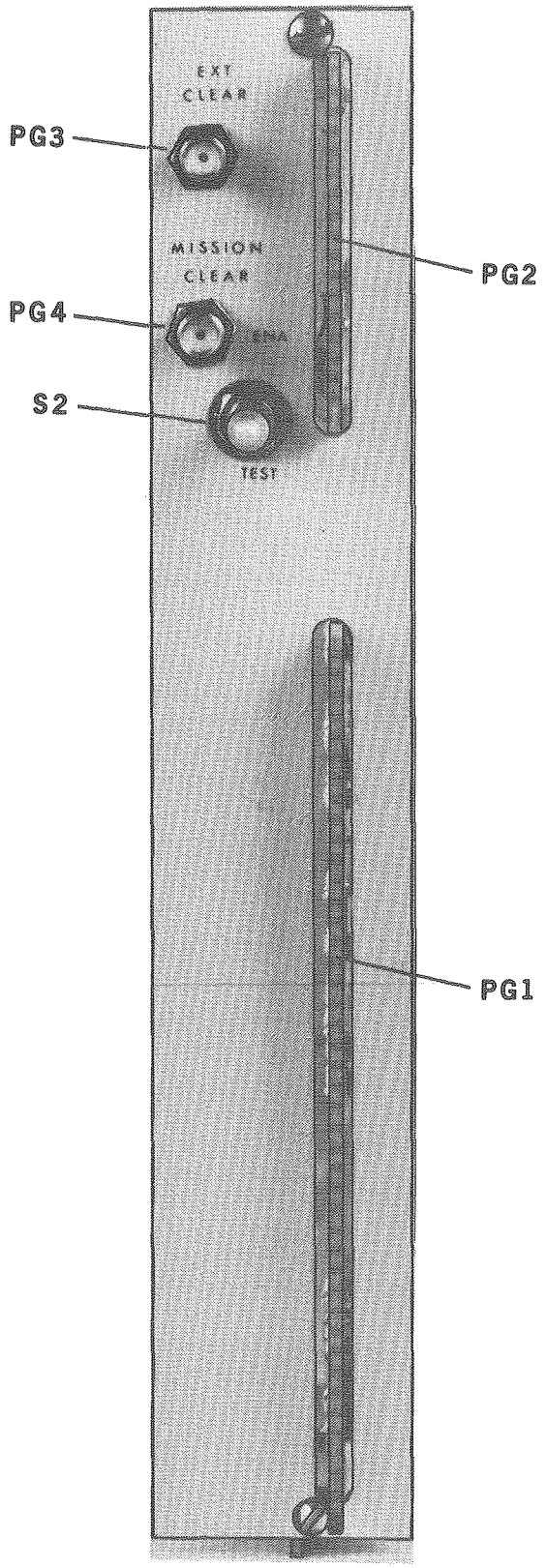
XBB 780-15617A

Fig. 14b



FRONT PANEL

Fig. 15a



REAR PANEL

XBB 780-15628A

Fig. 15b

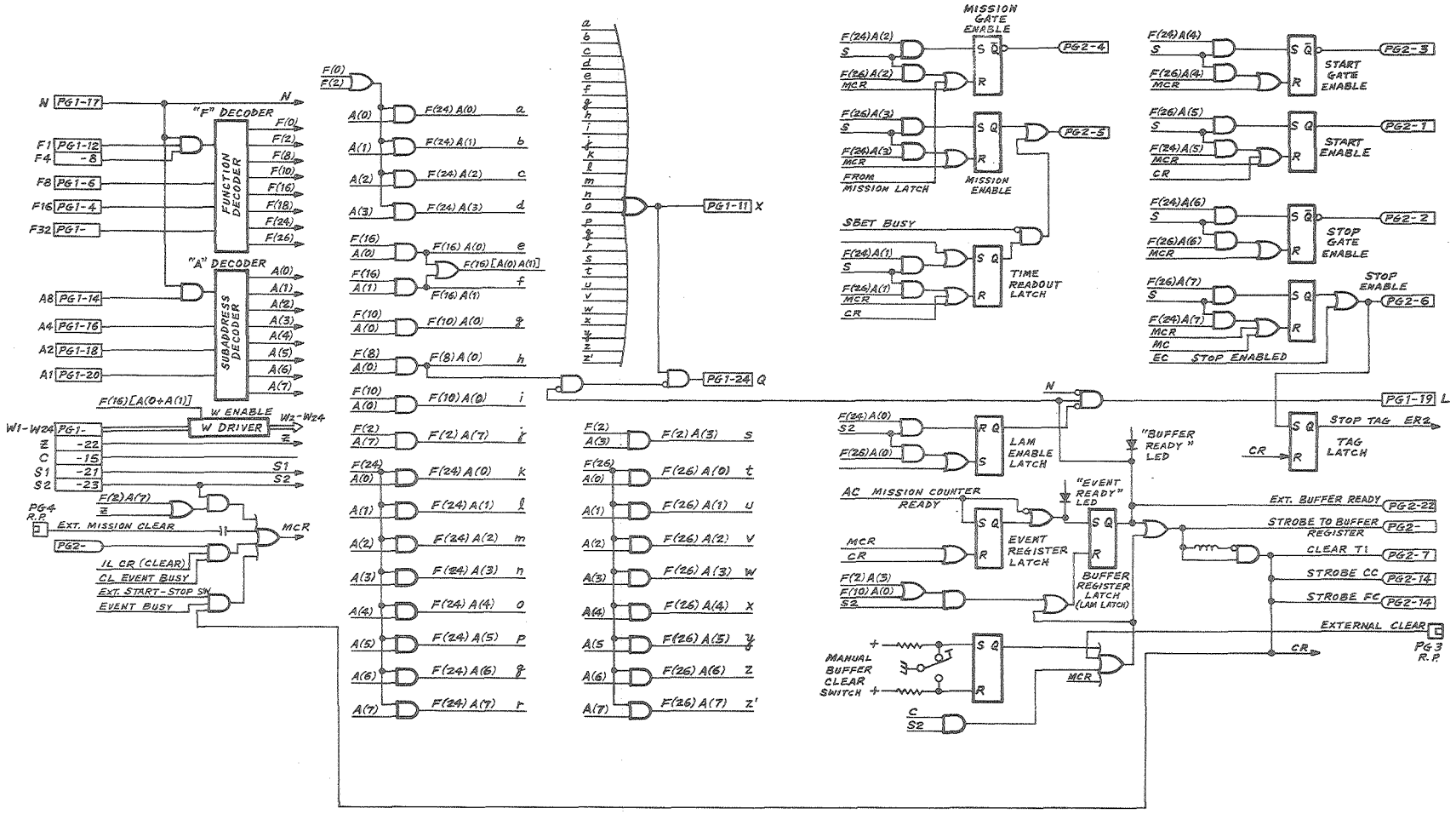


Fig. 16

XBL 791-7786

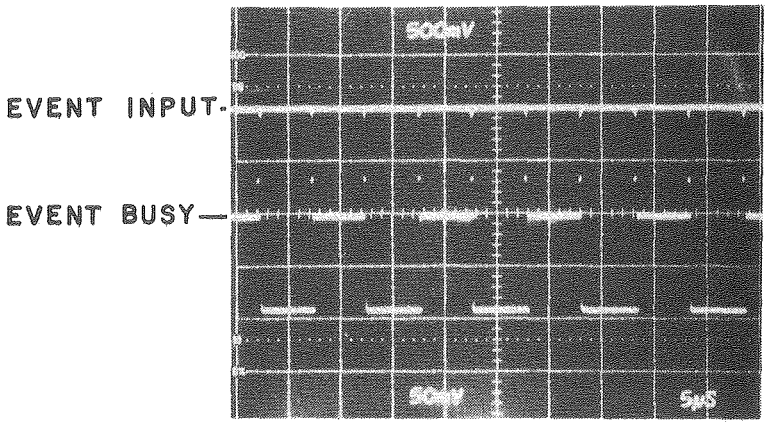


Fig. 17

SECTION OF MISSION TIME DIGITIZING A CONTINUOUS 10.24μs EVENT RATE FROM CALIBRATOR.

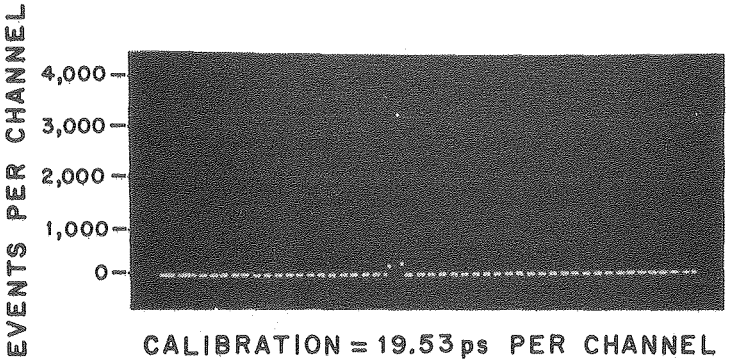


Fig. 18

DISTRIBUTION OF OVERLAPPED EVENTS FROM Fig. 17. EACH EVENT IS ACTUALLY SEPARATED BY 10.24μs.

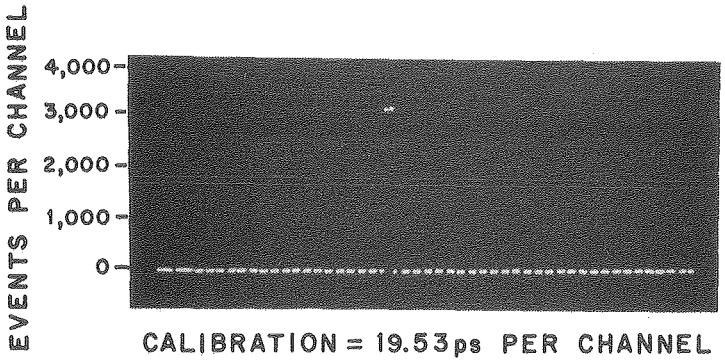


Fig. 19

DISTRIBUTION OF OVERLAPPED EVENTS FROM Fig. 17, BUT DELAYED BY HALF A CHANNEL WITH RESPECT TO THE MISSION START. SEPARATION BETWEEN EACH EVENT IS 10.24μs.

X88 791-337

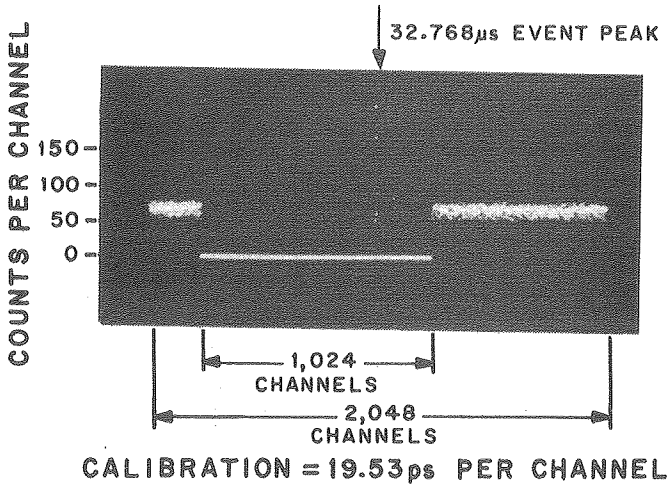


Fig. 20

RANDOM PHASE DISTRIBUTION OF MISSION STARTS OBTAINED BY 32.768μs INPUT EVENT RATE.

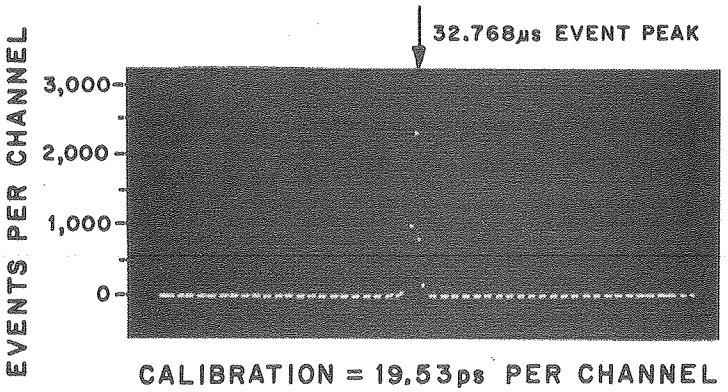


Fig. 21

DISTRIBUTION OF RANDOM 32.768μs TIME INTERVALS IN RELATION TO THE MISSION START (EXPANDED PEAK PORTION OF Fig. 20).

XBB 791-338

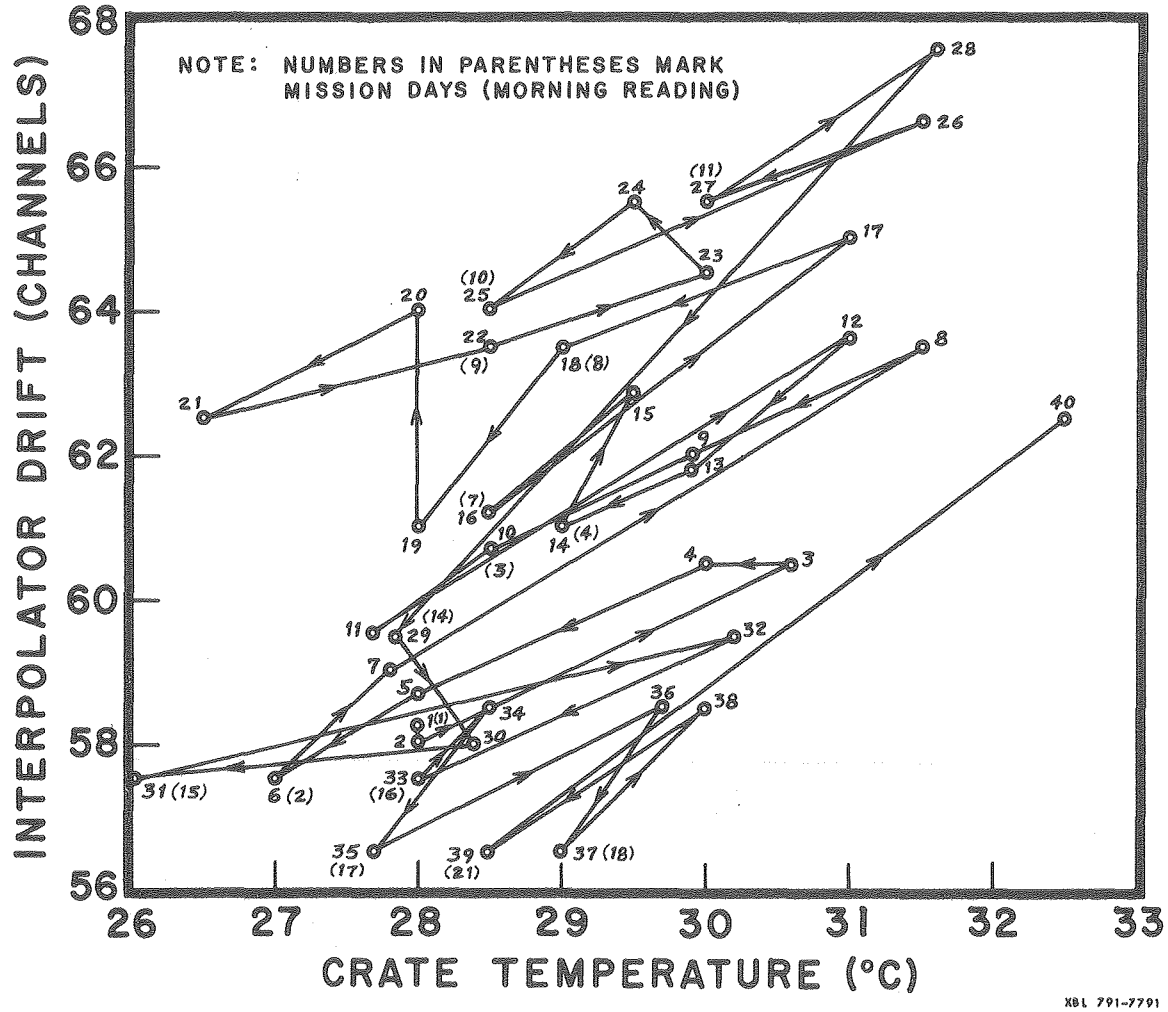

NOTE: NUMBERS IN PARENTHESES MARK MISSION DAYS (MORNING READING)
INTERPOLATOR DRIFT (CHANNELS)
CRATE TEMPERATURE (°C)
68
66
64
62
60
58
56
26
27
28
29
30
31
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Fig. 22

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