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Dopant Profiling of III-V Nanostructures for Electronic Applications

By

Alexandra Caroline Ford

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Professor Yuri Suzuki, Chair
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Abstract

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High electron mobility III-V compound semiconductors such as indium arsenide (InAs) are promising candidates for future active channel materials of electron devices to further enhance device performance. In particular, compound semiconductors heterogeneously integrated on Si substrates have been studied, combining the high mobility of III-V semiconductors and the well-established, low cost processing of Si technology. However, one of the primary challenges of III-V device fabrication is controllable, post-growth dopant profiling. Here InAs nanowires and ultrathin layers (nanoribbons) on SiO_2/Si are investigated as the channel material for high performance field-effect transistors (FETs) and post-growth, patterned doping techniques are demonstrated.

First, the synthesis of crystalline InAs nanowires with high yield and tunable diameters by using Ni nanoparticles as the catalyst material on SiO_2/Si substrates is demonstrated. The back-gated InAs nanowire FETs have electron field-effect mobilities of ~4,000 cm^2/Vs and I_{ON}/I_{OFF} ~10^4. The uniformity of the InAs nanowires is demonstrated by large-scale assembly of parallel arrays of nanowires (~400 nanowires) on SiO_2/Si substrates by a contact printing process. This enables high performance, "printable" transistors with 5-10 mA *ON* currents.

Second, an epitaxial transfer method for the integration of ultrathin layers of single-crystalline InAs on SiO_2/Si substrates is demonstrated. As a parallel to silicon-on-insulator (SOI) technology, the abbreviation "XOI" is used to represent this compound semiconductor-on-insulator platform. A high quality InAs/dielectric interface is obtained by the use of a thermally grown interfacial $InAsO_x$ layer (~1 nm thick). Top-gated FETs exhibit a peak transconductance of ~1.6 mS/μm at V_{DS}=0.5V with I_{ON}/I_{OFF} >$10^4$and subthreshold swings of 107-150 mV/decade for a channel length of ~0.5 μm.

Next, temperature-dependent *I-V* and *C-V* studies of single InAs nanowire FETs are utilized to investigate the intrinsic electron transport properties as a function of nanowire radius. From *C-V* characterization, the densities of thermally-activated fixed charges and trap states on the surface of as-grown (unpassivated) nanowires are investigated to allow the accurate measurement of the gate oxide capacitance. This allows the direct assessment of the electron field-effect mobility. The field-effect mobility is found to monotonically decrease as the radius is reduced to sub-10 nm, with the low temperature transport data highlighting the impact of surface

roughness scattering on the mobility degradation for smaller radius nanowires. Next, the electrical properties of the InAs XOI transistors are studied, showing the critical role of quantum confinement in the transport properties of ultrathin XOI layers.

Following the investigation of the electrical properties of undoped InAs nanostructures, post-growth, surface doping processes for InAs nanostructures are addressed. Nanoscale, sulfur doping of InAs planar substrates with high dopant areal dose and uniformity by using a self-limiting monolayer doping approach is demonstrated as a means to create ultrashallow junctions. From transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS), a dopant profile abruptness of ~3.5 nm/decade is observed without significant lattice damage. The n^+/p^+ junctions fabricated using this doping method exhibit negative differential resistance (NDR) behavior, demonstrating the utility of this approach for device fabrication with high electrically active sulfur concentrations of ~$8x10^{18}$ cm^{-3}.

Next, a gas phase doping approach for InAs nanowires and ultrathin XOI layers using zinc is demonstrated as an effective means for enabling post-growth dopant profiling of nanostructures. The versatility of the approach is demonstrated by the fabrication of gated diodes and *p*-MOSFETs. Electrically active zinc concentrations of ~$1x10^{19}$ cm^{-3} are achieved which is necessary for compensating the high electron concentration at the surface of InAs to enable heavily *p*-doped structures. This work could have important applications for the fabrication of planar and non-planar devices based on InAs and other III-V nanostructures which are not compatible with conventional ion implantation processes that often cause severe lattice damage and local stoichiometry imbalance.

Lastly, an ultrathin body InAs XOI tunneling field-effect transistor (TFET) on Si substrate is demonstrated. The post-growth, zinc surface doping approach is used for the formation of a p^+ source contact which minimizes lattice damage to the ultrathin body InAs XOI compared to ion implantation. The transistor exhibits gated NDR behavior under forward bias, confirming the tunneling operation of the device. In this device architecture, the *ON* current is dominated by vertical band-to-band tunneling and is thereby less sensitive to the junction abruptness. This work presents a device and materials platform for studying III-V tunnel transistors.

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Chapter 1: Introduction and Motivation

1.1. Interest in III-V Nanowires for Device Applications

III-V compound semiconductors such as indium arsenide (InAs) are likely future active channel materials in field-effect transistors (FETs) due to their high electron mobilities. III-V semiconductor devices offer the promise of both higher performance and lower power consumption for energy efficient electronics.[1,2,3,4,5] However, the use of III-Vs presents a number of challenges, ranging from cost-effectiveness to means of post-growth, patterned doping.

III-V heterogeneous integration on Si substrates has been studied as a way to combine the high mobility of III-Vs with the well-established, low cost processing of Si technology.[4,5,6] For example, nanowires can be readily assembled on Si and other substrates.[7,8,9,10] Z. Fan, et al. recently demonstrated highly-ordered, parallel arrays of Ge nanowires with wafer-scale uniformity through use of a contact printing process on Si and flexible plastic substrates.[7] R. Yerushalmi, et al. developed a roll printing approach to print large-scale, highly-aligned Ge/Si core/shell nanowire arrays.[8] In both cases, the success of the assembly method was shown by fabrication of nanowire array FETs delivering high *ON* currents.[7,8] The printing approach has also been used for the integration of optically active CdSe nanowires and Ge/Si core/shell nanowires for image sensor circuitry.[11] The contact printing approach has also been extended to III-Vs to print InAs nanowires on SiO_2/Si substrates (as will be discussed in Chapter 3) as well as on polyimide substrates to study the radio frequency response of flexible InAs nanowire array transistors.[12] The ability to assemble different types of nanowires on Si and other substrates, as well as control their size, structure, composition and morphology, makes them ideal one-dimensional building blocks for various applications in high performance nanoelectronics and/or large-area, flexible electronics (Figure 1).[12,12,13,14,15,16,17,18,19]

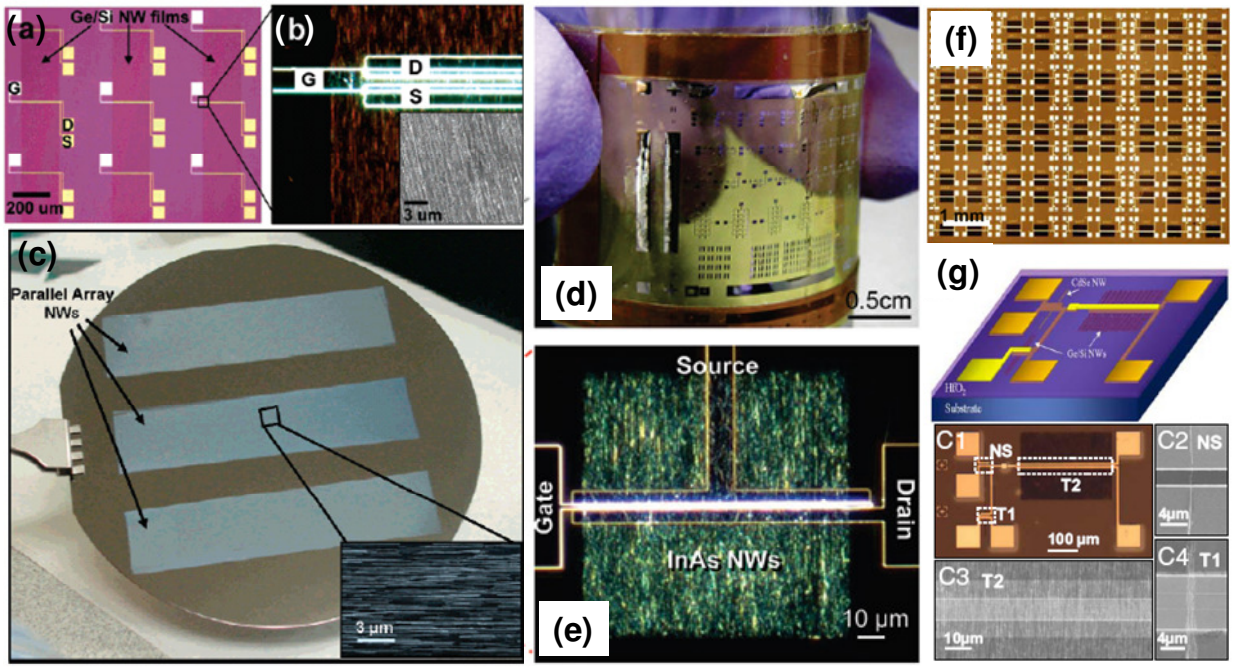

Figure 1. Examples of nanowire printing on Si and flexible substrates. (a),(b) Ge/Si nanowire FET arrays on SiO_2/Si. (c) Ge nanowire arrays printed over wafer-scale areas on SiO_2/Si. (d), (e) InAs nanowire arrays printed on polyimide substrates and configured into flexible InAs nanowire array transistors. (f),(g) CdSe and Ge/Si core/shell nanowires printed for image sensing circuits.[7,9,11,12]

Single Ge/Si core/shell nanowire FETs integrated with high-κ gate dielectrics have already been demonstrated to out-perform state-of-the-art MOSFETs.[18] Potentially more promising, InAs nanowires have been widely studied as the channel material for high performance transistors owing to both their high electron mobility and ease of near-ohmic metal contact formation due to the intrinsic surface charge accumulation layer.[14,14,20,21,22] T. Bryllert, et al. demonstrated a vertical, wrap-gated InAs nanowire transistor using ~80 nm diameter InAs nanowires grown using chemical beam epitaxy (CBE) with catalysts at lithographically patterned locations.[14] The devices had field-effect mobilities of ~3000 cm^2/Vs, sub-threshold swings of ~100mV/dec, and *ON* currents of ~400 μA at V_{DS}=1V and V_{GS}=0.1V for a 40 nanowire matrix array device. S. Dayeh, et al. also reported field-effect mobility values of ~2740 to 6580 cm^2/Vs (depending on the method used for mobility extraction) for ~30-75nm diameter InAs nanowires grown by metal organic chemical vapor deposition (MOCVD) configured into top-gate devices.[22] X. Jiang, et al. demonstrated ~25 nm diameter single nanowire InAs/InP core/shell back-gated FETs with field-effect mobilities as high as ~11,500 cm^2/Vs.[21] In addition to device applications, InAs has a large bulk exciton Bohr radius (~34 nm) which is on the order of the size of the nanowire diameter, resulting in 1-D quantum confinement of the carriers with potentially interesting carrier transport properties.[23] In Chapters 2 and 3 a means to grow high-quality InAs nanowires using a lower cost method (compared to CBE and MOCVD) will be demonstrated, and the field-effect mobilities of the InAs nanowires as a function of their diameter will be studied.

1.2. Interest in III-V Microstructures Utilizing Epitaxial Transfer for Device Applications

Epitaxial lift-off and transfer of crystalline microstructures to various support substrates, including Si, has also been shown to be a versatile technique for applications ranging from optoelectronics to large-area electronics (Figure 2).[24,25,26,27] Specifically, high performance, mechanically flexible macro-electronics and photovoltaics have been demonstrated on plastics, rubbers, glass, and Si substrates utilizing this method.[28,29,30] In one example of epitaxial lift-off and transfer of III-Vs, GaAs/AlAs multilayer structures grown by MOCVD, with layer thicknesses of several nanometers to micrometers and areas of micrometers to centimeters, have been separated and released by etching of the AlAs layers in hydrofluoric acid (HF) (Figure 2a-d).[30] Assuming high etch selectivity between the materials of the different layers (here the GaAs etch rate is 10^6 times lower than the etch rate of AlAs), this technique can be applied to different layered materials. *n*-doped GaAs layers separated by AlAs were released by this method and then printed onto polyimide-coated glass substrates to serve as the active layer for MESFETs, which were then configured into circuits. More complex versions of this technique were applied by growth and release of multiple undoped GaAs/*n*-doped GaAs bilayers separated by AlAs, followed by printing the bilayers onto polyurethane coated Si substrates for the fabrication of near-infrared detectors. Arrays of detectors were then used as infrared imagers (Figure 2e, f). The technique was also used to release and transfer multiple *n*-GaAs/*n*-AlGaAs/*n*-GaAs/*p*-GaAs/*p*-AlGaAs/*p*-GaAs six-layer stacks separated by AlAs to polyethylene terephthalate (PET) substrates for the fabrication of flexible single-junction solar cells (Figure 2g, h). As shown in Figure 3d, the layers for all three types of devices could be grown on one GaAs substrate, which could then be reused after all the device layers were released by etching of the AlAs.

In addition, transfer printing processes have been extended to the nanoscale by transferring *n*- and *p*-type ultrathin body Si nanoribbon arrays onto polyimide and poly(dimethylsiloxane) (PDMS) substrates to create flexible CMOS circuits (Figure 2i).[29] The performance of these circuits is comparable to circuits fabricated on silicon-on-insulator (SOI) wafers.

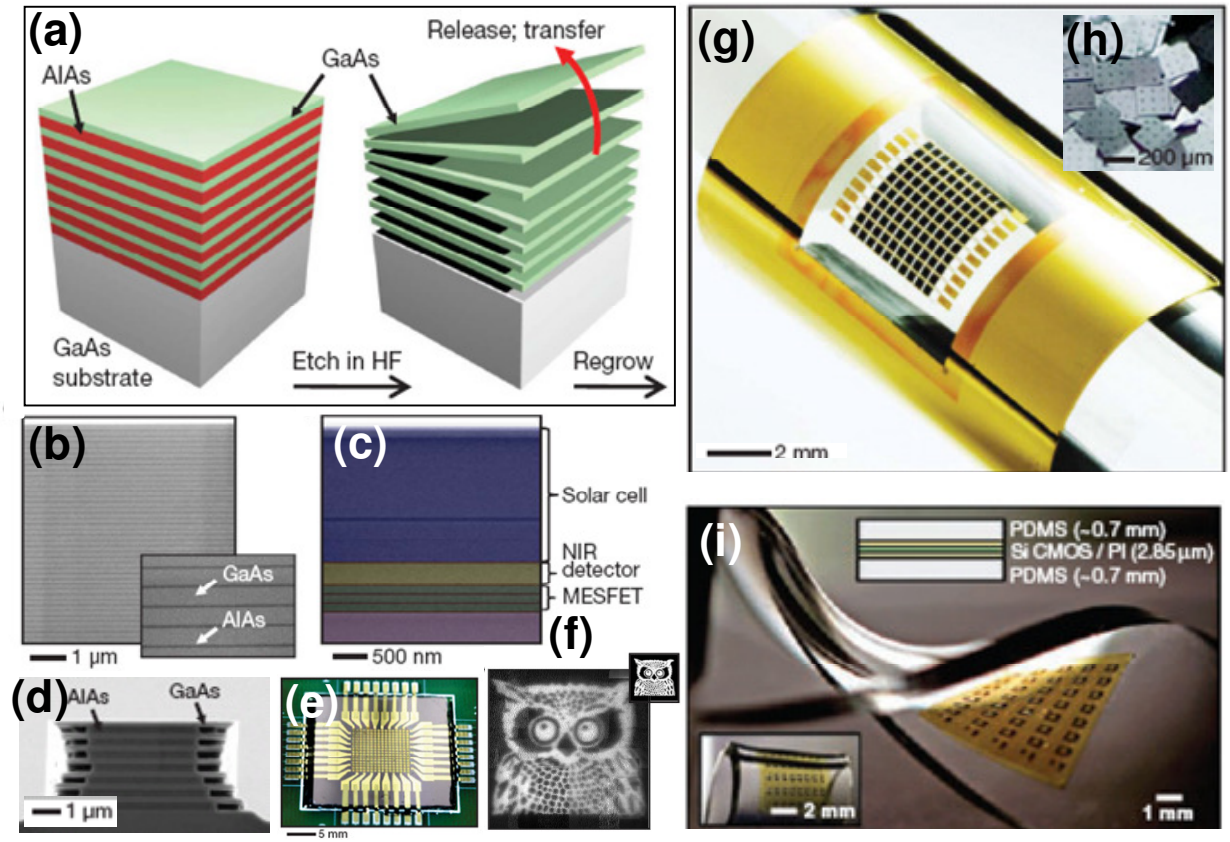

Figure 2. Examples of micro- and nanostructure epitaxial transfer onto different substrates. (a) Schematic of epitaxial lift-off and transfer of GaAs microstructures by AlAs layer etching. (b) SEM image of as-grown GaAs/AlAs layers. (c) SEM image of undoped, *n*-doped, and *p*-doped GaAs layer stacks separated by AlAs layers (red) grown on a single GaAs wafer. The stacks were epitaxially transferred and configured into MESFETs, near-infrared detectors, and solar cells. (d) SEM image showing partially etched AlAs layers. (e) Near-infrared imager mounted on a printed circuit board and image taken (f) using the device (picture in upper right corner is original image), (g) flexible and (h) rigid solar cells fabricated using epitaxially transferred GaAs microstructures. (i) Transfer printing of *n* and *p*-type Si nanoribbon arrays onto PDMS for flexible CMOS circuits.[29,30]

1.3. Use of III-V Nanowire or Epitaxially Transferred Nanostructures for Novel Devices

The use of nanowire or epitaxially transferred ultrathin III-V layers on SiO_2/Si offers the benefit of reduced leakage currents due to 1) smaller junction areas and 2) no junction leakage path to the semiconductor body, thereby permitting lower *OFF* state currents critical to the use of low band-gap semiconductors like InAs.[31] Smaller diameter or thickness nanostructures are therefore more desirable from an electrostatics point of view. It is of technological interest to investigate the mobility-diameter or mobility-thickness dependence in InAs nanostructures, particularly given the contradictions in the literature regarding the effect of reduction of nanowire radius on mobility.

The lower *OFF* state currents of nanowires and ultrathin layers-on-insulator allows for the study of different device architectures, such as tunneling field effect transistors (TFETs),

which are promising to potentially replace or complement metal-oxide-semiconductor field effect transistors (MOSFETs) due to their improved sub-threshold swing (*SS*) and reduced power consumption.[32,33,34,35,36,37] Small band gap III-V semiconductors like InAs are ideal for use in tunneling devices, as the small direct band gap provides a low effective tunneling barrier and the low effective mass results in a high tunneling probability to achieve high *ON* currents.[38] Use of different III-V semiconductors also enables heterojunctions with band alignments optimized to achieve a low effective tunneling barrier.[39]

Figure 3 shows the device structure for one of the best III-V TFETs to date. The device has an *ON* current density of ~50 μA/μm, I_{ON}/I_{OFF} ratio >10^4 and *SS* ~93 mV/dec at V_{DS} = 1.05V for a channel length *L*=100nm. The device is based on an MBE grown InGaAs n^+-*n*-*i*-p^+ structure on InP, making it incompatible with (and expensive compared to) current Si technology.[40] It is therefore desirable to investigate a way to integrate III-V nanostructures on Si as a means toward a manufacturable TFET. In Chapter 5, an ultrathin body InAs nanoribbon TFET on Si substrate will be demonstrated.

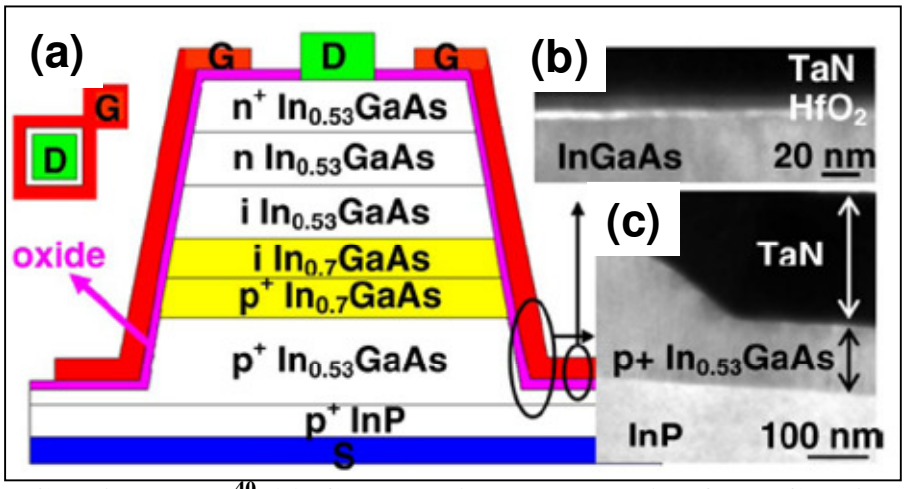

Figure 3. $In_{0.7}Ga_{0.3}As$ TFET.[40] (a) Cross-sectional schematic of $In_{0.7}Ga_{0.3}As$ TFET with a HfO_2 gate oxide and TaN gate. (b) TEM image showing TaN/HfO_2/InGaAs interface. (c) TEM image showing sidewall structure. The complexity of the device structure and fabrication on InP substrate renders the device impractical for manufacturing.

1.4. Post-growth, Patterned Doping of III-V Nanostructures

Since the device processing requirements for III-V semiconductors are significantly different from elemental semiconductors such as Si, they impose a major challenge on nanoscale III-V device fabrication.[41,42] One of the primary challenges of III-V device fabrication is controllable, post-growth dopant profiling. Doping during growth has been previously reported for III-V nanostructures, but post-growth, patterned doping is desired for most device fabrication schemes.[43,44,45] In the Si industry, ion-implantation has been the dominant doping technique for decades due to its advantages of precise species, dose, and depth control. However, the sub-5 nm ultrashallow junction (USJ) depths necessary for use with sub-10 nm gate lengths to achieve efficient electrostatics and acceptable leakage currents are already difficult to successfully achieve using conventional ion implantation and rapid thermal annealing (RTA) in Si technology. During ion implantation, atoms are displaced by dopant ions, creating damage to the crystal lattice. The ions are then activated onto the desired lattice sites and the crystal quality is

restored by rapid thermal annealing. However, the use of ion implantation and RTA to achieve sub-5 nm USJs is severely limited by the transient-enhanced diffusion (TED) caused by ion-implantation induced crystal damage. The TED broadens the junction profile. Research efforts to minimize TED and create shallow doping profiles while still using ion implantation as the doping technique include the use of heavier implantation dopant sources (i.e. molecular implantation, gas cluster ion beam, and plasma doping) followed by flash or laser annealing.[46,47,48,49,50]

These USJs are used for the source/drain extensions in MOSFETs and must have depths of ~1/3 the gate length in the device for efficient electrostatics and acceptable leakage currents. As gate length is reduced to enable the device to operate at faster switching speeds, the junctions (and operating voltage) must also be reduced by the same factor so as to obtain the same electric field patterns in the device. The device cannot scale down without also reducing the junction depth because of drain-induced barrier lowering (DIBL). DIBL is the result of the electric field from the drain attracting carriers from the source into the channel when the device is supposed to be in the *OFF* state, thereby increasing *OFF* current and reducing the threshold voltage V_t (V_t roll off). DIBL (and therefore device *OFF* current) is minimized by keeping the junctions shallow. However, a shallow junction of depth x_j results in a higher sheet resistance ρ_s, by $\rho_s = \frac{1}{\bar{\sigma} x_j} = \frac{1}{e\int_0^{x_j}[N_D(x)-N_B]\mu[N_D(x)]dx} \propto \frac{1}{N_D x_j}$, so in order to combat this the junction must also be heavily doped to a concentration N_D (where N_B is the background doping concentration of the semiconductor body). To ensure that the *ON* current is not reduced, $R_{contact}+R_{souce}+R_{extension} < 0.1R_{channel}$, with each parasitic resistance R component illustrated in Figure 4. Therefore, to meet both DIBL and sheet resistance (i.e. $R_{extension}$) requirements, it is necessary to use a heavily doped, ultra-shallow junction. Currently, ion implantation followed by flash (anneal time ~0.1s) or laser (anneal time ~1μs) annealing is used to make the ultrashallow junction extensions to achieve (at best) 10 nm deep junctions. However, to obtain these 10 nm junctions, the doping in the source-drain extensions has to be much lower (to minimize lattice damage and TED) than the doping in the source (S) and drain (D) regions, which increases the sheet resistance (i.e. $R_{extension}$) and lowers the *ON* current.

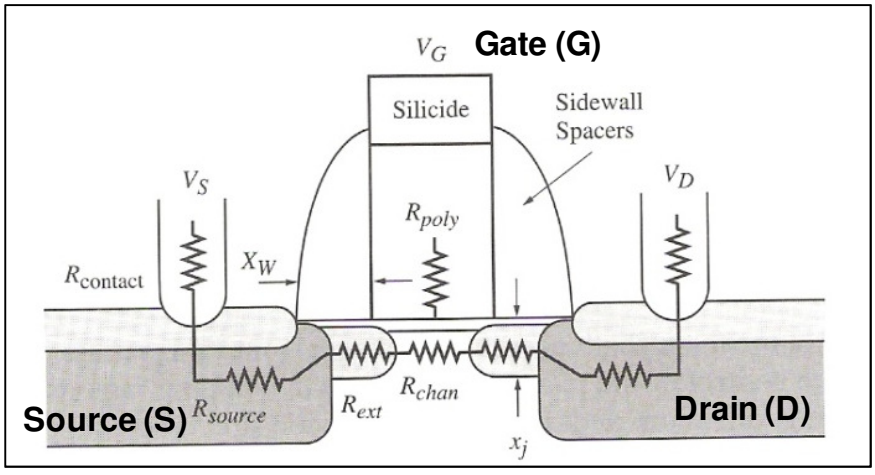

Figure 4. MOSFET schematic showing source-drain extensions and parasitic resistance contributions that degrade *ON* current.[51]

In addition to these problems of doping at the nanoscale in Si, ion implantation presents additional problems for compound semiconductors which consist of two or more chemically and electronically non-equivalent lattice sites. The stoichiometry can be altered and difficult to recover from implantation induced crystal damage which cannot be fixed by a subsequent annealing process.[52,53,54] The residual damage can lead to higher junction leakage and lower dopant activation in compound semiconductors.[55] As a result, surface doping processes such as monolayer and gas-phase doping that create minimal lattice damage are highly attractive.[56,57] While the monolayer doping (MLD) approach is limited to the maximum surface areal dose, it provides high dopant areal dose control and good uniformity due to the self-limiting nature of the monolayer formation reaction. Following the formation of the self-assembled monolayer of molecules containing the desired dopant atoms on the semiconductor surface, the dopant atoms are driven in using RTA. Figure 5a shows a schematic of an MLD process developed for boron doping of Si.[57] Both *p*- and *n*- doping of planar Si (*p*-doping by boron-MLD shown in Figure 5) and Si nanowires/nanobelts (nanoribbons) has been achieved by MLD using molecular precursors containing boron (allylboronic acid pinacol ester (ABAPE)) and phosphorous (diethyl 1-propylphosphonate (DPP) or trioctylphosphine oxide (TOP)).

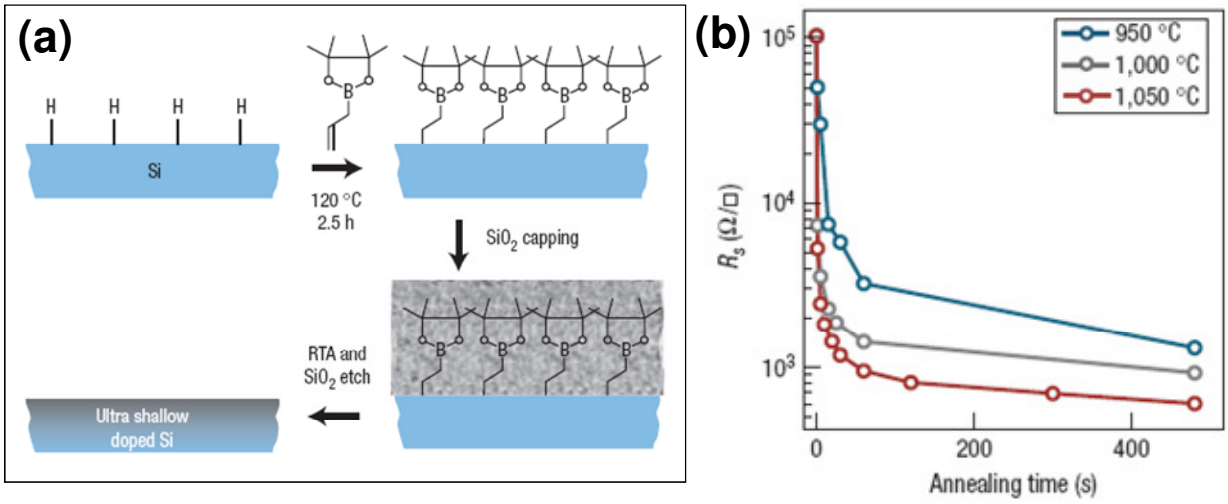

Figure 5. Boron monolayer doping (B-MLD) of Si.[57] (a) The native oxide is first removed from the Si substrate, followed by reaction with the boron containing molecular precursor to form the self-assembled monolayer, capping with electron-beam evaporated SiO_2, RTA to break down the molecular precursor and drive in the boron atoms, and, finally, removal of the SiO_2 cap. (b) Sheet resistance vs. annealing time profiles at different RTA temperatures following B-MLD.

The dopant concentration can be modulated by the size of the molecular precursor footprint, with smaller footprint molecular precursors leading to higher doping concentrations due to a higher surface concentration of dopant containing molecules. This is illustrated by comparing sheet resistance R_s values from two phosphorous monolayer doped samples where two different sized phosphorous containing molecular precursors were used.[57] The larger molecular precursor (TOP) has a ~6 times larger footprint than the smaller molecular precursor used (DPP). Total phosphorous doses estimated from sheet resistance vs annealing time profiles (Figure 6) where TOP was used were ~6 times smaller than for DPP, corresponding to a higher sheet resistance.

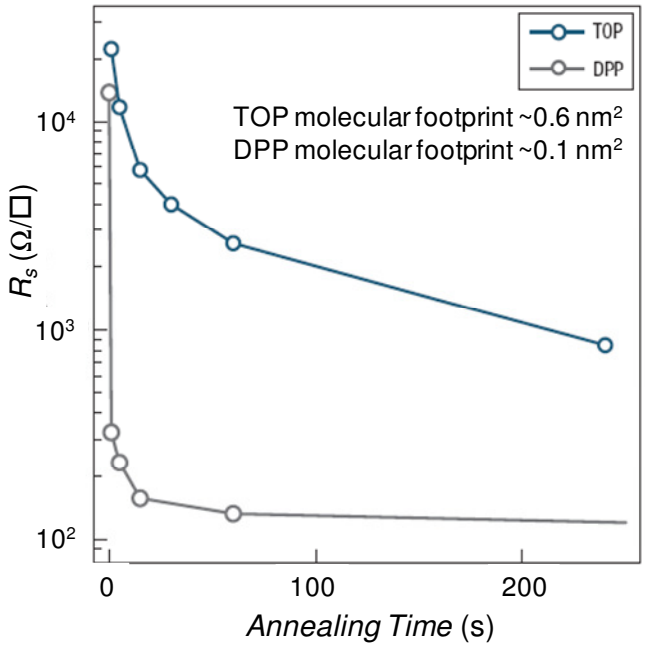

Figure 6. Sheet resistance vs annealing time profile for an RTA temperature of 1000 C using two different sized phosphorous containing molecular precursors for phosphorous monolayer doping (P-MLD) of Si.[57] Use of a smaller molecular footprint molecular precursor results in a higher dopant dose (and lower R_s).

Depths of ~18 nm (950 C for 5s RTA) for boron MLD and ~30 nm (900 C for 5s RTA) for phosphorous MLD doped junctions were obtained from Secondary Ion Mass Spectrometry (SIMS) profiles. Follow-up to this work was able to achieve sub-5nm USJs by using the same B-MLD and P-MLD techniques (utilizing the same molecular precursors ABAPE and DPP) followed by spike annealing in an RTA tool.[56] The process achieved sub-5nm USJs with low sheet resistance (Figure 7a), high dopant activation efficiency (Figure 7b), and minimal junction leakage currents (<1μA/cm^2) with wafer-scale uniformity.

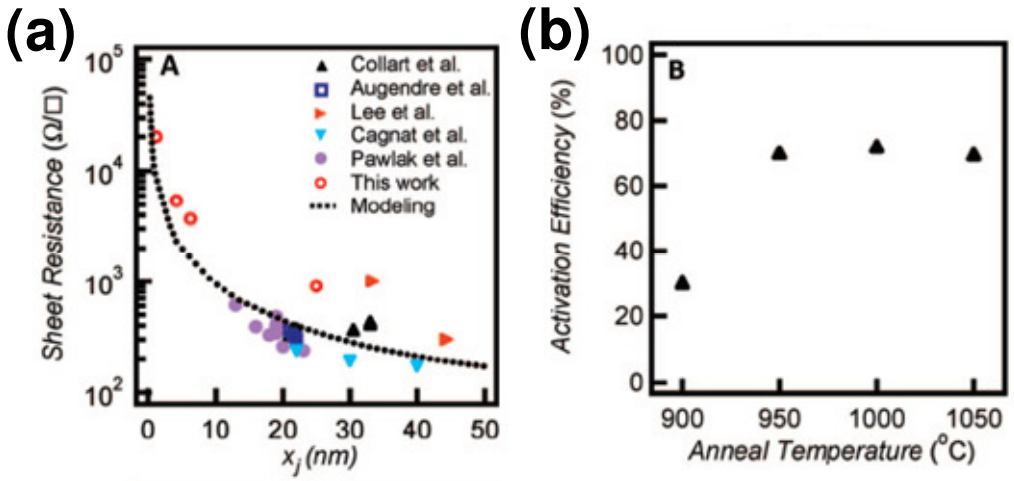

Figure 7. Electrical characterization of USJs achieved by P-MLD. (a) Sheet resistance vs. junction depth for P-MLD process shown alongside conventional doping methods. The dotted line corresponds to modeling using the constant source diffusion model. (b) Dopant activation efficiency as a function of spike anneal temperature.[56]

Additionally, since the monolayer provides uniform surface coverage (and, therefore, uniform doping), the MLD approach can be used with non-planar, three-dimensional structures (for example, vertically oriented nanowire or nanopillar arrays) unlike ion implantation. The monolayer doping approach also has the advantage of being relatively inexpensive and, as previously shown, creates minimal lattice damage (and, therefore, minimal TED). Chapters 4 and 5 demonstrate the successful extension of the monolayer doping process using an appropriate molecular precursor to III-V semiconductors for *n*-doping to create n^+/p USJs. However, due to surface chemistry limitations, finding a molecular precursor for an MLD process that would enable p^+/n USJs (*p*-doping) proved challenging. As a result, a gas phase surface doping method for *p*-doping was used instead. Gas phase doping is limited by the solid solubility, is a higher temperature process than ion implantation combined with RTA, and it is often difficult to achieve a low surface concentration without a long drive-in. Additionally, gas-phase diffusion lacks the uniformity and areal dose control of the monolayer doping approach. However, with the need for *p*-doping, continued device scaling, and use of III-Vs, these disadvantages are offset by the advantage that gas-phase doping creates minimal lattice damage. Chapter 4 and 5 will demonstrate monolayer and gas-phase doping for post-growth, patterned doping of III-V nanostructures.

1.5 Overview of Work

Here two methods are demonstrated to integrate InAs as the channel material on SiO_2/Si substrates for high-performance FETs. This combines the high mobility of III-V semiconductors with the low-cost, well-established processing of Si technology. This also allows for the fabrication of different novel devices, without the constraints of the original growth substrates. First, a "bottom-up" low-cost method to grow high quality InAs nanowires is demonstrated, followed by a means to assemble them through a printing process on SiO_2/Si substrates. Second, a "top-down" epitaxial transfer process is demonstrated as a means of integrating InAs on SiO_2/Si substrates. This is an extension of the previously discussed epitaxial layer transfer

processes to the nanoscale with III-Vs for the demonstration of high-performance FETs on SiO_2/Si substrates. Mobility as a function of nanowire diameter or ultrathin body thickness is then investigated (as there are conflicting reports in the literature on this topic), with important trade-offs between mobility and electrostatics (improved gate control and lower leakage currents) highlighted. Finally, doping processes which cause minimal lattice damage and are compatible with III-Vs at the nanoscale are demonstrated. Compared to previous work demonstrating doping during the growth of the material, the methods demonstrated here are patterned, post-growth doping techniques which present a route for manufacturing.

Chapter 2: InAs Nanostructures

2.1. Chapter Introduction

Recently, a variety of semiconductor nanostructures have been the focus of intensive research efforts and have been proposed as the building blocks for various technological applications due to their unique properties.[11,12,13,14,15,16,17,18,19] The miniaturized dimensions of these nanostructures provide improved electrostatics for nanoscale transistors (i.e. enhanced gate control and lower leakage currents due to both 1) smaller junction areas and 2) no leakage path to the semiconductor body). The ability to transfer and assemble these nanostructures on almost any substrate, including Si, presents a means toward high-performance, printable electronics.[7,8,9,10,11,12]

There has been major interest in the use of InAs as the channel material for high-performance transistors due to its high electron mobility.[12,14,20,21,22] However, in order to utilize InAs nanostructures in high-performance transistors, methods must be developed to synthesize and integrate high quality InAs nanostructures with current Si technology. This chapter reports on two such methods, one being a "bottom-up" approach to grow InAs nanowires using the vapor-liquid-solid (VLS) / vapor-solid-solid (VSS) process using solid-source InAs and annealed Ni thin films to form catalyst particles. Using this method, the diameter of the nanowires is controlled by the thickness of Ni film deposited (i.e. catalyst size). The second method involves a "top-down" approach to form ultrathin body InAs nanoribbons by lithography and etching of molecular beam epitaxy (MBE) grown InAs thin films. Using this method, the thickness of the nanoribbons is controlled by MBE growth of the InAs film, while the nanoribbon width is controlled by lithography and subsequent etching. The successful transfer and integration of the InAs nanostructures fabricated using each method on SiO_2/Si substrates is then demonstrated by configuring the InAs nanostructures into field-effect transistors.

2.2. InAs Nanowires

The reported synthesis of non-epitaxial, semiconductor nanowires often involves the vapor-liquid-solid (VLS) or vapor-solid-solid (VSS) mechanisms, where a metal nanoparticle catalyzes the growth.[21,22,58] Here the synthesis of crystalline, high-mobility InAs nanowires with tunable diameters using Ni nanoparticles as the catalyst is demonstrated. These nanowires are then successfully transferred to receiver substrates in highly regular arrays by a contact printing process and configured as the channel material for high performance transistors.

Ni nanoclusters used for the InAs nanowire growth were obtained by thermal annealing (800-900ºC) of thin Ni films (thermally evaporated) on 50 nm thermally grown SiO_2/Si substrates in a hydrogen environment. Due to the mobility and diffusion of the Ni atoms on SiO_2 surfaces at elevated temperatures, nanoparticles are formed. The nanoparticle diameters can be

tuned by the corresponding thin film thickness and the annealing conditions. Figure 1 shows the atomic force microscopy (AFM) images and corresponding particle diameter distributions of Ni particles formed by the thermal annealing of 0.5 nm (Figure 8a and b), 1.5 nm (Figure 8c and d), and 3 nm (Figure 8e and f) Ni films at 850 ºC for 10 min. The nanoparticle diameters obtained from AFM and scanning electron microscopy (SEM) for the 0.5, 1.5, and 3 nm films are 10±2, 14±3, and 26±5 nm, respectively. The diameter variation as a percent of the mean for all three particle sizes is ~20%. This is very good considering the simplicity of this method, and that the variation for commercially available colloidal Au nanoparticles used to grow nanowires of similar diameter (20-40 nm) is ~10%.

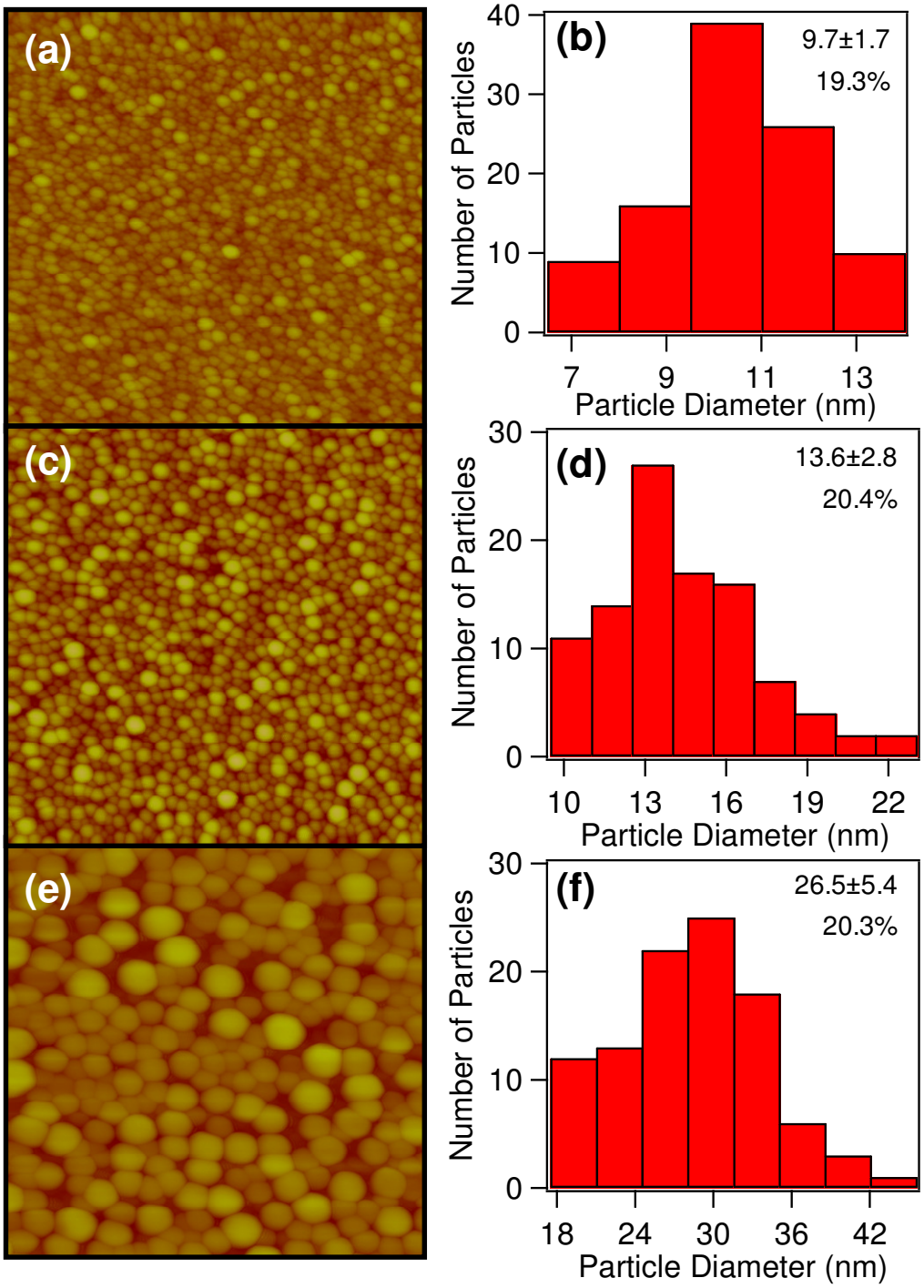

Figure 8. AFM images and nanoparticle diameter distribution histograms for Ni particles resulting from the thermal anneal of (a,b) ~0.5 nm, (c,d) ~1.5 nm, and (e,f) ~3 nm Ni films at 850 ºC for 10 min. All AFM images show an area of 1 µm x 1 µm. Particle diameter average and standard deviation are shown in the upper right corners of the histograms.

The nanoparticles attained from thin film annealing were used as catalytic seeds for the growth of InAs nanowires. After the thermal annealing process, the sample temperature was reduced to 470-550ºC, and InAs nanowires were then grown for ~1 hr by vaporization of InAs solid source (source temperature 720ºC). The growth furnace consisted of two independently controlled temperature zones, one for the solid source and the other for the sample, similar to the previously reported Au-catalyzed InAs nanowire growth set up.[21] Hydrogen (150 s.c.c.m.) was used as the carrier gas for the delivery of the thermally vaporized solid InAs source. The pressure was maintained constant at ~1 torr. The nanowires were grown chemically intrinsic without any intentional doping. SEM images of Ni-catalyzed InAs nanowires grown from different particle diameters are shown in Figure 9. From the SEM images, it is evident that the nanowires are relatively straight with low structural defect density. Furthermore, Ni nanoparticles can be observed at the tips of the nanowires (Figure 9), which is a distinct characteristic of the tip-based, VLS/VSS growth mechanism. The nanowire diameter shows a direct correlation with the catalytic nanoparticle diameter. Nanowire diameters of 23±6, 26±8, and 38±9 nm were obtained for 10, 14, and 26 nm nanoparticles, respectively. The variation as a percent of the mean for the grown nanowires is 25-32% which is slightly larger than that of the nanoparticle distribution. The optimal sample temperature is found to depend on the nanoparticle diameter. For the 10, 14, and 26 nm nanoparticles, sample temperatures of 475, 500, and 520ºC were found to yield the highest density of nanowires, respectively (Figure 10). The higher growth temperature for larger particles may be expected as the larger particles may have higher eutectic temperatures. Also, while relatively high nanowire growth yields are observed at the optimal temperatures for both 10 and 14 nm nanoparticles (5-50 nanowires/μm^2), significantly lower yield is observed for the 26 nm nanoparticles (~1 nanowires/μm^2).

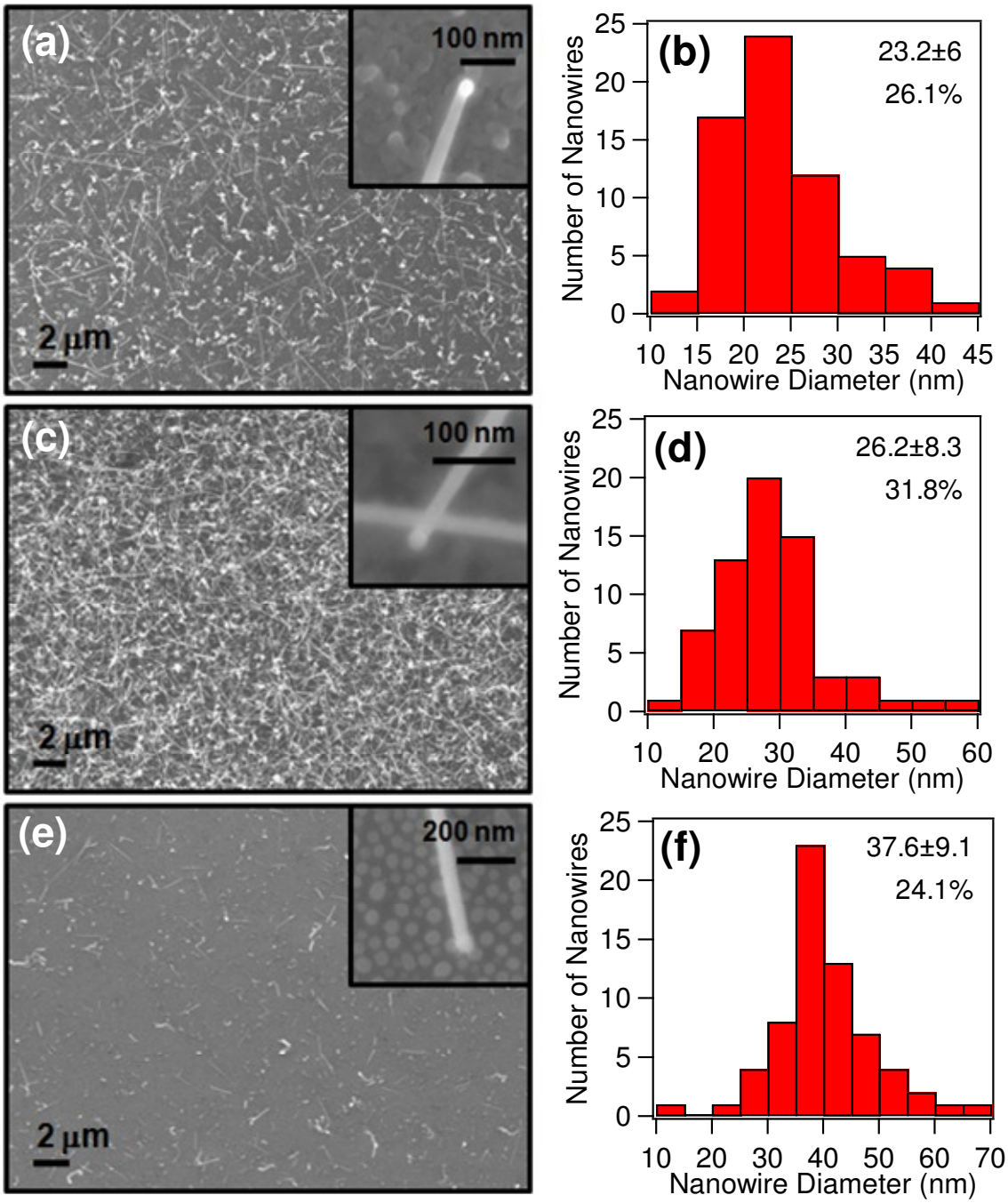

Figure 9. SEM images and nanowire diameter distribution histograms for InAs nanowires grown using Ni catalyst particles produced by the thermal anneal of (a,b) 0.5 nm, (c,d) 1.5 nm, and (e,f) 3 nm Ni films. SEM image insets clearly show the Ni catalyst tips at the ends of the nanowires, depicting the tip-based growth mechanism. Nanowire diameter average and standard deviation are shown in the upper right corners of the histograms.

This diameter dependent growth yield may be explained by the higher activation energy and higher InAs source delivery rate required for the successful nucleation and growth of larger diameter nanowires. However, the phase diagrams for Ni-In-As have not been well-studied, either experimentally or theoretically. It should be noted that growth temperatures using Ni and Au nanoparticles of similar diameter are approximately the same (Figure 10), suggesting similar eutectic temperatures for the Au-In-As and Ni-In-As systems at this scale.

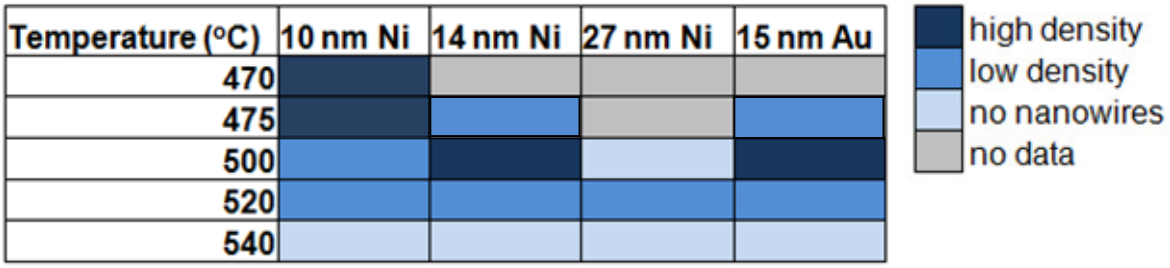

Figure 10. InAs nanowire growth yield studies at different sample temperatures for annealed Ni films of various thicknesses and commercially available Au colloids. High density corresponds to >5 nanowires/μm^2 while low density corresponds to ~1 nanowire/μm^2.

The structure of the InAs nanowires was studied by transmission electron microscopy (TEM). Low and high resolution TEM images confirm the crystallinity and low defect density of the nanowires as well as the presence of a 2-3 nm thick amorphous surface layer. This layer thickness is consistent with the typical native oxide present on the surface of bulk InAs. Most of the nanowires have diameters ranging from ~20-40 nm. The diameters are uniform along the nanowire and no "tapering" is observed, confirming the lack of uncontrolled over-coating during the growth process. Figure 11 shows typical HRTEM images of InAs nanowires grown at 475 ^{o}C. No dominant growth axis was observed. Several nanowires studied by TEM grew in the [211] direction, with one such nanowire shown in Figure 11a. Nanowire growth along the [210] direction (Figure 11b) was also observed. Figure 11c shows a nanowire grown ~7^{o} off the [111] direction. Data obtained from standardless x-ray EDS elemental analysis gave In/As ratios ranging from 1.2 to 1.5, suggesting the composition of the nanowires is close to the expected stoichiometry.

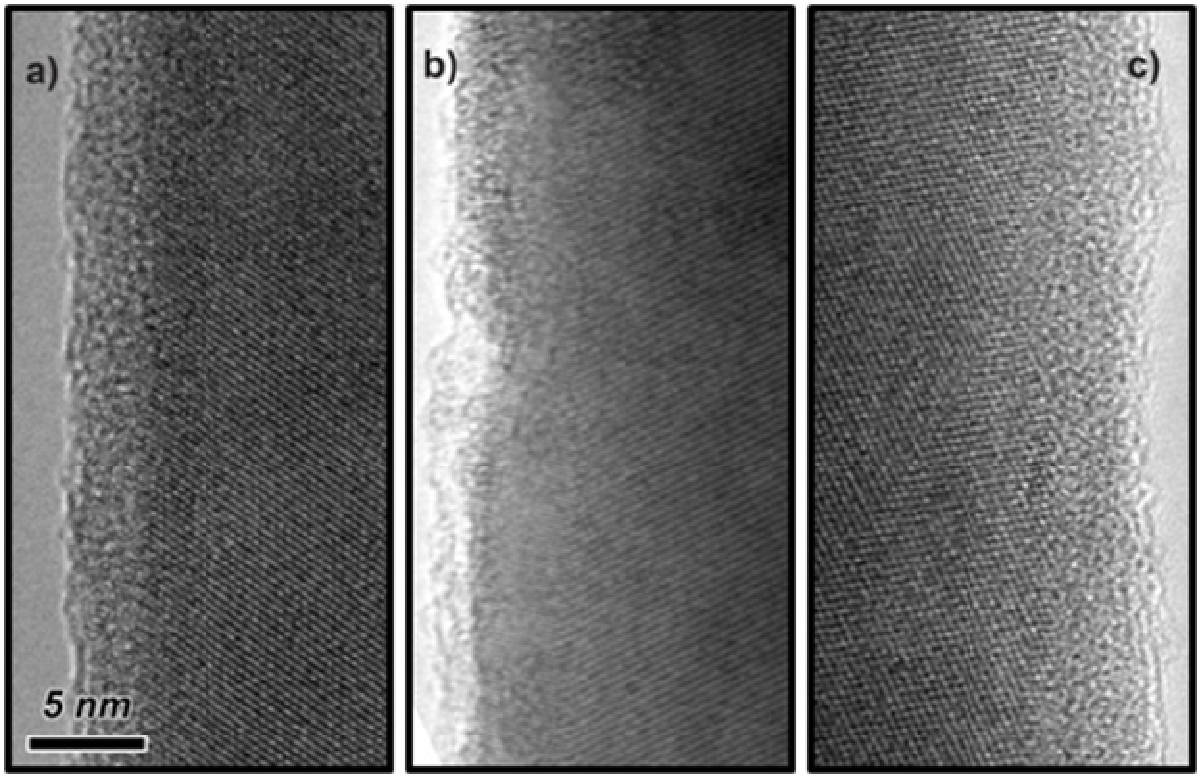

Figure 11. HRTEM images of typical InAs nanowires grown using Ni catalyst nanoparticles. (a) Growth axis along the [211] direction, (b) growth axis along the [210] direction, and (c) growth axis 7^{o} off the [111] direction.

To characterize the electrical properties of the Ni-catalyzed InAs nanowires, FETs were fabricated (Figure 12a) by using Ni (~50 nm) source/drain (S/D) metal contacts in a back-gated geometry (50 nm thermal oxide as gate dielectric, and heavily B doped Si substrate as the gate). The electrical properties of a representative FET consisting of an individual InAs nanowire as the channel material with diameter (i.e. channel width) d~25 nm (actual nanowire diameter is ~29 nm with ~2 nm native oxide shell subtracted) and a channel length of L~9.9μm are shown in Figure 12b and c. The transistor shows minimal hysteresis (Figure 12b) with an *ON* current I_{ON}~12 μA at V_{DS} = 3V and V_{GS}=5V, corresponding to a current density of ~0.5 mA/μm as normalized with the nanowire diameter. It is important to note that the *ON* current for this long channel device is comparable to that of state-of-the-art Si MOSFETs (I_{ON}~1 mA/μm), even though the channel length is over two orders of magnitude larger. The device also exhibits a respectable $I_{ON}/I_{OFF}>10^3$ (Fig 12b, inset) at V_{DS}=0.5V. The low-bias *ON*-state conductance of this nanowire as normalized by the channel length is G_{ON}~60 μS.μm. The nanowire transistors exhibit a uniform response in terms of both *ON* and *OFF* state conductance with G_{ON}=40-120 μS.μm and $G_{ON}/G_{OFF}>10^2$ for over 100 measured devices (d=20-30 nm and L=2-10 μm).

The high *ON* current and conductance of the InAs nanowires result from their high electron mobility, and demonstrates the utility of these materials for high performance electronics. Electron mobility is an important figure of merit since it relates the drift velocity of electrons to an applied electric field and is used to evaluate FET performance. The field-effect

mobility of the nanowires was estimated from the transfer characteristics and is depicted in Figure 12d as a function of the back-gate voltage V_{GS}. The field-effect mobility was deduced from the low-bias (V_{DS}=0.1 V) transconductance, $g_m = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{V_{DS}}$, and the analytical expression, $\mu_{n,FE} = g_m \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{DS}}$ where C_{ox} is the gate capacitance. The capacitance C_{ox} = 0.52 fF was obtained from modeling using the finite element analysis software Finite Element Method Magnetics. From the square law model, a peak electron field-effect mobility of $\mu_{n,FE}$~2,700 cm^2/Vs is obtained.

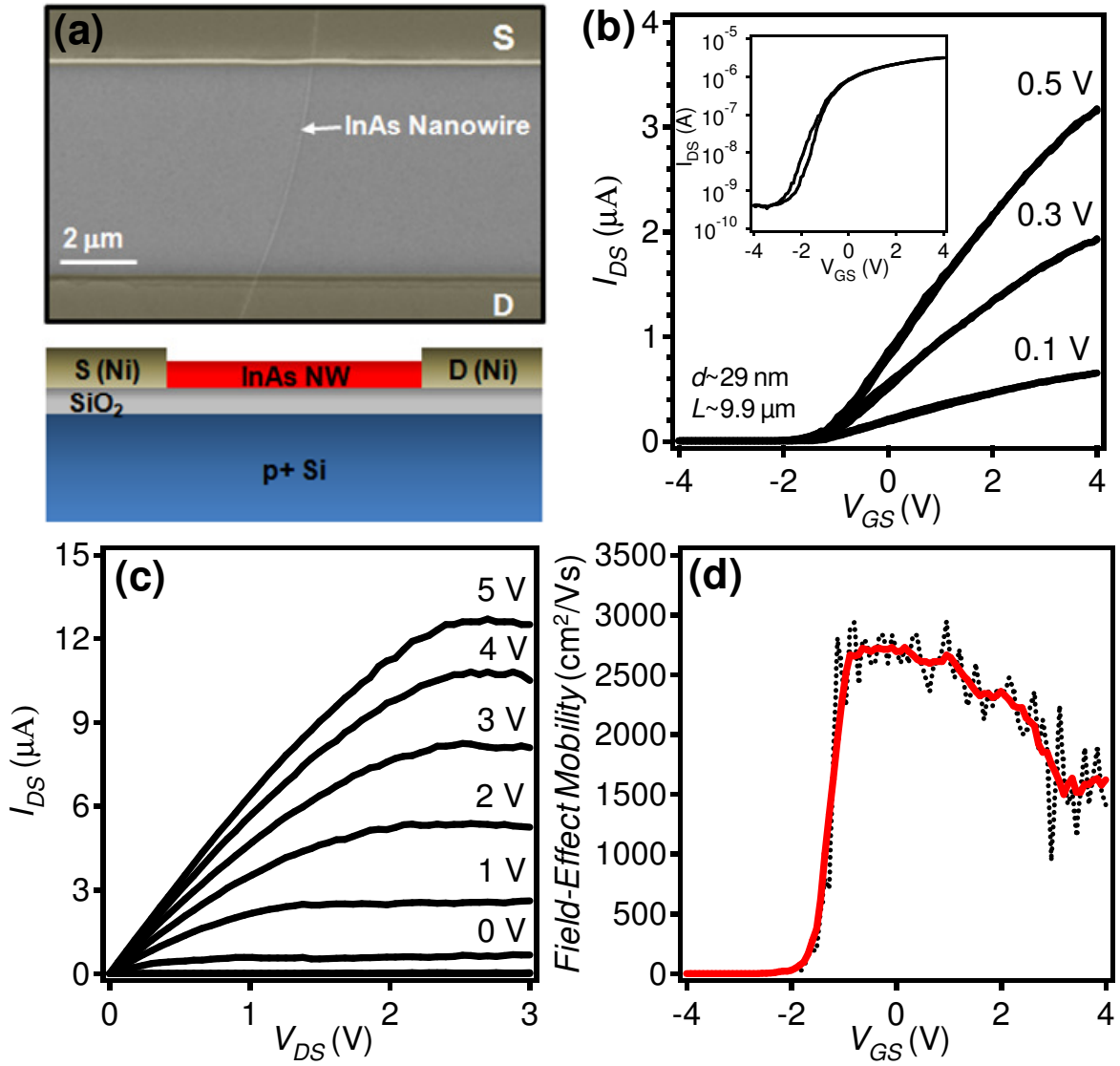

Figure 12. Electrical characteristics of single InAs nanowire FET. (a) A SEM image and a schematic of a back-gated InAs nanowire FET with Ni S/D metal contacts. (b) Linear scale, transfer characteristics of a representative Ni-catalyzed InAs FET with *d*~29 nm (~25 nm InAs core with ~2 nm thick native oxide shell) and *L*~9.9 for V_{DS} = 0.1, 0.3, and 0.5 V. Both forward and backward gate voltage sweep directions are shown, exhibiting a minimal hysteresis. The inset shows the log scale I_{DS}-V_{GS} curve for V_{DS} = 0.5 V. (c) Output characteristics of the same nanowire device at various V_{GS}. (d) Electron field-effect mobility vs. V_{GS} estimated from the transfer characteristic at V_{DS} = 0.1 V. The black dotted line shows the actual data with a peak field-effect mobility of ~3000 cm^2/Vs and the solid red line shows the smoothed values (peak field-effect mobility ~2700 cm^2/Vs). All electrical measurements were conducted in vacuum to minimize hysteresis.

This electron field-effect mobility estimation presents the lower boundary limit since no correction was taken into account, for example, for possible contact resistance. The Ni-catalyzed InAs nanowire mobility is comparable to the previously reported Au-catalyzed nanowires.[14,20,21,22] Further enhancement of the mobility may be achieved in the future by the passivation of the nanowire surfaces with a large band-gap InP shell as previously demonstrated.[21]

2.3. InAs XOI

Here, a modified epitaxial transfer process for integrating ultrathin InAs layers with nanometer-scale thicknesses on Si/SiO_2 substrates for use as high performance nanoscale transistors is demonstrated. The nanoscale thick InAs layers are fully depleted which is important for achieving high performance FETs with respectable *OFF* currents based on small band gap semiconductors. The transfer is achieved without the use of adhesive layers, which allows for purely inorganic interfaces with low interface trap densities and high stability. The process for the fabrication of InAs XOI substrates is shown in Figure 13a. Single-crystalline InAs thin films (10-100 nm thick) were grown epitaxially on a 60 nm thick $Al_{0.2}Ga_{0.8}Sb$ layer on bulk GaSb substrates. Polymethylmethacrylate (PMMA) patterns with a pitch and line-width of ~840 nm and ~350 nm, respectively, were lithographically patterned on the surface of the source substrate. The InAs layer was then pattern etched into nanoribbons by using a mixture of citric acid (1 g/ml of water) and hydrogen peroxide (30%) at a 1:20 volume ratio, which was chosen for its high selectivity and low resulting InAs edge roughness.[59] To release the InAs nanoribbons from the source substrate, the AlGaSb layer was selectively etched by ammonium hydroxide (3%, in water) solution for 110 min.[60] The selective etching of the AlGaSb layer was high enough not to affect the nanoscale structure of the InAs nanoribbons. Next, an elastomeric polydimethylsiloxane (PDMS) substrate (~2 mm thick) was used to detach the partially released InAs nanoribbons from the GaSb donor substrates and transfer them onto Si/SiO_2 (50 nm thermally grown) receiver substrates by a stamping process.[61] In this process, the initial epitaxial growth process is used to control the thickness of the transferred InAs nanoribbons, while the lithographically defined PMMA etch mask is used to define the length and width. Atomic force microscopy (AFM) was utilized to characterize the surface morphology and uniformity of the fabricated XOI substrates. Figures 13b and c show representative AFM images of an array of InAs nanoribbons (~18 nm thick) on a Si/SiO_2 substrate, clearly showing the smooth surfaces (< 1 nm surface roughness) and high uniformity of the structures over large areas. The process allows for the heterogeneous integration of different III-V materials and structures on a single substrate through a multi-step epitaxial transfer process. To demonstrate this capability, a two-step transfer process was used to form ordered arrays of 18 and 48 nm thick InAs nanoribbons that are perpendicularly oriented on the surface of a Si/SiO_2 substrate (Figures 13d and e). This result demonstrates the potential ability of the proposed XOI technology for generic heterogeneous and/or hierarchical assembly of crystalline semiconducting materials. In the future, a similar method may be used to fabricate both *p*- and *n*- type transistors on the same chip for complementary electronics based on the optimal III-V semiconductors.

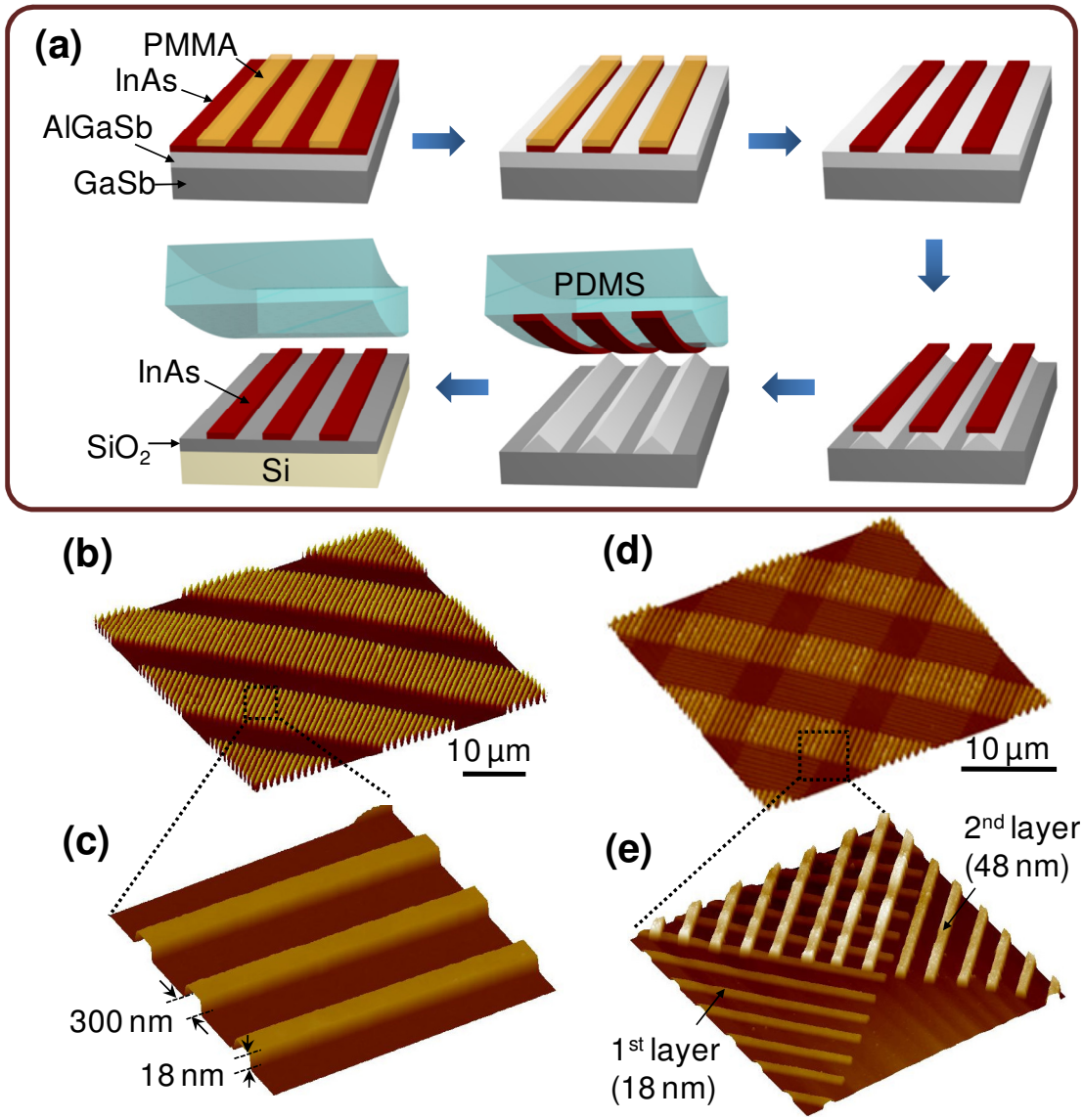

Figure 13. Ultrathin InAs XOI fabrication scheme and AFM images. (a) Schematic procedure for the assembly of InAs XOI substrates by an epitaxial transfer process. The epitaxially grown, single-crystalline InAs films are patterned with PMMA and wet etched into nanoribbon arrays. A subsequent selective wet etch of the underlying AlGaSb layer and the transfer of nanoribbons by using an elastomeric PDMS slab result in the formation of InAs nanoribbon arrays on Si/SiO_2 substrates. (b,c) AFM images of InAs nanoribbon arrays on a Si/SiO_2 substrate. The nanoribbons have a length of ~10 µm, height of ~18 nm and width of ~300 nm. (d,e) AFM images of InAs nanoribbon superstructures on a Si/SiO_2 substrate, consisting of two layers of perpendicularly oriented nanoribbon arrays with 18 and 48 nm thicknesses as assembled by a two-step epitaxial transfer process.

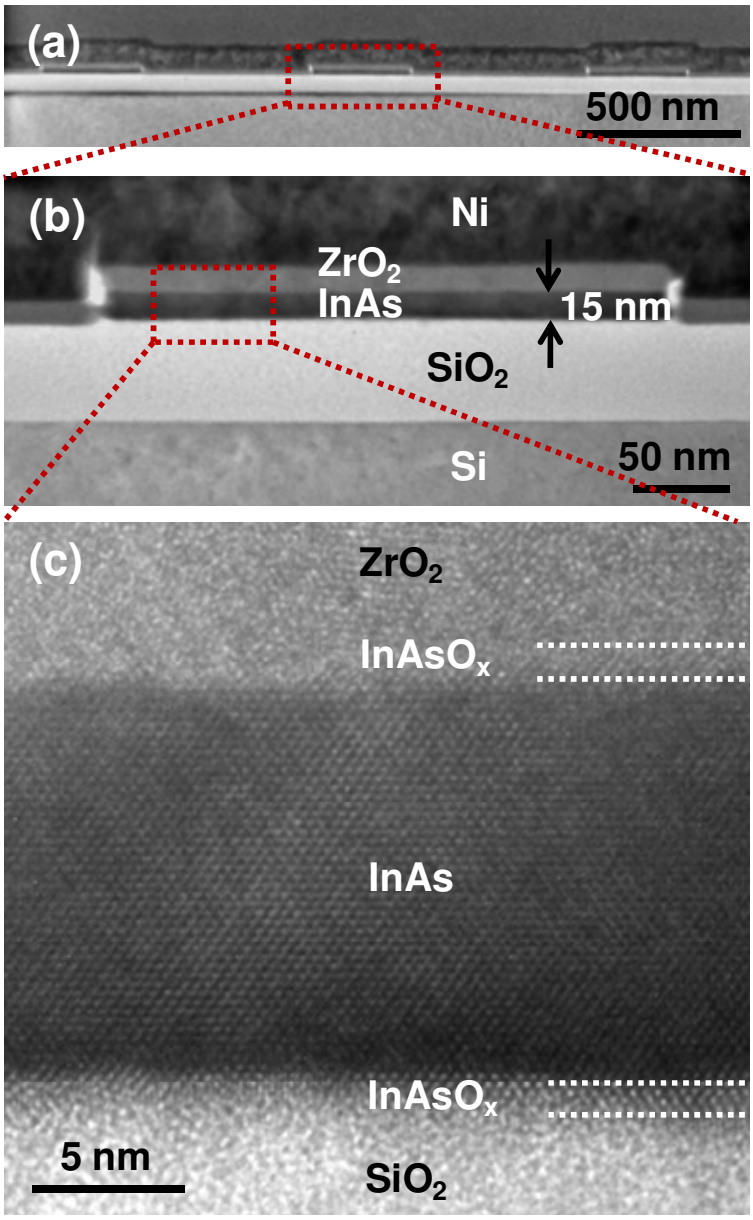

Figure 14. Cross-sectional TEM analysis of InAs XOI substrates. (a) A TEM image of an array of three InAs nanoribbons on a Si/SiO_2 substrate. (b) A magnified TEM image of an individual ~13 nm thick InAs nanoribbon on a Si/SiO_2 (~50 nm thick) substrate. The nanoribbon is coated with a ZrO_2/Ni bilayer (~15 and ~50 nm, respectively) which acts as a top-gate stack for the subsequently fabricated FETs. (c) A HRTEM image showing the single-crystalline structure of an InAs nanoribbon with abrupt atomic interfaces with ZrO_2 and SiO_2 layers on the top and bottom surfaces, respectively. A ~1 nm thick $InAsO_x$ interfacial layer formed by thermal oxidation and used for surface passivation is clearly evident.

To look at the atomic structure of the interfaces, cross-sectional TEM images of an InAs XOI device were taken and are shown in Figure 14. The HRTEM image (Figure 14c) illustrates the single-crystalline structure of InAs nanoribbons (~13 nm thick) with atomically abrupt interfaces with the SiO_2 and ZrO_2 layers. The TEM image of the InAs/SiO_2 interface does not exhibit visible voids (Figure 14c), although only a small fraction of the interface is examined by TEM. As later described, InAs nanoribbons were thermally oxidized prior to the top-gate stack deposition to lower the interfacial trap densities. The thermally grown $InAsO_x$ layer is clearly evident in the HRTEM image (Figure 14c) with a thickness of ~1 nm.

To investigate the performance limits of InAs XOI devices, top-gate FETs with high-κ gate dielectric and channel length L~0.5 µm were fabricated. Ni S/D contacts were lithographically patterned on InAs nanoribbons followed by the atomic layer deposition of ~8 nm thick ZrO_2 (ε ~ 20) as the gate dielectric. A local top-gate (Ni, 50 nm thick), underlapping the S/D electrodes by ~100 nm was then lithographically patterned. Importantly, thermal oxidation of InAs was found to significantly improve the interfacial properties and FET characteristics. Prior to the S/D contact formation, the XOI substrates were first treated with 3% NH_4OH to remove the native oxide followed by the thermal oxidation at 350ºC for 1 min to form a ~1 nm thick $InAsO_x$ layer as shown by TEM (Figure 14c). Figure 15a shows typical I_{DS}-V_{GS} characteristics of a top-gate FET, with the channel material a single ~18 nm thick InAs nanoribbon with a width of ~320 nm. The XOI FET has I_{ON}/I_{OFF}~10^4, a subthreshold swing of $SS=dV_{GS}/d(logI_{DS})$ ~150 mV/decade (Figure 15a), and a peak g_m ~1.6 mS/µm at V_{DS}=0.5V. The lowest measured SS for the XOI FETs is ~107 mV/decade as compared to InAs and InGaAs QW-FETs in literature which have exhibited SS ~ 70 and 75 mV/dec, respectively.[6,62]

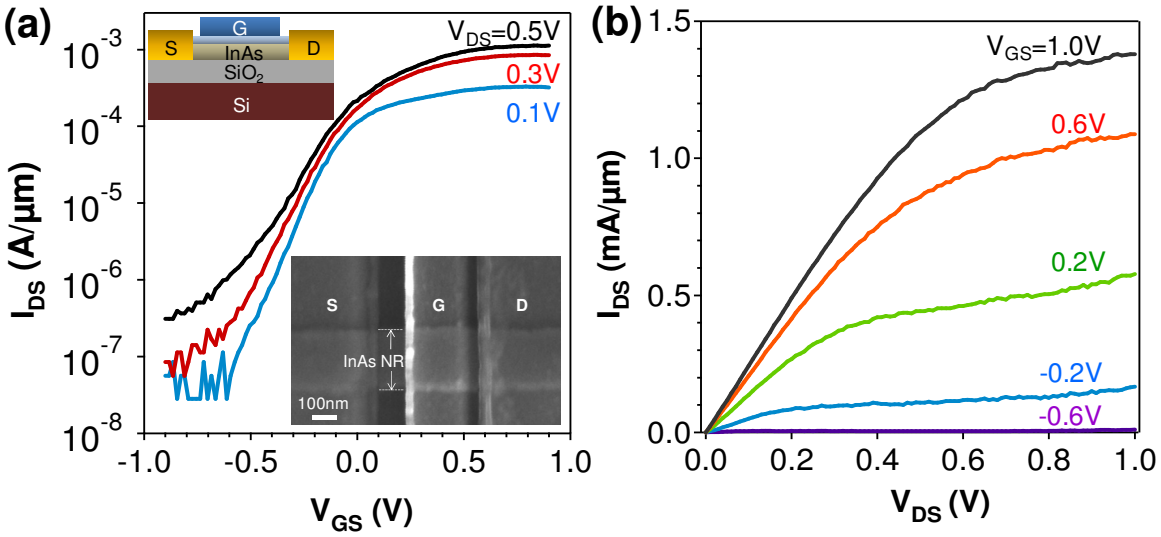

Figure 15. Top-gated InAs XOI FETs. (a) Transfer characteristics of a top-gated InAs XOI FET, consisting of a single nanoribbon (~18 nm thick) with L~0.5 µm and 8 nm thick ZrO_2 gate dielectric. A device schematic (top) and a representative SEM image (bottom) of a top-gated FET are shown in the inset. (b) Output characteristics of the same device shown in (a). Nanoribbons were thermally oxidized at 350ºC for 1 min to form ~1 nm thick interfacial $InAsO_x$ layer for surface passivation of InAs.

The devices reported here use a relatively thick gate dielectric which can be scaled down in the future to further improve the gate electrostatic control and the *SS* characteristics. The single nanoribbon transistor output characteristic is shown in Figure 15b, with an I_{ON}~1.4 mA/μm at an operating voltage of $V_{DD}=V_{DS}=V_{GS}=1$V. To analyze the performance, a device simulation was performed. A close match of the experimental data is obtained with $D_{it}=10^{11}$ states $cm^{-2}eV^{-1}$ used as the fitting parameter, which is a ~60× improvement over devices without any surface treatment (i.e. with a native oxide layer). The fitted D_{it} values represent an estimation. While *C-V* measurement is conventionally used for D_{it} extraction in Si devices, it is challenging and given to error for narrow bandgap semiconductors like InAs.[63] In the future, the development of more accurate techniques for D_{it} measurement in InAs XOI devices is needed. The thermal oxidation process for surface passivation is counter-intuitive as the previous works have focused on the removal of surface oxides.[4] It is speculated that unlike the native oxide layer, thermal oxidation results in the formation of a dense oxide with minimal dangling bonds. Similar to thermally grown SiO_2, the thermal oxide of InAs provides an ideal surface passivation layer, addressing one of the important challenges for InAs devices.

Chapter 3: Electrical Properties of Undoped InAs Nanostructures

3.1. Chapter Introduction

The dependence of the carrier mobility on nanostructure radius (nanowires) or thickness (ultrathin body nanoribbons) for a given material is of particular interest because smaller nanostructures are more attractive for use as the channel material of nanoscale transistors. This is because smaller nanostructures have improved electrostatics and lower leakage currents. In this chapter, electrical properties as a function of nanowire radius or ultrathin body nanoribbon thickness are investigated. Most theoretical studies have found carrier mobility to increase with radius for sub-10 nm Si nanowires (no data available for InAs nanowires), either attributing the trend to the dominant surface roughness scattering in smaller radius nanowires, or an enhanced phonon scattering rate due to an increased electron-phonon wavefunction overlap in smaller radius nanowires.[64,65,66] On the other hand, experimental reports in the literature have been contradictory, ranging from observation of mobility enhancement to degradation with Si nanowire miniaturization for diameters down to 10 nm.[67,68] From these studies, the diameter dependency of the mobility highly depends on the specific nanowire material system, the diameter range, and the method used to extract the electron mobility.[64,65,66,67,68,69] The challenge in attaining accurate experimental data is primarily due to the difficulty of both ohmic contact formation to nanoscale materials and the direct measurement of the gate capacitance.

In this chapter, ohmic contact formation to InAs nanostructures is discussed, followed by current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements of individual InAs nanowires configured into back-gated FETs with ohmic contacts. A method developed by S. Ilani, et al. to measure small capacitance signals is used to perform *C-V* measurements on the InAs nanowire devices, thereby permitting the direct measurement of the gate oxide capacitance as a function of nanowire diameter.[70] This experimentally measured gate oxide capacitance is then compared to analytical and modeled gate oxide capacitance values. The *I-V* and *C-V* electrical measurements are performed over a range of temperatures for nanowires of different diameter. This allows for the direct assessment of field-effect mobility as a function of nanowire diameter and looks at the role of surface/interface fixed charges and trap states on the electrical properties. Field-effect mobility of InAs nanowire array devices is also discussed. Similarly, *I-V* measurements are taken

for ultrathin body InAs nanoribbons of different thickness configured into back-gated field-effect transistors. The field-effect mobility is extracted, allowing for the direct investigation of field-effect mobility as a function of ultrathin body nanoribbon thickness.

3.2. Ohmic Contacts to InAs Nanowires

One of the major challenges associated with nanowire devices, and all nanoscale devices in general, is the development of nanoscale and ohmic Source/Drain (S/D) contacts.[57,71] Nanoscale dimensions for the contacts are needed to reduce the parasitic capacitances and minimize the drain induced barrier lowering (DIBL) effects while low contact resistivity with ohmic interfaces are desired for reduced parasitic resistances. To address this challenge, recently Y. Hu, et al, demonstrated sub-100 nm FETs based on $NiGe_xSi_y$-Ge/Si-$NiGe_xSi_y$ nanowire heterostructures in which $NiGe_xSi_y$ was utilized as the nanoscale metal contact to the Si channel.[72] The fabricated transistors have excellent electrical properties with minimal short channel effects. Additionally, silicide and germanide contacts are known to exhibit higher chemical stability and lower junction resistance as compared to elemental metal contacts, which presents another advantage for the alloyed contacts. While silicides and germanides have been well characterized for both bulk and nanowire structures, metal/InAs alloys are not well-studied with only limited information available in the literature.[73,74] Characterizing metal/InAs alloys with low resistivity and abrupt interfaces as the contact material to InAs is of major interest. Here, the formation and materials properties of Ni_xInAs/InAs/Ni_xInAs heterojuctions by using a simple solid source reaction of Ni with InAs nanowires at annealing temperatures of 220-300 C in N_2 is demonstrated.

InAs nanowires used in this work were synthesized on Si/SiO_2 substrates by the vapor-liquid-solid / vapor-solid-solid process by using Ni nanoparticle catalysts as discussed in Chapter 2. The nanowires were then dropcast on Si/SiO_2 (50 nm thermally grown) substrates followed by photolithography patterning of S/D electrodes, 5 sec 0.5% HF dip, thermal evaporation of Ni (~50 nm thick), and lift-off. The InAs nanowire devices were then thermally annealed at 220-300 C for 5-120 min in N_2 at a pressure of 40 torr. During the annealing process, Ni atoms diffuse into InAs nanowires to form Ni_xInAs (Figure 16a and b). The formation of Ni_xInAs/InAs junctions were observed by optical and scanning electron microscopy (SEM) as the two materials exhibit distinct contrast (Figure 16c). TEM was then used to characterize the crystalline structure and interface abruptness of the InAs/Ni_xInAs heterojunctions. The atomically abrupt junctions are clearly resolved under TEM for a sample annealed at 300 C for 30 min (Figure 16d). The Ni_xInAs is identified as Ni_3InAs from the diffraction pattern and EDS analysis for which a Ni:In:As atomic ratio of 53:24:23 is obtained (Figure 16e).

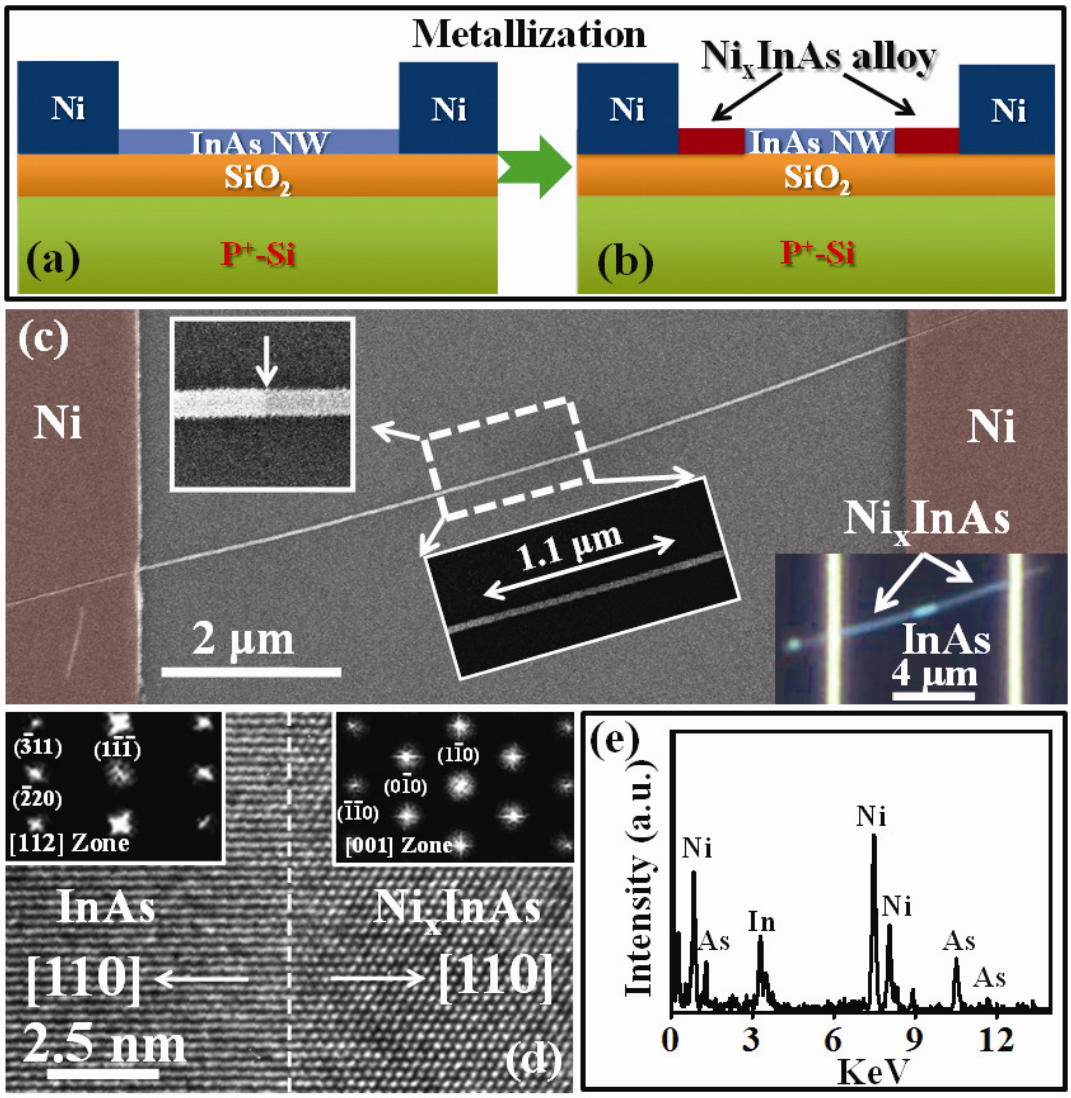

Figure 16. $Ni_xInAs/InAs/Ni_xInAs$ nanowire heterojunctions. Schematic of the long channel InAs devices with Ni S/D electrodes (a) before and (b) after the thermal annealing process. (c) The corresponding SEM image after the thermal diffusion of Ni. The center inset shows the $Ni_xInAs/InAs/Ni_xInAs$ heterojunction. The high magnification SEM image in the upper inset shows the sharp interface. The bottom inset shows the dark-field optical microscopy image of the same nanowire device. The bright nanowire segment in the middle of the device corresponds to InAs which is connected to Ni_xInAs nanowire segments at the two ends. (d) High resolution TEM of a $InAs/Ni_xInAs$ heterojunction, showing the atomically abrupt interface. The insets are the corresponding diffraction patterns extracted by Fast-Fourier Transform, indicating the epitaxial relationship of (220)InAs//(110)Ni_xInAs with [112]InAs//[001]Ni_xInAs. (e) Energy dispersive X-ray spectroscopy of a Ni_xInAs nanowire.

The diffusivity of Ni atoms at 220, 250, and 280 C by examining the diffusion length, x, as a function of annealing time, t, is investigated. An example is shown in Figures 17a-e for which a Ni-contacted InAs device is annealed at 250 C for 25, 40, 50, and 60 min while being inspected by dark-field optical microscopy after each annealing cycle. Figure 17f shows the linear behavior of x vs. $t^{1/2}$ for each diffusion temperature. The observed trend is consistent with the diffusion limited model, that is $x=(Dt)^{1/2}$ where D is the diffusivity of Ni in InAs. The results suggest that the Ni/InAs alloying reaction is limited by how fast the Ni atoms can diffuse in the InAs nanowire. Once Ni atoms diffuse to the Ni_xInAs/InAs nanowire interface, the solid reaction of Ni and InAs takes place, resulting in sharp epitaxial interfaces. This reaction behavior is similar to the previously explored Ni silicidation of Si nanowires.[72] From the diffusion length studies of the Ni/InAs system, diffusion coefficients of $D=8\times10^{-12}$, 3.35×10^{-11}, 1.13×10^{-10} cm^2/sec were obtained for temperatures of 220, 250, 280 C (Figure 17f).

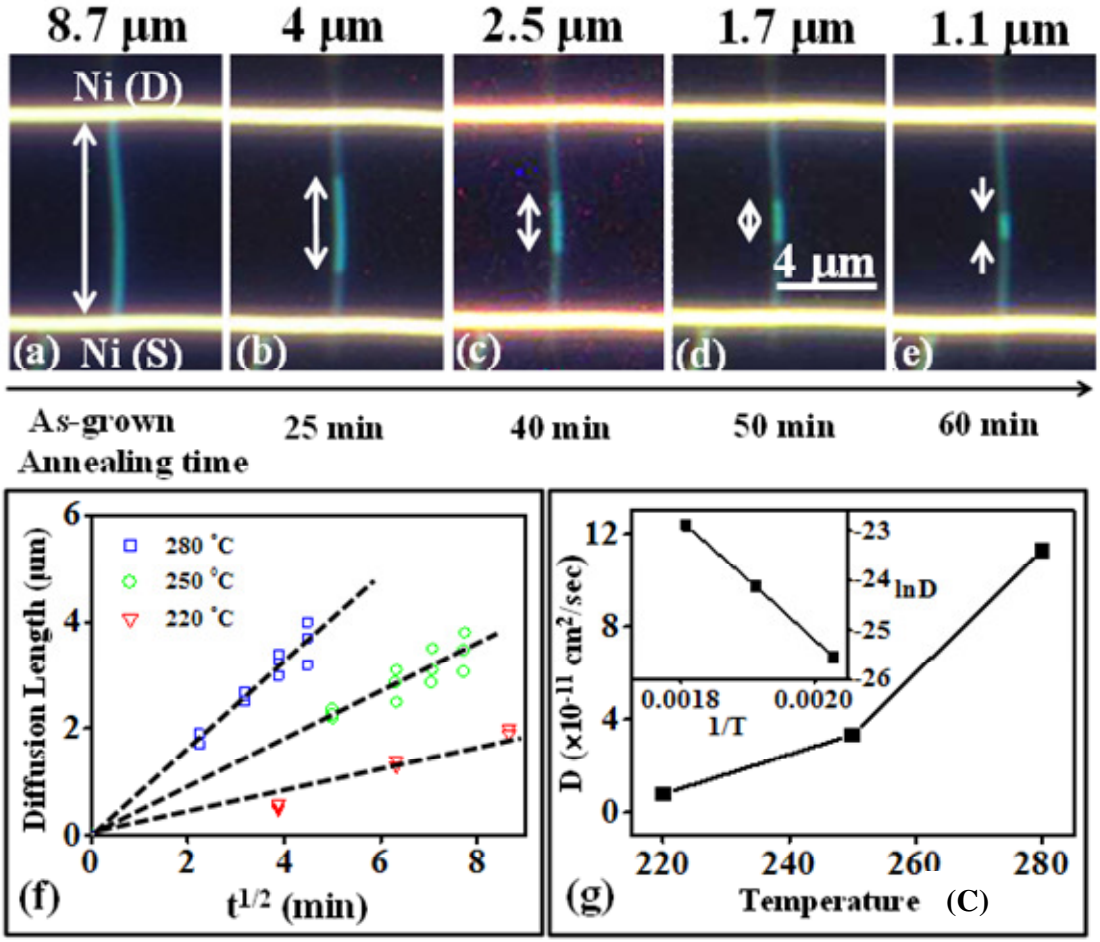

Figure 17. Study of Ni_xInAs formation by a solid source reaction. (a)-(e) Dark-field optical microscopy images of a Ni-contacted InAs nanowire device after subsequent thermal annealing steps. The white arrows indicate the remaining InAs nanowire segments. (f) Ni diffusion length vs the square root of diffusion time for diffusion temperatures of 220, 250, and 280 C. (g) The diffusivity as a function of the temperature. Inset shows the Arrhenius plot of diffusivity vs 1/T.

Ni diffusivity and Ni/InAs alloying reaction rate are independent of the nanowire diameter for d=20-40 nm. This is in distinct contrast to the Ni/Si nanowire system for which a significant diameter-dependence was previously reported by K.-C. Lu, et al. and attributed to the diffusion flux of Ni atoms through the native SiO_2 shell of Si nanowires as the limiting reaction step.[75] In that study, Ni nanowires, overlapped on the top of Si nanowires, were used as the Ni source. In such a system, native SiO_2 is expected between Ni and Si at the point contact interfaces. It was speculated that as a result, for smaller diameter nanowires with smaller contact interface area, a slower injection of Ni atoms is obtained, leading to the observed diameter-dependence of the silicidation reaction rate. In the study here, however, Ni is evaporated on the end segments of InAs nanowires following a HF dip to remove the native oxides (i.e., InO_x and AsO_x) at the interface. As a result, the Ni flux at the contact interfaces is not expected to be the rate-limiting step which may explain the lack of diameter dependence for Ni diffusivity.

Additionally, the electrical properties of the $Ni_xInAs/InAs/Ni_xInAs$ nanowire heterojunctions were investigated. The heterojunctions were back-gate configured transistors with Ni_xInAs serving as nanoscale contacts and InAs as the channel material. The channel length was tuned by the Ni diffusion time, to allow for a systematic study of the electrical properties as a function of the channel length. An example of a characterized device is shown in Figure 18a for which the I_{DS}-V_{GS} curves were measured after subsequent diffusion steps (250 C in N_2) with channel length L=4.6-0.28 μm. For channel length L~4.6 μm, a peak transconductance, $g_m=dI_{DS}/dV_{GS}$=0.23 μS at V_{DS}= 0.1 V is obtained which increases to ~1.4 μS for the same device when L is reduced to 280 nm. There is no significant change observed in the threshold voltage, V_t or the *OFF* current, I_{OFF} as L is reduced to the sub-1-μm regime. This implies that (i) there is no Ni doping of the InAs channel since the $InAs/Ni_xInAs$ interface is atomically abrupt, and (ii) short channel effects are limited even for this device configuration with 50 nm SiO_2 back-gate dielectric. In contrast, severe short channel effects were observed for the sub-micron InAs FETs with bulk Ni contacts fabricated by e-beam lithography, instead of Ni_xInAs nanowire contacts (Figure 19). This result clearly illustrates the advantage of using nanoscale contacts for improved electrostatics, as was also previously reported for Ge/Si nanowire FETs.

Figure 18b illustrates the resistance, R as a function of L at $|V_{GS}-V_t|$=4 V for two different nanowire diameters (d=26 and 30 nm). The smaller diameter nanowire exhibits a larger R which is expected due to the reduced effective channel width. The length-dependent resistance for both nanowire diameters exhibits a similar behavior, consisting of two distinct regimes (Figure 18b). For L>1 μm, a linear dependence of the resistance on the channel length with a slope of ~7.5 kΩ/μm is observed. For L<1 μm, the resistance shows a significantly smaller dependence on the length, approaching the saturation resistance of ~38.5 kΩ. This trend suggests an electron mean free path on the order of a few hundred nm which results in diffusive carrier transport for L>1 μm and quasi-ballistic/ballistic transport for L<1 μm. This extracted mean free path is consistent with that of the bulk InAs which was previously reported to be ~0.3 μm.[76]

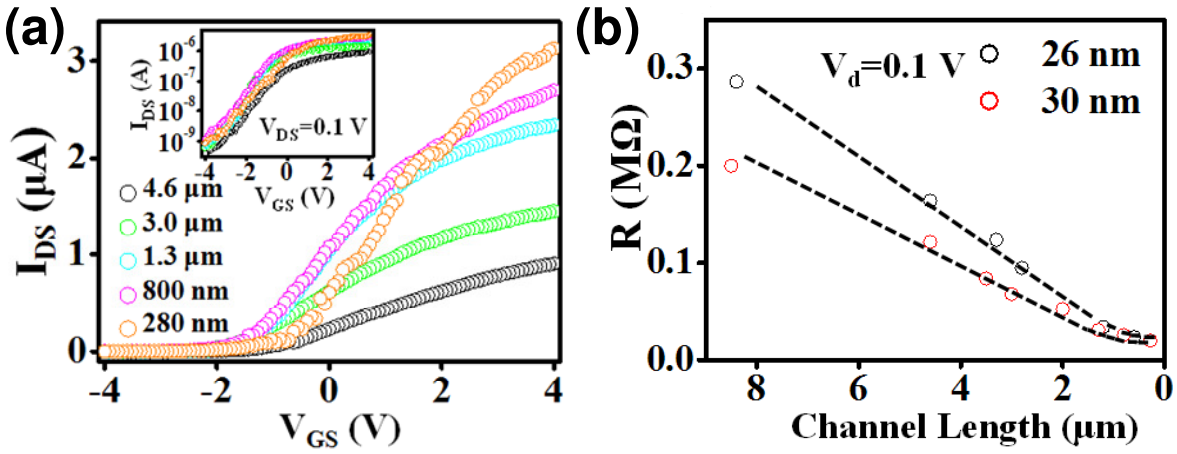

Figure 18. Electrical characteristics of Ni_xInAs/InAs/Ni_xInAs heterojunction. (a) Transfer characteristics (V_{DS}=0.1 V) of a Ni_xInAs/InAs/Ni_xInAs nanowire FET (d=30 nm) after subsequent annealing steps were used to gradually reduce the length of the InAs nanowire channel through the formation of Ni_xInAs. Inset shows the corresponding logscale plot. (b) The *ON*-state resistance vs. channel length for 26 nm and 30 nm InAs nanowires.

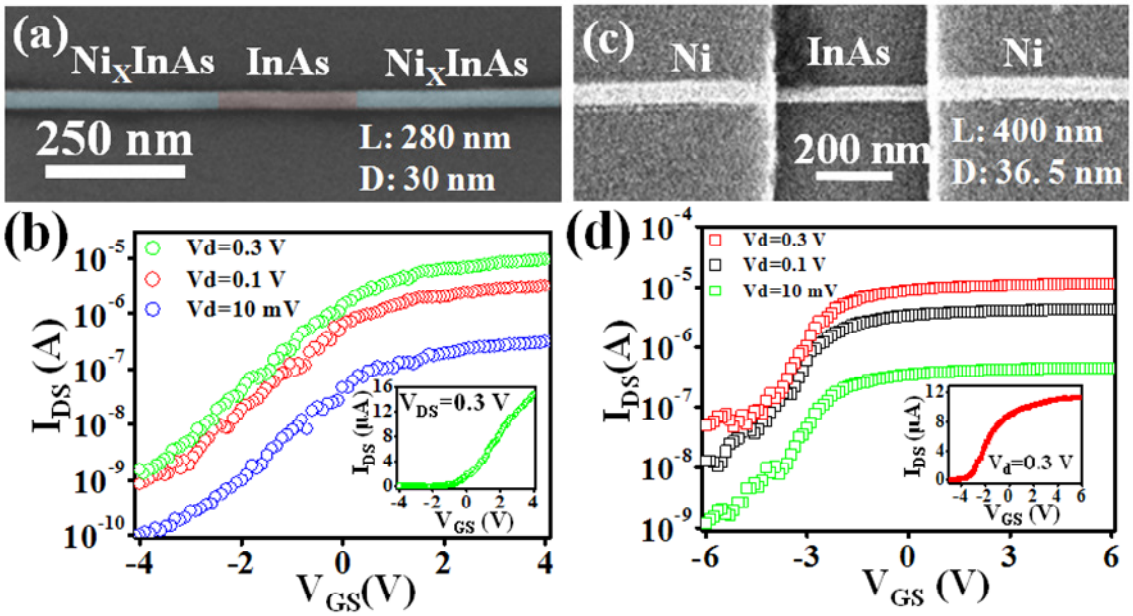

Figure 19. Comparison of short-channel InAs FETs formed by two different approaches. (a) SEM image of a short channel, back-gated FET formed by using the InAs metallization approach, with nanoscale Ni_xInAs contacts. The channel length is ~280 nm. (b) The corresponding logscale I_{DS}-V_{GS} behavior at V_{DS}=0.01, 0.1 and 0.3 V. Inset shows the linear I_{DS}-V_{GS} plot at V_{DS}=0.3V. (c) SEM image of a short channel, back-gated FET fabricated by electron-beam lithography, with bulk Ni contacts. The channel length is ~400 nm. (d) The corresponding logscale I_{DS}-V_{GS} behavior at V_{DS}=0.01, 0.1 V, and 0.3 V. Inset shows the linear I_{DS}-V_{GS} plot at V_{DS}=0.3V. It is clearly evident that the FET with bulk contacts exhibits ~2 orders of magnitude higher I_{OFF} (~10^{-7} vs. 10^{-9} A) due to short channel effects.

3.3. Diameter-Dependent Electron Mobility of InAs Nanowires

InAs nanowires used in this study were synthesized on Si/SiO_2 substrates by a physical vapor transport method using Ni nanoparticles as the catalyst as previous discussed in Chapter 2. The InAs nanowires were over 10 μm long with a radius range of 7-20 nm (Figure 20a). The nanowires are single crystalline with a native oxide thickness of 2-2.5 nm as evident from TEM (Figures 20b and c). The nanowires grown using the condition reported in Chapter 2 do not exhibit any noticeable tapering effect, having uniform diameter along the length of each nanowire, as confirmed by TEM and SEM. EDS, as shown in Figure 20d, indicates that the chemical composition of In:As is nearly 1:1.

For the electrical transport measurements, FETs in a back-gated configuration were fabricated (Figures 20e and f). First, InAs nanowires were harvested in an ethanol solution by a sonication process, and dropcast on a p^+ Si/SiO_2 (50 nm thermally grown) substrate. Metal source/drain (S/D) contacts were then defined by photolithography, Ni evaporation (~50 nm thick), and lift-off.

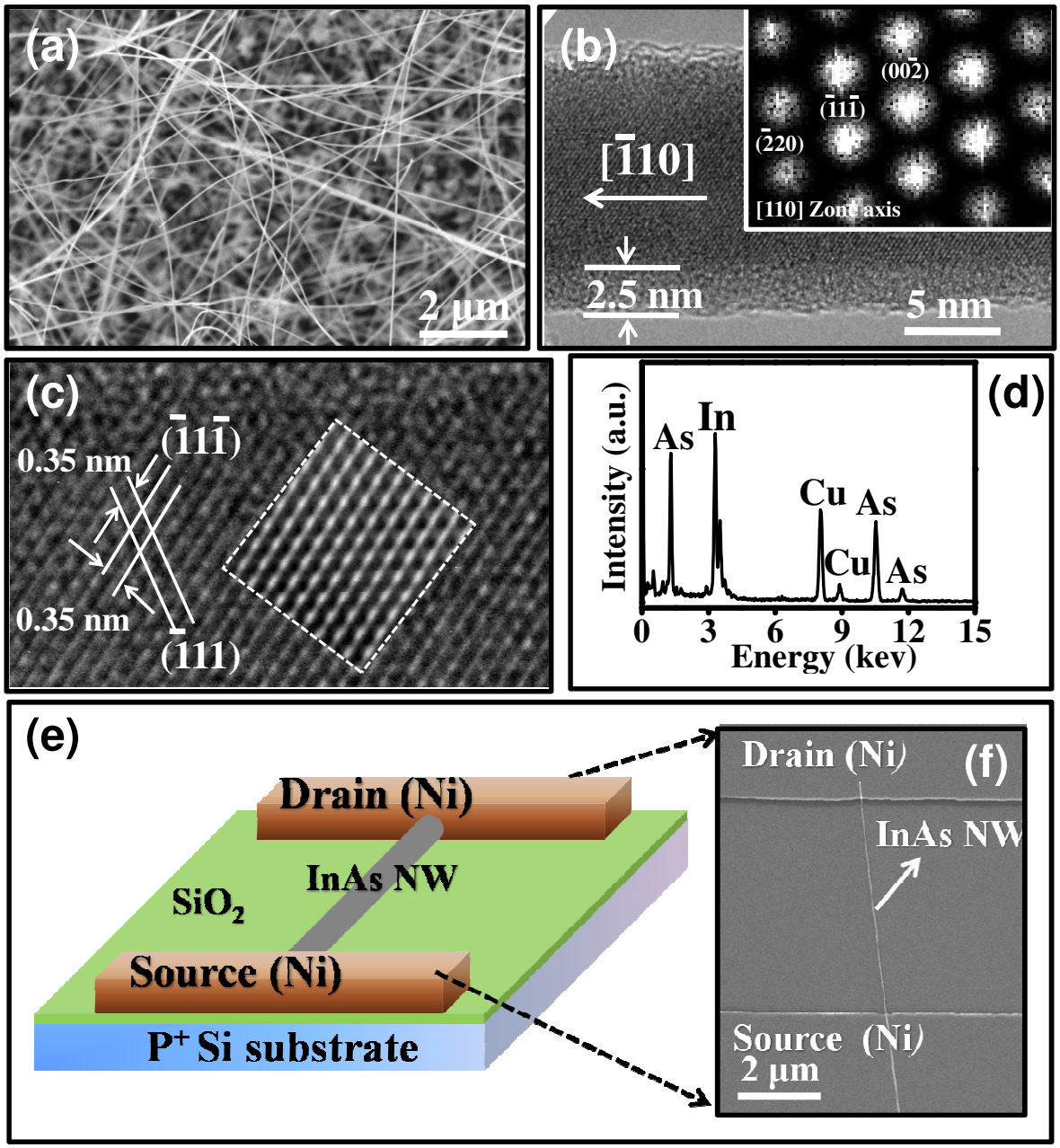

Figure 20. Electron microscopy characterization of InAs nanowires. (a) SEM image of InAs nanowires grown on a SiO_2/Si substrate using Ni nanoparticles as the catalyst. (b) TEM image of a representative InAs nanowire. The inset shows the corresponding diffraction pattern converted by fast-Fourier transform where the zone axis of [110] can be identified. (c) The corresponding high resolution TEM image taken from the nanowire in (b). (d) The EDS analysis shows that the chemical composition of In:As is nearly 1:1. (e) A top-view schematic of a global back-gated nanowire FET, used for the *I-V* characterization. (f) SEM image of a representative back-gated nanowire FET.

In this configuration, the p^+ Si substrate serves as the global back-gate with a gate dielectric thickness of t_{ox}~50 nm SiO_2. To ensure an ohmic contact formation, a 5sec HF etch (~0.1%) was applied immediately prior to the Ni contact evaporation to remove the native oxide on the exposed nanowire surfaces. Additionally, the fabricated devices were annealed at 250ºC for 1 min to further improve the contact properties.[77]

Electrical properties of representative FETs with nanowire radius r=7.5-17.5 nm are shown in Figure 21. Long channel lengths, L=6-10 μm, were used for this study in order to ensure diffusive transport of carriers (rather than ballistic or quasi-ballistic transport), from which intrinsic transport properties, such as carrier mobility, can be extracted. Although the nanowires were not intentionally doped, as expected, the devices exhibit an *n*-type behavior due to the high electron concentration of "intrinsic" InAs. For the channel lengths and nanowire diameters investigated in this study, a linear dependence of the device resistance as a function of channel length is observed which indicates ohmic metal source/drain contacts (Ni) to the InAs nanowires. From the *I-V* characteristics (Figure 21b-d), it is clear that larger diameter nanowires exhibit higher *ON* currents and more negative threshold voltages. Unit length normalized *ON* currents (V_{DS}=2 V and V_{GS}-V_t=6 V) of ~40, 110, and 140 μA-μm are obtained for nanowires of radius r=7.5, 12.5, and 17.5 nm, respectively. This trend can be attributed to a larger cross-sectional area (i.e. effective channel width) for large diameter nanowires, but could also be indicative of reduced carrier scattering with increasing diameter. To better understand this trend, investigation of the electron transport properties as a function of nanowire radius is needed. Electron mobility, μ_n, is an important figure of merit because it relates the drift velocity of electrons to an applied electric field. However, accurate and direct measurement of the gate oxide capacitance is needed for the extraction of field-effect mobility from *I-V* characteristics.

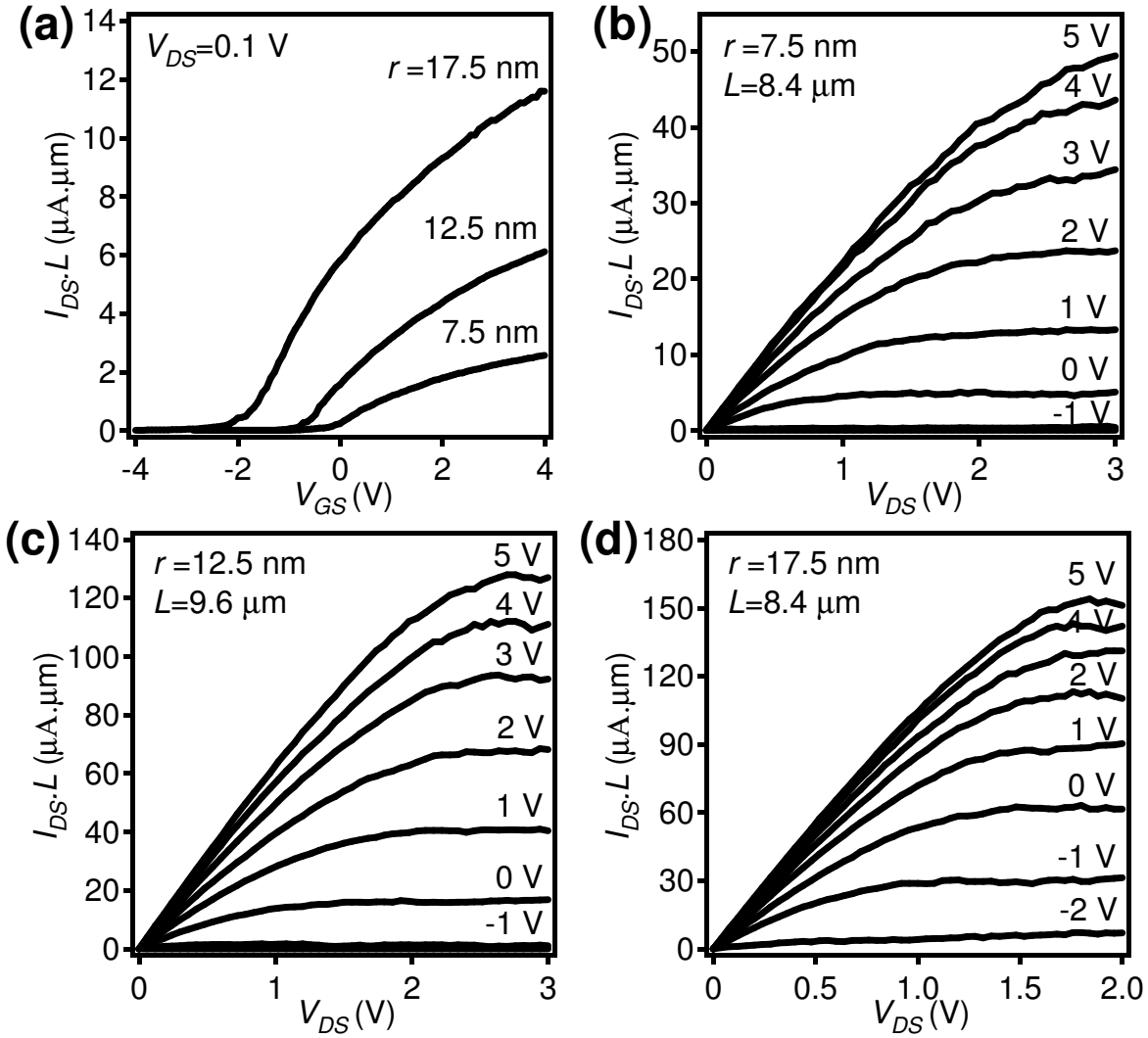

Figure 21. *I-V* characterization of InAs nanowire FETs. (a) Device output characteristics normalized for channel length (I_{DS}.L-V_{GS}) at V_{DS}=0.1 V for three separate long channel devices (L=8.4, 9.6, and 8.4 μm, respectively) with nanowire radii of r=17.5, 12.5, and 7.5 nm, respectively. The 2.5 nm oxide shell was subtracted from the measured nanowire radius. Length normalized I_{DS}.L-V_{DS} plots for various V_{GS} for the (b) 7.5 nm, (c) 12.5 nm, and (d) 17.5 nm radius nanowire devices. The nanowire diameter for each device was measured by AFM or SEM. All measurements were conducted in vacuum and have minimal hysteresis.

In order to determine the gate oxide capacitance of nanowire FETs, and to better understand the density and characteristics of the surface/interface trap states and fixed charges, direct *C-V* measurements were performed on single-InAs nanowire devices at various temperatures. Previously, the only reported *C-V* measurements for InAs nanowire FETs have been for parallel arrays of nanowires (>100 vertical NWs per device) and at room temperature.[78] For this work, temperature-dependent *C-V* of single-nanowire devices with known nanowire radius are required to minimize the averaging effects and understand the properties of individual

nanowires. Here a method previously developed by S. Illani, et al. was used in order to measure the small capacitance signal (10aF-1fF) for nanowire FETs over a large background parasitic capacitance (~30fF).[70] A similar method was also used in the past by R. Tu, et al. to examine the gate oxide capacitance of single Ge nanowire-FETs.[79] As depicted in Figure 22a, buried-gate InAs nanowire FETs with t_{ox}~60 nm, S/D length L_{SD}~10 μm, and buried-gate length L_{LG}~5 μm were fabricated. First, ~225nm thick SiO_2 was grown on top of a p^+ Si substrate by wet oxidation at 1000°C for 27 min 30 sec. The local gates (LG) were then defined by photolithography, 60 sec 10:1 HF etch, DI water rinse, Ti/Pt evaporation (~1 nm/24 nm thick), and lift-off. The oxide etching and metal evaporation steps were well controlled to ensure the flatness of the local gate fingers with the nearby oxide regions. After this, 60 nm thick low-temperature oxide (LTO) was grown by LPCVD at 400°C for 4 min 30 sec and annealed at 700°C in forming gas for 5 min. InAs nanowires were then dropcast onto the sample. Metal source/drain (S/D) contacts were defined by photolithography, Ni evaporation (~50 nm thick), and lift-off. A 5sec HF etch (~0.1%) was applied immediately prior to the Ni evaporation to remove the native oxide in the control regions. Finally, the fabricated devices were annealed at 250ºC for 1 min to further enhance the contact properties.

The relatively long (~2.5 μm) underlapped region on each side of the local-gate (LG) reduces the parasitic capacitance between the local gate LG and S/D, allowing the direct measurement of the nanowire/LG capacitance. The two underlapped nanowire segments effectively work as nanoscale contacts to the nanowire channel with their conduction being modulated by the global back-gate (GG, i.e. p^+ Si substrate) potential. The capacitance measurements were carried out with a capacitance bridge (Andeen-Hagerling, model 2700A) in a variable temperature cryogenic probe station (Lakeshore, model TTPX). During the *C-V* measurements, S/D electrodes were electrostatically grounded, and a constant bias of V_{GG}=2V was applied to the global back-gate GG to turn *ON* the underlapped regions while the charge in the nanowire channel was modulated by the local gate LG voltage, V_{LG}. The background capacitance was measured by applying a negative bias to the global back-gate GG, V_{GG}=-5V, in order to turn *OFF* the underlapped nanowire segments to enable the accurate extraction of the capacitance, C_{LG} as a function of V_{LG}.

Figure 22b shows the temperature dependency of the *C-V* characteristics for a representative InAs nanowire-FET (r~11nm, L_{LG}=4.7μm, L_{SD}=9.3μm) obtained with an AC signal of 125mV at 2kHz. For this device, a flat-band voltage of V_{FB}~0V (corresponding to the on-set voltage of the sharp decrease in the measured capacitance) is observed, with V_{LG}>V_{FB}~0V resulting in the accumulation of electrons in the *n*-type InAs channel (i.e. *ON* state). This is in contrast to the operation mode of conventional MOSFETs in which the *ON* state corresponds to the inversion of the channel (rather than accumulation). The gate capacitance value obtained in the accumulation regime corresponds to the oxide capacitance, $C_{LG,accumulation}$=C_{ox}, which is temperature independent. When V_{LG} <V_{FB} (i.e., V_{LG}<0 V), the channel is depleted of electrons, thus resulting in the reduction of the total gate capacitance due to the addition of the semiconductor capacitance, C_s, in series with C_{ox} (i.e., $C_{LG,depletion}$ = C_{ox} C_s / (C_{ox}+C_s)). In this state, the nanowire channel is effectively turned *OFF*. The temperature dependent *C-V* measurements illustrate two important effects (Figure 22b). First, a shift in V_{FB} is observed as a function of temperature which can be attributed to the change in the population density of the thermally activated, donor-like fixed charges, N_s cm^{-2} (near the conduction band edge), at the nanowire surface/interface. Second, the capacitance in the depletion region is greatly reduced as the temperature is lowered from 200K to 150K, but relatively unchanged after that. This trend is

a clear signature of thermally activated, surface/interface traps (D_{it}) as they induce a capacitance, C_{it}, in parallel to C_s (Figure 22a). This effectively increases $C_{LG,depletion}$. For this case, the gate capacitance in the depletion regime is given as, $C_{LG,depletion} = C_{ox}(C_s+C_{it}) / (C_{ox}+C_s+C_{it})$. Below 150K, the measured depletion capacitance is independent of temperature, indicating that the traps stop responding.

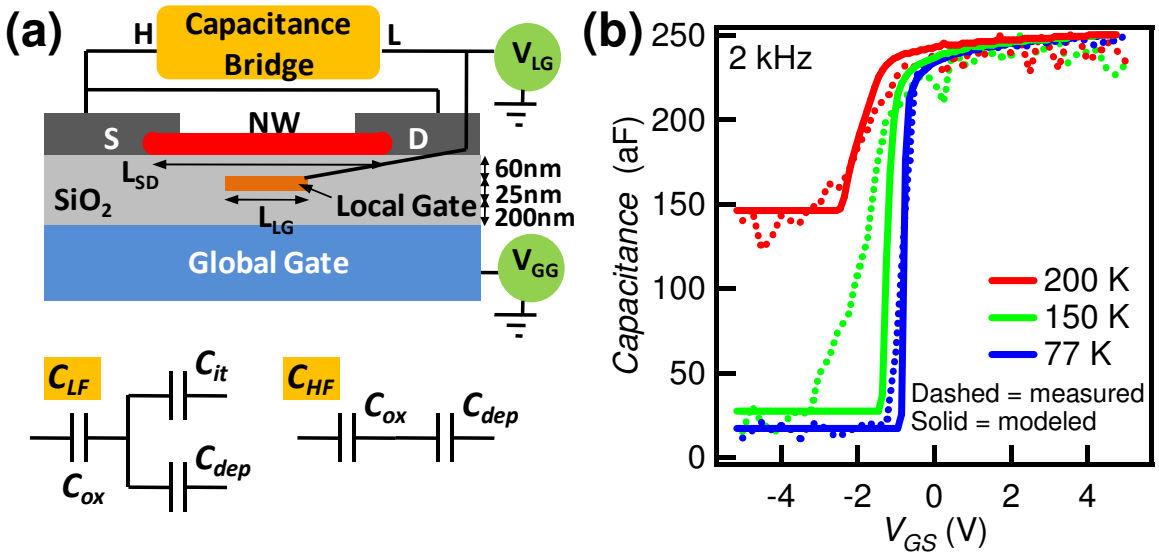

Figure 22. *C-V* characterization of InAs nanowire-FETs. (a) Schematics for *C-V* measurement of a single nanowire device (top) and the equivalent capacitance circuits in the depletion regime for low frequency (LF) and high frequency (HF) measurements (bottom). H and L represent the "high" and "low" terminals of the bridge, respectively. (b) Temperature dependent *C-V* characteristics for a local-gated nanowire FET with *r*~11 nm and L_{LG}~4.7 μm. Electrostatic modeling is also applied and fitted to all measurements for the normalized gate capacitance.

Based on this analysis, a C_s~10.5 aF and C_{it}~0, 11.3, 316 aF at 77, 150, 200K, respectively, was extrapolated. Beside *C-V* measurements at 2kHz, measurements at a higher frequency of 20kHz were performed in order to investigate the surface/interface traps. At high frequencies, it is expected that the traps would not have enough time to charge and/or discharge, and so would not affect the *C-V* characteristics. Similar C_{it} values with D_{it}~2×10^{11} states $cm^{-2}eV^{-1}$ at 200K were obtained from frequency-dependent measurements of 2 and 20kHz.

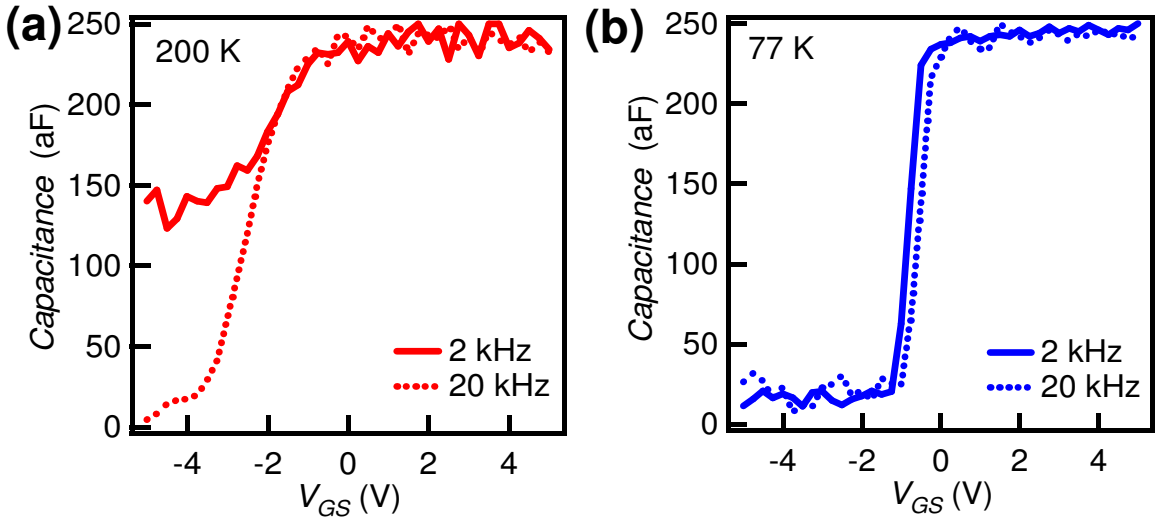

Figure 23. *C-V* characterization of InAs nanowire-FETs at two different temperatures and frequencies. (a) *C*-V characteristics for two different measurement frequencies (2kHz and 20kHz) at 200K. This data is for the same device as that of Figure 22. (b) *C*-V characteristics for two different measurement frequencies (2kHz and 20kHz) at 77K for the same nanowire device shown in (a) and Figure 22.

Figure 23 demonstrates the frequency dependence of *C-V* for the same nanowire FET at 200K and 77K, respectively. At 200K, similar capacitance values are obtained in the accumulation regime for both high (HF) and low frequency (LF) measurements. This is expected since C_{ox} does not exhibit any dependence on the operation frequency. However, the depletion regime exhibits a large frequency-dependent response. The frequency dependent response of the capacitance in the depletion region is attributed to C_{it} with a density of surface/interface traps of $D_{it} = \frac{C_{LF} - C_{HF}}{q\left(1 - \frac{C_{LF}}{C_{ox}}\right)\left(1 - \frac{C_{HF}}{C_{ox}}\right)2\pi r L_{LG}}$, where C_{LF} and C_{HF} are the low and high frequency gate capacitances, respectively.[80] From this analysis, C_{it}~335aF and D_{it}~2x10^{11} states cm^{-2}eV^{-1} are extracted at 200K, both of which are consistent with the values obtained from the temperature dependent analysis previously described. At 77K, there is no obvious difference between the HF and LF *C-V* characteristics in the accumulation or depletion regimes, suggesting that the majority of traps are frozen out. The maximum and minimum frequencies of 20kHz and 2kHz used in this study were the limits of the instrumentation set up, as at lower frequencies, inadequate signal to noise was attained while the capacitance bridge was limited to 20kHz in operation. 2kHz may not present the true low frequency operation regime as some traps may already be irresponsive at that frequency. Because of this, the extracted D_{it} values only represent a lower bound limit. *C-V* measurements at temperatures higher than 200K could not be performed due to the thermal noise and leakage currents of low band-gap (E_g~0.36 eV) InAs nanowire channels (resulting from the band-to-band thermal generation of carriers).

Electrostatic modeling was also performed to investigate the effect of fixed charges and trap states on the *C-V* characteristics. A two-dimensional Poisson equation was self-consistently solved with the equilibrium carrier statistics for the InAs nanowire and the native oxide layer for a cross section perpendicular to the nanowire axis. Both N_S and D_{it} were treated as the fitting parameters in the simulation. A close fit of the experimental data for the normalized gate capacitance, as shown in Figure 22b, is obtained when assuming N_s=0, 1.5x10^{11}, 4.5x10^{11} states cm^{-2} and C_{it}=0, 17.4, 344 aF for 77, 150, 200 K, respectively, which is consistent with the values extrapolated from the analytical expressions described above. When quantum effects are taken into consideration by self-consistently solving the Poisson and Schrödinger equations in the quantum simulation, it is found that quantum effects decrease the semiconductor capacitance by shifting the centroid of the charge away from the nanowire surface. However, since the gate oxide thickness is much larger than the nanowire radius (~3 to 7 times larger) in the InAs nanowire FETs, the quantum effects on the total gate capacitance are relatively small.

In addition to the characterization of C_{it} and D_{it}, C_{ox} was directly measured as a function of nanowire radius. Figure 24 shows the experimentally obtained C_{ox} for different nanowire-FETs with r=10-20 nm. Electrostatic modeling of the oxide capacitance values by using the finite element analysis software package Finite Element Method Magnetics was also performed (Figure 24). The measured and modeled capacitance values are in qualitative agreement, with the experimental values ~25% higher than the modeled results. This discrepancy is likely due to the infringing capacitances between the local gate LG and the underlapped nanowire segments which were ignored in the simulation and/or the geometric uncertainties associated with the fabricated nanowire-FETs (i.e. the exact thickness of the gate oxide deposited on Pt LGs). Additionally, C_{ox} was calculated from the analytical expression, $C_{ox} = \frac{2\pi\varepsilon\varepsilon_0 L}{\cosh^{-1}[(r+t_{ox})/r]}$, which corresponds to the capacitance of a cylindrical wire on a planar substrate and is often used in the literature for nanowire device analysis.[81,82,83,84,85] Here, ε is the dielectric constant of the gate insulator (ε=3.9 for SiO_2) and ε_0 is the permittivity of free space. The capacitance values obtained from this analytical expression are ~2x higher than the experimental values (Figure 24), demonstrating the lack of accuracy of this analytical method for nanowire-FET analysis.

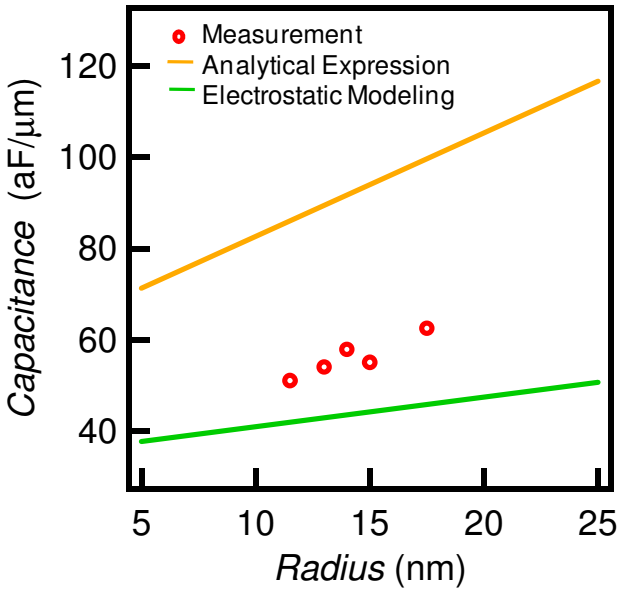

Figure 24. Measured and simulated gate oxide capacitance as a function of radius per unit of local buried gate length. For the simulation, a semiconductor nanowire with ε=15 was assumed. Additionally, the capacitance values obtained from the analytical expression of $C_{ox} = \frac{2\pi\varepsilon\varepsilon_0 L}{\cosh^{-1}[(r+t_{ox})/r]}$ are shown.

From the *C*-*V* and *I*-*V* measurements, the field-effect electron mobility of the InAs nanowire FETs is extracted by using the low-bias (V_{DS}=0.1 V) transconductance, $g_m = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{V_{DS}}$, and the analytical expression, $\mu_{n,FE} = g_m \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{DS}}$. Figure 25a shows $\mu_{n,FE}$ as a function of V_{GS} for three nanowires of different radius, corresponding to the I_{DS}-V_{GS} plots of Figure 21. The peak field-effect mobility is higher for larger diameter nanowires with $\mu_{n,FE}$ ~2,500, 4,000, and 6,000 cm^2/Vs for r~7.5, 12.5, and 17.5 nm, respectively. The $\mu_{n,FE}$-V_{GS} characteristics for all measured nanowire-FETs exhibit a near identical behavior with the field-effect mobility at first increasing with V_{GS}-V_t before sharply decaying at high electric fields. This decay is due to the enhanced surface scattering of the electrons at high gate fields, similar to the behavior that is observed in conventional Si MOSFETs. Additionally, in quasi-1-dimensional (1-D) nanowires, due to the quantization of sub-bands, the metal contacts may not allow sufficient injection of electrons into the channel at high electric-fields as desired by the gate potential. Because of the finite sub-band energy spacing, Schottky barriers to the higher sub-bands may form at the nanowire-metal contact interfaces, thereby lowering the transconductance and the mobility of the FETs at high gate voltages.

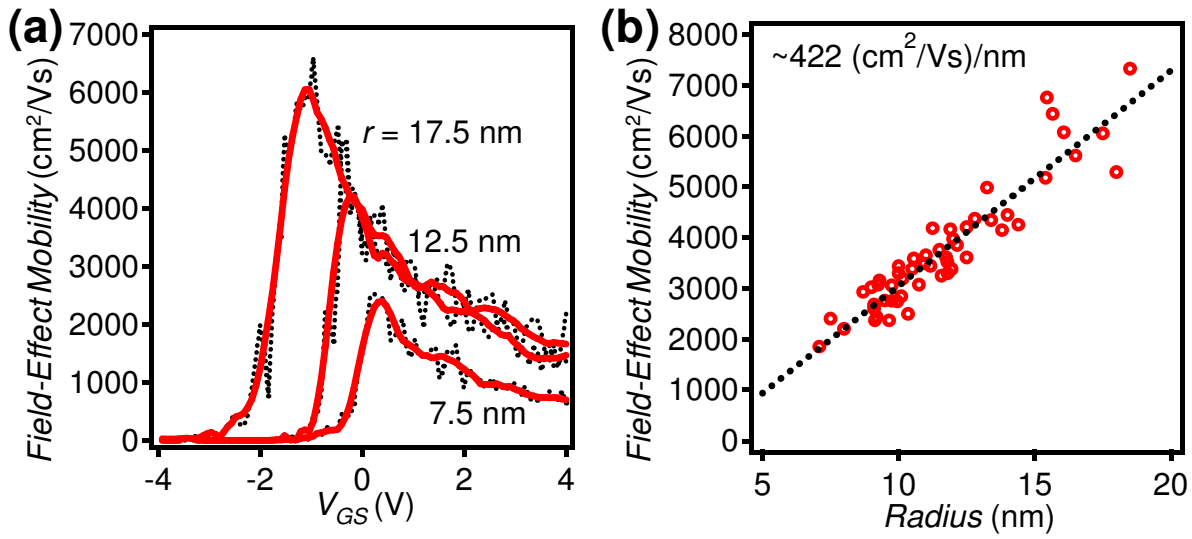

Figure 25. Room temperature field-effect mobility. (a) Field-effect mobility as a function of V_{GS} for three nanowires of different radius (r=17.5, 12.5, and 7.5 nm), corresponding to the I_{DS}.L-V_{GS} plot of Figure 21a. (b) Peak field-effect mobility as a function of radius for more than 50 different devices with nanowires ranging from 7-18 nm in radius post oxide subtraction. Over this nanowire radius range, the peak field-effect mobility linearly increases with radius, closely fitting the linear expression $\mu_{n,FE}$=422r-1180. The I_{DS}-V_{GS} plots were smoothed before the transconductance, g_m was calculated for field-effect mobility extraction.

While the nanowires used in this study may seem rather large to exhibit quantization effects, due to the large Bohr radius of InAs (~34 nm), even a r=10 nm nanowire can be treated as quasi 1-D because the confinement energies for the lowest and second lowest sub-bands are ~100 and 240 meV, respectively (Figure 26).[86] Here an electron effective mass of 0.023m_e was used. A two-dimensional Schrodinger equation was solved for the cylindrical cross section of the nanowire to obtain the sub-bands, and the density-of-states is subsequently computed by the summation of the density of states over all the sub-bands. Electron wave penetration from the InAs nanowire to the oxide is neglected. The result shows that the sub-band spacing is larger than the room temperature thermal energy even for a nanowire with a 20nm diameter.

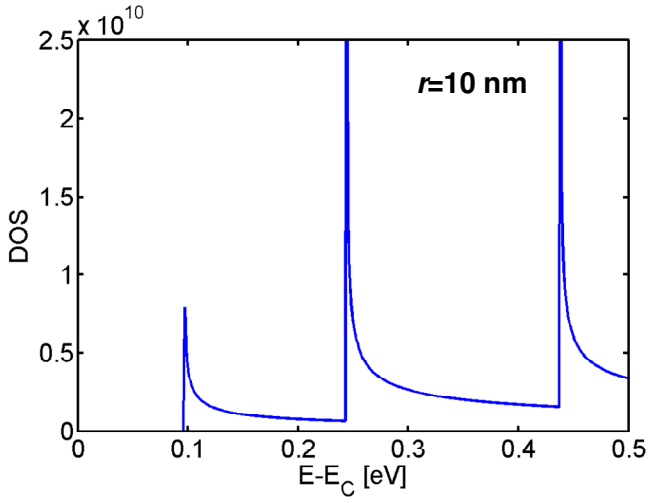

Figure 26. The computed density-of-states (DOS) for an InAs nanowire with a radius of 10nm.[86]

Figure 25b illustrates the peak field-effect mobility as a function of InAs nanowire radius for more than 50 different FETs with r=7-18 nm. Over this nanowire radius range, the peak field-effect mobility linearly increases with radius with a slope of ~422 (cm^2/Vs)/nm. Nanowires with larger or smaller radii beyond the range shown here were not investigated due to the difficulty with their growth using the condition described in Chapter 2. The linear drop in the field-effect mobility with reducing nanowire radius may be attributed to a number of factors, including the enhanced phonon-electron wavefunction overlap (i.e. enhanced phonon scattering of electrons), the increased surface scattering, enhanced defect scattering, and the lower effective gate coupling factor due to the surface states (D_{it}) for smaller nanowires with higher surface area to volume ratio.[87] Additionally, a diameter dependent contact resistance might be expected which could also affect the extracted field-effect mobility.[88] However, this appears not to be a factor here since for the diameters and lengths investigated here, there is a linear dependence of the *ON*-state resistance as a function of the channel length. Therefore, the main source of the total device resistance is due to the channel resistance.

It should be noted that the electron mobility reported here is the field-effect mobility, which is different from the effective mobility and the Hall mobility. Hall mobility represents the bulk carrier transport with no major contributions from the surface and quantization effects, while both the field-effect and effective mobilities are used to characterize the carrier transport in the surface inversion (or accumulation, in the case of InAs nanowires) layer of the MOSFETs. However, the field-effect and effective mobilities are extracted from the *I-V* characteristics by using different analytical models. The effective mobility is extracted using the drain conductance, $g_D = \left.\frac{dI_{DS}}{dV_{DS}}\right|_{V_{GS}}$ with $\mu_{n,eff} = g_D \times \frac{L^2}{C_{ox}} \times \frac{1}{(V_{GS} - V_t)}$. On the other hand, as described above, the field-effect mobility is extracted using the transconductance, g_m. Therefore, the main difference between the field-effect and effective mobility is the neglect of the gate electric-field dependence in the field-effect mobility expression.[89] For device modeling, effective mobility is typically used to predict the current and switching speeds. A difficulty in the accurate extraction

of the effective mobility results from the error associated with finding V_t from the measured *I-V* characteristics. Therefore, for the purpose of this study, the field-effect mobility is presented. However, when the effective mobility is used, a similar diameter dependence for the peak mobility is observed for the InAs nanowires (Figure 27).

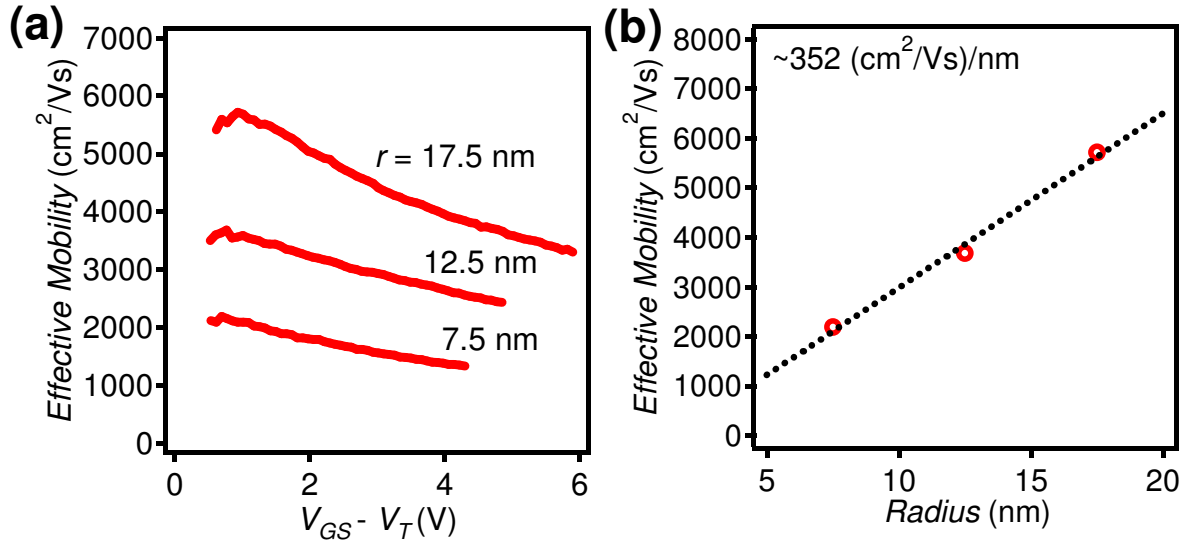

Figure 27. Room temperature effective mobility. (a) The effective mobility extracted for the devices shown in Figures 21 and 25. (b) Peak effective mobility as a function of nanowire radius for the three devices shown in (a).

Here, the effective mobility was extracted from the I_{DS}-V_{GS} characteristics (Figure 21a) by using, $\mu_{n,eff} = g_D \times \frac{L^2}{C_{ox}} \times \frac{1}{(V_{GS} - V_t)}$, where $g_D = \left.\frac{dI_{DS}}{dV_{DS}}\right|_{V_{GS}}$. The threshold voltage V_t is extrapolated from the I_{DS}-V_{GS} characteristics. For a constant V_{DS} in the linear regime (i.e. V_{DS}=0.1 V), g_D is just $\frac{I_{DS}}{V_{DS}}$, so the effective mobility can be extracted for each gate voltage as shown in Figure 27a. The effective mobility at first increases with the vertical electric field due to a decrease in the Coulomb scattering, but then decreases for large vertical fields due to the enhanced surface scattering and contact resistance associated with the Schottky barriers to the higher sub-bands. It should be noted that the above analytical expression for effective mobility is not accurate for V_{GS}-V_t<0.5, so only the effective mobility for the larger V_{GS}-V_t is shown. The C_{ox} values used to calculate the effective and field-effect mobilities were taken from a fit line of the experimental data.

In an effort to understand the source of mobility degradation for smaller nanowires, temperature-dependent electron transport measurements were performed (Figure 28). Typical I_{DS}-V_{GS} plots at V_{DS}=0.01 V for a back-gated nanowire device with r=18 nm and L=6.7 μm are shown in Figure 28a over a temperature range of 50-298 K. Figure 28b shows the corresponding peak field-effect mobility as a function of temperature for this device, showing a linear enhancement of the peak electron field-effect mobility from ~6,000 to 16,000 cm^2/Vs as the temperature is dropped from 298 K to 200 K. Below ~200K, minimal change in the field-effect

mobility is observed. This can be attributed to the transition temperature at which the surface roughness scattering becomes dominant over other scattering events caused by acoustic phonon and/or surface/interface trap states. Additionally, at lower temperatures, since the surface trap states are fully frozen, they should not have an impact on the gate coupling factor.

The dependency of field-effect mobility on the nanowire radius was also investigated at different temperatures. The data for four nanowire FETs with r=8-20 nm at 298K and 50K is shown in Figure 28c. Even at low temperatures (50 K), in the regime where phonons and surface/interface traps are frozen out, the monotonic increase of mobility with radius is evident. At 50 K, a near-linear trend is observed for small radius nanowiress (i.e. $r \leq 12$ nm, with a slope of ~2077 (cm^2/Vs)/nm) with the field-effect mobility approaching a saturation value of ~18,000 cm^2/Vs for larger nanowires (i.e. r>18 nm). The phonon contribution is drastically reduced at 50 K, so the acoustic phonon scattering for low-field transport can be assumed to be non-existent. Additionally, most surface/interface traps are frozen out at such low temperatures and should not affect the gate electrostatic coupling or the electron transport properties near the surface. Impurity scattering should not be a factor since the nanowires are not intentionally doped. As a result, the observed dependence of electron field-effect mobility on nanowire radius at 50K is primarily due to the enhanced surface roughness scattering of electrons in smaller radius nanowires. For smaller radius nanowires, electron transport near the surface dominates the electrical characteristics. However, the atomic roughness of the surface results in increased carrier scattering, thereby lowering the carrier mobility. Because the surface roughness scattering rate depends on the surface-area to volume ratio, a near linear dependence of μ_n on radius for smaller diameter nanowires is expected. Since surface roughness scattering is nearly independent of temperature, the difference between the observed trends at 50K and 298K results from a combination of phonon scattering, surface/interface traps, and fixed charges that contribute to additional surface scattering and lower gate coupling.

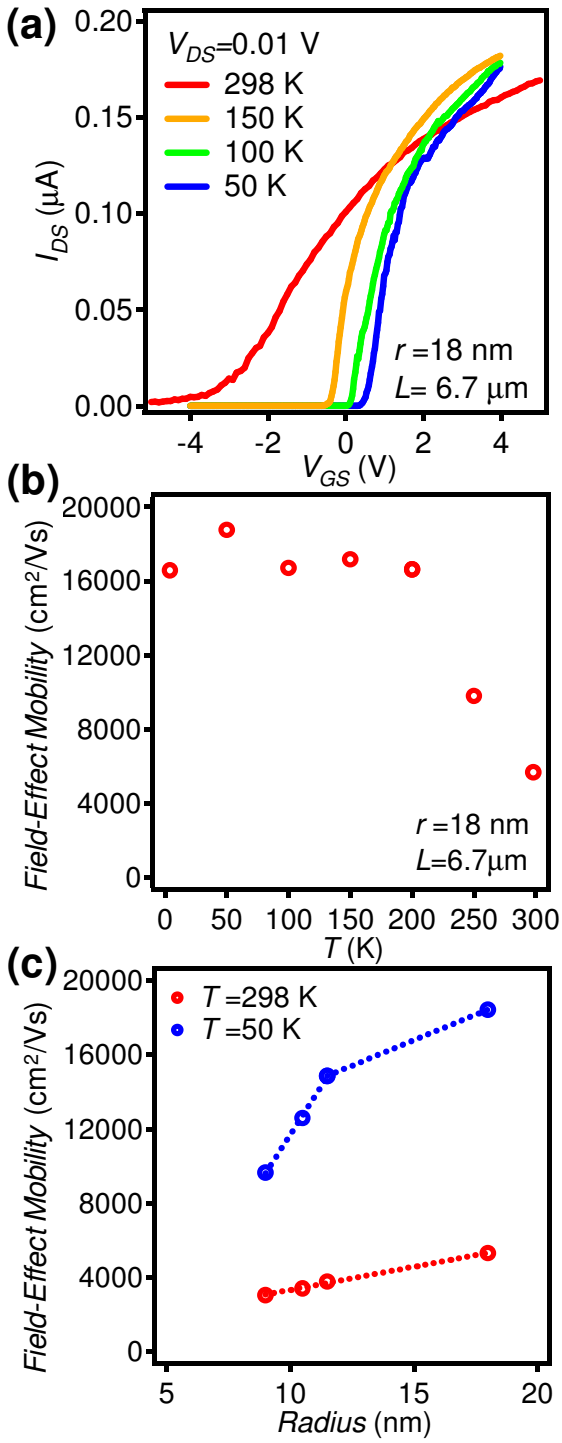

Figure 28. Temperature dependent InAs nanowire electron transport properties. (a) I_{DS}-V_{GS} at V_{DS}=0.01 V for a representative nanowire FET with r=18 nm and L=6.7 μm over a temperature range of 50-298 K. (b) The corresponding peak field-effect mobility as a function of temperature for the same device. (c) The dependence of field-effect mobility on radius for four nanowires of different radius at temperatures of 50 and 298 K.

Further analysis of the scattering events discussed above is needed to give more quantitative understanding of the role of each scattering mechanism for a given nanowire radius and temperature range. Additionally, the electron effective mass may increase with diameter reduction which could also have an impact on the diameter dependence of the mobility. Clearly the results presented here demonstrate the dramatic effect of nanowire radius on the field-effect mobility. This is of concern since small diameter nanowires (r<~10 nm) are more desirable for the channel material of future sub-10 nm FETs since they allow improved gate electrostatic control of the channel and lower leakage currents. However, this work suggests that the aggressive diameter scaling of nanowires may only be obtained at the cost of field-effect mobility degradation, thereby requiring device design considerations for achieving the best device performance. Additionally, improving the surface properties is necessary for enhancing the electron transport and electrostatics of InAs nanowire FETs.[90] A similar approach of using *C-V* and *I-V* characterization may be used in the future to study the role of surface functionalization or high-κ gate dielectrics on the electrical properties of InAs nanowire FETs.

3.4. InAs Nanowire Array Devices

To further investigate the electrical properties and uniformity of the Ni-catalyzed InAs nanowires, a contact printing approach to controllably transfer and assemble parallel arrays of nanowires on Si/SiO_2 substrates over large areas with an average pitch of ~0.5 μm was used.[7] Poly-*L*-lysine (0.1%w/v in H_2O, Sigma-Aldrich) was applied to the receiver substrate prior to the printing process to improve the nanowire-substrate chemical interactions and yield a higher nanowire density. Octane:mineral oil (2:1 v/v) was used as a lubricant for the printing process to reduce nanowire-nanowire friction and allow for controlled transfer of aligned nanowires. Following nanowire printing, back-gate FETs were fabricated based on the printed InAs nanowire arrays by using Ni (~50 nm) source/drain (S/D) metal contacts and 50 nm thermal oxide as the gate dielectric. Figure 29a shows an SEM image and device schematic of a printed InAs nanowire device. The electrical properties of a representative FET made from an array of printed InAs nanowires (width~200 μm and channel length L~3 μm) are shown in Figure 29b and c. The transistor has an *ON* current of ~6 mA at V_{DS} = 3V, which corresponds to ~15 μA per nanowire (~400 nanowires bridging S/D) with I_{ON}/I_{OFF} ~100. The transconductance $g_m = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{V_{DS}}$ was obtained from the I_{DS}-V_{GS} curve for V_{DS} = 0.1V and the analytical expression $\mu_{n,FE} = g_m \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{DS}}$ was used to calculate the field-effect mobility $\mu_{n,FE}$, where L is the channel length and C_{ox} is the gate oxide capacitance. The gate oxide capacitance was approximated by two different methods. As an upper bound estimate for C_{ox} (therefore, a lower bound estimate for the field-effect mobility), the parallel plate capacitor model $C_{ox} = (\varepsilon\varepsilon_0 A)/d$ was used. Here ε is the dielectric constant of the oxide (3.9 for SiO_2), ε_0 is the permittivity of free space, A is the channel area (width ~200 μm x length ~3 μm), and d is the thickness of the gate dielectric (~50 nm). This model gives C_{ox} = 4.14x10^{-13} F and $\mu_{n,FE}$ = 92 cm^2/Vs for the parallel array InAs nanowire FETs. A lower bound estimate for C_{ox} (upper bound estimate for the field-effect mobility) was found by multiplying the electrostatically modeled gate oxide capacitance for a single InAs nanowire (C_{ox} ~0.16x10^{-15} F assuming an average nanowire

diameter of ~27 nm and L = 3 μm) by the number of nanowires in the array FET (~400). This gives C_{ox} = 6.49x10^{-14} F and $\mu_{n,FE}$ = 587 cm^2/Vs (Figure 29d).

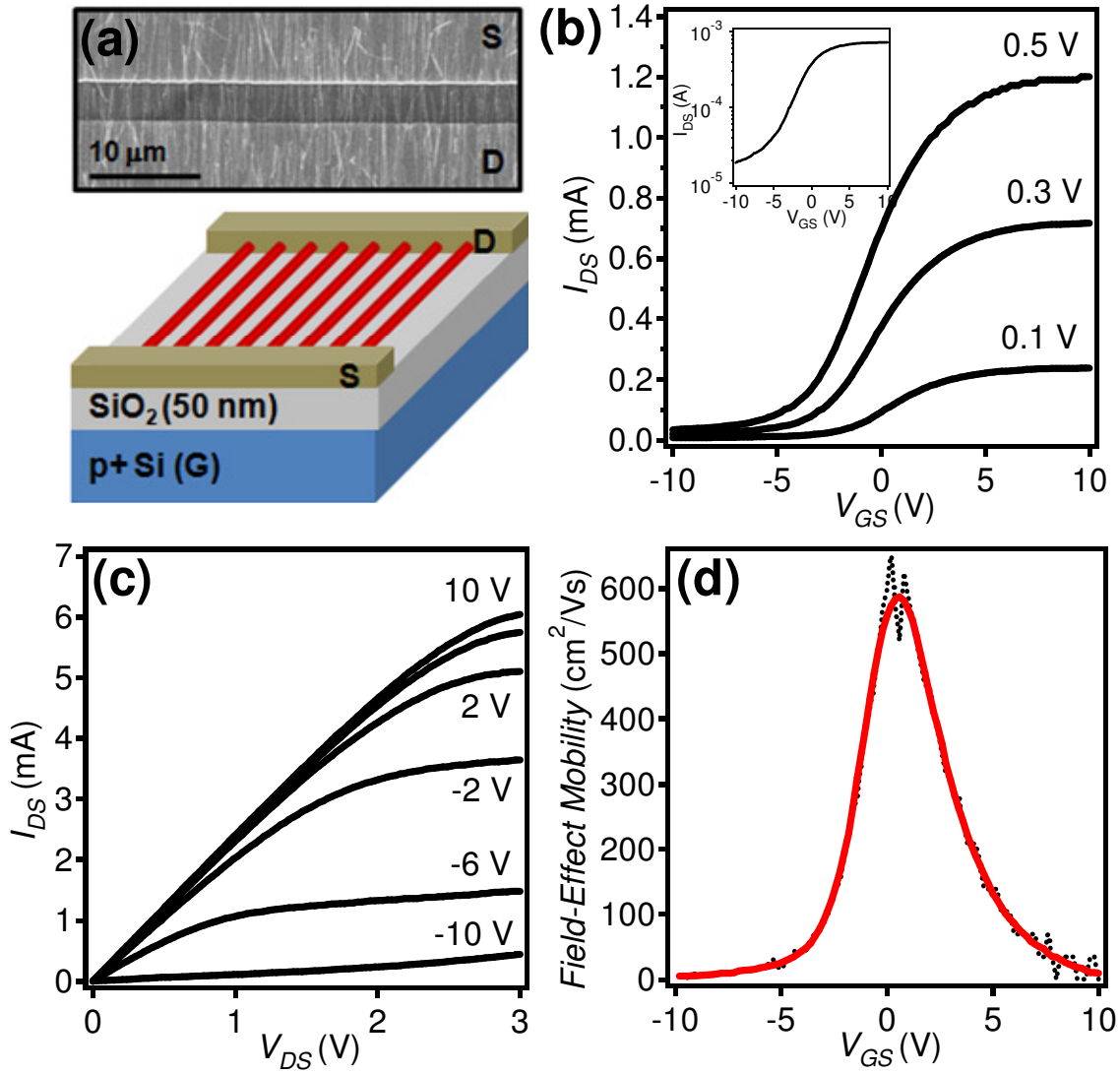

Figure 29. Contact printed InAs nanowire array devices. (a) An SEM image and a device schematic of a back-gated FET fabricated on a printed, parallel array of InAs nanowires. (b) Linear scale, transfer characteristics of a representative FET with *W*~200 μm (~400 NWs bridging S/D) and *L*~3 μm at V_{DS} = 0.1, 0.3, and 0.5 V. The inset shows the log scale I_{DS}-V_{GS} curve for V_{DS} = 0.3 V. (c) Output characteristics of the same device at various V_{GS}. (d) Field-effect mobility-V_{GS} curve extracted using the low-bias (V_{DS} = 0.1V) transconductance and the standard square-law model. The curve corresponds to the same array FET with characteristics shown in (a) and (b).

Since the parallel plate capacitor model assumes (incorrectly) that the printed nanowires form a continuous sheet across the channel, the actual field-effect mobility of the InAs array FET is likely closer to this upper bound field-effect mobility estimate. The field-effect mobilities reported here are much higher than those of organic semiconductors and amorphous Si, which

are typically on the order of ~1cm^2/Vs. This shows the distinct advantage of using crystalline inorganic materials, such as InAs nanowires, as the channel material for high performance printable electronic devices. The parallel-array nanowire FETs demonstrate the possibility of using a printing technology for making high performance devices with potentially high switching speeds. Since during the printing process, all of the InAs nanowires are transferred from the growth substrate to the receiver substrate, the results show the high purity and uniformity of the InAs nanowires grown by using Ni nanoparticles as catalysts. In the future, the nanowire device performance can be enhanced through channel length scaling and integration of high-κ dielectrics in a top-gate configuration.

3.5. Thickness-Dependent Electron Mobility of InAs XOI

Long-channel, back-gate FETs based on single ultrathin body InAs XOI nanoribbons were fabricated in order to study the intrinsic electron transport properties of InAs nanoribbons as a function of thickness. The process involved the fabrication of XOI substrates with the desired InAs thickness as described in Chapter 2 followed by the formation of source/drain (S/D) metal contacts by lithography and lift-off (~50 nm thick Ni). A p^+ Si substrate was used as the global back-gate with a 50 nm thermal SiO_2 as the gate dielectric. Ni contacts were annealed at 225ºC for 5 min in a N_2 ambient to allow the formation of low resistance contacts to the conduction band of InAs. The transfer characteristics at V_{DS}=0.1V of the back-gated XOI FETs with a channel length, L~5 μm and InAs thicknesses of 8-48 nm are shown in Figure 30a. Two trends are evident from the measurements. First, the *OFF* current monotonically increases with increasing thickness due to the reduced electrostatic gate coupling of the back-gate. Second, the *ON* current increases with InAs thickness due to the thickness dependence of electron mobility, μ_n. Since L~ 5μm, the devices are operating in the diffusive regime, which allows for the direct extraction of the field-effect mobility by using the analytical expression $\mu_{n,FE} = g_m \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{DS}}$, where the transconductance $g_m = \left.\frac{dI_{DS}}{dV_{GS}}\right|_{V_{DS}}$ was obtained from the I_{DS}-V_{GS} curve for V_{DS} = 0.1V, L is the channel length, and C_{ox} is the gate oxide capacitance. Figure 31 shows the extracted field-effect electron mobility as a function of V_{GS} for representative XOI FETs with InAs nanoribbon thickness of 8, 13, and 48 nm. The peak field-effect mobility increases with the thickness of InAs as depicted in Figure 30b and 31. It is also evident from the $\mu_{n,FE}$ - V_{GS} plots that the field-effect mobility increases with the gate voltage at first and then decreases at high gate voltages due to the enhanced surface scattering of electrons at high electric fields, similar to conventional MOSFETs.

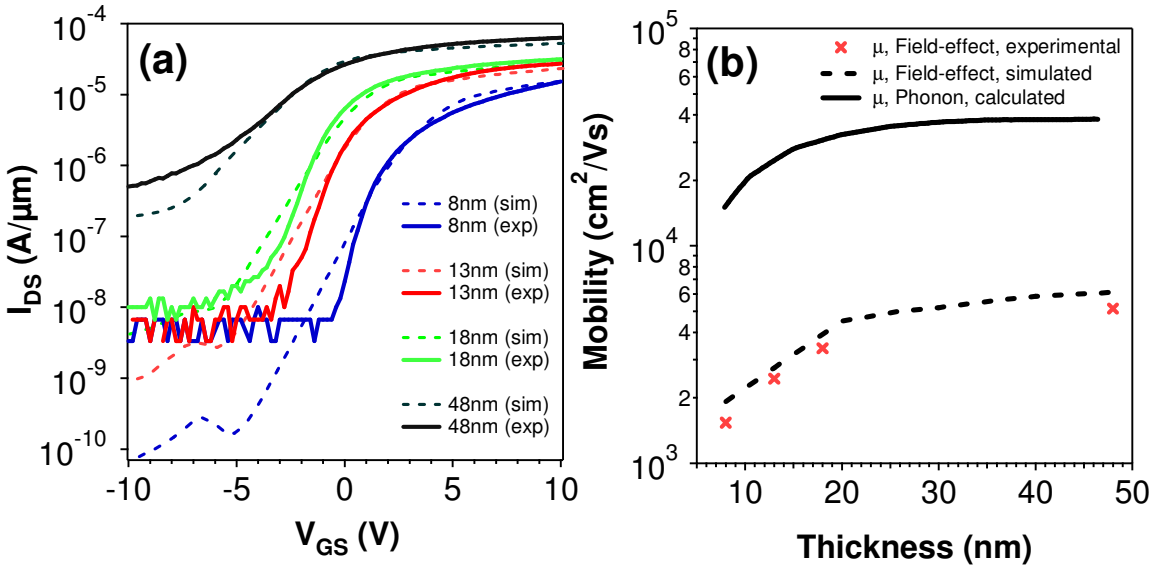

Figure 30. Back-gated, long-channel InAs XOI FETs. (a) The experimental (solid lines) and simulated (dashed lines) I_{DS}-V_{GS} characteristics of back-gated (50 nm SiO_2 gate dielectric) XOI FETs at V_{DS}=0.1V with L~5 μm for different InAs nanoribbon thicknesses (8, 13, 18, 48 nm). Each FET is a single nanoribbon device. (b) The experimental and simulated peak field-effect electron mobilities of InAs nanoribbons as a function of nanoribbon thickness. The calculated phonon mobility is also shown.

For this analysis, parasitic resistances were ignored since Ni forms near ohmic metal contacts. The gate oxide capacitance was estimated from the parallel plate capacitor model $C_{ox} = (\varepsilon A)/d$, where ε=3.9 and d=50 nm are the dielectric constant and thickness of SiO_2, respectively. The effect of quantum capacitance, C_Q was neglected due to the relatively thick gate dielectrics used in this study (i.e. $C_{ox} << C_Q$). Figure 30b shows the peak $\mu_{n,FE}$ as a function of InAs thickness, T_{InAs}. The mobility at first linearly increases with thickness for T_{InAs} < ~18 nm with a slope of ~221 (cm^2/Vs)/nm, after which it nearly saturates at $\mu_{n,FE}$ ~5,500 cm^2/Vs. The measured XOI field-effect mobility is close to the reported Hall mobilities for InGaAs (~10,000 cm^2/Vs) and InAs (13,200 cm^2/Vs) quantum well (QW) structures.[6,62] The Hall mobility is typically higher than the field-effect mobility since device and surface state contributions to carrier transport are not accounted for in the Hall effect measurements.

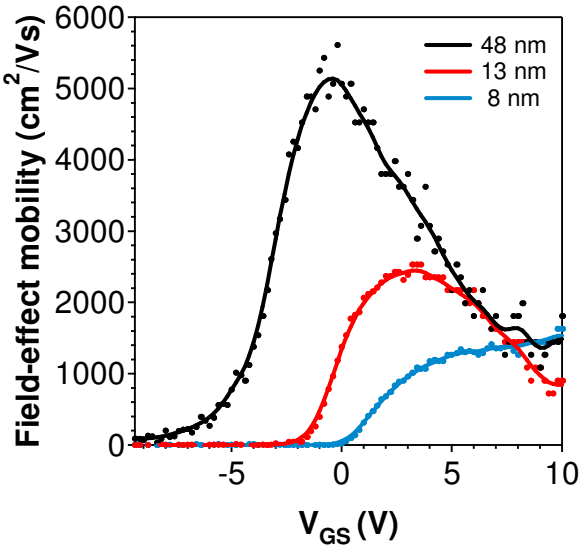

Figure 31. Field-effect mobility of back-gated InAs XOI FETs as a function of V_{GS} for different InAs nanoribbon thickness (8, 13, 48 nm) at V_{DS}=0.1 V. The field-effect mobility is extracted from the measured I_{DS}-V_{GS} curves at V_{DS}=0.1 V (Figure 30a).

To understand the observed mobility trend, the low-field phonon mobility, $\mu_{n,phonon}$ was calculated from $\mu_{n,phonon} = e/(m^* \left\langle 1/\tau \right\rangle)$, where e is the electronic charge and m^* is the effective mass. Average scattering rate $\langle 1/\tau \rangle$ is calculated from $\left\langle \frac{1}{\tau} \right\rangle = \frac{\int \frac{1}{\tau(E)} \frac{\partial f_0}{\partial E} dE}{\int \frac{\partial f_0}{\partial E} dE}$ where f_0 is the equilibrium Fermi-Dirac distribution function. τ(E) was calculated using Fermi's golden rule, with the matrix elements of the scattering potentials evaluated in the basis of the nanoribbon eigenfunctions. Both acoustic and optical (including polar) phonon scattering events were considered. The calculated $\mu_{n,phonon}$ vs. T_{InAs} is shown in Figure 30b. For small thicknesses, the mobility linearly increases with the thickness. This behavior is attributed to the gradual transition of the channel from a 2D to 3D system as the nanoribbon thickness is increased, with more transport modes (sub-bands) contributing to the current flow. As the thickness surpasses the Bohr radius of bulk InAs (~34 nm), the electronic structure of the nanoribbons approaches the 3D regime, resulting in a mobility saturation for T_{InAs}>~35 nm to the bulk value of InAs (~40,000 cm^2/Vs). While the onset thickness of saturation closely matches the experiments, there is 5-10× discrepancy in the actual mobility values. This is expected since the extracted data represents the field-effect mobility, due to phonon scattering along with other device contributions, including interface trap states, surface roughness scattering, and vertical-field-induced mobility degradation. Both surface roughness and vertical-field (gate-field) induce additional carrier scattering events at the surface/interface, while the primary effect of interface trap states is to degrade the modulation of the channel conductance (charge density) by the gate-field. These effects degrade the extracted g_m and $\mu_{n,FE}$. To simulate $\mu_{n,FE}$, a device simulation was performed. An interface trap density D_{it}= 6×10^{12} states $cm^{-2}eV^{-1}$ was used as the fitting parameter. The simulated *I-V* characteristics of XOI back-gated FETs are shown in Figure 30a. The simulated *I-V* curves match the experimental data closely for all InAs thicknesses, especially in the *ON*-state.

Next, peak $\mu_{n,FE}$ was extracted from simulation and plotted as a function of T_{InAs} (Figure 30b), again closely matching the experimental $\mu_{n,FE}$. The close matching of the experimental and simulated results demonstrates the effectiveness of the XOI platform as a predictable material system for investigating high performance devices. It also shows the critical role of quantum confinement and surface contributions on the transport properties of InAs, even for relatively large thicknesses. It should be noted that since the nanoribbon width used is 10 to 30 times larger than the thickness, there is minimal dependence of the device performance on the nanoribbon width, so the structures can be treated like thin films.

Chapter 4: Post-growth, Surface Doping Approaches for InAs Nanostructures

4.1. Chapter Introduction

In order to successfully integrate InAs nanostructures into more complex device geometries, post-growth, patterned doping approaches are necessary. Doping during growth has been well-investigated for Si and some III-V nanostructures, but the post-growth, patterned doping approaches that are necessary for device fabrication and manufacturing are not as well studied, especially in III-Vs.[91,92] While ion implantation and rapid thermal annealing are used for post-growth, patterned doping in the Si industry, ion implantation may be unsuitable for use with III-V nanostructures. Due to transient enhanced diffusion (TED), ion implantation is already reaching its limits for the fabrication of <10 nm ultrashallow junctions in Si. Surface doping approaches which minimize lattice damage are therefore desirable. Ion implantation presents additional problems in III-V semiconductors like InAs since compound semiconductors have two non-equivalent lattice sites. This makes ion implantation induced crystal damage especially problematic since stoichiometry can be altered and difficult to recover and dopants may not effectively activate onto the desired lattice site, leading to low electrically active dopant concentrations. In addition, ion implantation is not well-suited for three-dimensional (as opposed to planar) nanostructures.

Recently, a controllable nanoscale doping approach for Si substrates through use of molecular monolayers to achieve sub-5nm ultra-shallow junctions (USJs) was developed.[56,57] This approach allowed for both *p*- and *n*- doping of Si nanostructures depending on the selected monolayer chemistry. This monolayer doping (MLD) approach minimizes lattice damage and, as opposed to conventional surface doping techniques such as solid-source diffusion and spin-on-dopant methods, provides high areal dose control of the dopants with good uniformity resulting from the self-limiting nature of the monolayer formation reaction.[93,94,95] In this chapter, an *n*-doping MLD process using sulfur monolayers is developed and extended for use with compound semiconductors to form ultrashallow n^+/p^+ junctions. The process is demonstrated to be suitable with both planar (patterned ultrashallow junctions in InAs wafers) and non-planar (InP nanopillars) III-V nanostructures. Due to the difficulty in developing a *p*-doping MLD process for III-V semiconductors, a gas-phase surface doping approach using zinc was used and is presented here for both planar and non-planar (nanowire and ultrathin body nanoribbon) InAs nanostructures. It is important to note that *p*-type doping of InAs is particularly challenging given the high "intrinsic" surface electron concentration due to the Fermi level being pinned ~0.15 eV into the conduction band. This gas-phase approach is directly compared to zinc ion implantation of InAs nanowires and is clearly shown to be more effective.

4.2. Nanoscale Doping of III-Vs via Sulfur Monolayers

A well-established sulfur (S) monolayer formation reaction on InAs substrates is used to controllably position sulfur dopant atoms on the surface, followed by a subsequent thermal annealing step.[96,97,98,99,100,101,102] As a result, 5nm sulfur doped junctions are formed, giving n^+/p^+ USJs with the diodes exhibiting negative differential resistance (NDR) behavior as reported in Chapter 5.

The schematic shown in Figure 32 illustrates the MLD approach used. First, InAs (001) substrates cleaned with acetone and isopropanol are placed in an ammonium sulfide, $(NH_4)_2S_x$, solution (20% in water, Sigma Aldrich) with excess sulfur (0.2g S per 15 mL of solution).

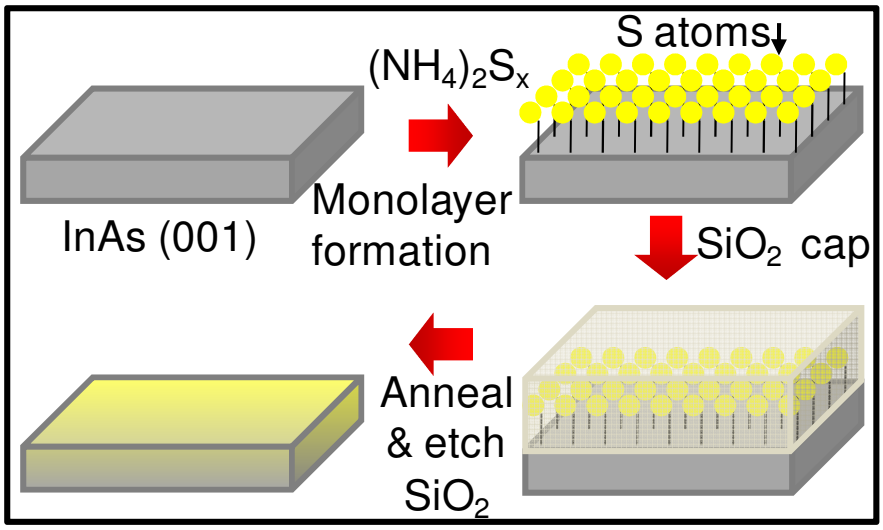

Figure 32. Schematic showing the sulfur monolayer doping (S-MLD) approach.

The $(NH_4)_2S_x$ solution is maintained in a water bath at 35 ^oC. The reaction is performed for 15 minutes. The InAs substrates are then rinsed in deionized water and immediately capped with electron-beam evaporated silicon oxide (SiO_x). Subsequently, thermal annealing at 350 to 450 ^oC for 300s is performed to drive-in the sulfur atoms to the desired junction depth.

The ammonium sulfide treated surfaces were characterized by x-ray photoelectron spectroscopy (XPS) in an ultrahigh vacuum (~10^{-9} torr) with a monochromated aluminum (Al) Kα source and pass energy set to 35.75 eV. Figure 33 shows the sulfur 2p peak spectra for a monolayer-reacted InAs (001) substrate compared to the signal from a control substrate without sulfur treatment, with the sulfur 2p 3/2 and 2p 1/2 doublet peak fits.

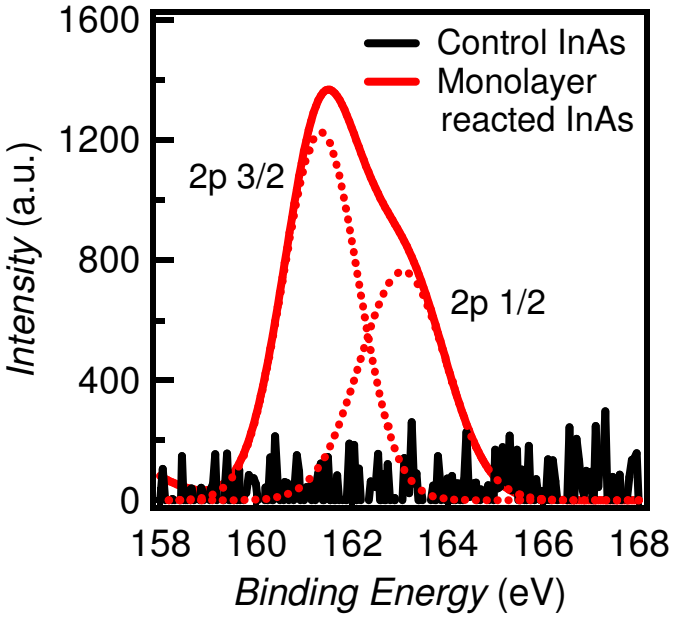

Figure 33. Surface characterization of ammonium sulfide-treated InAs (001) by XPS. The energy range corresponds to the sulfur 2p binding energy.

In the monolayer-reacted sample, the sulfur 2p 3/2 peak occurs at 161.6 eV as reported in the literature, with the In 3d and As 3d peak spectra observed (not shown) closely matching the results reported by Y. Fukuda, et al.[102] Because the In-S peak intensity is much stronger than the As-S peak intensity and the binding energies of sulfur to metals lie within the 160 to 162 eV range, it can be concluded that the S-2p peak spectra primarily represents S-In bonding with only minimal S-As bonding present. This is indicative of an InAs surface terminated by an In plane with which the sulfur monolayer is reacted, or the so-called "layer-cake" S-on-In-on-As model. These results are highly consistent with the findings of D. Petrovykh, et al. and Y. Fukuda, et al. suggesting the presence of a sulfur monolayer as the source for our doping technique.[100,101,102] The atomic surface density of InAs (001) is 5.6×10^{14} cm^{-2}, which represents the maximum areal sulfur dose, assuming a perfect monolayer.

After thermal annealing to drive in the dopants, the InAs/SiO_2 and junction interfaces were investigated by TEM. The high resolution TEM image for a sample annealed at 450°C for 300s shows the single crystalline nature of the sulfur doped region and the abrupt SiO_2/InAs interface (Figure 34a and b). This is in distinct contrast to the number of defects induced in conventional ion-implantation techniques. In order to characterize the chemical profile of the junction, EDS line profiling was performed across the SiO_2/InAs interface by using scanning TEM mode with a probe size of 0.2 nm, as shown in Figure 34c. The red, black, and green lines represent the In, As, and S signals respectively. There is a clear sulfur peak at the onset of the In and As signals, indicating the chemical presence of sulfur in the monolayer doped junction. There is ~3.08 atomic % sulfur ~1 nm from the InAs/SiO_2 interface based on the EDS analysis. The abrupt sulfur profile (~3.5 nm/decade) is further quantitatively confirmed with secondary ion mass spectrometry (SIMS) in Figure 34d. A high sulfur concentration of $\sim 1 \times 10^{21}$ cm^{-3}, in agreement with the EDS result, is measured at the InAs surface. This shallow sulfur profile

demonstrates the effectiveness of the MLD technique in compound semiconductors for USJ formation.

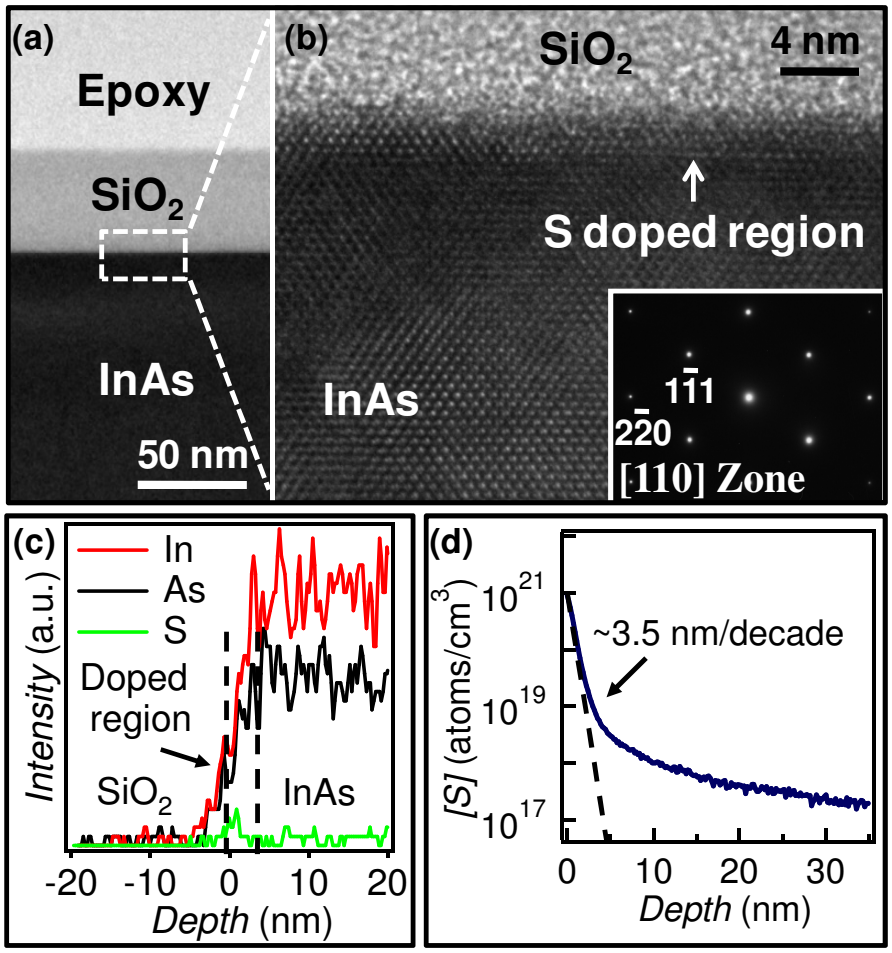

Figure 34. Structural and chemical profiling of S-doped InAs using an annealing condition of 450 ^{o}C for 300s. (a) and (b) Low and high resolution TEM images showing SiO_2/S-doped InAs interfaces. The ~4 nm dark contrast region corresponds to the S-doped layer. (c) EDS demonstrating the In, As, and S chemical profiles across the junction interface. (d) SIMS profile of S in InAs. The profile abruptness is ~3.5 nm/decade near the doped surface region.

The S-MLD technique was also extended to achieve conformal surface *n*-doping of *p*-InP nanopillars.[103] Unlike other doping methods, this technique results in conformal monolayer coverage on 3D structures which results in the ultrashallow incorporation of dopants at high concentrations following annealing in the surface of the nanopillars to give high quality, radial (i.e., core/shell) *p*-*n* junctions (Figure 35). Semiconductor nanopillar arrays with radially doped junctions have been proposed as an attractive device architecture for cost effective and high efficiency solar cells.[104,105] Until application of the sulfur MLD method, the challenge in the fabrication of three-dimensional nanopillar devices was the need for highly abrupt and conformal junctions along the radial axes.

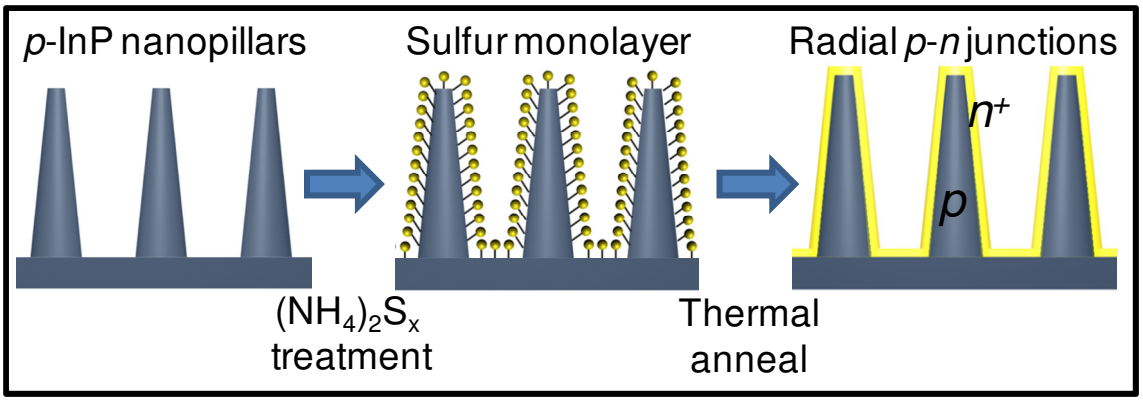

Figure 35. Schematic of the sulfur monolayer doping approach applied to InP nanopillars.[103]

The sulfur monolayer formation on the InP surface after ammonium sulfide treatment (with treatment conditions identical to those described for sulfur monolayer formation on InAs) was characterized by XPS. Figure 36 shows the sulfur 2p peak spectra for a monolayer-reacted InP substrate with sulfur 2p 3/2 and 2p 1/2 doublet peak fits. A peak at ~162 eV is observed, which is the binding energy of core shell electrons for the sulfur 2p shell.[106] No sulfur peaks are observed for untreated InP control samples. These results are consistent with the findings of previous reports, including the one here, on the presence of the sulfur monolayer on the surface using ammonium sulfide treatment.[107]

SIMS profiling and Hall measurements confirmed that through use of the sulfur MLD approach, conformal ultra-shallow junctions with sub-10nm depths and a high electrically active dopant concentration of 10^{19}~10^{20} cm^{-3} are achieved in the InP nanopillar arrays. Solar cells fabricated from these arrays exhibit a respectable conversion efficiency of 8.1% and a short circuit current density of 25mA/cm^3, again demonstrating the utility of well-established surface chemistry for fabrication of non-planar junctions for complex devices.[103]

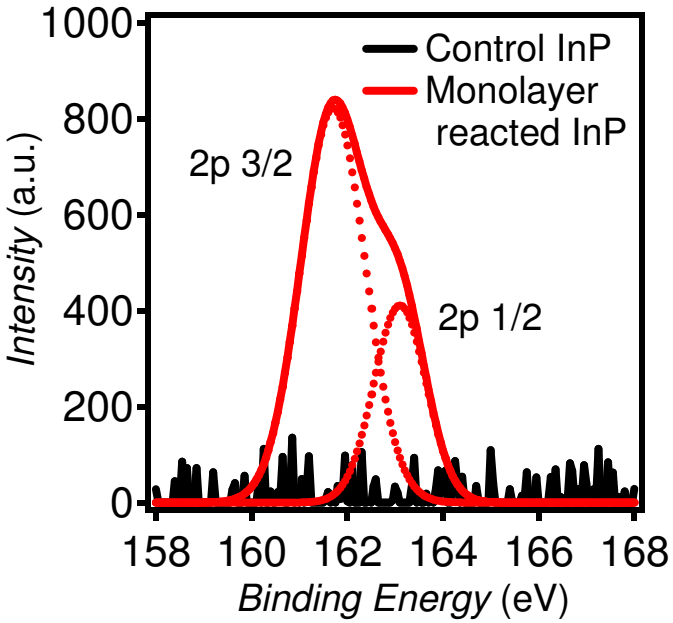

Figure 36. Surface characterization of ammonium sulfide-treated InP by XPS. The energy range corresponds to the sulfur 2p binding energy.

4.3. Doping of InAs Nanowires by Zinc Gas-Phase Surface Diffusion

Patterned *p*-doping of InAs nanowires with zinc (Zn) by using a post-growth, surface doping approach is reported here. The effectiveness of the approach is demonstrated by configuring the doped nanowires into p^+-*n* diodes and *p*-MOSFETs as reported in Chapter 5.

InAs nanowires used in this work were grown using the vapor-liquid-solid/vapor-solid-solid method by chemical vapor deposition in a two-zone tube furnace using solid InAs powder source as described in Chapter 2. As previously described, a 0.5 nm thick Ni film was annealed at 800 °C for 10 min to create nanoparticles that serve as catalysts. A substrate temperature of 490 °C, source temperature of 720 ºC, pressure of 5 torr with H_2 carrier gas (200 SCCM flow rate) were used. The nanowires were harvested by sonication in anhydrous ethanol and dropcast on Si substrates. To *p*-dope the nanowires with zinc, the samples were placed in a tube furnace with solid zinc powder used as the source. The Si substrate with dropcast nanowires and the zinc source were placed ~6 cm apart with the furnace temperature set at 400-415 ºC for 1 min (as counted from temperature stabilization time). A chamber pressure of 650 torr with Ar atmosphere was used. To achieve patterned doping, a SiO_x mask was deposited by electron-beam evaporation to partially cover the dropcast nanowires on Si substrates. The diffusion length x of zinc atoms can be approximated as $x = 2(Dt)^{1/2}$ where D is the diffusion coefficient

and t is the diffusion time. A diffusion coefficient $D \sim 1.4 \times 10^{-12}$ cm^2/s at 400 °C for zinc in InAs bulk substrates is reported in the literature.[94] Given this diffusion coefficient value, a diffusion length of ~180 nm is estimated for the time used (t=1 min). This indicates that for these process conditions, the InAs nanowires are fully doped across their diameter (i.e. $d <$ diffusion length). This diffusion length is much smaller than the channel lengths of L=6-10 μm reported here. It should be noted that the diffusion parameters used are for bulk substrates since there are no values reported for nanostructures. In the future, more detailed studies of dopant diffusion in different nanowire materials are needed.

Low and high-resolution TEM images of a zinc-doped InAs nanowire are shown in Figure 37a and b. The high resolution TEM image shows the single-crystalline nature of the doped InAs nanowire for which two planes, (222) and (220), are indexed. The diffraction pattern is shown in the inset with a [112] zone axis. Figure 37c shows the EDS analysis of a Zn-doped InAs nanowire for which the elemental composition of ~5 at. % Zn can be identified. Given the atomic density of 1.8×10^{22} cm^{-3} for InAs, this corresponds to a zinc concentration ~9×10^{20} cm^{-3}. This high concentration is more likely the result of some of the zinc remaining on the surface of the nanowires.

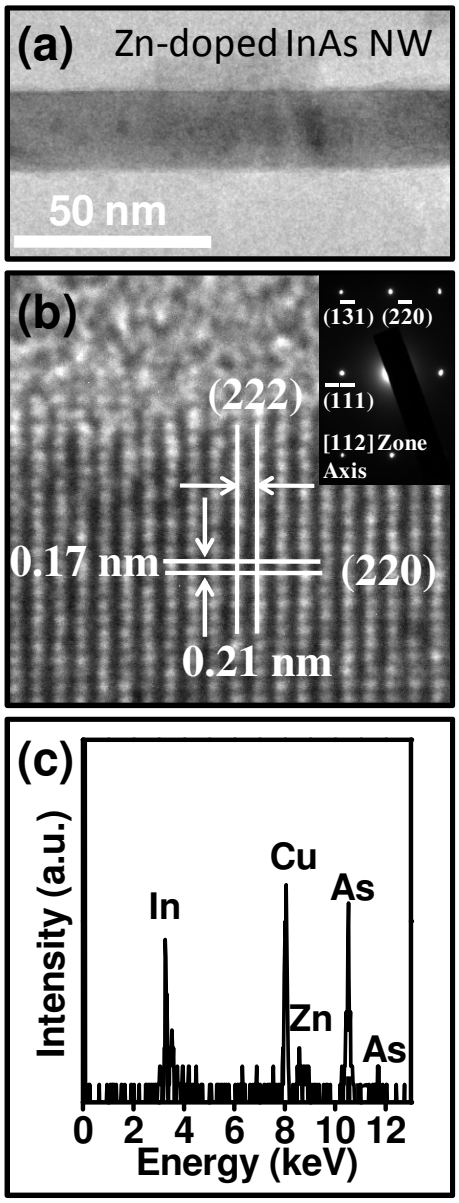

Figure 37. TEM of Zn-doped InAs nanowires. (a) Low-resolution and (b) high-resolution TEM images of a Zn-doped InAs nanowire with diffraction pattern shown in the inset. (c) EDS analysis of a Zn-doped InAs nanowire, depicting an elemental composition of ~5 at. % Zn. This high concentration is likely the result of some of the Zn remaining on the surface of the nanowires.

To find the electrically active content of zinc dopant atoms, back-gated devices were fabricated by photolithography on the dropcast nanowire substrates (p^+Si / 50 nm SiO_2) to define source (S) and drain (D). Ni was then thermally-evaporated into the S/D regions to form contacts. The inset in Figure 38a shows a scanning electron microscope (SEM) image of a representative back-gated nanowire device. Long channel lengths, L=6-10 μm, were used to make sure that transport of carriers is in the diffusive, as opposed to ballistic or quasi-ballistic, regime. This allows for the extraction of intrinsic transport properties, such as carrier mobility.

The *I-V* characteristics of a representative as-grown InAs nanowire and blank (i.e. unpatterned) Zn-doped InAs nanowire are shown in Figure 38. The as-grown InAs nanowire is *n*-type due to the high electron concentration of intrinsic InAs.

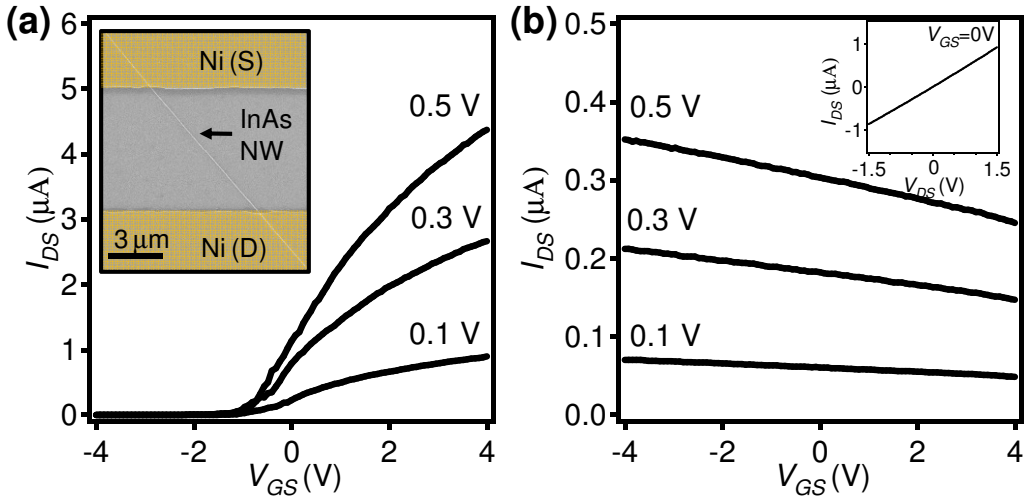

Figure 38. The I_{DS}-V_{GS} characteristics of a representative (a) as-grown InAs nanowire with an SEM image of a representative device shown in the inset and (b) blank (i.e. unpatterned) Zn-doped InAs nanowire with I_{DS}-V_{DS} plot for V_{GS}=0 shown in inset. The heavily doped Si substrate is used as the global back gate with a gate dielectric thickness of 50 nm SiO_2.

As previously discussed, there is a linear dependence of the device resistance on channel length, establishing that the Ni source/drain contacts to the conduction band of as-grown InAs nanowires are ohmic. The as-grown nanowire exhibits an *ON* current of ~4.4 μA at V_{DS} = 0.5V, I_{ON}/I_{OFF} > 10^4, and field-effect mobility of 4400 cm^2/Vs for channel length L = 8 μm and nanowire diameter d = 27 nm, consistent with the results shown in Chapter 3. The doped InAs nanowires using the described process conditions are p^+ due to heavy Zn doping, with an *ON* current of ~0.4 μA at V_{DS} = 0.5V with minimal gate dependence (Figure 38b). The linear behavior of the I_{DS}-V_{DS} plot (Figure 38b) confirms that the contacts to the p^+ nanowire are near ohmic. This is due to the thinning of the Schottky barriers at the contacts to the valence band of nanowires resulting from the heavy Zn doping. From the I_{DS}-V_{GS} characteristics, a hole field-effect mobility of ~30 cm^2/Vs for a nanowire diameter of d ~ 30 nm is estimated. This field-effect mobility is reasonable given that the hole Hall mobility of bulk InAs substrates for a doping concentration of ~$1x10^{19}$ cm^{-3} acceptors is ~100 cm^2/Vs at room temperature and that the measured Hall mobility is always larger than the extracted field-effect mobility. Using the conductance G ~ $6x10^{-7}$ S and d ~ 30 nm, the resistivity, ρ ~ 0.02 Ω-cm is estimated for the doped nanowire. From ρ and μ, the electrically-active [Zn] is estimated to be ~ $1x10^{19}$ cm^{-3}. This high electrically-active [Zn] corresponds to degenerate doping, with the Fermi level E_F located ~0.024 eV below the valence band edge E_v. This electrically active Zn concentration is consistent with those reported for various dopants in bulk InAs substrates.[94,108] While most (~70%) nanowires exhibited p^+ behavior (with minimal gate dependence) for doping temperatures of >400 ºC, some (~30%) nanowires exhibited lightly *p*-type or ambipolar behavior. For doping temperatures <400 °C,

roughly half of the nanowires were ambipolar while the other half remained *n*-type. For the p^+ nanowires, there was enough zinc doping to fully compensate the high intrinsic electron concentration, especially at the surface. However, for the ambipolar nanowires, it is likely that the core of the nanowire is doped *p*-type while the high surface electron concentration "shell" remains *n*-type.

For comparison, InAs nanowires were also doped using zinc ion-implantation. An ion implantation energy of ~ 35 keV with dopant areal dose of $3.5x10^{12}$ to $3.5x10^{13}$ cm^{-2} were used, followed by thermal annealing at 375 ºC for 30 min. (It is noted that this is still a relatively high energy for use with nanostructures, but it was the lowest energy the implanter was capable of.) Scanning electron microscopy (SEM) clearly indicates that the nanowire surfaces are severely damaged by the ion implantation, and in some cases, the nanowires were even broken with damage being the most apparent for the highest dopant dose of ~ $3.5x10^{13}$ cm^{-2} (Figure 39).

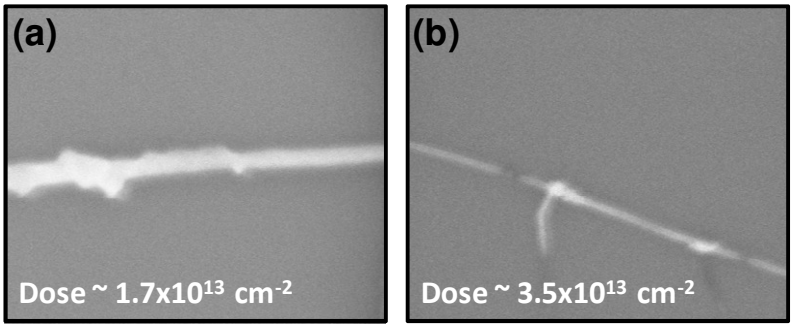

Figure 39. SEM images of InAs nanowires doped by Zn ion-implantation and subsequent annealing at 375 ºC for 30 min. The nanowires are severely damaged for (a) a dopant areal dose of ~$1.7x10^{13}$ cm^{-2} and (b) a dose of ~ $3.5x10^{13}$ cm^{-2}.

Furthermore, back-gated devices fabricated from the zinc ion-implanted InAs nanowires remained *n*-type with degraded *ON* currents and did not turn off, even after thermal annealing, suggesting that the incorporated dopants are not electrically active and that the damage to the nanowire lattice degraded the electrical properties and enhanced the leakage currents (Figure 40). The failure of the zinc ion-implantation approach to produce defect-free *p*-type nanowires highlights the importance of the zinc surface doping method presented here for compound semiconductor nanostructures.

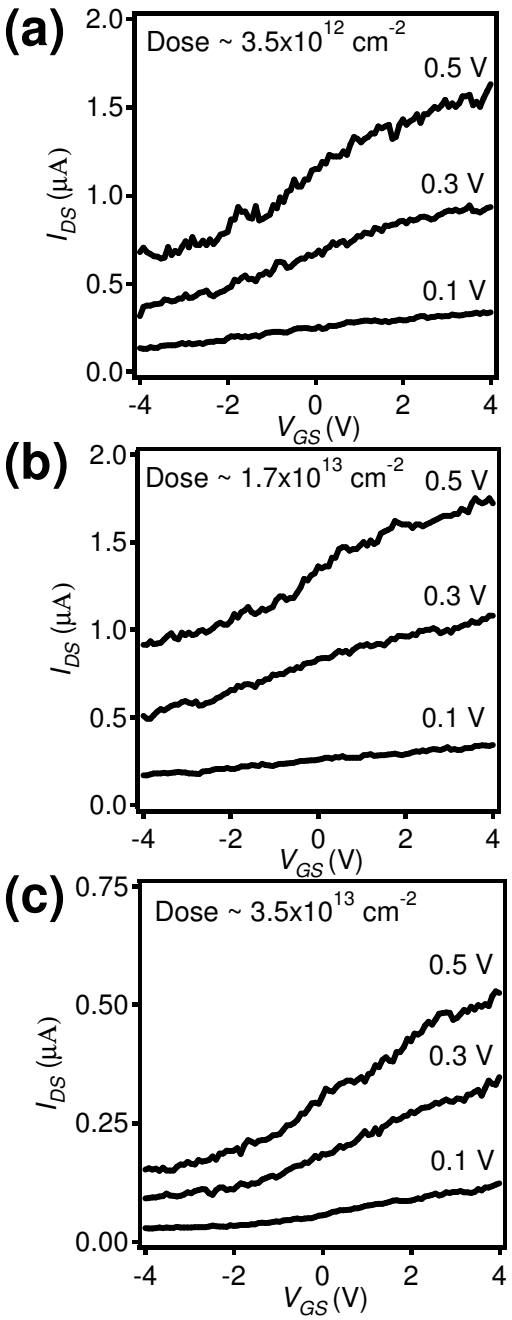

Figure 40. I_{DS}-V_{GS} characteristics of InAs nanowires doped by Zn ion-implantation for dopant areal dose of (a) ~ 3.5x10^{12} cm^{-2}, (b) ~ 1.7x10^{13} cm^{-2}, and (c) ~3.5x10^{13} cm^{-2} and subsequent annealing at 375 °C for 30 min. The channel length and nanowire diameter for all three devices is ~2 μm and ~30 nm, respectively.

In order to show the effectiveness of the gas-phase doping approach, InAs nanowire p^+-n diodes and p-MOSFETs were fabricated and tested and are discussed in Chapter 5.

Chapter 5: Post-Growth, Patterned Doping of InAs Nanostructures

5.1. Chapter Introduction

Post-growth, patterned doping techniques compatible with III-V nanostructures are necessary for their integration into various device architectures. In this chapter, by using the sulfur monolayer doping (MLD) method for *n*-doping and the zinc gas-phase surface diffusion method for *p*-doping as described in Chapter 4, different device structures are demonstrated. First, n^+/p^+ InAs tunnel diodes are fabricated using the sulfur MLD doping process. Next, back-gated InAs nanowire *p*-MOSFETs and diodes are shown using the zinc gas-phase surface diffusion approach. Finally, an ultrathin body InAs nanoribbon TFET is demonstrated using zinc gas-phase doping. It is important to note that all of these InAs nanostructure-based devices are fabricated on SiO_2/Si or Si_3N_4/Si substrates, effectively demonstrating a way to integrate III-V nanostructures with well-established, low-cost Si technology.

5.2. Tunnel Diodes Fabricated Using Sulfur Monolayer Doping

To characterize the electrical properties of the sulfur monolayer doped junctions discussed in Chapter 4, n^+/p^+ tunnel diodes were fabricated on heavily Zn-doped InAs substrates (N_B ~$6x10^{18}$ cm^{-3}). First, 125nm of field-oxide was deposited on the substrate by electron-beam evaporation. Photolithography and wet etching using 50:1 hydrofluoric acid was used to define the well regions. The sulfur-containing monolayer was then reacted on the exposed InAs well regions and a 35 nm thick SiO_2 cap was then deposited. The sample was annealed in a rapid thermal annealing (RTA) tool at 400°C for 300s, followed by Ni contact (~150 nm thick) formation on top of the sulfur doped regions by defining vias through photolithography and hydrofluoric acid (HF) etching (Figure 41a). Figure 41b shows the *I-V* electrical characteristic of a representative tunnel diode with negative differential resistance (NDR) behavior. For reverse bias (< 0V), the current is due to band-to-band tunneling as the electrons tunnel from the valence band on the *p*-side of the junction into the conduction band on the *n*-side of the junction and the current increases with bias indefinitely. For forward bias (> 0V), the electrons tunnel from filled states in the conduction band (n^+ side) to unoccupied states in the valence band (p^+ side) to result in a peak current at point "a" (Figure 41b). Here the peak voltage V_p = 0.08 V and the peak current I_p = 0.26 mA. As the forward bias continues to increase, the band overlap diminishes, resulting in the observed NDR. When the *n*-side conduction band edge rises above the *p*-side valence band edge, there are no more states for tunneling resulting in the valley current at point "b" (Figure 41b). Here, the minimum (valley) voltage, V_m = 0.16 V and the minimum (valley) current, I_m = 0.15 mA. This gives a peak-to-valley ratio I_p/I_m = 1.7, which is a slight improvement over the peak-to-valley ratio of 1.61 reported in the literature obtained by other doping processes for InAs diodes exhibiting NDR behavior.[95] From this onset, normal diffusion current starts to dominate the forward current. The gamma factor for the diode shown in Figure 41b is $\gamma = (d^2I/dV^2)/(dI/dV)$ ~ 6.8, also an improvement over the γ~ 4.5 found in the literature.[95] This NDR observation is direct evidence of band-to-band tunneling which requires degenerate doping in both *n*- and *p*-regions with a small tunneling barrier width (i.e. an abrupt junction).

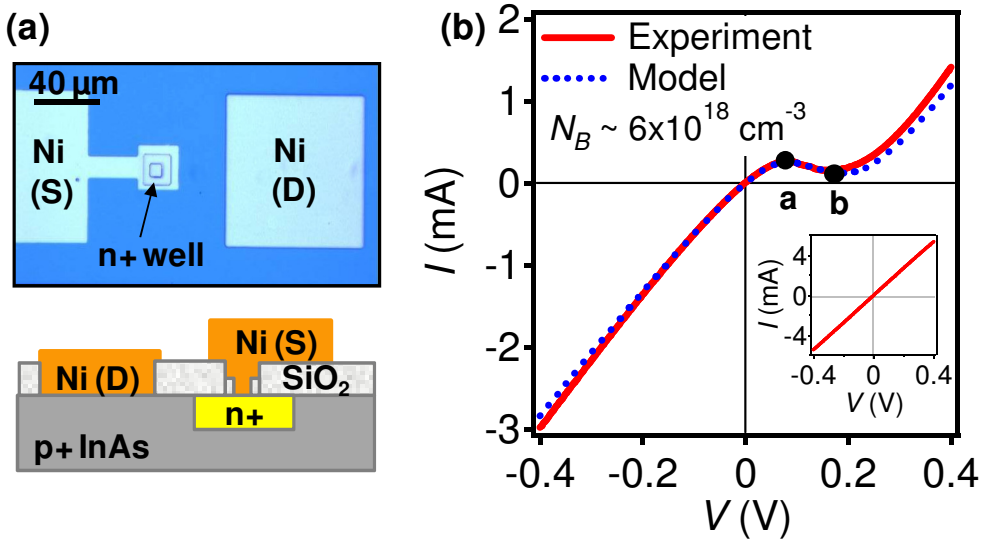

Figure 41. Electrical characterization of diodes fabricated using the sulfur MLD process on p^+ InAs substrates (N_B ~6x10^{18} cm^{-3}) using an annealing condition of 400 °C for 300s. (a) Optical image (top) and schematic (bottom) of a representative diode. (b) *I-V* characteristic of a fabricated diode showing NDR behavior. The junction area is ~314 µm^2. The dashed blue line shows the modeled *I-V* curve, assuming a sulfur doping concentration of N_D = 8x10^{18} cm^{-3}. The inset shows the electrical properties of a control device, fabricated by the exact procedure, however, without the application of the sulfur monolayer.

Based on Kane's model of tunneling where the electric field is assumed to be constant, the electrically-active sulfur concentration is estimated to be N_D~8x10^{18} cm^{-3} which is close to the highest activate concentration found in the literature.[109,110] The modeled *I-V* curves based on this doping concentration are shown in Figure 41b, where $n = N_D - N_B$ since the sulfur doping compensates the Zn dopants in the substrate. For the tunnel diode, N_B = 6 x 10^{18} cm^{-3} and n = 2 x10^{18} cm^{-3}. A series resistance of 100 Ω was included in the modeling to account for the parasitic resistance due to the substrate and/or contacts. The modeled tunneling current matches the experimental data very closely. The discrepancy between the modeled and SIMS concentration values indicates that only a fraction of the sulfur atoms is electrically active, with the remaining sulfur atoms likely still passivating the surface or occupying non-electrically active sites in the bulk. The observation of NDR behavior with this monolayer doping approach is a clear indication of heavy sulfur doping with sharp junction abruptness.

Since the surface Fermi-level for InAs is known to be pinned at ~ 0.15 eV above the conduction band, control experiments were performed to demonstrate that the observed NDR behavior of the fabricated diodes is due to sulfur-doping rather than the surface electron inversion layer.[111,112] Control devices were made using the exact same fabrication procedure described above and the same p^+ InAs substrate, but without the sulfur monolayer treatment. As a result, the fabricated devices are just two Ni source/drain contacts formed directly on the p^+ InAs substrate. The *I-V* behavior of a representative control device is shown in the inset of Figure 41b. This linear behavior can be attributed to the ohmic contact formation to p^+ InAs. (This is in contrast to the lightly *p*-doped InAs substrates that are known to be hard to form ohmic contacts due to the surface inversion layer.) For the heavily doped p^+ InAs substrates with

N_B~6x10^{18} cm^{-3} used here, near ohmic contacts are readily formed by Ni, likely due to the thinning of the tunnel barrier width for such high background dopant concentrations as previously reported.[93] In addition, control devices were fabricated involving sulfur monolayer formation on the surface of the p^+ InAs substrate, but without the thermal annealing step to drive-in the dopants, followed by Ni contact formation. These control devices also showed linear *I-V* characteristics, indicating the lack of diode formation. The results from the control experiments are in contrast to the S-MLD treated samples that exhibit a clear NDR behavior due to the heavy *n*-doping of the surface by the sulfur dopants.

Besides the practical implications of the S-MLD approach, the results here call into question whether the improvements in the electrical contact behavior observed by "passivating" compound semiconductor surfaces with sulfur monolayers is at least partly due to doping the semiconductor as opposed to merely passivating it (unpinning the Fermi level at the contacts). This is especially true for experiments where subsequent annealing was used.[96,113] The results shown here indicate that consideration of the thermal budget needs to be applied if sulfur passivation is used at the InAs/gate dielectric interface, for instance for the atomic layer deposition of gate dielectrics.[114,115]

5.3. InAs Nanowire *p*-MOSFETs Fabricated Using Zinc Gas Phase Surface Diffusion

Back-gated InAs nanowire *p*-MOSFETs were fabricated using gas phase Zn-doping to form the p^+ S/D contacts, with a schematic of the process shown in Figure 42a. Undoped InAs nanowires were dropcast on p^+Si/SiO_2 (50 nm thermally grown) substrates and photolithography was used to pattern SiO_2 (~70 nm thick) masks on top of the nanowires. Nanowire substrates were then Zn-doped as previously described in Chapter 4. The exposed nanowire ends were made p^+ while the nanowire segment under the SiO_2 mask remained undoped. Photolithography and thermal evaporation were then employed to form the Ni contacts to the p^+ S/D regions. The heavily doped Si substrate was used as the back-gate with a gate dielectric thickness of ~50 nm SiO_2.

The *I-V* characteristics of a representative InAs nanowire *p*-MOSFET are shown in Figure 42b and d, with an SEM image of a representative device shown in the inset in Figure 42d. The *p*-MOSFET has I_{ON} ~ 0.17 μA and I_{OFF} ~ 0.1 nA at V_{DS} = 0.5V, with an $I_{ON}/I_{OFF} > 10^3$. The threshold voltage V_t is shifted to a positive voltage, likely as a result of fixed oxide and interface trapped charges at the interface of the nanowire *n*-segment and the evaporated SiO_2 mask. The field-effect mobility as a function of V_{GS} is shown in Fig. 43c, with a peak hole mobility of ~60 cm^2/Vs.

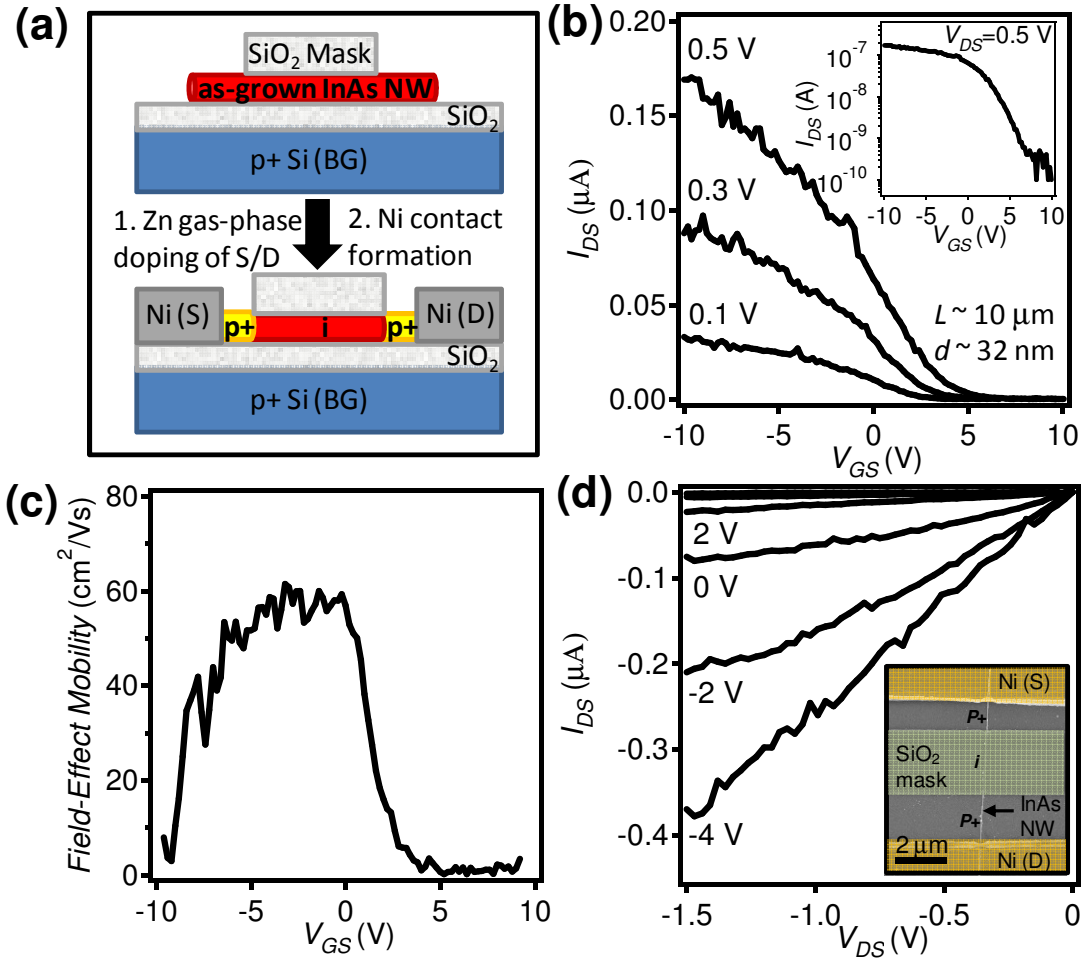

Figure 42. InAs nanowire *p*-MOSFET. (a) A schematic of the fabrication process for back-gated InAs nanowire *p*-MOSFETs. (b) The I_{DS}-V_{GS} behavior of a representative *p*-MOSFET with the logscale plot shown in the inset. (c) Hole field-effect mobility of the device as a function of the back gate voltage. (d) The output characteristics of the same nanowire *p*-MOSFET with SEM image of a representative *p*-MOSFET shown in the inset.

The hole mobility for InAs nanowires is significantly lower than the electron mobility as expected. This mobility is ~9x lower than the Hall mobility of ~450 cm^2/Vs reported for lightly doped, *p*-type InAs bulk substrates. The difference may be due to surface scattering and contact resistance associated with the field-effect mobility extraction. The *I-V* behavior of the patterned Zn-doped *p*-MOSFET is in contrast to the behavior of the blank Zn-doped nanowire device shown in Chapter 4, Figure 38b which exhibits very little gate dependence. Also, in contrast to the blank doped p^+ nanowire devices where the entire doped nanowire serves as the channel material, the *p*-MOSFET exhibits a higher hole mobility (~2x higher) since the channel is undoped, resulting in minimal impurity scattering.

5.4. InAs Nanowire Back-Gated Diodes Fabricated Using Zinc Gas Phase Surface Diffusion

Back-gated diodes were fabricated by patterned Zn doping of InAs nanowires. The process flow is shown in Figure 43a. First, 60 nm of Si_3N_4 was grown by PECVD on p^+ Si substrates. As-grown InAs nanowires were then dropcast on the nitride substrate and 70 nm electron-beam evaporated SiO_2 was deposited on regions patterned by photolithography to cover parts of the nanowires, followed by lift-off. The evaporated SiO_2 served as the diffusion mask during the doping. The nanowire substrates were then Zn-doped by the gas-phase surface doping process, with only the unmasked segments of the nanowires exposed to Zn-doping. Ni contacts were then made to the Zn-doped segments of the nanowires by photolithography and thermal evaporation. A final photolithography step, followed by etching in 50:1 HF to remove the SiO_2 mask and a subsequent Ni thermal evaporation were applied to contact the undoped regions (as-grown, *n*-type segments) of the nanowires. The *I-V* behavior of a representative diode is shown in Figure 43b. Here, the channel length $L \sim 7$ μm and nanowire diameter $d \sim 28$ nm.

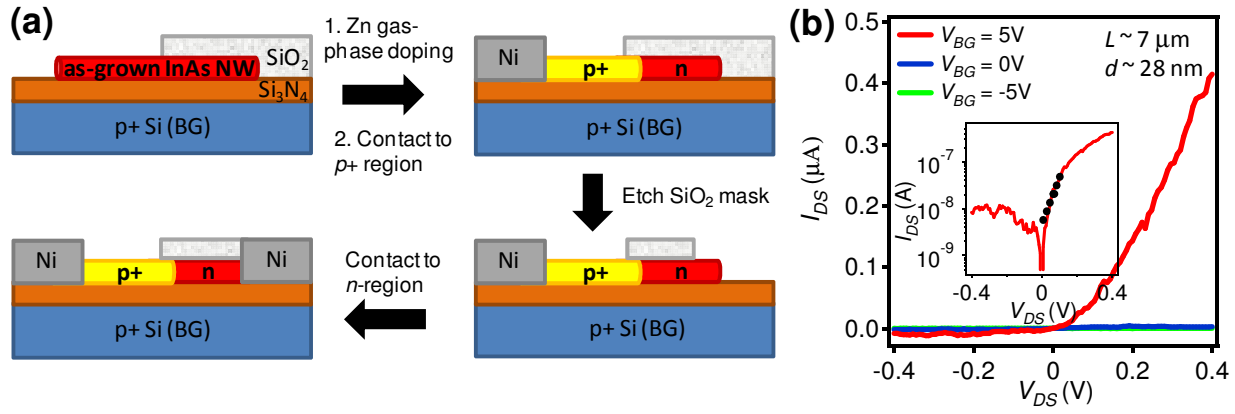

Figure 43. InAs nanowire back-gated diode. (a) The process flow for the fabrication of back-gated InAs nanowire diodes. (b) The *I-V* behavior of a representative diode as a function of the back-gate voltage, V_{BG}. The inset shows the logscale plot for V_{BG}=5V and the fit to the ideal diode equation indicated by the dotted line.

A rectifying behavior is observed for $V_{BG} > 0$. The device is insulating for $V_{BG} \leq 0$. This, along with the I_{DS}-V_{GS} curves of Figure 38b, indicates that the Zn-doped region of the nanowire is in fact p^+ and is always in the hole accumulation mode, while the *n*-type region is being modulated by the back-gate. The *n*-type segment becomes fully depleted for $V_{BG} \leq 0$, but turns to the accumulation mode for $V_{BG} > 0$ and $V_{DS} > 0$. The ideality factor of the p^+-*n* diode shown in Figure 43b is ~1.5, with the fit to the ideal diode equation indicated by the dotted line in the logscale inset. The Zn doping process is also compatible with bulk InAs substrates with the nanowire and bulk diodes fabricated using the same approach exhibiting similar properties (Figure 44).

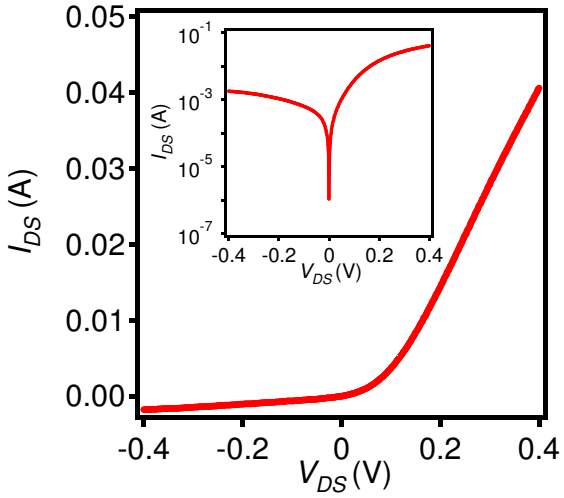

Figure 44. *I-V* characteristics of a representative InAs diode fabricated on a bulk intrinsic substrate (electron concentration ~2x10^{16} cm^{-3}) by the gas-phase Zn surface doping approach. The junction area is ~10,000 μm^2.

5.5. InAs XOI TFETs Fabricated Using Zinc Gas Phase Surface Diffusion

As previously discussed in Chapter 2, a method to integrate ultrathin layers of InAs on SiO_2/Si substrates has been developed by using an epitaxial layer transfer technique. As with InAs nanowires on SiO_2/Si substrates, this integration of ultrathin layers of InAs-on-insulator, offers the advantages of combining III-V semiconductors with well-established Si technology. III-V nanowires and XOI is advantageous for tunneling field effect transistors (TFETs) due to the reduced leakage currents and better electrostatic control of the tunnel junction. Lower *OFF* state currents are essential for the use of low band-gap semiconductors like InAs.[31] In addition, the XOI platform offers the advantage of incorporating different III-V active layers with low defect densities on insulator/Si (and not limited by the original III-V growth substrate) to permit the fabrication of heterojunction devices with band alignments optimized to achieve a low effective tunneling barrier.[39] Here an ultrathin body InAs TFET on a Si substrate is demonstrated. TFETs are promising candidates to replace or complement MOSFETs because of their improved sub-threshold swing (*SS*) and reduced power consumption.[32,33,34,35,36,37,38,39,40] InAs is an ideal material for use in TFETs, since its small direct band gap makes for a low effective tunneling barrier and its low effective mass results in a large tunneling probability to achieve high *ON* currents.[38]

A schematic of the InAs XOI TFET fabrication process is shown in Figure 45. InAs nanoribbons ~18 nm in height and ~350 nm in width were transferred to 60 nm low-stress silicon nitride on p^+ Si substrates using the epitaxial layer transfer process described in Chapter 2 (Figure 45a). Photolithography followed by electron-beam evaporation of 80 nm SiO_x and liftoff was used to pattern SiO_x masks to partially cover the InAs nanoribbons (Figure 45b). The unmasked, exposed segments of the InAs nanoribbons were then doped p^+ with zinc using gas phase surface diffusion as described in Chapter 4 at temperatures of 390-410 ºC for ~30s to 1 min. The diffusion length ($x = 2(Dt)^{1/2}$, where D and t are the diffusion coefficient and time, respectively) of Zn in InAs is 130-180nm for the doping temperatures (D = 1.4x10^{-12} cm^2/s at

400 ºC) and times used, resulting in a non-abrupt lateral junction. The diffusion length is longer than the InAs thickness of ~18nm, resulting in the entire depth of InAs getting doped during the patterned doping process. The SiO_x masks were then etched in 50:1 HF and the p^+ source (S) and n^+ drain (D) nickel (Ni) contacts were formed by photolithography, Ni evaporation, and liftoff (Figure 45c). As previously discussed, undoped InAs is intrinsically *n*-type, making the TFET p^+-*n* structure possible without the use of an *n*-type dopant. Following S/D metal contact formation, 8 nm ZrO_2 was deposited by atomic layer deposition at 130 °C for the gate dielectric and a Ni top-gate (G) overlapping S/D was formed by photolithography, Ni evaporation, and liftoff (Figure 45d).

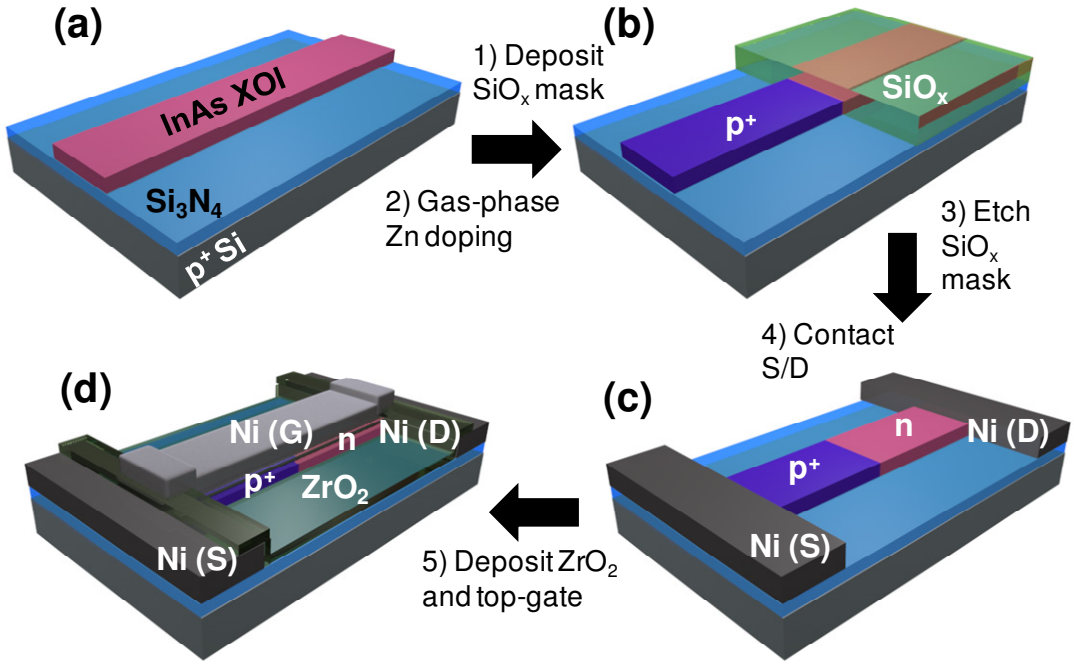

Figure 45. Schematic of the InAs XOI TFET fabrication process. (a) InAs nanoribbons (~18 nm thick, ~350 nm wide) were transferred to low-stress nitride on p^+ Si substrates. (b) SiO_x masks were deposited followed by Zn gas phase doping to form the p^+ S contacts. (c) Ni S/D contacts were formed. (d) For the gate dielectric, 8 nm ZrO_2 was deposited by atomic layer deposition and a Ni top-gate (G) overlapping S/D was formed.

Confirmation of p^+ doping was obtained by having back-gated InAs nanoribbon devices that were blank-doped (i.e. unpatterned) on the same chip with the TFETs. The p^+ blank-doped devices (channel length L=5μm) have *ON* current densities of ~15 μA/μm at V_{DS} = 1V and V_{GS} = -4V, with minimal back-gate dependence (Figure 46a). The electrically active [Zn] is estimated to be ~$1x10^{19}$ cm^{-3} which is in good agreement with the result for Zn-doped InAs nanowires in Chapter 4 and bulk substrates.[94] InAs nanoribbon *p*-MOSFETs (InAs nanoribbon p^+-*n*-p^+ structure on SiO_2/Si, channel length L=5μm) were fabricated in parallel to the blank-doped and TFET devices and have an *ON* current density of 3.5 μA/μm for V_{GS} = -5V and V_{DS} = 0.5V, $\mu_{p,FE}$

~300 cm^2/Vs, and I_{ON}/I_{OFF} ratio of ~60 (Figure 46b). As expected, the hole mobility is much lower than the electron mobility and the field-effect mobility is lower than the reported Hall mobility (450 cm^2/Vs) for lightly doped *p*-type InAs substrates.[94] The *p*-MOSFET field-effect mobility is higher than the blank-doped device field-effect mobility due to the channel being undoped, resulting in minimal impurity scattering. These InAs nanoribbon *p*-MOSFET devices again confirm the effectiveness of the p^+ doping as well as the successful doping of p^+-*n* junctions in XOI.

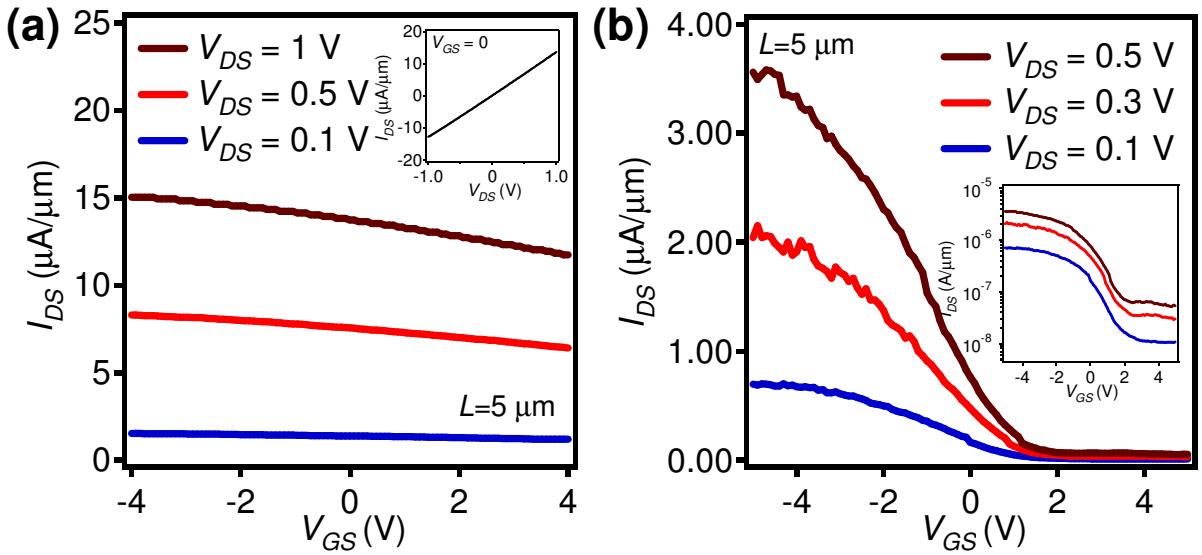

Figure 46. InAs XOI nanoribbon (a) p^+ blank-doped device and (b) *p*-MOSFET (logscale shown in inset) I_{DS}-V_{GS} transfer characteristics.

The room temperature *I-V* characteristics of a representative TFET device (channel length *L*~2.5μm) are shown in Figure 47. The device has sub-threshold swings (*SS*) of ~170 and 190 mV/dec for V_{DS} = 0.01 and 0.1V, respectively (Figure 47a). The *SS* exceeding 60 mV/decade is likely the result of surface trap states, and/or trap-assisted tunneling (TAT) where electrons tunnel to energy states in the bandgap and are then thermally emitted.[40,116] Figure 47b shows the room temperature output characteristics of the same device.

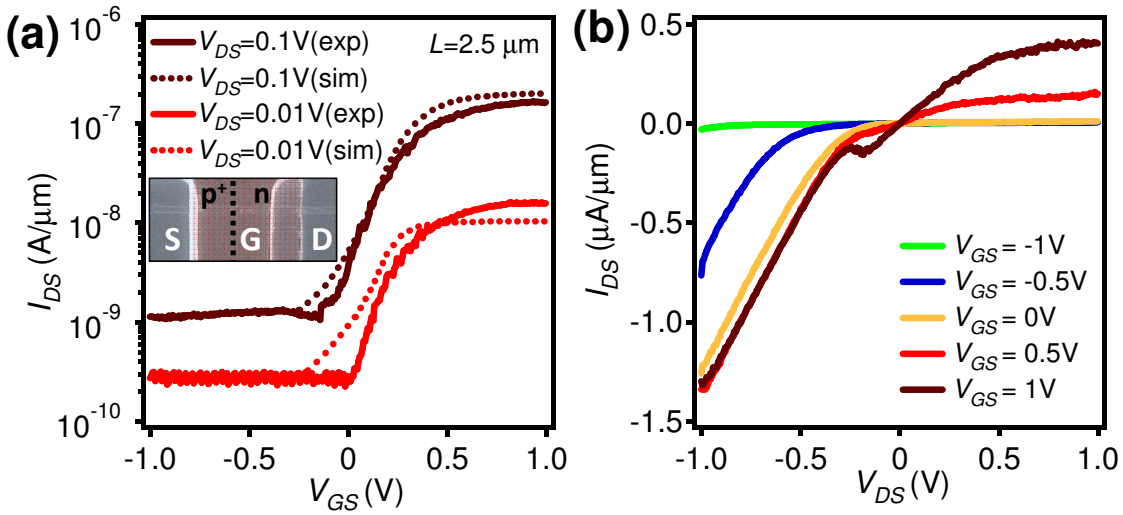

Figure 47. Room temperature (a) transfer and (b) output characteristics of a representative InAs XOI TFET (channel length *L*~2.5µm).

The *ON* current density is ~0.5 µA/µm at V_{DS} =V_{GS} = 1V. The device is forward biased for negative V_{DS} and, under positive V_{GS}, negative differential resistance (NDR) behavior is observed, clearly confirming the inter-band tunneling operation of the device. The NDR peak current $|I_{DS}|$ and voltage are ~0.15 µA/µm and -0.18V and the valley $|I_{DS}|$ and voltage are 0.12 µA/µm and -0.24V for V_{GS} = 1V, giving a peak-to-valley ratio of 1.3 at room temperature. This is in good agreement with the InAs tunnel diodes reported at the beginning of the Chapter and in the literature.[95]

To better understand the device operation, two-dimensional device simulations using TCAD Sentaurus were performed. The dynamic nonlocal path band-to-band model is used so that the band-to-band tunneling path is determined dynamically based on the gradient of the energy band profile. Standard Shockley–Read–Hall recombination and drift-diffusion models were used for carrier transport, and Fermi statistics were assumed. An electrically active [Zn] of $1x10^{19}$ cm^{-3} for the p^+ source, intrinsic InAs electron concentration of $1x10^{17}$ cm^{-3} for the channel, equivalent oxide thickness of 2 nm, and Zn lateral diffusion length (junction abruptness) of 180 nm were used. To take into account the effects of quantization, a bandgap of 0.385eV and electron effective mass of $0.026m_e$ were used. The simulated transfer characteristics of the TFET are plotted alongside the experimental results in Figure 47a and are in good agreement. From the Kane and Keldysh models in the uniform electric field limit, the fitted *A* and *B* parameters for the simulation were $7x10^{16}$ $cm^{-3}s^{-1}$ and $1.3x10^6$ V/cm, respectively.[109] The fitted *B* parameter is in good agreement with the calculated value of $1.3x10^6$ V/cm, but the fitted *A* parameter differs substantially from the calculated value of $9x10^{19}$ $cm^{-3}s^{-1}$ by ~3 orders of magnitude. This large discrepancy is likely the result of the density of interface traps, D_{it}, at the ZrO_2/InAs interface being unaccounted for in the simulation. The electric field in the actual device is therefore lower than in the simulation as a result of reduced gating efficiency due to D_{it}. It is also possible that there are other effects due to quantum confinement that are not fully taken into account by the simulation. Further studies are needed to find the reason for this discrepancy.

The simulated band-to-band tunneling contour plots and the corresponding vertical band diagrams for the device in the *ON* (V_{GS} = 0.65V) and *OFF* (V_{GS} = -0.25V) states at V_{DS} = 0.1V are shown in Figure 48. The band-to-band tunneling current has vertical and lateral contributions as clearly shown on the contour plot (Figure 48a). The tunneling current is dominated by the vertical contribution, as well as a mixed vertical-lateral contribution where band-to-band tunneling occurs perpendicular to the energy band contour (i.e. at a ~45 degree angle to the *Depth* axis on the contour plot). Figure 48b shows the vertical band diagram for the device in the *ON* state. Since the p^+ side of the tunnel junction overlaps the gate, it can be inverted at the surface for positive V_{GS}. This surface inversion is particularly easy to achieve at a relatively small V_{GS} for a small band gap semiconductor like InAs.

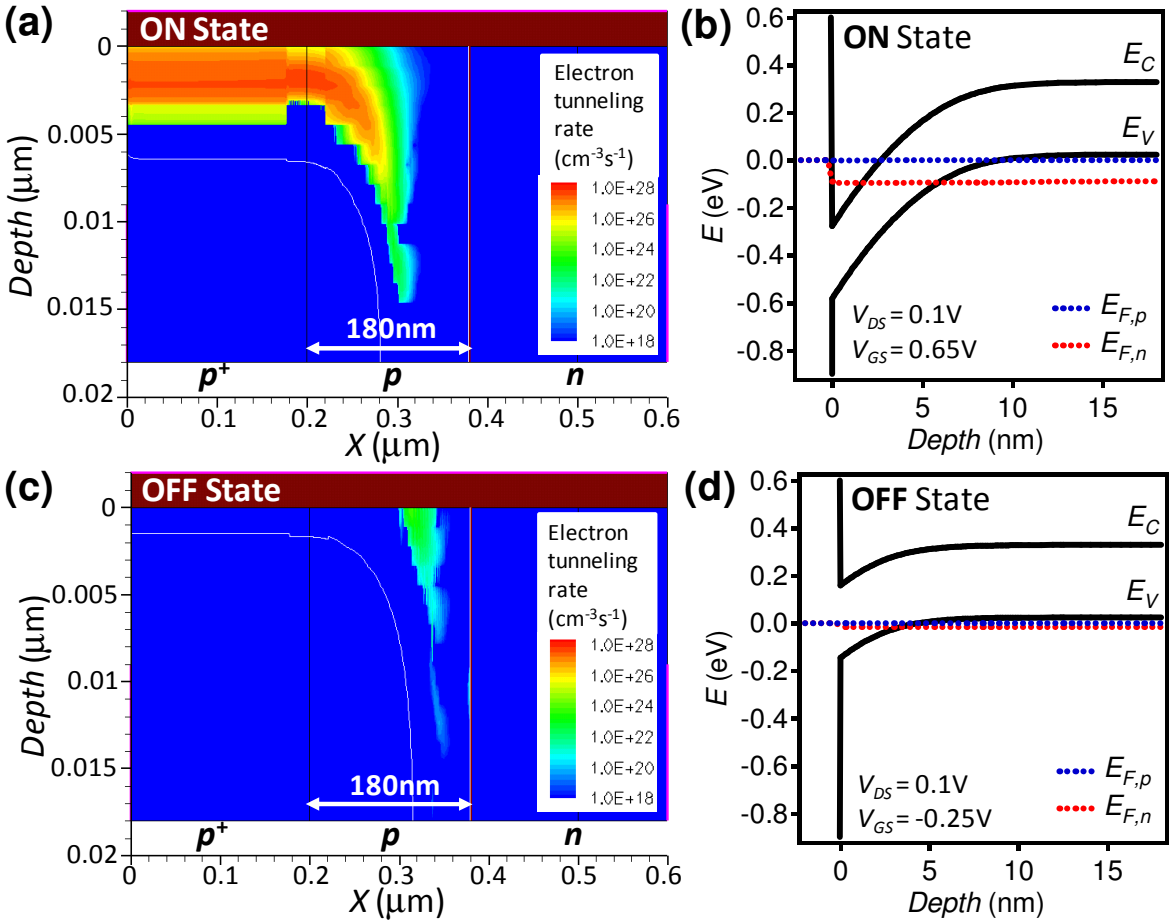

Figure 48. Simulated band-to-band tunneling contour plots and the corresponding vertical band diagrams for the device in (a, b) *ON* (V_{GS} = 0.65V) and (c, d) *OFF* (V_{GS} = -0.25V) states at V_{DS} = 0.1V.

Here, the valence band overlaps the conduction band in the vertical orientation, a large electric field is present (1.3×10^6 V/cm) and the depletion width is small (<10 nm). Because of this, a high vertical band-to-band tunneling current results as the electrons tunnel from the valence band into the conduction band. The vertical depletion width of <10 nm is significantly smaller than the

lateral junction abruptness of ~180 nm achieved by zinc doping, resulting in the vertical tunneling being the dominant current component.

To better characterize the XOI TFETs, temperature dependent electrical measurements were performed. Figure 49a shows the temperature dependent transfer characteristics of a device for V_{DS} = 0.1V.

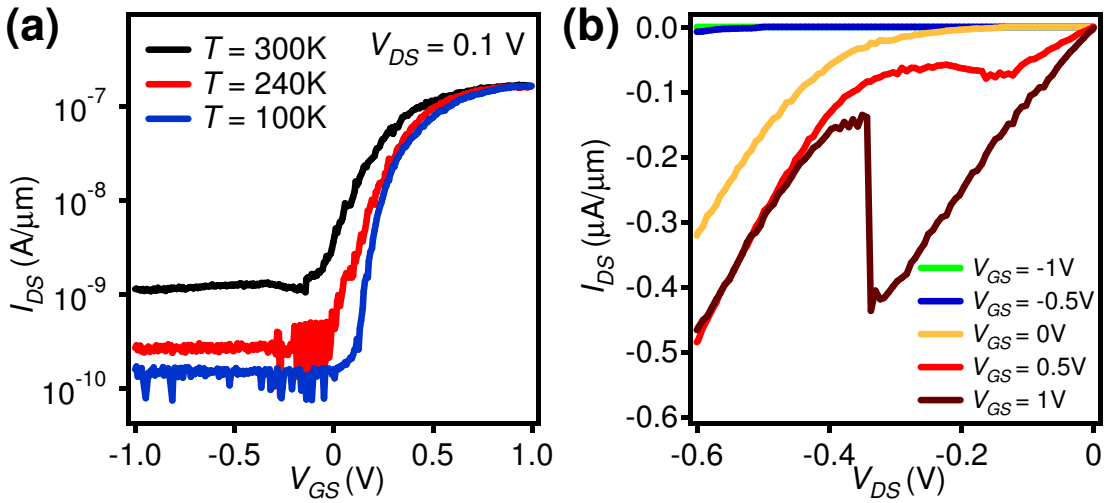

Figure 49. Temperature dependent (a) transfer characteristics of a representative TFET for V_{DS} = 0.1V, and (b) output characteristics at 100 K showing NDR in forward bias.

The *OFF*-state current and sub-threshold swing decrease with decreasing temperature, while the *ON* current is nearly independent of temperature. The *OFF*-state current in the device is most likely dominated by the Shockley-Read-Hall generation-recombination current, which is strongly dependent on temperature through the intrinsic carrier concentration, and the background thermal radiation effect.[116,117] In addition, at low temperatures, interface traps freeze out, resulting in the reduction of TAT and *SS*. Specifically, *SS* is ~60mV/dec at 100 K and increases with temperature to ~190mV/dec at 300 K. Figure 49b shows the temperature dependent output characteristics at 100 K showing NDR in forward bias. The NDR peak-to-valley current ratio increases at low temperatures and is ~3 at 100 K. This compares well to the peak-to-valley ratio of 2 at 150 K reported in the literature for an InGaAs TFET.[116]

The best reported III-V TFET to date has an *ON* current density of ~50 μA/μm, *ON*/*OFF* ratio >10^4 and *SS* ~93 mV/dec at V_{DS} = 1.05V for a channel length *L*=100nm.[40] This TFET is based on a MBE grown InGaAs n^+-*n*-*i*-p^+ structure on InP with in-situ doping during growth to ensure abrupt junctions to maximize tunneling current. The figures of merit shown here are respectable given that a non-ideal dopant (Zinc) was used for the p^+ S junction formation and the device has a long channel of *L*~2.5 μm. However, this InAs XOI TFET is fabricated on a Si substrate which presents a route for future manufacturing. The XOI TFET figures of merit shown here can be improved by scaling the device dimensions, further improving the surface properties, using a slower diffusing dopant, or other more optimal III-V materials stack, including heterojunctions.

Chapter 6: Conclusions

Here both a "bottom-up" and "top-down" approach have been demonstrated for the fabrication and integration of InAs nanostructures on Si/SiO_2 substrates. For the "bottom-up" approach, a method to grow single crystalline, high-mobility InAs nanowires on amorphous substrates by the VLS/VSS process with the use of Ni catalysts has been shown. Ni nanoparticles are shown to serve as effective catalysts for InAs nanowire growth. The high performance nanowire back-gate devices have typical electron field-effect mobilities of ~3,000-5,000 cm^2/Vs and I_{ON}/I_{OFF} ~10^4. The high yield and good quality of the as-grown InAs nanowires allow for the successful aligned transfer of nanowires from the growth substrate to a receiver substrate by a contact printing process. For the "top-down" approach, a method to epitaxially transfer ultrathin layers of single-crystalline InAs on Si/SiO_2 substrates (XOI) is demonstrated. A high quality InAs/dielectric interface is obtained by using a thermally grown ~1 nm thick interfacial $InAsO_x$ layer. Top-gated ultrathin body InAs FETs made using this epitaxial transfer approach have a peak transconductance of ~1.6 mS/μm at V_{DS}=0.5V, I_{ON}/I_{OFF} >104, and subthreshold swings of 107-150 mV/decade for a channel length of ~0.5 μm. The abilities to grow high mobility, printable InAs nanowires and epitaxially transfer ultrathin layers of single-crystalline InAs onto Si/SiO_2 substrates may allow for future integration of InAs nanostructures for various electronic applications. For the InAs XOI, more research on the scalability of the process for waferscale processing is needed. Wafer bonding of Si/SiO_2 and III-V wafers followed by etching of a sacrificial layer may be a means toward the manufacturable processing of ultrathin InAs or other III-V XOI devices.

In addition to fabrication of InAs nanostructures, the intrinsic electronic properties of the InAs nanostructures are studied using *C-V* and *I-V* measurements. The *C-V* behavior of single InAs nanowire-FETs was studied for different temperatures and measuring frequencies. From *C-V* measurements, information regarding C_{ox}, C_{it} and D_{it} was acquired to allow for the accurate extraction of the field-effect mobility. The room temperature, field-effect mobility is found to linearly increase with radius over a nanowire radius range of r=7-18 nm. The dependence of mobility on radius at low temperature (50K) where the phonons and interface traps are thermally frozen out shows the enhanced role of surface transport and surface scattering in smaller radius nanowires. Similarly, for ultrathin layers of InAs, the field-effect mobility is found to increase with increasing layer thickness. For small thicknesses (T_{InAs} < ~18), the field-effect mobility linearly increases, then at larger thicknesses nearly saturates. This suggests a gradual transition from a 2D to 3D system as the thickness is increased past the Bohr radius, with more sub-bands contributing to the current flow. Given that smaller radius or thickness InAs nanostructures are more desirable from an electrostatic point of view, but are less advantageous due to their lower mobilities, this indicates that trade-offs will have to be made for their device integration.

Following fabrication and electrical characterization of the InAs nanostructures, methods were developed to effectively post-growth, pattern *n*- and *p*-dope them using surface doping processes that minimize lattice damage. First, *n*-doping of InAs substrates with sulfur to ultrashallow junction depths with sharp junction interfaces was developed by using a monolayer doping approach. The junctions were characterized by TEM/EDS and SIMS. Diodes made from junctions exhibited NDR behavior, confirming the heavy doping of ~$8x10^{18}$ cm^{-3} and sharp junction abruptness. Second, an equilibrium-based method to heavily *p*-dope InAs nanowires and ultrathin epitaxially transferred InAs layers by Zinc gas-phase surface diffusion is demonstrated. The electrically active [Zn] is estimated to be ~$1x10^{19}$ cm^{-3} from blank (unpatterned) doping of the nanostructures. Through use of patterned doping, InAs nanowire and ultrathin body *p*-

MOSFETs are achieved. While InAs *p*-MOSFETs are not ideal devices due to the low hole mobility of InAs, this shows the effectiveness of the patterned doping approach for fabrication of different device structures. Next, this post-growth, patterned doping technique is used to demonstrate an ultrathin body InAs TFET on Si substrate. This shows the possibility of integrating high performance III-V materials with existing Si technology for various device structures. The InAs TFET on Si substrate operates by vertical band-to-band tunneling as the dominant *ON* current contribution, making the device performance less sensitive to the lateral junction abruptness. In the future, InAs XOI devices with abrupt lateral junctions can be fabricated by using a different dopant to examine the device performance as a function of lateral versus vertical tunneling current components.

Fabrication and electrical characterization of various device structures indicates that both the sulfur monolayer doping and zinc gas phase doping approaches are promising as ways toward the well-controlled, post-deposition doping of III-V semiconductors at the nanoscale, which may not be compatible with conventional ion implantation processes. This is a critical step toward the development of nanoscale III-V transistors.

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