UNIVERSITY OF CALIFORNIA, SAN DIEGO

A W-Band SiGe 4×4 Polarimetric Transmit-Receive Phased Array and CMOS THz Multiplier Arrays

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronic Circuits and Systems)

by

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Professor William S. Hodgkiss

2013

The dissertation of Fatih Golcuk is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

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DEDICATION

To my parents, Duran and Hatice

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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- F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90-100 GHz 4×4 SiGe BiCMOS Polarimetric Transmit-Receive Phased Array with Simultaneous Receive-Beams Capabilities," *IEEE Trans. Microwave Theory and Tech.*, vol. 61, no. 8, pp. 3099-3114, Aug. 2013.
- F. Golcuk, T. Kanar, and G. M. Rebeiz, "A 90-100 GHz 4×4 SiGe BiCMOS Po-

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Chapter 3 is based on and mostly a reprint of the following papers:

- F. Golcuk, O. D. Gurbuz, and G. M. Rebeiz, "A 0.37-0.43 THz 2×4 Amplifier-Quadrupler Array with Peak EIRP of 3-4 dBm in CMOS 45nm SOI," *IEEE Transactions on Microwave Theory and Techniques*, submitted for publication, June 2013.
- F. Golcuk, A. Fung, and G. M. Rebeiz, "A 0.37-0.43 THz Wideband Quadrupler with 160 μW Peak Output Power in 45 nm CMOS," *IEEE IEEE Int. Microwave Symp.*, pp. 1-4, June 2013.

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- F. Golcuk, J. M. Edwards, B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz, "A 163-180 GHz 2×2 Amplifier-Doubler Array with Peak EIRP of 5 dBm," *IEEE Radio Frequency Integrated Circuit Symp.*, pp. 363-366, June 2013.

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M. Uzunkol, F. Golcuk, B. Cetinoneri, Y. A. Atesal, O. D. Gurbuz, J. M. Edwards, and G. M. Rebeiz, "Millimeter-wave and terahertz sources and imaging systems based on 45nm CMOS technology," *IEEE Int. Microwave Symp. Dig.*, pp. 1-3, June 2012.

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ABSTRACT OF THE DISSERTATION

A W-Band SiGe 4×4 Polarimetric Transmit-Receive Phased Array and CMOS THz Multiplier Arrays

by

Fatih Golcuk

Doctor of Philosophy in Electrical Engineering (Electronic Circuits and Systems)

University of California, San Diego, 2013

Professor Gabriel M. Rebeiz, Chair

The thesis presents a W-band transmit-receive phased array and THz multiplier arrays in SiGe BiCMOS and CMOS technologies. First, a 4×4 transmit/receive SiGe BiCMOS phased array chip in an advanced SiGe technology (IBM8HP) at 90-100 GHz with vertical and horizontal polarization capabilities, 3-bit gain control (9 dB) and 4-bit phase control is presented. The 4×4 phased array fits into a 1.6×1.5 mm^2 grid, which is required at 94 GHz for wide scan-angle designs. The chip has simultaneous receive beam capabilities (V and H) and this is accomplished using dual-nested 16:1 Wilkinson combiners/divider with high isolation. The phase shifter is based on a vector-modulator with optimized design between circuit level and electromagnetic simulation and results in < 1 dB and $< 7.5^\circ$ rms gain and phase error, respectively, at 85-110 GHz. The behavior of the vector modulator phase distortion versus input power level is investigated and measured, and design guidelines are given for proper operation in a transmit chain.

The V and H receive paths result in a gain of 22 dB and 25 dB, respectively, a noise figure of 9-9.5 dB (max. gain) and 11 dB (min. gain) measured without the T/R switch, and an input P_{1dB} of -31 to -26 dBm over the gain control range. The measured output P_{sat} is $\sim$-5 dBm per channel, limited by the T/R switch loss. Measurements show $\pm$0.6 dB and $\pm$0.75 dB variation between the 4$\times$4 array elements in the transmit mode (P_{sat}) and receive mode, respectively, and $<$ -40 dB coupling between the different channels on the chip. The chip consumes 1100 mA from a 2 V supply in both the transmit and receive modes. The design can be scaled to $>$ 10,000 elements using polyimide redistribution layers on top of the chip and the application areas are in W-band radars for landing systems.

Next, a CMOS amplifier-multiplier-antenna array capable of generating an EIRP of 3-4 dBm at 420 GHz is presented. The chip is built using a 45nm CMOS SOI (IBM12SOI) process and efficient on-chip antennas are used to extract the power out of the chip. The design is based on a 90-110 GHz distribution network with splitters and amplifiers, and a balanced quadrupler capable of delivering up $>$ 100 μW of power at 370-430 GHz. The amplifier-multiplier concept is proven on a 2$\times$4 array, and can be also scaled to any N$\times$M array using additional W-band splitters and amplifiers.

Finally, a 2$\times$2 amplifier-multiplier array with on-chip antennas at 163-180 GHz in 45 nm CMOS SOI technology is presented. The measured EIRP is $>$ 2 dBm at 165-175 GHz with a peak value of 5 dBm at 170 GHz meeting the stringiest metal-density rules for antennas. The design is based on a 80-100 GHz distribution network with splitters and amplifiers, and a balanced doubler capable of delivering up $>$ 0.5 mW of power at 170-190 GHz.

Chapter 1

Introduction

1.1 Phased Array Systems

Phased array systems are widely used in radars and communications systems for beam forming and scanning [1–5]. The relative phases of received or transmitted signal are controlled by a phased array systems to steer the effective radiation pattern of an antenna array to a particular direction to construct the signals in desired direction and suppress the signal in undesired direction. The spatial filtering of the phased array increases the spectral efficiency of the receive (transmit) system [6]. The phased array system increases the signal-to-noise ratio (SNR) by combining the signal coherently and noise incoherently from the different elements, results in higher data rate systems [1]. The effective pattern is shaped by controlling the amplitude of the each antenna element and the direction of the beam is controlled by the phase weighting at each antenna element. The beam steering can be done by mechanically or electronically. In mechanically steering array, the antenna reflective surface is rotated mechanically to determine the beam angle. However, the phase and amplitude is weighted electronically in electronically scanned arrays and thus the beam steering and shaping are much faster than mechanical systems [1,7]. Fig. 1.1 shows the conceptual block diagram of the 8-element received phased array. The incoming signal from the desired angle θ reaches the each antenna element with a time difference of ΔT , which creates $\Delta\phi$ phase difference between the antenna element, where

$$\Delta T = \frac{dcos\theta}{c}, \Delta\phi = kdcos\theta, k = \frac{2\pi}{\lambda} \tag{1.1}$$

and d is the distance between the elements, λ is the wavelength, and c is the speed of light. Thus, the progressive phase shift, $\Delta\phi$, between the antenna elements is required in electronically beam

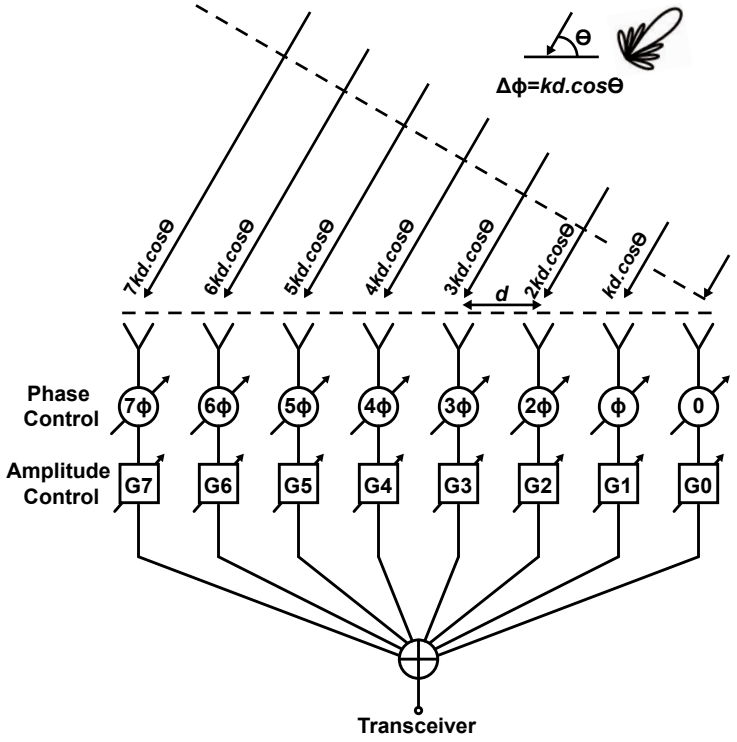

Figure 1.1: An 8-element phased array block diagram.

steering arrays to receive the signal from desired direction, θ. The phase and amplitude difference between the elements are compensated by variable time delay and variable amplifier (or variable attenuator) to sum the desired signal constructively while adding the signals in the undesired direction de-constructively. Time delays can be employed as phase shifters to compensate the time delay between the elements in narrow band systems since the carried information change slowly in the narrow band applications. Using silicon technologies, both variable phase shifters and gain blocks together with all digital controls can be realised in single chip, and hence it can replace the complex and bulky modules which use III-V technologies.

1.2 Phased Array Architectures

The phase shifting to compensate the time delay between the antenna elements to add them in-phase at the sum port can be done in the RF [8–16], LO [17–19], IF [20] paths or the digital domain [21, 22] of the receiver modules(Fig. 1.2). An RF phase shifter is employed in each element in the RF phase shifting (All-RF) architecture to compensate the time delay

between the elements and the signal is summed in RF domain constructively before the mixer (Fig. 1.2(a)). In the LO phase shifting architecture, each channel requires a mixer and a LO signal with variable phase, an hence results in more complex and power hungry systems (Fig. 1.2(b)). In the IF phase shifting architecture, similar to the LO phase shifting architecture, a mixer at each channel and a LO distribution network are required, but the phase shifters are employed in IF paths (Fig. 1.2)(c)). In the digital beam-forming architecture, the phase of the each element is processed in the digital domain using baseband signal processing techniques (Fig. 1.2)(d)). This architecture can be configured to have multiple beams and polarization. However, it requires high dynamic range A/D converters at each channel, and hence results in a more power consumption system.

Among these architectures, the All-RF architecture is the most commonly used since it requires only one mixer while the other architecture require a mixer at each channel and an LO distribution network. Thus, a more compact phased array and less power consumption can be achieved in the All-RF architecture. The other advantage of this architecture is that the desired signals are summed in RF domain constructively and the interferers are added de-constructively. Thus, the interferers are suppressed before the non-linear mixing and this architecture results in higher signal-to-interferer ratio (SIR). The mixer's linearity and A/D converter's dynamic range are relaxed due to the high SIR. However, disadvantage of the All-RF architecture is the high loss of the RF phase shifter and RF combiner network, but the loss can be compensated using an active phase shifter or using gain blocks in the RF path.

1.3 THz Multiplier Arrays and Wafer Scale Approach

THz systems have being used for various applications at THz frequencies, such as short distance high data rate communication, radio astronomy, sensor systems, and active and passive imaging [23–38]. The systems at THz frequencies are dominated by III-V technologies. However, advance silicon technologies with high f_t and f_{max} can replace III-V technologies at THz frequencies and are becoming popular for THz applications. Signal sources are one of the key building blocks of the communication, active imaging and atmospheric remote sensing systems. Signal can be generated at THz frequencies using injection-locked or N-push oscillator [37, 39, 40] and multipliers [41–43]. Multipliers have better phase noise performance than oscillators which have poor phase noise performance due to operating close to f_{max} since the source at lower frequencies has low phase noise and can be locked to a low frequency reference using a phase-locked-loop (PLL). Another advantage of the multiplier approach is to have the

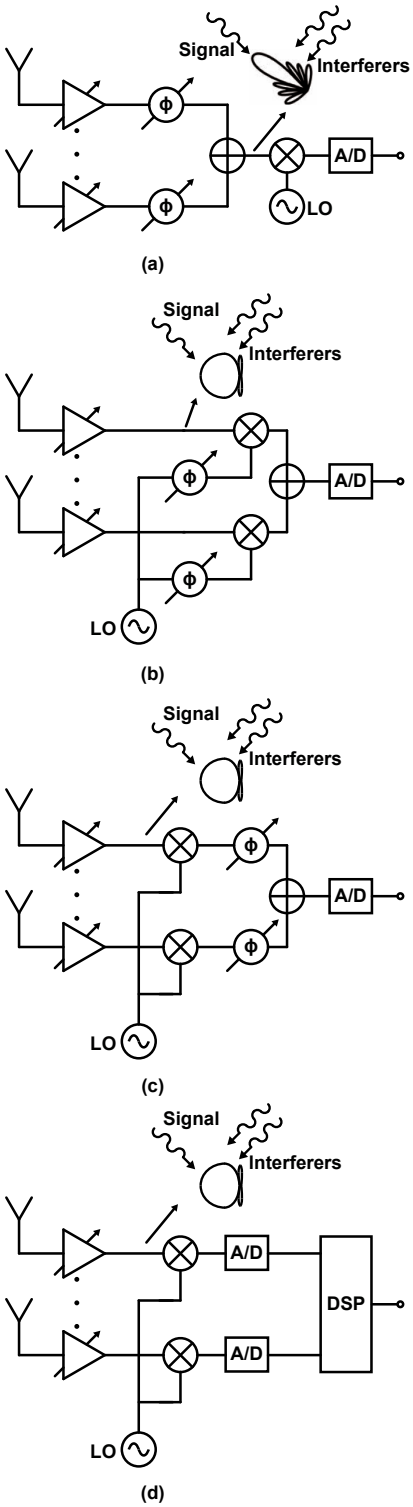

Figure 1.2: Phased array receiver architectures: (a) RF phase shifting, (b) LO phase shifting, (c) IF phase shifting and (d) digital beam forming.

higher frequency bandwidth than the oscillator approach. The multiplier approach is scalable to large N×M arrays using high efficiency on-chip antennas since the distribution network is at lower frequencies and has much less loss. Also, phase shifters can be integrated to scan the beam.

1.4 Thesis Overview

The thesis presents a 90-100 GHz 4×4 SiGe BiCMOS polarimetric transmit-receive phased array with simultaneous receive-beams capabilities and THz multiplier arrays using 45 nm CMOS SOI process.

Chapter 2 presents a 4×4 transmit/receive SiGe BiCMOS phased array chip in an advanced SiGe technology (IBM8HP) at 90-100 GHz with vertical and horizontal polarization capabilities, 3-bit gain control (9 dB) and 4-bit phase control. The 4×4 phased array fits into a 1.6×1.5 mm^2 grid, which is required at 94 GHz for wide scan-angle designs. The chip has simultaneous receive beam capabilities (V and H) and this is accomplished using dual-nested 16:1 Wilkinson combiners/divider with high isolation. The phase shifter is based on a vector-modulator with optimized design between circuit level and electromagnetic simulation and results in $<$ 1 dB and $<$ 7.5° rms gain and phase error, respectively, at 85-110 GHz. The behavior of the vector modulator phase distortion versus input power level is investigated and measured, and design guidelines are given for proper operation in a transmit chain. The V and H receive paths result in a gain of 22 dB and 25 dB, respectively, a noise figure of 9-9.5 dB (max. gain) and 11 dB (min. gain) measured without the T/R switch, and an input P_{1dB} of -31 to -26 dBm over the gain control range. The measured output P_{sat} is ∼-5 dBm per channel, limited by the T/R switch loss. Measurements show ±0.6 dB and ±0.75 dB variation between the 4×4 array elements in the transmit mode (P_{sat}) and receive mode, respectively, and $<$ -40 dB coupling between the different channels on the chip. The chip consumes 1100 mA from a 2 V supply in both the transmit and receive modes. The design can be scaled to $>$ 10,000 elements using polyimide redistribution layers on top of the chip and the application areas are in W-band radars for landing systems.

Chapter 3 presents a CMOS amplifier-multiplier-antenna array capable of generating an EIRP of 3-4 dBm at 420 GHz. The chip is built using a 45nm CMOS SOI (IBM12SOI) process and efficient on-chip antennas are used to extract the power out of the chip. The design is based on a 90-110 GHz distribution network with splitters and amplifiers, and a balanced quadrupler capable of delivering up $>$ 100 μW of power at 370-430 GHz. The amplifier-multiplier concept

is proven on a 2×4 array, and can be also scaled to any N×M array using additional W-band splitters and amplifiers.

Chapter 4 presents a 2×2 amplifier-multiplier array with on-chip antennas at 163-180 GHz in 45 nm CMOS SOI technology. The measured EIRP is $>$ 2 dBm at 165-175 GHz with a peak value of 5 dBm at 170 GHz meeting the stringiest metal-density rules for antennas. The design is based on a 80-100 GHz distribution network with splitters and amplifiers, and a balanced doubler capable of delivering up $>$ 0.5 mW of power at 170-190 GHz.

Chapter 2

A 90-100 GHz 4×4 SiGe BiCMOS Polarimetric Transmit-Receive Phased Array with Simultaneous Receive-Beams Capabilities

2.1 Introduction

SiGe and CMOS RFICs are now the technology of choice for millimeter-wave phased arrays due to their high f_t/f_{max} and density of integration. Designs with 8-32 elements based on the All-RF architecture have been successfully demonstrated at 45-110 GHz in transmit (Tx), receive (Rx) or transmit/receive (T/R) modes [8–15]. The silicon designs allow the integration of several elements on the same chip, together with the power combining network, up/downconversion blocks, synthesizers, and all the necessary digital control electronics. The silicon designs also result in nearly identical response between the different channels and allow for compact built-in self-test circuitry, which greatly reduces the cost of mm-wave phased array systems [13, 44].

This paper presents the first 90-100 GHz 4×4 phased array with full polarimetric capabilities. The chip is designed for a W-band radar system consisting of $>$ 10,000 elements, and requires vertical (V) and horizontal (H) polarization capabilities in both the transmit and receive modes [45]. In this design, the transmit mode is sequentially polarimetric, that is, a single polarization is transmitted at a time (V or H). On the other hand, the receive mode is fully polarimetric and two simultaneous phased-array receivers, one for the vertical and one for the

horizontal polarization, are employed. This requires that two nested 16:1 Wilkinson combiner networks be used in the receive mode, each with an equiphase distribution to all the 16-elements for ease of system calibration (Fig. 2.1).

The 4×4 phased array chip will be packaged using polyimide layers above the top metal surface (typically called RDL Redistribution Layers or CSP - chip-scale package). These layers contain short RF distribution sections and connect the 4×4 outputs of the RFIC to the 94 GHz antennas. They also contain the global RF signal distribution layer, DC feeds and digital control lines, and result in an extremely low RF and DC ground and supply inductance. This technology has been used with success at 45 GHz [46] and 77 GHz [47] and is readily scalable to 94 GHz.

The 4×4 phased array must also fit into an area less than the $\lambda/2$ spacing at 94 GHz (1.6 mm) for wide scan-angle performance. The size of the RFIC unit cell consisting of a transmit and two receive chains, and the Wilkinson couplers, is 1.6×1.5 mm^2, meeting this requirement. Finally, the chip consumes 1100 mA (simulated 950 mA) from a 2 V supply in the receive and transmit modes, which is low enough to allow for large subarrays (256 elements) using the RDL technology.

2.2 Design

The single-element block diagram with the required polarimetric capabilities is shown in Fig. 2.2. The design is single-ended due to the compact size requirements for each phased array cell, and the low ground inductance (2-5 pH) offered by the chip-scale package. The chip is fabricated in the IBM8HP SiGe BiCMOS process with an f_t/f_{max} of 200 GHz, 0.12 μm CMOS transistors, and 7 metal layers with 2 thick top metals (Fig. 2.3). Grounded coplanar waveguide (G-CPW) transmission lines are used throughout the chip with a simulated loss of 1 dB/mm and 1.2 dB/mm at 90-100 GHz for 50 Ω and 70 Ω designs, respectively.

Each element is composed of two receive paths, a power amplifier with an active switch for V and H selection in the transmit path, and CMOS single-pole double-throw (SPDT) switches for T/R control. Also, active phase shifters using vector modulators are employed since passive phase shifters result in high loss at W-band frequencies using 0.12 μm CMOS [48, 49]. Therefore, each unit element also requires three phase shifters, one in the transmit path and two in the receive paths. Note that the low noise amplifier (LNA) and power amplifier (PA) and switch are single-ended, but the active phase shifter is differential, and therefore, input and output baluns are used around each phase shifter.

All active blocks are designed with 50 Ω input and output ports so as to allow for indi-

vidual break-out testing of each block, and all transmission-lines components are simulated with Sonnet [50], a full-wave EM program, for added accuracy. A lot of effort was placed on the T/R block to reduce its size and power consumption since it is replicated 16 times in the chip. Therefore, all active circuit blocks are based on cascode designs since it provides the lowest power consumption per gain block, and the highest gain per area.

2.2.1 SPDT Switch

Starting from the V or H antenna ports, the SPDT transmit/receive switch is a tuned λ/4-shunt design since it results in lower loss at W-band frequencies than a series-shunt design (Fig. 2.4). This design has been demonstrated before at 90-100 GHz with an insertion loss of 2.3 dB at 94 GHz [32]. Also, the λ/4 section is needed for the physical separation between the (V) and (H) antenna ports. The shunt switching elements are standard CMOS transistors with a W/L=125 μm/0.12 μm which has deep trench around it to increase the substrate resistance to the ground, and a shunt-stub with an equivalent inductance of 70 pH is used to resonate out the CMOS off-state capacitance when the switch is not activated (in the pass state). The shorted shunt stub also acts as an electrostatic discharge (ESD) protection for the entire channel. The simulated insertion loss is 2.1 dB with an isolation of 25 dB at 90-100 GHz with near-zero power consumption.

2.2.2 LNA and RX Amplifier

The LNA is a two-stage cascode design biased to get moderate gain with low noise figure at 0.7 mA/μm for the first and second stages (Fig. 2.5). The first stage employs emitter degeneration for wideband input impedance matching, and a complex interstage match is used for maximum gain. Inductances are used between the common-emitter and common-base transistors and at the collector of the common-base transistors to boost the gain of the LNA [51, 52]. Also, several ground pads to the RDL system ground surround the LNA for minimum additional ground inductance. The LNA consumes 10 mA from a 2 V supply including all bias and gain control circuits and results in a simulated gain and noise figure (NF) of 18.5 and 8.3 dB, respectively, at 94-95 GHz, a 3-dB bandwidth of 85-104 GHz, and an input P_{1dB} of -25 dBm at 94 GHz. The LNA has a 4.5 dB total gain control with 1.5 dB steps using 2-bits digital control. Gain is controlled using a current steering topology in the second stage of the LNA [53].

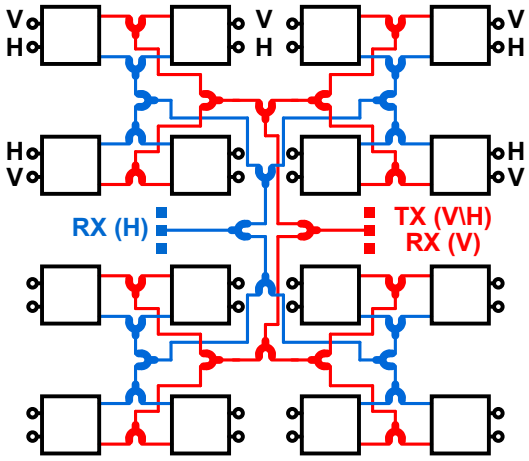

Figure 2.1: Polarimetric transmit-receive 16:1 4×4 phased array with simultaneous receive-beams and dual nested Wilkinson combiners.

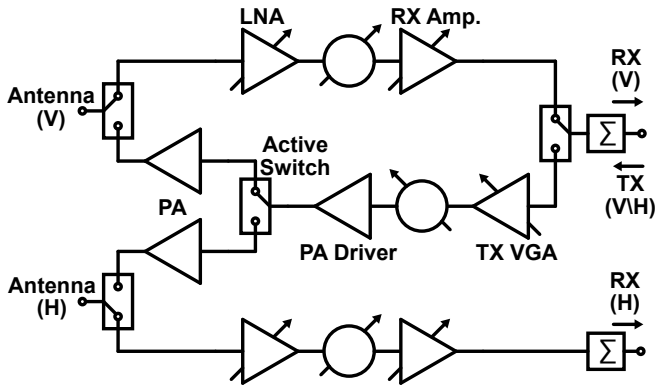

Figure 2.2: T/R unit (single element) block diagram.

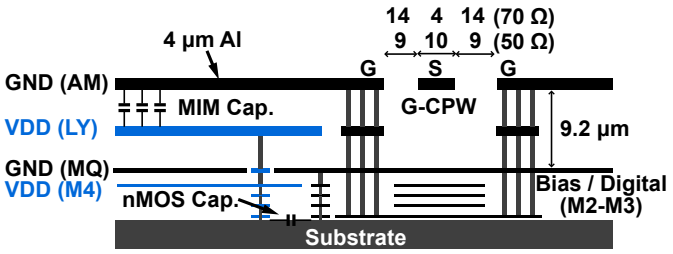

Figure 2.3: IBM8HP metal stack-up with representative 50 Ω and 70 Ω G-CPW lines.

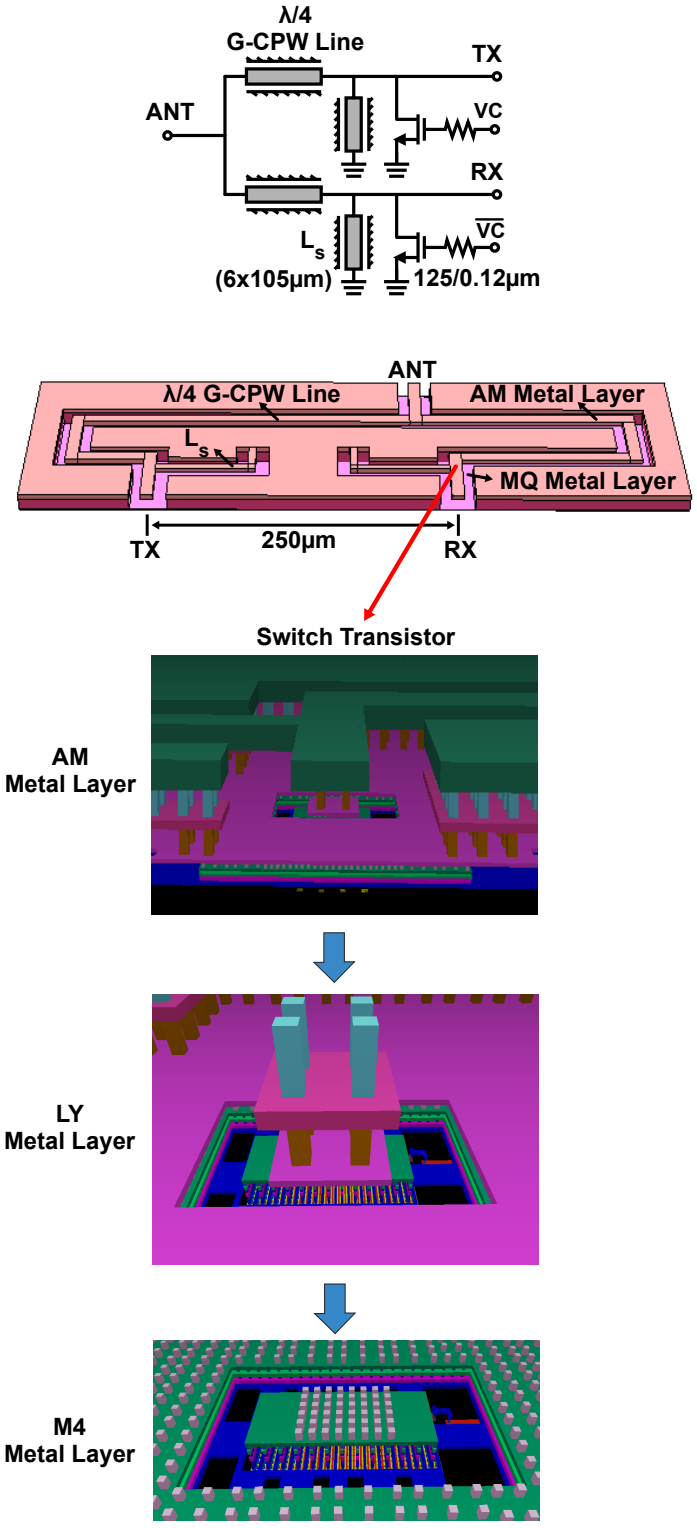

Figure 2.4: SPDT switch schematic and Sonnet layout.

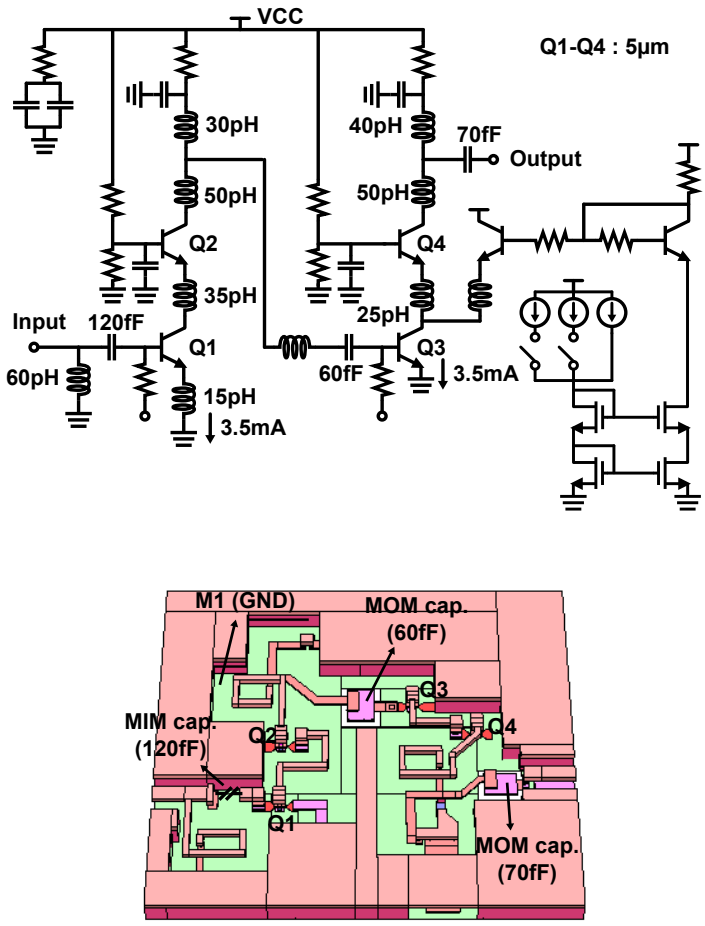

Figure 2.5: LNA with gain control schematic and Sonnet layout.

The RX amplifier has the same topology as the LNA but with different component values. It also consumes 10 mA from a 2 V supply and results in 15.5 dB gain with a 3-dB bandwidth of 83-105 GHz. The RX amplifier also uses the same current steering technique, and has 1-bit digital control for a 6 dB gain variation. The total gain control in the Rx path is therefore 10.5 dB using 3-bits.

2.2.3 Power Amplifier and Active Switch

The power amplifier is a 3-stage design with the 2^{nd} stage used as a cascode active switch with $>$ 40 dB isolation for V and H polarization control (Fig. 2.6). The input stage employs an emitter inductor for a wideband impedance match, and conjugate matching is employed between all stages for maximum power transfer. The last stage is also a class A design with P_{sat} (saturated power) of 3.5 dBm, and a PAE (power added efficiency) of 3$\%$ at 94 GHz. All biasing is done at $\sim$1-1.3 mA/μm which corresponds to maximum gain bias. Again, as with the LNA, careful layout is done to minimize parasitic inductance in the interconnects and Sonnet models are used for the MOM (metal-oxide-metal) capacitances and inductors in the Cadence simulations. The simulated gain and NF are 21 dB and 10 dB, respectively, at 94 GHz with a 3-dB gain bandwidth of 80-102 GHz. At P_{sat}, the gain drops to 16 dB, and therefore, an input power of -12.5 dBm is required to achieve full saturation. This is still low enough and the preceeding phase shifter can deliver this power level with low phase distortion.

The TX-VGA (transmit variable gain amplifier) on the transmit path is a single-stage cascode amplifier with a current steering topology for gain control (not shown). It consumes 5 mA from a 2 V supply and results in 9.5 dB gain with a 3-dB bandwidth of 81-108 GHz. It also has 5.5 dB gain control with $\sim$0.8-dB steps using a 3-bit digital control. The simulated output saturated power is -4 dBm which is enough to drive the phase shifter.

2.2.4 Phase Shifter

The phase shifter is the hardest component to design due to its interconnect complexity. Fig. 2.7 presents the phase shifter topology, which is based on a vector modulator with input and output baluns. First, the passive 50 Ω (single-ended) to 100 Ω (differential) balun is designed using the top two metal layers with an insertion loss of $<$2 dB at 90-100 GHz, and stub inductors and MOM capacitors are used for input and output matching (Fig. 2.8). This is followed by a differential I/Q network using two 3-dB distributed λ/4 couplers that are built using the top two metal layers and in a spiral configuration for compactness (Fig. 2.9) [54, 55]. This network is

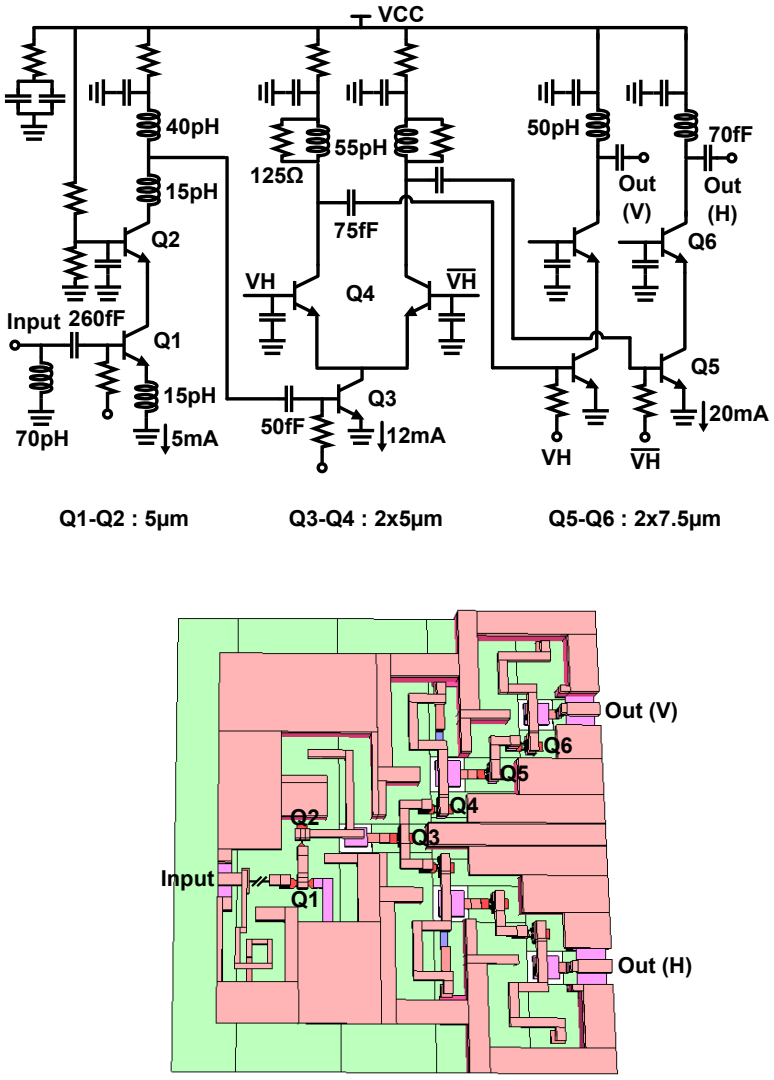

Figure 2.6: Power amplifier with active switch schematic and Sonnet layout.

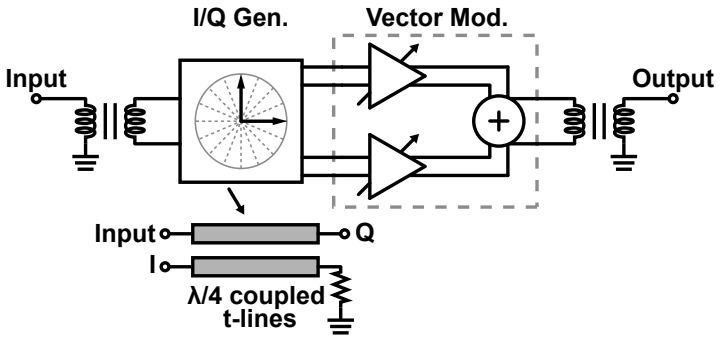

Figure 2.7: Phase shifter block diagram.

simulated using Sonnet and results in $\sim$1 dB loss at 94 GHz and a 90°$\pm$1° and $<$ 1 dB phase and amplitude difference between the I and Q outputs, respectively.

The I/Q coupler outputs are then attached to the vector modulator consisting of SiGe transistors for the variable gain stages and a 0.12 μm CMOS switching network to select the different quadrants for 180° phase shift (Fig. 2.10). The bias currents, I_I and I_Q, for the SiGe differential pairs, are controlled using a 4-bit digital-analog-converter (DAC). The output of the I and Q stages are summed together in the current domain and an output balun is used as the inductive load. Also, a differential shunt matching inductor is used at the input for a wideband impedance match (Fig. 2.11). The I_I and I_Q currents (and the DAC reference currents) are determined using Cadence simulations for the 0°, 22.5°, 45°, 67.5° and 90° phase settings by using the IBM transistor models and including all the extracted input, output, and interconnect parasitics (using Sonnet) for the I and Q paths, and are tabulated in Table 4.1. The vector modulator results in a simulated gain of -5 dB with rms gain error of 0.7 dB, a noise figure of 16 dB, an input P_{1dB} of -2 dBm all at 94 GHz.

Due to the importance of this block, breakout measurements and discussions will be presented in this section. The phase shifter breakout microphotograph is shown in Fig. 2.12. The phase shifter was measured using GSG W-band probes with SOLT calibration to the probe tips. Measurements agree well with simulations with $<$ 1 dB rms gain error and $<$ 7.5° rms phase error at 85-110 GHz (Fig. 2.13). At 95 GHz, the results show $<$ 0.8 dB and $\sim$ 3.5° rms gain and phase error, respectively, stressing the importance of full-wave simulations. Fig. 2.14 presents details of the measured gain and P_{1dB} versus 16 phase states at 94 GHz. The gain variation can be equalized using a small-step VGA, which is available in the phased array element if a better rms gain error is required.

The measured phase versus input power is presented in Fig. 2.15-(a), and is dependent

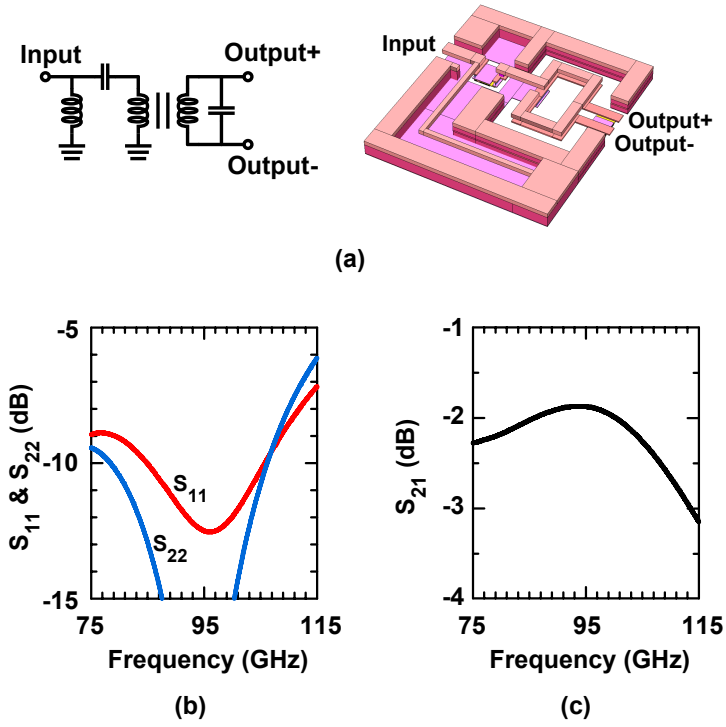

Figure 2.8: Input balun schematic, Sonnet layout and simulation results.

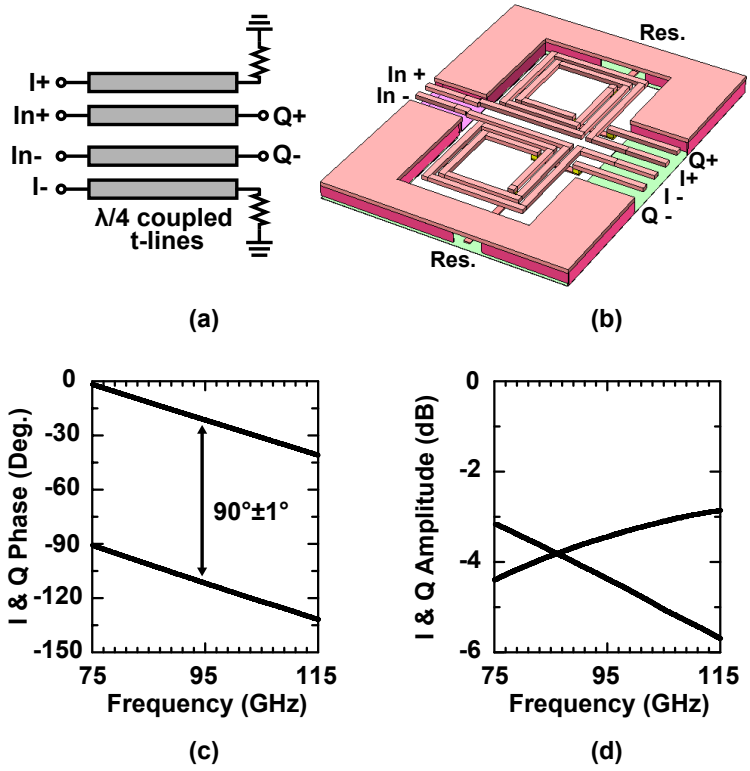

Figure 2.9: I/Q generator schematic, Sonnet layout and simulation results.

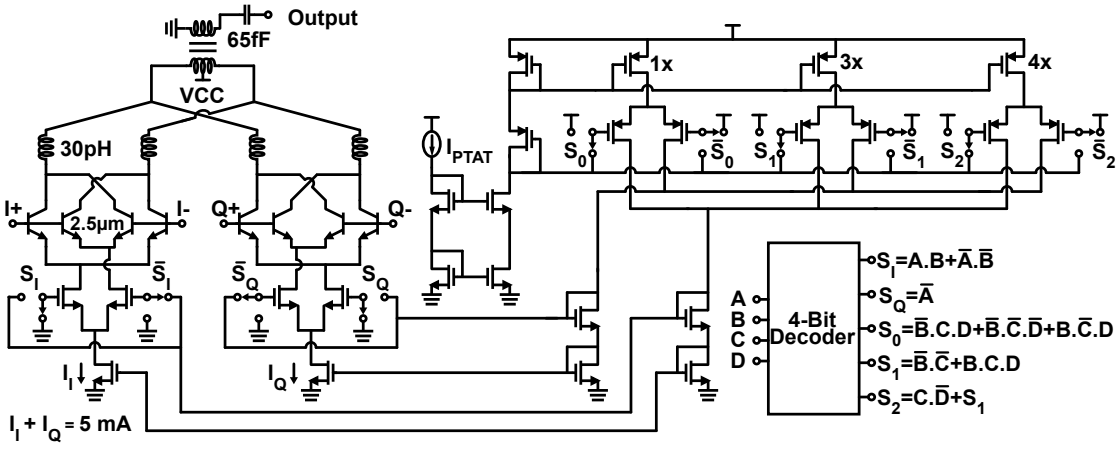

Figure 2.10: Vector modulator and DAC (Digital to Analog Converter) schematic.

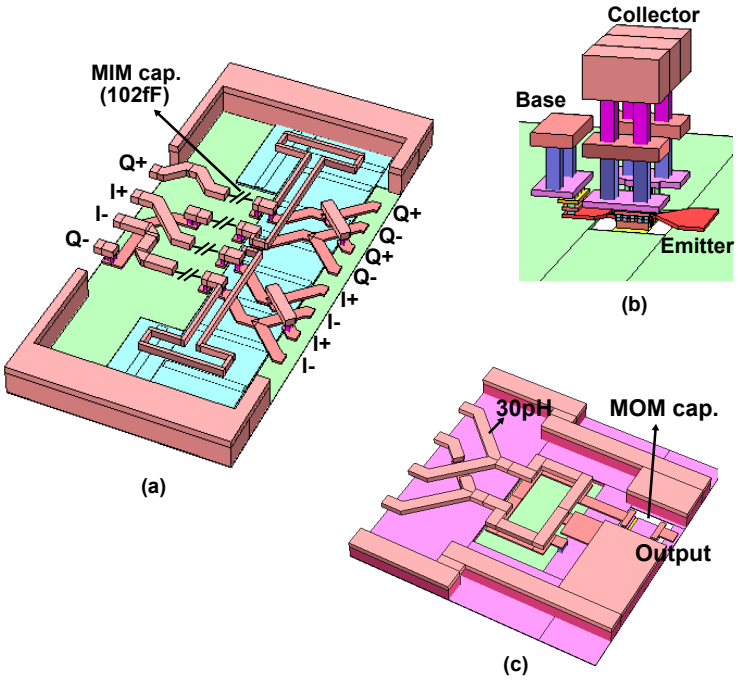

Figure 2.11: Vector modulator Sonnet layout of (a) input matching, (b) transistor interconnection and (c) output load balun.

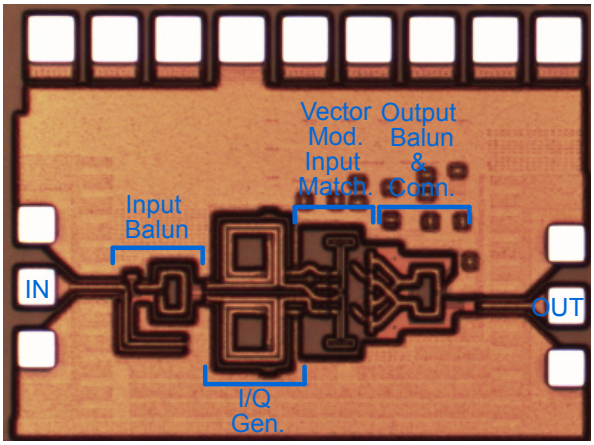

Figure 2.12: Phase shifter breakout chip microphotograph (0.75×0.65 mm^2 including DC pads).

Table 2.1: Vector Modulator I and Q Path Currents for Phase States

Phase State (Deg.)	$\mathbf{I}_I$	$\mathbf{I}_Q$
0	8x	0
22.5	7x	1x
45	4x	4x
67.5	1x	7x
90	0	8x

x = 0.625 mA

on the input power at $P_{in} >$ -10 dBm. This is explained as follows: The output current in the I and Q paths are composed of two components: a) I_x due to the collector-base capacitance and b) I_y due to the transistor g_m source. Note that these two currents are not at the same phase. Also, the collector-base (CB) capacitance is due to a p-n junction and therefore is dependent on the voltage across the CB junction. As the RF power increased, the voltage across the CB junction increases, and I_x increases more than I_y, which results in distortion in the 22°, 45° and 67° bits. Therefore, while the P_{1dB} values are $\sim$-4$\pm$2 dBm, the phase shifter should be operated around -10 dBm for low rms phase errors (Fig. 2.15 (b)).

To our knowledge, this phase shifter presents state-of-the-art performance as compared to all published W-band designs [48, 56–58].

2.2.5 Nested Wilkinson Combiners

The 4×4 chip also contains two passive 16:1 Wilkinson combiner/divider networks since one of the distribution layers must be bi-directional (carries the Tx signal and one of the Rx signals). The Wilkinson networks should also be symmetrical with an equiphase distribution to all 16 elements. This was done by nesting the two 16:1 Wilkinson combiners in the 100-200 μm space between the 4×4 elements as shown in Fig. 2.1.

Two different Wilkinson combiners with λ/4 70.7 Ω sections and different geometries are designed for the nested combiners (Fig. 2.16). Sonnet simulations show that both designs have a loss of $\sim$0.55 dB with $>$ 30 dB impedance match and isolation at 95 GHz. The combiner networks also have a large number of cross-overs and this was accomplished by moving the ground plane to the LY layer at the cross-over thus creating a ground plane island (50×50 μm^2) under the top transmission line, and lowering the other transmission line to the MQ layer (below the ground plane). Both transmission-line dimensions are also changed so as maintain a 50 Ω environment. The simulated cross-over insertion loss using Sonnet is 0.1-0.15 dB at 95 GHz, with an isolation $>$ 70 dB (Fig. 2.17).

The nested Wilkinson combiners also require transmission-lines which are electrically long and placed parallel to each other due to the narrow spacing between the T/R elements. Therefore, electromagnetic simulation was done in order to determine the minimum distance required for high isolation. A center-to-center spacing of 40-60 μm results in an isolation of 40-50 dB at 95 GHz which is sufficient for this application (Fig. 2.18).

Finally, each 16:1 Wilkinson network was simulated including the individual Wilkinson stages, connecting transmission lines and cross-overs. Both networks result in an ohmic loss of

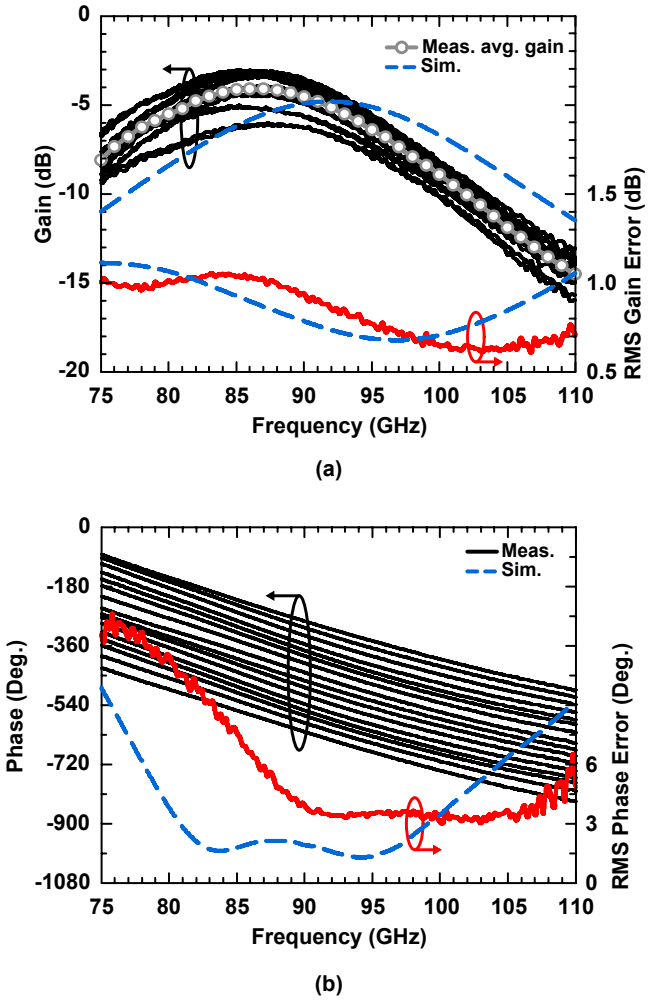

Figure 2.13: Phase shifter (a) gain and rms gain error and (b) phase and rms phase error over 16 phase states.

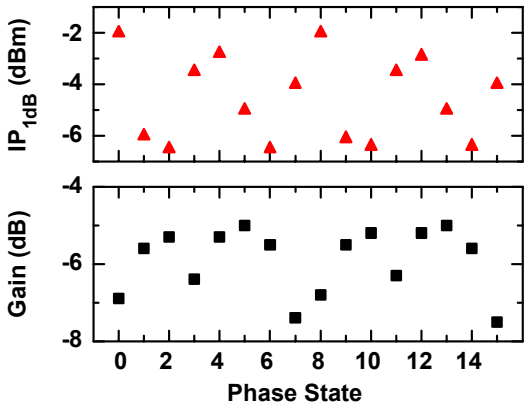

Figure 2.14: Measured gain and IP_{1dB} versus 16 phase states at 94 GHz.

5-5.5 dB at 95 GHz with a wide band impedance match (S_{nn} < -28 dB at 90-100 GHz) (Fig. 2.19). The V and H networks are individually symmetric from the common port to the 4×4 elements, so there is no phase difference in simulations. The isolation between any two elements is given mostly by the first Wilkinson coupler and is > 30 dB at 95 GHz.

2.2.6 System-Level Simulations

The gain and noise figure of a single receive channel (V or H polarization) is shown in Fig. 2.20 (a). Note that the Wilkinson combiner gain is taken as -5.5 dB since the 12 dB combining gain will be accounted for in the antenna-array gain calculations. The line-up results in 19.3 dB gain and 10.7 dB NF at 95 GHz, with an input P_{1dB} of -33 dBm which is limited by the RX amplifier. On the transmit side, the Wilkinson network is represented by 17.5 dB loss due to the 16:1 power division (12 dB) which is required to feed the 4×4 T/R modules (Fig. 2.20 (b)). The linear gain from the common port to a radiating element port is 3.8 dB, and the output P_{sat} is 1.4 dBm and is limited by the active switch PA which is followed by the SPDT switch loss. At P_{sat}, and due to gain compression in the PA, the total network gain is ∼-0.5 dB and an input power of 2 dBm is required at the common port in order to saturate all the 4×4 T/R modules.

2.2.7 Chip Power Supply and Control

The entire 4×4 phased array chip is shown in Fig. 2.21 and consumes 1100 mA from a 2 V supply in the Rx and Tx modes. To ensure the same bias current for the same components on the entire chips, a 125 μA reference current source is generated at the center of the chip

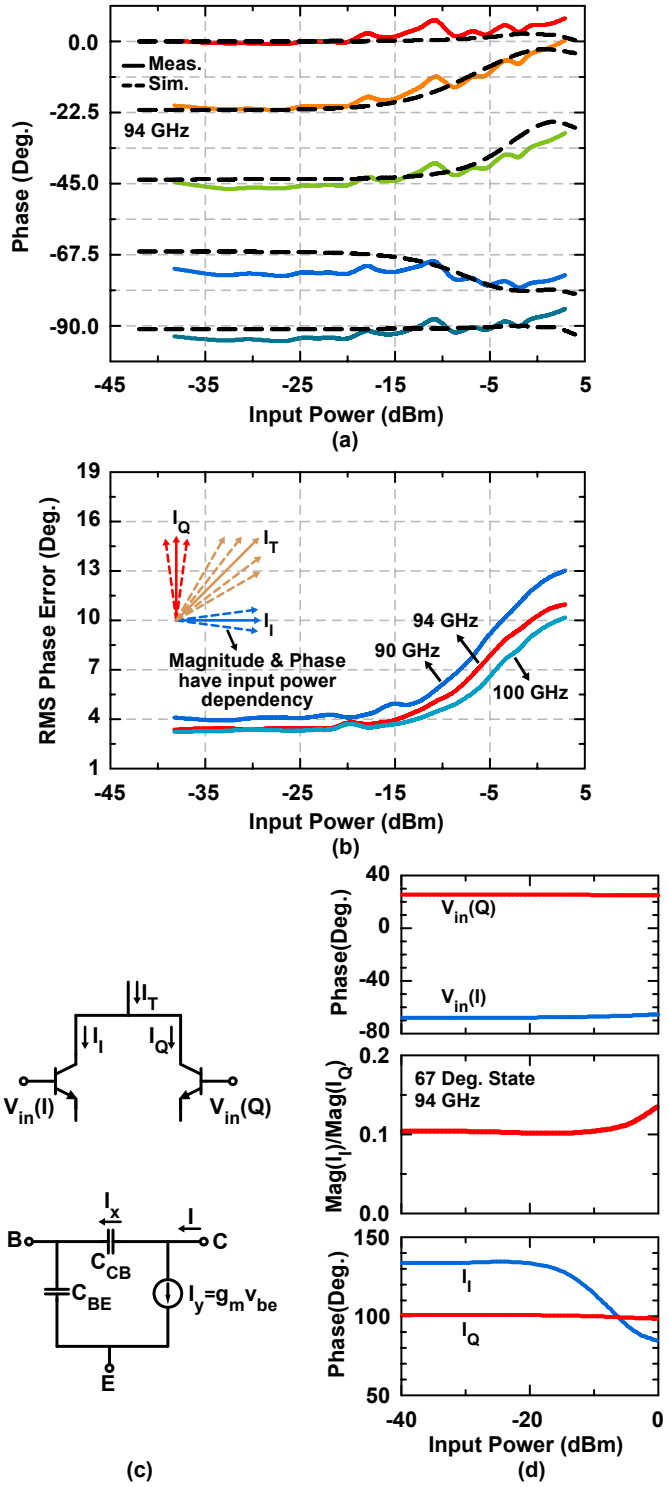

Figure 2.15: Measured (a) relative phase versus input power at 94 GHz, (b) rms phase error versus input power at 90, 94 and 100 GHz, (c) a block diagram of current components for phase shifter and (d) simulated I_I and I_Q current versus input power.

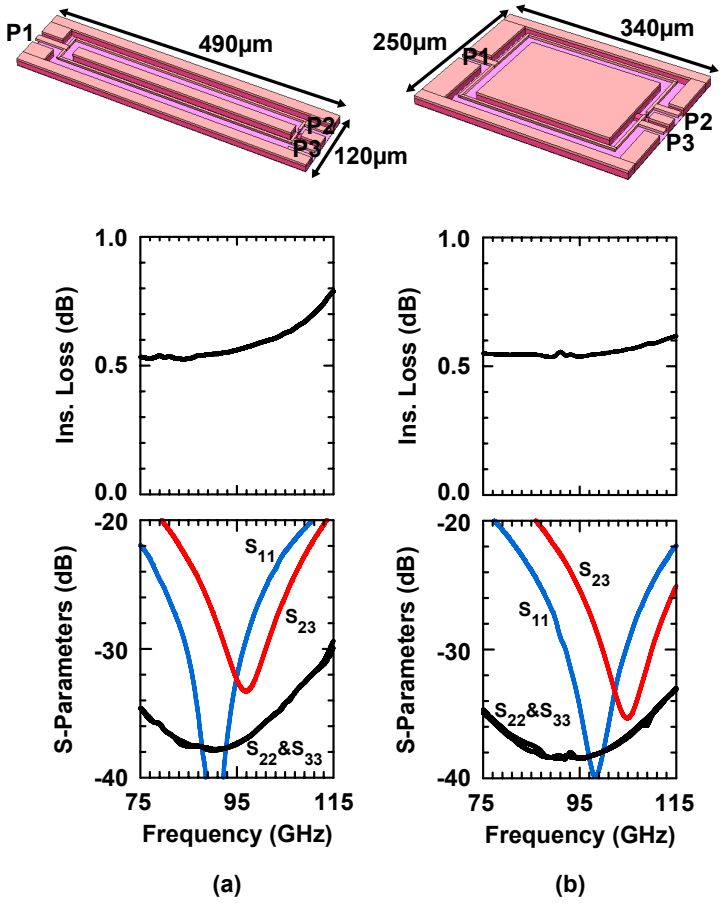

Figure 2.16: Wilkinson combiner/divider Sonnet layouts and simulated S-parameters. Two different Wilkinson combiners/dividers were used, shown in (a) and (b).

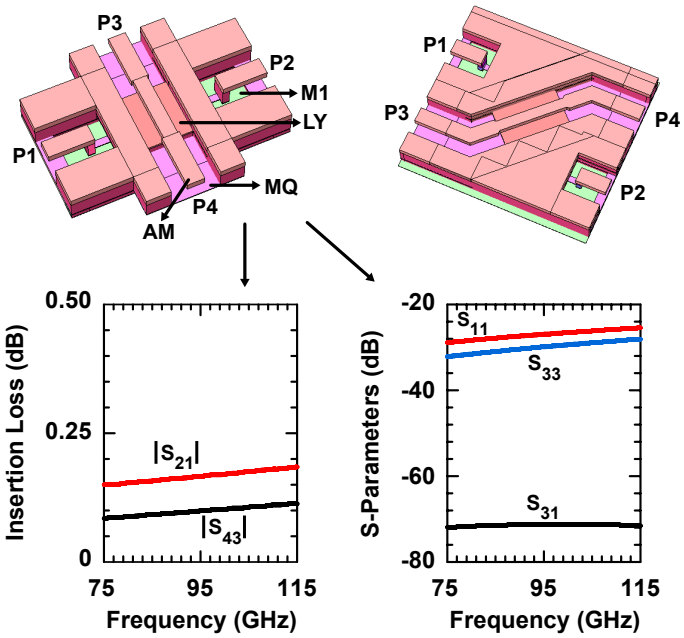

Figure 2.17: V and H polarization combiner/divider network cross-over Sonnet layouts and simulated S-parameters.

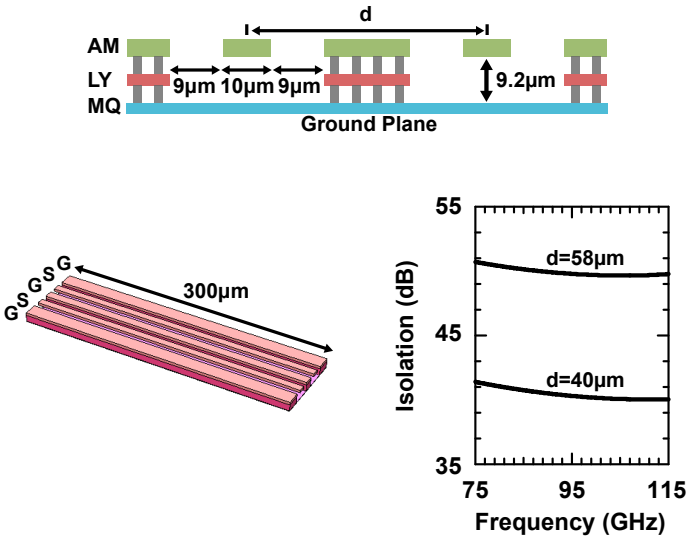

Figure 2.18: Parallel G-CPW line Sonnet layout and coupling simulations results for 40 μm and 58 μm center to center spacing.

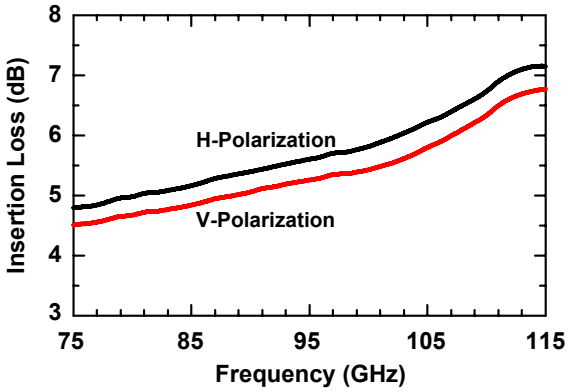

Figure 2.19: Simulated insertion loss for the V and H polarization 16:1 Wilkinson combiner/divider networks.

and distributed to the 16 T/R elements using current mirrors. A PTAT circuit is designed as the reference current source to maintain a nearly constant gain for different temperatures (up to 70 °C). M2 and M3 are used for reference current distribution. M1, MQ and AM metal layers are used together for the ground layer to decrease the ground inductance. LY and M4 metal layers are used together as VCC distribution between the elements to decrease the I×R drop. In the front-end components (LNA, Phase shifter, etc.), MIM and MOS capacitances are employed together between the supply and ground as bypass capacitances. A total of 4 nF capacitance is placed between the supply and the ground on the entire chip.

All individual channels have their own registers (D-type latch) for digital controls. A 4-bit address decoder is used to select the T/R unit element. The Rx channels have a total of 8-bit registers for 4-bit phase, 3-bit gain and 1-bit On/Off control. The Tx channels has one additional register for V/H polarization control. All channels can be switched from Rx (Tx) mode to Tx (Rx) mode using a digital level input. All channels can be turned off using a 1-bit reset input. Thus, a total of 16 bits (4-bit phase, 3-bit gain, 1-bit On/Off, 1-bit V/H, 4-bit address, 1-bit address enable and 1-bit reset and 1-bit Rx-Tx mode) parallel digital interface is required to control the 4×4 phased array. The 2 V logic circuits are designed with 0.24 μm thick-oxide CMOS transistors, and M2 and M3 are used for the digital control lines with the longest control line is ∼10 mm / 1 μm with an M1 ground layer. The total delay of the control network including interconnection lines and logic circuits is ∼2.5 ns, resulting in ∼100 MHz maximum control speed.

All RF pads except the Rx(H) common port have ESD protection using the shunt inductances of the SPDT switches. VCC supply pads are ESD protected using an RC-clamp ESD

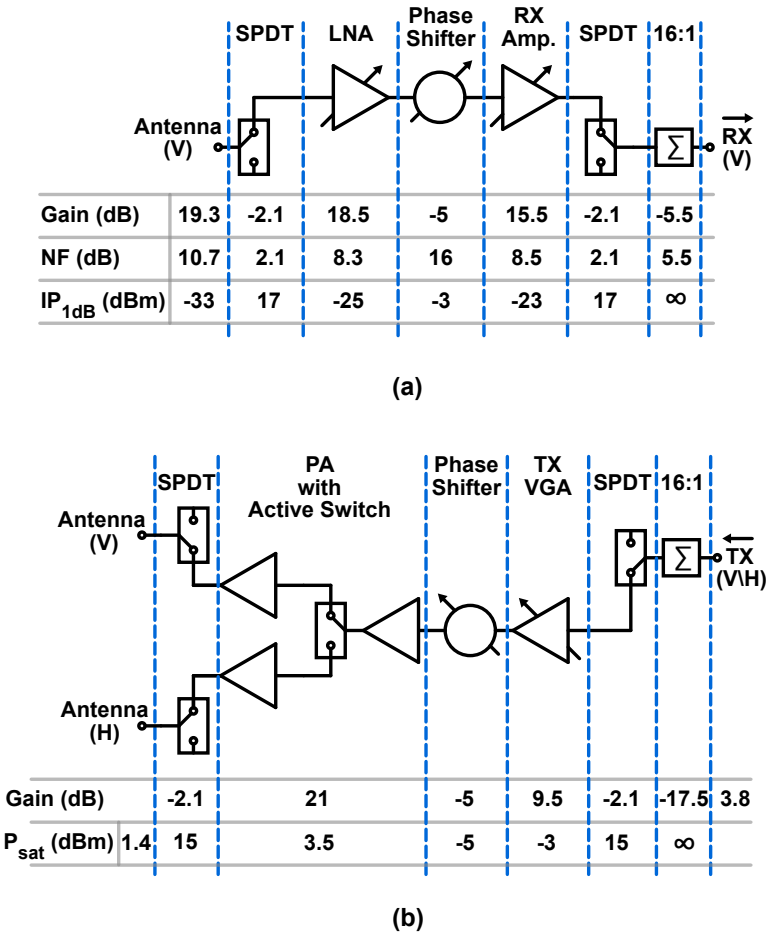

Figure 2.20: (a) Rx channel block diagram with simulated component values for gain, NF and IP_{1dB} and (b) Tx channel block diagram with simulated component values for gain and P_{sat}.

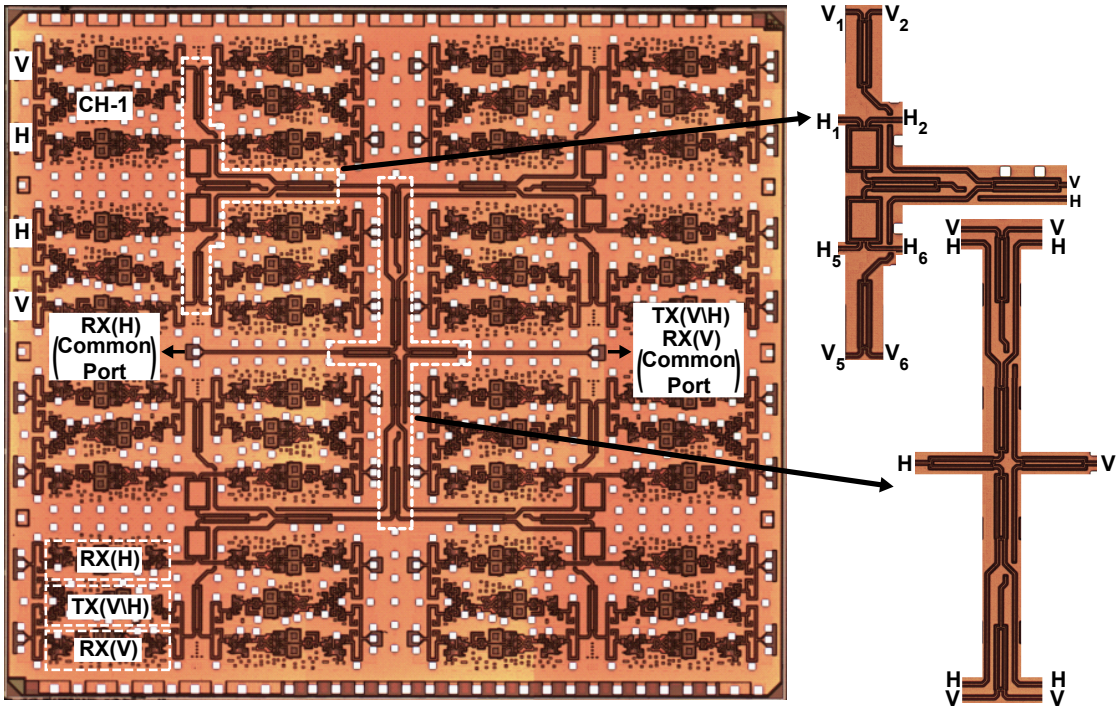

Figure 2.21: Polarimetric transmit-receive 4×4 phased-array chip microphotograph (6.6×5.9 mm^2). The chip contains 48 phased-array channels. Note the multitude of ground pads over the entire chip used to equalize the on-chip ground to the RDL system-ground.

cell and a reverse diode between VCC and ground for positive and negative polarity spikes, respectively [59]. All other I/O pads have a dual-diode to VCC and ground for ESD protection.

2.3 Measurements

2.3.1 Individual Breakouts

Chip breakouts were available for all individual components and also, for a stand-alone T/R module. All measurements are done using GSG probes and referenced to the probe tips using SOLT calibration, but the SPDT switch break-out is measured using both SOLT and TRL calibration standards. There is a significant difference in the measured (1.6 dB) and simulated (0.2 dB) thru loss at 94 GHz which is basically composed of two GSG pad (Fig. 2.22). In this measurement, S_{11} and S_{22} are $<$ -17 dB up to 100 GHz, and therefore, S_{21} is a correct indication of the thru loss. This is currently being investigated and could be due to electric fields extending into the silicon substrate since M1 was not used under the GSG signal pads. Due to brevity, the measurements on the individual components are summarized below. 1) Fig. 2.23(a) shows the LNA breakout chip microphotograph. The measured LNA gain was 17.1 dB with 4.8 dB gain control. These values are close to simulations (actually 1.3 dB higher) and the peak shifted to 100-102 GHz instead of 94 GHz, but the input and output GSG pad losses, 1.6 dB of total, was not de-embedded from the measured gain. The measured LNA NF was 8.7 dB (the GSG pad loss, 0.8 dB, was not de-embedded) and agrees with the simulated value of 8.3 dB (Fig. 2.24). 2) The measured SPDT switch S-parameters using TRL calibration show a gain of -2.0 dB at 94 GHz and result in an excellent agreement with simulations (Fig. 2.25). 3) The measured phase shifter was very close to simulations as shown in Section II. 4) Fig. 2.23(b) shows the PA breakout chip microphotograph. The measured PA with the active switch showed a gain of 15.6 dB (instead of 21 dB) at 94 GHz as shown in Fig. 2.26, with an isolation $>$ 40 dB between the (V) and (H) outputs, and a P_{sat} of 1 dBm (instead of 3.5 dBm, but the GSG pad loss, 0.8 dB, was not de-embedded from the measured value). To match the simulations with the measurements, the MOM capacitances between the stages are decreased by 12% from the simulated values (by increasing the distance between M3 and M4 metal layers), but the input and output GSG pad losses, 1.6 dB of total, was not de-embedded from the measured gain. This is still in accordance to the IBM8HP design rules for process variation ($\pm 23\%$). In the future, it is preferable to use MIM capacitors which do not suffer from such variation.

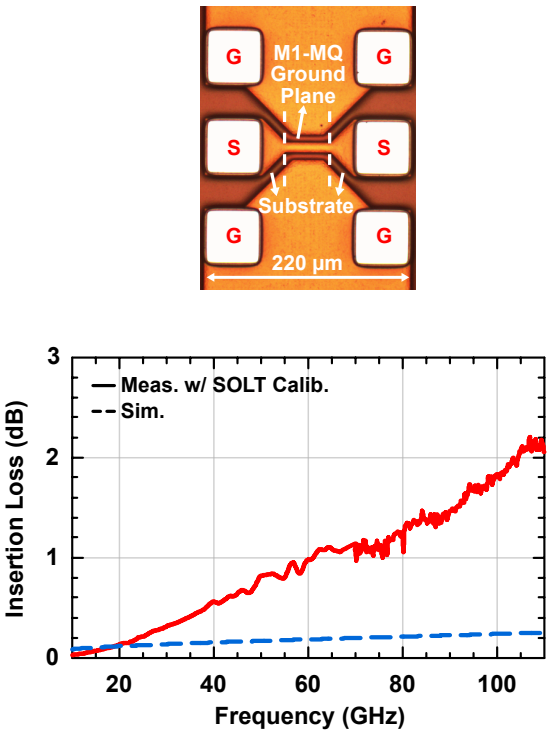

Figure 2.22: Measured and simulated THRU pad losses.

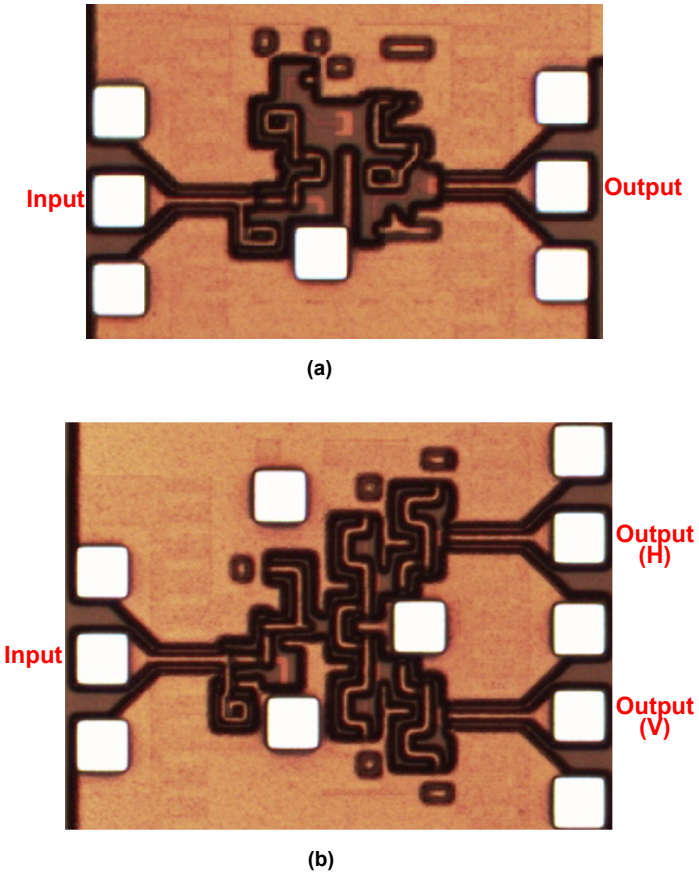

Figure 2.23: (a) LNA breakout chip microphotograph (0.58×0.45 mm^2 not including DC pads), and (b) PA breakout chip microphotograph (0.65×0.55 mm^2 not including DC pads).

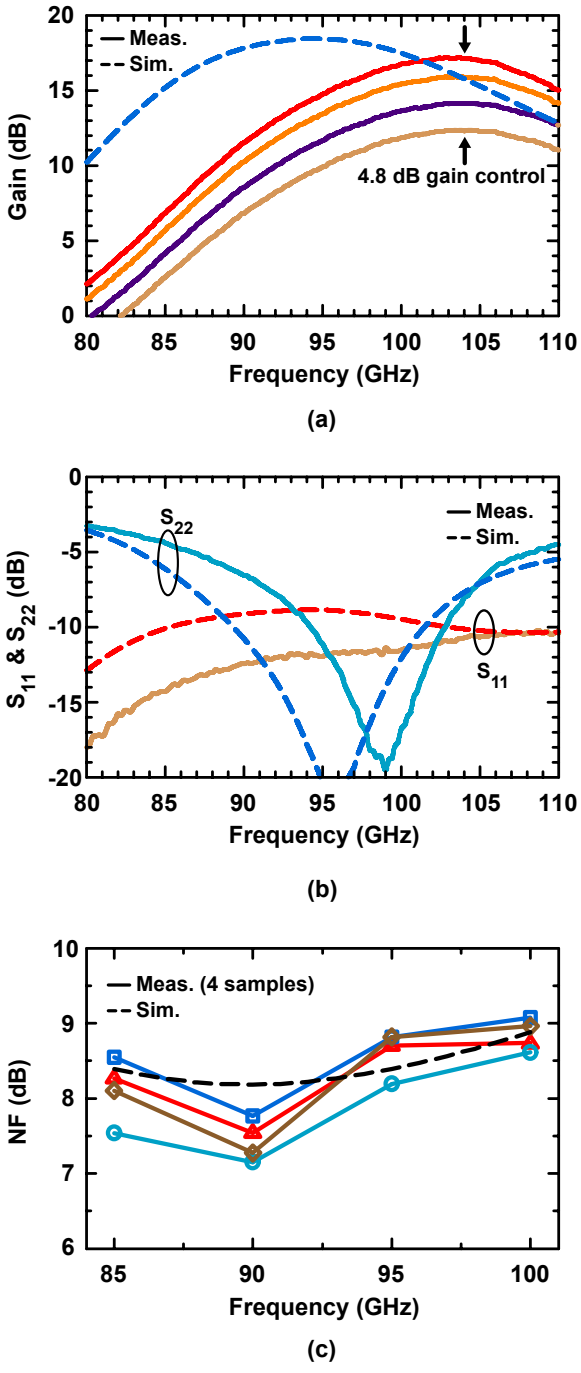

Figure 2.24: Stand-alone LNA: measured and simulated (a) gain, (b) return losses, and (c) noise figure.

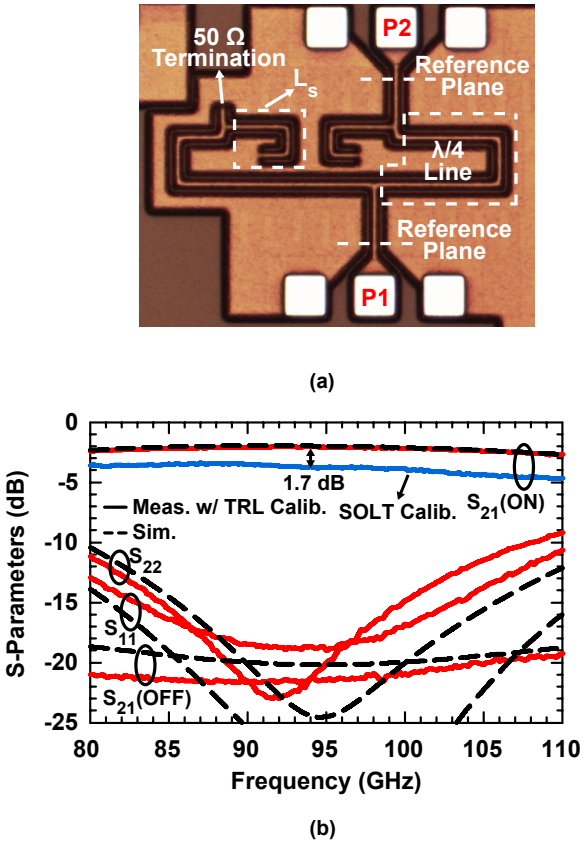

Figure 2.25: (a) Stand-alone SPDT switch chip microphotograph, and (b) measured and simulated S-parameters. S_{21} measurements are done with both SOLT and TRL calibration.

2.3.2 T/R Module Receive

The stand-alone T/R module is measured in both Rx and Tx modes (Fig. 2.27). The measured gain and phase response at maximum gain settings for the V and H polarization paths are shown in Fig. 2.28. Both paths result in a wide band impedance match with a 10 dB return loss up to 105 GHz (Fig. 2.29). Note that, for clarity, the average gain value is presented for the 16 different phase states. As presented in Fig. 2.14, there is a $\pm$1.2 dB gain variation over all phase states at 94 GHz, thereby resulting in an rms gain error of $\sim$0.8 dB. The H polarization path has 2-3 dB higher gain at 94 GHz than the V-polarization path due to the absence of an additional SPDT switch at the Wilkinson port (see Fig. 2.2). The measured phase response is very similar to the individual phase shifter results shown in Section II, with an rms phase error $< 4^\circ$ at 90-100 GHz. Note that both V and H polarization result in essentially identical phase shifter response. The measured gain control is 9 dB with a $\pm 2.5^\circ$ phase error and agrees with simulations (Fig. 2.30). The measured P_{1dB} is -31 dBm to -26 dBm at maximum and minimum gain settings and agrees well with simulations (Fig. 2.31).

The receive path noise figure was also measured without the switches (LNA, PS, RX amplifier) for 4 different samples, and resulted in 9-9.5 dB NF (the GSG pad loss, 0.8 dB, was not de-embedded) at 95 GHz which is close to the simulated value of 8.7 dB (Fig. 2.32). The noise figure increases to $\sim$11 dB at the minimum gain setting also in agreement with simulations.

2.3.3 T/R Module Transmit

The measured S-parameters of the Tx paths are shown in Fig. 2.33 for the V and H polarization paths for 16 different phase states at maximum gain setting, with a peak gain of 13 dB at 95 GHz, and are within $\pm$0.5 dB of each other (this is the calibration accuracy at W-band). Note that there is an $\sim$8.5 dB difference between the simulated and measured response and this is attributed to the increased pad loss and the reduced measured PA/active-switch gain ($\sim$4 dB gain difference). Again, the average gain over 16 phase states is presented and there is a $\pm$2 dB gain variation versus all phase settings. The measured Tx channel phase response is also very similar to the individual phase shifter (see Fig. 2.13) and of course, is identical for the V and H paths since they pass by the same phase shifter. The measured S_{11} and S_{22} show a -10 dB response up to 100 GHz (Fig. 2.34).

The measured gain control is 5.3 dB, which agrees well with simulations, over 8 steps with very low phase error since only the gain of the TX-VGA is adjusted (Fig. 2.35). This means that the TX-VGA can correct for the rms gain error in the transmit phase shifter.

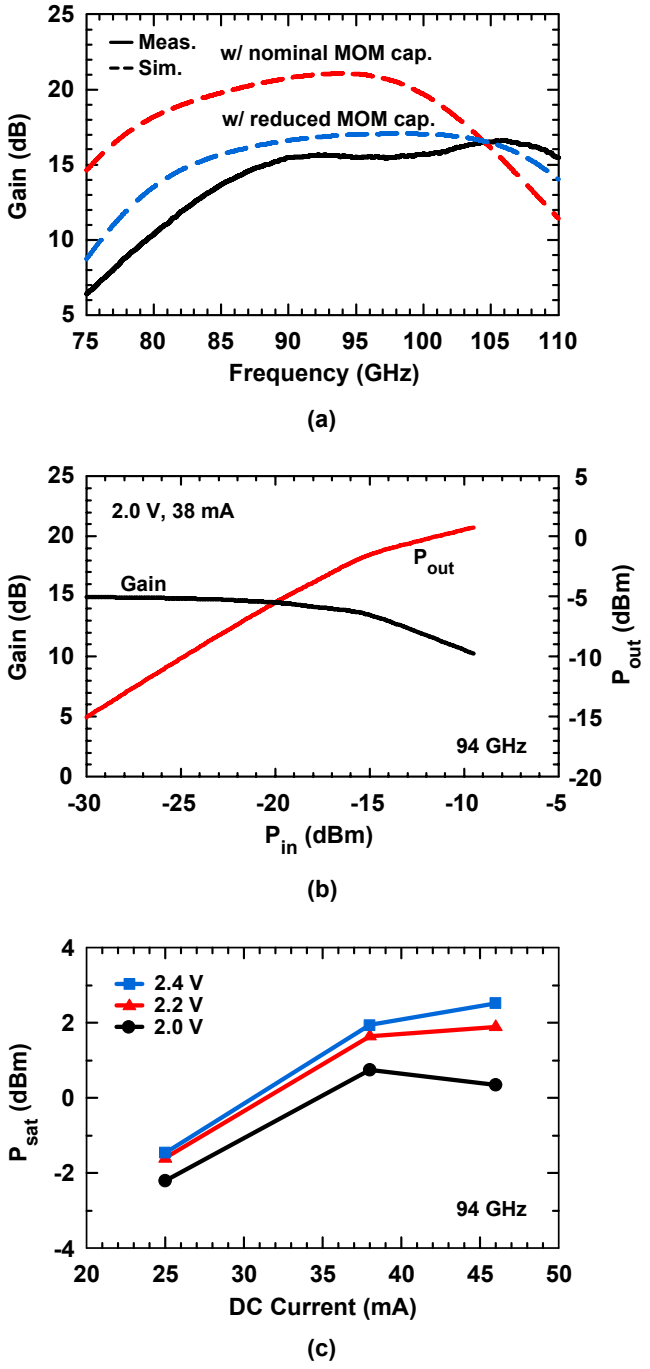

Figure 2.26: Stand-alone power amplifier: (a) measured and simulated gain, (b) measured output power and gain versus input power at 94 GHz, and (c) measured saturated output power versus DC current at 2 V, 2.2 V and 2.4 V supply voltages.

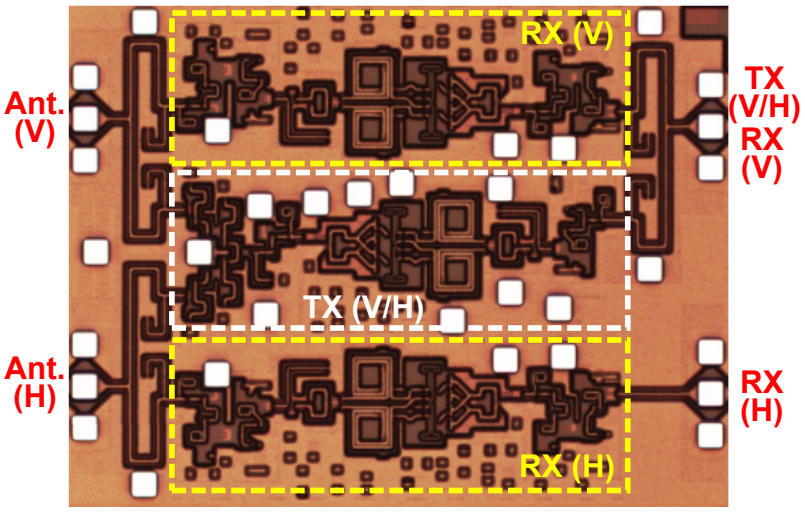

Figure 2.27: T/R unit (single element) chip microphotograph (1.6×1.2 mm^2 not including DC pads).

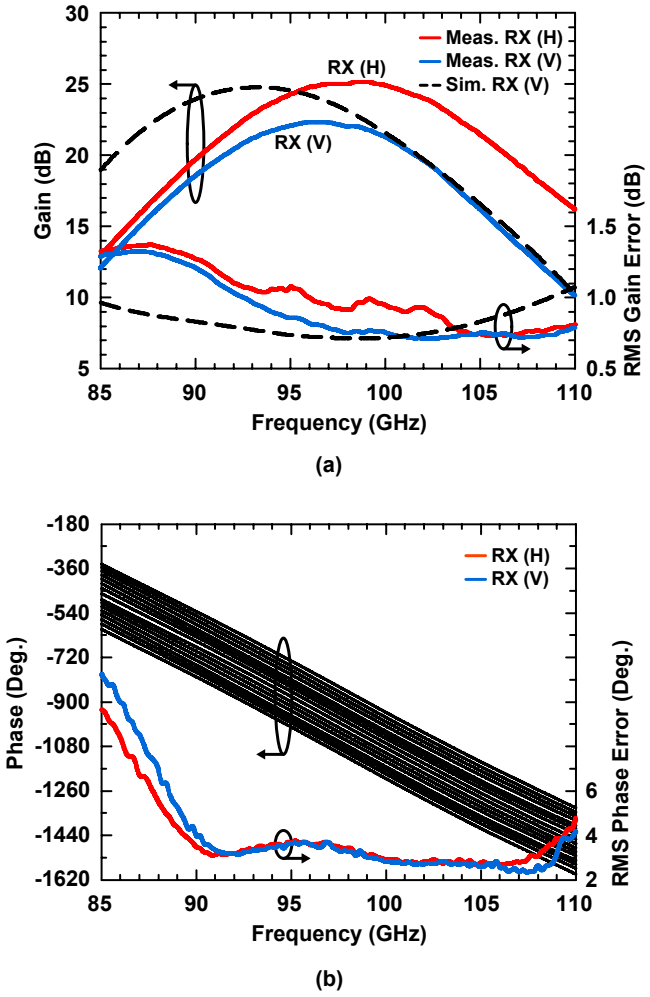

Figure 2.28: Measured average gain and phase of both Rx channels on a T/R unit over 16 phase states at maximum gain state.

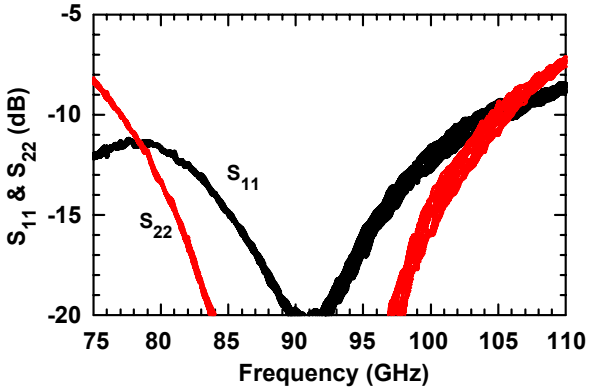

Figure 2.29: Measured input and output return losses of Rx(V) channel on a T/R unit over 16 phase states.

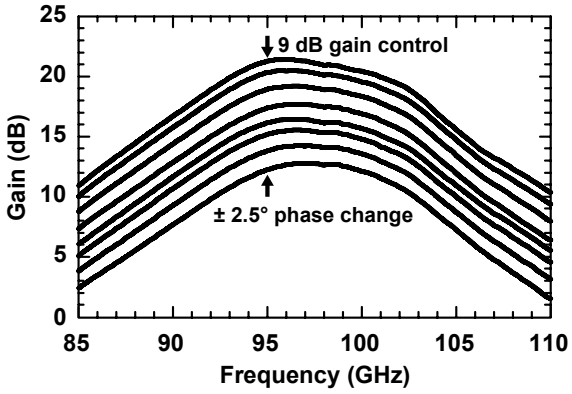

Figure 2.30: Measured gain of Rx(V) channel on a T/R unit over 8 gain states at 0° phase state.

The measured output P_{sat} is -5$\pm$0.5 dBm for the transmit element versus different phase states for both V and H paths (Fig. 2.36). This is lower than simulations due to the reduced power amplifier P_{sat} and the increased loss of the GSG pad (0.8 dB).

2.3.4 Isolation in the T/R Module

Fig. 2.37 presents the measured isolation between the V and H polarization ports in the transmit path since the active switch in the PA selects one output (V or H) at a time. In this measurement, the active switch is activated for the V channel, and both input and output SPDT switches are set for the Tx path (Rx channels are turned off). A wideband isolation of $>$ 40 dB is achieved in the active switch, with a peak of 46 dB at 95 GHz, which is very close to simulations.

The isolation between the dual-receive beam chains was measured on-chip using GSG probes and by energizing one receive port (V or H) and measuring the power at the two output ports (V and H) as shown in Fig. 2.38. In this measurement, the Tx chain is turned off. The finite isolation is due to the single-ended design and the residual ground and VCC inductance which is of the order of few pH [60]. Measurements indicate an isolation of $\sim$30 dB at the output ports when the input is on the V port, and an isolation of $\sim$40 dB when the input is on the H port. The $\sim$10 dB difference is understandable because for the first case, the main signal on the V-channel is attenuated by the SPDT switch ($\sim$2 dB loss), while in the latter case, the coupled signal on the V-channel is attenuated by the SPDT switch. The measurements indicate that the inherent power-supply/ground coupling between the two receive chains in a T/R module from the output of one receive chain to the input of the other chain is $\sim$-60 dB knowing that each receive chain has a gain of 22 dB (V) and 25 dB (H).

2.3.5 4$\times$4 Phased Array

The 4$\times$4 phased array chip was mounted on a control board, and the bias and control pins bonded to individual lines with decoupling capacitors for the DC supply lines (see Fig. 2.39). The chip was biased at 2 V and consumed 1100 mA in the Tx and Rx modes, which is $\sim$150 mA higher than the simulations and could be due to an increase in the temperature of the PTAT reference circuit at the center of the chip, or to process variations in the reference resistors. The RF measurements were done using GSG probes and referenced to the probe tips. Due to the position of a GSG probe on the common V and H polarization ports at the left and right center of the 4$\times$4 chip (see Fig. 2.21), only 8 channels could be tested with the other GSG probe.

The measured individual channels (from the antenna port to the common port) showed

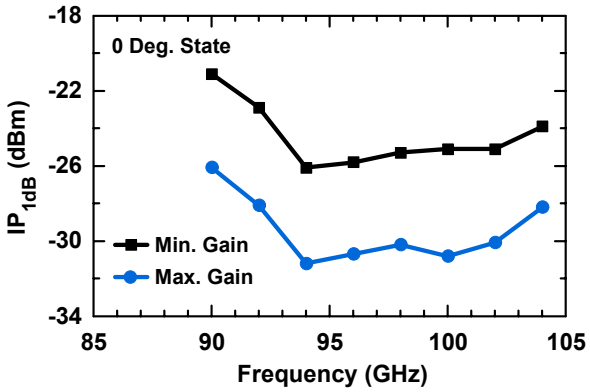

Figure 2.31: Measured Rx channel IP1dB versus frequency at minimum and maximum gain settings and 0° phase state.

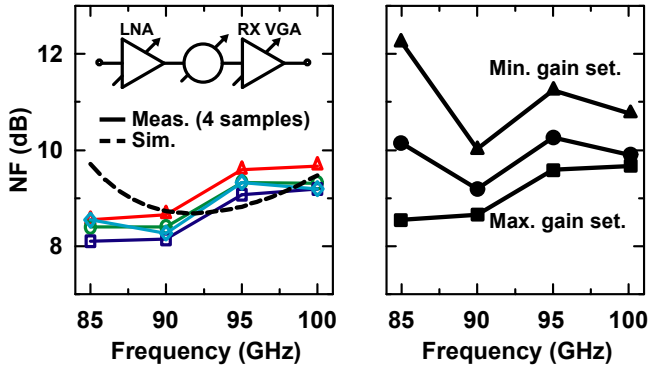

Figure 2.32: Measured Rx channel NF (LNA, phase shifter and RX amplifier).

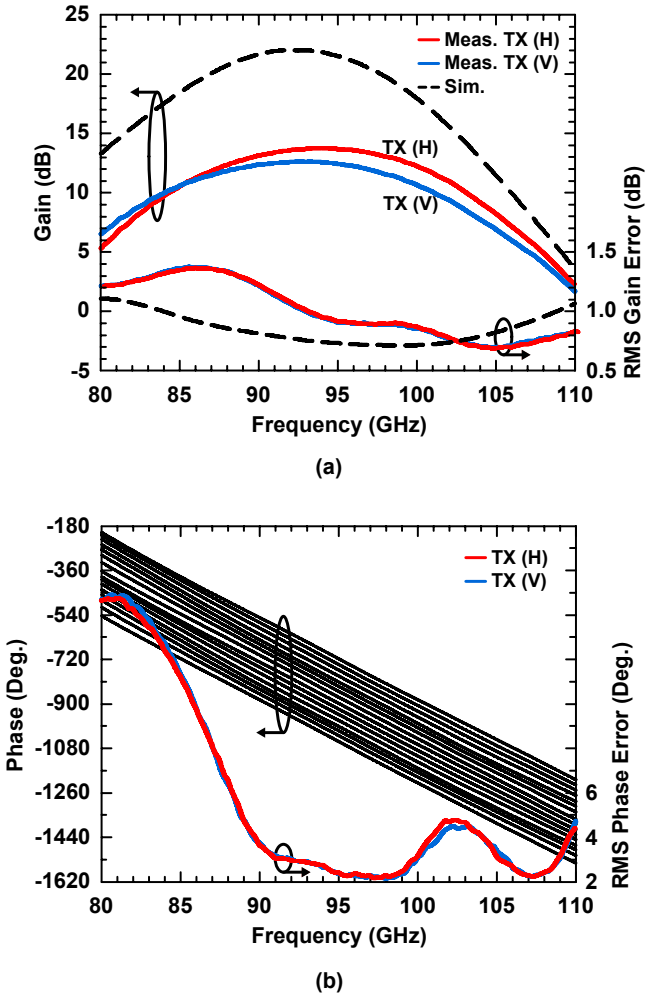

Figure 2.33: Measured average gain and phase of Tx(V) and Tx(H) channel on a T/R unit over 16 phase states at maximum gain state.

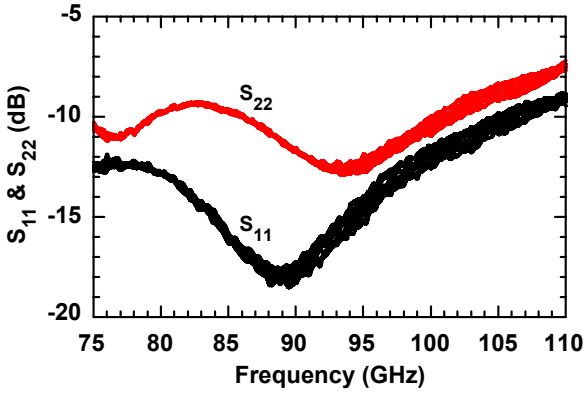

Figure 2.34: Measured input and output return losses of Tx(V) channel on a T/R unit over 16 phase states at maximum gain state.

the same phase and gain response versus the 16 phase states as presented before and, therefore, are not shown. Fig. 2.40 presents the measured average gain for 8 different channels in the Rx(V) and Rx(H) paths, and with only a $\pm$0.75 dB peak-to-peak difference between all 8 channels. The measured average gain includes the 16:1 Wilkinson ohmic loss and is 5-6 dB lower than the channel gain measured on the T/R module breakout, showing excellent agreement with Wilkinson loss simulations.

The measured Tx(V) from the common port to an antenna port results in $\pm$1.25 dB gain difference over all 8 channels, which is still good knowing that there is more variation because of increasing temperature than in the LNA due to the high current density of the PA transistors (Fig. 2.41). In this case, the 16:1 Wilkinson power division loss is added to the ohmic loss resulting in 17.5 dB overall distribution loss. The measured output P_{sat} for the 45° state for 8 channels is -5.1$\pm$0.5 dBm (the GSG pad loss, 0.8 dB, was not de-embedded) which is achieved for an input power of 6 dBm at the common port (Fig. 2.42). This measured saturated power is lower than simulations but similar to the single T/R module measurements. Overall, the 4$\times$4 phased array with the Wilkinson combiners functioned as expected with very low amplitude error between the elements.

2.3.6 Coupling in the 4$\times$4 Phased Array

Since this is a pulsed-based radar phased array, the coupling between the Tx and Rx paths is not applicable since only one path is turned on at a time. However, in the Rx or Tx mode, one can have un-wanted coupling between the different T/R elements, or between two receive channels in the same channel.

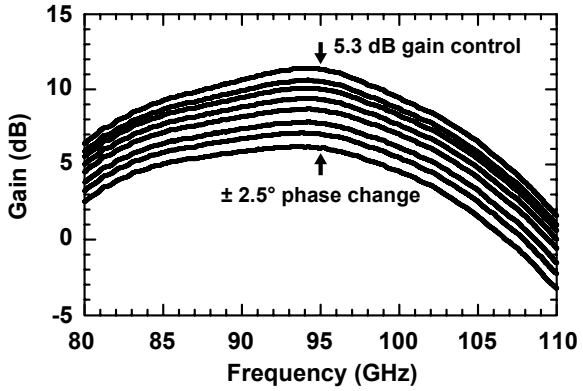

Figure 2.35: Measured gain of Tx(V) channel on a T/R unit over 8 gain states at 0° phase state.

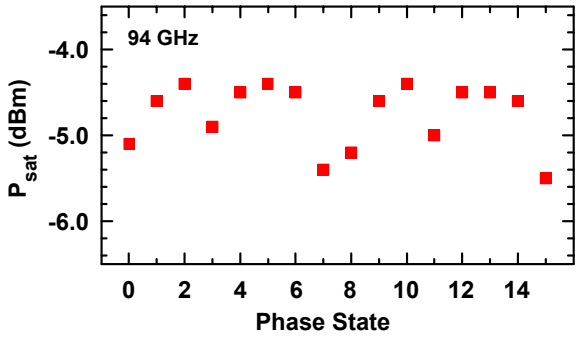

Figure 2.36: Measured Tx channel saturated output power on a T/R unit over 16 phase states at 94 GHz.

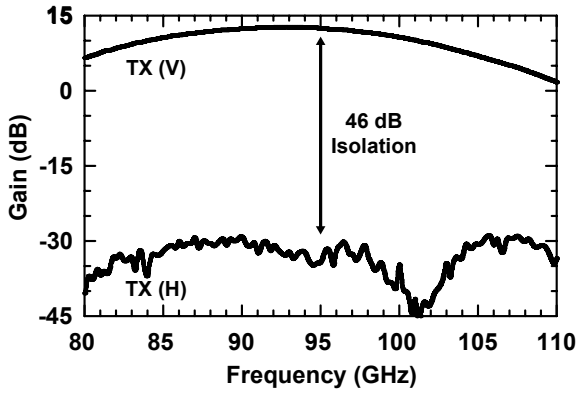

Figure 2.37: Measured isolation of Tx(V) and Tx(H) channels on a T/R unit at maximum gain state.

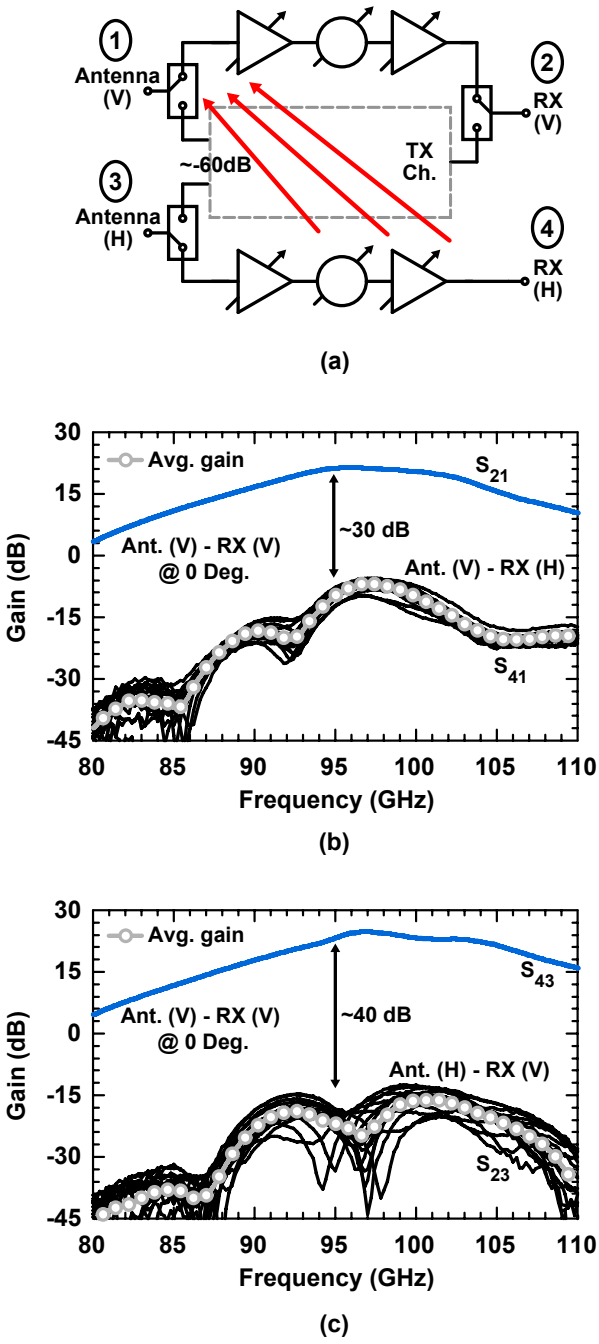

Figure 2.38: (a) Block diagram of Rx channel isolation setup: Measured isolation of (b) Rx(V)-Rx(H) (Rx(H) phase is toggled) and (c) Rx(H)-Rx(V) (Rx(V) phase is toggled) on a T/R unit. The isolation does not vary over the 16 phase states.

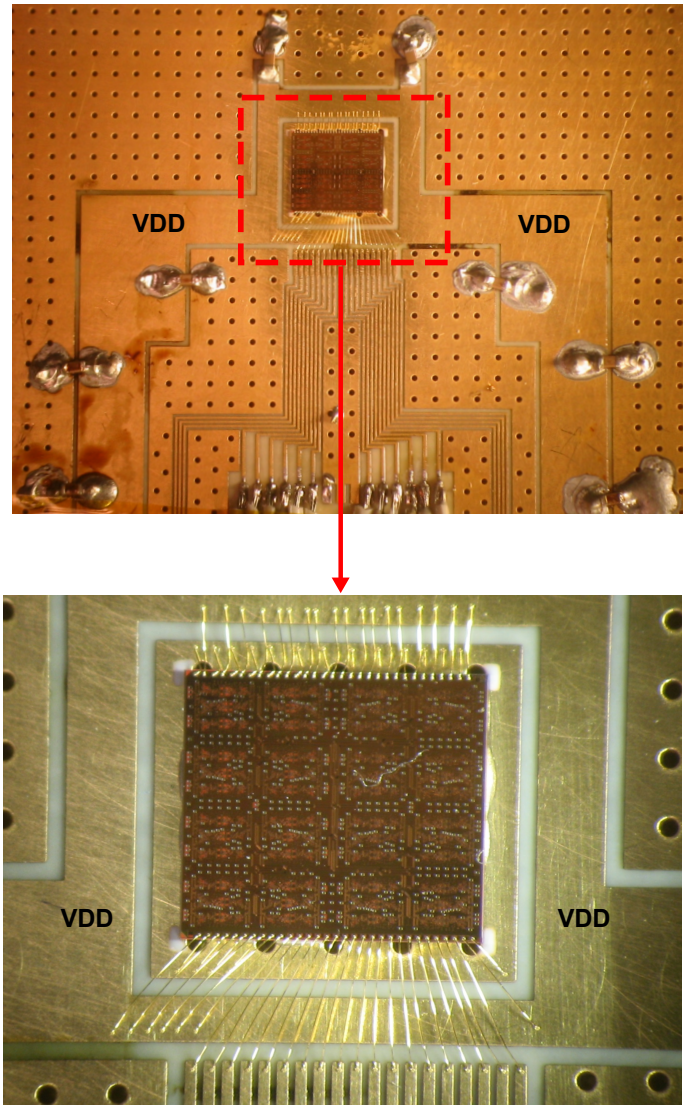

Figure 2.39: Bonded a 4×4 array chip on a dc biasing board.

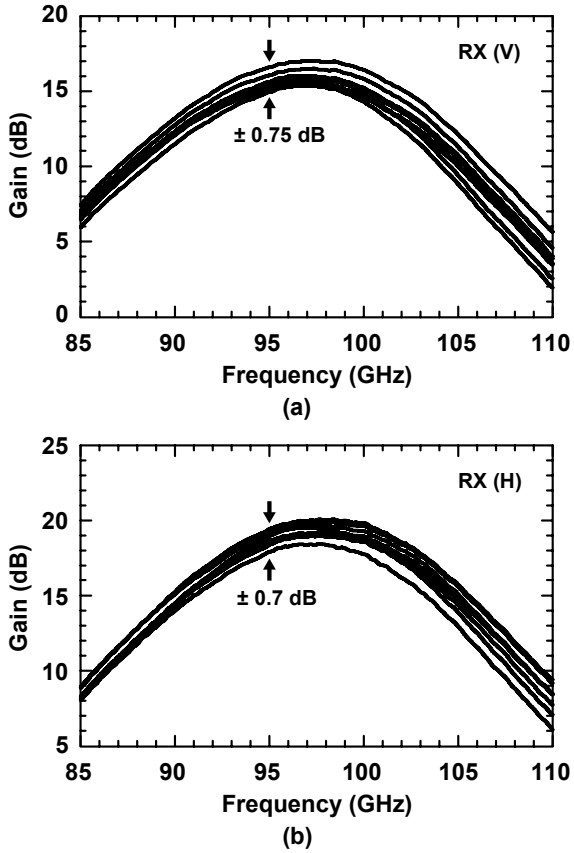

Figure 2.40: Measured average gain of (a) Rx(V) and (b) Rx(H) channels on 4×4 array for 8 channels at maximum gain settings. The measurement includes 5-6 dB ohmic loss of 16:1 Wilkinson power combiner. (Measured channel numbers for Rx(V) are 1, 5, 6, 7, 9, 10, 11 and 13, and measured channel numbers for Rx(H) are 4, 6, 7, 8, 10, 11, 12 and 16.).

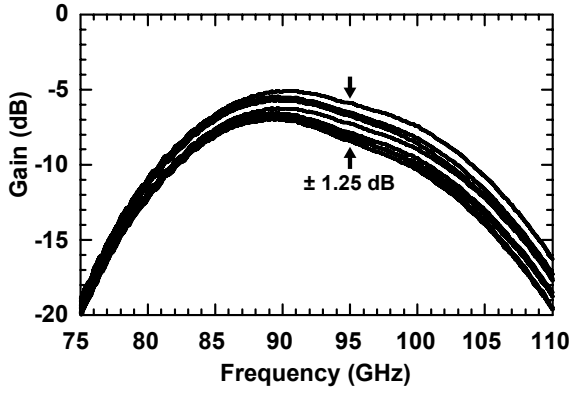

Figure 2.41: Measured average gain of Tx(V) channel on 4×4 array for 8 channels at maximum gain settings. The measurement includes 5-6 dB ohmic and 12 dB division loss of 16:1 Wilkinson power divider. (Measured channel numbers are 1, 5, 6, 7, 9, 10, 11 and 13).

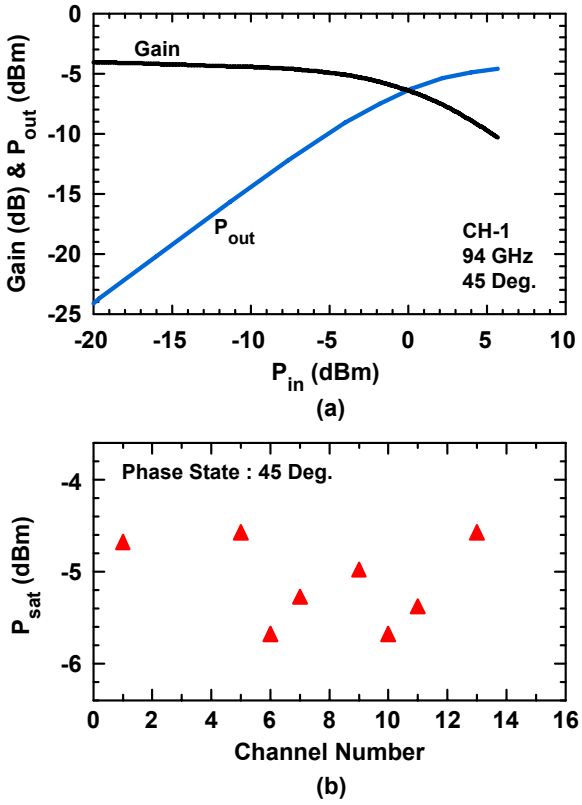

Figure 2.42: Measured (a) gain and output power versus input power for channel-1 and (b) saturated output power of Tx(V) channel on 4×4 array for 8 channels at 45° phase state at 94 GHz. (Measured channel numbers are 1, 5, 6, 7, 9, 10, 11 and 13)

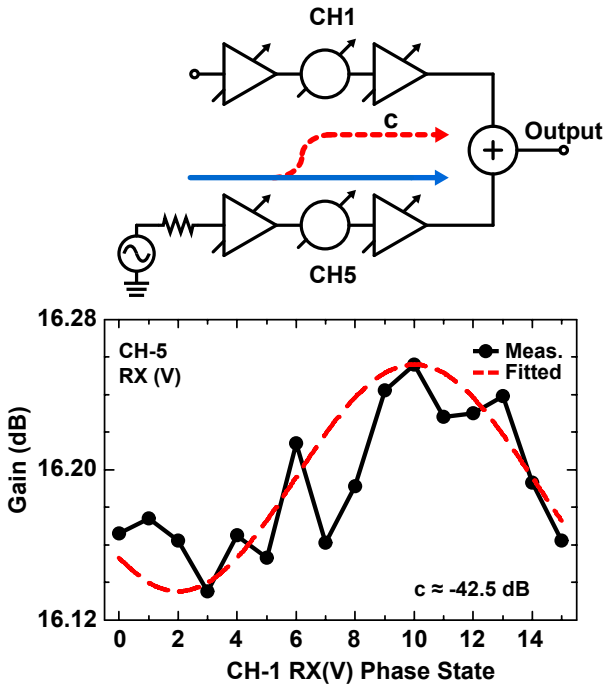

Figure 2.43: Measured Rx channel coupling at 94 GHz. Rx(V) on CH-5 is measured while phase state of Rx(V) on CH-1 is changed.

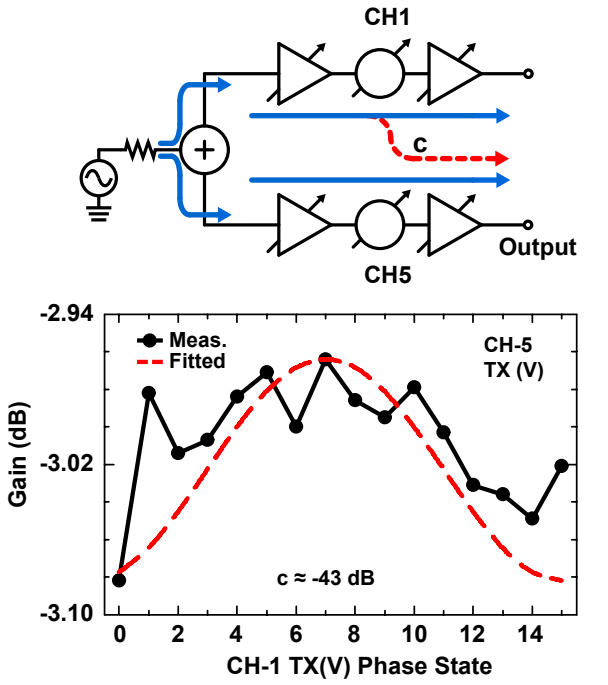

Figure 2.44: Measured Tx channel coupling at 94 GHz. Tx(V) on CH-5 is measured while phase state of Tx(V) on CH-1 is changed.

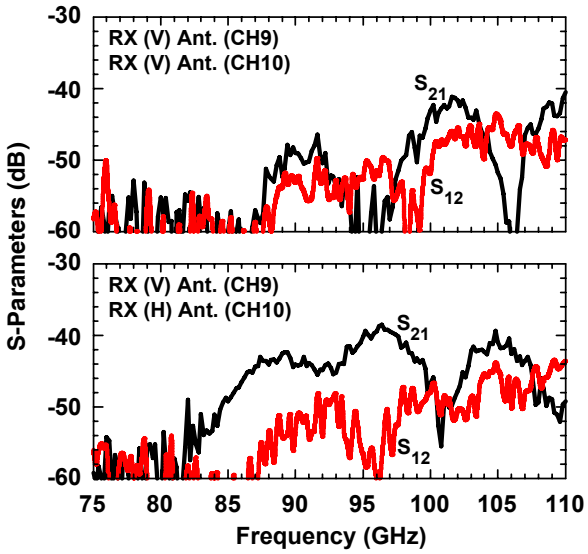

Figure 2.45: Rx channel antenna port to Rx channel antenna port coupling.

The coupling between two different elements in the 4×4 phased array was done by measuring the S_{21} of a specific channel (for ex: Channel 5) and changing the phase of another channel (for ex: Channel 1) [8, 11]. Any coupling to Channel 1 results in a small error vector which adds to Channel 5, thus creating amplitude and phase modulation in Channel 5 response as the phase of Channel 1 is varied. Fig. 2.43 and Fig. 2.44 show the measured and fitted coupling from Channel-1 to Channel-5 on the Rx and Tx modes, respectively. Several channel combinations were done and all resulted in a coupling of ∼-42 dB between the channels, which is insignificant compared to antenna-to-antenna coupling in a phased array (-25 dB).

A final coupling test is done on the receive ports of different T/R channels. In this case, the V or H receive port is energized on a specific channel and the power is measured on the receive ports of a different channel. While this is not forward coupling as shown in Figures 2.43 and 2.44, it still gives an idea of the channel-to-channel coupling due to power supply and ground inductance. In a sense, this is congruent to the V and H coupling measurements done on a single channel (see Fig. 2.38) but on a 4×4 array level. A coupling of $<$ -40 dB is seen between channels as shown in Fig. 2.45.

2.3.7 Isolation in the 4×4 Phased Array

All isolation measurements are done on-chip using GSG probes and with all other ports left open-circuited.

Fig. 2.46 presents the measurement isolation between the V and H receive chains with one channel energized (V or H) and the output measured at both the V and H common ports. Measurements on Channels 6,8,11 and Channels 5,7,10 are shown depending on probe alignments. It is seen that all result in an isolation $>$ 30 dB and this is due to the inherent coupling in the single T/R module (see Fig. 2.38 in Section III-D) and to residual coupling in the Wilkinson networks. Note that all ports are left open circuited except the energized ports, and therefore, there is additional standing waves in the Wilkinson combiners which degrades the isolation.

Another test of isolation is to place the GSG probes on the common V and H ports and do a full S-parameter measurement (Fig. 2.47). That is, the common V (or H) port is energized and the leakage signal at the common H (or V) port is measured. It is seen that $>$ 40 dB isolation is achieved if the 4$\times$4 T/R modules are turned off (ie, nested Wilkinson combiners with 4$\times$4 loading impedances of 55-j15 Ω and 40+j18 Ω at 94 GHz for V and H polarization, respectively), and $>$ 35 dB when the T/R 4$\times$4 are biased. This is very good for a single-ended design at W-band.

2.4 Conclusion

This paper presented a W-band 4$\times$4 transmit-receive phased array chip with full polarimetric capabilities and the measured performance is summarized in Table 2.2. Extensive measurements on a single T/R channel and on the 4$\times$4 phased array show very low coupling between the channels and between the simultaneous V and H receive channels. Future work includes a redesign of the GSG pad and the power amplifier chain for improved performance. The phased array consumes 2.2 W in the Tx and dual-Rx modes and the design is scalable for $>$ 10,000 elements using polyimide redistribution layers (RDL) on top of the chip.

2.5 Acknowledgement

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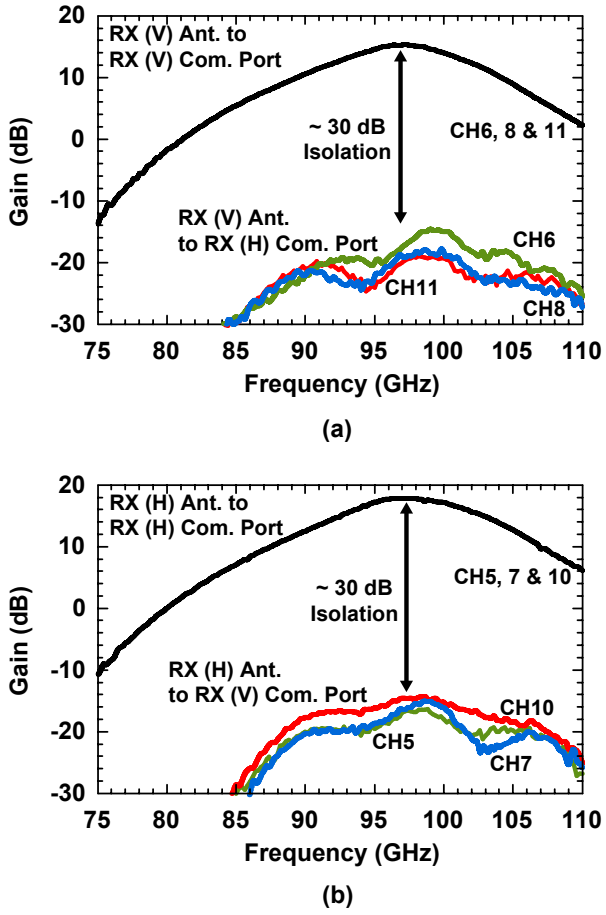


Figure 2.46: Rx channel antenna ports to Rx channel common ports isolation.

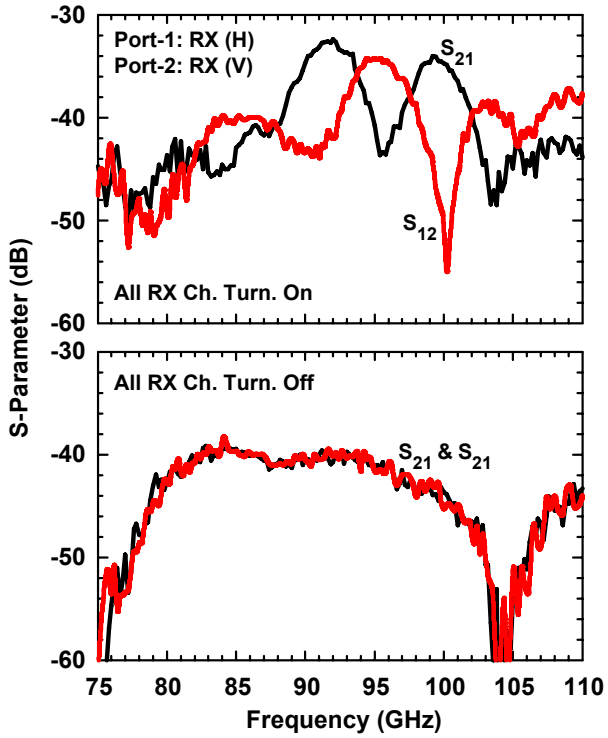


Figure 2.47: Rx(H) common port to Rx(V) common port isolation.

Table 2.2: Performance Summary of 4×4 Transmit-Receive Phased Array

	Receive Mode	**Transmit Mode**
Frequency (GHz)	90-102	84-102
Number of Elements	32 (16 channels V & H)	16
T/R Channel Gain (dB) [a]	22 (V polarization) 25 (H polarization)	13
Array Gain (dB)	17[b] (V polarization) 20[b] (H polarization)	-6[c]
Number of Phase Bits	4	4
Number of Gain Bits	3	3
RMS Phase Error	$< 4°$ @ 90-110 GHz	$< 5°$ @ 90-110 GHz
RMS Gain Error	$<$ 1.2 dB @ 90-110 GHz	$<$ 1.2 dB @ 90-110 GHz
Channel NF (dB)[d]	8.5-9.5 (max. gain) 10-11 (min. gain) @ 90-100 GHz	N/A
System NF (dB)[e]	10.5-11 @ 90-100 GHz	N/A
Input P_{1dB} (dBm)	-31 (max. gain) -26 (min. gain)	-
Output P_{sat} (dBm)	-	-5
Gain Control (dB)	9 (1.3 dB steps)	5.3 (0.8 dB steps)
Power Consumption (W)	2.2 (@ 2 V)	2.2 (@ 2 V)

[a] w/ SPDT switches.

[b] w/ Wilkinson ohmic loss.

[c] w/ 16:1 Wilkinson division and ohmic loss.

[d] w/o SPDT switch.

[e] simulated.

Chapter 3

A 0.39-0.44 THz 2×4 Amplifier-Quadrupler Array with Peak EIRP of 3-4 dBm

3.1 Introduction

Silicon THz systems are an active area of research for passive and active imaging applications, and communication and sensor systems [23–38]. Most of the work in THz is done in the 100-300 GHz range, but some researchers have pushed imaging systems, receivers and transmitters at $>$ 300 GHz with varied results [24–30]. The main issue of $>$ 300 GHz silicon THz systems is that the operating frequency is higher (or very close) to the transistor f_T and f_{max}, which precludes the use of amplifiers at these frequencies. And therefore, most $>$ 300 GHz systems are based on direct detectors (imaging), mixers (receivers), or multipliers (transmitters) [24, 27, 30].

Silicon THz systems also use integrated on-chip antennas so as to eliminate the transitions in and out of the silicon chip. This idea has been borrowed from THz bolometer and GaAs Schottky-diode receiver/multiplier implementations in the 1980s and 1990s, and greatly simplifies the system especially for large arrays. Furthermore, the silicon chip can be placed on a hyper-hemispherical or extended dielectric lens for improved efficiency and greatly increased antenna gain [26, 27, 37, 61]. However, silicon lenses are expensive and it is preferable to design antennas which radiate efficiently from the top surface of the silicon chip (without the use of a silicon lens). At $>$ 300 GHz, it is possible to design efficient microstrip antennas [25, 62] and

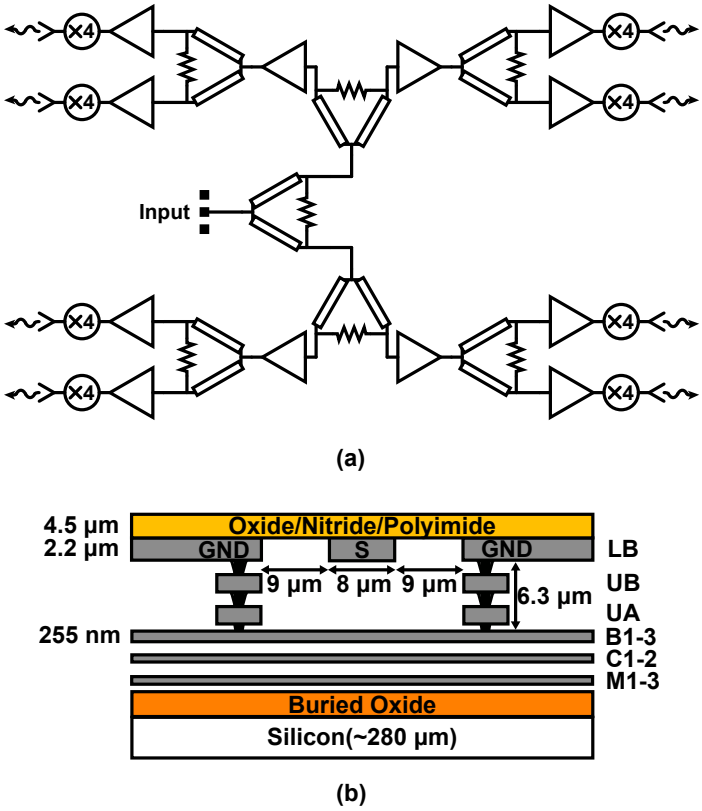


Figure 3.1: (a) Block diagram of the 2×4 amplifier-quadrupler array, and (b) 45-nm SOI CMOS process metal stack-up and 50-Ω G-CPW transmission-line cross section.

slot-ring antennas with a dielectric superstrate [24, 63] using a standard silicon backend containing a top metal and 5-8 μm of dielectric layers.

This paper presents the first amplifier-multiplier array capable of generating an EIRP $>$ 3 dBm at 420 GHz without the use of a dielectric lens (Fig. 3.1(a)). The idea is to distribute the RF signal at W-band frequencies where the transmission-line is relatively low loss (1-1.2 dB/mm) and amplifiers are available for signal amplification. The signal is converted to 370-440 GHz using a quadrupler just before the planar antenna for reduced transmission-line loss at 400 GHz [64]. Furthermore, the W-band RF signal can be locked to a 100 MHz reference using dividers [65]. Also, multipliers result in much wider band performance than oscillators which is important for spectroscopy and active imaging arrays. The amplifier-multiplier concept is proven on a 2$\times$4 array with state of the art results, but can be also scaled to any N$\times$M array using additional W-band splitters and amplifiers.

3.2 Design

The chip is implemented in IBM 45-nm SOI process (IBM12SOI) with 220-230 GHz f_{max} referenced to the top metal layer [41]. The cross section of this process is shown in Fig. 3.1(b). Grounded coplanar waveguide (G-CPW) transmission lines with 9/8/9 μm (Z_0 = 50 Ω) are implemented using LB for the signal line and B3 for the ground plane. The simulated G-CPW line loss is 1 dB/mm and 1.2 dB/mm at 90-100 GHz resulting in a Q of 15 and 16 for 50 Ω and 70 Ω lines, respectively. IBM CMOS transistor models are used in all linear and non-linear simulations.

3.2.1 Quadrupler

The schematic of the quadrupler is shown in Fig. 3.2. It is a balanced design with an input balun which converts the single-ended input to differential signal for the transistor pair. Electromagnetic simulation (Sonnet 2.5-D EM solver) and RC extraction are used together to model the transistor interconnection to the top metal layer. The transmission lines, input balun and interconnects are also modeled using Sonnet. A 48° shunt transmission line, a 25 fF series capacitor, a balun with a 10 fF shunt capacitor at the balun output and a 30° differential G-CPW line are used to match the multiplier input impedance to 50 Ω. The input balun has 2.5° and 0.2 dB phase and amplitude imbalance at 95 GHz, respectively (Fig. 3.3).

In order to select the transistor size, the input and output matching networks are opti-

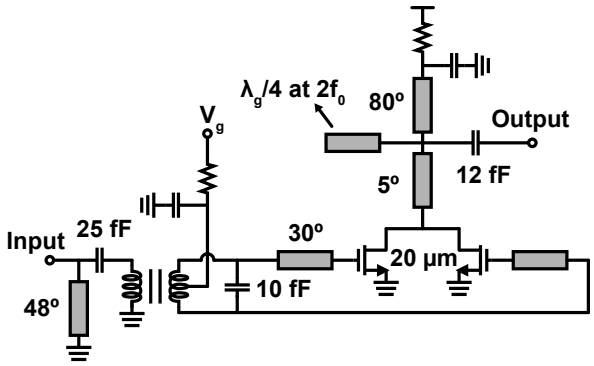


Figure 3.2: Quadrupler schematic with second harmonic reflector at the output.

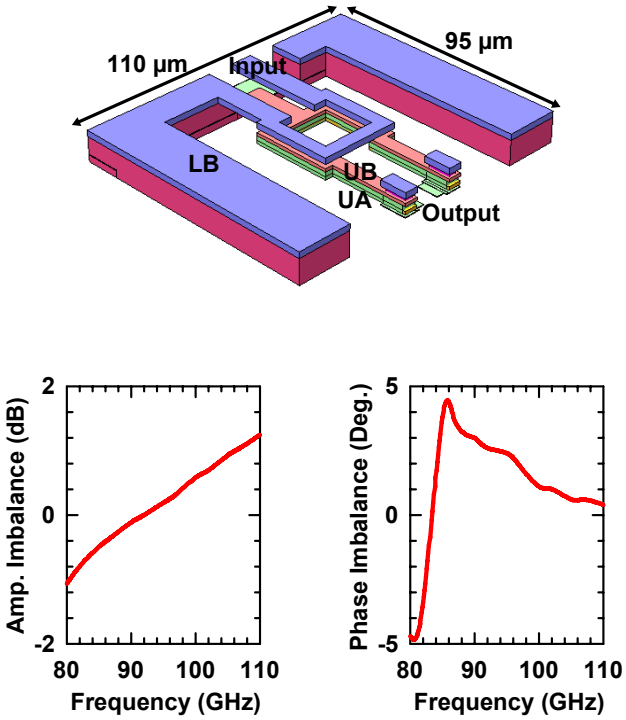


Figure 3.3: Input balun Sonnet layout, and simulated amplitude and phase imbalance.

mized individually for three different transistor sizes: 50×0.5 μm, 40×0.5 μm and 30×0.5 μm (Fig. 3.4(a)). The 40×0.5 μm transistor shows the best output power and conversion loss for an input power of 5-10 dBm which can be achieved from a W-band amplifier in this process [41]. The desired output 4^{th} harmonic level should also be maximized by setting the conduction angle correctly using the gate bias, and this is achieved using a conduction angle of 60°-70° [66]. Fig. 3.4(b) presents the input power versus gate bias voltage for an output power level of -12 dBm to -6 dBm. The required input power and the gate bias voltage both decrease at the saturated output power level. Thus, the gate bias should be set to 0 V to improve the conversion loss.

The balanced transistor drain currents are out-of-phase and in-phase for the odd and even harmonics of the input signal, respectively. Thus, the even harmonics are combined in phase at the drain node of the balanced transistor pair while the fundamental and odd harmonics are canceled due to a broadband virtual ground. A λ_g/4 open-stub at 2×f_0 is used to suppress the 2^{nd} harmonic of the input signal. Simulated output harmonic levels versus input power at 95 GHz with and without λ_g/4 stub are shown in Fig. 3.5. The λ_g/4 stub suppresses the 2^{nd} harmonic by 17 dB for an input power level of 10 dBm at 95 GHz. The finite suppression of the fundamental and the 3^{rd} harmonic are due to the phase and amplitude imbalance of the input balun, but, still, they are much lower than the desired 4^{th} harmonic level.

3.2.2 Slot-Ring Antenna

The 375 GHz elliptical slot-ring antenna is single-ended and placed on the top metal layer (LB) with the ground plane defined as B3 (Fig. 4.3). This creates a parallel-plate condition which can greatly reduce the antenna efficiency. Therefore, an un-patterned quartz superstrate is used to equalize the TEM mode in the dielectric underneath LB and the TM_0 mode in the quartz superstrate [24, 63, 67]. This results in a high-efficiency antenna since the two radiating slots in the elliptical slot-ring antenna are placed at λ_{TM0}/2 = λ_{TEM}/2 apart, and therefore cancel any spurious radiation in the X-Y plane. The slot-ring antenna, without meeting any metal-density rules, results in a radiation efficiency of 57% and a gain of 4.3 dB at 375 GHz using a quartz superstrate (Case 2) (Fig. 3.7). In this work, the antennas are designed to meet the most stringent metal-density rules even if this results in a detrimental effect on the antenna performance due to increased capacitance effects and added loss. This is done so that no metal exclusion is taken on the wafer, which is congruent with a full mask containing thousands of transmitter array chips. In this process, the metal density rules are 23% for LB to B3 and this reduces the gain and radiation efficiency to 1.6 dB and 35%, respectively (Case 1). Note that the slot-ring antenna without a

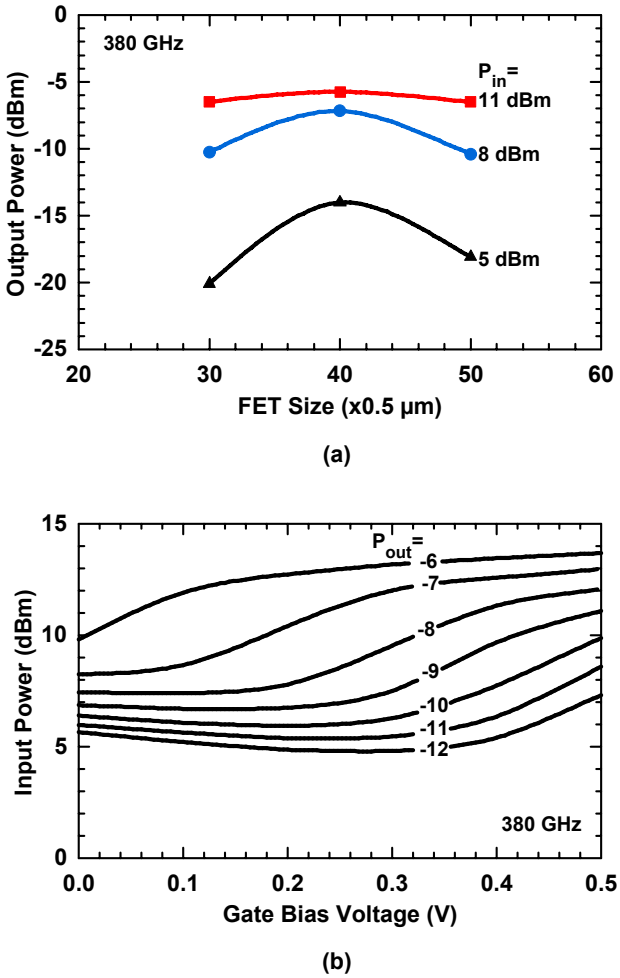


Figure 3.4: (a) Simulated output power at 380 GHz versus transistor size at 5, 8 and 11 dBm input power and (b) simulated input power versus gate voltage for an output power range of -6 dBm to -12 dBm at 380 GHz (transistor size is $40\times0.5\mu$m).

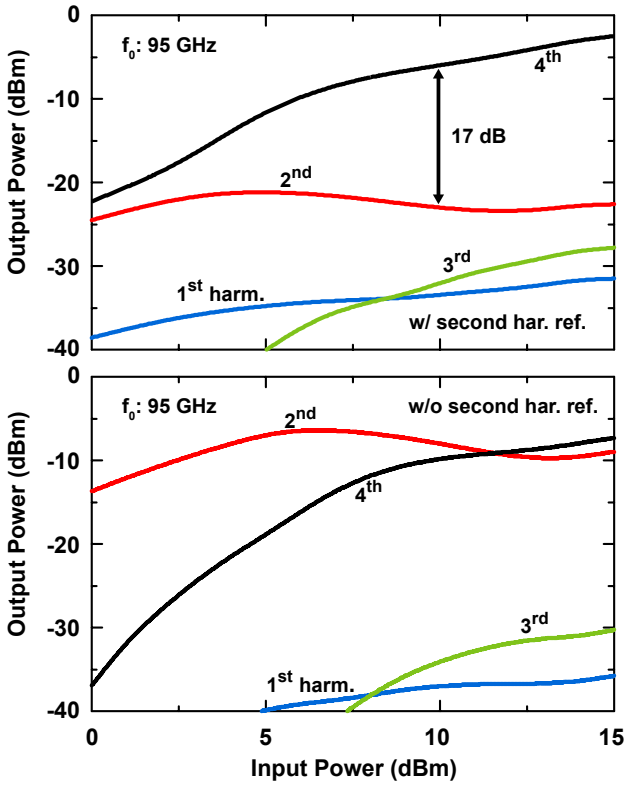


Figure 3.5: Simulated harmonic levels of quadrupler with and without a second harmonic reflector versus input power at 95 GHz.

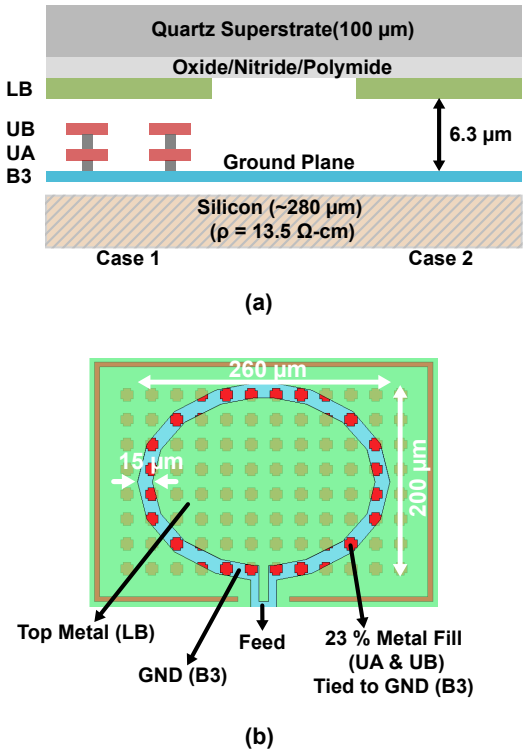


Figure 3.6: (a) Metal fill cases and (b) on-chip single-ended elliptical slot ring antenna with metal-fill underneath the antenna.

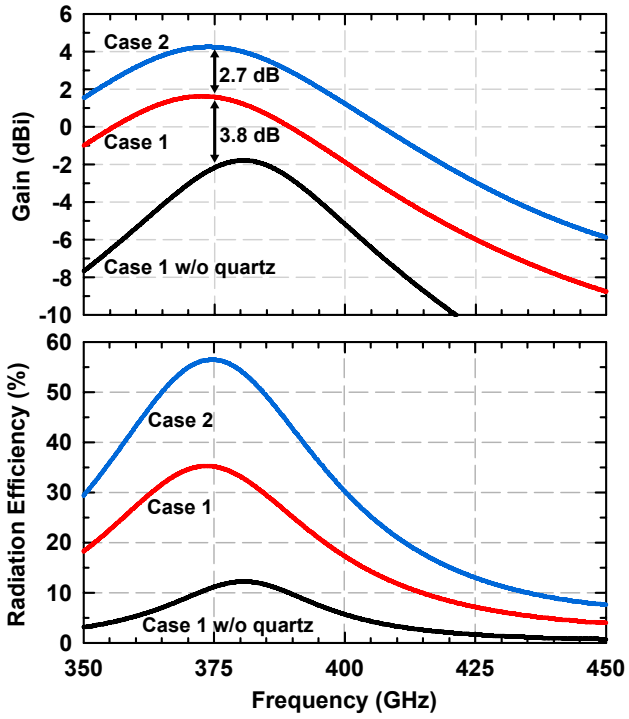


Figure 3.7: Simulated elliptical slot-ring antenna gain and efficiency.

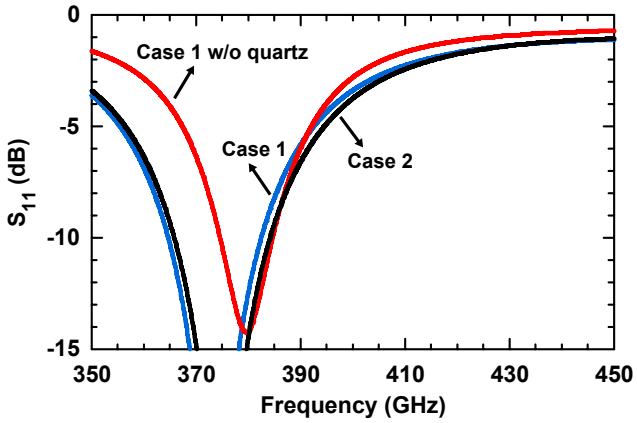


Figure 3.8: Simulated elliptical slot-ring antennas input return losses.

quartz superstrate (and meeting metal density rules) results in much reduced gain, efficiency, and bandwidth. Simulated return losses are $>$ 6 dB at 360-390 GHz in both cases (Fig. 3.8).

3.2.3 Amplifier/Splitter Distribution Network and 2×4 Antenna Array

A W-band amplifier is used to drive the quadrupler. The amplifier is similar to a design presented in [41] and results in a gain of 12 dB at 95 GHz and an output power of ∼8 dBm. The 2×4 array power distribution network is based on an equiphase 8:1 Wilkinson divider network. Three different Wilkinson combiners with similar performance are designed due to layout considerations. Sonnet simulations show a typical Wilkinson loss of ∼0.7 dB with $>$ 20 dB return losses and isolation at 95 GHz (Fig. 3.9). Referring to Fig. **??**, the input signal passes by three Wilkinson couplers (each 3.7 dB loss), transmission-line segments (∼2.5 dB loss total) and is amplified using an in-line amplifier with 12 dB gain. The overall distribution network gain is ∼-2 dB at 90-100 GHz where the gain is defined as the power at each amplifier/quadrupler port over the available input power.

The simulated 2×4 antenna array results in a directivity of 15 dB at 380 GHz and with a wide bandwidth, but the array gain is limited by the bandwidth of the antenna element. The simulated 2×4 array gain is 10.6 dB at 380 GHz with a 3 dB bandwidth of $>$ 50 GHz (Case 1) (Fig. 3.10). The simulated EIRP assuming an amplifier/quadrupler output power of 110-10 μW at 380-420 GHz is 9.5 dBm at 380 GHz with a 3 dB bandwidth of 350-390 GHz. A wider antenna bandwidth and higher EIRP can be achieved using a silicon lens, but as mentioned above, this increases the cost and is not used here.

3.3 Measurements

3.3.1 Standalone Quadrupler

The quadrupler chip is shown in Fig. 3.11. The input GSG pad is designed at W-band frequencies with 100-μm pitch. The output GSG pad is designed at WR-2.2 frequencies with $>$ 40-μm pitch using HFSS. The output return loss is measured using an OML 325-500 GHz extender and GGB 40-μm pitch GSG WR-2.2 waveguide probe. The measured output return loss (Fig. 3.12) is $>$ 7.5 dB at 330-430 GHz. The second harmonic reflector has virtually no effect on S_{22} since it results in an open circuit at the output node. The measured output return loss is more wideband than simulations due to the higher measured loss of the CPW line than obtained by simulations [41, 68].

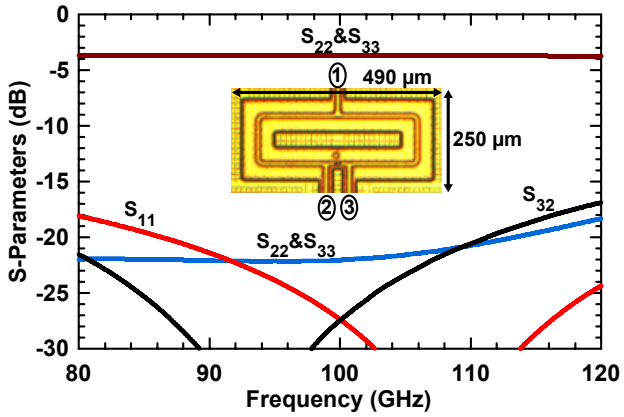


Figure 3.9: Simulated S-parameters of the W-band Wilkinson power divider.

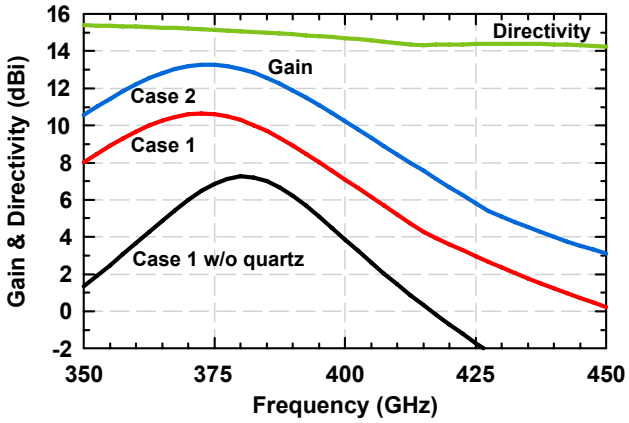


Figure 3.10: Simulated 2×4 antenna array gain and directivity.

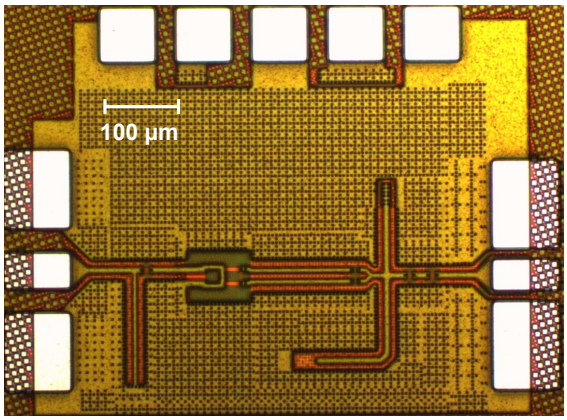


Figure 3.11: Microphotograph of the quadrupler (0.73 x 0.55 mm^2).

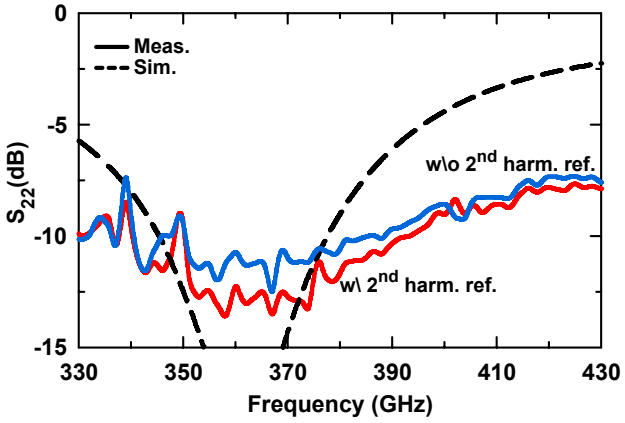


Figure 3.12: Measured and simulated output return loss.

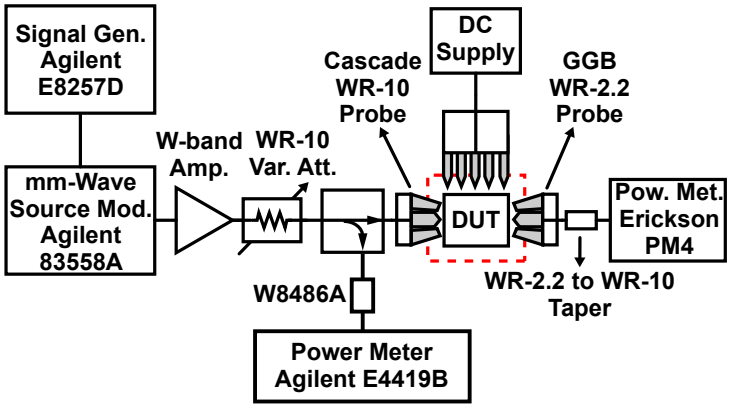


Figure 3.13: Measurement setup for quadrupler output power and conversion loss.

Fig. 3.13 presents the measurement setup for output power and conversion loss. All measurements are referenced to the GSG input and output pads (simulated loss of output pad is ∼0.5 dB at 400 GHz). The output is directly connected to an Erickson power meter (PM4) using WR-2.2 probe and a WR-2.2 to WR-10 taper. The measured loss of WR-10 probe is 1.5 dB at 100 GHz whereas the WR-2.2 probe has a loss of 4.9-8.5 dB across the WR-2.2 band [69]. Both probe losses are de-embedded from measurements and quoted results are referenced to GSG pads. The WR-2.2 section in the probe ensures that the first, second and third harmonic components (if present) are greatly attenuated before reaching the power meter.

Fig. 3.14 (a) presents the measured output power at 400 GHz versus input power with and without an output second harmonic reflector. No substantial difference is seen between these two cases, mostly due to the intrinstic low second harmonic level ($<$ 0.2-0.3 mW at 200 GHz while the input power is 10-20 mW). The measured peak output power is -8 dBm at an input power of 11-12 dBm with 19.5 dB conversion loss, and $>$ 100 μW of power can be obtained at 370-425 GHz (Fig. 3.14 (b)). The quadrupler is biased at 0 V gate bias to maximize the 4^{th} harmonic, and the drain current increases from ∼0 to 22 mA for an input power of -10 dBm to +13 dBm due to self-biasing. The measured output power is 2-3 dB lower than simulations and shifted to higher frequencies. Measurement beyond 425 GHz could not be performed due to the limitation of the W-band power amplifier, but it is fair to assume that the measured output power is $>$ 100 μW up to 430 GHz. The output power level and conversion loss is congruent with the best HEMT $\times$4 multipliers [70, 71]. The second harmonic was measured with a different set-up and the output second harmonic reflector results in a wideband rejection at 90-105 GHz ($2f_0$=180-210 GHz) (Fig. 3.14 (c)).

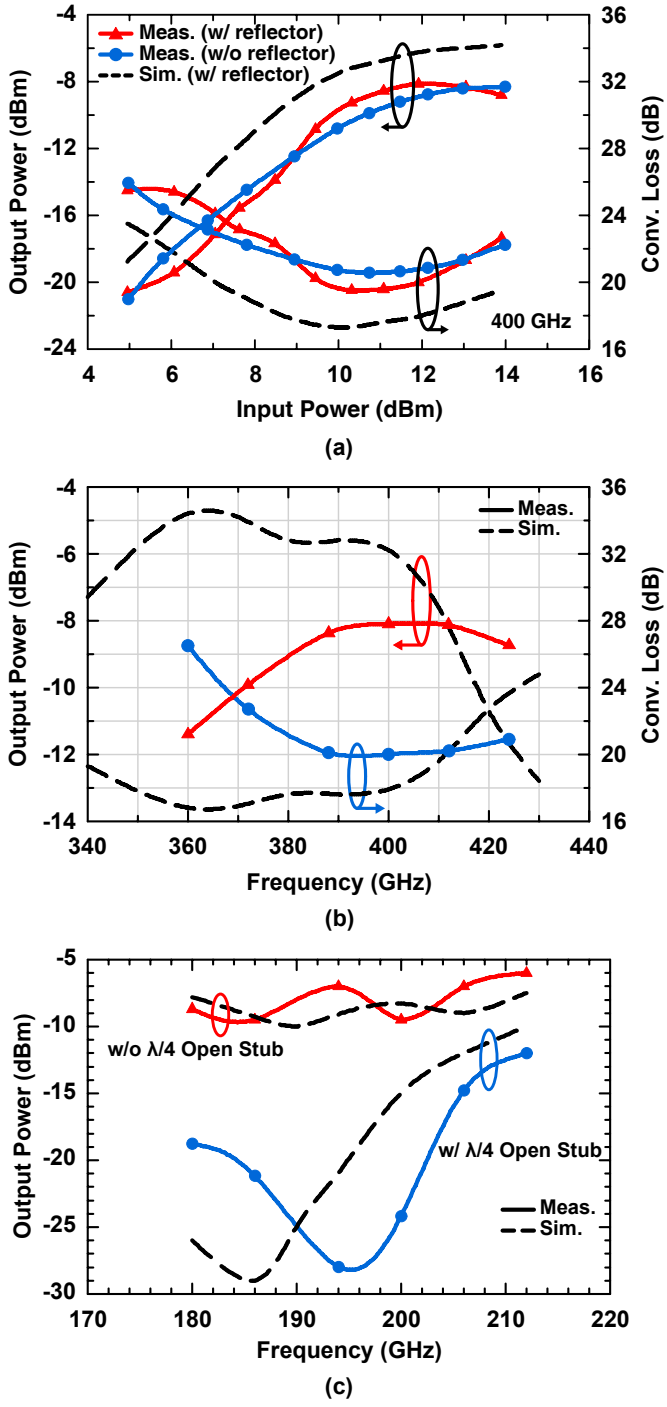


Figure 3.14: Measured and simulated (a) output power and conversion loss at 400 GHz of the quadrupler versus input power, (b) peak output power and (c) 2^{nd} harmonic output power versus frequency.

3.3.2 Quadrupler with Integrated W-band Driver

The chip microphotograph of the amplifier/quadrupler breakout is shown in Fig. 3.15(a) and with a size of 1 mm x 0.62 mm including the pads. The measured saturated output power is -11.8 and -11 dBm at 400 GHz and 412 GHz, respectively (Fig. 3.15(b)). The output power of the amplifier/quadrupler is smaller than the quadrupler standalone mesurements due to the limited output power of the driver amplifier.

3.3.3 2×4 Transmit Array

The microphotograph of the 2×4 transmit array is shown in Fig. 3.16 and consumes ∼500 mA from a 1.4 V supply in saturation level. The transmit array was measured using an external 23 dB standard gain horn placed 12 cm away from the silicon chip (Fig. 3.17 (a)). The far-field region for the standard gain horn is ∼3.5 cm and for the 2×4 array is ∼3.5 cm, and therefore, a distance of 12 cm is sufficient for accurate pattern measurements. A WR2.2 zero-bias Schottky detector was used for antenna pattern and power measurements, and its responsivity (∼2 kV/W) was measured at VDI. For pattern measurements, the transmit signal was pulse modulated at 1 kHz and the detected envelope of pulsed signal was measured using a lock-in amplifier. The signal to noise ratio was $>$ 20 dB for 10 ms integration time, resulting in clear patterns and sidelobes. Fig. 3.17 (b) presents the measured H-plane pattern at 400 GHz which agrees well with simulations. The 3-dB beamwidth is 10°, and the high sidelobe level at 50° is due to the element-to-element spacing of $1.45\lambda_0$ and $1.1\lambda_0$. Pattern measurements at 360-432 GHz show a similar behavior and agree well with simulations (Fig. 3.18).

The measured EIRP was calculated using the standard formula:

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi R}\right)^2$$

and

$$EIRP = P_t G_t = \frac{P_r}{G_r}\left(\frac{4\pi R}{\lambda}\right)^2$$

In this case, G_r = 22-24 dB at 360-420 GHz for the WR2.2 standard gain horn. Measurements were done every 500 MHz at W-band frequency which translate to a 2 GHz frequency step around 400 GHz. The measured EIRP is 3-4 dBm at 420 GHz with a 3-dB bandwidth of 395-435 GHz (Fig. 3.19 (a)). Measurements were done on two different set-ups with two different VDI detectors (calibrated at VDI) with the same chip. Note that the EIRP will become 6-7 dBm at 420 GHz if the antennas are built without any metal fill.

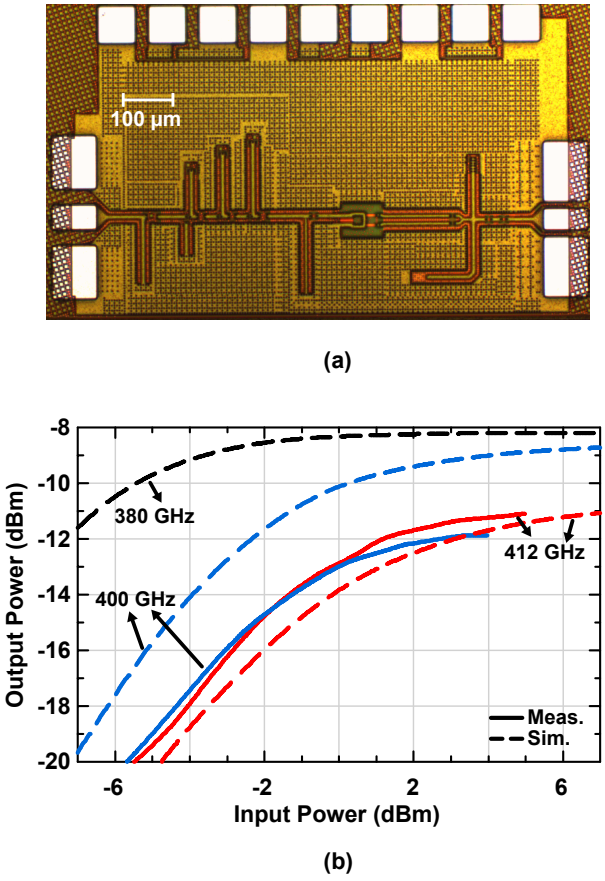


Figure 3.15: (a) Microphotograph of the amplifier/quadrupler (1 x 0.62 mm^2) and (b) simulated and measured output power at 380, 400 GHz and 412 GHz of the amplifier/quadrupler.

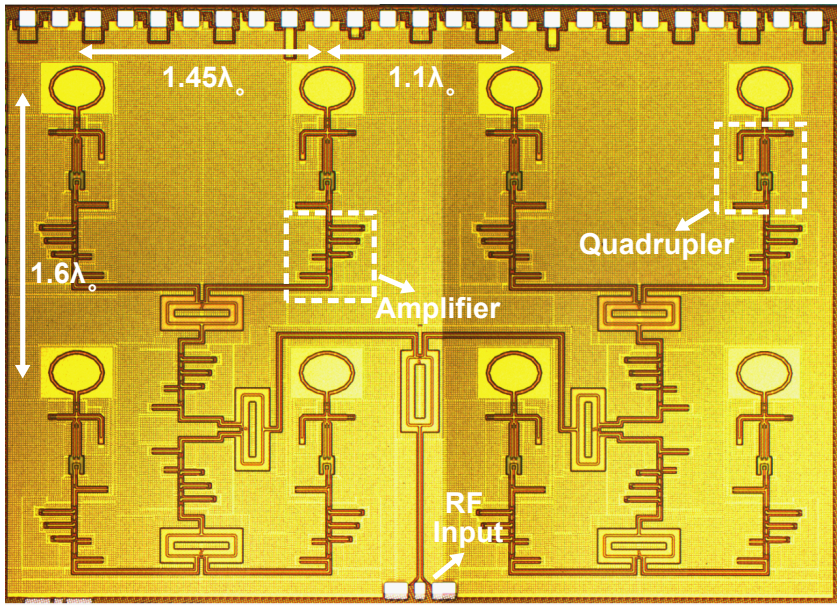


Figure 3.16: Chip microphotograph of the 2×4 amplifier-quadrupler array (2.7×3.8 mm^2).

There is a significant difference between measurement and simulations due to multiplier shifting in frequency to 420 GHz. At this frequency, the simulated 2×4 antenna array gain is 3 dB (see Fig. 3.10) and also, the on-chip driver amplifier does not result in 12 dBm of drive power [41]. Fig. 3.19(b) shows the measured EIRP at 400, 420, 432 GHz versus input power. The EIRP saturates at 400 GHz for an input power of 6 dBm at 100 GHz, while an input power of 12 dBm is required at 105 GHz due to the W-band amplifier response.

The radiated power from the array is 100 μW assuming an array directivity of 14 dB at 420 GHz (see Fig. 3.10). The power available at the 2×4 antenna inputs is a total of 1 mW at 420 GHz assuming a gain of 3 dB for the 2×4 array. This means that each amplifier-multiplier has an output power of ∼120 μW, which is not possible knowing that the on-chip W-band amplifier does not generate 12-13 dBm of power. Therefore, the only conclusion is that the slot-ring antenna shifted up in frequency and that the 2×4 array gain is ∼6-7 dB and not 3 dB at 420 GHz. This results in a total available power of ∼500 μW at the antenna inputs (∼65 μW per antenna) which is possible to obtain from the amplifier/multiplier at 105 GHz (as shown in Fig. 3.15).

Still, to our knowledge, this is the highest EIRP obtained from any CMOS chip to-date at 380-440 GHz (and without the use of any dielectric lenses which can significantly enhance the antenna gain and EIRP). The EIRP will increase by ∼3 dB if no metal fill is used under the antennas.

3.4 Conclusion

A 0.38-0.44 THz 2×4 CMOS amplifier-multiplier-antenna array was presented with a measured EIRP of 3-4 dBm at 420 GHz and the measured performance is summarized in Table 4.1. The array combines low-loss signal distribution and efficient signal amplification at W-band frequencies, together with a balanced quadrupler at each antenna element. The design can be scaled to any N×M array size for additional EIRP as shown in Fig. 3.20 for a 4×4 configuration, and can also be scaled to 600-700 GHz using a 150-175 GHz amplifier/distribution network. Also, it is expected that this topology can be used to generate 1 THz radiation using the recent work on 250 GHz amplifiers in advanced SiGe processes [65, 72].

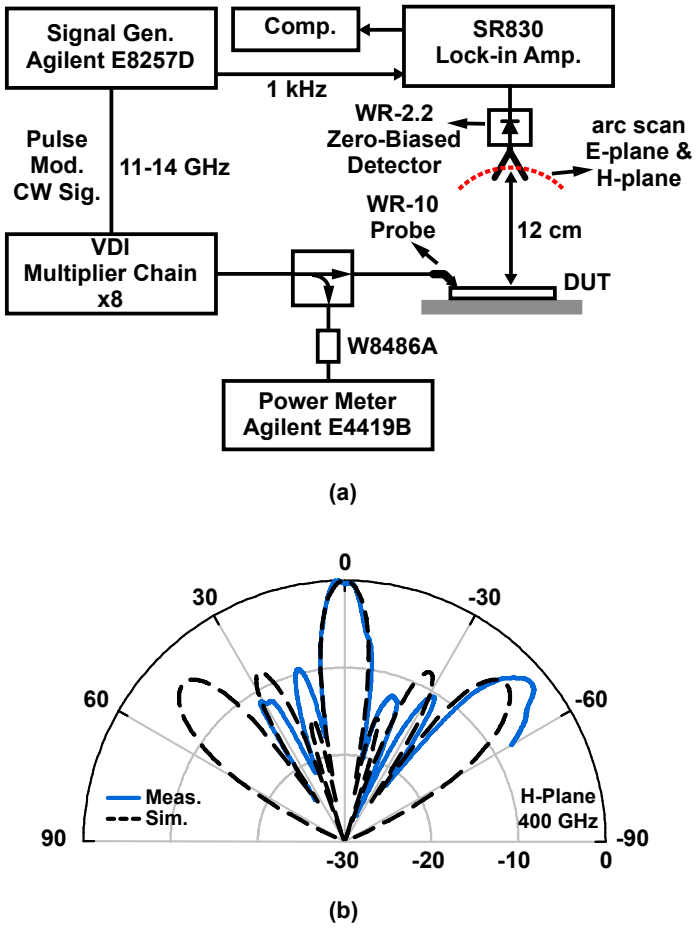


Figure 3.17: (a) Measurement setup for antenna patterns and EIRP and (b) measured and simulated H-plane antenna patterns of the 2×4 array at 400 GHz.

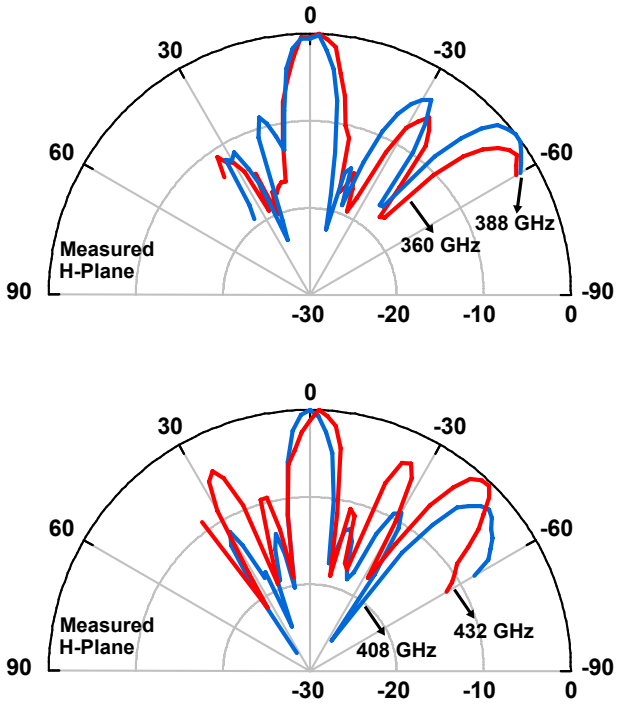


Figure 3.18: Measured H-plane antenna patterns of the 2×4 array at 360, 388, 408 and 432 GHz.

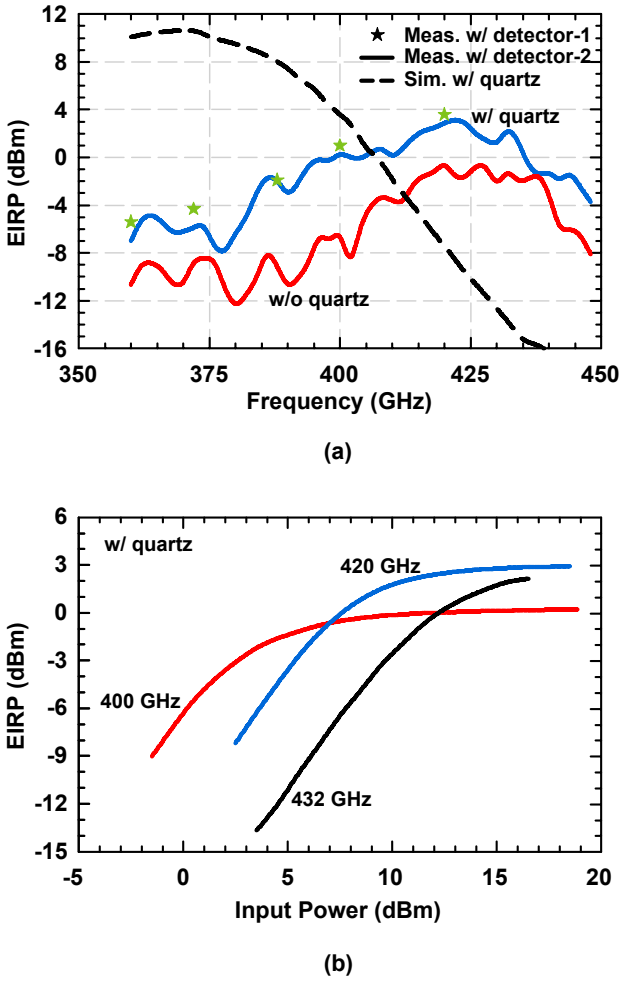


Figure 3.19: (a) Measured and simulated EIRP for the 2×4 array versus frequency with and without a quartz superstrate and (b) measured EIRP at 400, 420 and 432 GHz versus input power.

3.5 Acknowledgement

This work at UCSD was supported by the C2S2 Focus Center, one of six research centers funded under the Focus Center Research Program (FCRP), a Semiconductor Research Corporation entity. Part of this research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration. The authors would like to thank Ozgur Inac, University of California at San Diego (UCSD), La Jolla, and Dr. Mehmet Uzunkol, Qualcomm Inc., for his help in the measurements.

Chapter 3 is mostly a reprint of the material as it appears in IEEE Transactions on Microwave Theory and Techniques, 2013 and IEEE International Microwave Symposium, 2013. F. Golcuk, O. D. Gurbuz, Andy Fung and G. M. Rebeiz. The dissertation author was the primary author of this material.

Table 3.1: Summary of Antenna-Coupled Transmitters for 2×4 Amplifier-Quadrupler Array

	[38]	[36]	[37]	This work
Frequency (GHz)	260	280	288	420
Technology	65-nm Bulk CMOS	45-nm SOI CMOS	65-nm Bulk CMOS	45-nm SOI CMOS
Design	4×2 Oscillator	4×4 oscillator injection-locked	2×1 Triple-push oscillator	2×4 active quadrupler array
Antenna Type	Slot-antenna with silicon lens[c]	Diff. ring on a thinned substrate	Diff. ring with silicon lens[b]	Slot ring with quartz superstrate
P_{rad} (μW)	1100	190	390	100
BW (%)	1.4[d]	3	0	10
EIRP (dBm)	15.7	9.4	16.1	3[a]
Pdc (mW)	800	817	280	700

[a] Metal-fill is used. 3 dB better performance can be achieved without a metal-fill.

[b] Silicon lens size is 6.8λ at 300 GHz with 0.55 mm extension length.

[c] Hemispherical lens is used.

[d] Oscillator tuning range.

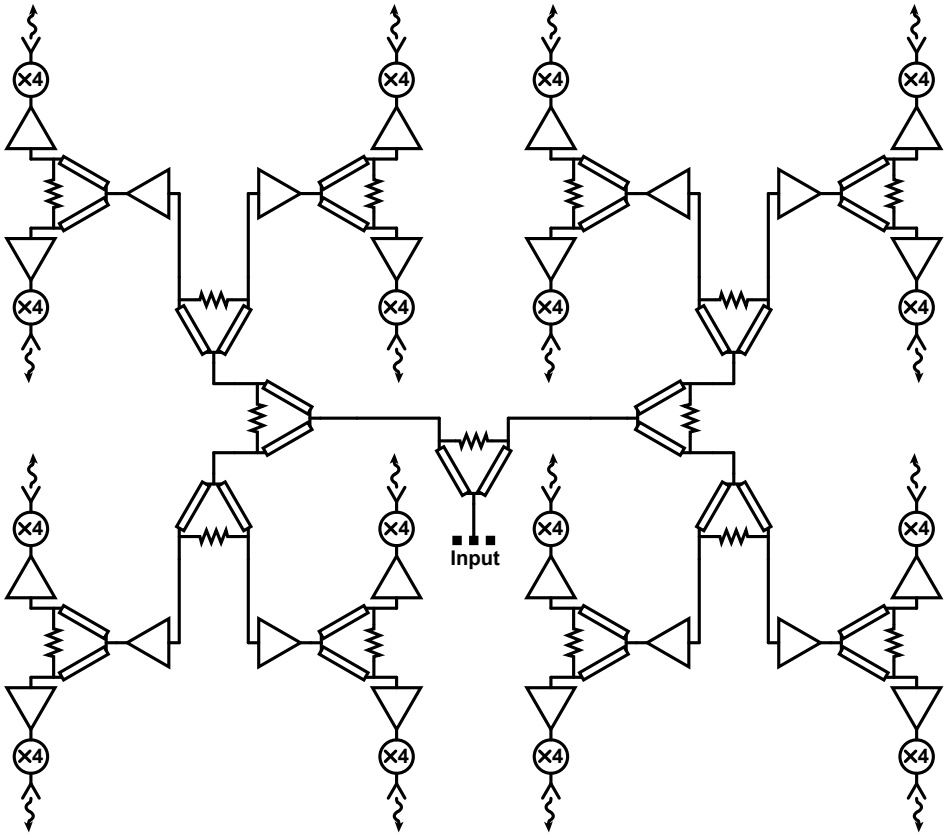


Figure 3.20: Block diagram of the 4×4 amplifier-quadrupler array.

Chapter 4

A 163-180 GHz 2×2 Amplifier-Doubler Array with Peak EIRP of +5 dBm

4.1 Introduction

Silicon systems at $>$ 150 GHz are becoming more popular for active and passive imaging systems, point-to-point communications and wideband spectroscopy [73, 74]. SiGe and CMOS sources have always been a challenge above 150 GHz due to their limited f_t and f_{max}. There are several solutions which have been proposed: 1) Injection-locked or N-push oscillators [37, 39, 40], and 2) multipliers [41–43]. The oscillator approach results in narrowband systems which are not suitable for wideband applications such as active imaging systems with low speckle, THz network analyzers, and spectroscopy. The multiplier approach results in wideband systems which can cover a 20-60 GHz bandwidth and can be easily locked to a W-band reference for low phase noise. Both can be placed in N×M arrays with on-chip antennas so as to increase the power and equivalent isotropic radiated power (EIRP) of the transmitter source.

This paper presents a 2×2 multiplier array at 163-180 GHz with a peak EIRP of +5 dBm in 45nm CMOS technology meeting the stringiest metal-density rules for antennas.

4.2 Design

Fig. 4.1(a) presents the architecture of the 2×2 transmitter array where each amplifier-doubler is connected to an on-chip slot-ring antenna. The amplifier-doubler is similar to a design presented in [41] and results in ∼0 dBm of power at 180 GHz (Fig. 4.1(b)). In order to keep the

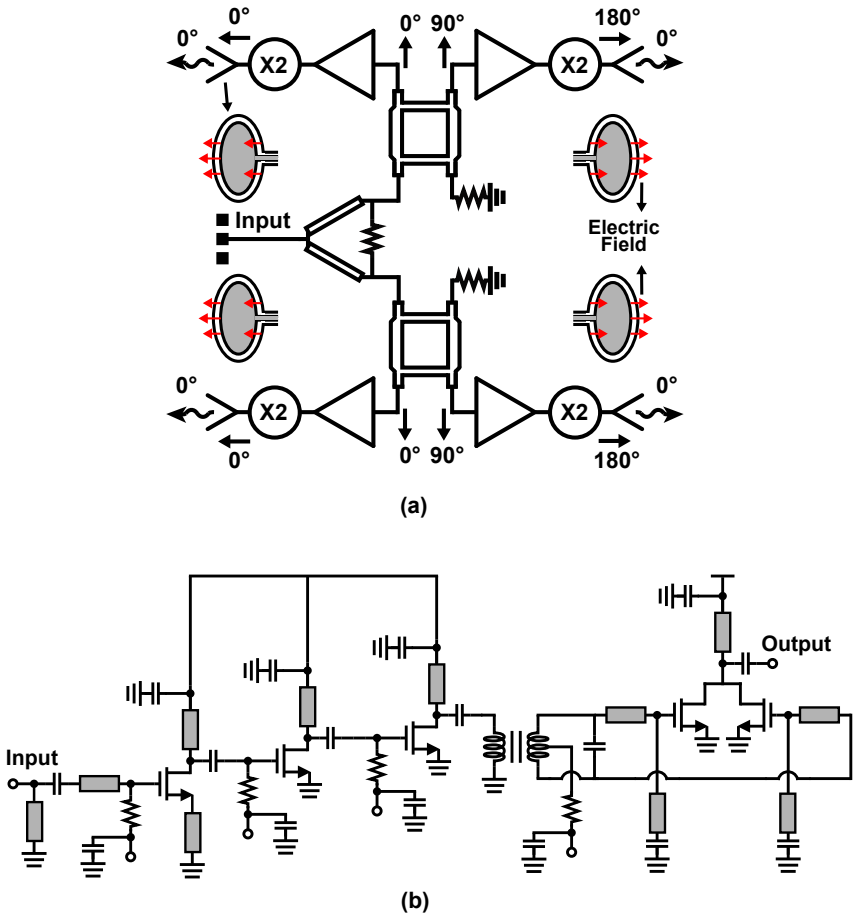


Figure 4.1: (a) Block diagram of the 2×2 amplifier-doubler array and (b) the amplifier-doubler schematic.

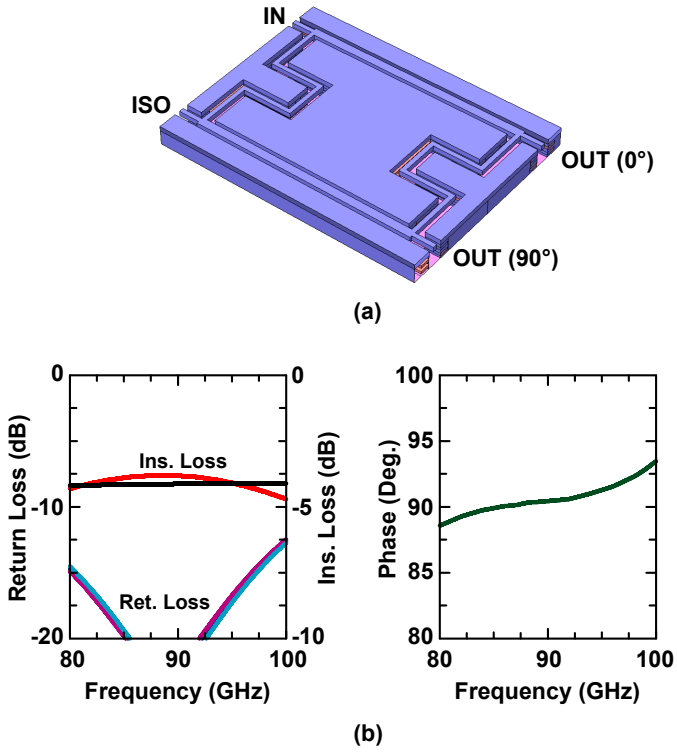


Figure 4.2: Branchline (a) sonnet layout and (b) simulated S-parameters.

antenna spacing $0.6\lambda_0$ at 180 GHz, and due to the layout consideration in 45nm CMOS where all the transistors have to be aligned in the same direction, the slot-ring antenna are fed on opposite sides for the left and right sides of the array. This configuration results in a 180° phase difference in the radiated fields from the left and right side antennas, which is not congruent with free-space power combining. Therefore, a branchline coupler is used before the amplifier-doublers at the left and right side antennas, and results in 3-dB power division and a 90° phase difference at 90 GHz. The output of the left and right side doublers are therefore 180° apart and the radiated fields are all in phase. Finally, a wilkinson power divider is used to divide the input signal in equal phase and amplitude between the top and bottom side of the array. This architecture is scalable to a 4×4 array (vertical and horizontal mirror with respect to the input port), using Wilkinson or active power dividers. In fact, the amplifier-multiplier approach is scalable to any N×M array size with no added complexity.

The chip is implemented in IBM 45-nm SOI process (IBM12SOI) with 220-230 GHz f_{max} referenced to the top metal layer [41]. Grounded coplanar waveguide (G-CPW) transmission lines with 9/8/9 μm (Z_0 = 50 Ω) are implemented using LB for the signal line and B3 for the ground plane. The measured loss of G-CPW line is 1.1 dB/mm at 90 GHz and ∼2 dB/mm

at 180 GHz [41]. The wilkinson and the branchline power dividers are designed using Sonnet 2.5-D EM solver with a simulated loss of 3.7 dB (Wilkinson). The branchline coupler shows an insertion loss of $\sim$4 dB with $<$ 0.3 dB and $<$ 2.5° gain and phase imbalance, respectively, at 80-98 GHz (Fig. 4.2(b)).

The 180 GHz elliptical slot-ring antenna is designed using a 200 μm quartz superstrate above the silicon chip (Fig. 4.3) [63]. The antenna is single-ended and placed on the top metal layer (LB), and the ground plane is defined as B3. This creates a parallel-plate condition which channels power away from the antenna and reduces its efficiency. The quartz superstrate is not patterned, and equalizes the propagation constant at the TEM mode in the dielectric layers on top of the silicon substrate, and the TM_0 mode in the quartz superstrate, to λ_d. This results in virtually little spurious radiation coupled to both modes from the two edges of the slot-ring antenna (spaced λ_d/2).

The slot-ring antenna with a quartz superstrate, and without meeting any metal-density rules, results in a radiation efficiency of 28$\%$ and a gain of 1.3 dB at 180 GHz with a 3-dB bandwidth of 165-195 GHz. However, in this work, the antennas are designed to meet the stringiest metal density rules so that no metal exclusion is taken on the wafer, which is congruent with industrial-level designs. The radiation efficiency drop to 13$\%$ and the gain drops to -2.3 dB when the metal fill is connected to each other (see Case 1). Still, this is $\sim$4 dB higher than the case without a quartz superstrate, showing the importance of this design technique (Fig. 4.4).

The 45 nm CMOS has such a high metal density requirement that it provides a severe environment for antennas radiating from the top side of the chip. Better performance can be obtained with the antennas radiating from the bottom side of the chip, but it either requires thinning the wafer to $\sim$100μm [36], or using a dielectric lens [37]. Both are expensive and not congruent with low cost techniques (mounting thick wafers on any standard PCB). It is for this reason that it has been decided to work with antennas with top-side radiation.

The simulated directivity and gain of the 2$\times$2 array is 12.5 dB and 3.6 dB (case 1) at 180 GHz, respectively (Fig. 4.5). The gain drops to 1.6 dB at 170 GHz since the array is electrically smaller and there is the inherent -10 dB bandwidth of the antennas. The mutual coupling between the antennas is very low ($<$ -25 dB) in both E and H planes. The simulated S_{11} for both antennas (with and without metal fill) shows a -10 dB bandwidth of 170-180 GHz (design was done at 180 GHz, more accurate HFSS simulations showed that it shifted to 175 GHz) (Fig. 4.6).

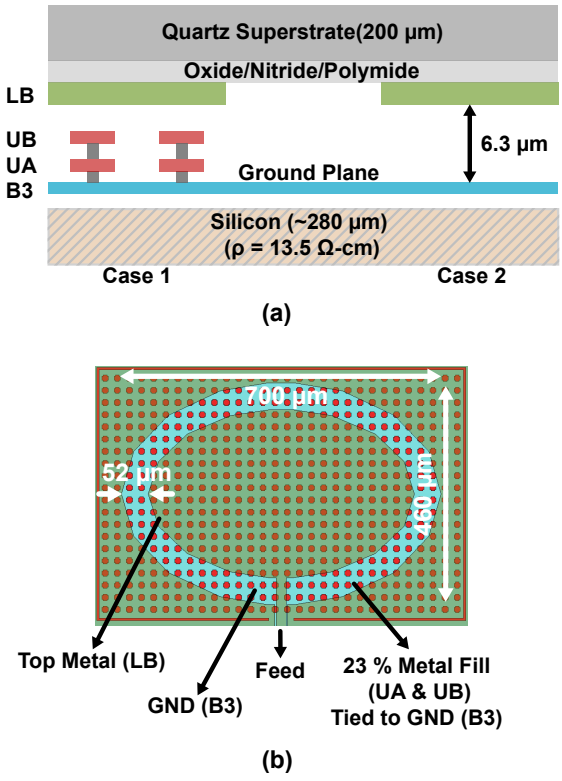


Figure 4.3: (a) Metal-fill cases and (b) on-chip single-ended slot antenna with the metal-fill underneath the antenna.

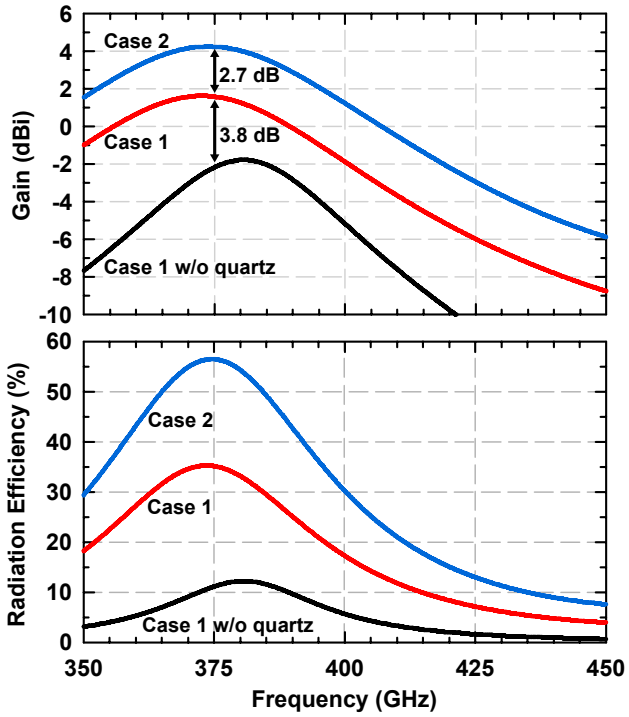


Figure 4.4: Simulated elliptical slot-ring antenna gain and efficiency.

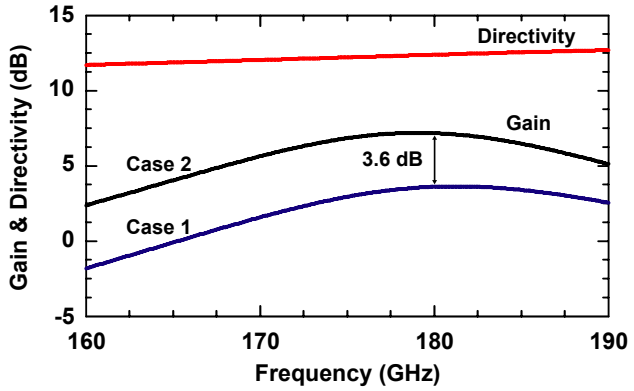


Figure 4.5: Simulated 2×2 antenna array gain and directivity with a quartz superstrate.

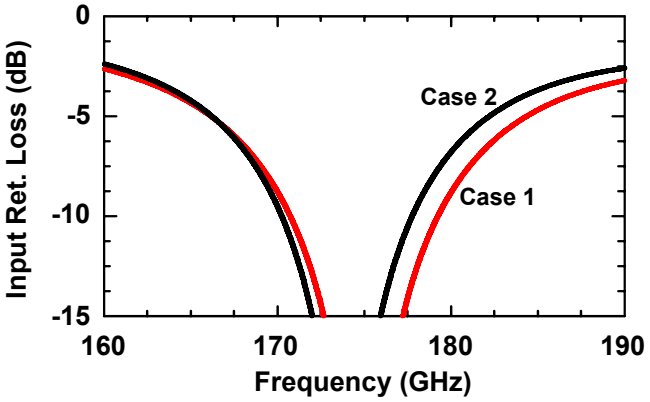


Figure 4.6: Simulated elliptical slot-ring antenna input return loss.

The 2×2 array results in a total EIRP of

$$EIRP = P_t \times G_t = 8.6 \ dBm$$

where P_t=+5 dBm is the power available at the four antenna inputs (0 dBm/element and -1 dB transmission-line loss between the doubler and the antenna). The EIRP can also be written in terms of the directivity as:

$$EIRP = P_{Radiated} \times D_t$$

an the total radiated power is found to be -3.9 dBm (400 μW) at 180 GHz.

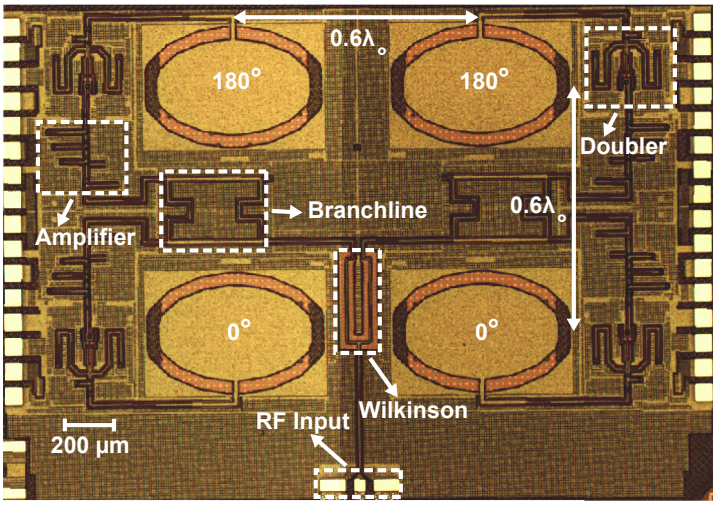
4.3 Measurements

Fig. 4.7(a) presents the chip microphotograph. The total size is 2×2.9 mm^2 including the RF and DC pads.

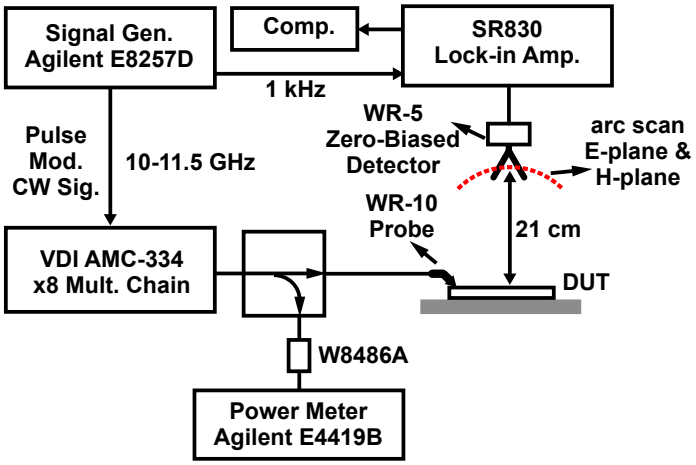
The current consumption of the W-band amplifier is 30 mA from 1.4 V supply, and the amplifier/doubler delivers $>$ -3 dBm at 170-190 GHz with 0 dBm peak output power at 180 GHz. The 2×2 amplifier-doubler array is characterized for antenna pattern and EIRP measurements using a far-field setup as shown in Fig. 4.7(b). The input signal is amplitude modulated at 1 kHz with 50 % duty cycle using an Agilent signal generater (E8257D) followed by a multiplier chain from Virginia Diodes, Inc. (VDI) with $>$ 20 dBm output power at 72-90 GHz [75]. The radiated signal is received by the WR-5 conical horn antenna followed by the zero-biased WR-5 detector with a responsivity of ∼250 V/W (characterized at UCSD using an Erickson Power Meter). The detected envelope of the radiated signal is sent to the SRS-830 lock-in amplifier.

The measured H-plane patterns at 166 GHz, 170 GHz and 180 GHz are shown in Fig. 4.8 together with the simulated H-plane pattern at 180 GHz. The antenna patterns are measured from -46° to +46° with a 2° step due to the physical limitation of the circular arm setup used over the probe station. The antenna is designed at 180 GHz, but the center frequency shifted to 170 GHz. Still, good agreement is seen between the simulated and measured results. Note the ±1 dB ripple in the measured patterns due to the presence of a large ground plane (metal chuck) below the chip.

Fig. 4.9 presents the measured broadside EIRP at 166 GHz, 170 GHz and 176 GHz versus input power. Since the on-chip W-band amplifier has a lower gain at 83 GHz than at 88 GHz, the required input power is higher to saturate the multipliers. The current consumption of the array is 124 mA from 1.4 V supply under quiescent condition, and 191 mA in saturation due



(a)



(b)

Figure 4.7: (a) Microphotograph of the 2×2 amplifier-doubler array (2 x 2.9 mm^2 including pads), and (b) Measurement setup for antenna patterns and EIRP.

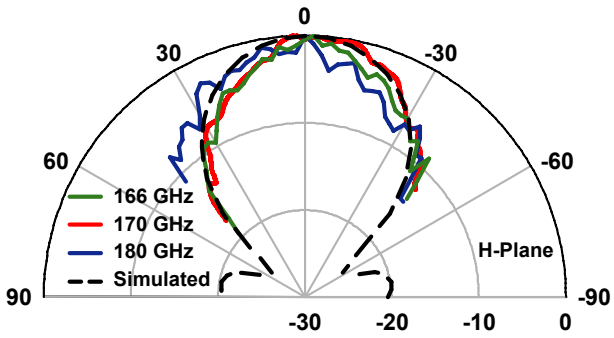


Figure 4.8: Simulated (180 GHz) and measured H-plane patterns with a quartz superstrate.

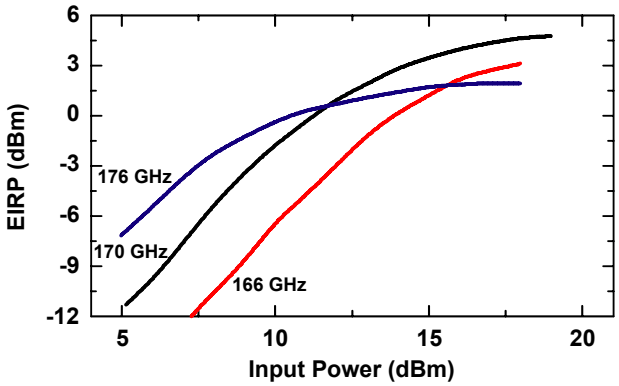


Figure 4.9: Measured EIRP versus input power at 166-176 GHz with a quartz superstrate.

to self-biasing. The measured EIRP versus frequency with and without the quartz superstrate is shown in Fig. 4.10.

The measured peak EIRP versus frequency with and without a quartz superstrate is shown in Fig. 4.10. The measured 3-dB bandwidth is 165-175 GHz with peak EIRP of +5 dBm at 170 GHz with a quartz superstrate. Again, the ripple in the EIRP versus frequency is due to the standing waves in the setup. The quoted EIRP is obtained using a 7-point rolling average to reduce the effect of the ripples. The measured (average) EIRP is very close to simulations at 170 GHz (5 dBm versus 5.6 dBm).

4.4 Conclusion

A 2×2 amplifier-doubler array has been presented at 165-180 GHz. The measured EIRP of the array meeting the metal density rules for the antennas is comparable to the oscillators in this frequency range (Table 4.1). It is seen that advanced CMOS technology can result in wideband sources for applications such as low-cost imaging systems and spectroscopy.

4.5 Acknowledgement

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Chapter 4 is mostly a reprint of the material as it appears in IEEE Radio Frequency Integrated Circuit Symposium, 2013. F. Golcuk, J. M. Edwards, B. Cetinoneri, Y. A. Atesal, and G. M. Rebeiz. The dissertation author was the primary author of this material.

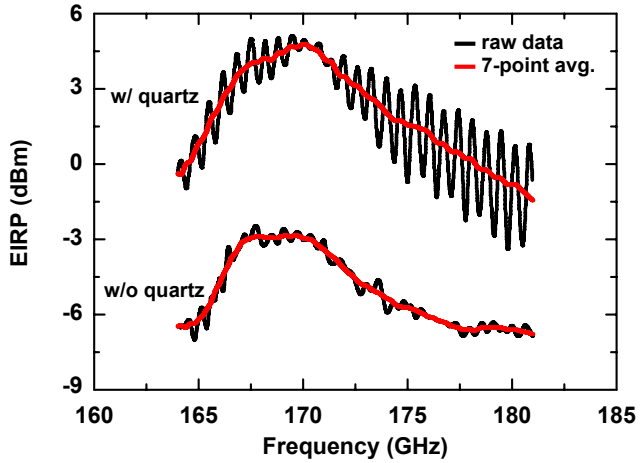

Figure 4.10: Measured EIRP versus frequency with and without quartz superstrate. Measurements are taken with 200 MHz steps.

Table 4.1: Summary of Antenna-Coupled Transmitters for 2×2 Amplifier-Doubler Array

	[38]	[36]	[37]	This work
Frequency (GHz)	260	280	288	170
Technology	65-nm Bulk CMOS	45-nm SOI CMOS	65-nm Bulk CMOS	45-nm SOI CMOS
Design	4×2 Oscillator	4×4 oscillator injection-locked	2×1 Triple-push oscillator	2×2 active doubler array
Antenna Type	Slot-antenna with silicon lens[c]	Diff. ring on a thinned substrate	Diff. ring with silicon lens[b]	Slot ring with quartz superstrate
P_{rad} (μW)	1100	190	390	200
BW (%)	1.4[d]	3	0	8
EIRP (dBm)	15.7	9.4	16.1	5[a]
Pdc (mW)	800	817	280	267

[a] Metal-fill is used. 3 dB better performance can be achieved without a metal-fill.

[b] Silicon lens size is 6.8λ at 300 GHz with 0.55 mm extension length.

[c] Hemispherical lens is used.

[d] Oscillator tuning range.

Chapter 5

Conclusion

In Chapter 2, a 4×4 transmit/receive SiGe BiCMOS phased array chip in an advanced SiGe technology (IBM8HP) at 90-100 GHz with vertical and horizontal polarization capabilities, 3-bit gain control (9 dB) and 4-bit phase control was presented. The 4×4 phased array fits into a 1.6×1.5 mm^2 grid, which is required at 94 GHz for wide scan-angle designs. The chip has simultaneous receive beam capabilities (V and H) and this is accomplished using dual-nested 16:1 Wilkinson combiners/divider with high isolation. The phase shifter is based on a vector-modulator with optimized design between circuit level and electromagnetic simulation and results in $<$ 1 dB and $<$ 7.5° rms gain and phase error, respectively, at 85-110 GHz. The behavior of the vector modulator phase distortion versus input power level is investigated and measured. The V and H receive paths result in a gain of 22 dB and 25 dB, respectively, a noise figure of 9-9.5 dB (max. gain) and 11 dB (min. gain) measured without the T/R switch, and an input P_{1dB} of -31 to -26 dBm over the gain control range. The measured output P_{sat} is ∼-5 dBm per channel, limited by the T/R switch loss. Measurements show ±0.6 dB and ±0.75 dB variation between the 4×4 array elements in the transmit mode (P_{sat}) and receive mode, respectively, and $<$ -40 dB coupling between the different channels on the chip. The chip consumes 2.2 W in both the transmit and dual-receive modes. Future work includes a redesign of the GSG pad and the power amplifier chain for improved performance. The design can be scaled to $>$ 10,000 elements using polyimide redistribution layers on top of the chip and the application areas are in W-band radars for landing systems.

In Chapter3, a CMOS 0.38-0.44 THz 2×4 amplifier-multiplier-antenna array was presented with a measured EIRP of 3-4 dBm at 420 GHz. The chip is built using a 45nm CMOS SOI (IBM12SOI) process and efficient on-chip antennas are used to extract the power out of

the chip. The array combines low-loss signal distribution and efficient signal amplification at W-band frequencies, together with a balanced quadrupler capable of delivering up $>$ 100 μW of power at 370-430 GHz at each antenna element. The amplifier-multiplier concept is proven on a 2$\times$4 array, and can be also scaled to any N$\times$M array size for additional EIRP, and can also be scaled to 600-700 GHz using a 150-175 GHz amplifier/distribution network. Also, it is expected that this topology can be used to generate 1 THz radiation using the recent work on 250 GHz amplifiers in advanced SiGe processes [65, 72].

In Chapter 4, a 2$\times$2 amplifier-doubler array with on-chip antennas at 163-180 GHz in 45 nm CMOS SOI technology was presented at 165-180 GHz. The design is based on a 80-100 GHz distribution network with splitters and amplifiers, and a balanced doubler capable of delivering up $>$ 0.5 mW of power at 170-190 GHz. The measured EIRP is $>$ 2 dBm at 165-175 GHz with a peak value of 5 dBm at 170 GHz meeting the stringiest metal-density rules for antennas and comparable to the oscillators in this frequency range. It is seen that advanced CMOS technology can result in wideband sources for applications such as low-cost imaging systems and spectroscopy. It is seen from the both multiplier arrays, the multiplier approach has a higher frequency bandwidth than the oscillator approach.

The 4$\times$4 phased array chip showed excellent on-chip performance in terms of the gain, phase, coupling and isolation using waveguide probes, but it is important to have the chip packaged with little performance degradation. Conventional bond-wire packaging will not be suitable due to the ground inductance effect and 4$\times$4 configuration since the chip is a single-ended design due to the area and power consumption limitations. Flip-chip package could be used if the design were differential. However, ground inductance will be much higher in a flip-chip package than in a package using polyimide RDL and can effect the performance metrics. Therefore, it is essential that the chip be packaged using Teledyne Scientific RDL technologies as shown in Fig. 5.1.

Both multiplier arrays in this dissertation have radiation pattern only at broadside. In order to have short range from multi-point to multi-point communication, it is necessary to have a capability to scan the beam. Therefore, an 8-element (1$\times$8) phase shifter-amplifier-quadrupler transmitter phased array at 400 GHz has been designed and taped-out by Yang Yang in June 2013 (Fig. 5.2). A 5-bit (11.25°) phase shifter was placed before the amplifier at each element to control the phase of the channel. It is also possible to design amplifier-quadrupler array at 1 THz using amplifiers at 200-250 GHz to drive the multipliers in advanced CMOS process such as IBM 32-nm CMOS SOI process.

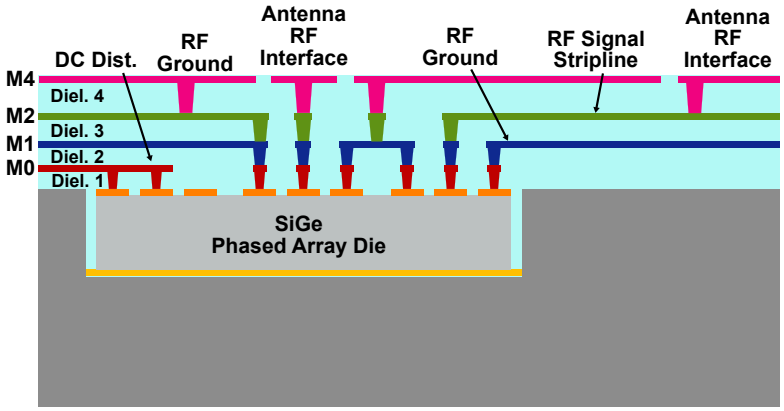

Figure 5.1: Polyimide RDL technology (Courtesy of Dr. Jon Hacker, Teledyne Scientific, CA).

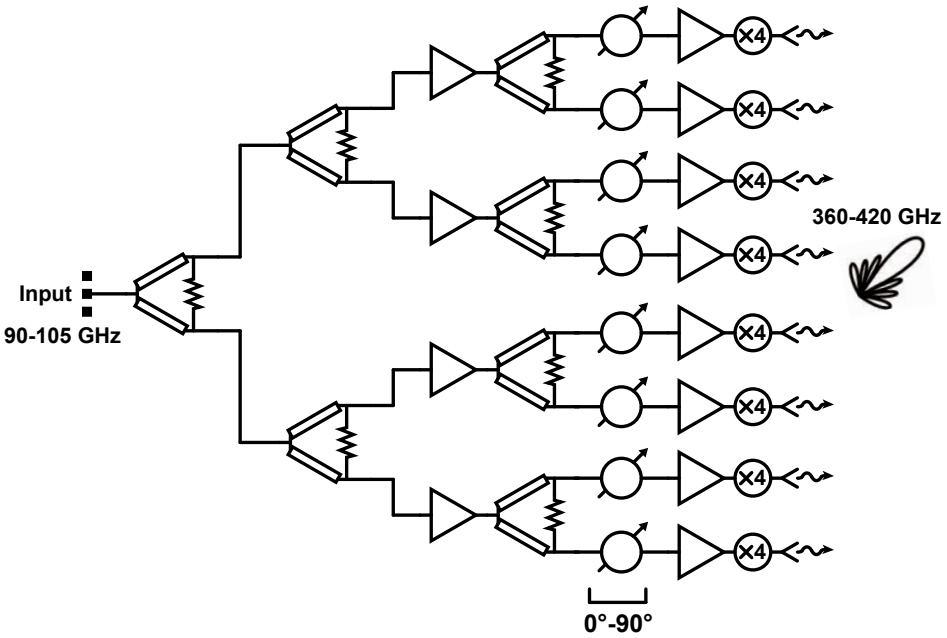

Figure 5.2: 8-element quadrupler based phased array with a low loss W-band distribution network.

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