UNIVERSITY OF CALIFORNIA, SAN DIEGO

Interference Mitigation Techniques for SAW-less CDMA Receivers

A dissertation submitted in partial satisfaction of the
requirements for the degree
Doctor of Philosophy

in

Electrical Engineering (Electronics Circuits and Systems)

by

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2009

The dissertation of Himanshu Khatri is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Chair

University of California, San Diego

2009

DEDICATION

To my parents,

brother Dhiraj and sister-in-law Shweta.

EPIGRAPH

Live as if you were to die tomorrow. Learn as if you were to live forever.

Mahatma Gandhi

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ACKNOWLEDGEMENTS

I am most thankful to my research advisors: Professor Larry Larson, Dr. Prasad Gudem and Professor Donald Lie. I always find Professor Larson's advices helpful and his comments constructive. Without his moral support, patience and perseverance, I could have never imagined to finish this dissertation. Dr. Gudem has a clarity of thought, a practical approach and a deep understanding of the RFIC systems. He is very helpful and provided invaluable comments to my research. Professor Lie advised me during the initial phase of my research. His comments were quite insightful for my very first paper. All of my advisors have always been a source of inspiration for me. I am indebted for their help and support.

I would also like to thank the members of my committee, Professors Chung-Kuan Cheng, Miroslav Krstic, Gabriel M. Rebeiz and Paul Yu, for their invaluable suggestions and recommendations to this dissertation.

I wish to acknowledge all my colleagues for their inspiring discussions and suggestions. I would especially like to acknowledge: Dr. Rahul Kodkani (NXP), Dr. Junxiong Deng (Qualcomm), Dr. Mahim Ranjan (Qualcomm), Dr. Vincent Leung (Qualcomm), Dr. Joe Jamp (Atheros), Mr. Yiping Han, Mr. Mohammad Farazian, Mr. Sanghoon Park, Mr. Pavel Kolinko, Mr. Sean Kim, Mr. Ankit Srivastava and Mr. Nikhil Rasiwasia. I also sincerely thank Dr. Donald Kimball, Mr. Pavel Kolinko and Mr. Cvong Vu for their support, discussions and debugging in the lab. I also gratefully acknowledge the financial provided by the Center for Wireless Communications and the UC Discovery Grant.

It would be unfair not to acknowledge my parents Dr. Arjun Dass Khatri and Mrs. Supreet Khatri, who left no stone unturned to support my efforts at each stage of my life. I am also thankful to my brother Mr. Dhiraj Anand Khatri, my sister-in-law Mrs. Shweta Khatri and my aunt Mrs. Jyoti Arora for their constant support and inspiration during this research work.

The text of Chapter Two, Three, Four and Five, in part of in full, is a reprint of the material as it appears in our published papers or as it has been submitted for publication in IEEE Transactions on Microwave Theory and Techniques, IEEE International Microwave Symposium and Silicon Monolithic Integrated Circuits in RF Systems

(SiRF). The dissertation author was the primary researcher and the first author listed in these publications. He directed and supervised the research which forms the basis for these chapters.

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PUBLICATIONS

H. Khatri, P. S. Gudem, and L. E. Larson, "A SAW-less CMOS CDMA receiver with active Tx filtering," submitted to *IEEE Custom Integrated Circuits Conf.*, CICC, 2009.

H. Khatri, P. S. Gudem, and L. E. Larson, "Distortion in current commutating passive CMOS downconversion mixers," submitted to *IEEE Trans. Microw. Theory Tech.*, 2009.

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ABSTRACT OF THE DISSERTATION

Interference Mitigation Techniques for SAW-less CDMA Receivers

by

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Doctor of Philosophy in Electrical Engineering (Electronics Circuits and Systems)
University of California San Diego, 2009
Lawrence E. Larson, Chair

This research work aims at eliminating the off-chip RF SAW filters from frequency division duplexed (FDD) receivers. In the first approach, a monolithic passive RF filter was constructed using on-chip capacitors and bondwire inductors. The bondwire characteristics were studied in details and the effect of mutual inductive coupling between the bondwires on the filter performance was analyzed. Based on that, a bondwire configuration was proposed to improve the frequency response of the filter. The filter was implemented in 0.18 μm CMOS process for WCDMA applications.

In the second approach, the downconverting mixer linearity performance was improved. It was observed that BSIM3 CMOS model fails to predict the transistor linearity behavior perfectly at zero drain-source bias voltage. It was analytically shown using Volterra series analysis that the incorrect simulation of passive mixer linearity is a consequence of this anomaly. Using Volterra series analysis, the second-order, third-order and cross-modulation linearity of a passive mixer was studied and analytical expressions were obtained to reflect their dependence upon the mixer source and load impedances. Based on this, it was formulated that the mixer linearity can be improved by selectively filtering the downconverted transmitted signal at the mixer output. A novel filtering mechanism was proposed that comprised of another downconverting mixer in cascade with a trans-impedance amplifier. This approach was used to implement a CDMA-2000 receiver for PCS band (1.96 GHz) in 0.18 μm CMOS process. The proposed technique improved the triple beat and IIP_2 by 6.5 dB.

Chapter 1

Introduction

1.1 Distortion in Cellular Receivers

Code-Division Multiple Access (CDMA) based cellular technologies are used worldwide for voice and data communication. These communication standards are frequency-division duplexed (FDD), i.e., the mobile station receives and transmits data simultaneously over different frequency bands. This feature provides uninterrupted communication without delay.

1.1.1 Transmitter Signal Leakage in Receiver Path

The transmitter (Tx) and receiver (Rx) in a mobile station communicate with the base-station via a single antenna. Typically, a three-port duplexer filter is employed for this interaction, so that it can provide ample isolation between the Tx and Rx. Consider the scenario when the mobile station is at the edge of a cellular boundary so that the signal strength from the base station is weak. In this scenario, the received signal is very weak, while the transmitted power is the strongest allowed, so that the base station can receive the uplink signal. In this extreme scenario shown in Fig. 1.1, there is significant Tx leakage in the receiver path.

For instance, in a W-CDMA transceiver, the maximum allowed transmitted power at the antenna is +24 dBm. This implies +26 dBm Tx power at the PA output. A typical duplexer provides 55 dB isolation between Rx and Tx. Hence, the Tx leakage at the

LNA input will be -29 dBm. At the same time, the minimum detectable signal (MDS) for the receiver is -114 dBm. Although in a different frequency band, the Tx leakage is 85 dB stronger than the desired Rx signal. Unless filtered, this Tx can produce in-band interference through different distortion mechanism.

Second-order Distortion

Zero Intermediate Frequency (ZIF) or Direct Conversion Receiver (DCR) architectures have gained widespread attention due to their lower cost and simplicity advantages over the heterodyne architectures. In a DCR, the received signal is downconverted to baseband. As the Tx leakage is a modulated signal, it creates interference in baseband due to the second-order distortion in the downconverter, as shown in Fig. 1.2. As the Tx signal is much stronger than the Rx, the receiver IIP_2 specification becomes very stringent. This would imply a larger power consumption to improve device linearity. The second-order distortion is also contributed by the mismatches in the devices. Hence, an expensive process with lower tolerances might be required to meet the stringent IIP_2 specification. This problem can be addressed by filtering the Tx leakage signal before it reaches the downconverter.

Typically, the LNA is coupled to the mixer through capacitors, which filters off any low frequency content generated due to second-order distortion in the LNA. Hence, the receiver IIP_2 specification is not affected by the LNA performance.

Cross-modulation Distortion

Another corner case is comprised of the scenario when – in addition to the above conditions (strong Tx and weak Rx), – another single-tone or continuous wave (CW) blocker is present in the vicinity of the Rx band as shown in Fig. 1.3. This CW blocker can be attributed to an AM signal or other communication standards. Due to the third-order distortion in the receiver, the modulated Tx leakage signal can cross-modulated with the CW blocker to create in-band distortion, as shown in Fig. 1.4 [1].

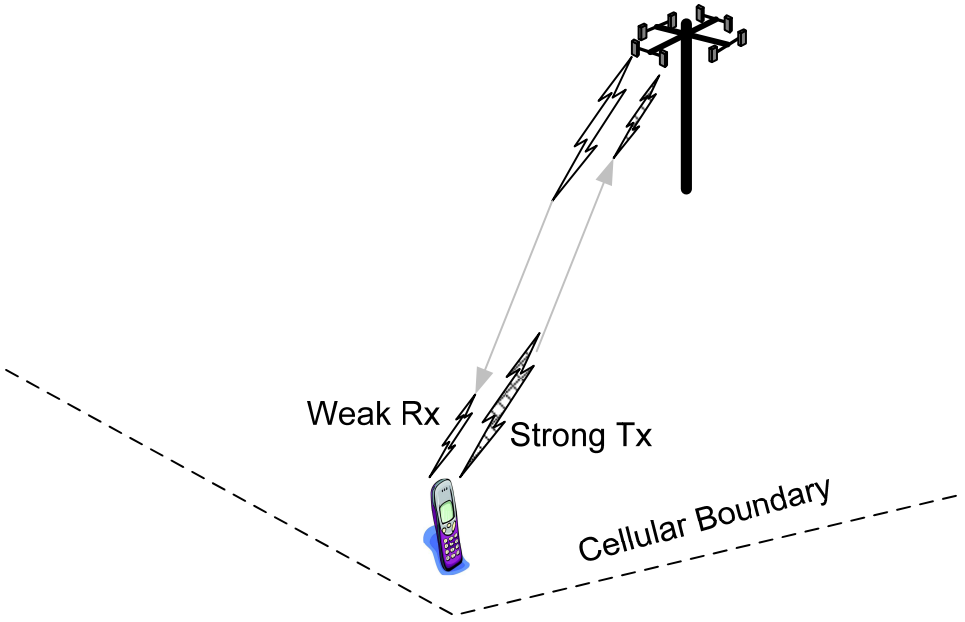


Figure 1.1: Base station and mobile station signals when the mobile station is at the edge of the cellular boundary.

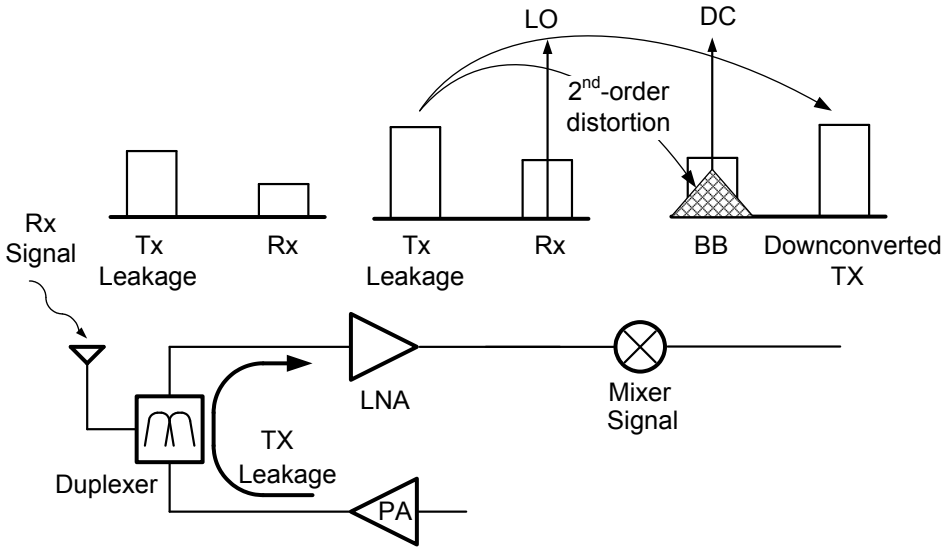


Figure 1.2: Tx leakage interference due to second-order distortion in the downconverter.

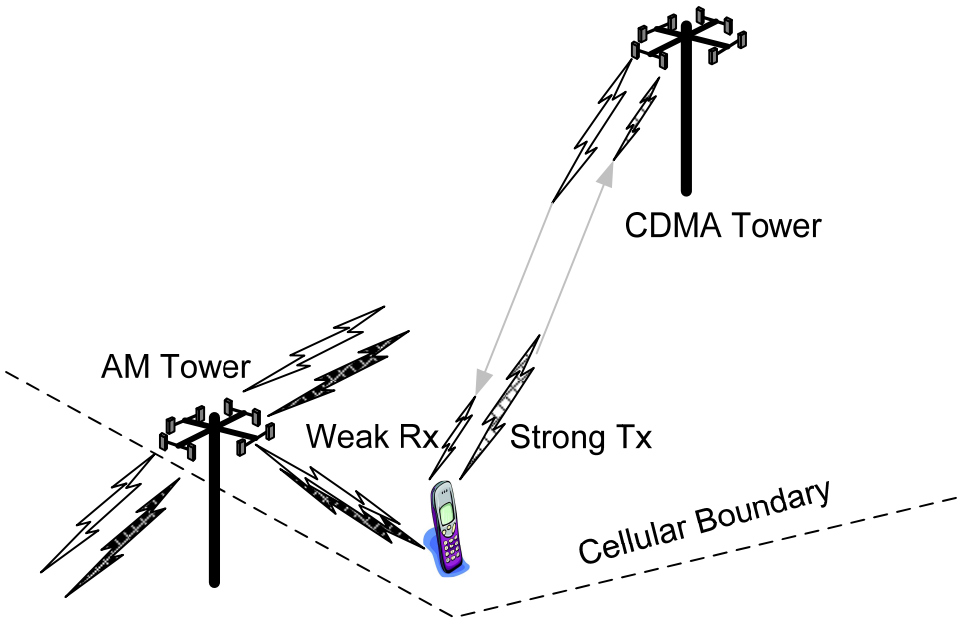


Figure 1.3: Base station and mobile station signals when the mobile station is at the edge of the cellular boundary and there is a strong AM signal presence.

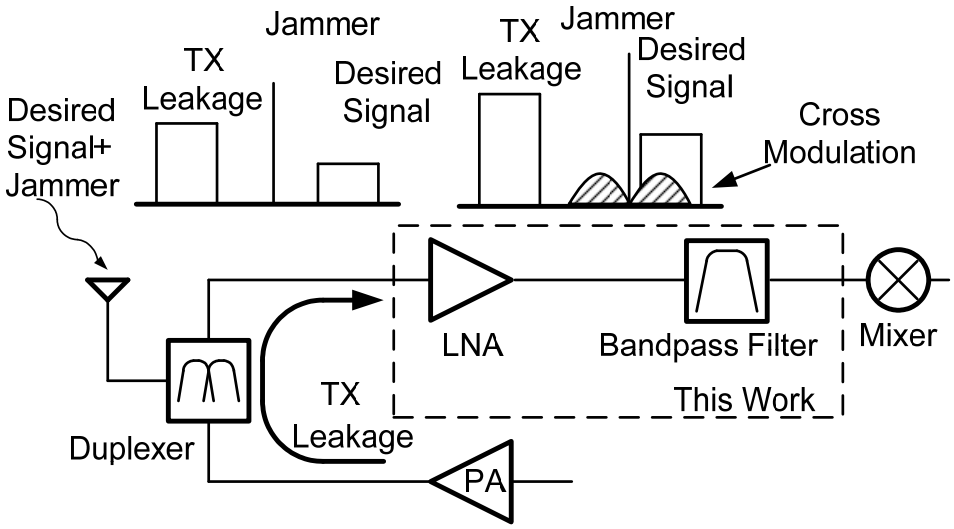


Figure 1.4: Cross-modulation distortion in CDMA receiver schematic [1].

Unlike the second-order distortion, this specification is affected by the LNA linearity. However, a Tx rejection filter can not be placed before the LNA as it can adversely affect the noise performance. Fortunately, CMOS LNAs can be designed for high IIP_3 using either the modified derivative superposition (MDS) method [13] or the active post distortion (APD) method [15]. However, the downconverter can not be designed to handle the strong blocker.

Another motivation for filtering the Tx leakage is to reduce the power consumption of baseband amplifier. In the absence of any filtering, the Tx signal will downconvert to tens of MHz (80 MHz for CDMA2000 and 190 MHz for W-CDMA). This can be 0.5 mA of current at the mixer output. To handle this current, baseband amplifier needs to burn much more power.

Hence, a Tx rejection filter must be placed between the LNA and baseband amplifier.

Triple Beat (TB) Test

The cross-modulation distortion mechanism involves the modulated Tx signal band and a CW blocker. As this test is difficult to conduct in simulation and measurement, another metric called Triple Beat (TB) was introduced. The Tx signal is modeled as two tones within the Tx band, each having half the power of the Tx signal. The triple beat test is conducted with these two tones and the CW tone, with the distortion tone appearing at frequency $f_1 - f_2 + f_3$, where, f_1 is the CW frequency, and, f_2 and f_3 are the Tx tones. The triple beat (TB) metric is defined as the difference between the output power of the CW blocker and the cross-modulation distortion tone. Using power series analysis, it can be shown that the TB is related to the IIP_3 through the relation,

$$IIP_3(\text{ dBm}) = \frac{1}{2}TB(\text{ dB}) + P_{TX}(\text{ dBm}), \tag{1.1}$$

where, P_{TX} is the input power of the modulated Tx signal. Each of the two tones representing Tx has power (P_{TX}-3) dBm.

Specifications for Inter-stage RF Bandpass Filter

Assuming the LNA with a gain of 15 dB and 2 dB noise figure, the filter loss and NF specification should be such that it does not alter the cascaded performance significantly. Assuming the cascaded NF to be 2.2 dB, the NF of the filter can be calculated as using the Friis formula,

$$F_{LNA+BPF} = F_{LNA} + \frac{F_{BPF}}{G_{LNA}}, \tag{1.2}$$

where, F is the noise factor and G is the gain. Thus,

$$\begin{aligned} NF_{BPF} &= 10\log\left(10^{\frac{15}{10}} \times (10^{\frac{2.2}{10}} - 10^{\frac{2}{10}})\right) \\ &= 3.7 \text{ dB}. \end{aligned} \tag{1.3}$$

However, the insertion loss of the filter should not exceed 3 dB in the passband to maintain sufficient gain before the noisy mixer. Both the IIP_2 and cross-modulation (XM) IIP_3 are dependent upon the square of the Tx power. Hence for achieving a 40 dB suppression of the Tx interference, a 20 dB rejection of the Tx signal should suffice.

The IIP_3's of the LNA and the BPF are related by the following expression,

$$\frac{1}{IIP_{3,LNA+BPF}(W)} = \frac{1}{IIP_{3,LNA}(W)} + \frac{G_{LNA}}{IIP_{3,BPF}(W)}. \tag{1.4}$$

Hence,

$$IIP_{3,BPF}(W) = G_{LNA}\Big(\frac{1}{IIP_{3,LNA+BPF}(W)} - \frac{1}{IIP_{3,LNA}(W)}\Big)^{-1} \tag{1.5}$$

For W-CDMA, assuming the LNA IIP_3 to be 0 dBm and the cascaded IIP_3 to be -1 dBm, the BPF IIP_3 can be computed to be +21 dBm. For CDMA, assuming the LNA and the cascaded IIP_3's to be +10 dBm and +8 dBm respectively, the BPF IIP_3 will be +27 dBm. The specifications of the interstage bandpass filter are summarized in Table 1.1.

1.1.2 SAW and F-BAR Filters

The interstage RF filters for Tx leakage rejection are typically implemented using off-chip surface acoustic wave (SAW) filters. These filters typically have 2 dB insertion loss and can provide more than 40 dB suppression in the Tx band. As these

Table 1.1: Specifications for the interstage RF bandpass filter

Parameter	Specification	Unit
Insertion Loss	3	dB
Tx rejection	20	dB
Noise Figure	3.7	dB
IIP_3 (W-CDMA)	+20	dBm
IIP_3 (CDMA)	+27	dBm

are passive filters, the noise figure of the filter is same as the insertion loss. In addition, these devices have high linearity and easily meet the IIP_3 specification. Typically, the interstage filter can be constructed with a single-ended input and differential output. This supports a single-ended LNA, while the differential output feeds a double-balanced mixers. Hence, the filter doubles as a balun.

Surface-acoustic wave (SAW) filters are constructed on a piezoelectric substrate, as shown in Fig. 1.5 [2]. The input signal is fed the input inter-digitized transducer (IDT), which creates the electric waves on the surface of the substrate. The piezoelectric substrate converts these electrical waves in surface bound mechanical waves, hence the name surface acoustic waves. These waves travel across the surface of the substrate and are converted back in the electrical signals through the output IDT. As shown in Fig. 1.5, surface acoustic wave absorbers are placed at the two edges to avoid interference due to the reflecting waves.

The piezoelectric substrate is typically constructed from lithium niobate ($LiNbO_3$). The filter characteristics are dependent upon the crystal cut and the design of the IDT. A small portion of the wave enters the substrate bulk and results in transmission losses. However, for most of the devices the losses are under 0.01 dB per surface wavelength [16].

The frequency response of a commercially available RF filter for W-CDMA using SAW technology is shown in Fig. 1.6 [3]. The filter has an insertion loss of less than 3 dB and achieves more than 40 dB rejection of the Tx signal.

Unfortunately, this amazing technology is based on surface-waves generated on a piezoelectric material which can not be integrated with the rest of the receiver on a silicon substrate. Hence, these filters are packaged separately. These devices are

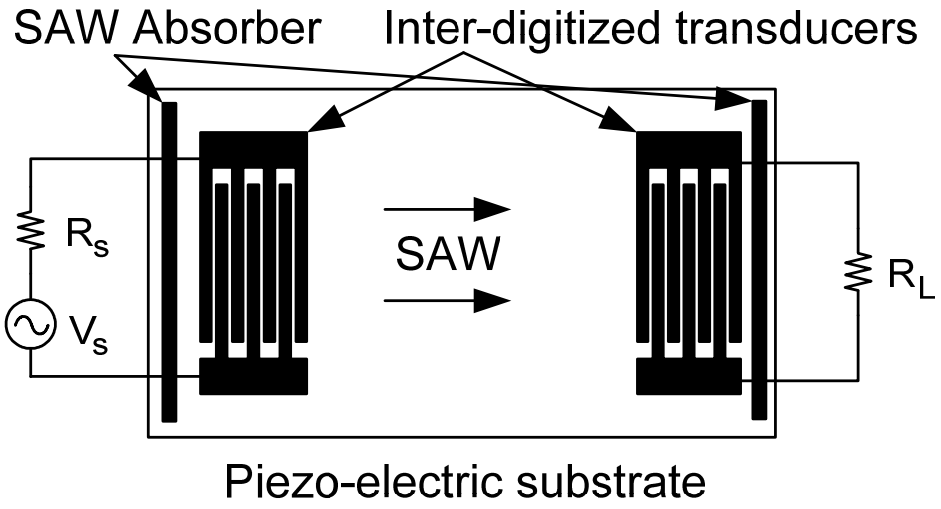


Figure 1.5: Basic surface-wave device [2].

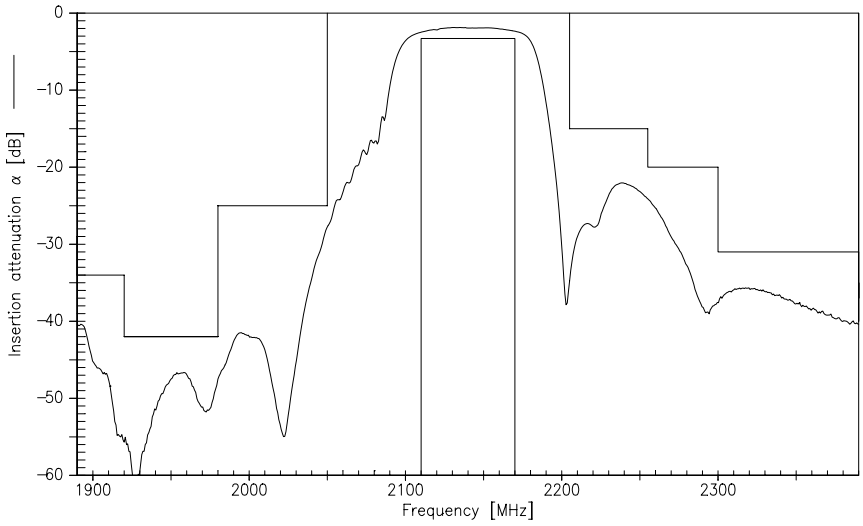


Figure 1.6: Typical frequency response of a SAW interstage RF filter for W-CDMA applications [3].

expensive and come at a cost comparable to that of the entire receiver chip. They have large form factor, and hence, occupy significant printed circuit board (PCB) area. As these are off-chip components, matching networks are required for efficient transfer of RF signal. Due to these numerous disadvantages and expenses, it is desired to find on-chip monolithic solution to this problem.

Recently, thin film bulk acoustic resonators (FBAR) have gained more attention due to their superior Quality factor and smaller form factors as compared to their SAW counterparts [17]. Filter Q of up to 67,000 has been reported [18]. A bulk acoustic resonator is constructed by depositing a layer of piezoelectric layer over the silicon substrate and applying terminals across the piezoelectric layer. The challenges lie in constructing high quality thin films over the silicon substrate which is vulnerable to corrosion and defects due to fabrication processes.

New fabrication techniques using nanotechnology have been reported for creating nanobelts of semiconductor oxides [19]. This can be used to construct thin film of zinc-oxide (ZnO), which is a piezoelectric material, with minimal defects [20, 21]. This has a potential of integrating the FBAR filter on the silicon substrate. Another approach involves creating system-in-package (SiP) by gluing the filter substrate on top of the receiver chip [22].

In a nutshell, either some variation in process technology or system-in-package approach or off-chip component implementation is required to accommodate the SAW or FBAR filter. All of these approaches have considerable cost disadvantages. Hence, a monolithic solution is desired.

1.2 UMTS RF Receiver Specification

Although, the SAW filter provide a 40 dB rejection in the Tx leakage, the receiver linearity specifications can be met with considerably less rejection. In this section, the RF receiver specifications are derived from the user equipment test conditions for a UMTS or W-CDMA standard. Subsequently, the downconverter specifications are derived and their dependence on interstage filter Tx rejection is explored to find an optimum Tx rejection specification for the filter.

Table 1.2: UMTS receiver specifications for W-CDMA 2100 [14].

Parameter	Specification	Units
Uplink frequency band (TX)	1920-1980	MHz
Downlink frequency band (RX)	2110-2170	MHz
Channel Spacing	5	MHz
Chip Rate	3.84	Mcps
Maximum Transmit Power (Class III)	+24	dBm

Table 1.3: WCDMA User Equipment (UE) Tests [14].

Test Signals	Power	Units
In-Band Blocking Test		
Downlink signal, $P_{R,DPCH}$	-114	dBm/3.84MHz
In-band modulated blocker @ $\pm$10 MHz offset	-56	dBm/3.84MHz
In-band modulated blocker @ $\pm$15 MHz offset	-44	dBm/3.84MHz
Out-of-Band Blocking Test		
Downlink signal, $P_{R,DPCH}$	-114	dBm/3.84MHz
Out-of-band CW blocker @ (2050-2095 and 2185-2230) MHz	-44	dBm
Out-of-band CW blocker @ (2025-2050 and 2230-2255) MHz	-30	dBm
Out-of-band CW blocker @ (1-2025 and 2255-12750) MHz	-15	dBm
Intermodulation Test		
Downlink signal, $P_{R,DPCH}$	-114	dBm/3.84MHz
In-band CW blocker @ $\pm$10 MHz offset	-46	dBm
In-band modulated blocker @ $\pm$20 MHz offset	-46	dBm/3.84MHz

1.2.1 UMTS Receiver Test Conditions

UMTS has prescribed several frequency bands for the deployment of the W-CDMA systems as a 3G communication standard. In this work, we have primarily focussed on the "W-CDMA 2100" frequency band, which is widely deployed in Europe, Africa, Asia and parts of America. The uplink and downlink frequency bands and other key receiver specifications are enumerated in Table. 1.2 [14]. 3GPP has formulated numerous test scenarios for characterizing the W-CDMA user equipment (UE). In these tests, the user bit rate is fixed at 12.2 kbps and the bit error rate (BER) should not exceed 0.001. These test conditions furnish the minimum detectable signal power in the

dedicated physical channel (DPCH), $P_{R,DPCH}$ in presence of blockers. A brief summary of the test conditions is presented in Table. 1.3.

1.2.2 UMTS Receiver Intermodulation Specifications

Using the test conditions in Table 1.3, the desired W-CDMA RF receiver specifications can be derived. As we are interested in intermodulation distortion, only specifications related to IIP_3 and IIP_2 are derived here. The user bit rate is 12.2 kbps and signal bandwidth is 3.84 MHz. Hence, the processing gain, G_p, can be computed as [23],

$$\begin{aligned} G_p &= 10\log_{10}\left(\frac{3.84\text{ MHz}}{12.2\text{ kbps}}\right) \\ &= 25\text{ dB}. \end{aligned} \tag{1.6}$$

The minimum signal to noise and distortion ratio, E_b/N_t, for a BER of 0.001 is computed to be 5.2 dB from the simulation [24]. With a practical margin for implementation, we may express the required SNDR as,

$$\left(\frac{E_b}{N_t}\right)_{eff} \approxeq 7\text{ dB}. \tag{1.7}$$

Second-Order Intercept Point

The second-order input intercept point, IIP_2, is a crucial metric in a direct conversion receiver design, because a poor IIP_2 would result in high-frequency modulated blockers being downconverted to baseband. As the TX signal in the RX path is the strongest blocker, even though separated from the RX band, it can land in baseband due to second-order nonlinearity and desensitize the receiver. The IIP_2 specification for W-CDMA can be derived from the in-band and out-of-band blocker tests. For both the cases, the minimum detectable signal power, $P_{R,DPCH}$, -114 dBm. Hence, the total acceptable interference power, $P_{I,total}$, for these tests can be computed as,

$$\begin{aligned} P_{I,total} &= P_{R,DPCH} - \left(\frac{E_b}{N_t}\right)_{eff} + G_p \\ &= -114\text{ dBm} - 7\text{ dB} + 25\text{ dB} \\ &= -96\text{ dBm}. \end{aligned} \tag{1.8}$$

Table 1.4: Typical W-CDMA Duplexer performance.

Parameter	Specification	Units
TX to Antenna insertion loss	2	dB
RX to Antenna insertion loss	2	dB
TX to RX isolation	55	dB
Antenna to RX loss @ 95 MHz offset	30	dB
Antenna to RX loss @ 380 MHz offset	45	dB

For the in-band test, the modulated blocker at $\pm$15 MHz offset has power, $P_{block,15M}$, of -44 dBm, which is much larger than the -56 dBm blocker at $\pm$10 MHz offset. Hence, IIP_2 is computed using the 15 MHz offset blocker. As the desired channel power, $P_{R,DPCH}$, is 3 dB above the sensitivity limit of -117 dBm, 50% of the total interference is contributed from the noise. Assigning 20% to the down-converted blocker and 10% for other out-of-band blockers, the second-order term should not contribute more than 20% (7 dB less). Thus, the maximum distortion power, P_{2dis}, due to this blocker is,

$$\begin{aligned} P_{2dis} &= P_{I,total} - 7 \text{ dB} \\ &= -103 \text{ dBm}. \end{aligned} \tag{1.9}$$

Using this information, IIP_2 due to the 15 MHz blocker can be computed as,

$$\begin{aligned} IIP_2(15M) &= 2P_{block,15M} - P_{2dis} \\ &= 2 \times (-44 \text{ dBm}) - (-103 \text{ dBm}) \\ &= +15 \text{ dBm}. \end{aligned} \tag{1.10}$$

In W-CDMA system, the transmitter and the receiver work simultaneously and are connected to the antenna through a duplexer. A typical W-CDMA duplexer performance is listed in Table. 1.4. 3GPP requires that for power class III, the maximum transmitted power at the antenna should not exceed +24 dBm. Hence, the Tx power at output of power amplifier, $P_{TX,PA}$ will be +26 dBm. With a 55 dB isolation between the TX and RX ports of the duplexer, the TX signal power at LNA input, $P_{TX,LNA}$, would be,

$$\begin{aligned} P_{TX,LNA} &= P_{TX,PA} - Isolation_{TX-RX} \\ &= +26 \text{ dBm} - 55 \text{ dB} \\ &= -29 \text{ dBm}. \end{aligned} \tag{1.11}$$

Table 1.5: WCDMA RF receiver intermodulation specifications.

Parameter	Specification	Units
IIP_2 (TX blocker)	+45	dBm
IIP_3 10MHz/20MHz (in-band)	-17	dBm
IIP_3 95MHz (TX blocker and 95 MHz blocker)	-7.5	dBm
IIP_3 380MHz (TX blocker and 380 MHz blocker)	-7	dBm
IIP_3 XM (TX blocker and 3.5 MHz blocker)	-3	dBm

Hence, IIP_2 requirement for this TX blocker will be,

$$\begin{aligned} IIP_2(TX) &= 2P_{TX,LNA} - P_{2dis} \\ &= 2 \times (-29 \text{ dBm}) - (-103 \text{ dBm}) \\ &= +45 \text{ dBm}. \end{aligned} \tag{1.12}$$

Thus, the overall minimum IIP_2 specification of the W-CDMA receiver is +45 dBm.

Third-Order Intercept Point

The third order intercept point can be computed from the in-band intermodulation tests and the out-of-band blocker tests. For the in-band test, the minimum signal power, $P_{R,DPCH}$, is -114 dBm. The two tones comprise of -46 dBm continuous wave (CW) blocker at 10 MHz offset and -46 dBm modulated blocker at 20 MHz offset. As for the IIP_2 computation, we assign 50% to noise, 15% (-8 dB) to the intermodulation, 20% to the CW blocker at 10 MHz offset, 10% to the modulated blocker at 20 MHz offset and 5% to others. Hence,

$$\begin{aligned} IIP_3(10M/20M) &= \frac{1}{2}(2P_{block,10M} + P_{block,20M} - (P_{I,total} - 8 \text{ dB})) \\ &= \frac{1}{2}(2 \times (-46 \text{ dBm}) + (-46 \text{ dBm}) - (-96 \text{ dBm} - 8 \text{ dB})) \\ &= -17 \text{ dBm}. \end{aligned} \tag{1.13}$$

The TX blocker is at an offset of 190 MHz from the RX channel. This can modulate with a CW blocker at 95 MHz offset to create in-band distortion. This CW blocker has maximum power of -15 dBm which is further attenuated by the duplexer to -45 dBm.

Using these two tones, the IIP_3 can be computed as,

$$\begin{aligned} IIP_3(95M/TX) &= \frac{1}{2}(2P_{block,95M} + P_{TX,LNA} - (P_{I,total} - 8\text{ dB})) \\ &= \frac{1}{2}(2 \times (-45\text{ dBm}) + (-29\text{ dBm}) - (-96\text{ dBm} - 8\text{ dB})) \\ &= -7.5\text{ dBm}. \end{aligned} \tag{1.14}$$

Similarly, the TX blocker can intermodulate with CW blocker at 380 MHz offset to produce in-band distortion. The 380 MHz blocker has power of -15 dBm at antenna and the duplexer attenuates it to -60 dBm at the LNA input. Hence,

$$\begin{aligned} IIP_3(TX/380M) &= \frac{1}{2}(2P_{TX,LNA} + P_{block,380M} - (P_{I,total} - 8\text{ dB})) \\ &= \frac{1}{2}(2 \times (-29\text{ dBm}) + (-60\text{ dBm}) - (-96\text{ dBm} - 8\text{ dB})) \\ &= -7\text{ dBm}. \end{aligned} \tag{1.15}$$

It is also observed that the TX blocker can also cross-modulate (XM) with a close-in blocker to create in-band distortions [1]. To analyze this effect, we can assume the modulated TX blocker to be composed of two tones 3.5 MHz apart with half the power each. This can cross-modulate with a 3.5 MHz blocker with a maximum power of -46 dBm. Hence, the cross-modulate IIP_3 can be computed as,

$$\begin{aligned} IIP_3(XM) &= \frac{1}{2}(2(P_{TX,LNA} - 3\text{ dB}) + P_{block,3.5M} - (P_{I,total} - 8\text{ dB})) \\ &= \frac{1}{2}(2 \times (-29\text{ dBm} - 3\text{ dB}) + (-46\text{ dBm}) - (-96\text{ dBm} - 8\text{ dB})) \\ &= -3\text{ dBm}. \end{aligned} \tag{1.16}$$

Hence, the cross-modulation distortion produces the largest interference and hence, the receiver IIP_3 should exceed -3 dBm for out-of-band test and -17 dBm for in-band test. The in-band IIP_3 is crucial because it imposes linearity constraint on the baseband filter. The out-of-band blockers are knocked off by the first-pole of the baseband filter and hence do not affect the later stages. The IIP_2 and IIP_3 for the various cases have been summarized in Table. 1.5.

Table 1.6: Typical specifications for LNA and proposed interstage bandpass filter in a W-CDMA system.

Parameter	Specification	Units
Low Noise Amplifier (LNA)		
Gain	15	dB
IIP_3	0	dBm
TX selectivity	0	dB
On-chip interstage Bandpass Filter (BPF)		
Selectivity at TX band	10	dB
Gain (RX) ($G_{BPF,RX}$)	-5	dB
Gain (95M) ($G_{BPF,95M}$)	-10	dB
Gain (TX) ($G_{BPF,TX}$)	-15	dB
Gain (380M) ($G_{BPF,380M}$)	-25	dB

1.2.3 Downconverter Intermodulation Specification versus BPF TX Rejection

To compute downconverter intermodulation specifications, we assume the LNA and the BPF specifications as enumerated in Table. 1.6.

Downconverter Second-Order Intercept Point

The maximum allowed interference at the mixer input can be computed by adding the LNA + BPF gain to the $P_{I,total}$. Thus,

$$\begin{aligned} P_{I,total,MIX} &= P_{I,total} + G_{LNA} + G_{BPF,RX} \\ &= -96 \text{ dBm} + 15 \text{ dB} - 5 \text{ dB} \\ &= -86 \text{ dBm}. \end{aligned} \tag{1.17}$$

There is no second-order distortion due to the LNA, because, it is blocked by the AC coupling capacitor between the LNA and the BPF. The TX power at the mixer input can be calculated as,

$$\begin{aligned} P_{TX,MIX} &= P_{TX,LNA} + G_{LNA} + G_{BPF,TX} \\ &= -29 \text{ dBm} + 15 \text{ dB} - 15 \text{ dB} \\ &= -29 \text{ dBm} \end{aligned} \tag{1.18}$$

Using a similar signal budget as earlier, the downconverter IIP_2 is,

$$\begin{aligned} IIP_{2,MIX} &= (2P_{TX,MIX} - P_{I,total,MIX}) \\ &= 2 \times (-29 \text{ dBm}) - (-86 \text{ dBm} - 7 \text{ dB}) \\ &= +35 \text{ dBm} \end{aligned} \tag{1.19}$$

Downconverter Third-Order Intercept Point

The mixer IIP_3 due to the cross-modulation distortion (XMD) can be computed in a similar fashion. Noting that the third-order distortion comprises of only 15% of the total interference, the maximum allowed third-order interference power at the mixer input can be computed as,

$$\begin{aligned} P_{3dis@MIX} &= (P_{I,total} - 8 \text{ dB}) + G_{LNA} + G_{BPF,RX} \\ &= (-96 \text{ dBm} - 8 \text{ dB}) + 15 \text{ dB} - 5 \text{ dB} \\ &= -94 \text{ dBm}. \end{aligned} \tag{1.20}$$

However, the distortion contributed by the LNA must be excluded from this power. At the LNA input, the third-order distortion due to the TX blocker and 3.5 MHz offset CW blocker can be computed as,

$$\begin{aligned} P_{3dis,LNA@LNA} &= (2(P_{TX,LNA} - 3 \text{ dB}) + P_{block,3.5M} - 2IIP_{3,LNA} \\ &= (2 \times (-29 \text{ dBm} - 3 \text{ dB}) + (-46 \text{ dBm}) - (2 \times 0 \text{ dBm}) \\ &= -110 \text{ dBm}. \end{aligned} \tag{1.21}$$

At the downconverter output, this power would amplify to,

$$\begin{aligned} P_{3dis,LNA@MIX} &= P_{3dis,LNA@LNA} + G_{LNA} + G_{BPF,RX} \\ &= -110 \text{ dBm} + 15 \text{ dB} - 5 \text{ dB} \\ &= -100 \text{ dBm}. \end{aligned} \tag{1.22}$$

To find the maximum third-order interference contribution, $P_{3dis,LNA@MIX}$ should be subtracted from $P_{3dis@MIX}$ in the voltage domain, as both the powers are contributed by

Table 1.7: WCDMA downconverter linearity specification for different interstage BPF TX selectivities.

BPF Selectivity	0 dB	10 dB	20 dB	Units
IIP_2	+55	+35	+15	dBm
IIP_3 (95M/TX)	+3.4	-6.7	-16.7	dBm
IIP_3 (TX/380M)	+4	-16	-36	dBm
IIP_3 (XM)	+10	0	-10	dBm

the same signal. Hence,

$$\begin{aligned} P_{3dis,MIX@MIX} &= 20\log_{10}\left(10^{\frac{P_{3dis@MIX}}{20}} - 10^{\frac{P_{3dis,LNA@MIX}}{20}}\right) \\ &= 20\log_{10}\left(10^{\frac{-94}{20}} - 10^{\frac{-100}{20}}\right) \\ &= -100 \text{ dBm}. \end{aligned} \tag{1.23}$$

As the BPF can not suppress the close-in blocker at 3.5 MHz, the blocker power at the mixer input is,

$$\begin{aligned} P_{block,3.5M@MIX} &= P_{block,3.5M} + G_{LNA} + G_{BPF,RX} \\ &= -46 \text{ dBm} + 15 \text{ dB} - 5 \text{ dB} \\ &= -36 \text{ dBm}. \end{aligned} \tag{1.24}$$

Hence, the downconverter cross-modulation IIP_3 specification is,

$$\begin{aligned} IIP_{3,MIX}(XM) &= \frac{1}{2}(2(P_{TX,MIX} - 3 \text{ dB}) + P_{block,3.5M@MIX} - P_{3dis,MIX@MIX}) \\ &= \frac{1}{2}(2 \times (-29 \text{ dBm} - 3 \text{ dB}) + (-36 \text{ dBm}) - (-100 \text{ dBm})) \\ &= 0 \text{ dBm}. \end{aligned} \tag{1.25}$$

In a similar fashion, the downconverter IIP_3 for (95 MHz, TX) and (TX, 190 MHz) blockers can be calculated to be -6.7 dBm and -16 dBm respectively. Fig. 1.7 shows the reduction in the downconverter linearity specifications as the interstage bandpass filter TX selectivity increases. For specific TX selectivities of 0 dB, 10 dB and 20 dB, the mixer IIP_2 and IIP_3 are enumerated in Table. 1.7.

It is quite challenging to design a downconverter with +55 dBm IIP_2 and +10 dBm IIP_3, but may be achieved at the expense of higher dc power. In addition, without

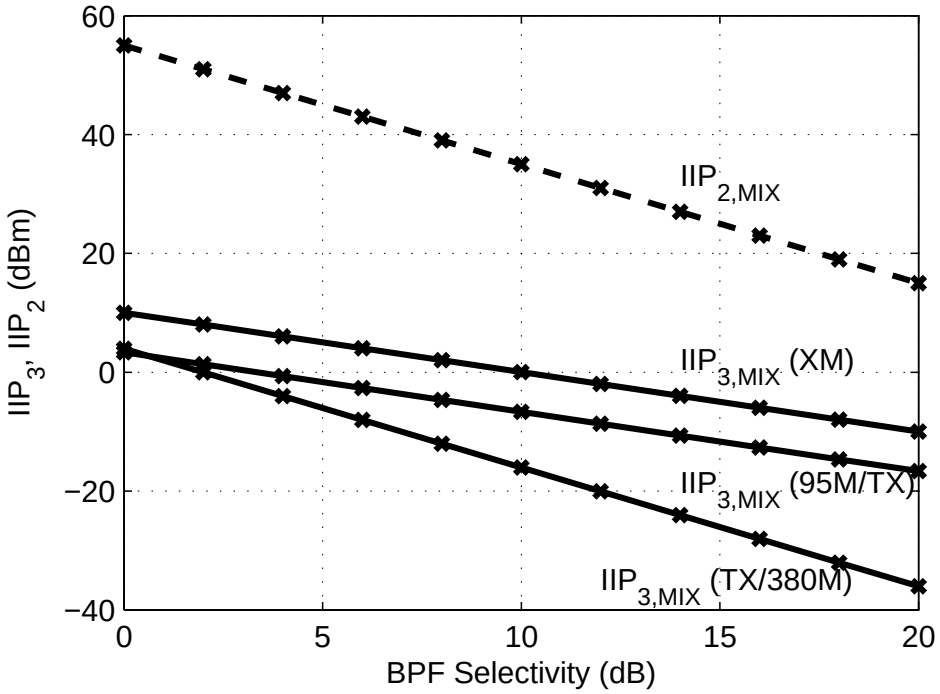


Figure 1.7: Variation in mixer cross-modulation distortion (XMD) IIP_3, two tone IIP_3 and IIP_2 with RX-TX suppression for LNA gains of 12dB and 10dB.

the interstage bandpass filter, the baseband filter must accommodate the unfiltered TX signal, which is amplified and downconverted by the mixer. At the same time, it is overkill to design on-chip filter for 20 dB TX selectivity which drastically relaxes the mixer linearity specifications. A 10 dB RX-TX selectivity in the interstage filter can relax the mixer IIP_2 and IIP3 specifications by 20 dB and 10 dB respectively. So, even a modest filter selectivity can result in substantial easing of the downconverter linearity requirements.

1.3 Active Filtering Techniques

1.3.1 Active LC Filters

Active-RC and Gm-C filters are not suitable for RF applications because of their very high f_t requirements and power consumption, apart from poor noise and linearity performances. LC filters are promising candidates as they have no power consumption.

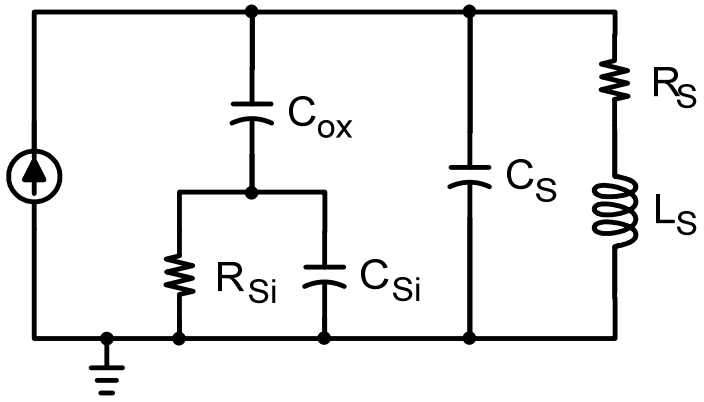


Figure 1.8: Lumped physical model of a spiral inductor in a silicon process [4].

However, the on-chip inductors are quite lossy.

On-chip Inductors

The Quality factor of any energy storing element (inductor or capacitor) is defined as,

$$Q = 2\pi . \frac{\text{Energy Stored}}{\text{Energy lost in one oscillation cycle}}. \tag{1.26}$$

This implies that for improving the Quality factor of an inductor, the magnetic fields should be strong to store more energy, while any energy radiation or dissipation should be minimized. A lumped physical model of a spiral inductor in a silicon process is shown in Fig. 1.8. Here, L_s is the series inductance, while, R_s is the series resistance which is attributed to the ohmic loss, radiation loss and substrate losses in the inductor. The series feed-forward capacitance, C_s, is attributed to the fringing capacitance between the inductor arms and any underpass overlap capacitance. A larger C_s is responsible for a lower self-resonance frequency of a spiral inductor.

The magnetic fields of a spiral inductor span the space above and below the inductor plane. As the magnetic fields tend to concentrate more in the materials with high electrical permittivity, the fields mostly lie in the silicon dioxide layer (ϵ_r=3.9) and the underlying silicon substrate (ϵ_r=11.9). As the silicon substrate is doped, it has low sheet resistance, R_{si}, which leads to substrate losses. Clearly, the Q-factor of a spiral

inductor degrades with its area, its proximity to the substrate and the sheet resistance of the substrate. At 1-2 GHz operation, the radiation losses are negligible and the ohmic resistance can be reduced by choosing the thickest metal layer. Hence, substrate losses should be reduced for improving the Q-factor.

The substrate losses can be reduced by placing a ground metal shield below the inductor on a lower metal layer [25, 26]. However, eddy currents are generated on the metal shield and the magnetic fields created by these currents tend to diminish the magnetic fields of the spiral inductor, lowering its Q-factor. This problem can be addressed by using a patterned ground plane on the poly-silicon layer. The ground plane reduces the substrate effect, while, the patterning inhibits the eddy currents. Using this technique, a 33% improvement in inductor Q-factor and 100% improvement in LC tank Q-factor has been reported for 1-2 GHz frequency range [27].

However, despite these amendments, the Quality factors of typical inductors lie between 10-20. Whereas, for high-Q LC filters with low insertion losses a Q-factor of 50-100 is desired.

Active LC Filters

Fig. 1.9 shows an LC tank with the lossy inductor modeled as an ideal inductor in series with a resistance. The effect of the resistance, R_s, can be canceled by a negative resistance cell in parallel with the tank as shown in Fig. 1.9. The negative resistance cell is typically constructed with two identical cross-coupled transistors as shown in Fig. 1.10. If g_m is the transconductance of each transistor, then the resistance of the block, R, is given by,

$$R = -\frac{2}{g_m}. \tag{1.27}$$

As the negative resistance can be controlled through the bias current of the circuit, the Quality factor of the tank can be considerably improved. Using this technique, several inter-stage RF filters have been implemented, which meet the frequency response specifications [28, 29].

However, apart from the power consumption, all of these implementations have

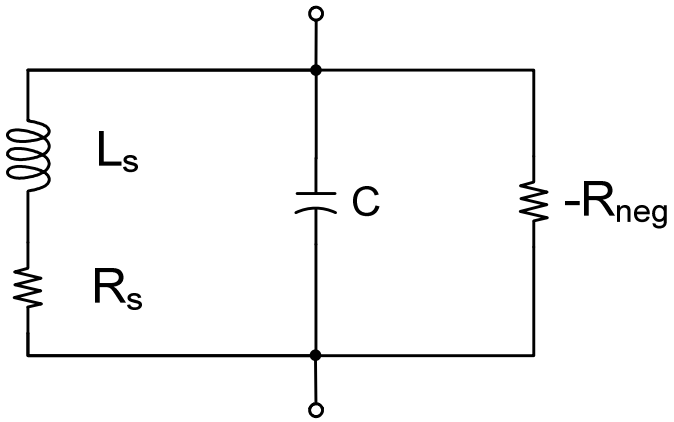


Figure 1.9: Simplified schematic of an LC tank with lossy inductor and negative resistance for Q-enhancement.

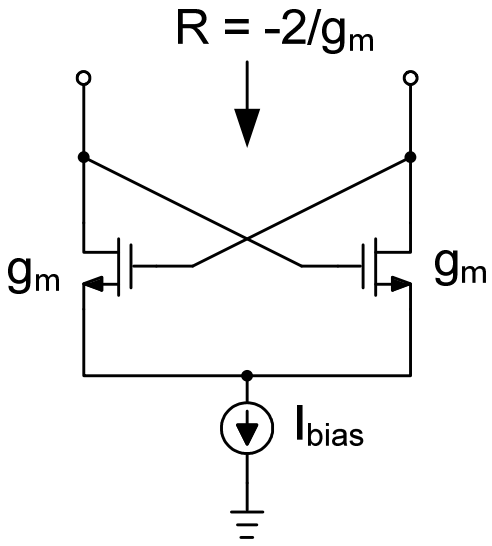


Figure 1.10: Simplified schematic of a negative resistance cell.

Table 1.8: Performance of active LC filters.

	Freq	Q	Power	P_{1-dB}	NF	Area	Process
Units	GHz		mW	dBm	dB	mm^2	
[30]	1.825	3-350	26.1	-18	36	0.38	Bipolar 0.8μm
[31]	1.035	5-180	11.4-15.5	-13	n/a	0.62	CMOS 0.35μm
[32]	2.06	20-170	5.2	-30	26.8	0.10	CMOS 0.35μm
[33]	0.84	n/a	207.9	-18	21	2	CMOS 0.60μm
[34]	0.994	4-400	68	-15.67	37	0.60	Bipolar 0.5μm
[29]a	1.882	n/a	49-60	-11.5	18	7.14	SiGe BiCMOS 0.25μm
[29]b	1.7	n/a	60-74	-6.9	33	6.44	SiGe BiCMOS 0.5μm
[28]	2.14	35.67	17.5	-13.4	19	2	CMOS 0.25μm

dismal noise and linearity performance. It has been shown that the Q-enhancement techniques are responsible for noise amplification. In general, the output noise voltage, $v_{n,out}^2$, can be expressed as

$$v_{n,out}^2 = 2\frac{kT}{C}\frac{Q}{Q_0}F, \tag{1.28}$$

where, k is the Boltzmann constant, Q is the enhanced Q-factor of the inductor, Q_0 is the original Q-factor of the inductor and F is the noise factor of the amplifier [30]. Equation (1.28) implies that the better the Q-factor, worse the noise figure.

An active implementation also suffers from linearity degradation. If V_{comp} is the 1-dB compression point of the amplifier shown in Fig. 1.10, the output dynamic range of the LC block is given by [30],

$$DR_{out} = \left(\frac{Q_0}{Q}\right)^2 \frac{V_{comp}^2}{2\frac{kT}{C}F}. \tag{1.29}$$

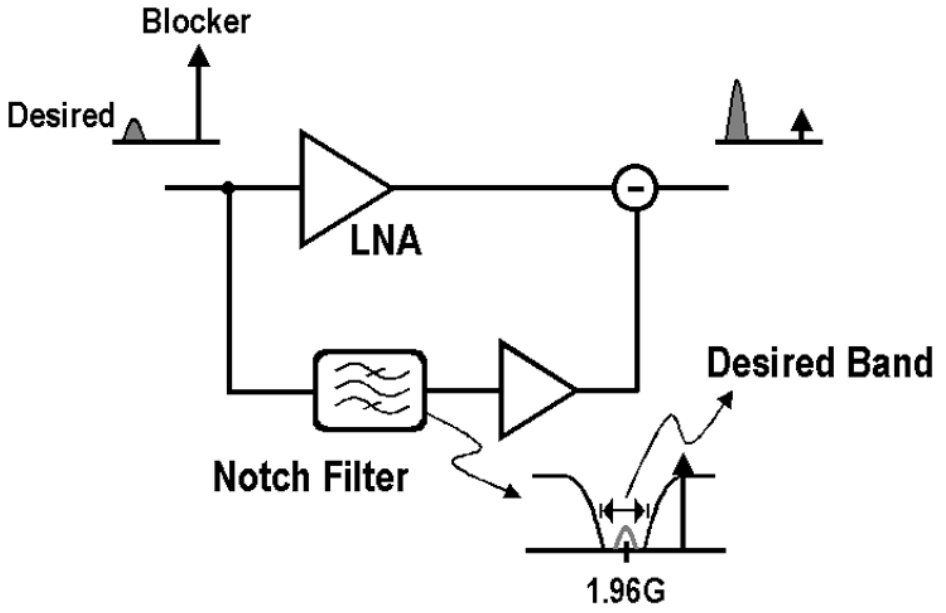
Evidently, as the Q increases, the linearity of the tank drops. This problem can be partly addressed by improving the amplifier linearity, albeit at an expense of higher power consumption. Table 1.8 summarizes the active LC filter implementations using Q-enhancement techniques. It is evident that all of them have poor noise figure and linearity performance. Consequently, they fail to meet the specification of a W-CDMA or CDMA receiver.

1.3.2 Feed-forward Filtering Technique

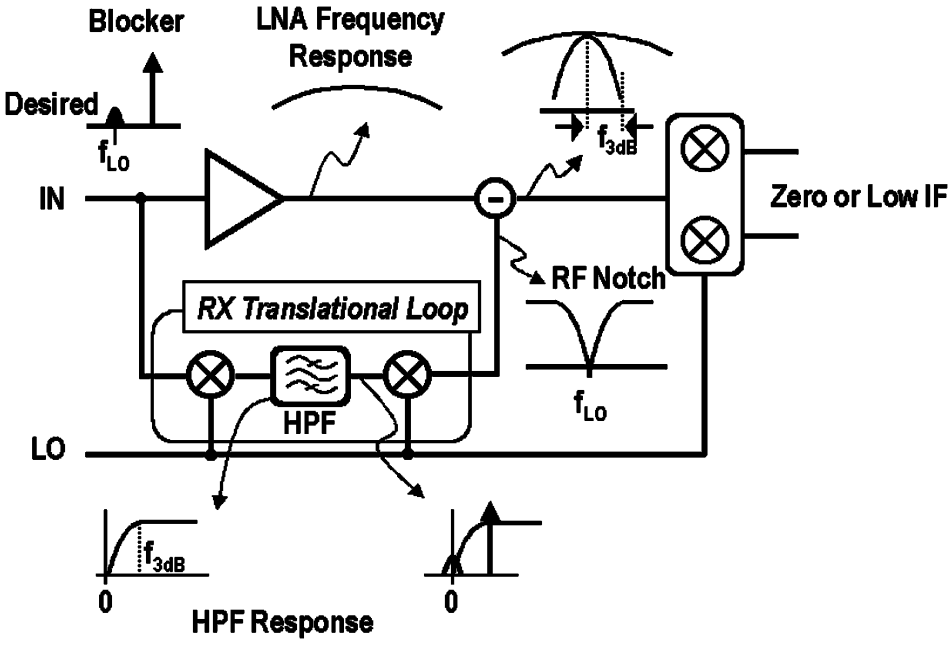
Several active feed-forward techniques have been proposed to eliminate the TX signal before hitting the downconverter. In the blocker filtering technique proposed by Darabi [5], the feed-forward path is comprised of a notch filter centered around the Rx band and cascaded with an amplifier, as shown in Fig. 1.11(a). This notch filter forces the desired signal through the LNA, while filters away a portion of the Tx blocker, which is subsequently amplified and added to the signal path after the LNA. The feed-forward path is designed such that the Tx signals cancel. The most challenging part is a high-Q notch filter design at the RF frequency, which is achieved by an RX transitional loop (Fig. 1.11(b), where the signal is first downconverted using the Rx LO. A high-Q baseband high-pass filter reflects back the downconverted signal, while it passes the undesired Tx signal through this feed-forward path. Subsequently, this filtered signal, which primarily consists of the downconverted Tx signal, is upconverted back to the RF domain using the same Rx LO. A careful design with accurate gain and minimal group delay is desired so that the signal through the feed-forward path can exactly cancel out the Tx signal from the main path.

A very similar methodology was proposed by Ayazian et. al [6], the high-pass filter in the auxiliary path comprised of a baseband amplifier sandwiched between two passive high-pass filter, as shown in Fig. 1.12.

Aparin et. al [7] proposed the adaptive least mean square (LMS) filter technique. As shown in Fig. 1.13, this technique takes advantage of the fact that the Tx and Rx circuits resides on the same chip. Instead of creating an auxiliary path in Rx path, which leads to a signal degradation and noise figure penalty, the Tx signal is sensed through the Tx path itself. This signal coupled from the output of the power amplifier (PA) is split in quadrature. Each of the quadrature signals are then multiplied by the output signal of the LNA in a feedback mechanism. This product signal is then integrated over the signal duration to create a matched filter with the output of the integrator being an estimate of the Tx signal power. The sensed Tx signal is scaled by this estimate so that it matches



(a)



(b)

Figure 1.11: (a) Feed-forward cancellation technique [5], (b) Feed-forward cancellation with notch filter implemented using receiver translational loop [5].

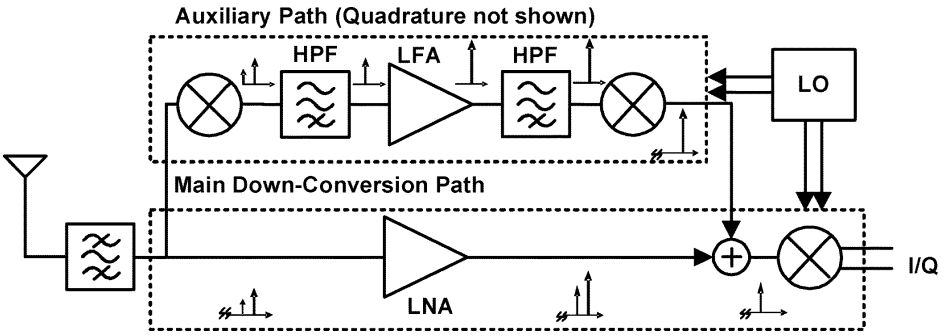


Figure 1.12: Another implementation of feed-forward interference cancellation [6].

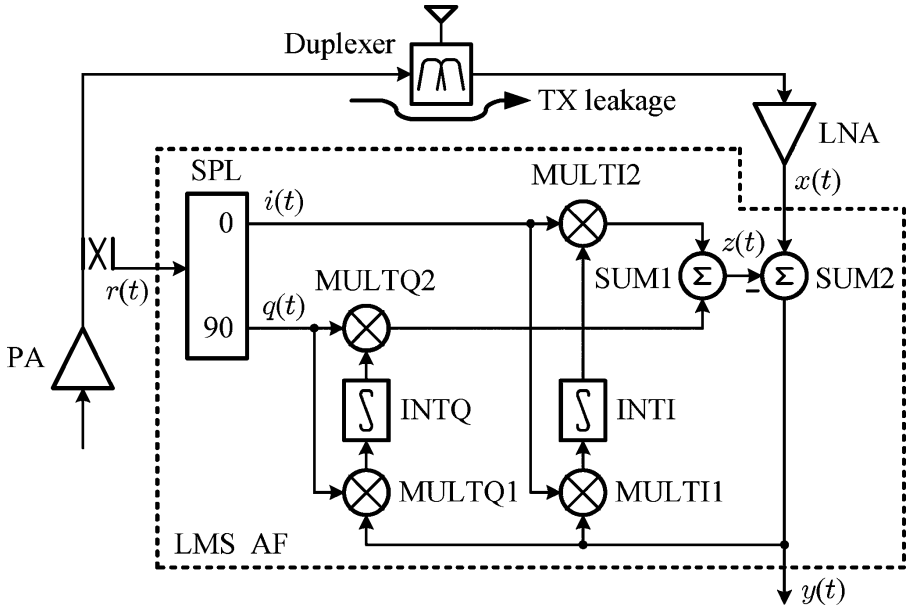


Figure 1.13: Adaptive LMS filtering technique [7].

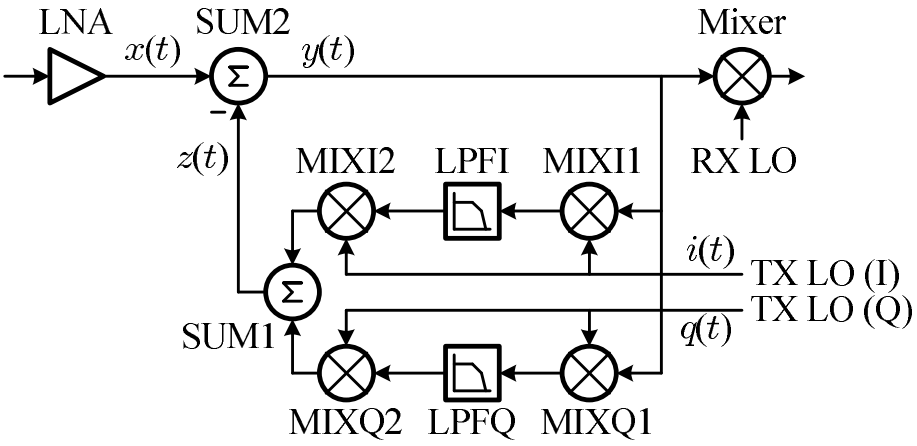


Figure 1.14: Modified LMS filtering technique using low-pass filters [8].

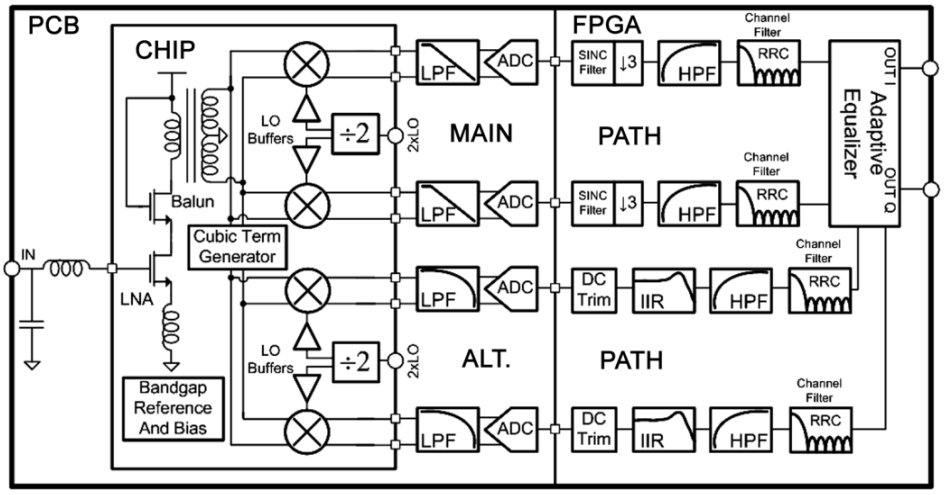


Figure 1.15: Feed-forward equalization. The third-order term is tapped after the LNA and equalization is done after downconversion using LMS algorithm [9].

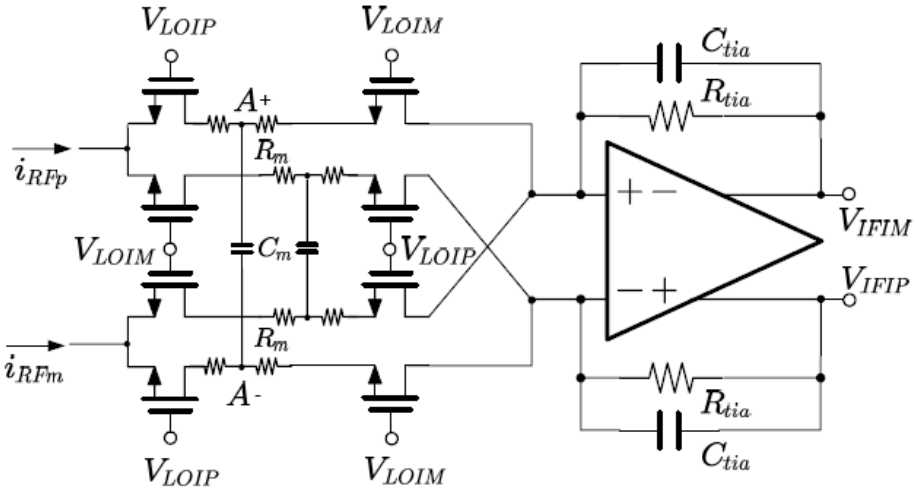


Figure 1.16: Simplified schematic of embedded filtering passive mixer [10].

the Tx signal in the Rx path and negatively fed back in the Rx path for cancellation. A similar approach is also presented in [8]. Here instead of the integrators, low-pass filters are used and the Tx LO is used as the reference signal (Fig. 1.14).

Another related approach was proposed by Keehr and Hajimiri for W-CDMA receivers at 2.1 GHz [9]. The LNA output is tapped into a third-order generator which feeds an auxiliary downconverter. The main and auxiliary downconverters are identical and provide separate in-phase and quadrature-phase outputs. These outputs are then fed into a complex digital equalizer, which is based on least-mean square (LMS) algorithm. The filtering and equalization was implemented in a separate digital FPGA chip as shown in Fig. 1.15. This work reports an improvement of out-of-band IIP_3 in excess of 12 dB, while the noise figure of the receiver was 5.5 dB. The drawbacks of the scheme are the area and power penalty for having two separate I and Q downconverters.

Recently Kim et. al [10] have proposed another technique which relies on filtering the Tx signal inside the downconverter rather than canceling it. This has the advantage of simplicity and robustness and does not require a precise feed-forward or feed-back path. The high linearity is achieved through an embedded filter passive mixer. The proposed mixer schematic is shown in Fig. 1.16. The signal downconversion is achieved in two-stages. The mixer employs a 50% duty-cycle LO signal. As shown in

Fig. 1.16, the first mixer acts as a current-commutating mixer and downconverts the signal to charge the capacitor. As the Tx signal is downconverted to a lower frequency (45 MHz for cellular band and 80 MHz for PCS band), it gets filtered due to the low-pass filter between the two mixers. Subsequently, in the next half cycle the second downconverter feed this charge stored on the capacitor to the trans-impedance amplifier (TIA).

1.4 Dissertation Focus

Several approaches for eliminating the RF interstage SAW filter were enumerated in this chapter. These techniques can be categorized into three broad categories:

– Replacing the SAW filter with an on-chip filter.

– Canceling Tx signal after LNA using feed-forward or feedback techniques.

– Filtering the Tx signal in the downconverter.

In this dissertation, the first and the third approaches have been investigated. The first half deals with approaching the problem from a passive filter implementation. Passive filters using bondwire inductors were constructed and studied. The later half focuses on an active approach. The root cause of mixer nonlinearity is established using Volterra series analysis. A novel active filtering technique is proposed for rejecting the Tx leakage after downconversion.

Chapter 2 deals with design techniques are presented for the realization of high performance integrated interference suppression filters using bond-wire inductors. A new configuration is proposed for mitigating the impact of mutual coupling between the bond-wires. A differential low-noise amplifier with an integrated on-chip passive interference suppression filter is designed at 2.1 GHz in a 0.18 μm CMOS process, and achieves a transmit leakage suppression of 10 dB at 190 MHz offset. The differential filter uses MIM capacitors and bond-wire inductors and occupies only 0.22 mm^2. The cascaded system achieves a measured gain of 9.5 dB with 1.6 dB NF and -5 dBm out-of-band IIP$_3$ and consumes 11 mA from 2 V supply.

Chapter 3 analyzes the effect of various models on a CMOS passive mixer linearity. In some models, the discontinuity in the second-order derivative of the drain-current leads to an erroneous slope of 2:1 for the third-order distortion. The mechanism behind

this 2:1 slope was precisely identified. A passive mixer was measured to confirm the slope of 3:1 for IMD_3, and excellent agreement between theory and measurement was obtained.

Chapter 4 focuses on analysis of CMOS passive mixer linearity using Volterra series analysis. Closed-form expressions for IIP_2, two-tone IIP_3, and, cross-modulation IIP_3 have been presented, exhibiting dependence upon the mixer source and load impedances. Design guidelines are suggested for improving the mixer linearity performance. Accurate expressions are presented for the input impedance of an ideal passive mixer with an arbitrary load impedance. The calculations are in close agreement with the measured results and the simulated response.

Chapter 5 involves design and implementation of a CDMA receiver in 0.18 μm CMOS technology. A new technique for eliminating the interstage SAW filter was presented. The receiver nonlinearity is attributed to the voltage swing at the output of the mixer due to the downconverted Tx signal. This problem was solved by sinking the Tx signal through an auxiliary path, which comprised of another downconverting passive CMOS mixer cascaded with a transimpedance amplifier. This mixer further downconverts the Tx signal to low frequency which is filtered by the TIA.

Three tone triple-beat (TB) test is used to characterize the cross-modulation linearity of the receiver. The proposed technique improved the TB performance by 6.5 dB, while the IIP_2 was also improved by 6.5 dB. The auxiliary path has no significant impact on the receiver gain and close-in IIP_3. However, the NF performance is degraded by 1.7 dB, which is attributed to the auxiliary mixer which folds the auxiliary TIA noise back into the signal path.

Chapter 2

RF Bandpass Filter Using Bondwire Inductors

In most frequency-division duplexed (FDD) wireless communication systems, like CDMA and WCDMA, the antenna is shared between the receiver and the transmitter through a duplexer filter. Despite the isolation provided by the duplexer, the transmitted signal appears as the strongest jammer in the receiver and creates cross-modulation distortion (XMD) which degrades the performance of the overall receiver. This often necessitates the use of an interstage RF filter, after the LNA, as shown in Fig. 2.1 [1]. Such a situation may also arise in multi-band receivers, with the transmitter of one band interfering with all the receivers.

Traditionally, on-board ceramic filters were the mainstay for RF filters in this application. Subsequently, they were replaced by surface acoustic wave (SAW) filters, which occupy lower volume [35]. Recently, thin film bulk acoustic resonator (FBAR) filters have gained much attention due to their smaller form factors, better power handling capabilities and temperature insensitivity. They provide excellent performance; for instance, filters centered at several GHz having less than 1% fractional bandwidth can be easily constructed with an insertion loss of approximately 3dB and very high roll-off [36]. Owing to this, the SAW and FBAR filters are extensively used as duplexers and band-select filters. However, these filters are fabricated on piezoelectric materials like $LiNbO_3$ or $LiTaO_3$, which cannot be easily integrated with active circuits. Hence, they are typically packaged separately and occupy additional board area.

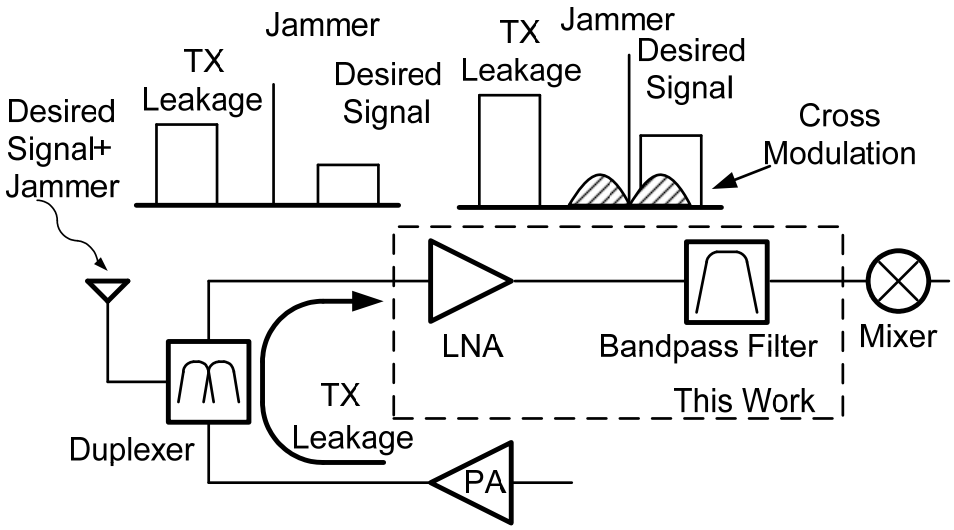


Figure 2.1: Cross-modulation in WCDMA systems [1].

In order to overcome this problem, a SAW filter has been successfully stacked on a transceiver chip [22], while an FBAR filter has been integrated at the wafer level [37]. Nevertheless, apart from additional matching networks, these integrations require expensive special masks and extra processing steps; a less expensive on-chip solution is desired.

Unlike the duplexers or other high selectivity filters, the interstage filters for cellular applications may not require very high roll-off. Fig. 2.2 shows the relaxation in a typical receiver's linearity specifications as a function of the interstage bandpass filter suppression. For example, a 10dB reduction in transmitter leakage can reduce the IIP_3 requirement by 15dB. Therefore, with recent advances in LNA and mixer design, overall receiver specifications can still be satisfied with an on-chip filter with modest suppression as compared to an FBAR filter. However, low noise figure and excellent linearity are still required.

Numerous attempts have been made to integrate interstage RF filters. For high-frequency operations, doubly terminated ladder filter topologies are preferred for their low sensitivities to filter elements [38]. At several GHz, constructing a narrow band (1% fractional bandwidth) bandpass filter employing active-RC or Gm-C blocks is quite

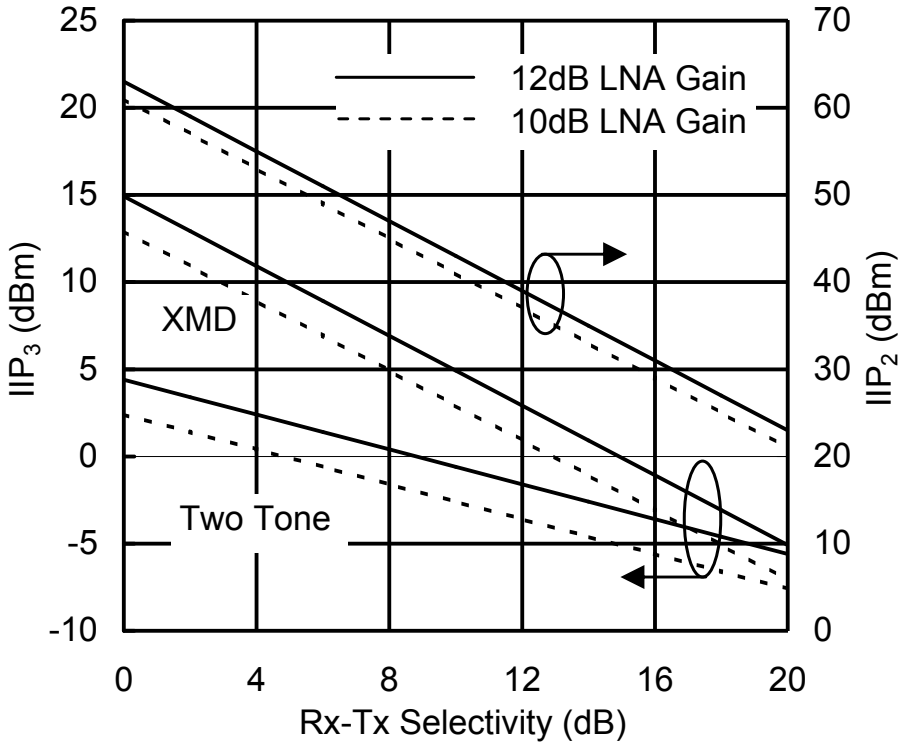


Figure 2.2: Variation in required mixer cross-modulation distortion (XMD) IIP_3, two tone IIP_3 and IIP_2 against RX-TX suppression of the inter-stage BPF, for LNA gains of 12dB and 10dB in a typical WCDMA system.

challenging, due to the resulting dc power and f_T requirements [39]. In addition, the resistors and the transistors of the active circuit add noise and nonlinearity to the circuit. A *passive* LC ladder filter is a viable option as it is not constrained by the dc power or transistor f_T.

For narrowband bandpass filters, the inductors and the capacitors of the LC filter should have a high Q-factor to maintain a low insertion loss. On-chip MIM capacitors with a Q-factor of 95 have been reported [40]. However, on-chip spiral inductors suffer from high parasitic resistance and capacitance. Despite this, monolithic LC filters have been constructed using Q-enhancement techniques [39, 28, 41, 42, 32, 43, 44]. All of these implementations occupy significant area and suffer from poor noise figure ($\geq$18 dB) and high nonlinearity (i.e., P_{1dBm} = -13.4 dBm with 17.5 mW power consumption at 2.14 GHz [28]).

Hence, there is a need to investigate alternative methods of high Q inductor implementations, which can be easily integrated and occupy a small die area. One such alternative is the use of bond-wires, which are known to be inductive in nature. Typically, the inductance of grounded down-bond-wires is in the sub-nH range. LC ladder filters centered at several gigahertz have similar inductor values and hence are amenable for implementation using bond-wires. Compared to on-chip spiral inductors, bond-wires enjoy high Quality Factors, and Q-factors in excess of 50 have been reported [45, 46].

In this chapter, a three-pole differential bandpass filter at 2.14 GHz using bond-wire inductors is presented. Section 2.1 gives the topology of a bandpass filter geared toward implementation using on-chip capacitors and bond-wire inductors. Section 2.2 summarizes the electrical characteristics of the bond-wire and discusses the bond-wire parasitics – resistance and mutual coupling, and their impact on the filter response. Impact of process variations and tuning options are also discussed in this section. A novel bond-wire configuration is proposed to address the parasitic mutual coupling between the bond-wires in Section 2.3. The LNA/filter combination determines the overall front-end performance. Such a cascaded system for WCDMA is also designed as a proof of concept in Section 2.3. Subsequent sections discuss the measurement results and discussions.

2.1 Topology for Bond-Wire Based Bandpass Filters

An LC bandpass ladder filter is typically constructed from low-pass prototypes, whose element values are tabulated in classical texts [47]. The top-C coupled resonator topology shown in Fig. 2.3(a) has minimum number of inductors, all terminating to the ground. This structure also has a narrow spread of the component values for high-Q bandpass filters [48]. The topology in Fig. 2.3(a) offers an opportunity to realize all of the inductors for the filter using equal-valued grounded bond-wires. Thus, it removes any need for an on-chip spiral inductor or a bond-wire stitched across two pads to realize a series inductor [49]. This has a potential to save tremendous area for on-chip implementations.

However, the practicality of a single-ended implementation of the filter is marred by several factors. The shunt capacitors are terminated to the same ground as the inductors. This is challenging in practice, since grounding the capacitors by separate bond-wires requires additional bond pads and the resulting $L_{BW}C$ series combination will alter the capacitor branch susceptance. The filter can still be implemented by scaling the capacitor values [50], but the resulting series resonators create additional attenuation poles. Another solution can be to connect the shunt capacitors together to a common grounded bond-wire. This will have an effect of coupling the resonators together, and provide alternate transmission paths creating unintended attenuation poles.

The common package inductance, which connects the package ground plane to the system ground is a non-negligible fraction of the bond-wire inductance, and can further alter the filter response. Depending on the component values, these parasitics can create attenuation poles, which may appear close to the pass-band resulting in serious degradation of the insertion loss.

A differential filter implementation (Fig. 2.3(b)) overcomes these problems, since there is no need for a common ground node, and the package parasitics appear as common-mode components. Unlike other circuits, where a differential implementation requires twice the die area of a single-ended version, the on-chip area requirement in this case is approximately halved, since the coupling capacitors (C_0) are comparatively smaller than the shunt capacitors ($C_a/C_0 = (1/\sqrt{2}).(1/fractional\ bandwidth) - 1$),

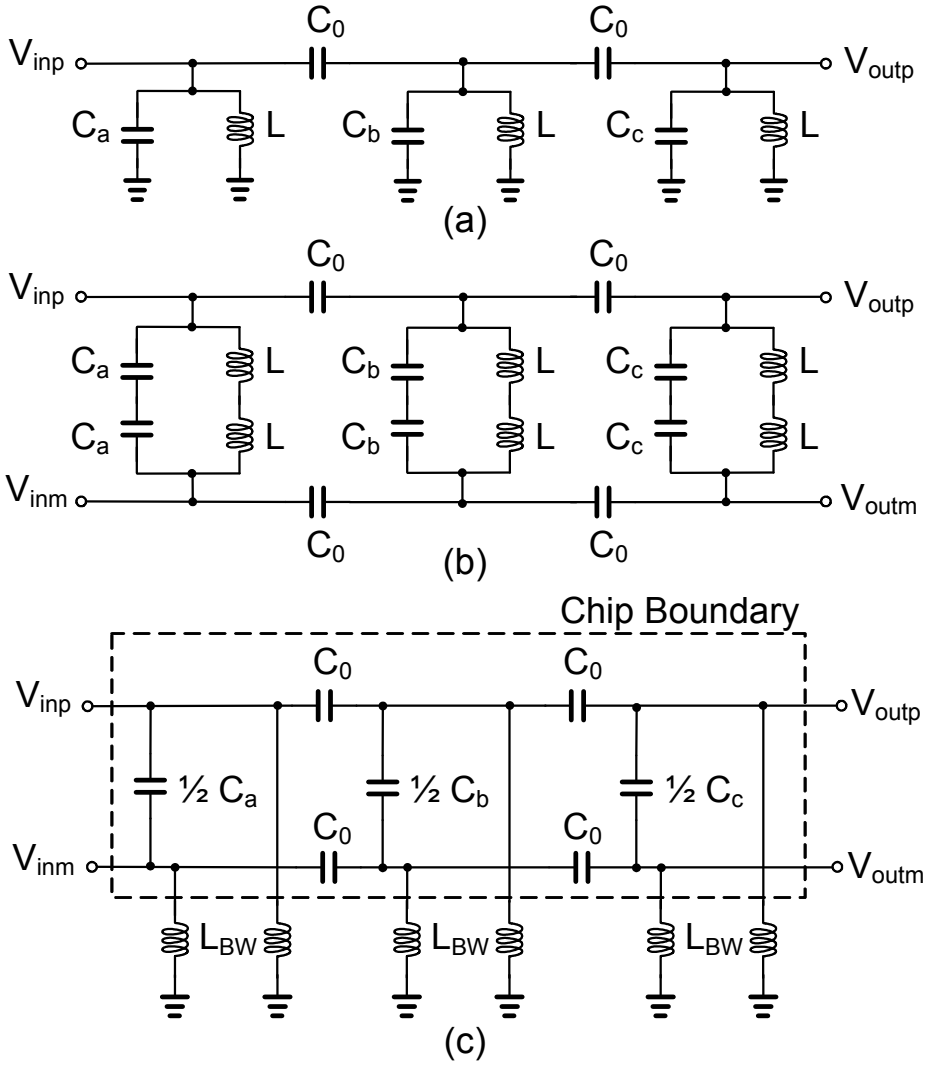


Figure 2.3: (a) Differential filter (b) Pseudo-differential filter with equal-value bondwires as inductor replacements.

for a third-order equiripple filter) and the shunt capacitor values can be halved because of the differential-mode operation. For ease of implementation, it is preferable to terminate the inductors to ground. Hence, a pseudo-differential filter (Fig. 2.3(b)) is chosen, where the shunt capacitors are merged together, but the inductors are separately terminated to ground. This configuration will affect the even-mode response of the filter, which will be discussed in Section 2.2.

Bond-wires have finite Quality factors which leads to insertion losses in the filter. Apart from parasitic resistance, closely placed bond-wire inductors have non-negligible mutual inductive coupling. The filter response is significantly altered by the mutual inductances between the bond-wires, and this effect must be carefully considered for accurate filter design. Fig. 2.4 shows one example of this effect: the simulated transmission and input reflection characteristics of a Butterworth third-order filter in the presence and the absence of mutual inductance. For the sake of simplicity, a constant coefficient of mutual inductance (k) is assumed and higher order mutual inductances are ignored. In this case, the mutual inductance results in frequency translation, an increased pass-band ripple, and a new finite attenuation pole. An explanation of this result is provided in the following section.

2.2 Design Considerations for Bond-Wire Based Band-pass Filter

2.2.1 Bond Wire Characteristics

An accurate model of the electrical characteristics of the bond-wires is crucial for their successful use in a high-performance filter application. In addition to the cross-section radius and material, the electrical properties of bond-wires depend on their physical dimensions — their height above the die plane (H), the horizontal length (D) and their distance between adjacent bond-wires, i.e. their pitch (P). Using the JEDEC-4 point model for the bond-wires (Fig. 2.5), the total wire length can be geometrically calculated from the horizontal distance (D), the height above the die plane (H) and the die thickness (H_1) [11]. 3D Ansoft HFSS^{TM} simulations were performed to study these

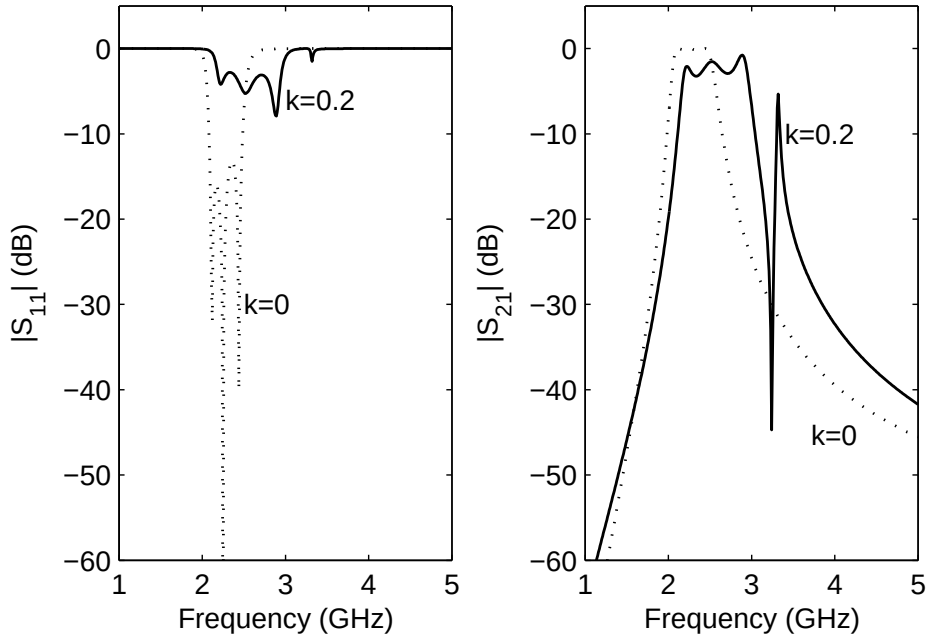


Figure 2.4: Simulated reflection (a) and transmission (b) characteristics of filter with and without mutual inductance.

variations. Fig. 2.7 shows the simulated variation in the bond-wire self-inductance, the coefficient of mutual inductance between adjacent bond-wires (k) and the coefficient of mutual inductance between next-to-adjacent bond-wires (k_2). The self inductance varies linearly with H and D, whereas k and k_2 do not vary significantly with H and D. With increasing pitch (P), the self inductance remains constant, whereas k and k_2 decay rapidly. Fig. 2.7(b) also shows the simulated $k_{corner}\ vs\ P$, which is the coefficient of mutual inductance between two bond-wires placed along adjacent edges of the die (Fig. 2.6). Here the pitch (P) is defined as the distance between the bond-wires measured along the edges. This demonstrates that mutual coupling is significantly lowered if bond-wires are placed along perpendicular edges.

For a typical die of height 280 μm , a down-bond with a height (H) of approximately 150 μm and horizontal distance (D) of 400 μm has a total wire length of roughly 780 μm . This corresponds to a self-inductance of about 0.7 nH. For closely

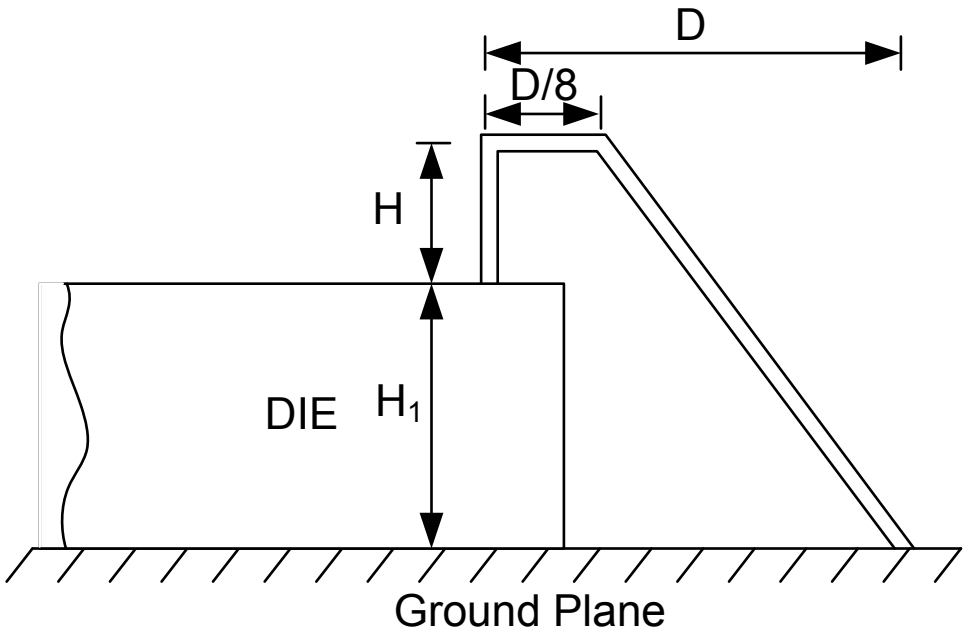


Figure 2.5: JEDEC 4-point bond-wire model [11].

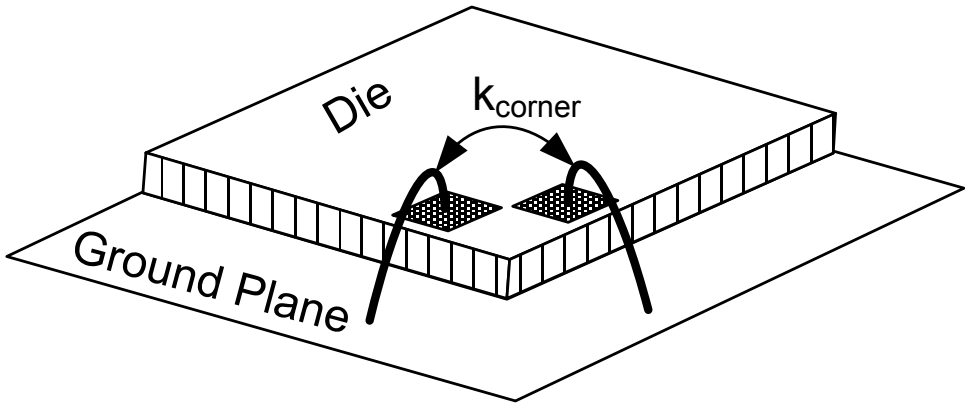


Figure 2.6: Orthogonal bond-wires at a chip edge.

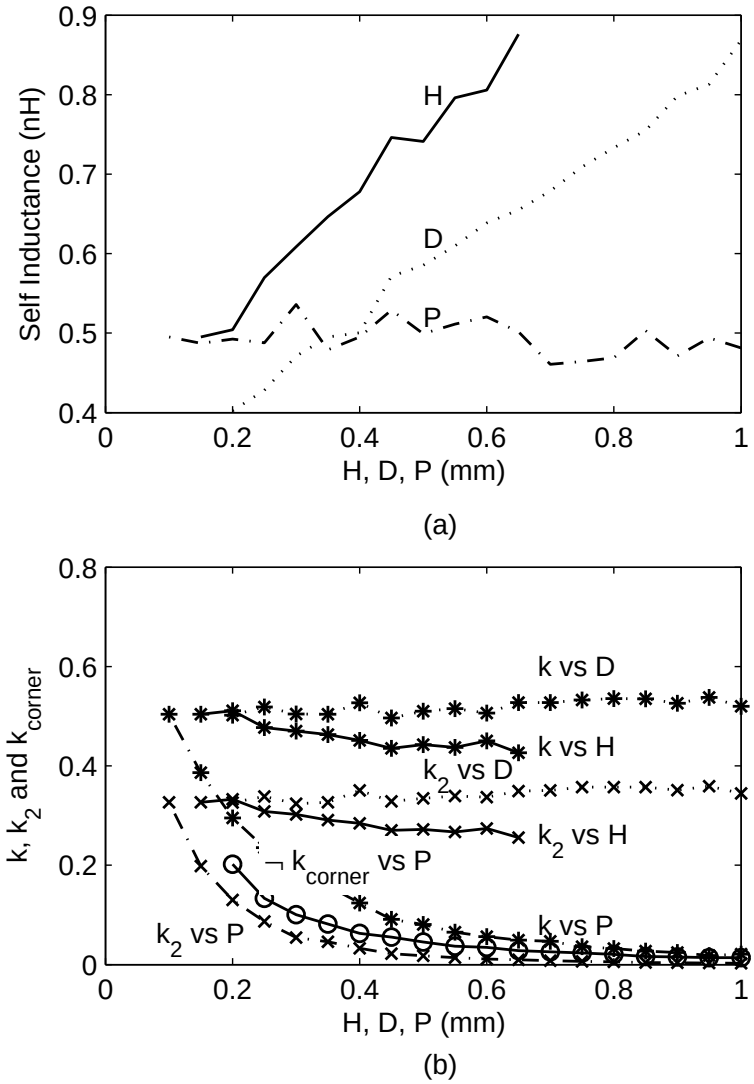


Figure 2.7: (a) Simulated variation in bond-wire self-inductance with horizontal length D, height H and pitch P (b) Simulated variation in coefficient of mutual inductance with adjacent bond-wire (k), coefficient of mutual inductance with next to adjacent bond-wire (k_2) and coefficient of mutual inductance between bond-wires placed along perpendicular edges (k_{corner}) vs H, D and P. Default H, D and P values are 150 μm , 350 μm and 100 μm respectively.

placed bond-wires with a pitch of 100 μm , the coefficient of mutual inductance (k) is approximately 0.5. Since the coefficient of mutual inductances depends primarily on the bond-wire pitch, it can be approximately controlled by the bond pad placement, and similar coupling can be assumed between uniformly spaced parallel bond-wires. The simulations also predict a Q-factor of higher than 50 for the bond-wires, which is much more than that of a typical on-chip spiral inductor.

However, it is difficult to target a bond-wire for a very specific inductance, so filters with bond-wires having different heights and lengths can be designed for testing purposes and, once an optimal filter performance is achieved, the bond-wires can be precisely reproduced by automatic die attach equipment [51].

2.2.2 Analysis of Filter Passband Insertion Loss

For a third-order Butterworth filter, $L_{prototype}$ = 2. The insertion loss can be derived for a $2n + 1$ section top-C coupled filter as

$$\frac{P_t}{P_{av}} \approx \left[1 - \frac{R_s}{\omega_0 L_{BW} Q}\right]^{n+1} \prod_{i=1}^{n} \left[1 - \frac{L_{prototype,2i}}{Q(\omega_c/\omega_0)}\right] \tag{2.1}$$

where, P_t and P_{av} are the transmitted power and the available power of the filter respectively, R_s is the source resistance, ω_0 is the center frequency and Q is the Quality factor. $L_{prototype,m}$ is the inductor value in the normalized low-pass prototype for the m^{th} section [48]. Fig. 2.8 shows the simulated and the calculated insertion losses of a three-pole filter designed with 0.5 nH inductors centered at 2.14 GHz. For higher Quality Factors, the calculated loss closely follows the simulated losses, but overestimates it at a lower Q when the source impedance, R_s, becomes comparable to the shunt resistance of the lossy resonators.

2.2.3 Analysis of Mutual Coupling Effect on Filter Response

The effect of mutual inductance on the filter response can be understood by separately examining the effect of mutual coupling *within* a resonator, and *between* resonators.

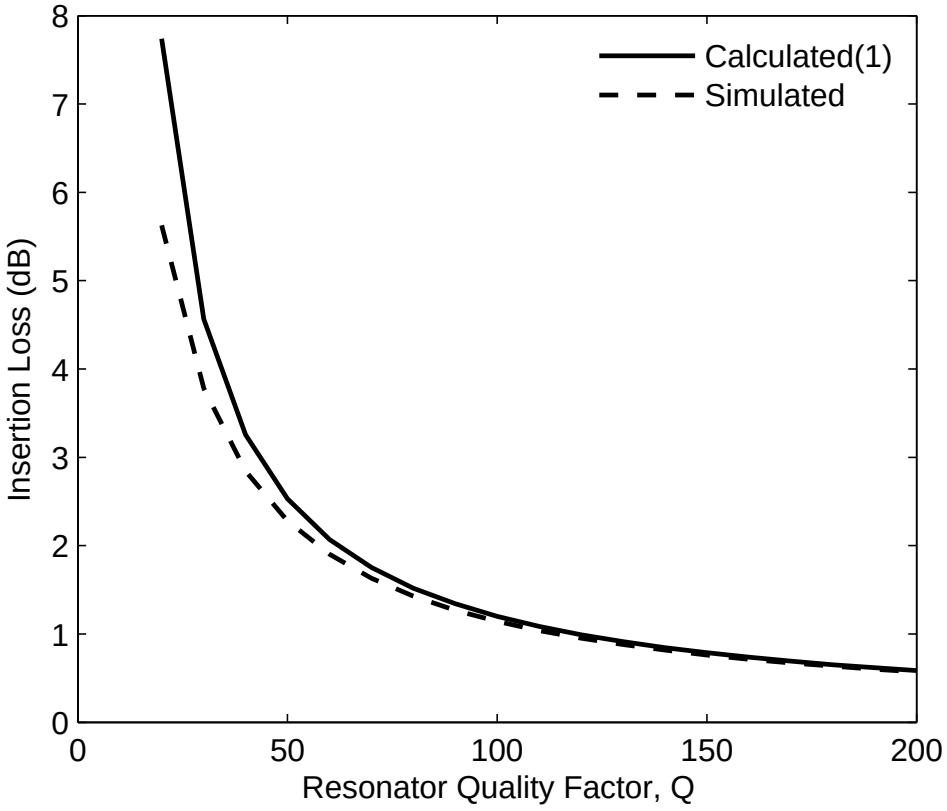


Figure 2.8: Simulated vs. calculated (using (2.1)) insertion loss for third-order filter as a function of resonator Q.

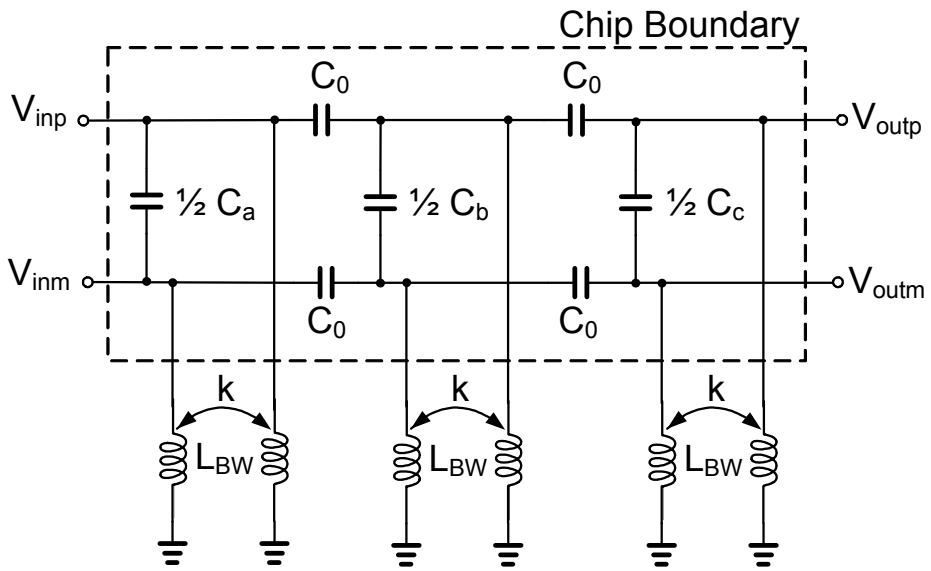


Figure 2.9: Differential filter with mutual inductance within the resonator.

Effect of Mutual Coupling Within Resonators

Consider the mutual inductances between inductors within the same resonators, as shown in Fig. 2.9. This effect can be equivalently modeled as a T-network of inductors (Fig. 2.10) [47]. In the differential mode, node A is a virtual ground and thus the effective self inductance of either inductor is reduced from L to $L(1-k)$. Hence the

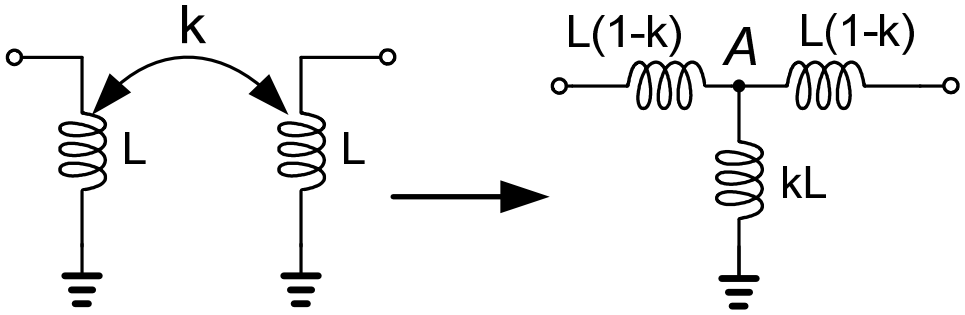


Figure 2.10: Equivalent schematic representation of a pair of coupled inductors.

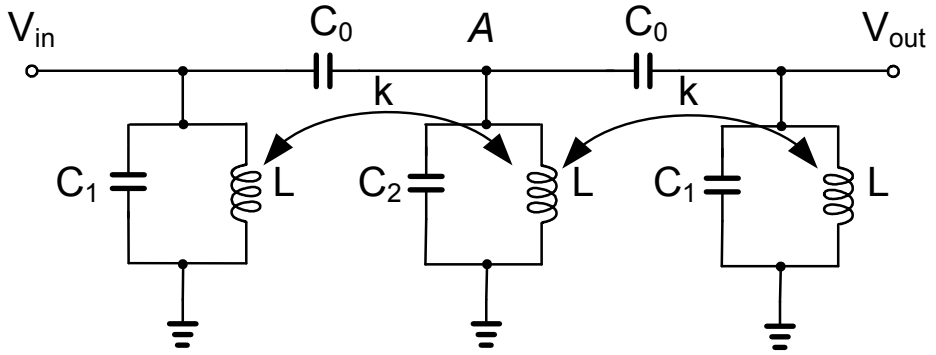


Figure 2.11: Ideal single-ended filter with mutual inductance between resonators.

new center frequency is given by

$$\omega_{new} = \frac{\omega_0}{\sqrt{1-k}} \tag{2.2}$$

The effect of the common-mode inductance kL on the circuit response will be considered later.

Effect of Mutual Coupling Between Adjacent Resonators

In order to examine some trends, a three-pole single-ended filter (Fig. 2.11) is analyzed under the following simplifying assumptions:

– The filter is designed for equal source and load terminations and so $C_1 = C_3$.

– The resulting filter is tested with an infinite load impedance and it is driven by an ideal current source. The load and source impedances affect the natural frequencies of the filter, but in this case, the Quality Factors of the attenuation zeros are sufficiently high, so that the effect is negligible.

– Only nearest neighbor mutual inductances are considered. For clarity, we first derive the attenuation zeros without any mutual inductance between resonators, and then examine the change in frequency when mutual inductance is present. The analysis is performed using a mode-splitting technique [52], where the circuit resonates at frequencies of the natural response of the system, which are also the attenuation zeros. Moreover, certain frequencies of the natural response can be selectively excited by appropriate choice of the initial excitement: either odd-mode or even-mode.

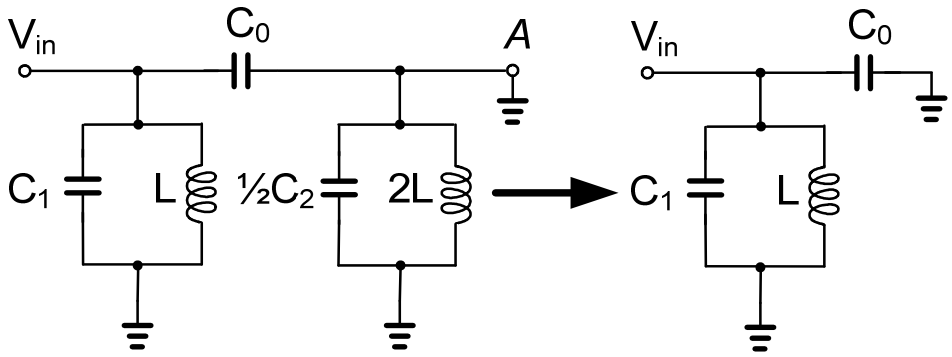


Figure 2.12: Odd-mode half-circuit of the single-ended filter.

Odd-Mode Analysis Without Mutual Inductance: In this case, equal and opposite current sources are placed at the input and output of the filter in Fig. 2.11. The center node A will therefore appear as a virtual ground and the filter can be reduced to Fig. 2.12. The resonant frequency is given by

$$\omega_1 = \frac{1}{\sqrt{L(C_1 + C_0)}} \tag{2.3}$$

Even-Mode Analysis Without Mutual Inductance: Another mutually exclusive manner to excite the system is to place equal current sources at the input and output. In this scenario, the filter can be drawn as in Fig. 2.13(a) and by symmetry, no current flows through the center node A and it appears as an open node. The filter can then be reduced to a half-circuit as shown in Fig. 2.13(b). For this system, the attenuation *zeros* are the *poles* of the input impedance Z_{in} [53]. Z_{in} can be expressed as,

$$Z_{in} = \frac{sL(1 + s^2L(C_2 + 2C_0))}{1 + s^2L(C_1 + C_2 + 3C_0) + s^4L^2(C_1C_2 + (2C_1 + C_2)C_0)} \tag{2.4}$$

Thus, the attenuation zeros — or frequencies of natural response of the filter without mutual inductance — are given by

$$\omega_2 = \sqrt{\frac{(C_1 + C_2 + 3C_0) - \sqrt{(C_0 + C_2 - C_1)^2 + 8C_0^2}}{2L(C_1C_2 + (2C_1 + C_2)C_0)}} \tag{2.5a}$$

$$\omega_3 = \sqrt{\frac{(C_1 + C_2 + 3C_0) + \sqrt{(C_0 + C_2 - C_1)^2 + 8C_0^2}}{2L(C_1C_2 + (2C_1 + C_2)C_0)}}. \tag{2.5b}$$

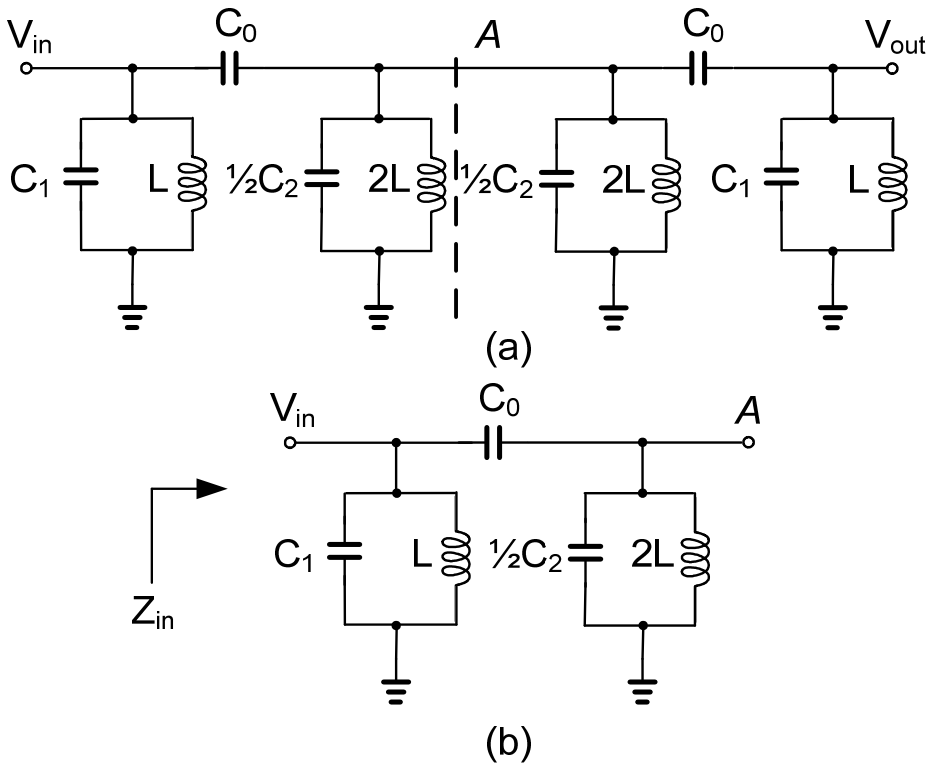


Figure 2.13: (a) Symmetric splitting of the single-ended filter (b) Even-mode half-circuit.

For $C_1 = C_2$, this reduces to

$$\omega_2 = \frac{1}{\sqrt{LC_1}} \tag{2.6a}$$

$$\omega_3 = \frac{1}{\sqrt{L(C_1 + 3C_0)}}, \tag{2.6b}$$

which indicates the coupling effects of the capacitor C_0. These three results (ω_1 , ω_2, and ω_3) are the approximate natural frequencies of the filter *without* the effect of coupling between the inductors. We will now examine the effects of mutual coupling between the inductors on the resulting natural frequencies.

Odd-Mode Analysis With Mutual Inductance: As in the case without mutual inductance, the odd-mode excitation renders the center node A as a virtual ground and the system again reduces to the circuit of Fig. 2.12. The resonant frequency is given by

$$\omega_{\mu 1} = \frac{1}{\sqrt{L(C_1 + C_0)}} \tag{2.7}$$

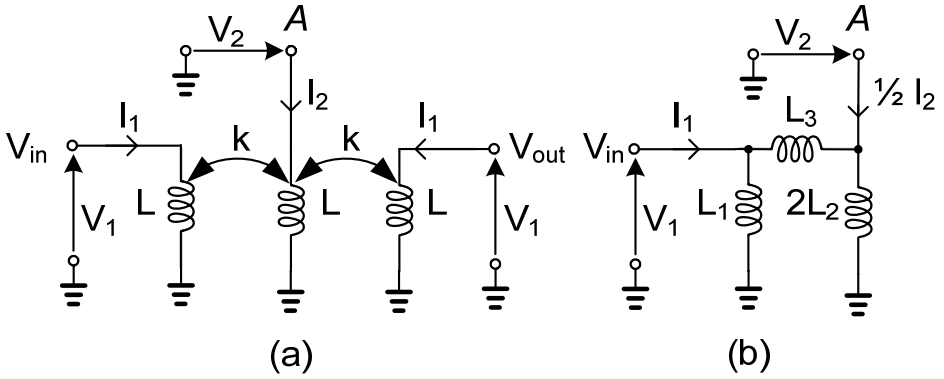


Figure 2.14: (a) Even-mode analysis of single-ended coupled filters with mutual inductance (b) Equivalent even-mode half circuit.

So there is no change in the natural frequency in the odd-mode case in the presence of coupling.

Even-Mode Analysis With Mutual Inductance: For the case of even-mode excitation, the filter needs to be symmetrically divided into two halves. Consider the network of inductors alone (without C_0, C_1, and C_2) as shown in Fig. 2.14(a). With even-mode excitation, the V_1 nodes will have equal current. Therefore, the equivalent even-mode half circuit is in the form of Fig. 2.14(b).

Writing the KVL for circuit in Fig. 2.14(a)

$$V_1 = sLI_1 + skLI_2 \tag{2.8a}$$

$$V_2 = 2skLI_1 + sLI_2 \tag{2.8b}$$

Similarly, for Fig. 2.14(b)

$$V_1 = s\left(\frac{L_1(L_3+2L_2)}{L_1+2L_2+L_3}\right)I_1 + s\left(\frac{L_1L_2}{L_1+2L_2+L_3}\right)I_2 \tag{2.9a}$$

$$V_2 = s\left(\frac{2L_1L_2}{L_1+2L_2+L_3}\right)I_1 + s\left(\frac{(L_1+L_3)L_2}{L_1+2L_2+L_3}\right)I_2 \tag{2.9b}$$

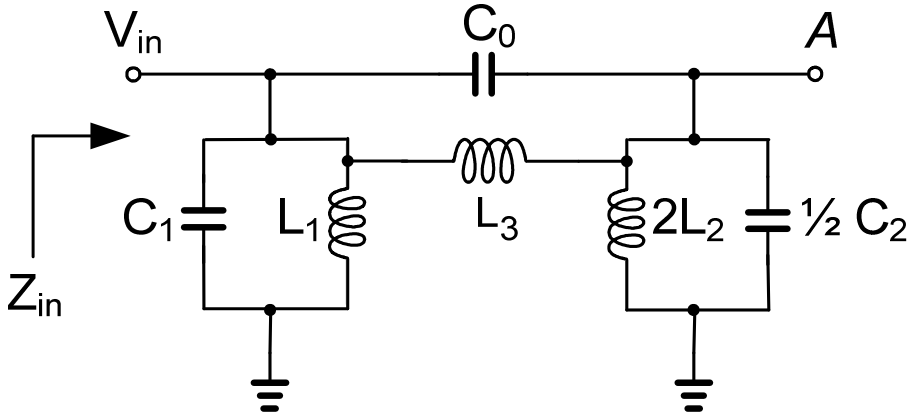


Figure 2.15: Equivalent even-mode half-circuit of the filter with mutual coupling between the sections.

Comparing (2.8a) and (2.8b) with (2.9a) and (2.9b) respectively, and solving yields

$$L_1 = \frac{1-2k^2}{1-k}L \tag{2.10a}$$

$$L_2 = \frac{1-2k^2}{1-2k}L \tag{2.10b}$$

$$L_3 = \frac{1-2k^2}{k}L \tag{2.10c}$$

Using the inductor model of Fig. 2.14, the circuit in Fig. 2.11 can be split into an even-mode half-circuit as shown in Fig. 2.15. The attenuation zeros can be computed from the poles of the input impedance Z_{in}.

$$Z_{in} = \frac{sL\left(1+(1-2k^2)s^2L(C_2+2C_0)\right)}{\left(1+s^2L\left(C_1+C_2+(3-4k)C_0\right)+s^4(1-2k^2)L^2\left(C_1C_2+(2C_1+C_2)C_0\right)\right.} \tag{2.11}$$

The denominator of (2.11) is quadratic in s^2, and the corresponding attenuation zero

locations are given by (2.12a) and (2.12b).

$$\omega_{\mu 2} = \left\{ \frac{C_1 + C_2 + (3-4k)C_0}{2(1-2k^2)L\left(C_1C_2 + (2C_1 + C_2)C_0\right)} - \frac{\sqrt{\left(C_1 + C_2 + (3-4k)C_0\right)^2 - 4(1-2k^2)\left(C_1C_2 + (2C_1 + C_2)C_0\right)}}{2(1-2k^2)L\left(C_1C_2 + (2C_1 + C_2)C_0\right)} \right\}^{\frac{1}{2}} \tag{2.12a}$$

$$\omega_{\mu 3} = \left\{ \frac{C_1 + C_2 + (3-4k)C_0}{2(1-2k^2)L\left(C_1C_2 + (2C_1 + C_2)C_0\right)} + \frac{\sqrt{\left(C_1 + C_2 + (3-4k)C_0\right)^2 - 4(1-2k^2)\left(C_1C_2 + (2C_1 + C_2)C_0\right)}}{2(1-2k^2)L\left(C_1C_2 + (2C_1 + C_2)C_0\right)} \right\}^{\frac{1}{2}} \tag{2.12b}$$

The preceding analysis suggests that the effect of coupling between the bond-wires *within* a resonator results in an upward frequency translation, which can be addressed by designing the filter for a slightly lower center frequency. However, the coupling *between* resonators causes the attenuation zeros to move together, and (as the coupling grows) then separate, as shown in Fig. 2.16. Fig. 2.17 depicts the zero movements on the complex s-plane. This pole-splitting has a detrimental effect on the filter performance, since it results in increased passband ripple and insertion loss. This mutual coupling can be reduced by placing the bond-wires further apart, inserting a grounded shielding bond-wire on the chip, or bonding the wires along perpendicular chip edges. Based on these observations, an improved bond-wire configuration is proposed in Section 2.3.

Additional Attenuation Poles and Zeros due to Mutual Coupling

In the above analysis, the inductive coupling within the resonators and between the resonators was considered separately. When all the inductors are coupled to each other, additional parallel transmission paths are created. In this case, there are two additional paths through mutual inductive coupling – from the input to the center node and from input to the output node. Since the direct coupling is capacitive and the bond-wire coupled paths are inductive, the mutual coupling creates two poles of attenuation

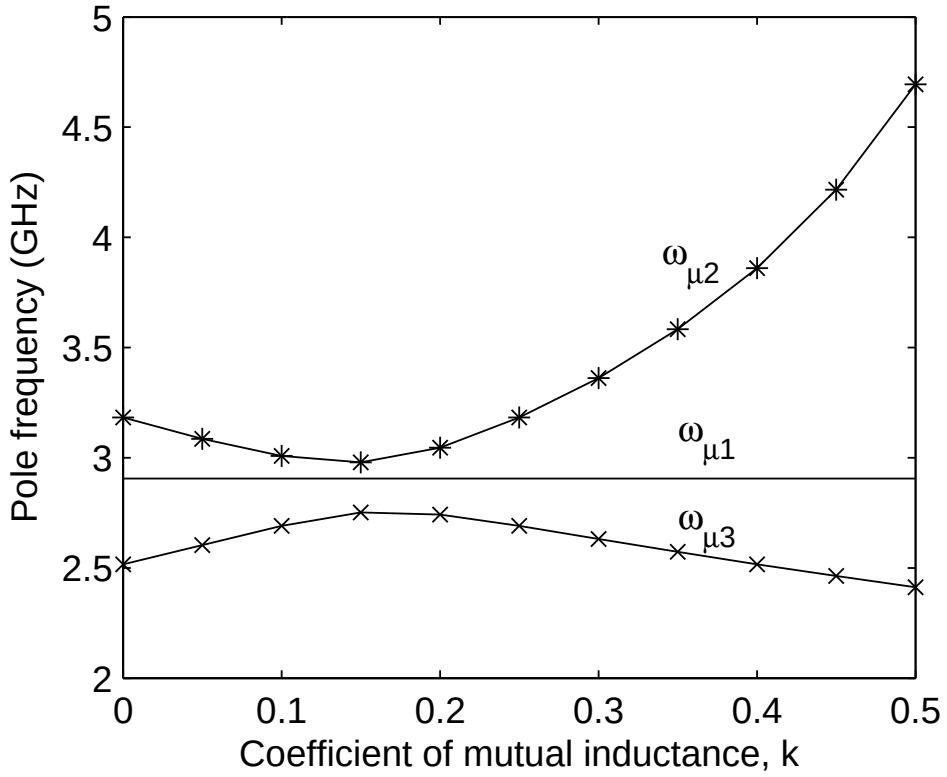


Figure 2.16: Variation in attenuation zeros with coefficient of mutual inductance for the filter centered at 2.14 GHz with L_{BW}=0.5 nH. $\omega_{\mu 1}$, $\omega_{\mu 2}$ and $\omega_{\mu 3}$ are given by (2.7), (2.12a) and (2.12b) respectively.

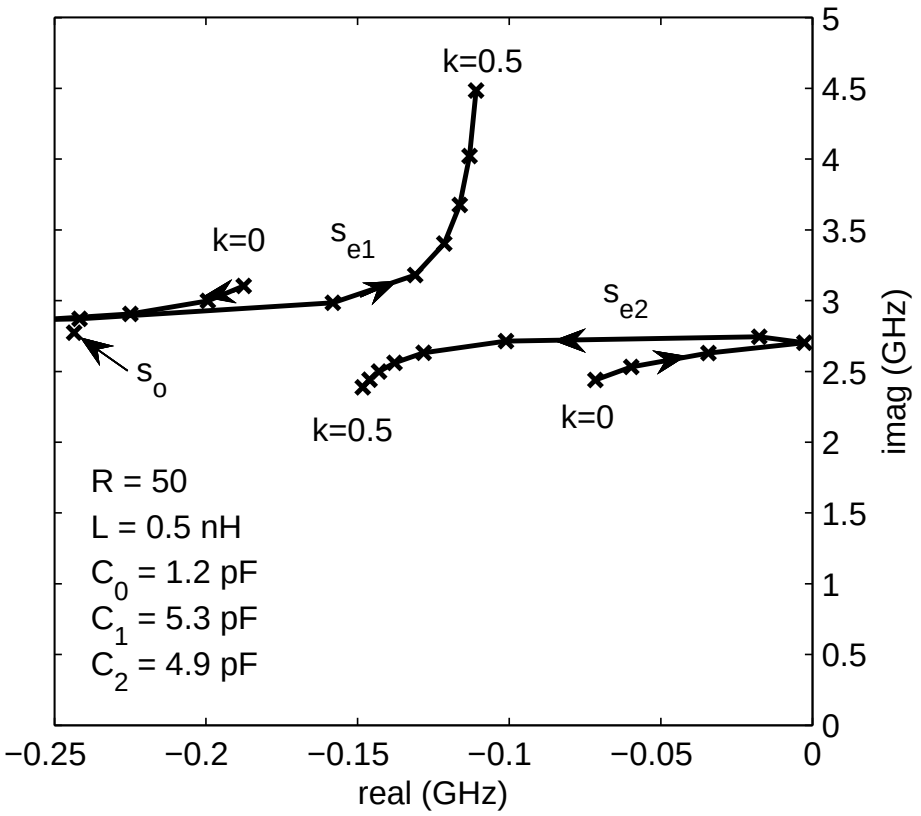


Figure 2.17: Pole positions in the complex s-plane with variation in the coefficient of mutual inductance, for a filter centered at 2.14 GHz with L_{BW}=0.5 nH. s_o is the odd-mode pole, whereas, s_{e1} and s_{e2} are the even-mode poles. Only the dominant poles in +y half plane are shown.

when the transmission along the parallel paths (through the inductor and capacitor) are equal in magnitude and opposite in phase. One of these poles is seen in Fig. 2.4.

It is evident from Fig. 2.7 that there is coupling between next-to-adjacent bondwires as well. These couplings create additional transmission channels and attenuation poles.

2.2.4 Analysis of Common-Mode Filter Response

We will first analyze the filter common-mode response when no mutual coupling is present. In the common-mode configuration, there is no current through the shunt capacitors in Fig. 2.3(b), hence the filter becomes high-pass. Using the previously described mode-splitting analysis, it can be found that the attenuation zeros are located at

$$\omega_{cm1} = \frac{1}{\sqrt{LC_0}} \tag{2.13a}$$

$$\omega_{cm2} = \frac{1}{\sqrt{3LC_0}} \tag{2.13b}$$

Since C_0 is typically much smaller than C_1, these attenuation zeros are located at higher frequencies than the differential filter passband. The resulting circuit is a five-element filter with a roll-off of 100 dB/decade, hence the CMRR can be approximately computed as

$$CMRR \approx 50 \log_{10} \left[\frac{1}{3} \left(1 + \frac{C_1}{C_0} \right) \right] \tag{2.14}$$

The common-mode configuration with mutual inductance lacks an equivalent line of symmetry, so the mode-splitting technique cannot be used. Intuitively, the mutual inductive coupling creates additional transmission paths, which cancel the signal though the direct path resulting in loss poles. Fig. 2.18 shows the simulated differential response along with the common-mode response for different coefficients of mutual inductance. This shows that the mutual inductances further degrade the CMRR response.

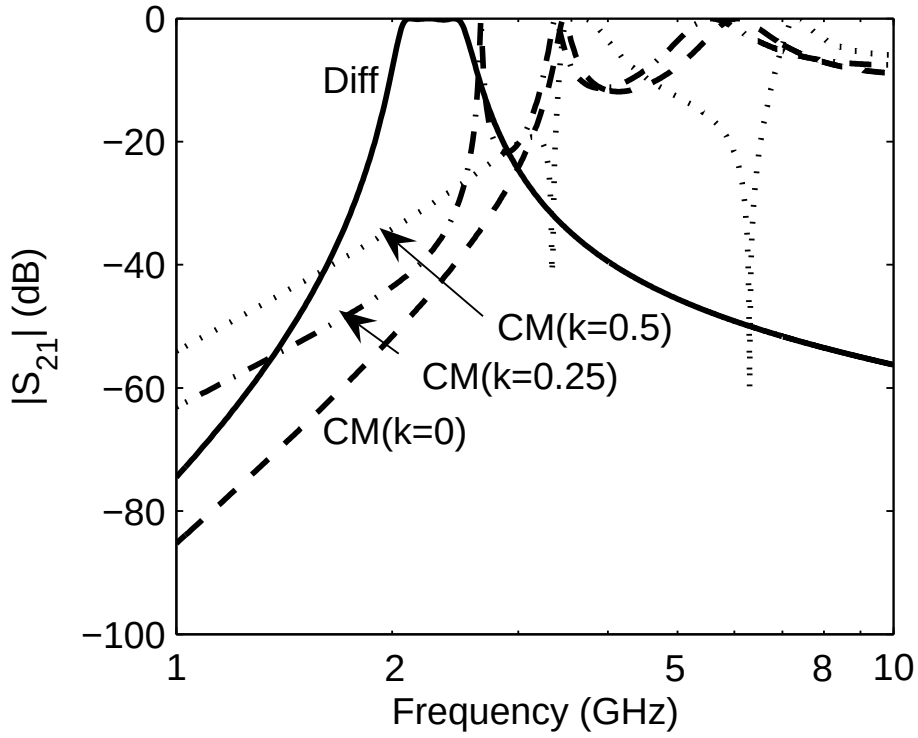


Figure 2.18: Differential-mode (k=0) response and common-mode responses for k=0, k=0.25 and k=0.5.

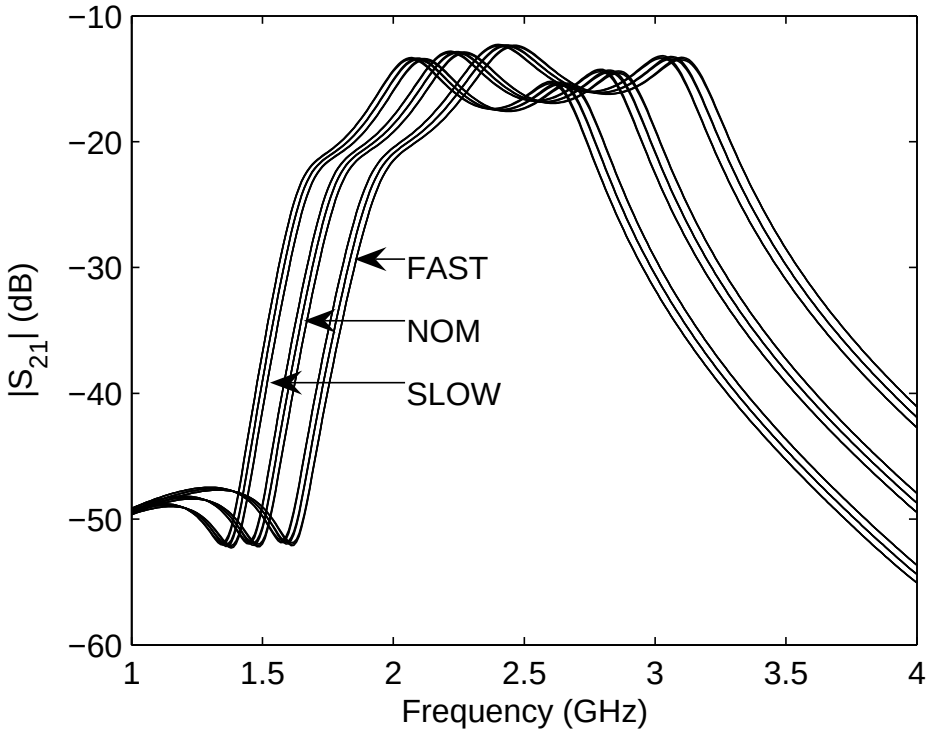


Figure 2.19: Corner simulation of the filter S_{21} with process corners and 5% variation in bond-wire inductance and Quality factor.

2.2.5 Process Variations

Any variation in on-chip capacitances or bond-wire inductances can alter the filter response. The capacitances change due to the process and temperature variations, whereas, the bond-wire variations are attributed to the inaccuracies in the bonding machine. The modern precision automated bonding machines can reliably reproduce the bonding with an error of less than 5 μm in the dimensions. Hence, once a bond-wire configuration is optimized for the desired filter response through experiments, the variation is less than 5% as the bond-wire dimensions are of the order of 100 μm .

Simulations are conducted on the process corners along with 5% variation in the inductance and Quality factor of the bond-wires. The filter S_{21} responses for different corners are shown in Fig. 2.19. The three separated groups of curves corresponds to the FAST, NOM and SLOW process corners. Typically, the FAST and SLOW corners correspond to $\pm$ 15% variation from the NOM capacitance. The curves within a group are due to the variations in the bond-wire elements. Hence, capacitance process variations are the primary contributor to the frequency translation. The effect on filter Q is negligible. Simulations reveal that the variations in mutual coupling between the inductors have some impact on the filter Q and bandwidth. However, they have negligible effect on the filter roll-off at the lower stop-band, where the transmitter signal lies.

2.2.6 Filter Tuning

The variations in the filter response necessitates a tunable filter. Metal-oxide-semiconductor (MOS) capacitors and p-n junctions are typically used as varactors for the tuning purposes. For tuning integrated circuits, MOS varactors are generally preferred for their broader tuning range ($\pm$ 30%) as compared to the p-n junction varactors ($\pm$ 20%) over the same tuning voltage range [54]. However, the MOS varactors are non-linear in the tuning range and the minimum Quality factor of the MOS varactors is around 20-30 [54, 55, 56, 57]. This may be acceptable in designs involving on-chip spiral inductors with lower Quality factors, but can be a significant contributor to the insertion losses in the filter under consideration.

As discussed in the previous sub-section, the variation in the bond-wires is much

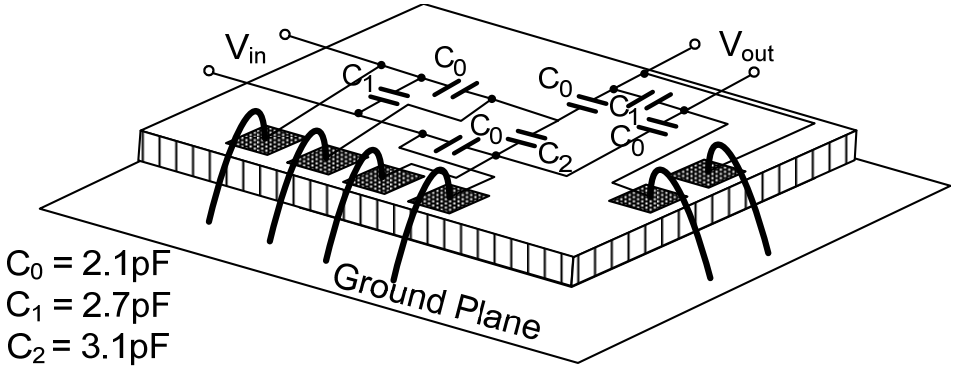


Figure 2.20: Proposed bond-wire configuration for on-chip filter.

smaller than that of the on-chip capacitors. Hence, $\pm$ 20% tuning range of the p-n junction varactor should suffice for tuning this filter. The p-n junction varactors usually have a better quality factor than the MOS varactors. Also, these varactors can be configured to achieve very high linearity [58]. Another approach can be using a parallel bank of MOS varactors, each varactor being biased either at high or low voltage. In these operating regions, the MOS varactors have high Quality factor and linearity [59].

2.3 WCDMA CMOS LNA and Bandpass Filter Design

As the mutual coupling analysis demonstrated, the input and output resonator sections should be isolated from each other to prevent finite attenuation poles being created around the passband. This can be accomplished by placing grounded bond-wires between the sections, or by placing the corresponding bond-wires along perpendicular sections, as shown in Fig. 2.6. The later method was preferred since it occupies less die area. In the proposed configuration, these bond-wires of the central resonator were placed in between the two bond-wires of the input resonator as shown in Fig. 2.20 to minimize the differential-mode to common-mode conversion by maintaining a differential symmetry. Full 3D EM simulations were performed for this bond-wire configuration and the results were used in the filter design. The on-chip capacitances were tuned to obtain the best performance with this bond-wire configuration.

The LNA/filter combination determines the overall front-end performance. As

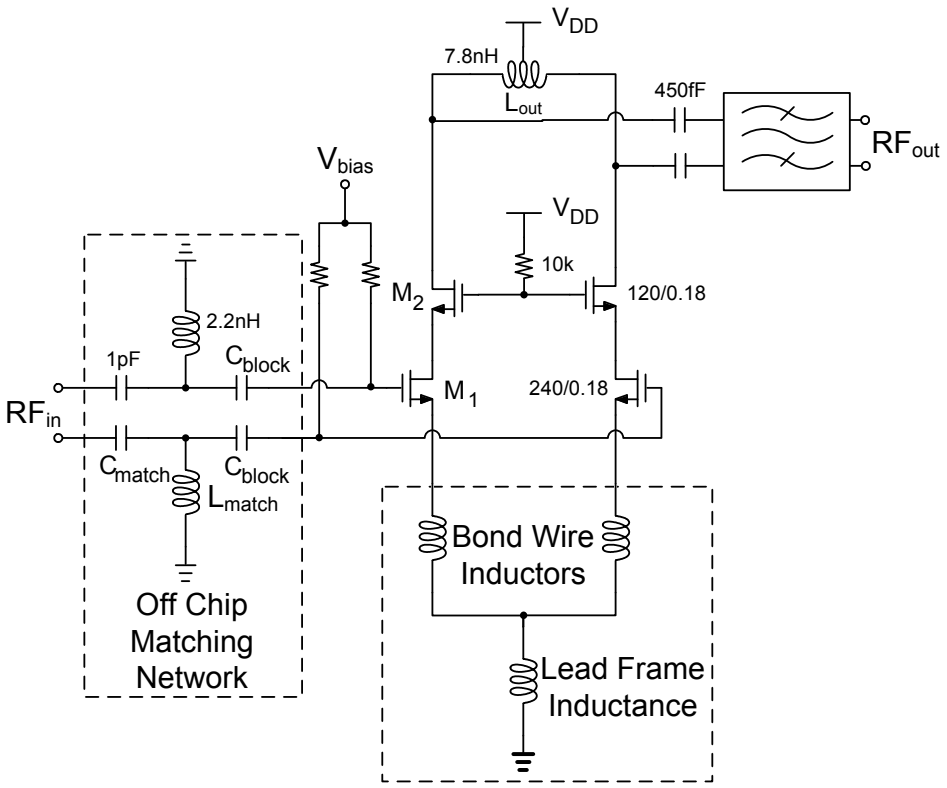


Figure 2.21: WCDMA CMOS LNA schematic. The output of the LNA drives the bandpass filter.

shown in Fig. 2.21, a pseudo-differential cascode topology is chosen for the low-noise amplifier for improved headroom and isolation, and ease of integration with the differential on-chip bandpass filter of Fig. 2.20. A bias current of 5.5 mA per branch is chosen to achieve optimum linearity, and the transistor width is optimized for noise performance. The source degeneration is provided by bond-wires terminating on a single lead pin, which is connected to ground through the lead frame of the package; the lead pin inductance provides some common-mode rejection.

The cascaded system of the LNA and the bandpass filter is optimized for end-to-end gain and noise performance. The LNA input is matched using an off-chip LC section, while the filter is tuned for 100 Ω differential output impedance. The LNA output is matched to the filter input.

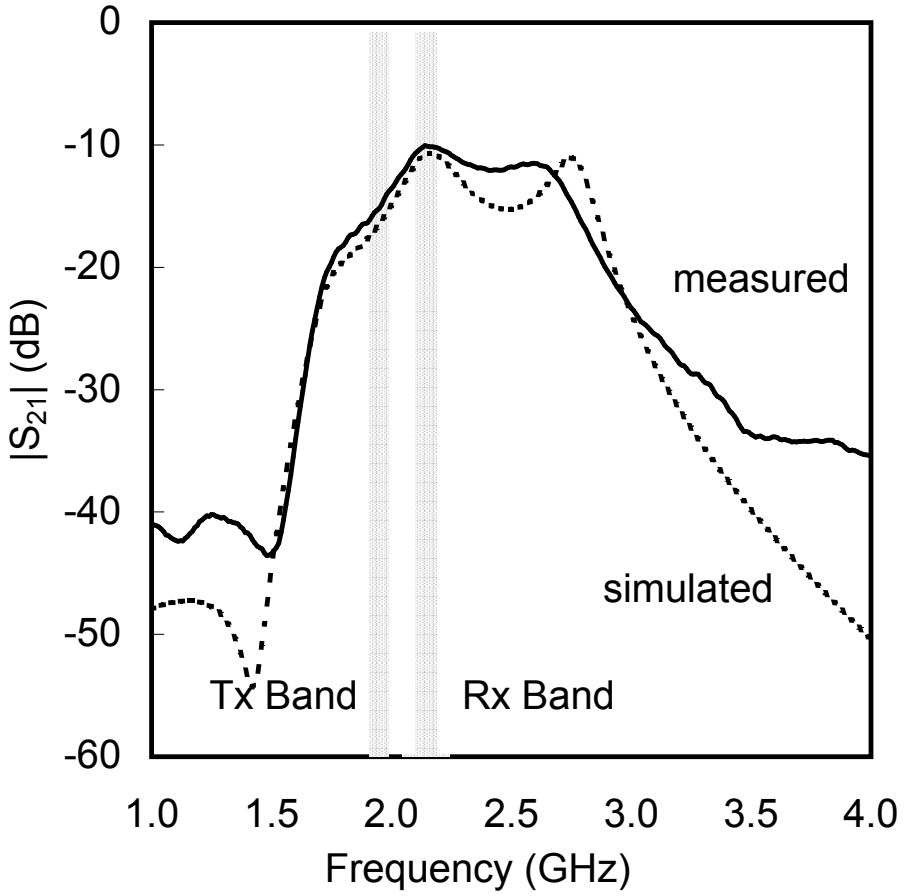


Figure 2.22: Measured and simulated S_{21} of the bandpass filter, shown in solid and dashed lines respectively.

2.4 Measurement Results

2.4.1 Bandpass Filter

For testing purposes, the filter was fabricated stand alone. It is comprised of 1 fF/ μm^2 MIM capacitors and 1.2mil gold bond-wires. The filter measures 400x550 μm^2 without the input and the output bonding pads. The input and the output were probed using GSSG differential probes and stripline 180^o hybrids were used for balanced to unbalanced conversion. Fig. 2.22 shows the measured filter transmission response along

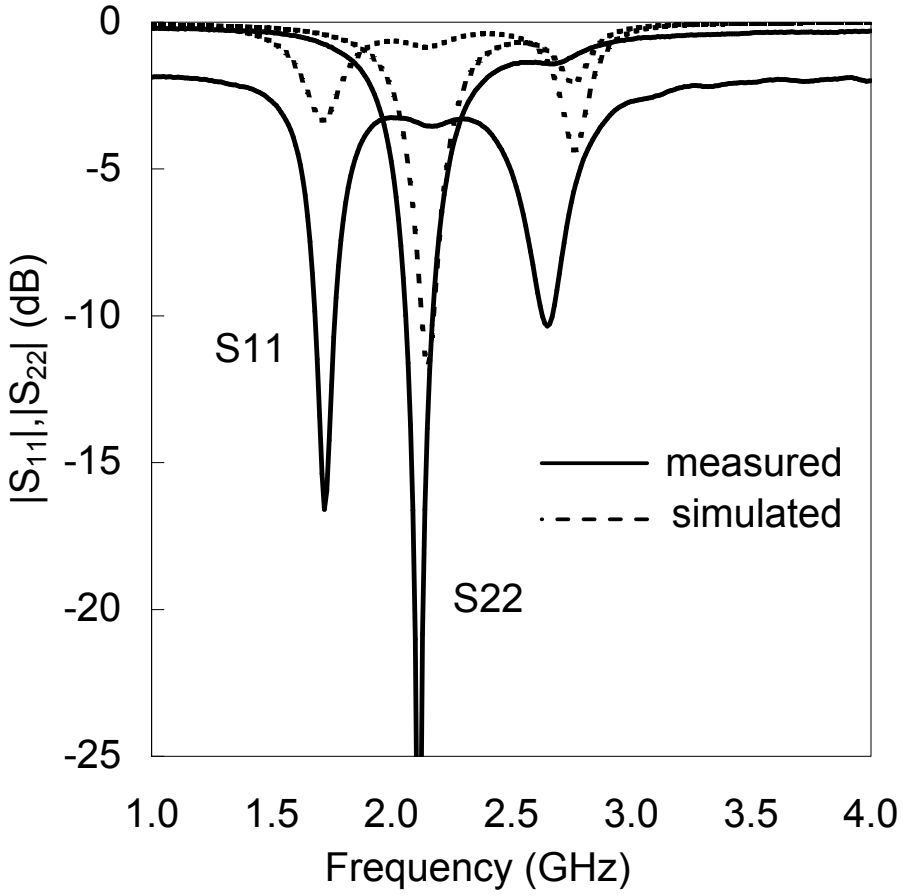


Figure 2.23: Measured and simulated S_{11} and S_{22} of the bandpass filter, shown in solid and dashed lines respectively.

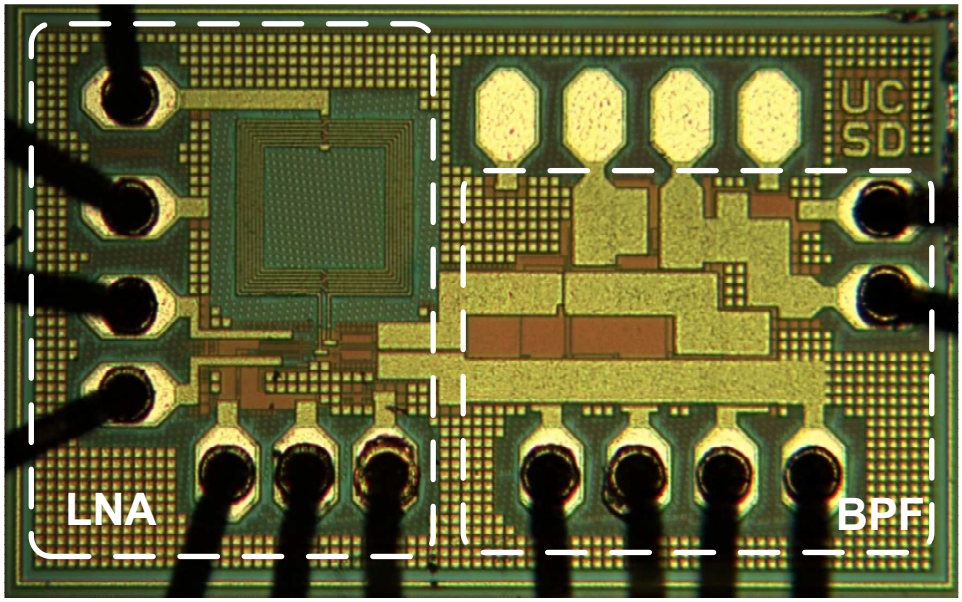


Figure 2.24: Microphotograph of the CMOS LNA and the BPF. The chip occupies 1025x600 μm ^{2}.

with the simulated transmission response with the layout parasitics back-annotated. The transmission zero appearing in the S_{21} plot around 1.5 GHz is attributed to the small residual mutual coupling between the orthogonal bond-wire sets. The measured and the simulated input and output reflection responses are shown in Fig. 2.23. The relatively high input reflection coefficient is due to the fact that the filter input is matched to the LNA output impedance, rather than 50 ohms. The slight mismatch between the measured and simulated S_{11} is due to series resistance in the balun and the GSSG probes.

2.4.2 Cascaded LNA and Bandpass Filter

The cascaded system of the LNA and the filter was fabricated in a 0.18 μm CMOS process. The LNA occupies 390x270 μm^2 without the bonding pads. A microphotograph of the complete system is shown in Fig. 2.24.

The circuit had a gain of 9.5 dB at 2110 MHz and achieved a TX/RX suppression of 10 dB at 1920 MHz (190 MHz offset) as shown in Fig. 2.25. The measured Noise Figure was less than 1.6 dB in the passband. The input and the output return losses were

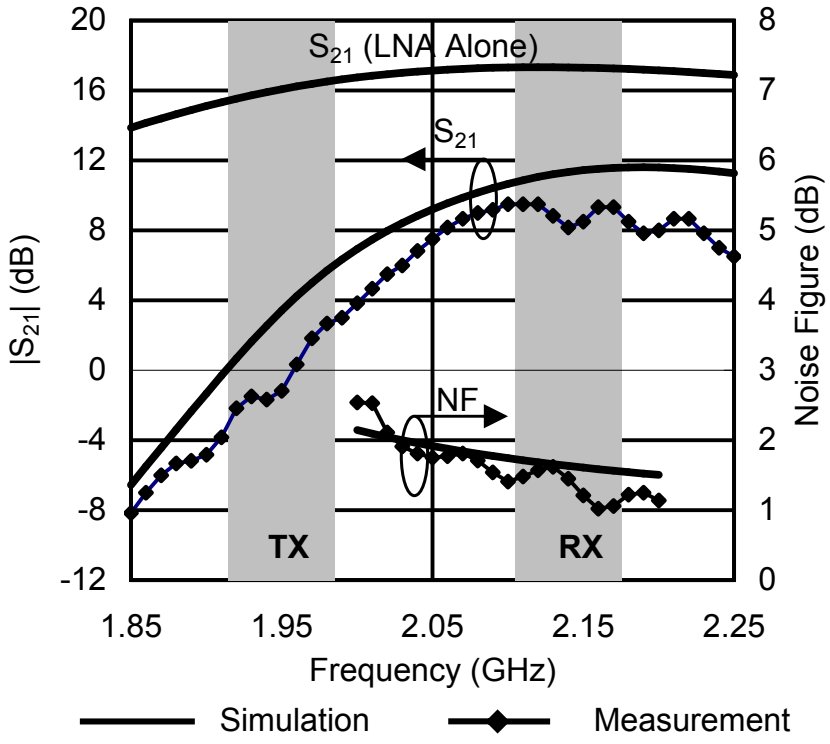


Figure 2.25: Measured gain of the LNA and BPF. The TX/RX suppression is 11 dB, and the Noise Figure is less than 1.6 dB.

Table 2.1: Measurement Results

Specification	Measurement	Simulation	Unit
RX Band	2110-2170	2110-2170	MHz
TX Band	1920-1980	1920-1980	MHz
Gain (Rx)	9.5	11.4	dB
Noise Figure	$\leq$ 1.6	1.45	dB
Tx Rejection	10	9	dB
IIP_3 (cross-modulation)	-5	-4	dBm
IIP_3 (out-of-band)	-5	-3	dBm
IIP_3 (in-band)	-10	-5.5	dBm
Gain Compression	-20	-12.5	dBm
S_{11}	-7		dB
S_{22}	-12	$\leq$ -10	dB
Power	11 mA @ 2V	11 mA @ 2V	

-7 dB and -12 dB respectively. For three-tone cross-modulation (XM) test, two -30 dBm tones were placed at the TX frequency of 1920 MHz $\pm$ 1.25 MHz and the third jammer tone with -45 dBm power was placed at 2137.5 MHz. The resultant XM distortion was measured at 2140 MHz and the corresponding XM IIP_3 was -5 dBm. The out-of-band linearity test was conducted with two tones at 1950 MHz and 2045 MHz and the resulting IIP_3 was -5 dBm. The in-band IIP_3 measurement was conducted with 10 MHz and 20 MHz offset tones and was found to be -10 dBm. The input 1 dB gain compression point at 2140 MHz was -20 dBm. The results are summarized in Table 2.1. The agreement between simulated and measured results is excellent, demonstrating the efficacy of the filter design approach described in the previous sections.

2.5 Conclusion

The challenge of on-chip bandpass filter design presents a perennial problem to the wireless system designer. The use of grounded bond-wires as a resonator technology is an attractive alternative to more traditional approaches. The advantage of the lower loss that these devices possess must be balanced against their limited range of values and high degree of mutual coupling.

This chapter highlighted some potential solutions to these limitations, and we

presented design techniques to mitigate some of the problems. A WCDMA CMOS LNA with an bond-wire-based integrated transmit interference suppression filter demonstrated that high performance could be achieved, at the expense of slightly higher Noise Figure, and the extra area required for the filter itself. These promising approaches point the way toward expanded use of these techniques in the future. This chapter has been published in part in the following publications:

1. H. Khatri, L. Larson, and D. Lie, "On-chip monolithic filters for receiver interference suppression using bond-wire inductors," in *Proc. IEEE Silicon Monolithic Integrated RF Systems, SiRF*, 2006, pp. 166-169.

2. H. Khatri, P. S. Gudem, and L. E. Larson, "Integrated RF interference suppression filter design using bond-wire inductors," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1024-1034, May 2008.

Chapter 3

CMOS Transistor Model for Passive Mixer Simulation

3.1 Introduction

Passive CMOS mixers have gained wide popularity in modern integrated receiver systems, owing to better voltage headroom, flicker noise and negligible power consumption as compared to active implementations. Several detailed studies have been undertaken to address passive mixer design concerns, such as noise, dc offset, and second-order distortion [60,61,62]. However, little detailed analysis has been published on the third-order nonlinear behavior of these mixers. With a motivation of eliminating the off-chip RF filter, it is important to pay close attention to the mixer nonlinearity and to obtain an accurate simulation estimate of the mixer nonlinearity.

At the V_{DS}=0 bias, the BSIM3v3, BSIM4, Philips MM9 and EKV models deviate from the measured results, due to discontinuities in the higher order derivatives of drain current and terminal charges [63, 64, 65, 66, 67]. These models typically predict an anomalous IM_3 slope of 2:1, instead of 3:1, for the third-order intermodulation distortion in a passive mixer. Nevertheless, these models still meet the Gummel symmetry condition, i.e., the drain current is a symmetric function of V_{DS}, when V_D+V_S is kept constant. This paper aims at explaining the mechanism through which the discontinuity in the second derivative of the drain current leads to a 2:1 slope for the third-order

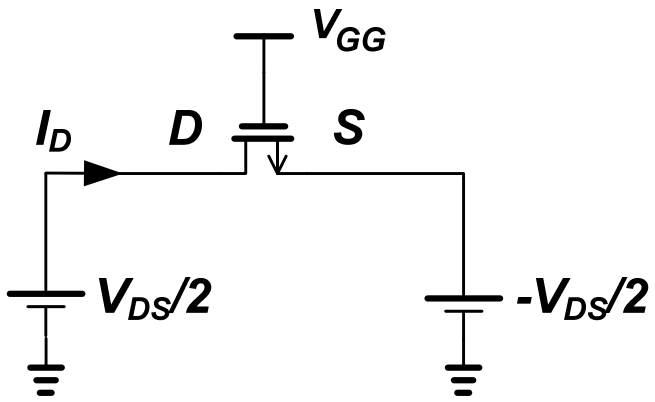


Figure 3.1: Schematic for DC analysis of a NMOS transistor.

distortion, and provide precise guidelines for minimizing anomalous IM_3 behavior in passive mixer simulation.

The latest surface-potential based model, PSP [68] and the next generation BSIM model, BSIM5 [69, 70] have overcome this limitation and give the correct slope of 3:1 for the third-order distortion.

3.2 CMOS I_D versus V_{DS} Relationship

For a MOS transistor, the typical Gummel symmetry test is conducted by exciting the source and drain terminals with equal and opposite voltages (odd mode excitation), as shown in Fig. 3.1. In this scenario, the drain current, I_D can be expressed as a polynomial function of the drain-source voltage, V_{DS}, as,

$$I_D = a_1 V_{DS} + a_2 V_{DS}^2 + a_3 V_{DS}^3 + a_4 V_{DS}^4 + \dots \tag{3.1}$$

The simulated drain current using the BSIM3v3 model for different gate voltages is shown in Fig. 3.2. Evidently, the model correctly exhibits Gummel symmetry, hence, it is required that,

$$I_D(V_{DS}) = -I_D(-V_{DS}) \tag{3.2}$$

This is possible when the even-order coefficients (a_2, a_4, etc) in (3.1) are either zero or are equal and opposite in sign for positive and negative values of V_{DS}. In the newer

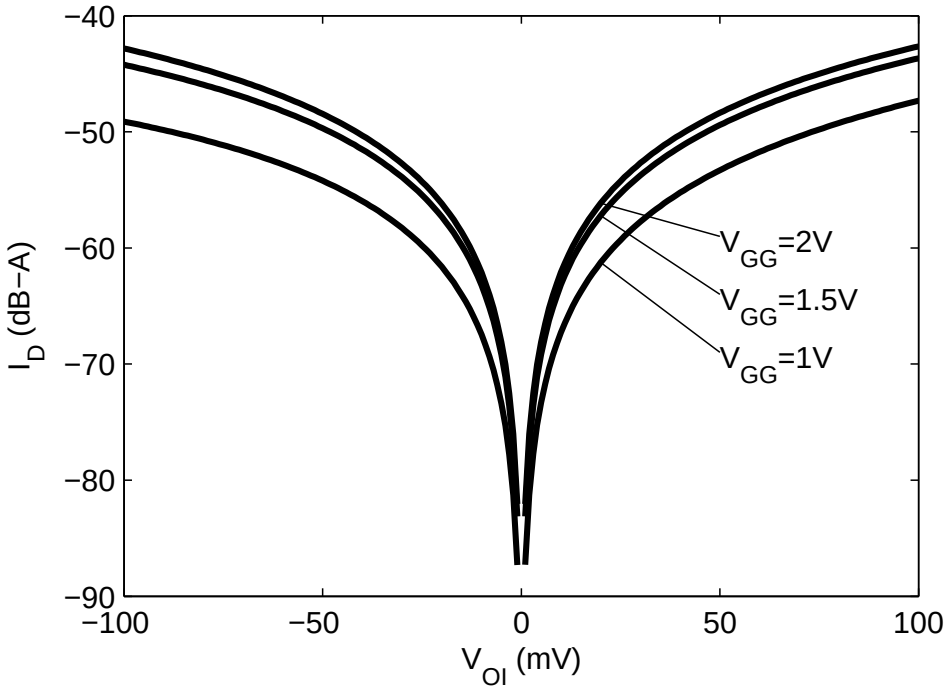


Figure 3.2: Simulated I_D versus V_{DS} curve for a 50 μm/0.18 μm NMOS transistor using BSIM3v3 model. $V_D + V_S = 0$, V_{GG} = gate voltage.

generation models (PSP, BSIM5), these even-order coefficients are zero, while in the earlier models these are discontinuous at $V_{DS} = 0$ and have equal and opposite values in the two regions. For these later cases, the drain current should be expressed as a piecewise polynomial function of the drain-source voltage as shown in (3.3), i.e.

$$I_D = \begin{cases} a_1 V_{DS} + a_2 V_{DS}^2 + a_3 V_{DS}^3 + ... & \text{for } V_{DS} > 0 \\ a_1' V_{DS} + a_2' V_{DS}^2 + a_3' V_{DS}^3 - ... & \text{for } V_{DS} < 0 \end{cases} \tag{3.3}$$

For maintaining the Gummel symmetry,

$$a_n' = \begin{cases} a_n & \text{for odd } n, \\ -a_n & \text{for even } n. \end{cases} \tag{3.4}$$

The advantage of this piecewise representation can be shown by comparing the DC I_D simulation response to its polynomial estimations. Fig. 3.3 shows the normalized error in I_D estimation using third-order and tenth-order polynomials for the entire V_{DS} range

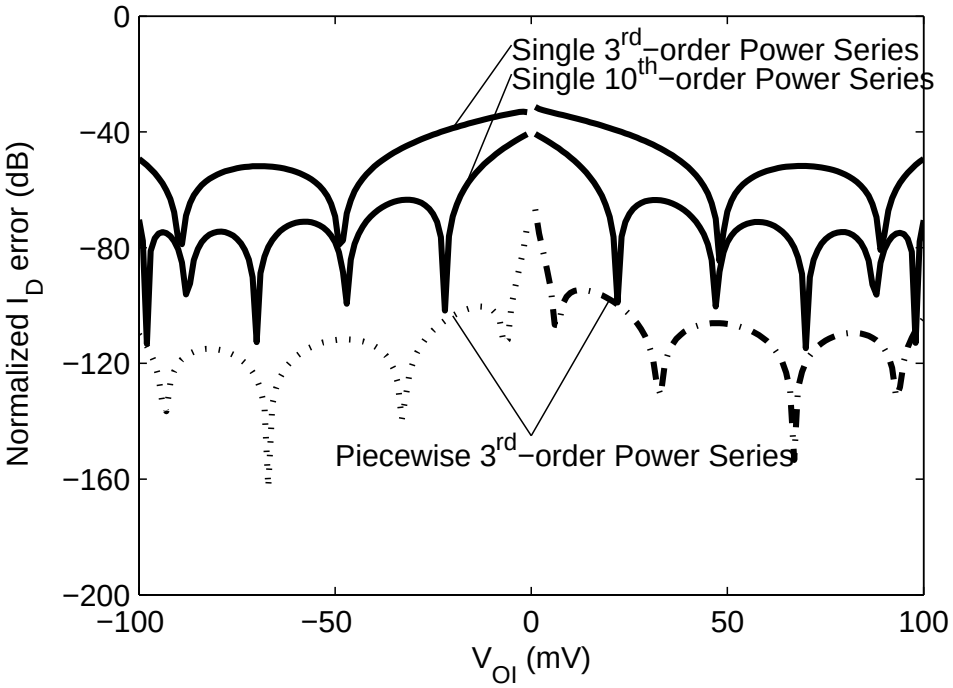


Figure 3.3: Normalized mean square error in I_D estimation of Fig. 3.2, obtained using BSIM3v3 model, for a single third-order polynomial and a pair of piecewise polynomials.

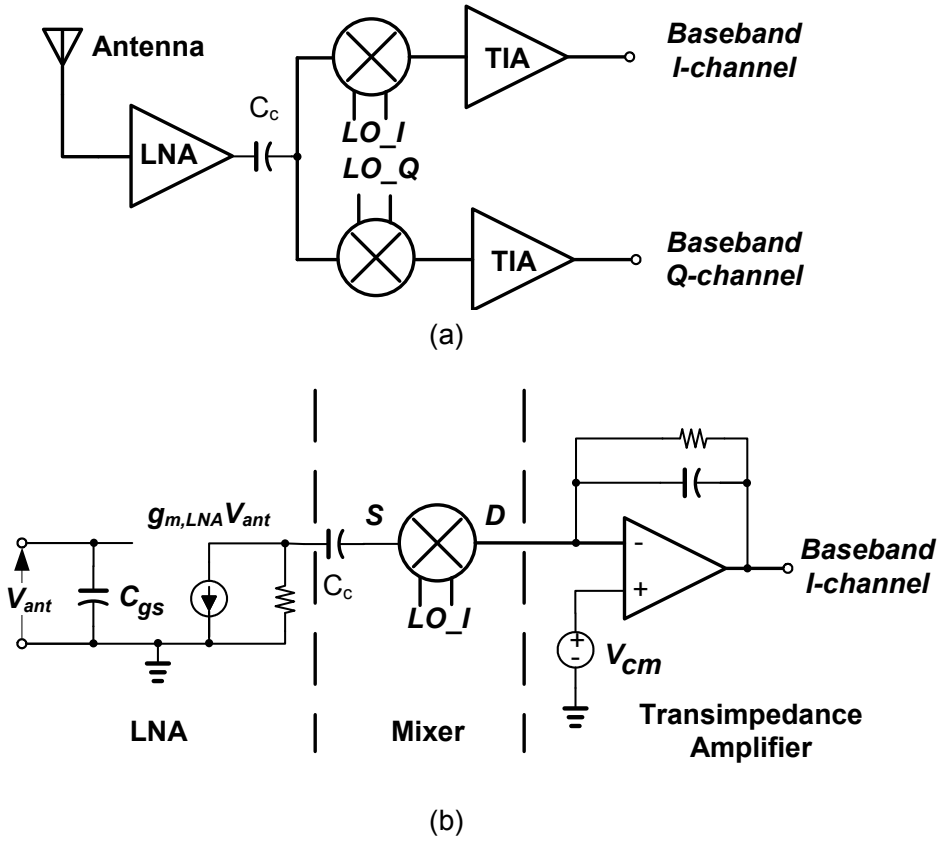


Figure 3.4: (a) Receiver block diagram, (c) Passive Mixer model, (d) Mixer MOS transistor model.

($\pm$100 mV). The third-order piecewise representation provides roughly 40 dB better estimation compared to a single power series representation of a much higher order.

3.3 Effect on Passive Mixer Linearity Simulation

Fig. 3.4(a) depicts a block diagram of a zero IF (ZIF) receiver. The low noise amplifier (LNA) acts as a transconductance stage and feeds the current to a current-commutating passive mixer. As we are concerned only with the mixer, Fig. 3.4(a) can be further simplified to Fig. 3.4(b) by replacing the LNA model with a current source i_{rf} and a shunt impedance, Z_S, and the TIA input with an impedance Z_L.

The primary sources of nonlinearity in a passive CMOS mixer driven by a square

wave LO are the

– non-zero rise and fall time of the LO,

– nonlinear C_{gs} and C_{gd},

– and the nonlinear I_D versus V_{DS} relationship.

At lower microwave frequencies, a square-wave LO can be faithfully achieved in an IC environment and hence, the contributions from the finite rise time and nonlinear capacitances are negligible for short gate length devices. Hence, the mixer nonlinearity is dominated by the nonlinear $I_D - V_{DS}$ relation. The mixer operation can be analyzed by expressing the mixer input and the output voltages as weakly nonlinear power series expanded about the periodically varying LO voltage [71]. The coefficients of the ensuing series are time-varying; however, for a low-frequency operation, the memory elements in the mixer and the load impedance can be ignored and the coefficients are assumed to be constants. Hence, the mixer linearity can be estimated from the simplified circuit of Fig. 3.4(d). The load impedance, Z_L, for a current commutating mixer is typically low due to the feedback of the baseband trans-impedance amplifier (TIA), while the mixer source impedance, Z_S, at the LNA output is relatively high.

For a two-tone intermodulation test, the current source can be expressed as,

$$i_{rf}(t) = A\cos(\omega_0 - \Delta\omega)t + A\cos(\omega_0 + \Delta\omega)t \tag{3.5}$$

As discussed in the previous section, for the MOSFET models that exhibit discontinuous even-order coefficient at $V_{DS} = 0$, the output voltage should be expressed as,

$$V_D(t) = \begin{cases} b_1 i_{rf}(t) + b_2 i_{rf}^2(t) + b_3 i_{rf}^3(t) & \text{if } V_{DS}(t) < 0, \\ b_1' i_{rf}(t) + b_2' i_{rf}^2(t) + b_3' i_{rf}^3(t) & \text{if } V_{DS}(t) \geq 0, \end{cases} \tag{3.6}$$

where, b_n and b_n' are constants dependent upon the transistor DC characteristics and the source and the load impedances. Assuming a high mixer linearity and assuming that the source impedance is much greater than $1/g_1$ and the load impedance combined, we can approximate $V_{DS}(t)$ as,

$$V_{DS}(t) \approx -\frac{i_{rf}(t)}{a_1}. \tag{3.7}$$

Hence, (3.6) can be rewritten as,

$$V_D(t) \approx \begin{cases} b_1 i_{rf}(t) + b_2 i_{rf}^2(t) + b_3 i_{rf}^3(t) & \text{if } i_{rf}(t) > 0, \\ b_1' i_{rf}(t) + b_2' i_{rf}^2(t) + b_3' i_{rf}^3(t) & \text{if } i_{rf}(t) \leq 0. \end{cases} \tag{3.8}$$

In this analysis, we find the fundamental and third-order intermodulation term of $V_D(t)$ by obtaining the contributions when $i_{rf}(t) > 0$ and $i_{rf}(t) < 0$ separately, and, then adding these contributions. We define the contribution from the positive half as,

$$\begin{aligned} V_D^+(t) &= \begin{cases} V_D(t) & \text{if } i_{rf}(t) > 0, \\ 0 & \text{if } i_{rf}(t) \leq 0, \end{cases} \\ &= V_D(t) \times SW^+(t), \end{aligned} \tag{3.9}$$

where, $SW^+(t)$ is a square wave defined as,

$$SW^+(t) = \begin{cases} 1 & \text{if } i_{rf}(t) > 0, \\ 0 & \text{if } i_{rf}(t) \leq 0. \end{cases} \tag{3.10}$$

Substituting from (3.5),

$$SW^+(t) = \begin{cases} 1 & \text{if } \Big[\cos{(\omega_0 - \Delta\omega)t} + \cos{(\omega_0 + \Delta\omega)t} \Big] > 0, \\ 0 & \text{otherwise.} \end{cases} \tag{3.11}$$

Noting that,

$$\cos{(\omega_0 - \Delta\omega)t} + \cos{(\omega_0 + \Delta\omega)t} = 2 \cos{\Delta\omega t} \cos{\omega_0 t}, \tag{3.12}$$

the threshold condition of (3.11) is satisfied when $\cos{\Delta\omega t}$ and $\cos{\omega_0 t}$ are either both positive or both negative. Consider another periodic square wave with angular frequency ω, defined as,

$$\begin{aligned} \Pi_\omega(t) &= \begin{cases} 1 & -\pi/2 \leq \omega t \leq \pi/2 \\ -1 & \pi/2 \leq \omega t \leq 3\pi/2. \end{cases} \\ &= \frac{4}{\pi} \Big(\cos{\omega t} - \frac{1}{3} \cos{3\omega t} + \frac{1}{5} \cos{5\omega t} - ... \Big) \end{aligned} \tag{3.13}$$

Note that $\Pi_{\omega}(t)$ has the same sign as $\cos\omega t$, and, hence, $\Pi_{\Delta\omega}(t)\Pi_{\omega_0}(t)$ has the same sign as $\cos\Delta\omega t\cos\omega_0 t$. Thus,

$$\Pi_{\Delta\omega}(t)\Pi_{\omega_0}(t) = \begin{cases} 1 & \cos\Delta\omega t\cos\omega_0 t > 0 \\ -1 & \cos\Delta\omega t\cos\omega_0 t < 0 \end{cases} \tag{3.14}$$

From (3.11), (3.12) and (3.14), we conclude that

$$SW^{+}(t) = \frac{1}{2}\Big\{1 + \Pi_{\Delta\omega}(t)\Pi_{\omega_0}(t)\Big\}. \tag{3.15}$$

Thus, the nonlinearity contribution due to the positive excursion of $i_{rf}(t)$ is,

$$V_D^{+}(t) = \sum_{n=1}^{3} b_n A\Big[\cos(\omega_0 - \Delta\omega)t + \cos(\omega_0 + \Delta\omega)t\Big]^n \times \frac{1}{2}\Big\{1 + SW_{\Delta\omega}(t)SW_{\omega_0}(t)\Big\} \tag{3.16}$$

The fundamental and the third-order intermodulation distortion (IMD_3) components can be calculated from the coefficients of $\cos(\omega_0 \pm \Delta\omega)t$ and $\cos(\omega_0 \pm 3\Delta\omega)t$ respectively in (3.16), i.e.

$$V_{1_D}^{+}(\omega_0 \pm \Delta\omega) = \frac{1}{2}b_1 A \tag{3.17a}$$

$$V_{3_D}^{+}(\omega_0 \pm 3\Delta\omega) = \frac{64}{45\pi^2}b_2 A^2 + \frac{3}{8}b_3 A^3 \tag{3.17b}$$

A similar analysis can be conducted for the negative half, and

$$V_D^{-}(\omega_0 \pm \Delta\omega) = \frac{1}{2}b_1' A \tag{3.18a}$$

$$V_D^{-}(\omega_0 \pm 3\Delta\omega) = -\frac{64}{45\pi^2}b_2' A^2 + \frac{3}{8}b_3' A^3 \tag{3.18b}$$

The combined fundamental and IMD_3 terms are obtained by combining (3.17) and (3.18), i.e.

$$V_D(\omega_0 \pm \Delta\omega) \approx \frac{1}{2}(b_1 + b_1')A \tag{3.19a}$$

$$V_D(\omega_0 \pm 3\Delta\omega) \approx \frac{64}{45\pi^2}(b_2 - b_2')A^2 + \frac{3}{8}(b_3 + b_3')A^3. \tag{3.19b}$$

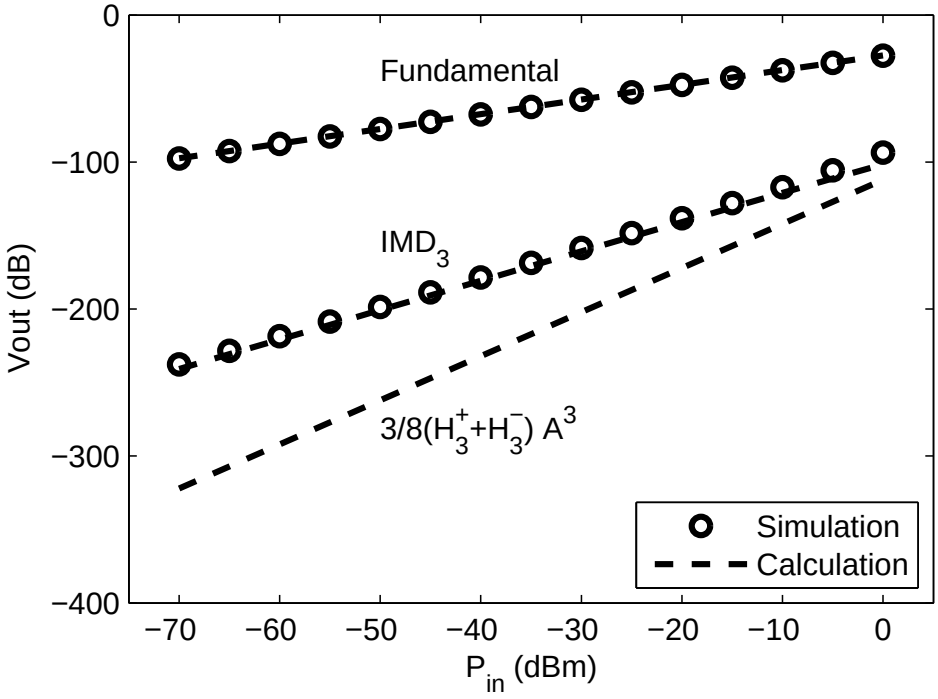


Figure 3.5: Comparison between simulated (using BSIM3v3 model) and calculated (from (3.20) fundamental and third-order distortion signals for a CMOS passive mixer driven by a square LO with input and output terminals biased at 0 V. P_{in} is the input power of the LNA with ($g_{m,LNA}$ = 30 mS) in Fig. 3.4(a). The mixer source and load impedances are 500 Ω and 5 Ω respectively and LO frequency is 1 MHz. The simulated third-order distortion has a predominant 2:1 slope. For comparison, the calculated third-order distortion from (3.20) with slope of 3:1 is also plotted.

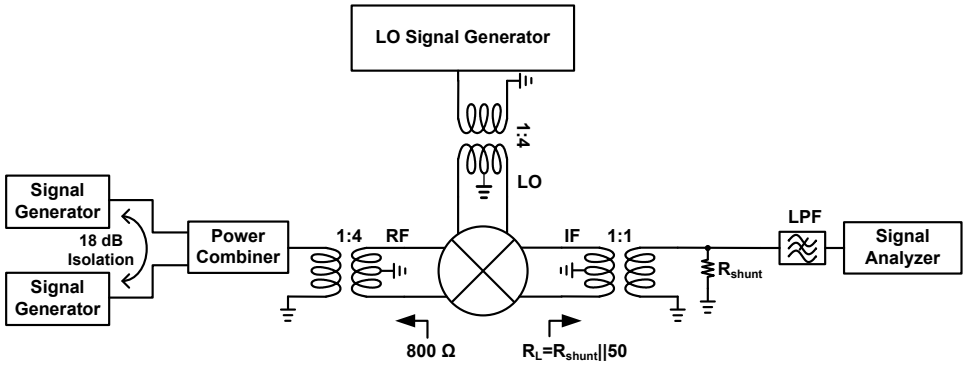


Figure 3.6: Passive mixer measurement setup.

Owing to the discontinuity in the second-order derivatives, the third-order intermodulation distortion becomes,

$$V_D(\omega_0 \pm 3\Delta\omega) \approx \frac{128}{45\pi^2} b_2 A^2 + \frac{3}{4} b_3 A^3. \tag{3.20}$$

The BSIM5 and PSP models use a single equation to define I_D in all regions, hence the coefficients are same in either region. Thus, in these cases

$$V_D(\omega_0 \pm 3\Delta\omega) = \frac{3}{4} b_3 A^3. \tag{3.21}$$

Eq. (3.20) reveals the contribution of the second-order nonlinearity to the third-order distortion. Fig. 3.5 shows the simulated (using BSIM3v3 model) and the calculated (from (3.19)) values for the fundamental and the third-order distortion of a passive mixer, demonstrating excellent agreement. At lower power levels, the second-order nonlinearity dominates IMD_3 simulation giving it a 2:1 slope with the input power. For comparison, the third-order term, $(3/4)b_3A^3$, from (3.21), with a 3:1 slope is also plotted.

3.4 Measurement Results

Measurements were conducted to verify these calculations with a double balanced passive MOSFET mixer fabricated in a CMOS Silicon-on-Insulator (SOI) tech-

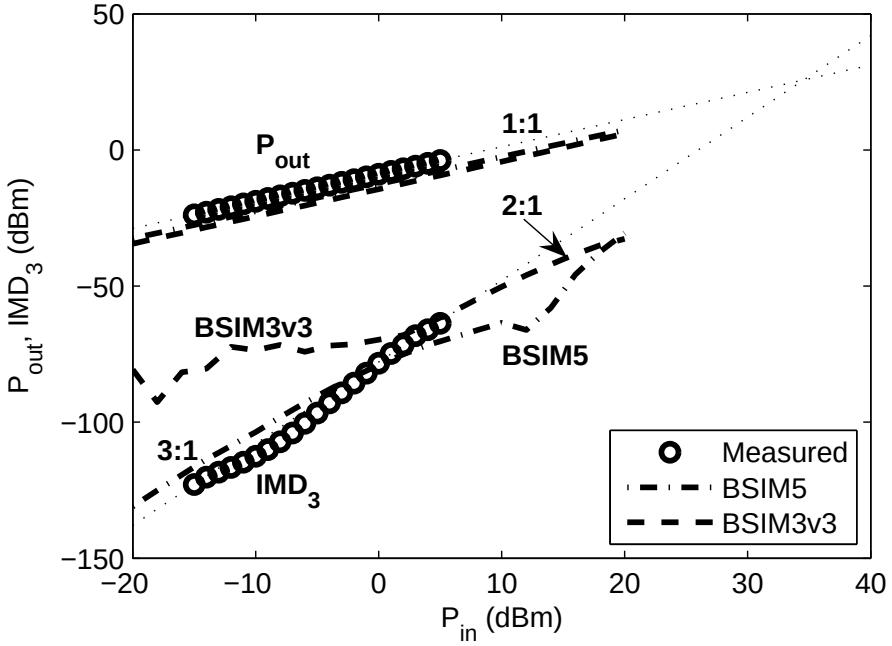


Figure 3.7: Measured and simulated (SpectreRF) fundamental and IMD_3 curves for the passive mixer with +15 dBm sinusoidal LO at 500 MHz. The downconverted fundamental tones were measured at 20 MHz and the third-order intermodulation distortion tone was measured at 500 kHz.

nology [72]. This technology uses an insulating substrate, which reduces the substrate losses and improves device performance.

Fig. 3.6 shows the measurement setup. The RF balun has a 1:4 turn ratio, which provides a high source impedance to the mixer. The two-tone spacing of 19.5 MHz was chosen to provide sufficient isolation and to minimize cross-talk between the signal generators. A low-pass filter is placed at the IF port to reject high-frequency signals. Fig. 3.7 shows the measured fundamental and IMD_3 curves for the passive MOSFET mixer driven by +15 dBm sinusoidal LO at 500 MHz. The measurement and simulations with BSIM5 model are in good agreement and have 3:1 slope for IMD_3, while, simulations with the BSIM3v3 model have a 2:1 slope for IMD_3 at higher power levels.

3.5 Conclusion

The linearity of a CMOS passive mixer was analyzed. In some models, the discontinuity in the second-order derivative of the drain-current leads to an erroneous slope of 2:1 for the third-order distortion. The mechanism behind this 2:1 slope was precisely identified. A passive mixer was measured to confirm the slope of 3:1 for IMD_3, and excellent agreement between theory and measurement was obtained. This chapter has been published in part in the following publication:

1. H. Khatri, P. S. Gudem, and L. E. Larson, "Simulation of intermodulation distortion in passive CMOS FET mixers," in *Proc. IEEE MTT-S Intl. Microw. Symp.*, IMS, June 2009.

Chapter 4

Passive CMOS Mixer Linearity Analysis

4.1 Introduction

Downconverting mixers are an indispensable part of any modern communication receiver. Active Gilbert mixers have been the mainstay of integrated receiver systems, due to their superior gain performance. However, they suffer from voltage headroom limitations and high flicker noise, as technologies scale to sub-100 nanometers. These drawbacks pose serious challenges in a direct conversion receiver (DCR) design. Despite higher conversion losses, current commutating passive CMOS mixers are preferred in integrated DCR designs, due to their modest headroom requirements and excellent flicker noise performance [73, 74, 62]. Several detailed studies have been undertaken to address passive mixer design concerns, such as noise, dc offset, and second-order distortion [60, 61, 62, 75, 76]. However, little has been published on the fundamental nonlinear behavior of these current-commutating passive mixers.

An analysis of the intermodulation distortion of current commutating CMOS *active* mixers was presented in [77]. A distortion analysis of MOS track-and-hold sampling mixers involving a time-varying Volterra series analysis was presented in [78]. These analyses cannot be directly applied to current commutating passive mixers, since the transistors in passive mixers are biased in deep triode, and the later case assumes

voltage commutation (i.e. a high load impedance) and does not account for the effects of source and load impedances.

High linearity passive mixers are crucial for successful design of CDMA receivers without the interstage RF filter between the LNA and the mixer. In these receivers, the transmitter signal leaking into the receiver cross-modulates with a close-in jammer to produce in-band distortion [1]. It is shown in this chapter that the mixer linearity is significantly affected by its source and load impedances. We have developed a general distortion theory of current commutating passive FET mixers and establish the relationship between mixer IIP_2, two-tone IIP_3 and cross-modulation IIP_3, and its frequency dependent source and load impedances.

Section 4.2 presents the mixer modeling for distortion analysis using a Volterra series, which is presented in Section 4.3. The effects of frequency-varying mixer source and load impedances are analyzed in Section 4.4. High-frequency effects arising from the transistor capacitances and LO feedthrough are discussed in Section 4.5. The paper concludes in Section 4.6 with measurement results that confirm the theory.

4.2 Mixer Modeling

4.2.1 Device Modeling

A typical monolithic direct conversion receiver block diagram is shown in Fig. 4.1(a). As shown in Fig. 4.1(b), the low-noise amplifier (LNA) can be modeled as a transconductance stage feeding its output current into the passive mixer. The mixer output current drives the transimpedance amplifier (TIA), which generates the baseband output voltage. Typically, the common-mode feedback loop of the TIA provides the DC bias (V_{CM}) to the input and output terminals of the mixer. Due to the AC coupling capacitor (C_c) between the LNA output and the mixer input, the transistors in the mixer are biased in deep triode region with $V_{DS} = 0$. We assume that the transistor gates are driven by an ideal square wave local oscillator (LO) signal.

Due to symmetric dependence of the drain current, I_D, either of the terminals can be assumed to be the drain or the source [79]. Hence, without loss of generality, we

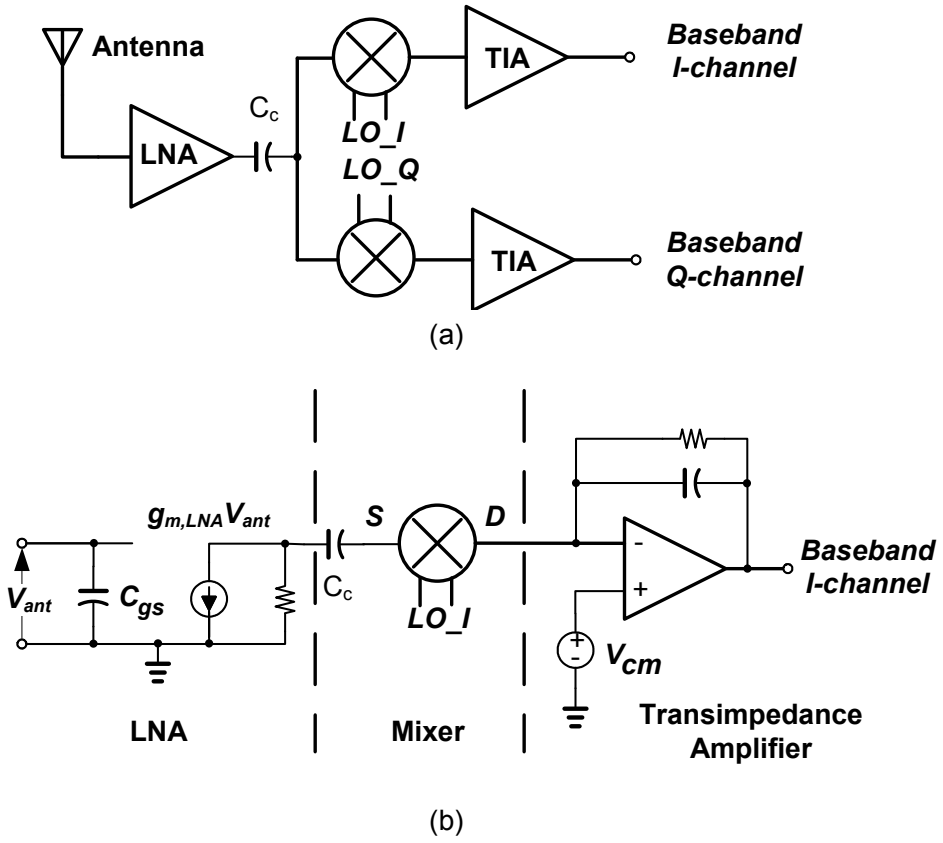


Figure 4.1: (a) Receiver block diagram, (b) Simplified receiver model.

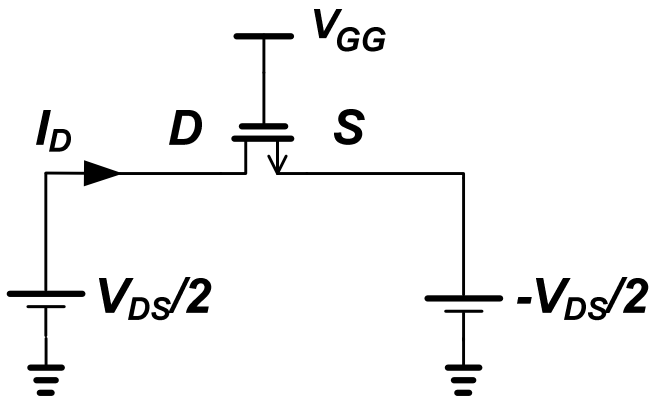


Figure 4.2: Schematic for DC analysis of an NMOS transistor.

assume the input node to be the source, S, and the output node to be the drain, D. It is crucial to choose a correct MOS model for analyzing the passive mixer nonlinearity. At the V_{DS}=0 bias, the industry standard models like BSIM3v3, BSIM4, Philips MM9 and EKV models deviate from the measured results, due to discontinuities in the higher-order derivatives of drain current and terminal charges [63,64,65,66]. The latest surface potential-based model, PSP [68] and the next generation BSIM model, BSIM5 [69, 70] use a single equation to define the drain current across all biasing conditions and have continuous first and higher derivatives.

The models are typically tested for Gummel Symmetry [80], where, equal and opposite voltages are applied at the source and drain terminals of MOSFET and drain current is measured (Fig. 4.2). The drain current and its first, second and third-order derivatives with respect to V_{DS} are plotted in Fig. 4.3 for BSIM3v3 and PSP models. The second-order derivative of I_D shows discontinuity at $V_{DS} = 0$ and this has been asserted as the reason behind the anomalous third-order distortion slope of 2:1, instead of 3:1, in passive mixer simulations [67, 81]. Hence, the PSP model was chosen for the simulation results presented in this chapter.

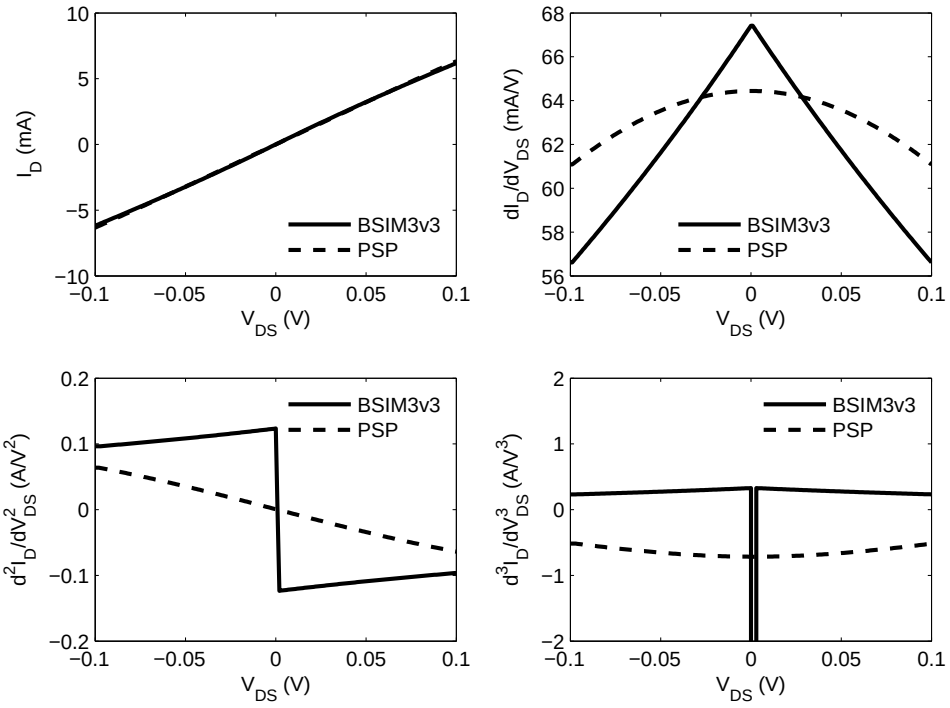


Figure 4.3: I_D and first three derivatives with respect to V_{DS} for a MOSFET transistor simulated with BSIM3v3 and PSP models. The source and drain voltages are equal and opposite (Fig. 4.2). V_{GG} = 1.5 V and the transistor size is 50 μm/0.18 μm.

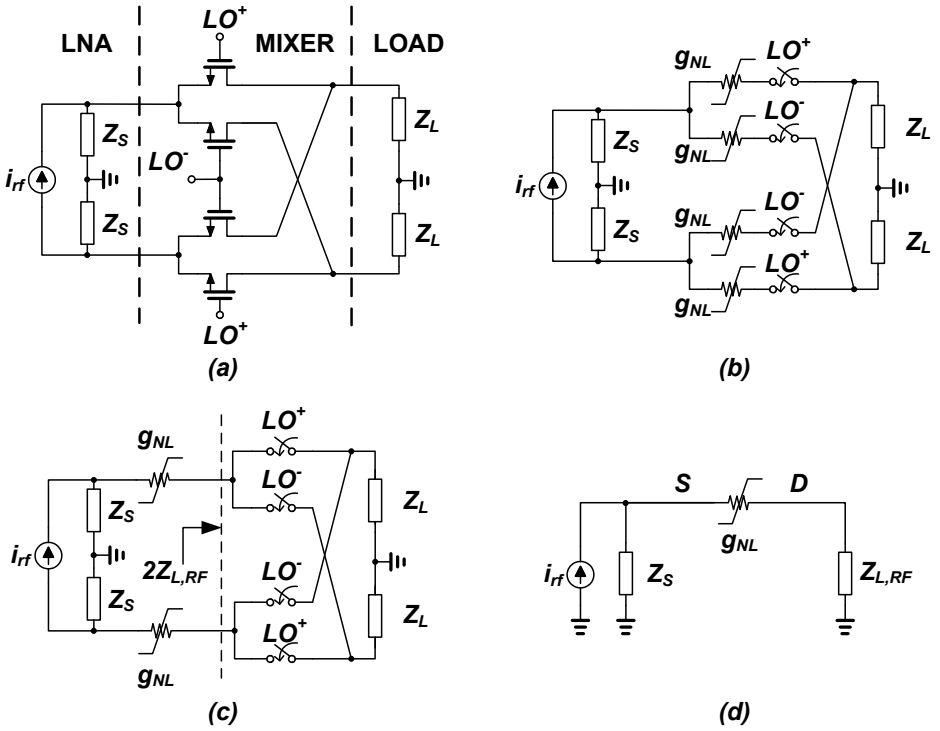


Figure 4.4: (a) A double-balanced passiver MOSFET mixer. (b) Passive FET mixer with transistors modeled as non-linear conductances and ideal switches. (c) Simplified model of (b) for non-overlapping LO^+ and LO^- and real load impedance. (d) Single-ended equivalent model of the mixer.

4.2.2 Nonlinearity Modeling

The primary sources of nonlinearity in a passive CMOS mixer driven by a square-wave LO are the

– non-zero rise and fall time of the LO,

– nonlinear device capacitances; C_{gs} and C_{gd},

– and, the nonlinear I_D versus V_{DS} relationship.

At lower microwave frequencies, a square-wave LO can be faithfully achieved in an IC environment and hence, the contributions from the finite rise time and nonlinear capacitances are negligible for short gate length devices. Those sources have been initially ignored; but at higher frequencies, these effects can be non-negligible and their impact is discussed later in Section 4.5. The receiver model in Fig. 4.1(b) can be further simplified to Fig. 4.4(a). The double-balanced passive mixer is assumed to be driven by

an ideal square wave LO with a fifty-percent duty cycle. The LNA output is modeled as an ideal current source, i_{RF}, shunted by impedance Z_S, which acts as a signal source for the mixer. Similarly, the TIA input is represented by the load impedance Z_L. In practice, the LNA load is typically a shunt LC tank terminated at V_{DD}, and the output buffer of the TIA provides the ground termination to Z_L, hence a common-mode ground is justified. Additional differential capacitances at the mixer output (not shown here) filters off the high frequency signals and have been ignored in this analysis, as they do not affect the signal and the intermodulation distortion tones.

The mixer operation can be analyzed by expressing the mixer input and output voltages as weakly nonlinear Volterra series expanded about the periodically varying LO voltage [71]. The series coefficients are time-varying; however, for low-frequency operation relative to the f_t of the transistor, the memory elements in the mixer and the load impedance can be ignored and the coefficients are assumed to be constants. Each transistor can be modeled as a nonlinear transconductance, g_{NL}, in series with an ideal switch as shown in Fig. 4.4(b). Assuming no device mismatches and non-overlapping LO waveforms, the circuit can be further simplified to Fig. 4.4(c), where, $Z_{L,RF}$ refers to the load impedance Z_L transformed into the RF domain. The relationship between $Z_{L,RF}$ and Z_L is developed later in Section 4.4. Due to its symmetry, the circuit can be further simplified to its single-ended version in Fig. 4.4(d).

4.3 Mixer Linearity Analysis

In general, the large signal drain current, i_D, is a function of the drain and the source voltages referred to the bulk, rather than the large-signal drain-source voltage, v_{DS}. Hence, i_D can be expressed as,

$$\begin{aligned} i_D = {} & g_1 v_D + g_{2_D} v_D^2 + g_{3_D} v_D^3 + \dots \\ & - g_1 v_S + g_{2_S} v_S^2 + g_{3_S} v_S^3 + \dots \\ & + g_{2_{D\&S}} v_D v_S + g_{3_{2D\&S}} v_D^2 v_S + g_{3_{D\&2S}} v_D v_S^2 + \dots, \end{aligned} \tag{4.1}$$

where, v_D and v_S are the large-signal drain and source voltages of the MOSFET referred to the bulk respectively. By symmetry, the coefficients of v_D and v_S are equal and

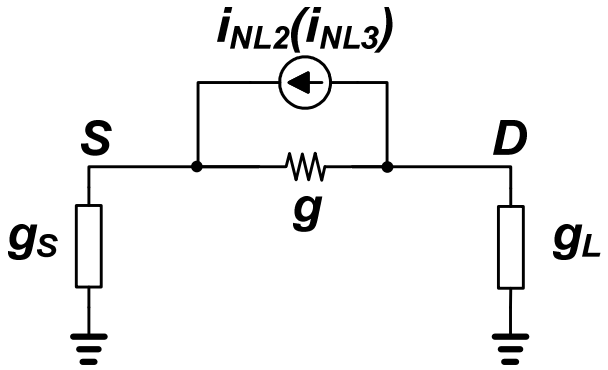


Figure 4.5: Schematic for computation of the second (and third) order Volterra kernels.

opposite. All the coefficients in (4.1) depend on the process technology, the gate bias voltage and the transistor size. Assuming g_{NL} to be a weakly nonlinear conductance, fourth and higher-order terms in (4.1) have been ignored. Hence, in Fig. 4.4(d), the input and the output voltages can be expressed as a converging Volterra series of the source current, i_{RF}. Thus,

$$\begin{aligned} v_S = {} & H_{1_S}(s) \circ i_{RF} + H_{2_S}(s_1, s_2) \circ i_{RF}^2 \\ & + H_{3_S}(s_1, s_2, s_3) \circ i_{RF}^3 + \dots \end{aligned} \tag{4.2a}$$

$$\begin{aligned} v_D = {} & H_{1_D}(s) \circ i_{RF} + H_{2_D}(s_1, s_2) \circ i_{RF}^2 \\ & + H_{3_D}(s_1, s_2, s_3) \circ i_{RF}^3 + \dots \end{aligned} \tag{4.2b}$$

where, H_{n_S} and H_{n_D} are the n^{th}-order Volterra kernels for the input and the output nodes respectively. The first-order Volterra kernels are,

$$H_{1_S}(s) = \frac{g_1 + g_L(s)}{\Delta(s)}, \tag{4.3a}$$

$$H_{1_D}(s) = \frac{2}{\pi}\frac{g_1}{\Delta(s)}, \tag{4.3b}$$

where,

$$\Delta(s) = g_1 g_S(s) + g_S(s) g_L(s) + g_L(s) g_1, \tag{4.4}$$

and the $2/\pi$ factor is added to $H_{1_D}(s)$ to account for the double-balanced mixer gain. The second-order Volterra kernels can be obtained by solving for the node voltages in

Fig. 4.5. The nonlinear current source, i_{NL2}, is a function of the first-order Volterra kernels [82], and is given by

$$i_{NL2} = \frac{1}{\Delta(s_1)\Delta(s_2)} \Bigg\{ g_{2_D} g_1^2 + g_{2_S} \Big(g_1 + g_L(s_1) \Big) \Big(g_1 + g_L(s_2) \Big) + g_{2_{D\&S}} g_1 \left(g_1 + \frac{g_L(s_1) + g_L(s_2)}{2} \right) \Bigg\} \tag{4.5}$$

Solving the circuit in Fig. 4.5 yields,

$$H_{2_S}(s_1, s_2) = \frac{g_L(s_1 + s_2)}{\Delta(s_1 + s_2)} i_{NL2}(s_1, s_2), \tag{4.6a}$$

$$H_{2_D}(s_1, s_2) = -\frac{2}{\pi} \frac{g_S(s_1 + s_2)}{\Delta(s_1 + s_2)} i_{NL2}(s_1, s_2). \tag{4.6b}$$

In a similar fashion, the third-order nonlinear current can be computed with i_{NL3} as the current source. The third-order Volterra kernels are,

$$H_{3_S}(s_1, s_2, s_3) = \frac{g_L(s_1 + s_2 + s_3)}{\Delta(s_1 + s_2 + s_3)} i_{NL3}(s_1, s_2, s_3), \tag{4.7a}$$

$$H_{3_D}(s_1, s_2, s_3) = -\frac{2}{\pi} \frac{g_S(s_1 + s_2 + s_3)}{\Delta(s_1 + s_2 + s_3)} i_{NL3}(s_1, s_2, s_3). \tag{4.7b}$$

i_{NL3} can be computed from lower-order Volterra kernels as outlined in [82].

4.3.1 IIP$_2$ and IIP$_3$

For two input signals at frequencies ω_1 and ω_2, the second-order input intercept point, IIP$_2$, refers to the input power when the output power due to second-order intermodulation distortion, $P_{out}(\omega_1 - \omega_2)$, equals the fundamental output power, $P_{out}(\omega_{LO} - \omega_1)$. Analytically,

$$\begin{aligned} IIP_2 &= \frac{P_{out}(\omega_{LO} - \omega_1)}{P_{out}(\omega_1 - \omega_2)} P_{in}(\omega_1) \\ &= \left\{ \frac{v_D(\omega_{LO} - \omega_1)}{v_D(\omega_1 - \omega_2)} \right\}^2 P_{in}(\omega_1) \end{aligned} \tag{4.8}$$

where, P_{in} is the input power. Similarly, the third-order intermodulation distortion due to two tones at ω_1 and ω_2, appears at $2\omega_1 - \omega_2$. For this downconverter, it can be

expressed as,

$$IIP_3 = \left\{ \frac{P_{out}(\omega_{LO} - \omega_1)}{P_{out}(\omega_{LO} - (2\omega_1 - \omega_2))} \right\}^{\frac{1}{2}} P_{in}(\omega_1)$$
$$= \frac{v_D(\omega_{LO} - \omega_1)}{v_D(\omega_{LO} - (2\omega_1 - \omega_2))} P_{in}(\omega_1) \tag{4.9}$$

The single-ended fundamental, second-order and third-order intermodulation distortion voltages at the mixer output can be evaluated as,

$$v_D(s_{LO} - s_1) = H_{1_D}(s_1) i_{RF}(s_1) \tag{4.10a}$$
$$v_D(s_1 - s_2) = H_{2_D}(s_1, -s_2) i^2_{RF}(s_1, s_2) \tag{4.10b}$$
$$v_D(s_{LO} - (2s_1 - s_2)) = \frac{3}{4} H_{3_D}(s_1, s_1, -s_2) i^3_{RF}(s_1, s_1, -s_2) \tag{4.10c}$$

Keeping in mind that $|Z_S|$ is typically much greater than both $1/g_1$ and $|Z_{L,RF}|$, we can therefore assume that,

$$g_S(s_1), g_S(s_1 - s_2), g_S(2s_1) \ll g_L(s_1), \tag{4.11a}$$
$$g_L(-s_2) \approx g_L(s_1), \tag{4.11b}$$
$$\Delta(s_i) \approx g_1 g_L(s_i), \tag{4.11c}$$

and the simplified expressions for H_{2_D} and H_{3_D} are given by,

$$H_{2_D}(\omega_1, -\omega_2) \approx -\frac{g_S(\omega_1 - \omega_2)}{g^2_L(\omega_1) g_L(\omega_1 - \omega_2)} \times$$
$$\Big[A_2 g^2_L(\omega_1) + A_1 g_L(\omega_1) + A_0 \Big], \tag{4.12a}$$
$$H_{3_D}(\omega_1, \omega_1, -\omega_2) \approx -\frac{2}{\pi} \frac{g_S(2\omega_1 - \omega_2)}{g^5_1 g^3_L(\omega_1) g_L(2\omega_1 - \omega_2)} \times$$
$$\Big[B_3 g^3_L(\omega_1) + B_2 g^2_L(\omega_1) + B_1 g_L(\omega_1) + B_0 \Big], \tag{4.12b}$$

The coefficients for the second-order Volterra kernel of the drain voltage in (4.12a) are given by,

$$A_2 = g_{2_S}/g^3_1 \tag{4.13a}$$
$$A_1 = (g_{2D\&S} + 2g_{2_D})/g^2_1 \tag{4.13b}$$
$$A_0 = (g_{2_D} + g_{2D\&S} + g_{2_S})/g_1, \tag{4.13c}$$

and, the coefficients for the third-order Volterra kernel of the drain voltage in (4.12b) are given by,

$$B_3 = 2g_{2_S}^2 + gg_{3_S} \tag{4.14a}$$

$$B_2 = g_1(3g_{2_{D\&S}}g_{2_S} + 6g_{2_S}^2 + g_1g_{3_{D\&2S}} + 3g_1g_{3_S}) \tag{4.14b}$$

$$\begin{aligned} B_1 = g_1^2(&g_{2_{D\&S}}^2 + 2g_{2_D}g_{2_S} + 6g_{2_{D\&S}}g_{2_S} \\ &+ 6g_{2_S}^2 + 2g_1g_{3_{D\&2S}} + g_1g_{3_{2D\&S}} + 3g_1g_{3_S}) \end{aligned} \tag{4.14c}$$

$$\begin{aligned} B_0 = g_1^3(&g_{2_D}g_{2_{D\&S}} + g_{2_{D\&S}}^2 + 2g_{2_D}g_{2_S} + 3g_{2_{D\&S}}g_{2_S} \\ &+ 2g_{2_S}^2 + g_1(g_{3_D} + g_{3_{D\&2S}} + g_{3_{2D\&S}} + g_{3_S})) \end{aligned} \tag{4.14d}$$

The coefficients for the Volterra kernel for the cross-modulation distortion in (4.22) are given by

$$C_3 = 3(2g_{2_S}^2 + g_1g_{3_S}) \tag{4.15a}$$

$$C_2 = g_1(3g_{2_{D\&S}}g_{2_S} + 6g_{2_S}^2 + g_1g_{3_{D\&2S}} + 3g_1g_{3_S}) \tag{4.15b}$$

$$\begin{aligned} C_1 = g_1^2(&g_{2_{D\&S}}^2 + 2g_{2_D}g_{2_S} + 6g_{2_{D\&S}}g_{2_S} + 6g_{2_S}^2 \\ &+ 2g_1g_{3_{D\&2S}} + g_1g_{3_{2D\&S}} + 3g_1g_{3_S}) \end{aligned} \tag{4.15c}$$

$$\begin{aligned} C_0 = 3g_1^3(&g_{2_D}g_{2_{D\&S}} + g_{2_{D\&S}}^2 + 2g_{2_D}g_{2_S} + 3g_{2_{D\&S}}g_{2_S} \\ &+ 2g_{2_S}^2 + g_1g_{3_D} + g_1g_{3_{D\&2S}} + g_1g_{3_{2D\&S}} + g_1g_{3_S}) \end{aligned} \tag{4.15d}$$

For verification, the circuit in Fig. 4.4(a) is simulated and the single-ended fundamental, IMD_2 and IMD_3 components of the mixer output voltage are compared with the calculated values. As we have assumed low frequency operation, all the simulation were carried out at LO frequency of 1 MHz to show the excellent agreement with the calculations. Later, in Fig. 4.13 mixer single-ended IIP_2 and IIP_3 are plotted against frequency to show that there is less than 3 dB variation up to 1 GHz. The device parameters in (4.1) are estimated from the DC analysis using the technique described in Appendix A. Fig. 4.6 shows an excellent agreement between the simulation and the calculation.

For the differential operation, the fundamental and the third-order voltages will

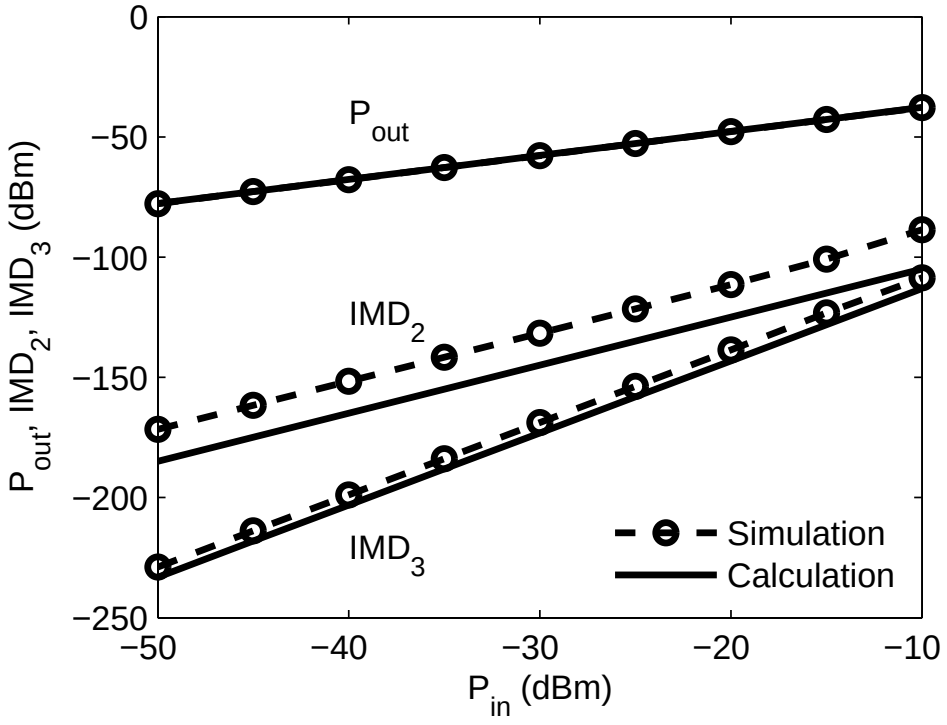


Figure 4.6: Comparison between simulated (using PSP model) and calculated (using (4.10)) single-ended fundamental, second-order and third-order intermodulation distortion signals for the mixer operated at low frequencies. P_{in} is the input to the LNA with $g_{m,LNA}$ = 30 mS in Fig. 4.1(a). The mixer source and load impedances are 500 Ω and 5 Ω respectively.

be doubled, while the second-order voltage will cancel and can be represented as,

$$v_D(\omega_1-\omega_2) = -\frac{g_S(\omega_1-\omega_2)}{g_L^2(\omega_1)g_L(\omega_1-\omega_2)}\times \left[\Delta_2 g_L^2(\omega_1)+\Delta_1 g_L(\omega_1)+\Delta_0\right] i_{RF}^2(s_1,s_2), \tag{4.16}$$

where, Δ_n's are the differences between A_n's for the positive and negative output terminals. This difference can be non-zero due to the mismatches and imbalances in the mixer and LO circuitry and signals. In an ideal case with no mismatches, Δ_n's are zero, resulting in zero $v_D(\omega_1-\omega_2)$ and infinite IIP_2.

Assuming a 50 Ω match at the LNA input in Fig. 4.1(a), the LNA input power can be expressed as

$$P_{in} = \frac{i_{RF}^2}{50 g_{m,LNA}^2}. \tag{4.17}$$

Thus, the second-order and third-order input intercept points are given by,

$$\begin{aligned} IIP_2(W) &= \left\{\frac{v_D(\omega_{LO}-\omega_1)}{v_D(\omega_1-\omega_2)}\right\}^2 \frac{i_{RF}^2}{50 g_{m,LNA}^2} \\ &\approx \frac{1}{50 g_{m,LNA}^2}\times\left\{\frac{g_L(\omega_1)g_L(\omega_1-\omega_2)}{g_S(\omega_1-\omega_2)}\right\}^2\times \\ &\quad \left[\Delta_2 g_L^2(\omega_1)+\Delta_1 g_L(\omega_1)+\Delta_0\right]^{-2} \end{aligned} \tag{4.18a}$$

$$\begin{aligned} IIP_3(W) &= \frac{v_D(\omega_{LO}-\omega_1)}{v_D(\omega_{LO}-(2\omega_1-\omega_2))}\frac{i_{RF}^2}{50 g_{m,LNA}^2} \\ &\approx \frac{2}{75 g_{m,LNA}^2}\times\frac{g_1^5 g_L^2(\omega_1)g_L(2\omega_1-\omega_2)}{g_S(2\omega_1-\omega_2)}\times \\ &\quad \left[B_3 g_L^3(\omega_1)+B_2 g_L^2(\omega_1)+B_1 g_L(\omega_1)+B_0\right]^{-1} \end{aligned} \tag{4.18b}$$

4.3.2 Cross-modulation (XM) IIP_3

The cross-modulation distortion is the most significant distortion mechanism in CDMA receivers, where the modulated transmitter (TX) signal in the receiver path cross-modulates with a close-in jammer to produce in-band distortion [1]. This can be modeled by representing the close-in jammer as a single tone at ω_1 and the modulated

TX signal as two closely spaced tones at ω_2 and ω_3; the distortion being at $\omega_1+\omega_2-\omega_3$. Let the IIP$_3$ due to these three tones be defined as,

$$\begin{aligned} IIP_{3,XM}(W) &= K_{XM}P_{in}(\omega_1)\times \\ &\quad \left\{\frac{P_{out}(\omega_{LO}-\omega_1)}{P_{out}(\omega_{LO}-(\omega_1+\omega_2-\omega_3))}\right\}^{\frac{1}{2}} \\ &= K_{XM}\frac{v_D(\omega_{LO}-\omega_1)}{v_D(\omega_{LO}-(\omega_1+\omega_2-\omega_3))}P_{in}(\omega_1) \end{aligned} \tag{4.19}$$

where, K_{XM} is a constant dependent on the spectral shape of the modulated signal [1]. The distortion voltage, $v_D(\omega_{LO}-(\omega_1+\omega_2-\omega_3))$, relates to the third-order Volterra kernel as,

$$\begin{aligned} v_D(\omega_{LO}-(\omega_1+\omega_2-\omega_3)) = \frac{3}{2}H_{3_D}(\omega_1,\omega_2,-\omega_3)\times \\ i^3_{RF}(\omega_1,\omega_2,-\omega_3). \end{aligned} \tag{4.20}$$

$H_{3_D}(\omega_1,\omega_2,-\omega_3)$ can be simplified by assuming (4.11) in addition to,

$$g_L(-\omega_3) \approx g_L(\omega_2) \tag{4.21a}$$

$$g_L(\omega_1+\omega_2) \approx \infty \tag{4.21b}$$

$$g_L(\omega_1-\omega_3) \approx \infty \tag{4.21c}$$

$$g_L(\omega_2-\omega_3) \approx \infty \tag{4.21d}$$

Equation (4.21a) is justified, since ω_2 and ω_3 are close together and the load impedance is assumed to be real. While, (4.21b)-(4.21d) imply that the load impedance at high frequency is assumed to be zero, which is justified due to large filtering capacitances at the mixer output. The simplified $H_{3_D}(\omega_1,\omega_2,-\omega_3)$ is given by,

$$\begin{aligned} H_{3_D}(\omega_1,\omega_2,-\omega_3) \approx \frac{g_S(\omega_1+\omega_2-\omega_3)}{3g_1^5 g_L(\omega_1)g_L^2(\omega_2)g_L(\omega_1+\omega_2-\omega_3)} \\ \Big[C_3 g_L(\omega_1)g_L^2(\omega_2) + C_2 g_L(\omega_1)\{g_L(\omega_2)+2g_L(\omega_1)\} \\ + C_1\{g_L(\omega_2)+2g_L(\omega_1)\} + C_0\Big] \end{aligned} \tag{4.22}$$

where, the C_n's, as defined in (4.15), are independent of the source and load impedances. Equation (4.23) gives the intercept point for the cross-modulation distortion.

$$IIP_{3,XM} \approx \frac{K_{XM}}{25 g_{m,LNA}} \frac{g_1^5 g_L^2(\omega_2) g_L(\omega_1+\omega_2-\omega_3)}{g_S(\omega_1+\omega_2-\omega_3)} \times \Big[C_3 g_L(\omega_1) g_L^2(\omega_2) + C_2 g_L(\omega_1)\{g_L(\omega_2)+2g_L(\omega_1)\} + C_1\{g_L(\omega_2)+2g_L(\omega_1)\} + C_0 \Big]^{-1} \tag{4.23}$$

4.4 Effect of Source and Load Impedances on Mixer Linearity

4.4.1 Computation of Mixer Input Impedance

$Z_{L,RF}$ is the input impedance of an ideal passive mixer with load impedance Z_L, as shown in Fig. 4.7(a). For this analysis, the mixer is driven by an ideal square wave LO with frequency ω_{LO} and i_{test} is an ideal single tone current source with amplitude A and frequency ω_{in}. The current at the load is given by multiplying the i_{test} with a periodic square wave function, f_{sw}. Analytically,

$$i_{test}(t) = A\cos\omega_{in}t, \tag{4.24}$$

$$f_{sw}(t) = \frac{4}{\pi}\sum_{n=1,3,5\ldots}^{\infty}\frac{1}{n}\sin n\omega_{LO}t \tag{4.25}$$

$$\begin{aligned} i_{out}(t) &= i_{test}(t) f_{sw}(t) \\ &= \frac{2A}{\pi}\sum_{n=1,3,5\ldots}^{\infty}\frac{1}{n}\Big(\sin(n\omega_{LO}+\omega_{in})t + \sin(n\omega_{LO}-\omega_{in})t\Big) \end{aligned} \tag{4.26}$$

The output voltage, $v_{out}(t)$, across nodes O^+ and O^-, can be computed as the product of $i_{out}(t)$ and $2Z_L(\omega)$.

$$v_{out}(t) = \frac{2A}{\pi}\sum_{n=1,3,5\ldots}^{\infty}\frac{1}{n}\times \Big[2|Z_L(n\omega_{LO}+\omega_{in})|\sin((n\omega_{LO}+\omega_{in})t+\theta_1) + 2|Z_L(n\omega_{LO}-\omega_{in})|\sin((n\omega_{LO}-\omega_{in})t+\theta_2)\Big], \tag{4.27}$$

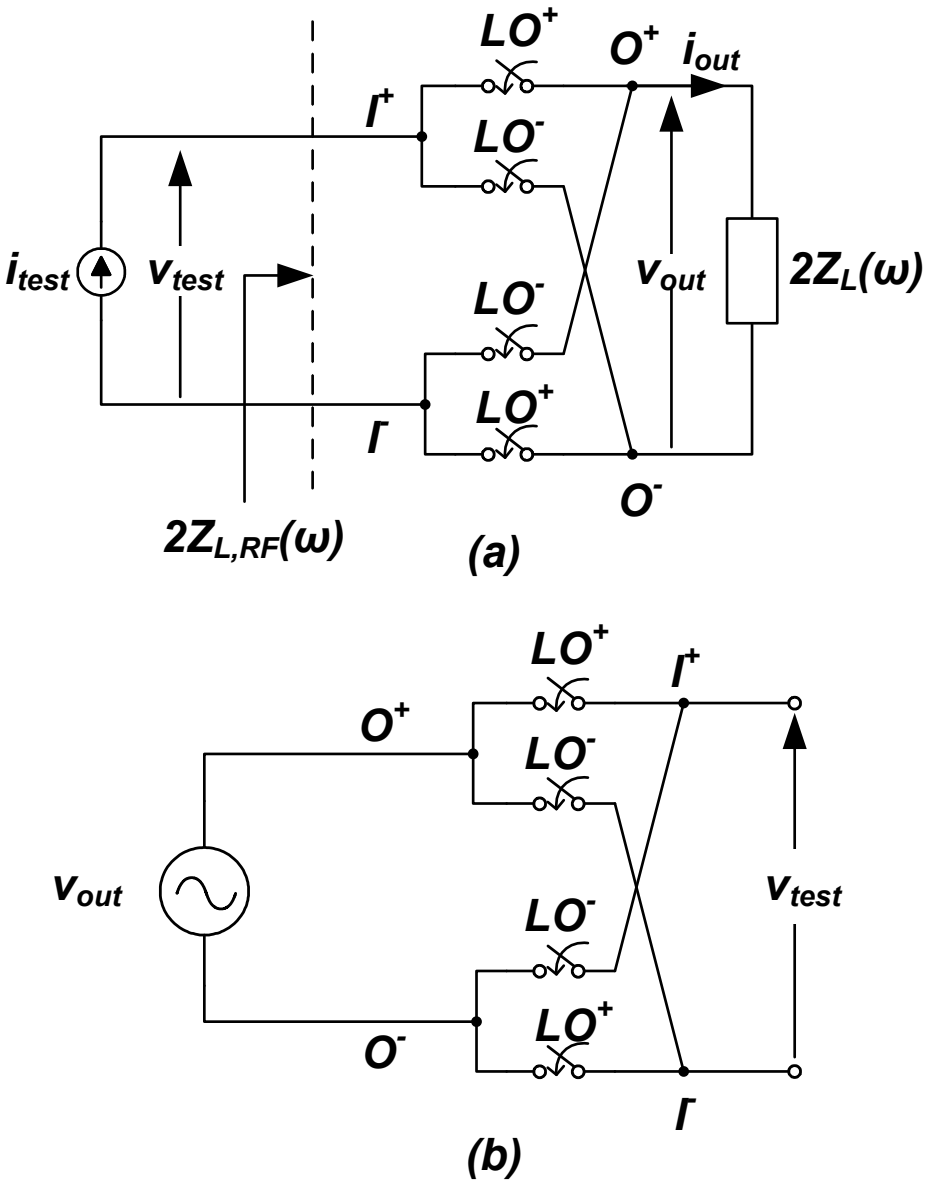


Figure 4.7: (a) Ideal current commutating mixer schematic with current source and load impedance. (b) The same mixer acts as an ideal voltage commutating mixer having open load with voltage v_{test} across it.

where, θ_1 and θ_2 are arguments of $Z_L(n\omega_{LO}+\omega_{in})$ and $Z_L(n\omega_{LO}-\omega_{in})$ respectively. The same mixer can be envisaged as a voltage commutator with $v_{out}(t)$ as the source voltage and $v_{test}(t)$ as the voltage across the open load (Fig. 4.7(b)). Hence,

$$\begin{aligned}
&v_{test}(t) = v_{out}(t) f_{sw}(t) \\
&= \frac{4A}{\pi^2} \sum_{n=1,3,5\ldots}^{\infty} \sum_{m=1,3,5\ldots}^{\infty} \frac{1}{nm} \times \\
&\Big[2|Z_L(n\omega_{LO}+\omega_{in})| \cos(((n-m)\omega_{LO}+\omega_{in})t+\theta_1) \\
&- 2|Z_L(n\omega_{LO}+\omega_{in})| \cos(((n+m)\omega_{LO}+\omega_{in})t+\theta_1) \\
&+ 2|Z_L(n\omega_{LO}-\omega_{in})| \cos(((n-m)\omega_{LO}-\omega_{in})t+\theta_2) \\
&- 2|Z_L(n\omega_{LO}-\omega_{in})| \cos(((n+m)\omega_{LO}-\omega_{in})t+\theta_2) \Big]
\end{aligned} \tag{4.28}$$

Using an approach similar to the conversion matrix approach [83], the input impedance, $Z_{L,RF}$ can be computed by finding the coefficient of $\cos\omega_{in}t$ in (4.28), which is given by,

$$\begin{aligned}
Z_{L,RF} &= \frac{4}{\pi^2} \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n^2} \Big[|Z_L(n\omega_{LO}+\omega_{in})| e^{j\theta_1} + |Z_L(n\omega_{LO}-\omega_{in})| e^{-j\theta_2} \Big] \\
&= \frac{4}{\pi^2} \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n^2} \Big[Z_L(n\omega_{LO}+\omega_{in}) + Z_L^*(n\omega_{LO}-\omega_{in}) \Big],
\end{aligned} \tag{4.29}$$

For a resistive load, R_L, this results in

$$\begin{aligned}
Z_{L,RF} &= \frac{4}{\pi^2} \Big[2R_L \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n^2} \Big] \\
&= R_L.
\end{aligned} \tag{4.30}$$

Whereas for a capacitive load, the higher-order terms ($n > 1$) can be ignored. Thus,

$$\begin{aligned}
Z_{L,RF} &\approx \frac{4}{\pi^2} \Big[\frac{1}{j(\omega_{LO}+\omega_{in})C} + \frac{1}{-j(\omega_{LO}-\omega_{in})C} \Big] \\
&= \frac{j8}{\pi^2 C} \frac{\omega_{in}}{\omega_{LO}^2 - \omega_{in}^2}
\end{aligned} \tag{4.31}$$

Specifically,

$$Z_{L,RF} \approx \begin{cases} \dfrac{4}{\pi^2} . \dfrac{1}{j(\omega_{in}-\omega_{LO})C} & \omega_{in} \approx \omega_{LO}, \\ \dfrac{8}{\pi^2} . j\omega_{in} \Big(\dfrac{1}{\omega_{LO}^2 C} \Big) & \omega_{in} \approx 0. \end{cases} \tag{4.32}$$

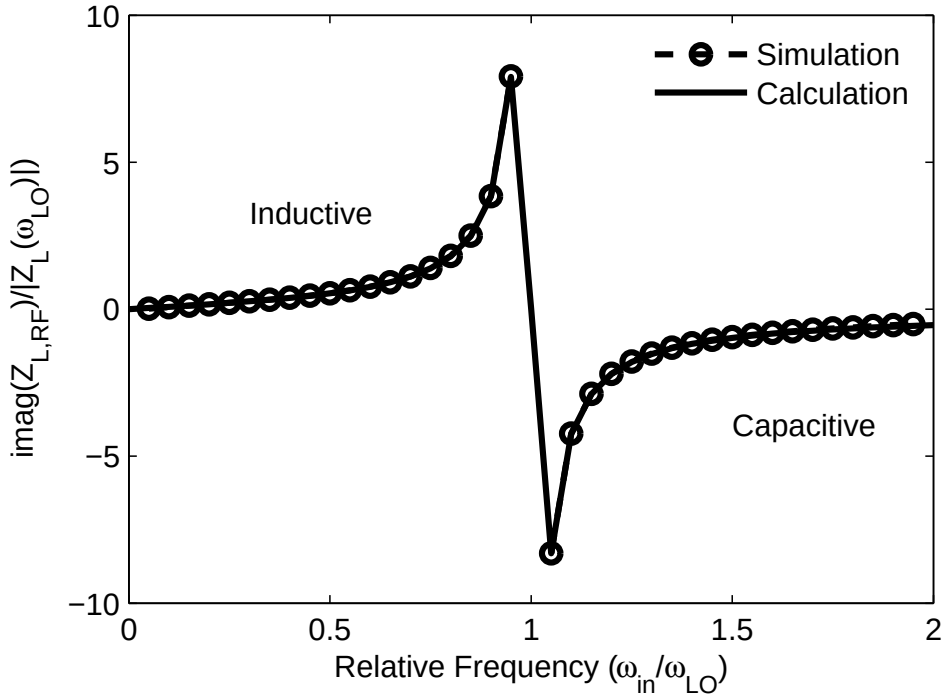


Figure 4.8: Normalized simulated and calculated (using (4.31)) input impedance for a capacitive load of 1 nF with 1 MHz LO frequency for a passive mixer with ideal switches.

This suggests that for a capacitive load at the mixer output, a very large reactive impedance at the mixer input when $\omega_{in} \approx \omega_{LO}$ is observed [76]. While at much lower input frequencies, a capacitive load appears as inductive at the mixer input. Fig. 4.8 depicts the normalized simulated and the calculated input impedance for an ideal mixer with a capacitive load.

The expression for $Z_{L,RF}$ can be simplified by observing that in a typical zero or low IF receiver design, large capacitances are placed at the mixer output to shunt away any undesired high-frequency signals. This implies that $Z_L(\omega_{LO} + \omega_{in})$ is negligible. Thus, (4.29) can be further simplified to,

$$Z_{L,RF} \approx \frac{4}{\pi^2}\Big[Z_L^*(\omega_{LO} - \omega_{in})\Big]. \tag{4.33}$$

Intuitively, this suggests that the load impedance is scaled and frequency translated by

ω_{LO} at the mixer input. Thus,

$$g_L(\omega) \approx \frac{\pi^2}{4} \frac{1}{Z_L^*(\omega_{LO} - \omega)}. \tag{4.34}$$

Hence, for a frequency dependent resistive load impedance, the IIP_2, IIP_3 and $IIP_{3,XM}$ can be computed using (4.18), (4.23) and (4.34) as,

$$IIP_2 \approx K_a \left\{ \frac{Z_L(\omega_1) Z_S(\omega_1 - \omega_2)}{Z_L(\omega_1 - \omega_2)} \right\}^2 \times \left[\Delta_2' + \Delta_1' Z_L(\omega_{LO} - \omega_1) + \Delta_0' Z_L^2(\omega_{LO} - \omega_1) \right]^{-2} \tag{4.35a}$$

$$IIP_3 \approx K_b \times \frac{Z_L(\omega_{LO} - \omega_1) Z_S(2\omega_1 - \omega_2)}{Z_L(\omega_{LO} - (2\omega_1 - \omega_2))} \times \left[B_3' + B_2' Z_L(\omega_{LO} - \omega_1) + B_1' Z_L^2(\omega_{LO} - \omega_1) + B_0' Z_L^3(\omega_{LO} - \omega_1) \right]^{-1}, \tag{4.35b}$$

$$IIP_{3,XM} \approx K_x \frac{Z_L^2(\omega_{LO} - \omega_1) Z_S(\omega_1 + \omega_2 - \omega_3)}{Z_L(\omega_{LO} - (\omega_1 + \omega_2 - \omega_3))} \times \left[C_3' Z_L(\omega_{LO} - \omega_1) + C_2' Z_L(\omega_{LO} - \omega_2) \{ Z_L(\omega_{LO} - \omega_1) + 2 Z_L(\omega_{LO} - \omega_2) \} + C_1' Z_L(\omega_{LO} - \omega_1) Z_L(\omega_{LO} - \omega_2) \times \{ Z_L(\omega_{LO} - \omega_1) + 2 Z_L(\omega_{LO} - \omega_2) \} + C_0' Z_L^2(\omega_{LO} - \omega_1) Z_L^2(\omega_{LO} - \omega_2) \right]^{-1}. \tag{4.35c}$$

where, K_a, K_b and K_x are independent of the load and source impedances, and,

$$\Delta_n' = \left(\frac{\pi^2}{4} \right)^n \Delta_n, \tag{4.36a}$$

$$B_n' = \left(\frac{\pi^2}{4} \right)^n B_n, \tag{4.36b}$$

$$C_n' = \left(\frac{\pi^2}{4} \right)^n C_n. \tag{4.36c}$$

4.4.2 Effect of Source Impedance on Mixer Linearity

Equation (4.35a) highlights the dependence of the second-order intercept point on the load and source impedances. It suggests that, for good IIP_2, $|Z_S(\omega_1 - \omega_2)|$ should

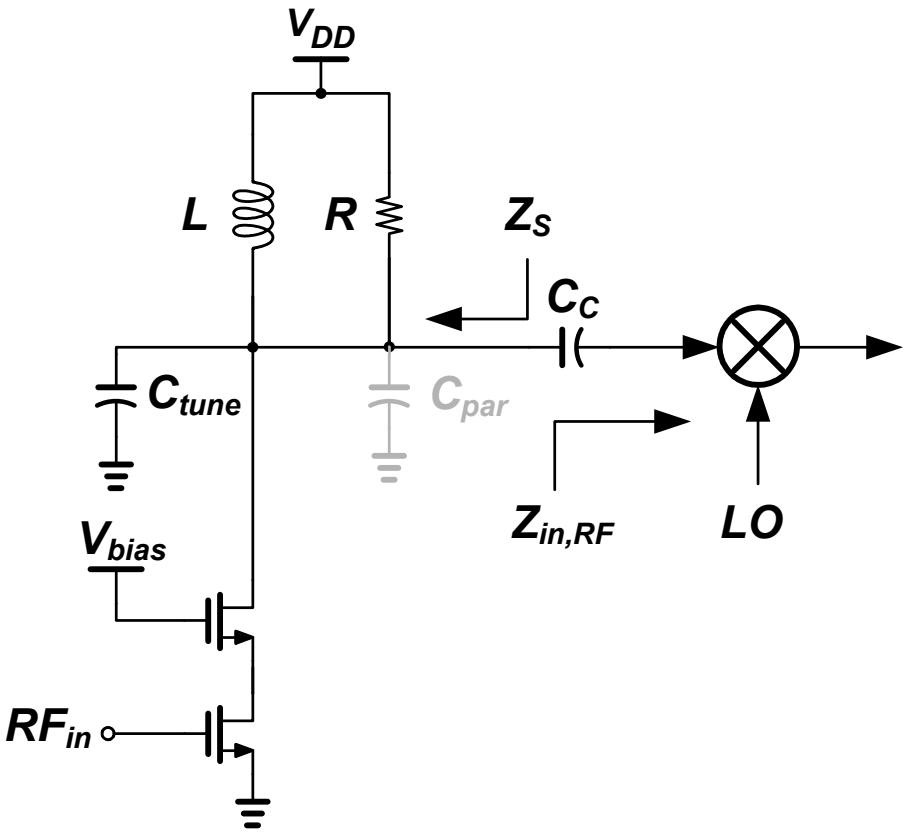


Figure 4.9: Constraints on the mixer source impedance for maximizing the linearity of a passive mixer preceded by a cascode CMOS LNA with an inductive load.

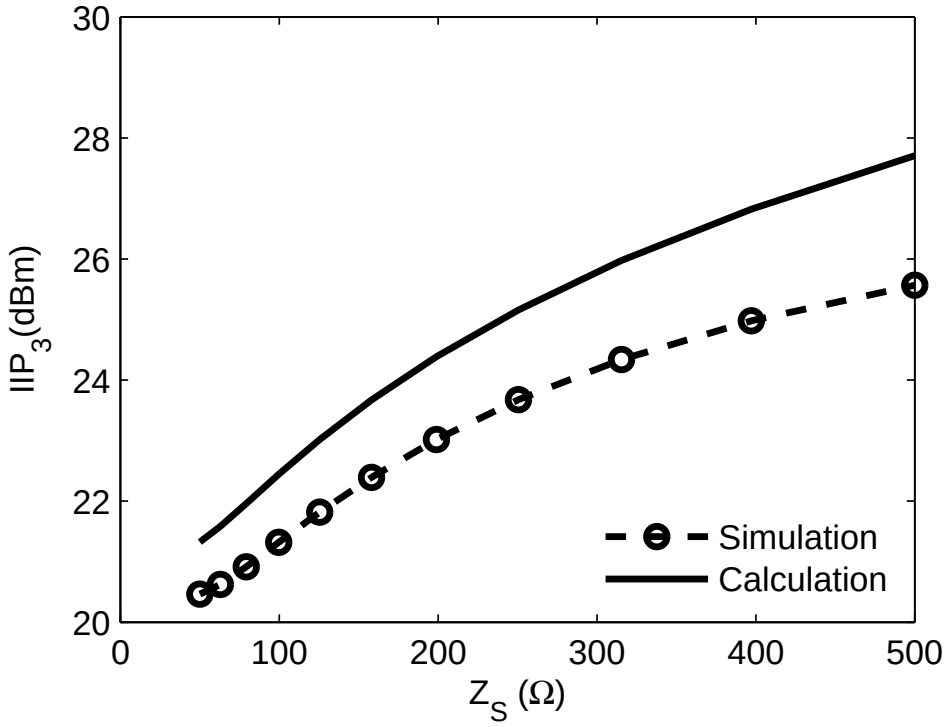


Figure 4.10: Simulated (using PSP model) and calculated low-frequency IIP_3 variation with the mixer source impedance. The RF tone power at the input of the LNA is -50 dBm with $g_{m,LNA}$ = 30 mS in Fig. 4.1(a). The mixer load impedance is 5 Ω.

be as large as possible. Physically, a low source impedance at $(\omega_1 - \omega_2)$ amplifies the IMD_2 currents due to the mismatches in the mixer transistors or LO signals. In a typical receiver, the parasitic capacitances at the LNA-mixer interface can lower the input impedance. Hence, in a receiver design with inductive LNA load, it is desired to resonate any capacitance at the LNA output node. Additionally, an AC coupling capacitor between the LNA and the mixer can boost the mixer source impedance at $(\omega_1 - \omega_2)$, while passing the RF signal [84]. For a non-inductive LNA load, it might be desirable to place additional series resistance at the interface to improve IIP_2 [10].

For improving both the two-tone IIP_3 and the cross-modulation $IIP_{3,XM}$, the source impedance at the RF signal frequency should be as large as possible. As depicted in Fig. 4.9, for an LNA with an inductive load, L, and Quality factor, Q, the mixer source impedance is constrained by,

$$|Z_S| < |\omega LQ|. \tag{4.37}$$

To maximize $|Z_S|$ a large high-Q inductor is desired which resonates with shunt capacitances at the signal frequency, i.e.,

$$L = \frac{1}{\omega_{RF}(C_{tune} + C_{par})}, \tag{4.38}$$

where, C_{tune} and C_{par} are the tuning and parasitic capacitors at the LNA output respectively (Fig. 4.9). Hence, for achieving high linearity, it is highly desired to minimize the parasitic capacitances at the LNA output node, so that a larger inductor can be accommodated while having some additional tuning capacitance.

4.4.3 Effect of Load Impedance on Mixer Linearity

A passive mixer is typically cascaded with a transimpedance amplifier (TIA) as shown in Fig. 4.1. Thus, the mixer load impedance is low at DC, but increases rapidly with frequency as the open-loop transimpedance amplifier gain drops. Hence, the downconverted jammers outside the desired signal band encounter a relatively high TIA input impedance.

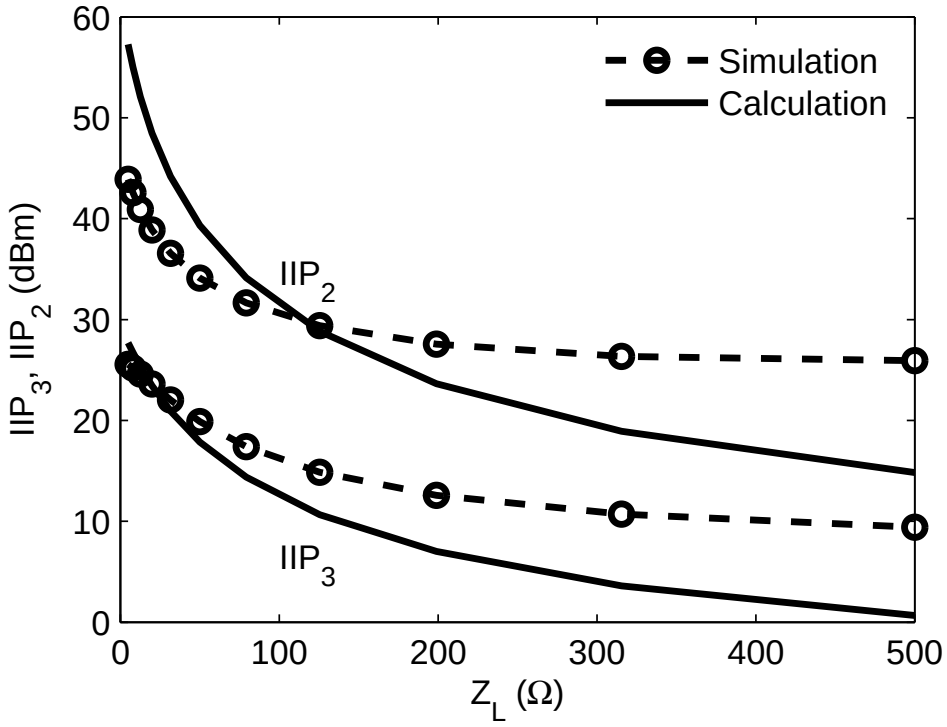


Figure 4.11: Simulated (using PSP model) and calculated low-frequency IIP_2 and IIP_3 variation with mixer load impedance. The RF tone power at the input of the LNA is -50 dBm with $g_{m,LNA}$ = 30 mS in Fig. 4.1(a). The mixer source impedance is 500 Ω.

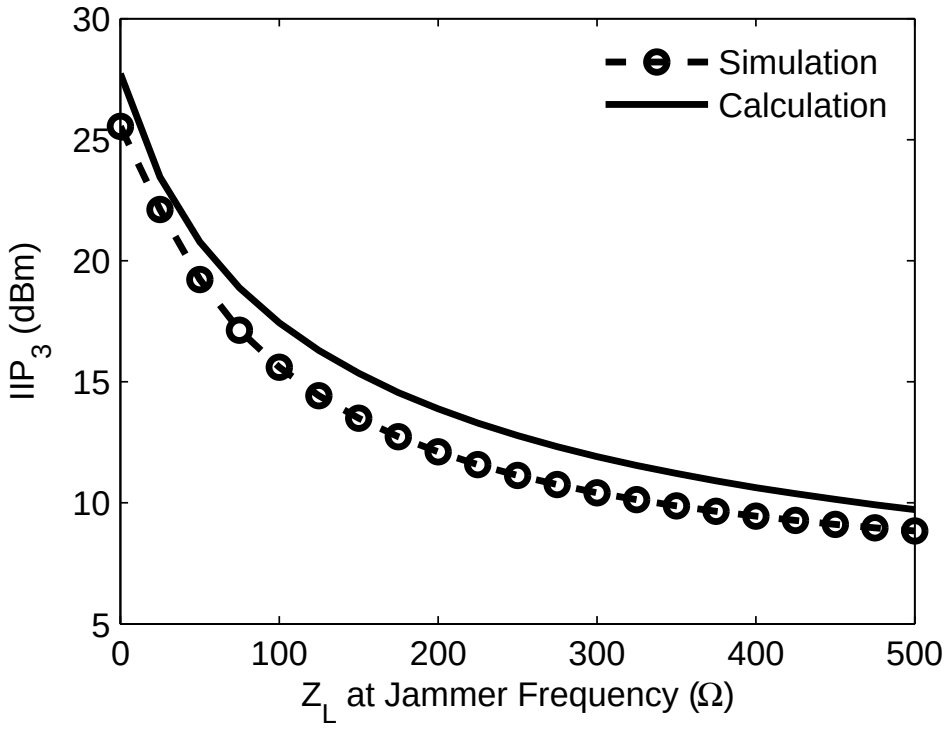


Figure 4.12: Simulated (using PSP model) and calculated IIP_3 variation with the mixer load impedance at the downconverted jammer frequency ($\omega_{LO}-\omega_1$). The RF tone power at the input of the LNA is -30 dBm with $g_{m,LNA}$ = 30 mS in Fig. 4.1(a). The mixer source impedance and load impedance at $\omega_{LO}-\omega_{RF}$ are 500 Ω and 5 Ω respectively.

From (4.35), it is evident that $|Z_L(\omega_{LO} - (\omega_1 - \omega_2))|$, $|Z_L(\omega_{LO} - \omega_{RF})|$ and $|Z_L(\omega_{LO} - \omega_1)|$ should all be minimized simultaneously to reduce IIP_2 and IIP_3. The first term corresponds to a load impedance at high frequency which is small due to the large filtering capacitors at the mixer output. The second term, $|Z_L(\omega_{LO} - \omega_{RF})|$, corresponds to the load impedance at baseband, which is small due to the low input impedance of transimpedance amplifier (TIA). The frequency $(\omega_{LO} - \omega_1)$ refers to the downconverted jammer frequency where the TIA input impedance may be high due to finite open-loop bandwidth of the amplifier, especially, for out-of-band jammers.

Similarly, for the cross-modulation distortion, $(\omega_{LO} - (\omega_1 + \omega_2 - \omega_3))$ and $(\omega_{LO} - \omega_1)$ correspond to the RF and the close-in blocker frequency locations, where the load impedance is small. However, the effect of out-of-band jammer at $(\omega_{LO} - \omega_2)$ is much more drastic in comparison to that for IIP_3. Hence, apart from providing low load impedance at baseband and high frequency, it is of paramount importance to filter off the out-of-band blockers.

For instance, consider the case of a CDMA-2000 receiver in the PCS band. The baseband bandwidth is 625 kHz, whereas the strongest jammer, due to transmitter leakage is downconverted to 80 MHz. At 80 MHz, the TIA input impedance is large, resulting in poor mixer linearity performance. As suggested by (4.35), this term contributes to IIP_2, IIP_3 and $IIP_{3,XM}$, making the high load impedance at the downconverted jammer frequency the single most dominant factor in degrading the passive mixer linearity. Hence, instead of placing an interstage RF filter, a linear filtering technique at the mixer output can be helpful in improving the mixer linearity [85].

Intuitively, a large $|Z_L(\omega_{LO} - \omega_1)|$ results in a large voltage swing at the mixer IF node. This voltage swing boosts the second-order and third-order nonlinear current sources resulting in larger distortions. In addition, this can amplify the nonlinear charging and discharging effects of the transistor capacitances.

Agilent Goldengate™ simulations were performed with low load resistances at $\omega_{LO} - (\omega_1 - \omega_2)$ and $\omega_{LO} - (2\omega_1 - \omega_2)$, while resistance at $\omega_{LO} - \omega_1$ is varied. As predicted, a rapid degradation in mixer linearity is observed with increasing mixer load impedance at downconverted jammer frequency $(\omega_{LO} - \omega_1)$, as shown in Fig. 4.12.

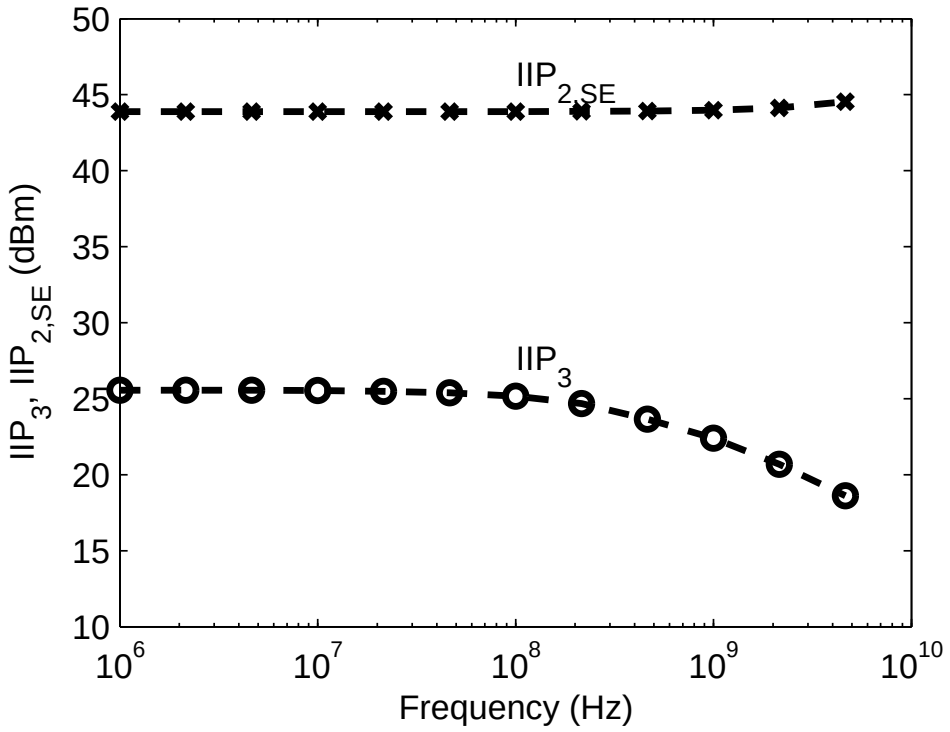


Figure 4.13: Simulated variation in mixer single-ended IIP_2 and IIP_3 with frequency. The RF tone power at the input of the LNA is -50 dBm with $g_{m,LNA}$ = 30 mS in Fig. 4.1(a). The mixer load and source impedances are 5 Ω and 500 Ω respectively.

4.5 High Frequency Effects on Mixer Linearity

As the LO frequency increases, the reactive impedances of the nonlinear gate-source and gate-drain capacitances becomes comparable to the transistor conductance (g_1), and the mixer linearity performance degrades due to the nonlinear charging and discharging of these capacitors. However, as the technology is scaling to shorter gate length, these parasitic capacitances are reducing, and their effects are typically negligible up to few GHz.

Another source of nonlinearity is introduced due to the LO rise and fall times [78]. It is straightforward to reduce the rise and fall times of the square-wave LO signal, so that its effect is minimal in this frequency range, albeit at the cost of slightly larger LO driver power consumption. These high-frequency effects will continue to reduce with the shrinking technology and parasitic capacitances. The simulated single-ended IIP_2

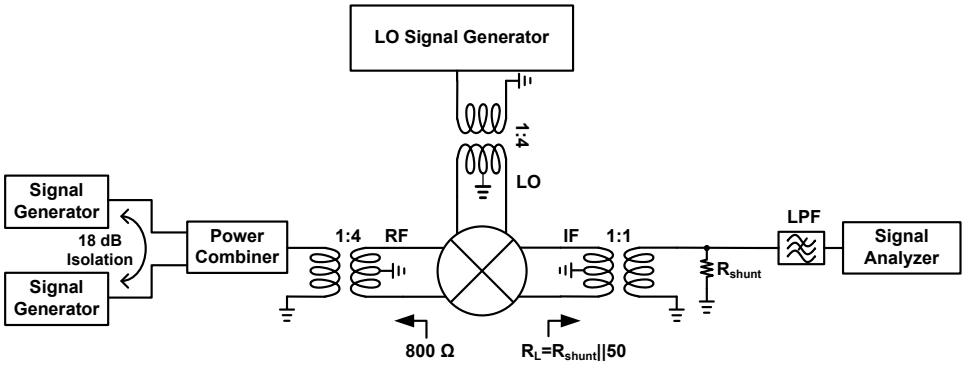


Figure 4.14: Passive mixer measurement setup.

and IIP_3 are plotted as a function of frequency in Fig. 4.13, and there is hardly any variation in the IIP_2 performance, while IIP_3 degrades by only 3 dB at 1 GHz with 50 μm $\times$ 0.18 μm transistors.

4.6 Measurement Results

Measurements were conducted with a double balanced passive MOSFET mixer fabricated in a CMOS Silicon-on-Insulator (SOI) technology [72]. This technology uses an insulating substrate, which reduces the substrate losses and improves device performance. Since the preceding analysis does not involve any assumptions based on the substrate, the results are valid for SOI and non-SOI technologies.

Fig. 4.14 shows the measurement setup. The RF balun has a 1:4 turn ratio, which provides a desirable high source impedance to the mixer. A shunt resistance, R_{shunt}, was added to create the desired load impedance at the IF port. The calculated and measured fundamental and third-order intermodulation voltage at the mixer output are plotted in Fig. 4.15. The measurements are done with +15 dBm sinusoidal LO at 500 MHz, 800 MHz and 1 GHz, with the two input tones placed at 20 MHz and 39.5 MHz offset.

Fig. 4.16 shows the measured IIP_3 with increasing load impedance, which is in close agreement with the calculated values. The IIP_3 is computed by comparing the distortion voltage at the mixer output to a reference voltage measured with 5 Ω load

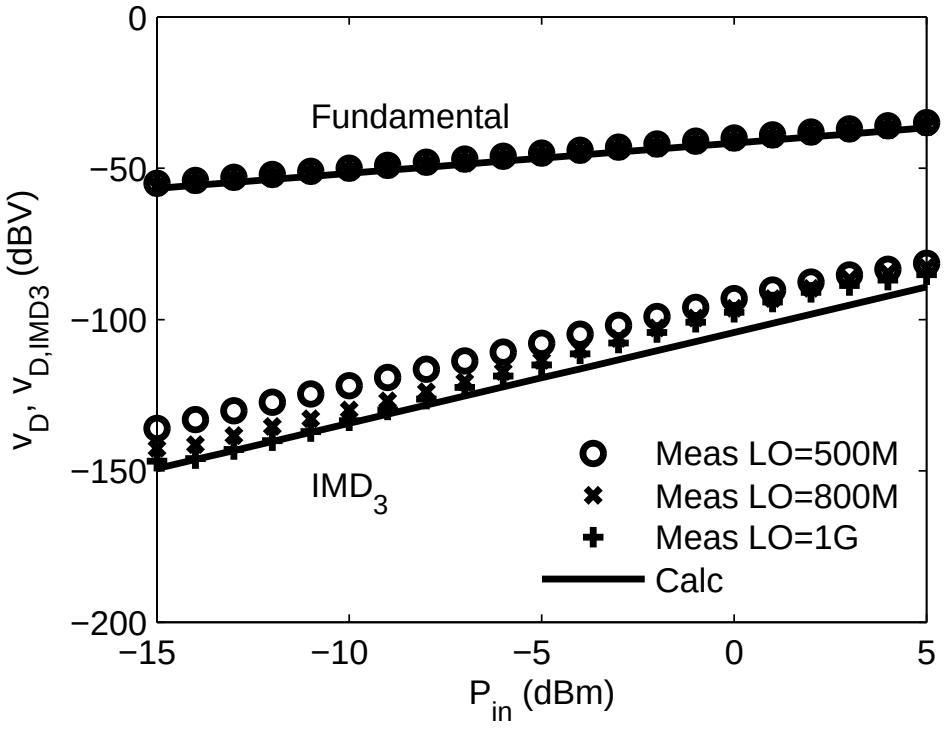


Figure 4.15: Measured and calculated fundamental and third-order intermodulation distortion voltages for the passive CMOS mixer with load impedance of 5 Ω. The LO power was +15 dBm.

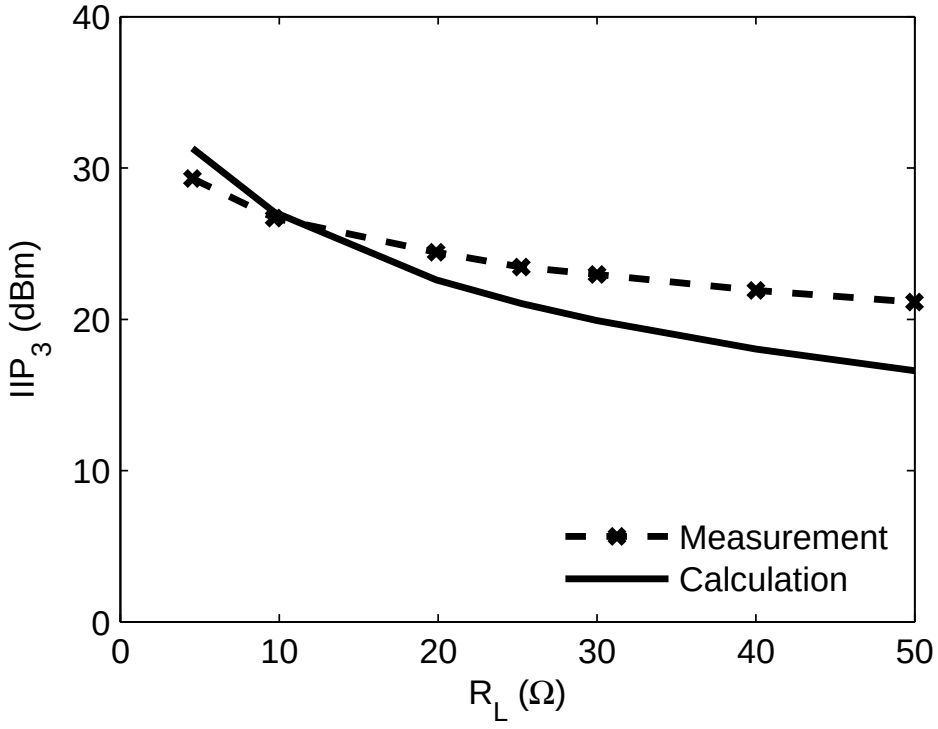


Figure 4.16: Degradation in the measured and calculated IIP_3 with increasing load impedance. The LO power was +15 dBm and the input power was -10 dBm, and the measurement was done at 800 MHz.

impedance. As predicted, the IIP_3 degrades with the increasing load impedance.

4.7 Conclusion

We have analyzed the linearity of a current-commutating passive CMOS ZIF downconverting FET mixer and highlighted its dependence on the mixer source and load impedances. Closed-form expressions have been presented for the second-order, third-order and cross-modulation input-intercept points of the mixer using a Volterra series analysis, and are found to be in close agreement with the simulated response with the PSP MOSFET device model.

An accurate relationship has been established between the input impedance and an arbitrary load impedance for an ideal passive mixer. Through this analysis, it is observed that while a resistive load appears unaltered at the mixer input, a capacitive

load undergoes a frequency translation, peaking at odd-orders of LO harmonics with the peak amplitude going down as $1/n^2$, n being order of the harmonic. In particular, the input impedance appears inductive from DC to ω_{LO} and then becomes capacitive from ω_{LO} to $2\omega_{LO}$.

Dependence of passive mixer linearity on the load and source impedances has been analyzed and design guidelines have been suggested for improving it. Through Volterra series analysis, it is shown that the load impedance should be minimized at downconverted jammer frequencies for improving mixer linearity, particularly, due to the cross-modulation distortion. Additionally, the source impedance should be kept as large as possible at DC and the RF signal frequency.

Measurements were conducted with SOI-based passive CMOS mixers and the results have been found to be in close agreement to the calculations for different load impedances. This chapter has been submitted for review for the following publication:

1. H. Khatri, P. S. Gudem, and L. E. Larson, "Distortion in current commutating passive CMOS downconversion mixers," submitted to *IEEE Trans. Microw. Theory Tech.*, 2009.

Chapter 5

CMOS Receiver Design for Improved Linearity

5.1 Introduction

Direct conversion receivers (DCR's) have gained wide attention for CDMA receivers due to their simplicity and improved integration compared to a heterodyne architecture. In some CDMA transmission scenarios, a strong transmitted signal (Tx) leaks into the receiver and creates in-band interference through two mechanisms. First, due to the second-order nonlinearity in the downconverter, it creates distortion in baseband. Second, it can cross-modulate with a close-in continuous wave (CW) blocker due to third-order nonlinearity [1]. The cross-modulation is typically measured using the triple-beat (TB) metric, where a three-tone test is conducted with Tx represented by two-tones and the TB is measured as the power ratio (in dB) between the single-tone blocker and the ensuing cross-modulation distortion. To suppress this distortion, the Tx leakage is typically filtered with an expensive off-chip interstage SAW filter. The cost of the SAW filter is comparable to that of the receiver itself, and has a large form-factor, which occupies board area and requires additional off-chip matching components.

Several attempts have been made to address this problem with a monolithic approach. A high-Q on-chip RF passive LC filter using bond-wire inductors was presented in [86]. But it suffered from high insertion loss and is dependent on the variations in the

bondwire characteristics. A least mean-square (LMS) adaptive filtering technique was proposed, which estimates the Tx leakage using a matched filter and fed it back to the LNA input for cancellation [7]. Active feed-forward approaches in the RF domain have also been reported, where the Tx leakage is downconverted, filtered out and then upconverted for cancellation [5, 6]. Yet another approach involves a feed-forward path after the LNA and cancellation with an adaptive digital LMS equalizer filter [9]. However, all of these techniques have considerable noise penalty and rely on precise amplitude and phase matching for cancellation. Recently, a SAW-less receiver using a mixer with embedded Tx filtering was proposed [85]. This implementation was at 900 MHz and required large capacitor area for filtering. Another approach using large filtering capacitors at the mixer output was presented [12]. However, it used 25% duty-cycle LO which has higher power consumption.

In this chapter, we suggest an active Tx filtering technique to alleviate the problem. The passive mixer linearity is discussed in section 5.2. In section 5.3, we present the architecture and implementation of the proposed receiver with Tx filtering. The measurement results are presented in section 5.4.

5.2 Passive Mixer Linearity

A simplified direct conversion receiver (DCR) architecture without the interstage SAW filter is shown in Fig. 5.1. In the presence of the Tx leakage signal, the LNA can be designed to accommodate the cross-modulation distortion using active post-distortion (APD) [15] or modified derivative superposition (MDS) methods [13]. For the CDMA-2000 system, the maximum modulated Tx leakage power at the LNA input can be as high as -28 dBm. Assuming an LNA gain of 15 dB, the Tx blocker at the input of downconverter is -13 dBm. However, the downconverter is unable to meet the desired TB specifications in presence of this large Tx signal.

The mechanism of nonlinearity in the passive mixer can be explained intuitively through Fig. 5.2. At the mixer output, the desired Rx signal is downconverted to baseband, where the input impedance of the TIA is small, resulting in a small voltage swing. However, due to the finite bandwidth of the opamp, the TIA input impedance is high

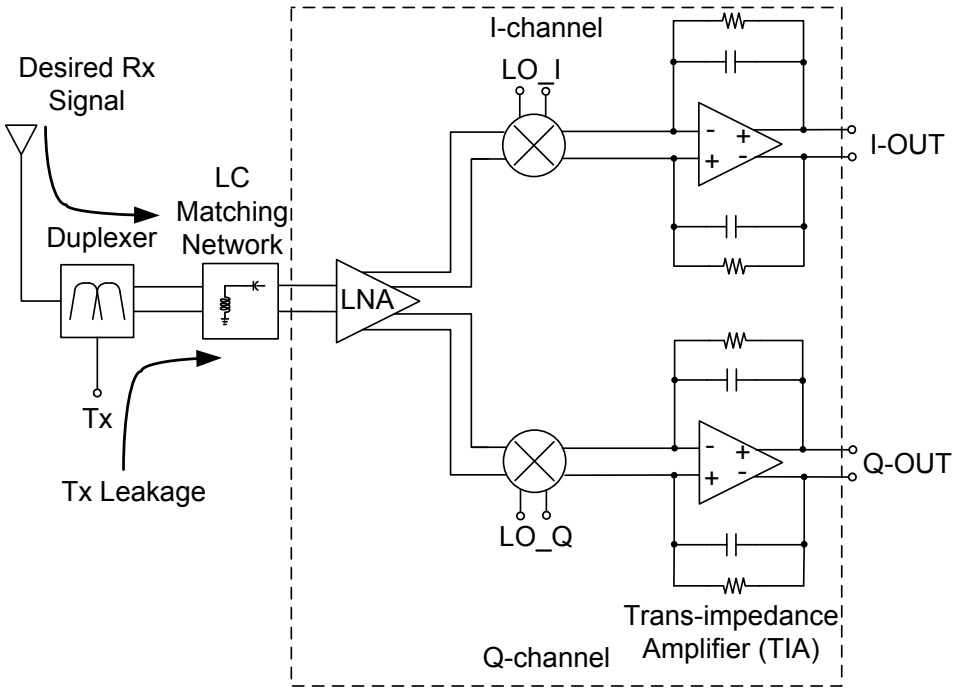


Figure 5.1: CDMA receiver without the SAW filter between the LNA and the mixers.

at the downconverted Tx signal frequency (80 MHz for CDMA-2000 PCS Band). This results in a large voltage swing at the mixer output, raising the second-order and third-order distortion. In addition, this can amplify the nonlinear charging and discharging effects of the mixer transistor capacitances.

5.3 Proposed Architecture and Implementation

To improve the linearity in the absence of the interstage RF filter, a linear frequency selective "sink" is placed at the mixer output, which filters out the downconverted Tx signal without affecting the desired baseband RF signal. This is illustrated in Fig. 5.3.

A grounded high-Q series LC resonator, centered at $f_{RX} - f_{TX}$, could effectively filter the downconverted Tx signal without affecting the desired RF signal. However, for PCS band applications, centered at 1.96 GHz and with a Tx offset of 80 MHz, even a

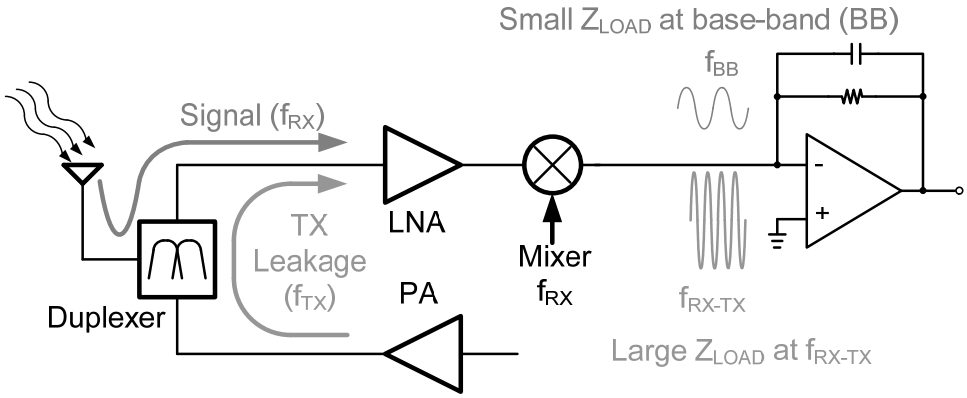


Figure 5.2: Mixer nonlinearity due to TX leakage current [12].

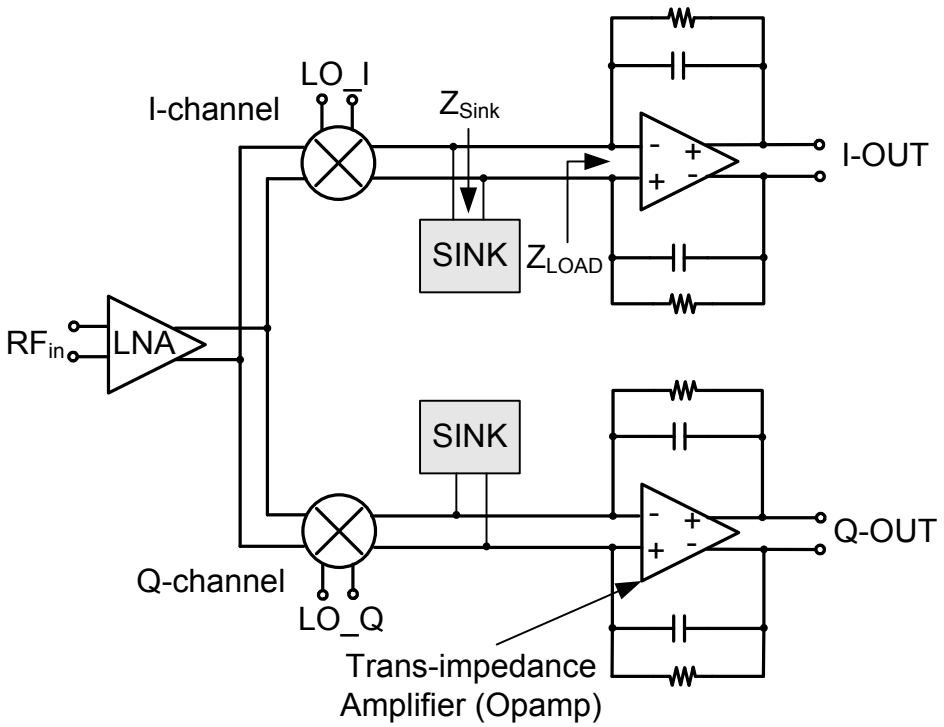


Figure 5.3: Proposed architecture to alleviate mixer nonlinearity due to TX leakage.

100 pF capacitance requires a high-Q 40 nH inductor for resonance, which is very challenging to implement monolithically. The active-RC and Gm-C filter implementations can also be ruled out due to their poor linearity and high f_T requirements at 80 MHz.

Consider the circuit shown in Fig. 5.4, where a passive CMOS mixer, whose LO is at the downconverted Tx frequency, is cascaded with a termination that offers low input impedance at baseband and a high impedance around 80 MHz. This auxiliary mixer will downconvert the Tx signal to baseband, while the desired Rx signal is upconverted to 80 MHz and will be reflected back by the termination. This termination can be implemented as a trans-impedance amplifier (TIA), as it meets the input impedance requirements. Fig. 5.5 shows the simulated impedances at the input of the auxiliary mixer (Z_{Sink}) and at the input of the auxiliary TIA (Z_{AuxTIA}). The two are related with the expression [87],

$$Z_{Sink} = \frac{4}{\pi^2} \sum_{n=1,3,5...}^{\infty} \frac{1}{n^2} \Big[Z_{AuxTIA}(n\omega_{LO} + \omega_{in}) + Z^*_{AuxTIA}(n\omega_{LO} - \omega_{in}) \Big], \tag{5.1}$$

where, ω_{in} and ω_{LO} are the auxiliary input frequency and auxiliary LO frequency respectively.

The sink operation is detailed in Fig. 5.6, and the schematic of the receiver with the proposed sink is shown in Fig. 5.7. At the input of the auxiliary mixer, the desired signal is at baseband, while the downconverted Tx is centered around 80 MHz. The auxiliary mixer *downconverts* the downconverted Tx signal close to baseband which is attenuated by the auxiliary TIA, and upconverts the downconverted Tx to 160 MHz. This portion is reflected back due to the relatively higher input impedance of the auxiliary TIA at this frequency. Similarly, the baseband signal is upconverted to around 80 MHz and is reflected back, as desired. The Tx signal at the auxiliary mixer output leaks back to the main signal path due to insufficient IF-RF isolation. Hence, to avoid this leakage from interfering with the desired signal, the auxiliary LO signal needs to be placed at one channel offset, i.e., at 78.75 MHz.

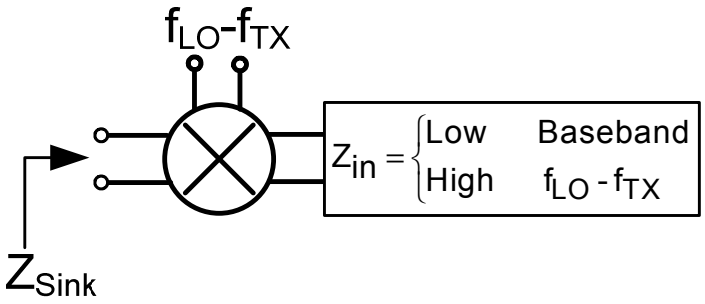


Figure 5.4: An active sink comprised of a passive mixer operating at the downconverted Tx frequency cascaded with a termination having low impedance at baseband and high impedance around 80 MHz.

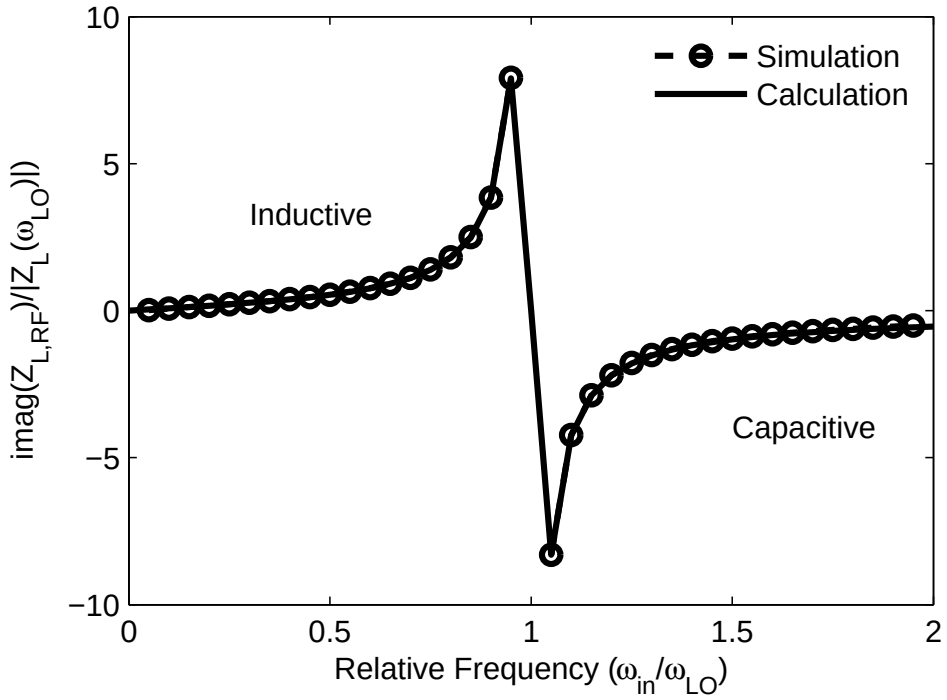


Figure 5.5: Impedance seen at the input of the auxiliary TIA and the input of the auxiliary mixer.

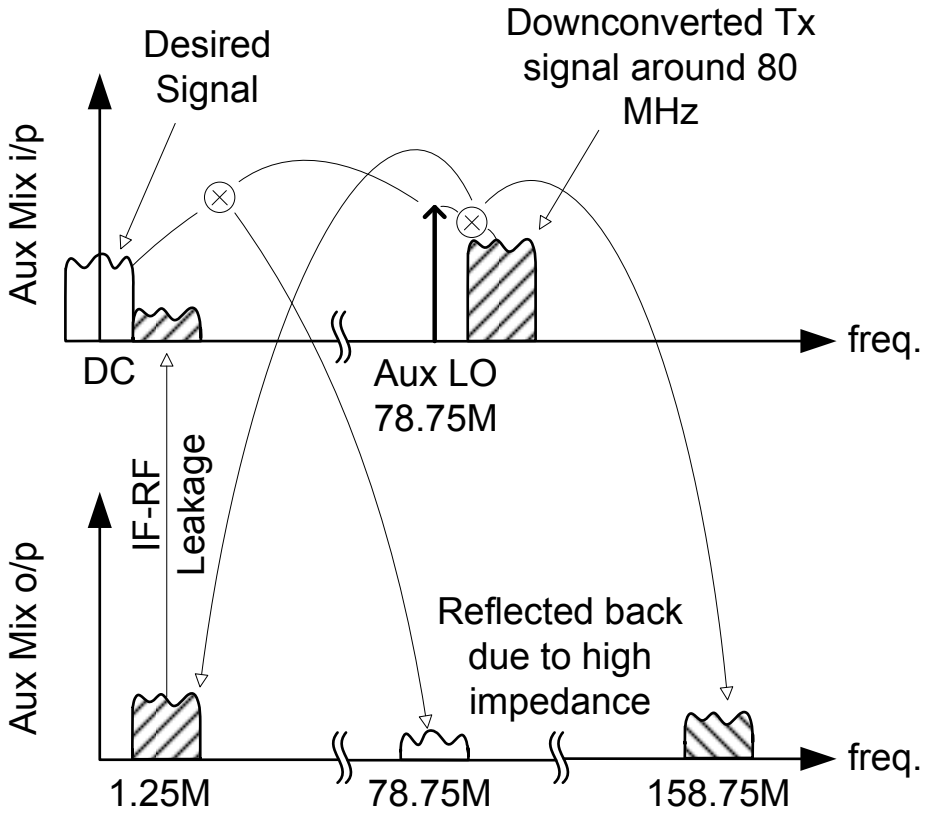


Figure 5.6: Auxiliary mixer operation.

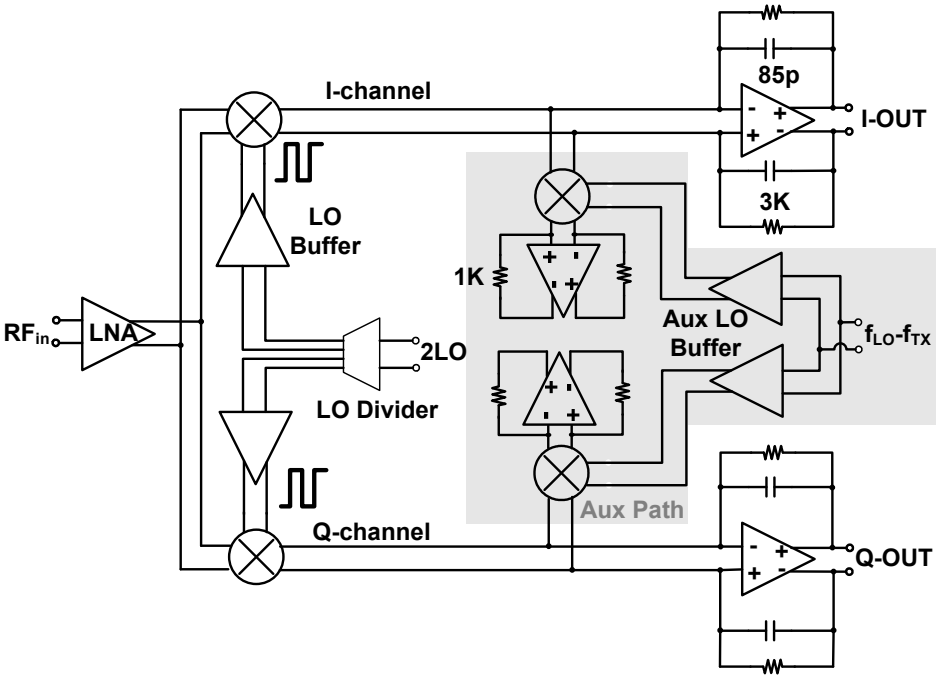


Figure 5.7: Proposed CDMA receiver.

In comparison with previously published techniques, this approach has several advantages. First, precise amplitude and phase matching is not required from the in-phase and quadrature-phase sinks, because the sink has very little effect on the desired signal. Second, large capacitors are not required in the filtering circuit, saving die area. Since, the high linearity of the receiver is required only in certain scenarios, when the Rx signal is small and Tx signal is maximum, the auxiliary path can usually be turned *off*. Hence, this technique should not adversely affect the battery life. However, there are certain drawbacks to the scheme. Only half the Tx signal is downconverted to baseband, while the other half is upconverted to 160 MHz. Hence, the TB and IIP_2 improvement is limited to approximately 6 dB.

5.3.1 I-Q Cancellation

This fundamental limitation in the Tx cancellation can be dropped with a selective filtering of the 160 MHz signal in the auxiliary path. This can be achieved with an *I-Q Cancellation* architecture shown in Fig. 5.8. Akin to the Weaver architecture, the

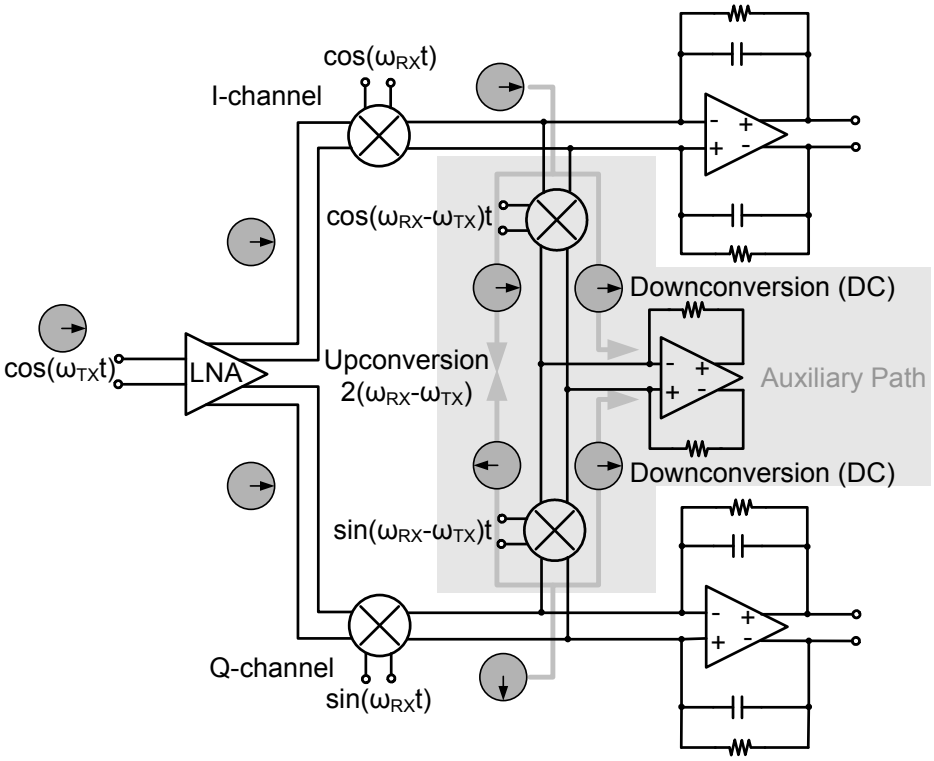


Figure 5.8: TX current path in the I-Q cancellation topology.

auxiliary mixers are also driven by quadrature LO signals at $(f_{RX} - f_{TX})$, such that the upconverted Tx signals in the auxiliary path from I and Q channels are in opposite phase. By symmetry, they have no systematic error in the amplitudes, and hence entire undesired Tx signal can be filtered out.

However, this I-Q cancellation technique also affects the desired signal. Upon upconversion by the auxiliary mixers, one half of the signal gets canceled by the corresponding signal from the other channel. This results in 3-dB signal loss. The mechanism of signal cancellation is depicted in Fig. 5.9. A 3-dB signal loss may be acceptable, but this also affects the receiver's noise performance. Due to reduced gain, the contribution of the main path TIA noise increases. However, there is another significant source of noise amplification in this architecture, which is discussed in next subsection.

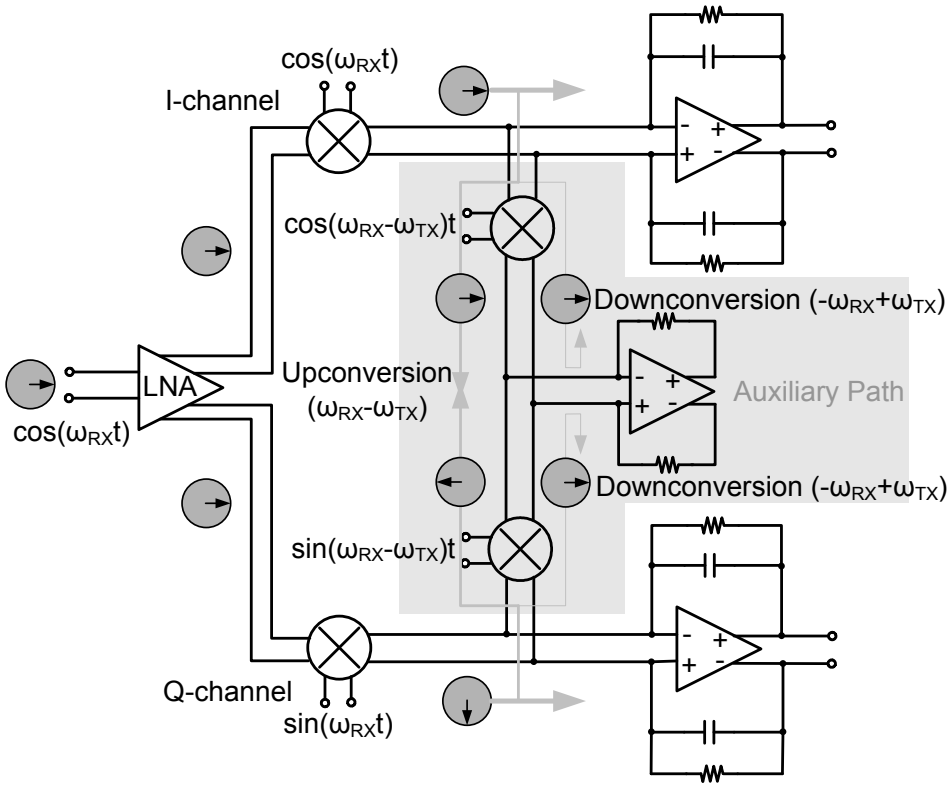


Figure 5.9: RX current path in the I-Q cancellation topology.

5.3.2 Noise in I-Q Cancellation

The effect of noise sources in the opamp can be represented using an equivalent voltage source (v_{eq}) and an equivalent current source (i_{eq}) at the input of the opamp. A simplified single-ended schematic of the opamp configured as TIA is shown in Fig. 5.10(a). The input of the amplifier is modeled as a current source with a finite source impedance Z_S. The input referred noise voltage, v_{irn} of the amplifier (Fig. 5.10(b)) is given by

$$i_{irn} = i_{eq} + \frac{v_{eq}}{Z||Z_S} \tag{5.2}$$

where, Z is the feedback impedance. Evidently, if Z and Z_S are large, then contribution of v_{eq} is negligible. On the other hand, if the source impedance Z_S is shorted then the contribution of v_{eq} becomes significant and can affect the overall noise performance [88].

The source impedance Z_S can be estimated through the circuit in Fig. 5.11 for estimating the source impedance, Z_S. The parasitic capacitance, C_{par} comprises of the mixer output capacitance, the opamp input capacitance and the high frequency filter capacitance at the output of the mixer. As the two mixers are driven in quadrature, during quarter of a period, M_1 and M_3 are conducting, which charges up the noise power in C_{par}. During the other quarter period, M_2 and M_4 are conducting, which discharges this power back. Effectively, this acts as a switched capacitor implementation of a short, resulting in lowering Z_S. Hence, despite several advantages, this architecture suffers from extremely poor noise performance.

Due this drawback, the previous architecture with no I-Q cancellation was chosen for implementation.

5.3.3 Low Noise Amplifier

In a cascode low-noise amplifier, the nonlinearity is primarily attributed to the transconductance of the input transistors. For distortion cancellation, the modified derivative superposition method was chosen, as this approach is less vulnerable to the impedance variations at the LNA-mixer interface [13].

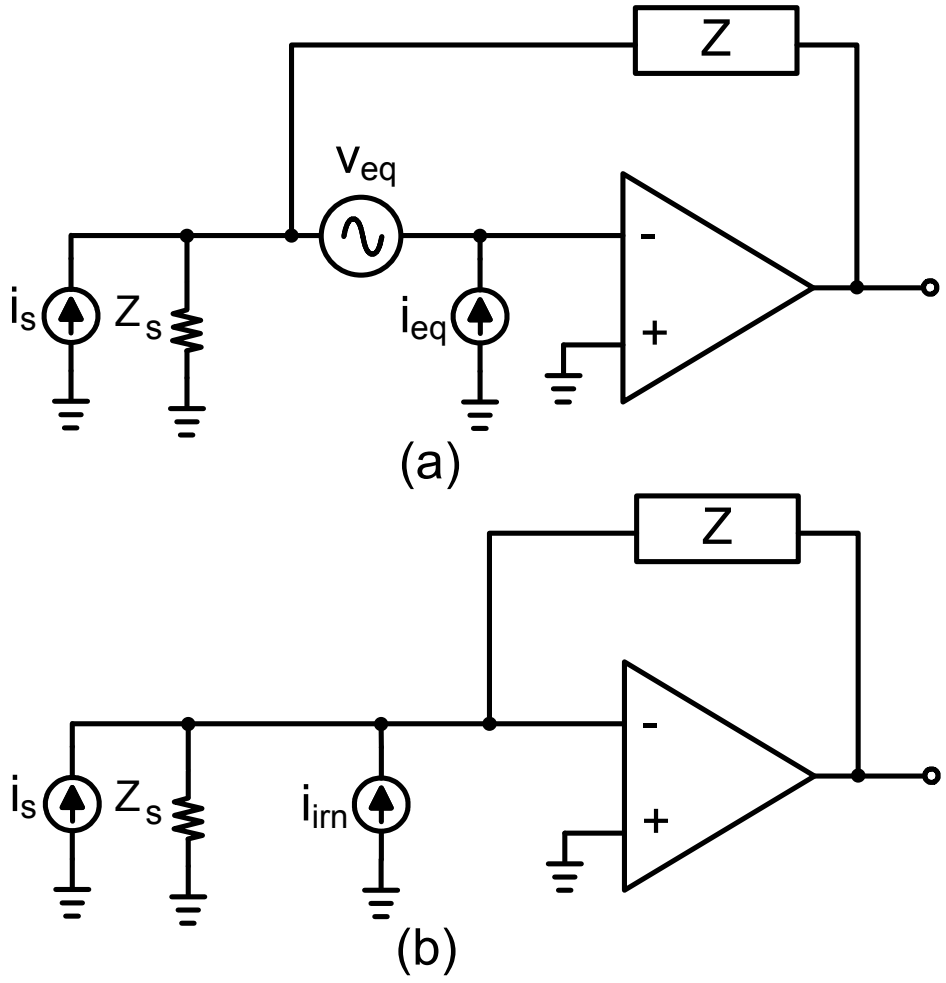


Figure 5.10: (a) Equivalent noise sources of an opamp. (b) Input-referred noise sources in a trans-impedance amplifier.

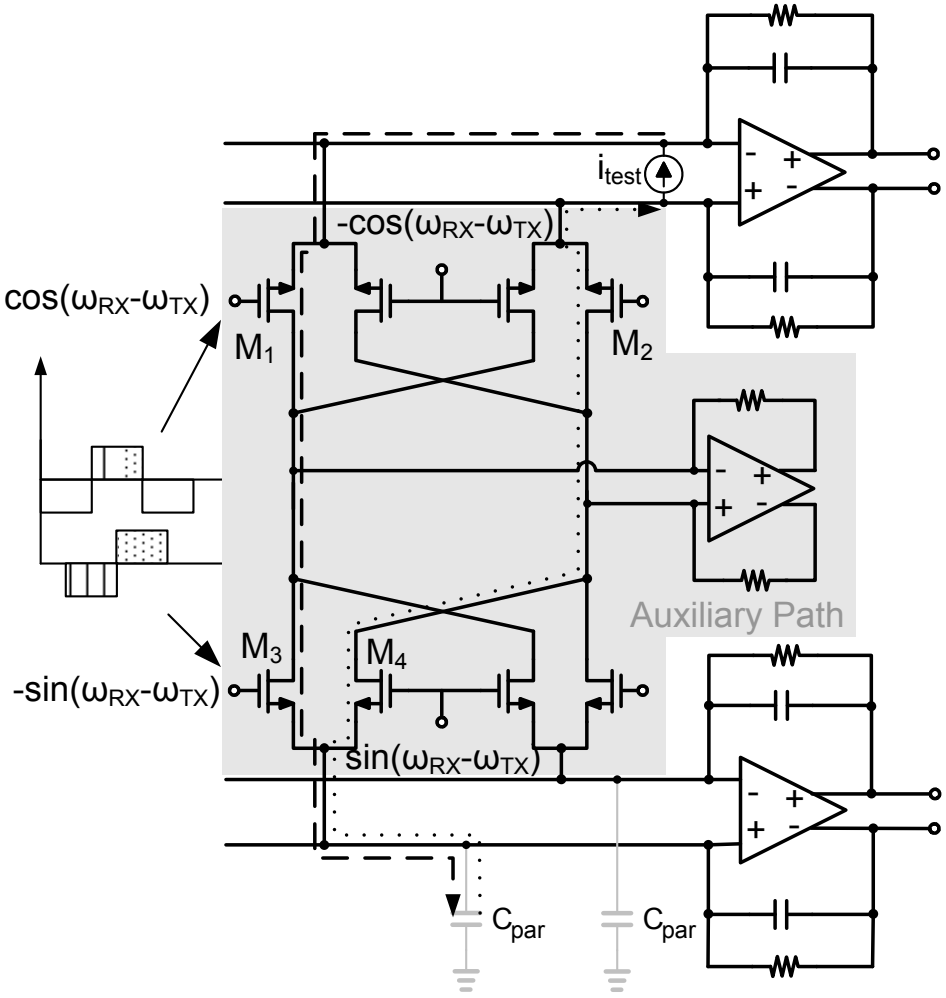


Figure 5.11: Noise generation in I-Q cancellation topology.

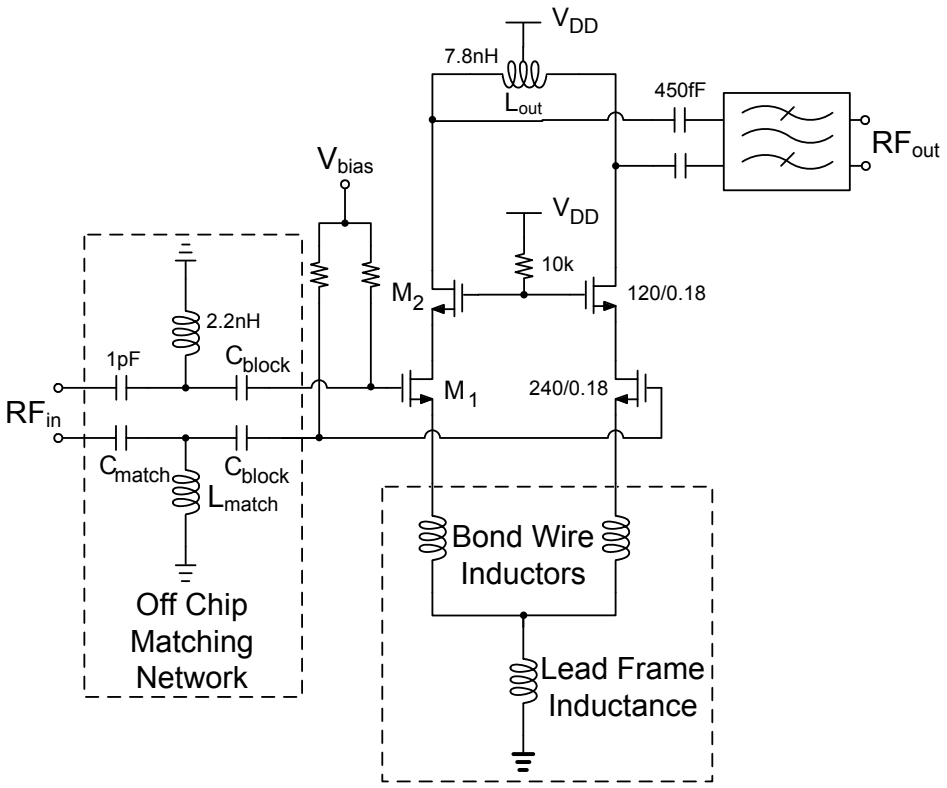


Figure 5.12: LNA based on modified derivative superposition method [13].

The main transistors are biased in strong inversion for high gain and 0.9 nH center-tapped differential inductor is used for source degeneration and DC biasing. The auxiliary transistors are biased in weak inversion, which creates third-order drain currents that are opposite in phase with the third-order drain currents of the main transistors as shown in Fig. 5.12. The main transistors are optimized for best noise performance and the the auxiliary transistors, degeneration inductance and the biasing currents are optimized for best linearity performance. The main path consumes 20 mA, and the auxiliary path consumes 2 mA.

5.4 Measurement Results

The chip microphotograph is shown in Fig. 5.13, and it occupies 1.6×1.6 mm^2 excluding bondpads. The key receiver specifications are enumerated in Table 5.1. As

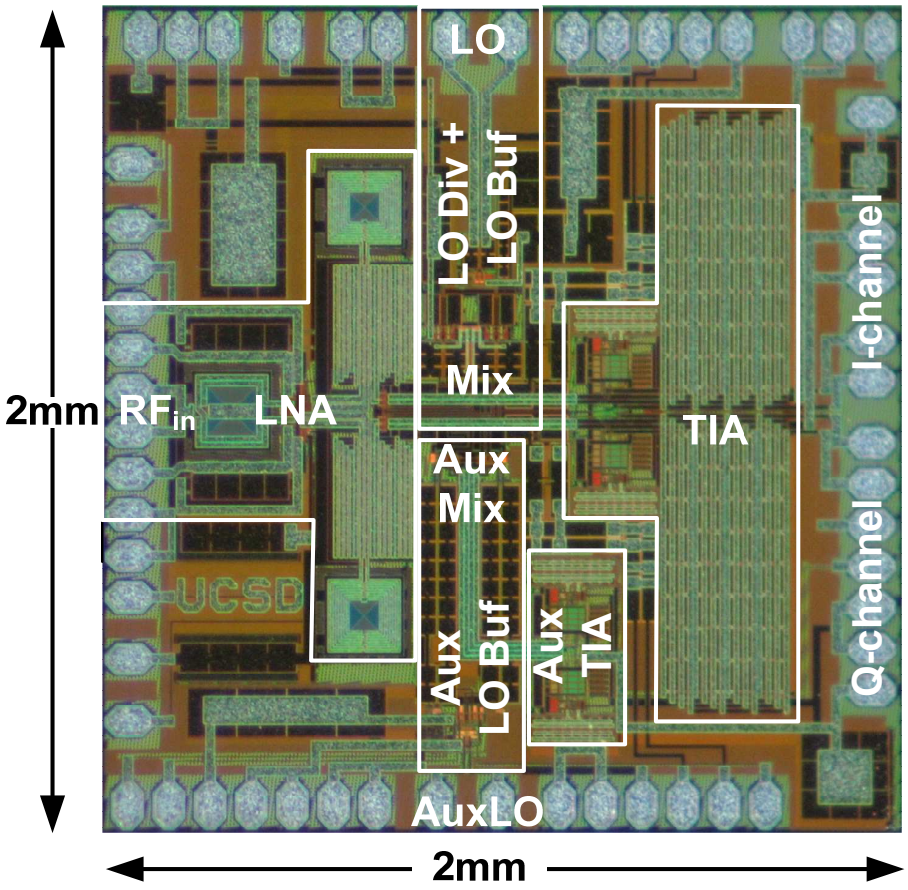


Figure 5.13: Microphotograph of the receiver.

expected, no significant difference was observed in the receiver gain with and without the sink. With -31 dBm two-tone Tx power and -28 dBm close-in jammer, the measured TB without and with the auxiliary path were 62.5 dB and 69 dB respectively. Hence, this filtering technique improves the TB by 6.5 dB. A similar improvement is observed in the IIP_2 performance. The close-in IIP_3 was measured with two tones at 1.25 MHz and 2 MHz offset from the LO. The close-in third-order distortion is due to the nonlinearity in the TIA and the blockers are close to baseband. Hence, as expected, the auxiliary path does not improve this performance. The auxiliary path degrades the noise figure by 1.7 dB. This is attributed to the noise of the auxiliary mixer, which folds the auxiliary TIA noise and LO Buffer noise into the signal path. Comparison with other works is shown

Table 5.1: Measured performance

Performance	w/o Aux	w/ Aux	Units
Rx Freq	1960		MHz
Tx Freq	1880		MHz
STJ[1] Freq	1961.25		MHz
V_{DD}	2		V
I_{DC} LNA	22		mA
I_{DC} LO Divider	4		mA
I_{DC} LO Buffer	23		mA
I_{DC} TIA	8		mA
V_{DD} Aux LO Buffer	0	3	V
I_{DC} Aux LO Buffer	0	8	mA
I_{DC} Aux TIA	0	12	mA
Gain	45	45.3	dB
NF	3.1	4.8	dB
TB	62.5	69.0	dB
IIP_2	39.5	46.0	dB
IIP_3 (Close in)	-5.3	-4.8	dBm
S_{11}	$<$-17	$<$-17	dB

[1]Single tone jammer (STJ) for three-tone triple-beat (TB) test.

in Table 5.2. This design has better TB performance than other designs at 1.96 GHz.

5.5 Conclusion and Discussion

A new technique for eliminating the interstage SAW filter was presented. The receiver nonlinearity is attributed to the voltage swing at the output of the mixer due to the downconverted Tx signal. This problem was solved by sinking the Tx signal through an auxiliary path, which comprised of another downconverting passive CMOS mixer cascaded with a transimpedance amplifier. This mixer further downconverts the Tx signal to low frequency which is filtered by the TIA.

Three tone triple-beat (TB) test is used to characterize the cross-modulation linearity of the receiver. The proposed technique improved the TB performance by 6.5 dB, while the IIP_2 was also improved by 6.5 dB. The auxiliary path has no significant

Table 5.2: Measured Receiver Performance and Comparison to other CMOS Receivers

Performance	[12]	[89]	**This Work**	Units
Frequency	1960	1960	1960	MHz
Gain	37.1	32	45	dB
NF	3.0	9.2	3.1/4.8[1]	dB
IIP_2	+62.5	+50.8	+46[2]	dBm
In-band IIP_3	-7.4	-	-4.8	dBm
IIP_3	+4.7[3]	+9.5	+6.6[3]	dBm
TB	65.3	-	69	dB
LNA+Mixer Idd	21	20	22	mA
Vdd	1.3	1.5	2	V
Technology	65nm	0.13um	0.18um	CMOS

[1]With cancellation circuit. [2]Without calibration. [3]Calculated from the triple beat (TB) performance.

impact on the receiver gain and close-in IIP_3. However, the NF performance is degraded by 1.7 dB, which is attributed to the auxiliary mixer which folds the auxiliary TIA noise back into the signal path. This chapter has been submitted for review for the following publication:

1. H. Khatri, P. S. Gudem, and L. E. Larson, "A SAW-less CMOS CDMA receiver with active Tx filtering," submitted to *IEEE Custom Integrated Circuits Conf.*, CICC, 2009.

Chapter 6

Conclusion

This dissertation focuses on finding a monolithic solution for the problem of transmitter leakage in a frequency division duplexer transceiver system. In these systems, the transmitter signal leaks into the receiver section and poses stringent IIP_2 and cross-modulation IIP_3 specifications. There are several techniques for addressing this problem. These approaches can be broadly categorized into three categories:

– Replacing the SAW filter with an on-chip filter.

– Tx signal cancellation using feed-forward or feedback mechanism in the LNA.

– Filtering the Tx signal in the downconverter.

In this work, firstly, passive filters were designed and implemented using on-chip MIM capacitors and bond-wire inductors. This technique successfully suppressed the Tx leakage signal, while maintaining the linearity requirements. The mutual inductance properties of bond-wire and its impact on the filter performance was studied in detail and a novel bond-wire configuration was proposed for address the adverse affect of parasitic mutual inductance. The filter was implemented for a WCDMA system with Rx-Tx separation of 190 MHz. However, for other system like CDMA-2000, this separation is merely 80 MHz, where the filter suppression is not sufficient. Furthermore, the filter had around 10 dB noise figure and required a corner of the chip for its bond-wire configuration.

Moving forward with an active approach, the linearity of passive mixer is studied in detail to understand the bottleneck of the receiver linearity. The mixer linearity was studied for frequency dependent source and load impedances using Volterra series

analysis. The analysis revealed that the mixer linearity can be improved by reducing its load impedance at all the frequencies, especially, at the downconverted Tx frequency. In principle, this approach reduces the voltage swing at the mixer output node and hence improves the switch linearity. Experiments were conducted using passive mixers with different load impedances and a close agreement was observed with the calculated response.

Another study was conducted to understand the MOS transistor model for a passive mixer, where the transistors are biased at zero drain-source voltage (V_{DS}=0). It was observed that many industry standard models like BSIM3v3, BSIM4, EKV etc fails to predict the correct nonlinear behavior of the transistor. This was attributed to the discontinuity in the second-order derivative of drain-current with respect to the drain-source voltage at V_{DS}=0. This phenomenon was explained using Volterra series analysis.

With a good understanding of the receiver linearity bottleneck due to the passive mixer, a novel filtering technique was proposed to reduce the mixer output impedance at the downconverted Tx frequency. To filter off the downconverted Tx signal after the downconversion, an active bandpass filter is placed in shunt with the TIA. Unlike the traditional implementations, this filter is constructed with another passive mixer having LO signal close to the downconverted Tx frequency. In principle, this mixer downconverts the Tx current at the main mixer output to a lower frequency band, which is then filtered by a low-pass filter. The receiver was implemented in 0.18 μm CMOS process and the measured results were found to be in accordance with the theory.

Appendix A

Power-series DC Parameter Extraction of a CMOS Transistor

For a CMOS transistor biased with a fixed body and gate voltage, the large signal drain current, i_D, is a function of drain and source voltages referred to the bulk, rather than the large-signal drain-source voltage, v_{DS}. Hence, i_D can be expressed as,

$$\begin{aligned} i_D = {} & g_1 v_D + g_{2_D} v_D^2 + g_{3_D} v_D^3 + \dots \\ & - g_1 v_S + g_{2_S} v_S^2 + g_{3_S} v_S^3 + \dots \\ & + g_{2_{D\&S}} v_D v_S + g_{3_{2D\&S}} v_D^2 v_S + g_{3_{D\&2S}} v_D v_S^2 + \dots, \end{aligned} \tag{A.1}$$

This equation can be rewritten as,

$$\begin{bmatrix} V_D - V_S \\ V_D^2 \\ V_D^3 \\ V_S^2 \\ V_S^3 \\ V_D V_S \\ V_D^2 V_S \\ V_D V_S^2 \end{bmatrix}' \begin{bmatrix} g \\ g_{2_D} \\ g_{3_D} \\ g_{2_S} \\ g_{3_S} \\ g_{2_{D\&S}} \\ g_{3_{2D\&S}} \\ g_{3_{D\&2S}} \end{bmatrix} = \begin{bmatrix} I_D \end{bmatrix} \tag{A.2}$$

$$\Rightarrow \qquad \mathbf{V} \qquad \mathbf{G} \qquad = \mathbf{I}, \tag{A.3}$$

where, V_D, V_S and I_D are the DC drain and source voltages, and, DC drain current respectively. From the DC simulation or measurement, the drain current can be obtained for numerous values of V_D and V_S. From n such evaluations, $\mathbf{V}$ and $\mathbf{I}$ will be $n \times 8$ and $n \times 1$ matrices respectively, with each row representing a measurement for particular V_D and V_S. Using singular value decomposition (SVD) [90], unitary matrices $\mathbf{X}$, and $\mathbf{Y}$ of sizes $n \times n$ and 8×8 respectively, can be obtained, such that,

$$\mathbf{V} = \mathbf{X}\mathbf{\Sigma}\mathbf{Y}', \tag{A.4}$$

where, $\mathbf{\Sigma}$ is an $n \times 8$ diagonal matrix. Equation (A.3) can be solved by finding the pseudo-inverse of $\mathbf{V}$, defined as,

$$\mathbf{V}^{+} = \mathbf{Y}\mathbf{\Sigma}^{+}\mathbf{X}', \tag{A.5}$$

where, $\mathbf{\Sigma}^{+}$ is transpose of $\mathbf{\Sigma}$ with every element being replaced by its reciprocal. Thus,

$$\mathbf{G} = \mathbf{V}^{+}\mathbf{I}. \tag{A.6}$$

This technique computes the least mean-square values of the coefficients in (A.1).

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