Title
A capacitive air touch sensor system in 65nm CMOS technology

Author
Hsieh, Ying-Ying

Publication Date
2012

Peer reviewed|Thesis/dissertation

UNIVERSITY OF CALIFORNIA

Los Angeles

A capacitive air touch sensor system in 65nm CMOS technology

A thesis submitted in partial satisfaction of the

requirements for the degree Master of Science

in Electrical Engineering

by

Ying-Ying Hsieh

2012

ABSTRACT OF THE THESIS

A capacitive air touch sensor system in 65nm CMOS technology

by

Ying-Ying Hsieh

Master of Science in Electrical Engineering

University of California, Los Angeles, 2012

Professor Mau-Chung Frank Chang, Chair

In this thesis, the new methodology of an oscillator-based capacitive air touch sensor system is introduced for future touch screen technology. This high sensitivity and low power solution is based on oscillation frequency shifts for air touch screening position identification with improved touch sensitivity and extended reliability.

This system includes two parts: first, analog circuits are used to sense signals from the antenna, and then digital circuits are used to determine and analyze the detected human's finger positions.

The system is designed and implemented using a 65nm CMOS technology. It is capable of detecting up to 20fF capacitance difference, which is 50 times more sensitive than current projected-capacitive touch screen products. With fixed 1V supply voltage, the power of the entire system is only 1.3mW. The core size is 1mm by 1.2mm, which is compact enough to be adopted in any commercial products.

The thesis of Ying-Ying Hsieh is approved.

Lei He

Tatsuo Itoh

Mau-Chung Frank Chang, Committee Chair

University of California, Los Angeles

2012

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ACKNOWLEDGEMENTS

I would like to thank my advisor, Professor Frank Chang, for providing the opportunity to do research and work with other PhD students in the High Speed Electronics Lab. Without the experience and knowledge I learned in this lab, it would not be possible to complete the thesis. I also want to thank Frank Hsiao, a PhD student in the High Speed Electronics Lab, for helping to solve the problems I encountered on this research topic. Without his help, I would not be able to realize this thesis.

I started working on this project at the beginning of my second academic year of graduate school in UCLA. Within this year, I have learned how to materialize a real circuit from a simple idea, and also how to co-operate with other engineers to achieve the goal. All of the experience will definitely help me develop any future work in my career.

In the end, I would like to show appreciation to my family and friends for the support they provide in my graduate school studies.

CHAPTER 1

Introduction

1.1 Research Motivation

There is no doubt that touch screens are rapidly becoming mainstream in the field of handheld telephony. A device with a touch screen is preferred, and all devices imaginable are now available with a touch screen mode.

Since the iPhone® was introduced in 2007, projected-capacitive touch has grown more than 100-fold, and it shows no signs of slowing down [1]. In contrast to resistive touch screens, capacitive touch screens gives a comparatively better image. Figure 1 shows the system block diagram of a capacitive touch screen.

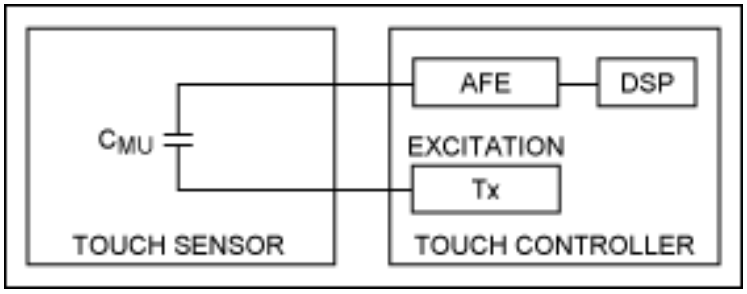

Figure 1 System block diagram of a generalized mutual-capacitance system

We can anticipate that capacitive touch screens will overwhelm the market in the future. But the capacitive touch screen also has a defect: sensitivity to finger touch. To make sure the capacitive touch screen can work well, first the system should be very sensitive to the slight capacitance change upon the approach of a human's finger. Also, in order

not to affect performance, the screen needs to be kept clean at all times, or the touch sensor cannot detect the finger.

The current touch screen technology may confront another important issue: when a human's finger touches the screen directly, there might be an electrostatic discharge (ESD) from the finger to the device, which may cause ESD induced time latch-up problem on the touch screen. In the end, the system might not able to operate properly, possibly getting stuck or detecting the movement of the human's finger incorrectly.

To overcome these defects, we envision changing the touch screen into an air touch screen. Besides, we can decrease the frequency with which we touch the screen, which can also help maintain cleanliness and extend the life of the screen.

1.2 Organization of Thesis

In Chapter 2, I will first show the inspiration of this system, and then the entire system and the design challenge of this work will be presented. A review of the theory used in the research will also be given.

In Chapter 3, each block of the system will be discussed separately in the sub-section, including the topology chosen, spec consideration, and the simulation result. Section 3.1 presents the design and simulation of the oscillator; section 3.2 provides the design and simulation of the two-to-one op-amp; section 3.3 presents the driver used in integration and driving clock; section 3.4 provides the switch used to connect the antenna and the system; section 3.5 will discuss the antenna used in this system.

In Chapter 4, an overview of the system integration will first be given, such as spec determination and the difficulties met in integration of analog parts and digital parts. The integration and simulation of the air touch sensor system will be presented. Also I will discuss several cases we need to consider when doing simulation to approach the real conditions.

Finally in Chapter 5, a conclusion and the performance will be provided.

CHAPTER 2

Research Overview

2.1 Inspiration

The theremin (shown in Figure 2), was originally the product of Russian government-sponsored research into proximity sensors. The instrument was invented by a young Russian physicist named Lev Sergeivich Termen after the outbreak of the Russian civil war. It is an electronic musical instrument controlled without discernible physical contact from the player [2].

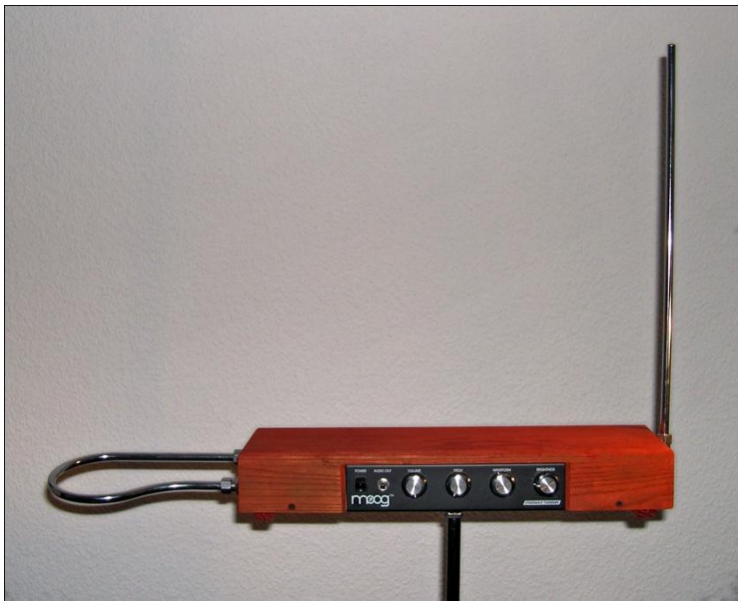

Figure 2 Picture of theremin, the loop antenna on the left controls the volume while the upright antenna controls the pitch

The theremin is rare among musical instruments in that it is played without physical contact. The musician stands in front of the instrument and moves his or her hands in the proximity of two metal antennas. The distance from one antenna determines frequency (pitch), and the distance from the other controls amplitude (volume).

We can use the principle of the theremin on the air touch sensor system: the distance from human's finger to the antenna will determine the frequency; with different frequency, we can judge if there is a human's finger approaching.

2.2 Overview of the Capacitive Air Touch Sensor System

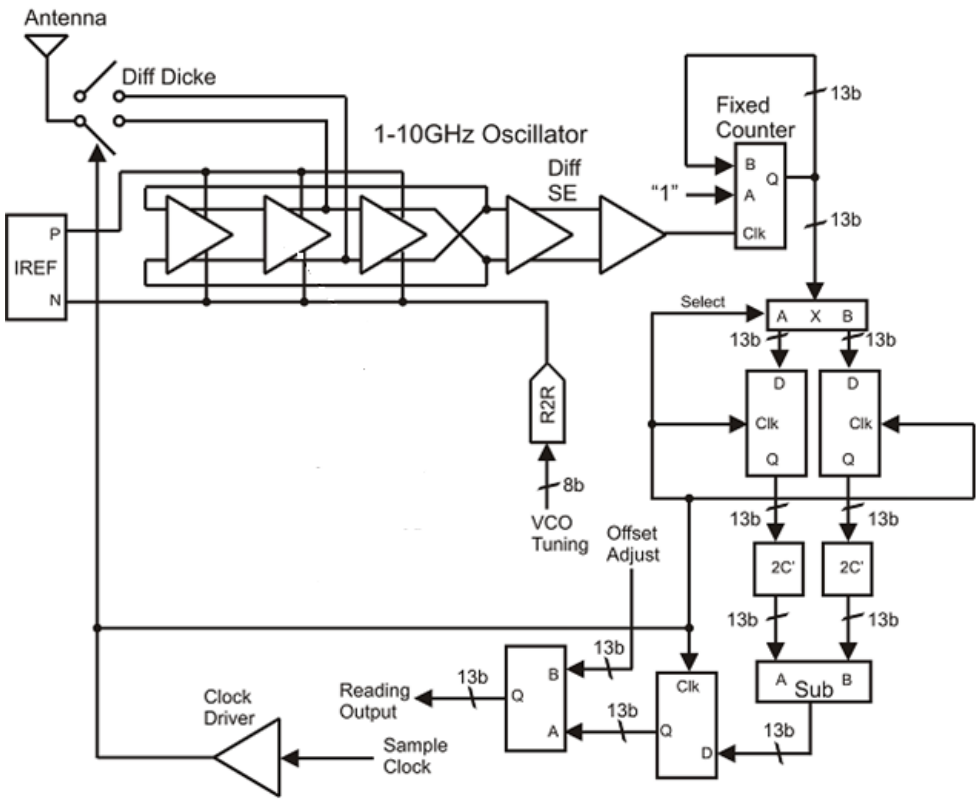

Figure 3 System block diagram of the air touch sensor

The differential antenna is designed to receive signals in the air, when there is a human's finger approaching, the antenna will detect a small capacitance difference, which is the key point for this system to operate.

The switches used in the system are considering the concept of dicke switches. When the switches turn on, they connect to the antenna with 50-ohm impedance matching; when the switches turn off, they will reset thru the 50-ohm loading. The switches are used to make a distinction between two different conditions:

(1) When the switches turn on: the antenna is connected to the oscillator, and the capacitance change from the antenna can affect the input capacitance of the oscillator.

(2) When the switches turn off: the antenna is isolated from the oscillator, so the input capacitance of the oscillator is fixed.

The switches are controlled by a slower clock (around 1MHz) to determine whether they turn on or off.

When a human's finger approaches the antenna, there should be a slightly capacitance change at the input terminal of oscillator.

$$f = \frac{1}{2\pi\sqrt{LC}} \propto \frac{1}{\sqrt{C}}$$

Thru the two-to-one op-amp and analog-to-digital driver, the analog blocks can generate square waves with different frequency. When there is a human's finger approaching, the capacitance should be sum of the input capacitance of oscillator and capacitance at antenna (affected by human's finger). From the formula above, we can know that the

oscillation frequency decreases when capacitance increases, so the generated square wave will have lower frequency. By using the counter and the subtractor, we can calculate a number that represents the difference between the case with human's finger and without human's finger, and then compare the number with the threshold we set:

$$number > threshold \rightarrow with\ finger$$

$$nubmer < threshold \rightarrow without\ finger$$

2.3 Consideration of Sensitivity

There must be a big enough difference between frequencies of two square waves (with human's finger and without human's finger) so that we can determine the result easier. The sensitivity of the system is a very important factor that might affect the difference we detected, and can be divided into three parts: sensitivity of the oscillator, the value of the capacitance that the human's finger might cause, and the length of sampling window. Since the sensitivity of the oscillator will be determined by the input capacitance itself, if we can keep input capacitance low enough, the sensitivity can become higher. The capacitance difference a human's finger will cause in the current touch screen system is around 1pF. Using remote air touch technology, the capacitance difference will be smaller. We set this possible capacitance difference to be 100fF, which is 90% smaller than the current touch screen spec. This capacitance difference might differ when the human's finger moves nearer or further from the screen. If the designed oscillator has input capacitance no greater than several pF, then the functionality of sensing the human's finger should be good enough.

Additionally, the phase noise of the oscillator also plays a role in sensitivity performance of the air touch sensor system [3]. If the phase noise is too high, it might generate jitter problems in the square wave imported to the digital block, and might cause the digital circuits to make incorrect decisions. That is, the smaller the phase noise of the oscillator is the better. The definition of phase noise is the noise power relative to the carrier contained in a 1Hz bandwidth centered at a certain offsets from the carrier which is clearly shown in Figure 4, and the unit is dBc/Hz.

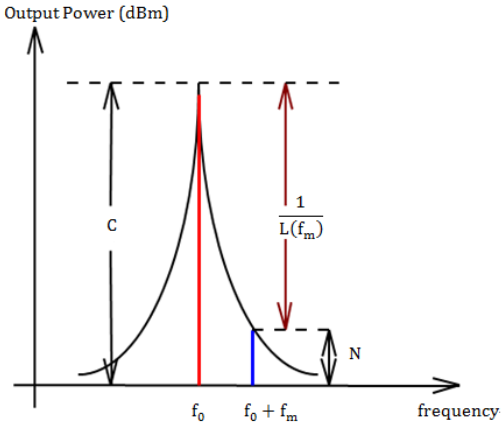

Figure 4 Definition of phase noise

The formula to calculate the phase noise is provided below:

$$L(f_m) = \frac{N(1\text{Hz BW})}{C}$$

$$L(f_m) = \frac{FKTB}{2P_{avs}}\left(\frac{1}{f_m^3}\frac{f_0^2 f_c}{4Q_L^2} + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2 + \frac{f_c}{f_m} + 1\right)$$

F: noise factor of transistor

K: boltzmann's constant

T: noise temperature of load

P_{avs}: average output power of oscillator

f_m: offset frequency

Q_L: Q factor of resonant circuit

f_0: center oscillation frequency

f_c: corner frequency of transistor

From the above formula, we know that if we want phase noise ($L(f_m)$) to be as small as possible, we can:

1. Choose transistor with lower noise factor
2. Choose transistor with lower corner frequency
3. Choose resonant circuit with higher Q factor
4. Under same bias, acquire largest power

Thus, we can either improve the sensitivity of the oscillator relative to its input capacitance, control the phase noise of the oscillator by choosing desirable higher Q topology or lengthen the clock which controls the switches to prolong the sampling window to obtain higher sensitivity of the system.

CHAPTER 3

Circuits Design and Discussion

3.1 Voltage-controlled Oscillator

Since we do not want to make interference to other devices (such as Blue-tooth devices operating at 2.4GHz), we set the oscillation frequency range from 1GHz to 10GHz originally, with such a wide tuning range, we can easily acquire the desired band by tuning the control voltage of oscillator.

The most challenge part of designing the oscillator is we need to carry a very wide tuning range, and keep the phase noise and power dissipation low at the same time. As mentioned in previous chapter, if the phase noise on the oscillator is too high, the square wave given to digital counter might have jitter problem, which may affect the decision of the digital block; while the system is used in the product, the power dissipation should not be too high. That is, when designing the oscillator, we need to monitor phase noise, power and tuning range (linearity) carefully, and find the best trade-off.

To decide the topology of the oscillator, two structures are considered: LC-tank oscillator or ring oscillator. The table of comparison between LC-tank topology and ring oscillator is shown next page (Table 1):

Considering the pros and cons of two structures, we choose ring oscillator, since the linearity (related to the tuning range) is the most important issue in the design. There is a trade-off between lower jitter and higher linearity (due to bandwidth), we need to

carefully control the phase noise when we increase the performance of linearity [4]. Besides, we want total system power below 4 mW. That is because the system is used on the glass, the power is need to be low to avoid burning issue. The input capacitance should be small enough (sensitivity issue) considering the finger will not produce more than 1pF capacitance change.

LC-tank oscillator	Ring oscillator
Higher Q (lower phase noise)	Lower Q (higher phase noise)
Larger area (inductor is used)	Smaller area
Smaller power	Larger power
Lower tuning range (10%~20%)	Higher tuning rang (up to 50%)

Table1 Comparison of LC-tank topology and ring oscillator

At first oscillation frequency from 1GHz to 10GHz is targeted, but later we find that there is a limitation in 65nm technology: the digital part can only deal with frequency no more that 3GHz. As the reason, we need to redesign the ring oscillator, now the oscillator frequency is from 1GHz to 5GHz in order to match up the digital part. To cut down the oscillation frequency, more identical delay cells in the ring oscillator are added (since we do not want to change the size of transistors anymore), this may increase the power and the area, but we can still meet the spec we set earlier.

Considering future uses, we target one delay cell to reach higher oscillation frequency (up to 40GHz with three delay cells). If the numbers of ring cell increase, the lower oscillation frequency can be obtained. If we can design digital circuits with higher speed in the future (now the limitation is 3 GHz), we can just simply reduce the numbers of ring

cell to acquire higher frequency. The structure of the delay cell used in the ring oscillator is shown in Figure 5.

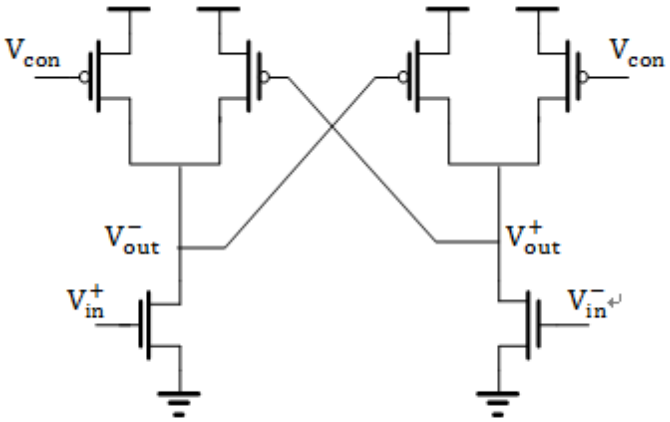

Figure 5 Delay cell of the ring oscillator

The number of delay cell used in the ring oscillator will determine the oscillation frequency, typically when the number increases, the oscillation frequency will decrease, and vice versa. To make sure the ring oscillator will oscillate successfully, if the number of delay cell is even, then the connection between two stages needs to be crossed. For odd numbers of delay cell, there is no need to cross the connection. We use night stages of delay cell in this designed ring oscillator, and the block diagram is shown at Figure 6.

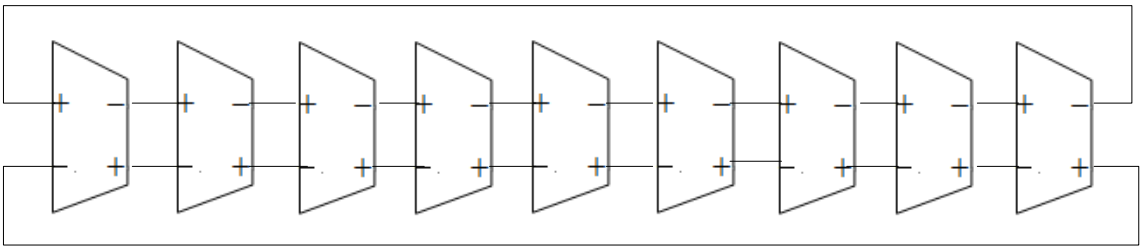

Figure 6 Overall block diagram of the ring oscillator

Considering Miller's effect, the capacitances between gate terminal and drain terminal can be transferred into two separate capacitances:

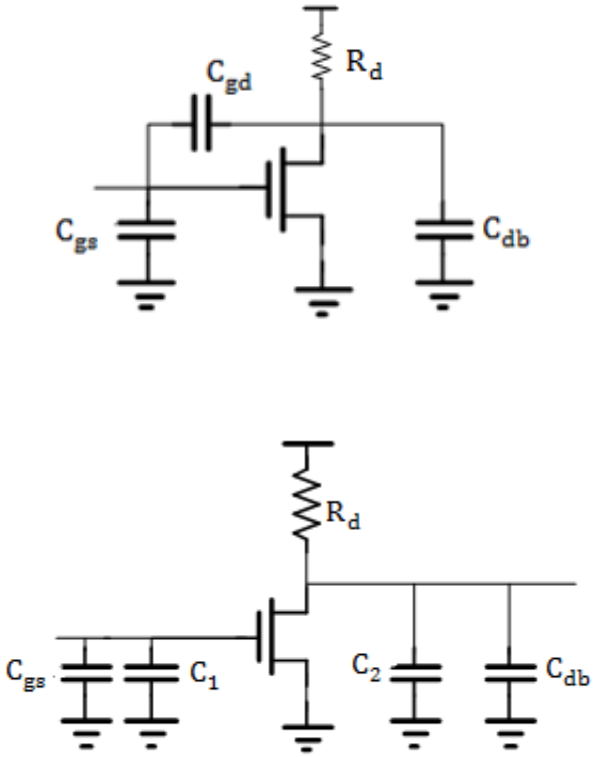

Figure 7 Miller's effect of the transistor

As shown in Figure 7, the upper circuit is the original expression of transistor, and the bottom one is the way how we disconnect the capacitance between gate and drain terminals:

$$C_1 = C_{gd}(1 + g_m R_d)$$

$$C_2 = C_{gd}(1 + \frac{1}{g_m R_d})$$

Where C_1 will affect the input capacitance of the ring oscillator, to improve the sensitivity of the entire system, we do not want the input capacitance of the ring oscillator be too high, or it might overwhelm all the system so that the system cannot be aware of small capacitance changing in the air. Since we know for current touch screen technology, a human's finger will cause around 0.5pF to 1pF capacitance change, we might need to carefully control the input capacitance of the ring oscillator. To decrease the value of C_1, we can decrease the value of g_m first, and we know:

$$g_m = uC_{ox}\frac{W}{L}(V_{gs} - V_{th})$$

So we can keep width of the input transistor small to suppress g_m. There is another benefit coming with suppressing g_m:

$$\text{thermal noise} = 4KTrg_m$$

For an analog/RF system, we want the noise to be as small as possible. Since flicker noise is almost fixed, if we can reduce the thermal noise, we can still keep the noise of the system low.

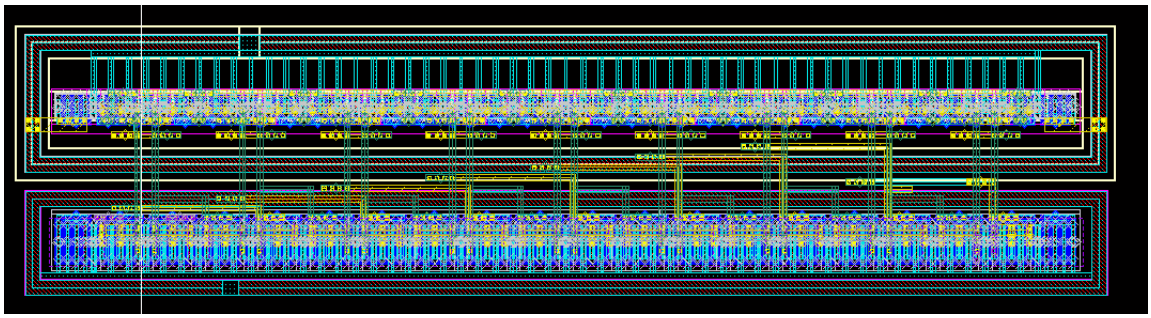

Figure 8 Layout of the ring oscillator

When the width and length of the transistor are carefully designed, we still need to consider the trade-off between linearity and phase noise. These two important specs will be discussed later. Figure 8 shows the layout of the ring oscillator.

Modulation sensitivity, which is also known as gain factor (K), help to describe the frequency variation when control voltage of the oscillator is changing. The unit of this factor is MHz/V. This parameter is the most important one for the designed oscillator, as we discussed before, we want to have wide range so that this product can be used worldwide without disturbing other devices. Figure 9 and Figure 10 shows the pre-simulation result and the post-simulation result separately.

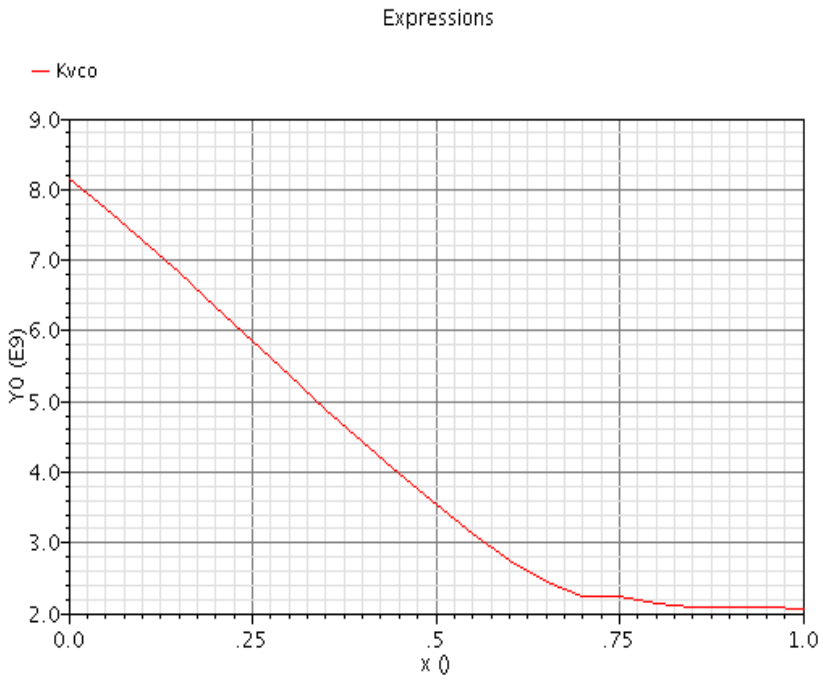

Figure 9 Pre-simulation result of gain factor of the ring oscillator

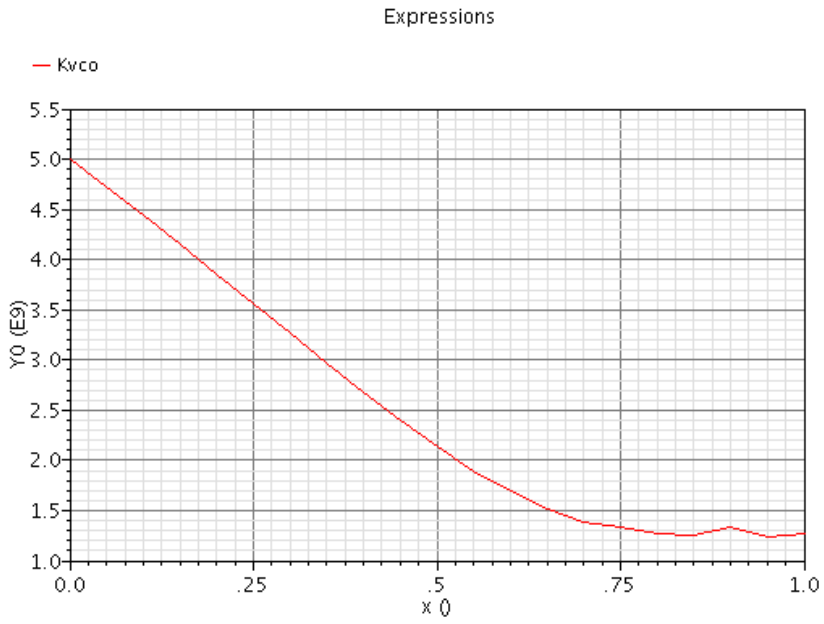

Figure 10 Post-simulation result of gain factor of the ring oscillator

The pre-simulation result shows the gain factor K equal to 6GHz/V, the oscillation frequency can change from 2GHz to 8GHz when the controlled voltage of the ring oscillator swings from 0V to 1V. The post-simulation result shows gain factor K equal to 3.8GHz/V, the oscillation frequency can change from 1.2GHz to 5GHz when the controlled voltage swings from 0V to 1V. To note that, since the highest frequency the digital counter can deal with under 65nm CMOS technology is around 3GHz, the post-simulation gain factor can perfectly match up the digital circuit with centering the oscillation frequency at 3GHz.

Besides gain factor K, there is another important spec for the designed ring oscillator, which is phase noise. As mentioned in previous chapter, if the phase noise is too high, it might generate jitter problem in the signal imported to the digital block, and might force the digital circuits determine decision incorrectly.

The formula to calculate the phase noise is provided below:

$$L(f_m) = \frac{FKTB}{2P_{avs}}\left(\frac{1}{f_m^3}\frac{f_0^2 f_c}{4Q_L^2} + \frac{1}{f_m^2}\left(\frac{f_0}{2Q_L}\right)^2 + \frac{f_c}{f_m} + 1\right)$$

Since TSMC 65nm CMOS technology is chosen, the thing we can do to improve phase noise is carefully control the Q factor of resonant circuit and the power of the oscillator, which also means to find the best trade-off between power, phase noise, and linearity (range). The phase noise performance of the designed ring oscillator is shown in Figure 11.

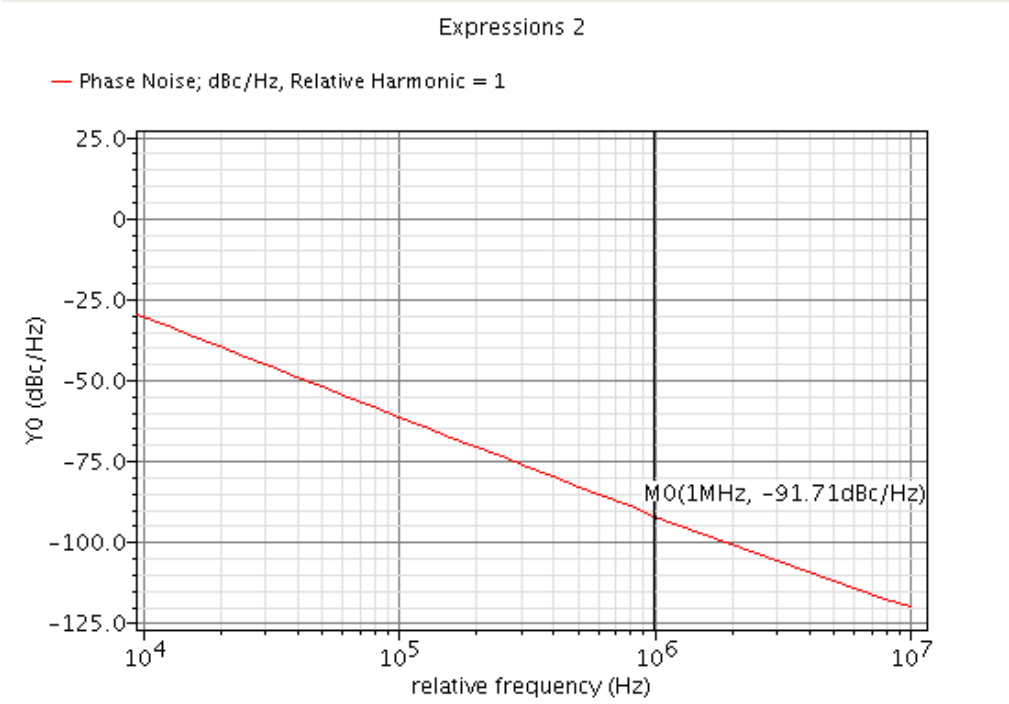

Figure11 Phase noise of the designed ring oscillator

3.1 Two-to-one Op-amp

For 65nm technology, the supply voltage is only up to 1V. As the reason, in order to have higher output swing (so the system will not saturate easily) we choose differential structure for the ring oscillator. But the digital counter is single-ended, so the two-to-one op-amp is needed to transfer differential-ended to single-end. We need to carefully design this op-amp so that there is no distortion in the signal and the power dissipation could not be too high.

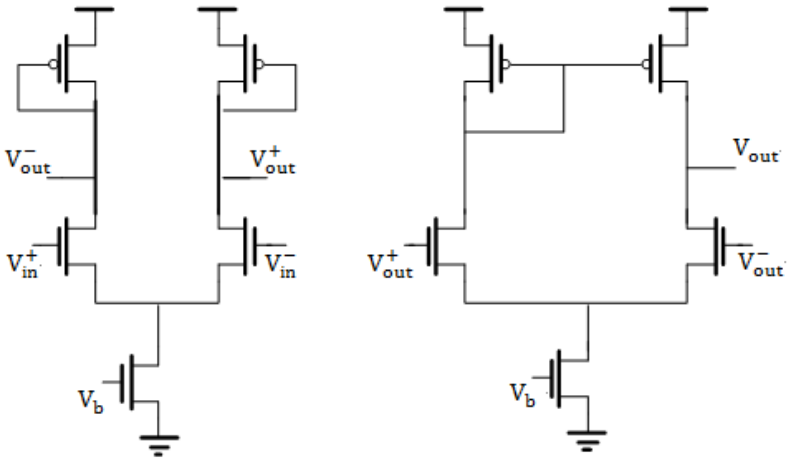

Figure 12 Structure of two-to-one op-amp

The Figure 12 shows the structure of the designed two-to-one op-amp, which is differential-ended input and single-ended output. The left circuit is used to rectify the signal from the ring oscillator. The re-shaped signal will approach ideal sine wave and will not saturate the supply voltage limitation which is equal to 1V. The right circuit cascaded after the left one will transfer differential-ended signal into single-ended signal so that it can be sent into digital counter. The Figure 13 shows the layout of the two-to-one op-amp.

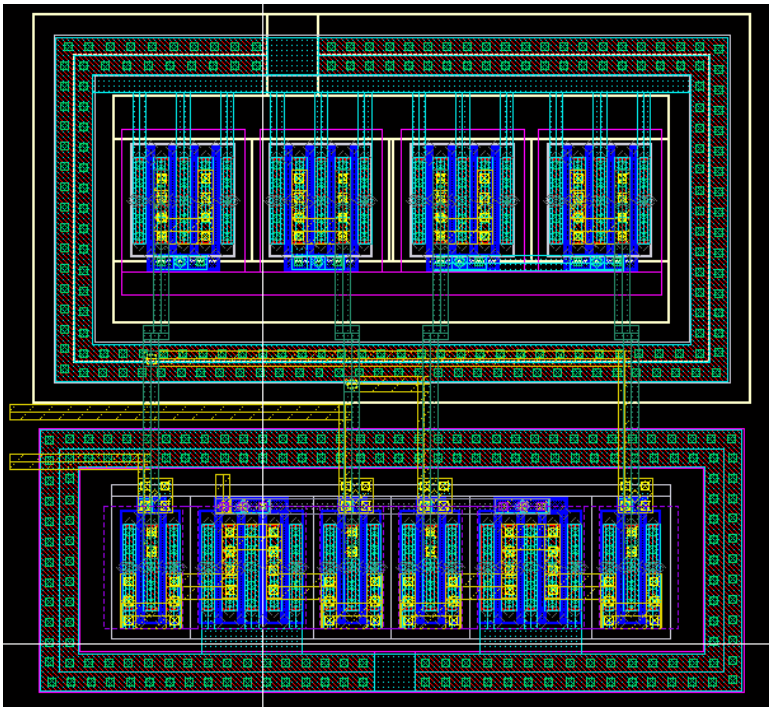

Figure 13 Layout of two-to-one op-amp

3.3 Analog –to-digital driver

Since analog and digital parts are separately designed, the output of the two-to-one op-amp cannot perfectly match the input of the digital counter. The analog-to-digital driver is added in the system to drive two parts successfully. We use fan-out method to design the driver, since the sizes are gradually increased, the matching and the capability of driving will be better. Figure 14 shows the structure of the designed analog-to-digital driver.

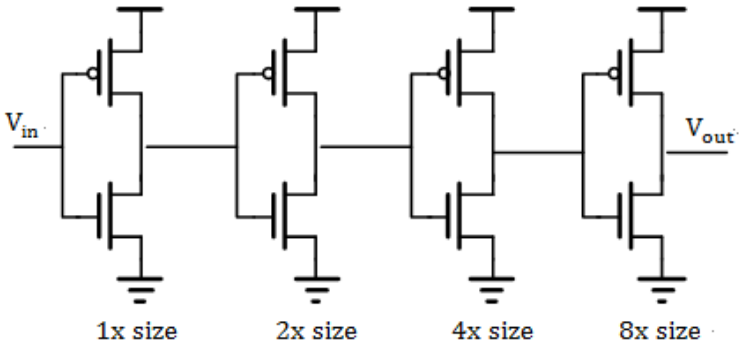

Figure 14 Structure of analog-to-digital driver

Since the size of the transistors in the driver is elaborately designed, the analog-to-digital driver can also be used as the clock driver, which drives the controlling clock for the switches. Figure 15 and Figure 16 shows the difference between case with driver and without driver.

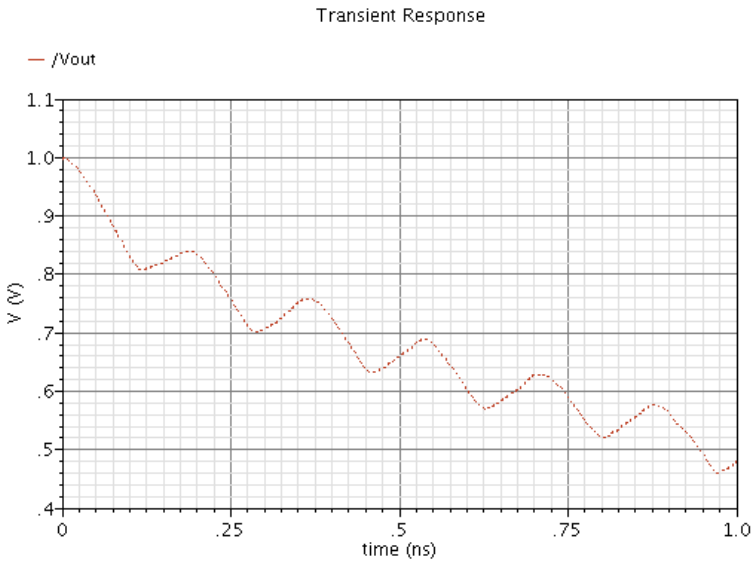

Figure 15 Signal imports to digital counter without analog-to-digital driver

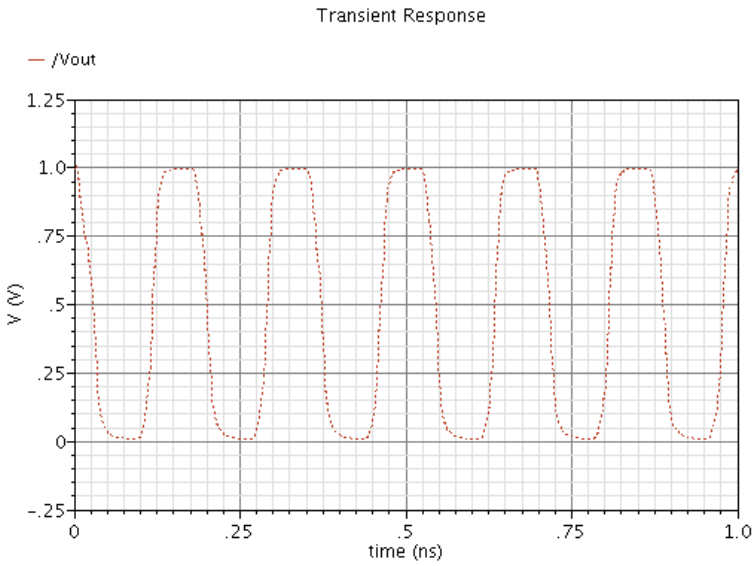

Figure 16 Signal imports to digital counter with analog-to-digital driver

A well-designed driver (also a buffer) can help increase the capability of driving and reduce distortion. It is obvious that with the help of analog-to-digital driver, the signal importing into the digital counter is perfect enough to be seen as ideal square wave. Figure 17 provides the layout of the designed analog-to-digital driver.

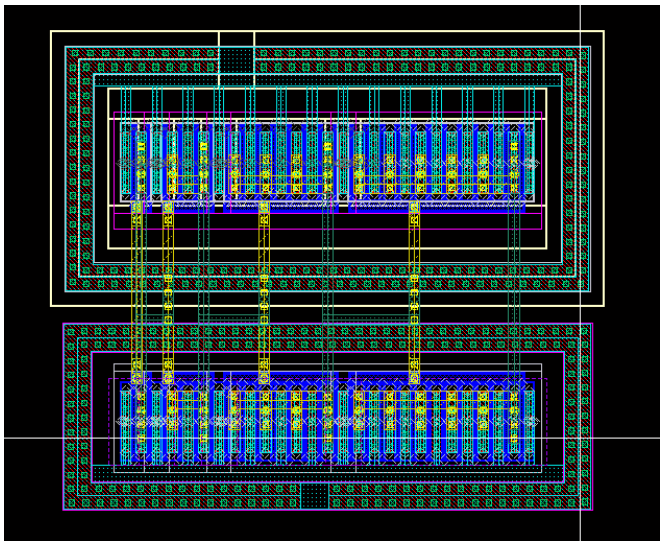

Figure 17 Layout of the analog-to-digital driver

3.4 Switch

When we use MOS transistor as analog switch, we need to consider the resistance between drain and source controlling by gate voltage. For a MOS transistor operating in triode (linear) region, the resistance can be expressed as:

$$R_{on} = \frac{1}{uC_{ox}\frac{W}{L}(|V_{gs}| - |V_{th}|)}$$

Complementary MOS switches structure is chosen: with proper control, NMOS and PMOS will turn on and off simultaneously. The NMOS transistor conducts for $0 \leq V_{in} \leq V_{DD} - V_{thn}$, while the PMOS conducts for $|V_{thp}| \leq V_{in} \leq V_{DD}$, then the structure can provide a rail-to-rail input and output range. Besides, since NMOS and PMOS are parallel together, on-resistance will be more linear than using NMOS or PMOS only [5] as shown in Figure 18.

To make switch being symmetric, connect body of NMOS to ground and body of PMOS to VDD. If body is connected to source, even if body effect can be ignored, the switch will be different looking from two different nodes.

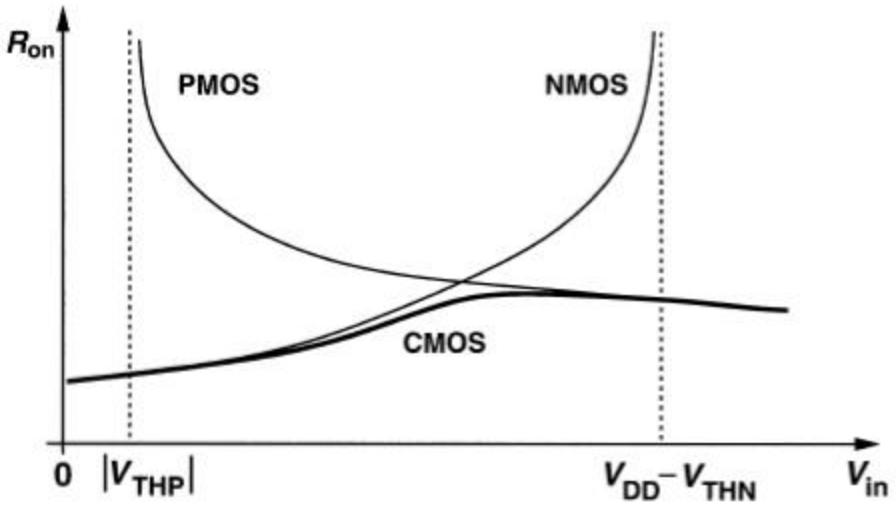

Figure 18 Variation of on-resistance of NMOS, PMOS, CMOS switches

The following Figure 19 shows the structure of the design complementary CMOS switch, while the Figure 20 shows the layout of the designed switch.

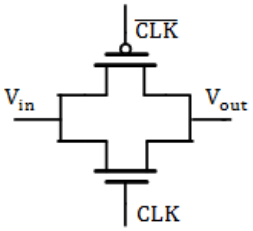

Figure 19 Structure of complementary CMOS switch

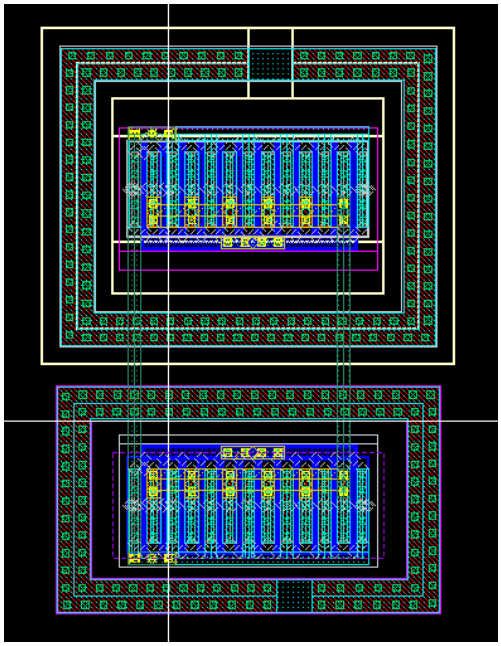

Figure 20 Layout of complementary CMOS switch

3.5 Antenna

The off-chip antenna is chosen when testing this system, and the antenna is differential structure to match up the differential ring oscillator. Since the antenna is soldered on PCB board separately, we need to make sure the transmission line on the PCB board has 50-ohm impedance for perfect matching.

CHAPTER 4

System Integration and Simulation

4.1 Overall Analog Blocks Integration

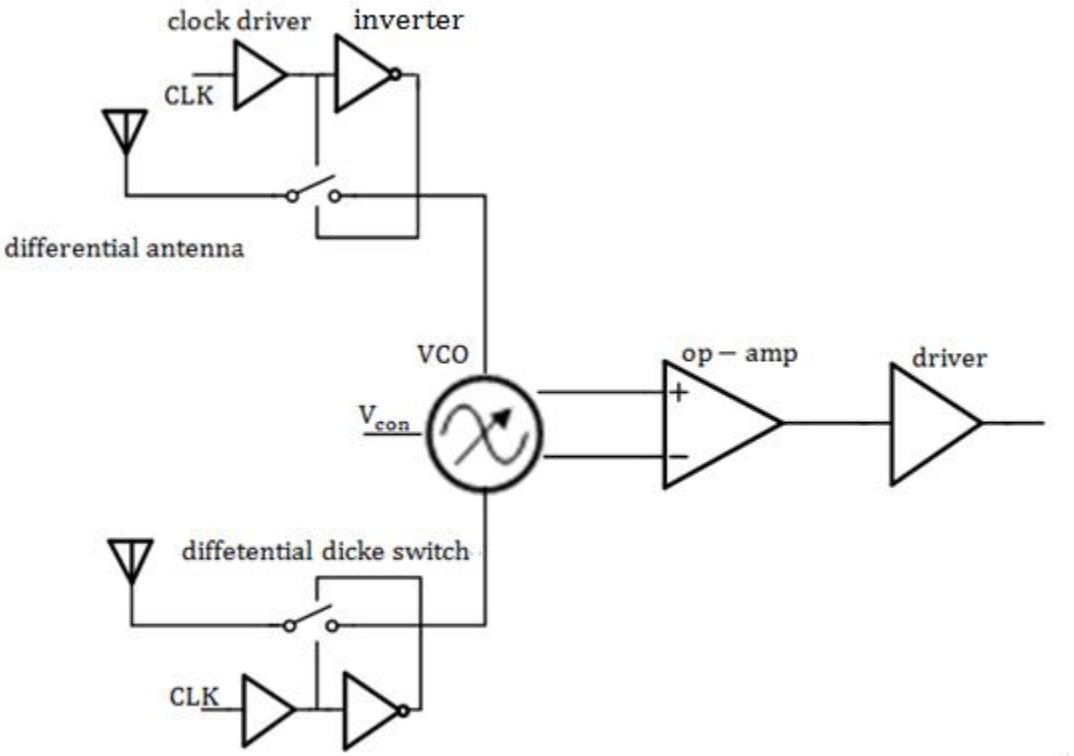

Figure 21 Overall connections of analog blocks

Compared with the original topology, the band-gap circuit is used to provide stable voltage supply to ring oscillator. When we correctly choose the topology of ring oscillator, the band-gap circuit can be removed. The clock driver and the inverter will provide controlling clock for the differential switches. The differential switches will

connect to the ring oscillator controlled by a tunable DC voltage (V_{con}), and followed by a two-to-one op-amp and an analog-to-digital driver. Finally the generated square wave will be provided to the digital counters and computation units to calculate the result.

In order to make analog parts integration easier, the size of layout, especially the height of each block needs to be strictly defined when doing layout of each blocks. So that the DC power supply (VDD/GND) of each block can be connected perfectly. Besides, the position to place each block needs to be elaborately designed. For example, the position of the clock driver could not be too far away from the differential switches, or there might be timing (delay) problem here. The metal used to connect each block should be wide enough to avoid burned-out conditions. Figure 22 shows the layout of all analog blocks integration, the layout is very compact and small enough to put in any product, the size is 16um by 45um.

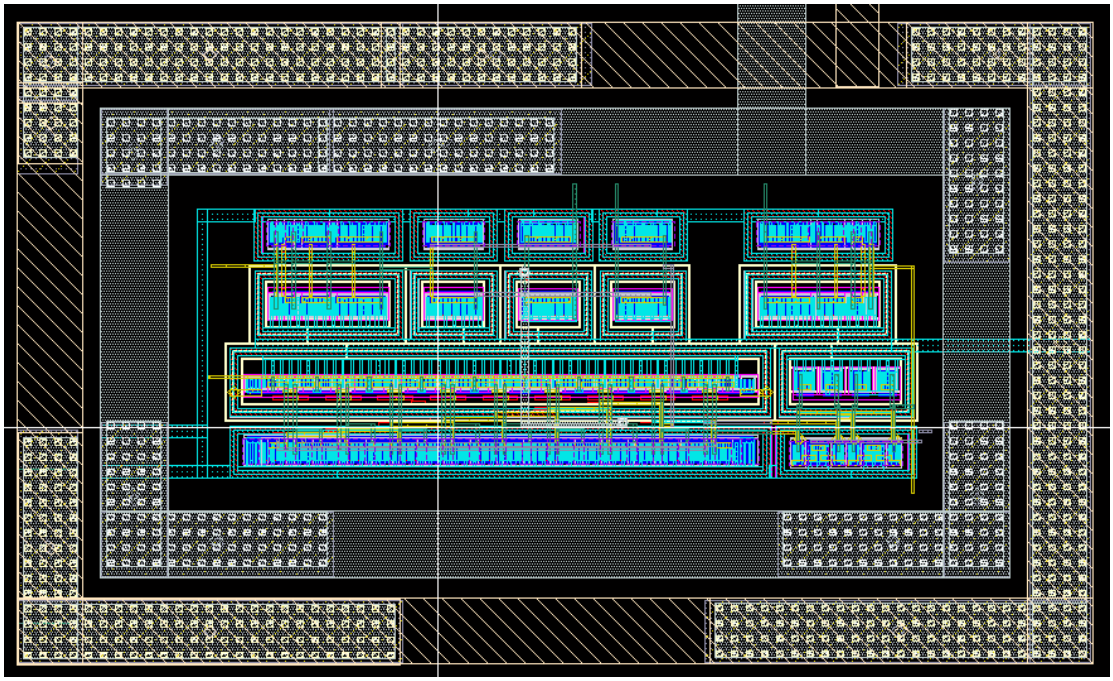

Figure 22 Layout of all analog blocks integration

4.2 Simulation for the integrated analog blocks

After all analog blocks are connected together, the simulation can be carried. The differential (subtracting) outputs of the ring oscillator should be an imperfect sine wave. When the signals go into the two-to-one op-amp, first thru the rectifying part, the signals should be a better sine wave with smaller amplitude (due to the structure of the rectifying part we designed), and after the transferring part, the signal should be an almost perfect square wave, since the signal will be amplified in these circuits. Finally, the signal imported by the analog-to-digital driver will be amplified again, so now the signal should be a perfect square wave.

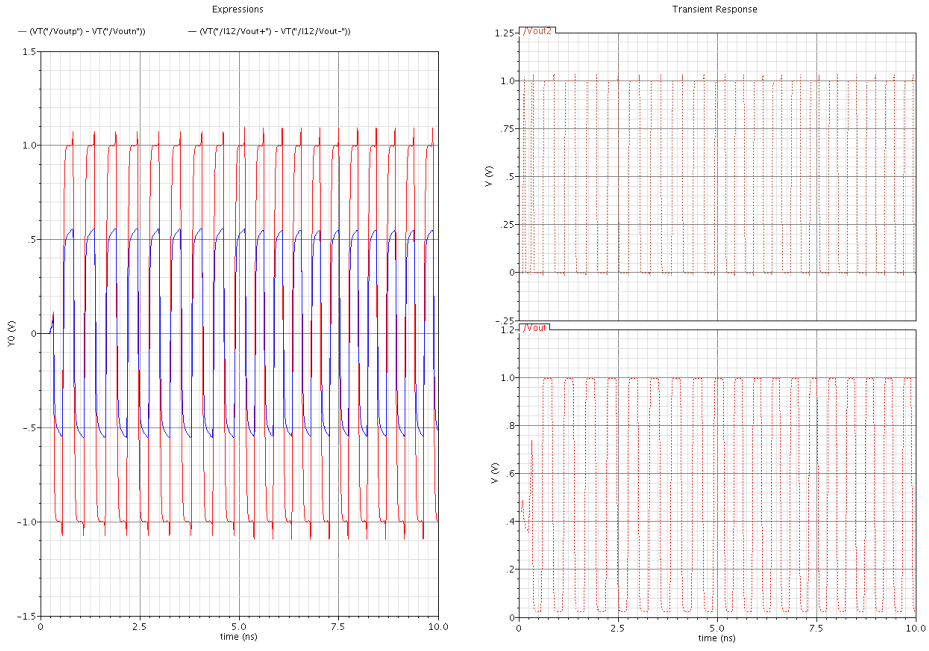

Figure 23 Simulation results of the integrated blocks

The simulation result shown in Figure 23 is same as we predicted, in the left block, the red imperfect sine wave with higher amplitude is the output of the ring oscillator; and the blue one with smaller amplitude is the output of the rectifying part in the op-amp. Since the signal is already rectified and re-shaped, it looks better than the original one. In the upper right block is the output of the transferring part in the op-amp, while the bottom right block is the output of the analog-to-digital driver. Compared these two plots, we can see that the bottom one is almost the perfect square wave, with all the spurs in the signal removed.

4.3 Simulation for the Integrated System

To confirm the functionality of the system, the analog parts are combined with the digital counter to do simulation. Considering the time and convenience of simulation, the sampling window (also equal to the length of the switches turning on or off) is set to 40ns. The digital counter is designed as a 14-bit outputs counter, since we need to transfer a 2GHz signal into a 1MHz one. In the case we set the sampling window short, only three or four bits of the outputs of the digital counter need to be plotted to make sure the functionality.

As shown in Figure 24, for the integrity of the system, the clock which is used to control the switches is generated by another digital block, digital computation unit. The generated clock is called “clk_fast”, which is eight times faster than the controlling clock (clk, which is used to control the switches). Besides providing the clock, the digital computation unit also helps do comparison and calculation of the difference between

signals from two sampling windows, and then determine if there is a human's finger approaching.

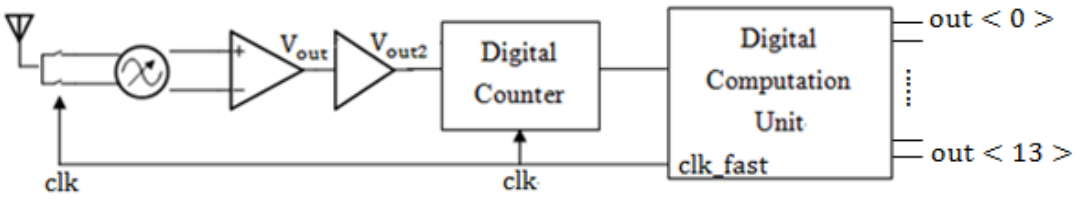

Figure 24 Block diagram of the analog blocks combined with the digital blocks

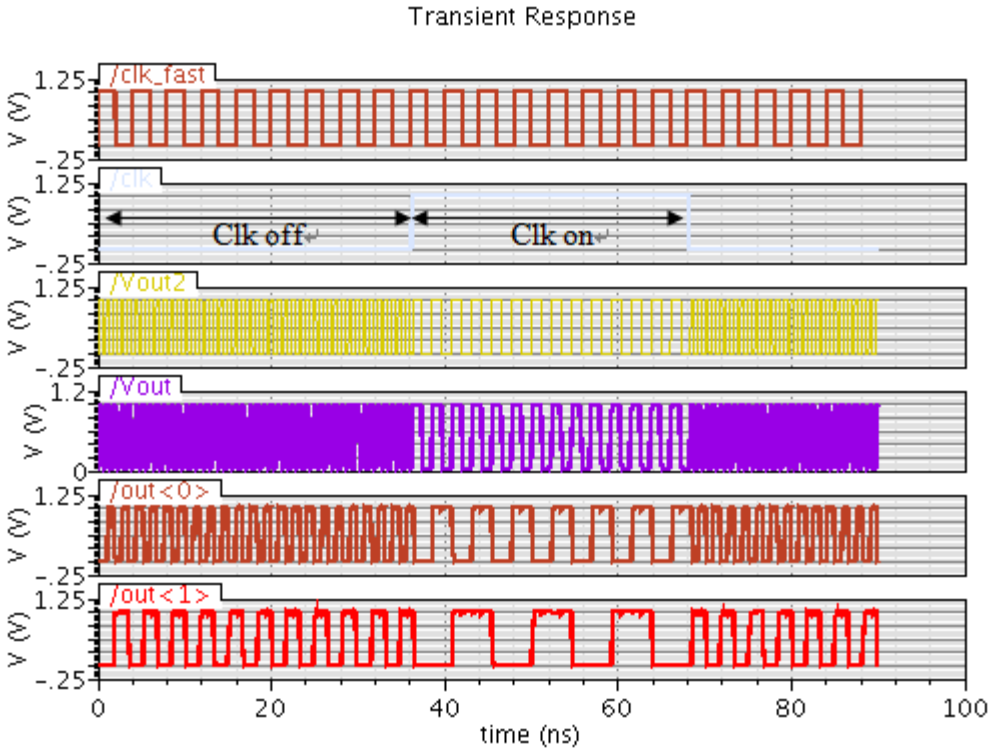

Figure 25 Simulation results of analog and partial digital counter outputs

The simulation in Figure 25 shows the result of the system, combined the result of “clk” and “Vout2”, we can see when the clock pulls down to zero (switches turn off), the capacitance of the ring oscillator is only the input capacitance itself, so the oscillation frequency should be a faster one; on the other hands, when the clock pulls up to one (switches turn on), the capacitance is the summation of the input capacitance of ring oscillator and the finger capacitance detected by the antenna, so the oscillation frequency should be a slower one. The result “Vout” is the output of the two-to-one op-amp, while the result “Vout2” is the output of the analog-to-digital driver. The result “Vout2” looks more like a perfect square wave than the result “Vout”, since the analog-to-digital driver will also help amplify signal again.

The result “Vout2” will import into the digital counter, we can see the result “Vout2”, “out<0>” and “out<1>” together, the counter will carry when the previous bit pulls up and down.

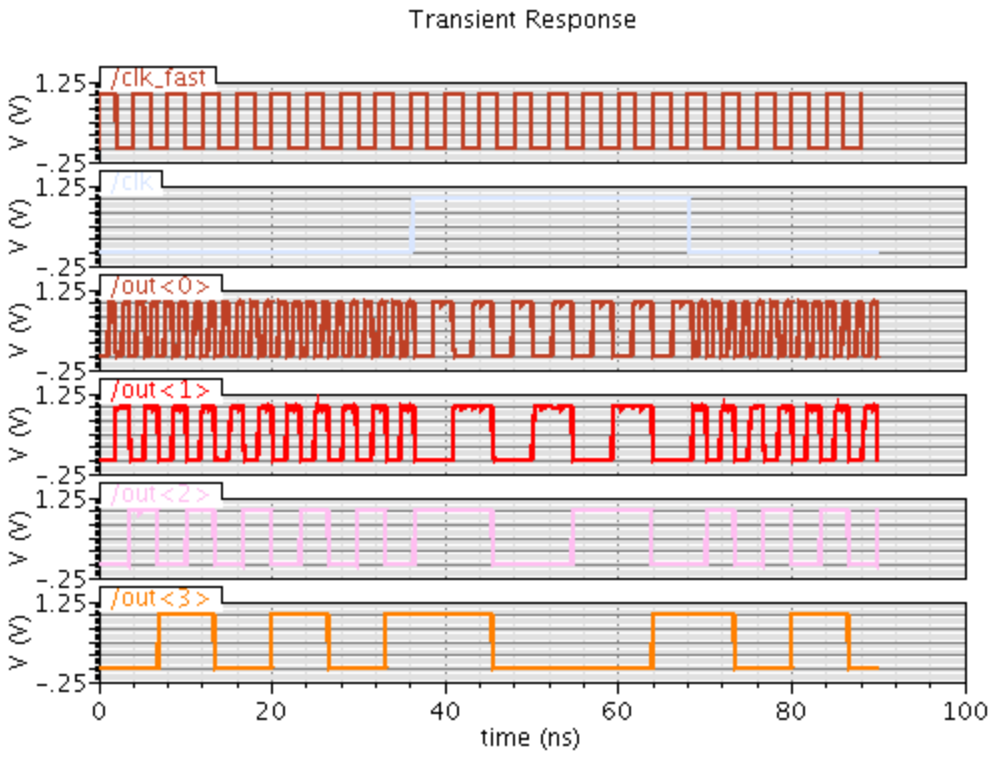

Figure 26 Simulation results of the digital counter outputs

Now we plot four outputs bits of the digital counter to see the result (Figure 26). From the simulation above, we can tell that the digital counter combined with the analog parts works correctly.

4.4 Simulation for the Integrated System in Realistic Condition

The way to determine if there is a human's finger approaching discussed above is inside the cadence simulation environment. For convenience, we plot the outputs of the digital counter to do judgment. But in realistic condition, we can only make decision based on the output of the digital computation unit which will connect to the measurement

machine. The following discussion will show the way to determine the result using the output of the digital computation unit:

The output of the digital computation unit is also a 14-bits binary expression. First we need to calculate the difference in cycles of the result “Vout2” between two sampling windows (one with switches on and the other one off). And then we plot the 14-bits output of the digital computation unit and transfer the binary expressions into decimal expressions. By comparing these two numbers, we can tell if the system make decision correctly.

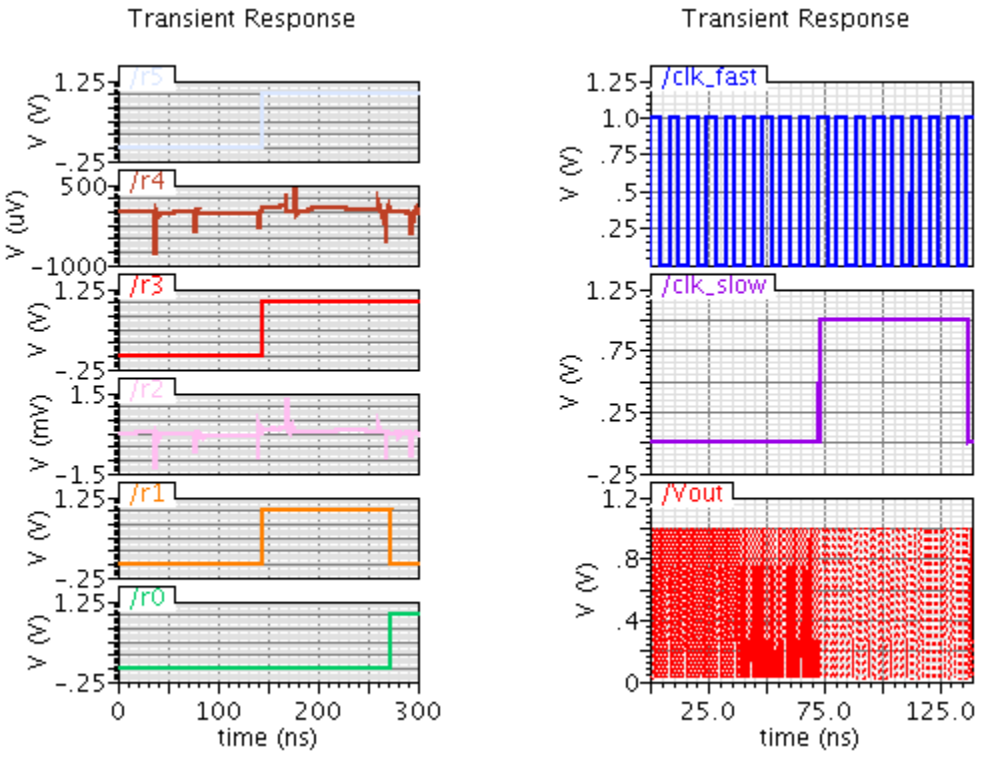

Figure 27 Simulation results of the analog and digital computation unit outputs

From the above simulation result (Figure 27), the left plot is the binary output of the digital computation unit:

r_0	r_1	r_2	r_3	r_4	r_5	Decimal
0	1	0	1	0	1	42

Table 2 Result of simulation in realistic condition

The right plot is the output of the analog parts, we can calculate the difference cycles of two sampling windows (one with switches off and one with switches on), and find the number is 44, compared with the outputs of the digital computation unit (42), there is a 6.7% error.

To confirm the system functionality, many testing cases are implied here:

Case	Differences	r_0	r_1	r_2	r_3	r_4	r_5	Decimal	error
1	44	0	1	0	1	0	1	42	4.5%
2	26	1	1	0	1	1	0	27	3.8%
3	55	1	0	0	1	1	1	57	3.6%
4	29	0	0	1	1	1	0	28	3.4%
5	52	1	0	1	0	1	1	53	1.9%

Table 3 Result of simulation in several cases

By setting the length of the sample windows and the human's finger input capacitance value, we can easily get many cases for testing, and we compare the difference between two sample windows within in each case with the digital computation unit outputs to see the error.

As shown in Table 3, the error is a stable constant below to 5%, which can indicate that the performance of the system is steady and the decision of the digital computation unit is reliable. If we prolong the sampling window, the error will definitely decrease since the number of samplings example increases.

CHAPTER 5

Conclusion

5.1 Final Version of Layout

The core of all analog blocks is very compact and small, but considering future test, we need to plot out every stage for debugging. The digital parts have to carry at least 14-bits outputs. Besides, to avoid interference (noise) between analog and digital parts, the supply voltages (VDD/GND) of analog and digital parts need to be separated. So even if the analog and digital cores are very small, we still have to put huge amounts of pads for testing consideration. This may let the layout looks kind of waste, but after we make sure the functionality of the chip, many pads can be removed, at that time the layout might look good.

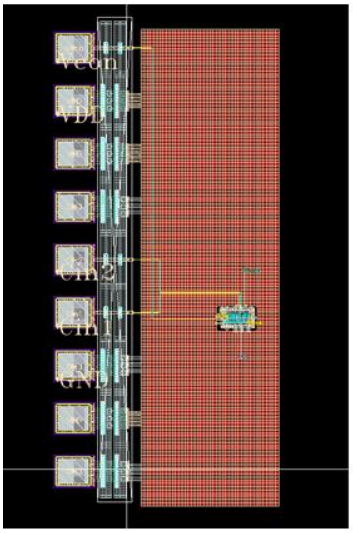

Figure 28 Layout of analog blocks combined with pads

Figure 28 shows the layout of all the analog blocks combined with the analog pads. There are not much inputs/outputs need to be plotted out in the analog parts, but to match up the numbers and sizes of the digital parts, so we still put 9 pads in analog layout. Within these 9 pads, 3 pads are used for VDD and 3 pads are used to provide stable AC ground. Using more than 1 pad to provide voltage supply can help the stable and convenience in connection. The rest 3 pads are differential antenna inputs and controlled voltage of the ring oscillator.

The size of the final analog parts layout with pads is 920um by 450um. The power dissipation is 1.07mW which is much smaller than the spec 4mW. The system can detect a very small capacitance change down to 20fF, which is 50 times smaller than the recent capacitive touch screen sensor system (1pF).

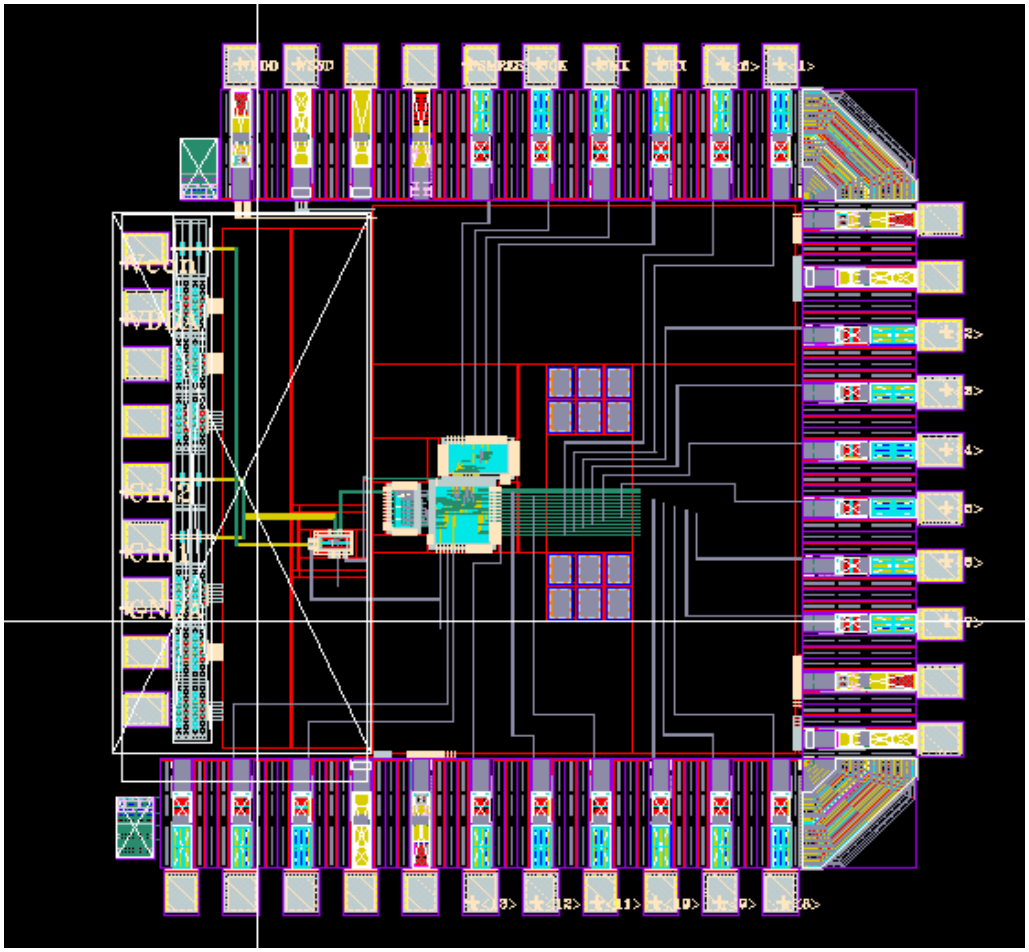

Figure 29 Layout of entire system

Figure 29 shows the layout of the entire system, including analog parts, digital parts and all pads. This is the layout of the integration of analog and digital blocks, and the size is 1mm by 1.2mm. And the power dissipation of the digital block is very small, around 200uW, so the power dissipation of the entire system is still no more than 1.3mW.

5.1 Spec comparison and Conclusion

	Existing touch screen	Air touch screen methodology in this thesis
Sensitivity of receiving capacitance	1pF	20fF

Table 4 Conclusion of spec

The total power of the system is 1.3mW, which is much smaller than the expected 4mW one. The sensitivity of the receiving capacitance is down to 20fF, compared with current capacitive touch screen technology (1pF), so the performance can be 50 times more sensitive. The system modulates the input capacitance difference into a higher frequency signal and deals with this signal, and now the frequency range of the modulated signal is from 0 to 3GHz, by tuning the controlled voltage of the ring oscillator, the system can avoid violation and interference with other devices easily. Since the ring oscillator can generate signals with oscillation frequency up to 5GHz, if the new structure is used in the digital counter and the speed of digital blocks can be improved, then the modulated frequency range can be wider, and the flexibility of this air touch sensor system can be increased too. The size now is 1mm by 1.2mm, but most of the area is reserved for future testing; once the functionally and performance is confirmed, most pads can be removed, reducing the area by 70 %.

References

[1] G. Barrett and R. Omote, "Projected-Capacitive Touch Technology," Information Display, Vol. 26, No. 3, March 2010, pp 16-21

[2] "IEEEGHN: The Theremin". IEEE. 2008. Retrieved 2008-10.22.

[3] Hajimiri, A. and Lee, T. H., "A general theory of phase noise in electrical oscillators," IEEE Journal of Solid-State Circuits, 1998.

[4] William Shing Tak Yan and Howard Cam, "A 900MHz CMOS Low-Phase-Noise Voltage-Controlled Ring oscillator," IEEE Trancitions on circuits and systems, 2001.

[5] B. Razavi, "Principles of data conversion system design"